Intel® 31244 PCI-X to Serial ATA Controller

Design Guide

April 2004

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Revision History

Date	Revision #	Description
April 2004	003	Removed Section 5.4.5, “Spread Spectrum Clocking” on page 35. Removed SSC pin in Table 2, “Terminology and Definition” on page 9. Updated SSCEN pin in Table 5, “Configuration Pin Descriptions” on page 20 and Table 30, “Terminations: Pull-up/Pull-down” on page 65. Removed Section 9.1, “Power Delivery for the Intel® 31244 PCI-X to Serial ATA Controller (TBD)” on page 59. In Appendix A, “Intel® IQ31244 Controller Evaluation Platform Board Bill of Materials”, replaced Bill of Materials table with a URL to the Intel® website.
December 2002	002	In Section 2.1, added a new table titled “Serial ROM Interface Pin Descriptions”. In Section 2.1, added note to Table 2, “Serial ATA Signal Pin Descriptions”, indicating that LED2 and LED3 as dual purpose pins. Replaced Figure 5, “PBGA Mapped by Pin Function” with a revised illustration. Added content to Section 3.4.1.1, “Intel GD31244 PCI-X to Serial ATA Controller Decoupling”, regarding the use of at least twelve 0.1 µF capacitors to decouple the VCC 2.5 V signal. Removed Section 3.4.1.2, “PCI-X Decoupling”. In Table 30, “Terminations: Pullup/Pulldown”, revised row with signal name of TRST# to include TDI#, TMS#, and TCK as 4.7K pull-ups. In Appendix A, revised the Bill of Materials.
October 2002	001	Initial release of this document.

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About This Document 1

1.1 Reference Documentation

For the latest revision and documentation number, contact your Intel representative.

Table 1. Reference Documents

Document	Intel Document Number or Source
Intel® Artisea PCI-X to Serial ATA Controller Developer's Manual	273603
Intel® Artisea PCI-X to Serial ATA Controller Datasheet	273595
Intel® Packaging Databook	240800
Printed Circuit Board (PCB)Test Methodology User's Guide, Revision 1.6	298179 http://developer.intel.com/design/chipsets/applnots/298179.htm
Terminating Differential Signals on PCBs, by Steve Kaufer and Kelee Crisafulli. Printed Circuit Design Magazine, March 1999	http://www.pcdmag.com

1.2 Terminology and Definitions

Table 2. Terminology and Definition (Sheet 1 of 3)

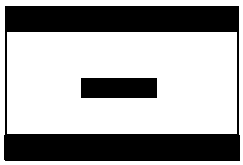
Term	Definition	
Stripline		Stripline in a PCB is composed of the conductor inserted in a dielectric with GND planes to the top and bottom. **NOTE:** An easy way to distinguish stripline from microstrip is that you need to strip away layers of the board to view the trace on stripline.
Microstrip		Microstrip in a PCB is composed of the conductor on the top layer above the dielectric with a ground plane below
Prepreg	Material used for the lamination process of manufacturing PCBs. It consists of a layer of epoxy material that is placed between two cores. This layer melts into epoxy when heated and forms around adjacent traces.	
Core	Material used for the lamination process of manufacturing PCBs. This material is two sided laminate with copper on each side. The core is an internal layer that is etched.	

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Table 2. Terminology and Definition (Sheet 2 of 3)

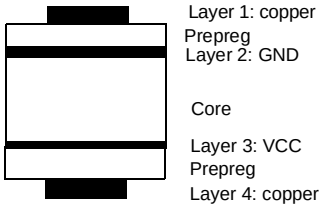
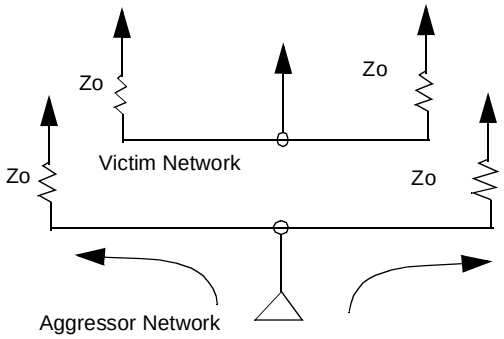
Term	Definition
PCB	 Example of a Four-Layer Stack Printed circuit board. Example manufacturing process consists of the following steps: • Consists of alternating layers of core and prepreg stacked • The finished PCB is heated and cured. • The via holes are drilled • Plating covers holes and outer surfaces • Etching removes unwanted copper • Board is tinned, coated with solder mask and silk screened
JEDEC	Provides standards for the semiconductor industry.
Aggressor	A network that transmits a coupled signal to another network is aggressor network. 
Victim	A network that receives a coupled cross-talk signal from another network is a called the victim network
Network	The trace of a PCB that completes an electrical connection between two or more components.
Stub	Branch from a trunk terminating at the pad of an agent.
CRB	Customer Reference Board
HBA	Host Bus Adapter
TX + / TX -	These signals are the outbound high-speed differential signals that are connected to the serial ATA cable.
RX + / RX -	These signals are the inbound high-speed differential signals that are connected to the serial ATA cable.
TX	This is a transmit port that contains the basic high-speed driver electronics.
RX	This is a receiver port contains the basic high-speed receiver electronics.
Termination calibration	This block is used to establish the impedance of the RX block in order to properly terminate the high-speed serial cable.
PLL	This block is used to synchronize an internal clocking reference so that the input high-speed data stream may be properly decoded.
Voltage Regulator	This block stabilizes the internal voltages used in the other blocks so that reliable operation may be achieved. This block may or may not be required for proper operation of the balance of the circuitry. The need for this block is implementation specific.
TxData	Serially encoded 10b data attached to the high-speed serial differential line driver.

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Table 2. Terminology and Definition (Sheet 3 of 3)

Term	Definition
RxData	Serially encoded 10b data attached to the high-speed serial differential line receiver.
10b encoding	The 8B/10B encoding scheme transmits eight bits as a 10-bit code group. This encoding is used with Gigabit Ethernet, Fibre Channel and InfiniBand*.
Jitter	Jitter is a high-frequency, semi-random displacement of a signal from its ideal location.
ISI	Inter-symbol interference. Data-dependent deterministic jitter caused by the time differences required for the signal to arrive at the receiver threshold when starting from different places in bit sequences (symbols). For example media attenuates the peak amplitude of the bit sequence [0,1,0,1...], more than it attenuates the peak amplitude of the bit sequence [0,0,0,0,1,1,1,1...], thus the time required to reach the receiver threshold with the [0,1,0,1...] sequence is less than required from the [0,0,0,0,1,1,1,1...] sequence. The run length of 4 produces a higher amplitude which takes more time to overcome when changing bit values and therefore produces a time difference compared to the run length of 1-bit sequence. When different run lengths are mixed in the same transmission the different bit sequences (symbols) therefore interfere with each other. ISI is expected whenever any bit sequence has frequency components that are propagated at different rates by the transmission media. This translates into high-high-frequency, data-dependent, jitter.
Differential Signal	A signal derived by taking the difference between two conductors. In this spec a differential signal is comprised of a positive conductor and a negative conductor. The differential signal is the voltage on the positive conductor minus the voltage on the negative conductor (i.e., TX+ – TX-).

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Overview 2

This document provides layout information and guidelines for designing platform or add-in board applications with the Intel® 31244 PCI-X to serial ATA controller (GD31244). It is recommended that this document be used as a guideline. Intel recommends employing best-known design practices with board-level simulation, signal integrity testing and validation for a robust design.

Designers should note that this guide focuses upon specific design considerations for the GD31244 and is not intended to be an all-inclusive list of all good design practices. It is recommended that this guide is used as a starting point and use empirical data to optimize your particular design.

Note: This pre-silicon analysis information is preliminary and subject to change. Sections marked with TBD are to be updated in future revisions.

2.1 Features

The GD31244 is a state-of-the-art, PCI-X to Serial ATA Controller with four Serial ATA ports running at 1.5 Gbits/s. The device is targeted at embedded applications such as PC motherboards, as well as standalone PCI-X Host Bus Adapter (HBA) cards and RAID controllers.

The GD31244 is both a PCI-X Bus Master and Slave, which automatically switches modes as required.

As a PCI-X Slave, the device supports:

- I/O Reads
- I/O Writes
- Memory Read Bus Cycles
- Configuration Read
- Configuration Write

As a PCI-X Bus Master, this device supports:

- Single Memory Reads
- Multiple Memory Reads
- Line Memory Reads
- Memory Writes

This device is compliant with a PCI-X bus operating at up to 64 bits at 133 MHz, resulting in burst data rates of 1064 Mbytes/s. The GD31244 provides four Serial ATA ports running at 1.5 Gbits/s transfer rate, which are compliant to the *Serial ATA: High speed Serialized AT Attachment Specification*, Revision 1.0e. The GD31244 derives its Serial ATA clocks from an internal PLL, with a reference clock of 37.5 MHz provided externally or from a crystal.

The GD31244 is fully compatible with parallel ATA operating system drivers and software. The chip may be configured in compatibility mode, mapping the PCI-X configuration space to match the x86 standard Primary and Secondary IDE ports. To support both on-board parallel IDE, plus the four Serial ATA ports, the chip may be configured for native PCI-X mode, allowing Plug-and-Play BIOS and operating systems to map the Serial ATA drives to non-conflicting task file and I/O address space. For higher performance in systems where compatibility is not required, all four channels may be configured as Direct Port Access (DPA).

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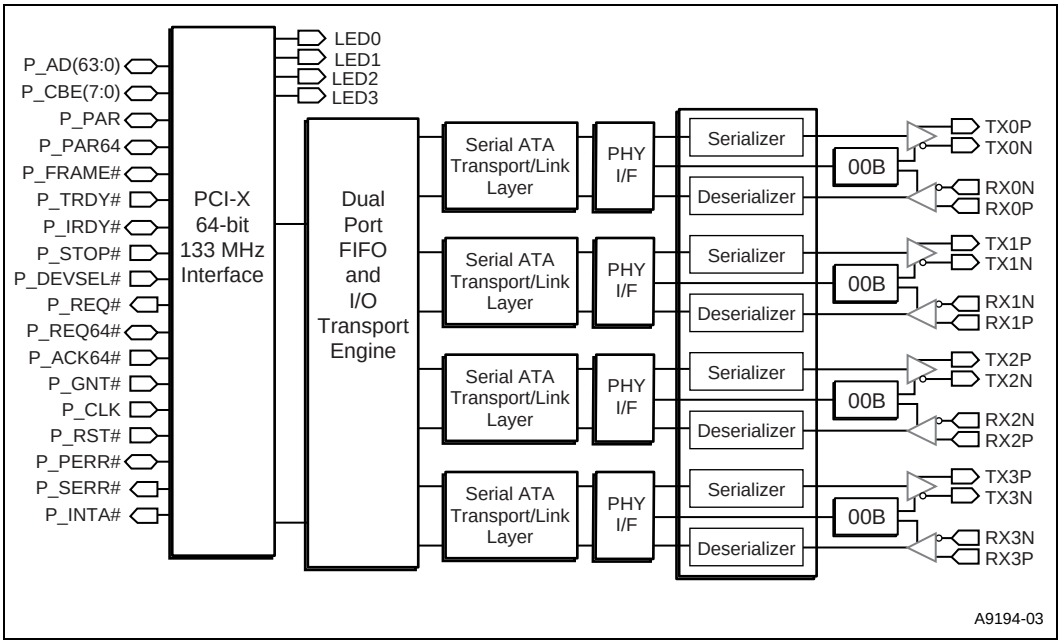
Feature Highlights:

- Four SATA Channels at 1.5 Gbits/s
- *Serial ATA: High speed Serialized AT Attachment Specification*, Revision 1.0e Compliant
- 64-bit/133 MHz PCI-X Bus. Backwards compatible to 32-bit/33 MHz and 64-bit/66 MHz
- Compatible with existing Operating Systems
- Supports native PCI IDE
- Hot-Plug Drives
- Supports Master/Slave Mode for Compatibility with existing Operating Systems
- Supports SATA Direct Port Access (Master/Master Mode)
- Independent DMA Masters for each SATA Channel
- 3.3 V and 2.5 V Supply, 2 W maximum

Figure 1. Intel® 31244 PCI-X to Serial ATA Controller Block Diagram



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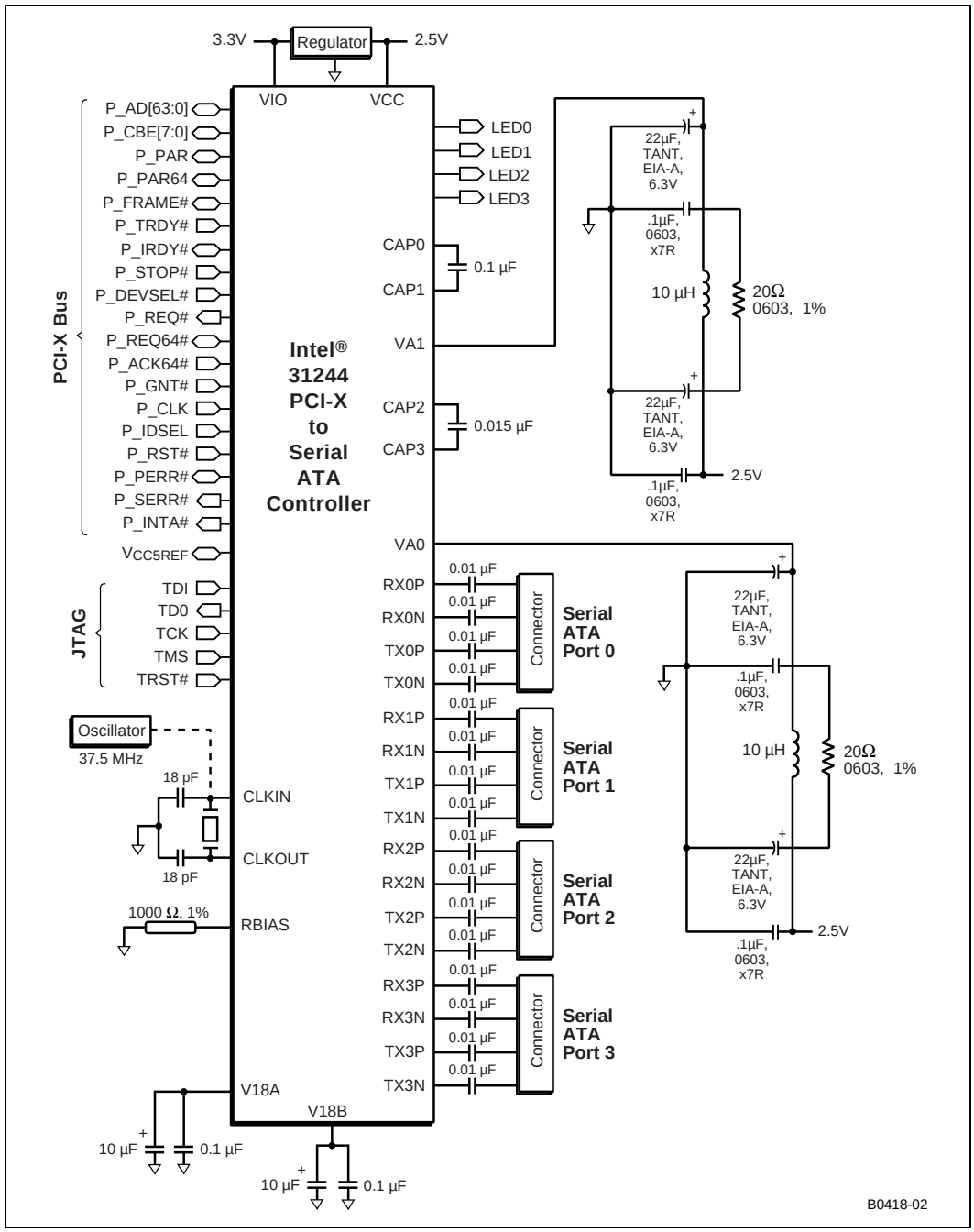
2.2 Applications

The GD31244 may be used to build a Serial ATA Host Bus Adapter which connects to the PCI-X bus. Control for external activity LEDs, a 37.5 MHz Crystal, a voltage regulator and some external resistors and capacitors are needed.

Figure 2. Quad Serial ATA Host Bus Adapter



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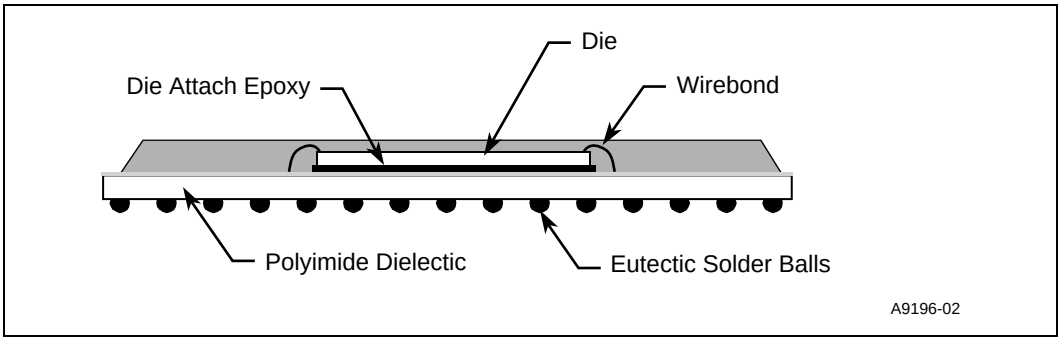
Intel® 31244 PCI-X to Serial ATA Controller Package 3

The GD31244 signals, are located on a 256-pin Plastic Ball Grid Array (PBGA) package to simplify signal routing and system implementation. For detailed signal descriptions refer to the *Intel® 31244 PCI-X to Serial ATA Controller Datasheet*. Contact your Intel sales representative to obtain a copy of this document. The construction of the packages is shown in Figure 3.

Figure 3. Packaging Considerations



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3.1 Signal Pin Descriptions

The signal pin descriptions for the GD31244 are provided as a reference. A complete list is also available in the *Intel® 31244 PCI-X to Serial ATA Controller Datasheet*.

Table 3. Serial ATA Signals Pin Descriptions

Name	Description
TX0P, TX0N, TX1P, TX1N, TX2P, TX2N, TX3P, TX3N	**OUTPUT - Differential High-Speed Outputs:** These are the differential serial outputs for each channel. When disabled, these outputs are driven to their DC-Bias point.
RX0P, RX0N, RX1P, RX1N, RX2P, RX2N, RX3P, RX3N	**INPUT - Differential High-Speed Inputs:** These are the differential serial inputs for each channel.
CLKOUT	**OUTPUT - LVTTL:** This is connected to one side of the 37.5 MHz crystal.
CLKIN	**INPUT - LVTTL:** This is the reference clock input for the clock multiplier unit at 37.5 MHz. It may be connected to either an external clock source or one side of a crystal.
CLKO	Buffered output of the 37.5 MHz clock.
RBIAS	**INPUT - ANALOG:** This pin is pull-down to ground with a 1000 Ω, 1% resistor in order to set the internal termination resistors to 1000 Ω.
CAP0, CAP1	**Analog:** An external 0.1 µF (+/- 10%) capacitor is connected between these pins to set the Clock Multiplier PLL loop filter response.
LED0, LED1, LED2†, LED3†	**OUTPUT - LVTTL:** These are the Activity LED outputs for channel 0, channel1, channel 2 and channel 3 (active LOW with 10 mA maximum sink capability).

† LED2 and LED3 are dual purpose pins. Refer to Table 7.

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Table 4. PCI-X Bus Pin Descriptions (Sheet 1 of 2)

Name	Description
CAP2, CAP3	**Analog:** An external 0.015 µF (+/- 10%) capacitor is connected between these pins to set the PCI PLL loop filter response.
P_ACK64#	**BIDIRECTIONAL - LVTTL:** Indicates that the device has positively decoded its address as the target of the current access and the target is willing to transfer data using the full 64-bit data bus.
P_AD[63:0]	**BIDIRECTIONAL - LVTTL PCI Address and Data:** The address and data lines are multiplexed on these pins. A bus transaction consists of an address phase followed by one or more data phases. P_AD[63:56] contains the most significant byte and P_AD[7:0] contain the least significant byte.
P_C/BE[7:0]#	**BIDIRECTIONAL - LVTTL:** Command and Byte Enable. The bus command and byte enable signals are multiplexed on these pins. During the address phase, the P_CBE# lines define the bus command. During the data phase, the P_CBE# lines are used as Byte Enables. The Byte Enables are valid for the entire data phase and determine which byte lanes carry meaningful data.
P_CLK	All PCI bus signals are referenced to this clock.
P_DEVSEL#	**BIDIRECTIONAL - LVTTL with Pull-Up Resistor:** Device Select. This signal is asserted by the target once it has detected its address. As a bus master, the P_DEVSEL# is an input signal to the Intel® 31244 PCI-X to serial ATA controller indicating whether any device on the bus has been selected. As a bus slave, the GD31244 asserts P_DEVSEL# to indicate that it has decoded its address as the target of the current transaction.
P_FRAME#	**BIDIRECTIONAL - LVTTL with Pull-Up Resistor:** Cycle Frame. This signal is driven by the current master to indicate the beginning and duration of a transaction. P_FRAME# is asserted to indicate the start of a transaction and de-asserted during the final data phase.
P_GNT#	**INPUT - LVTTL. Grant:** This signal is asserted by the bus arbiter and indicates to the GD31244 that access to the bus has been granted. This is a point-to-point signal and every master has its own GNT#.
P_IDSEL	**INPUT - LVTTL. Initialization Device Select:** This signal is used as a chip select during PCI-X configuration read and write transactions. This signal is provided by the host in PCI-X systems.
P_INTA#	**OUTPUT - Open Drain Interrupt A:** This signal is used to request an interrupt by the GD31244. This is an active low, level triggered interrupt signal.
P_IRDY#	**BIDIRECTIONAL - LVTTL with Pull-Up Resistor:** Initiator Ready. This signal indicates the bus master ability to complete the current data phase and is used in conjunction with the target ready (P_TRDY#) signal. A data phase is completed on any clock cycle where both P_IRDY# and P_TRDY# are asserted LOW.
P_PAR	**BIDIRECTIONAL - LVTTL:** Parity. Parity is even across P_AD[31:0] and P_CBE[3:0]# lines. It is stable and valid one clock after the address phase. For data phases, P_PAR is stable and valid one clock after either P_IRDY# is asserted on a write or P_TRDY# is asserted on a read.Once P_PAR is valid, it remains valid until one clock after the completion of the current data phase. The master drives P_PAR for address and write data phases; and the target, for read data phases.
P_PAR64	**BIDIRECTIONAL - LVTTL:** Parity for 64-bit Accesses. Parity is even across P_AD[63:0] and P_CBE[7:0]# lines. It is stable and valid one clock after the address phase. For data phases, P_PAR64 is stable and valid one clock after either P_IRDY# is asserted on a write or P_TRDY# is asserted on a read.Once P_PAR64 is valid, it remains valid until one clock after the completion of the current data phase. The master drives P_PAR64 for address and write data phases; and the target, for read data phases.
P_PERR#	**BIDIRECTIONAL - LVTTL with Pull-Up Resistor:** Parity Error. This signal is used to report data parity errors during all PCI-X transactions except a Special Cycle. This signal is asserted two clock cycles after the error was detected by the device receiving data. The minimum duration of P_PERR# is one clock for each data phase where an error is detected. A device cannot report a parity error until it has claimed the access by asserting P_DEVSEL# and completed a data phase.
P_REQ#	**OUTPUT - LVTTL. Request:** This signal indicates to the bus arbiter that the GD31244 desires use of the bus. This is a point-to-point signal and every bus master has its own P_REQ#.

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Table 4. PCI-X Bus Pin Descriptions (Sheet 2 of 2)

Name	Description
P_REQ64#	**BIDIRECTIONAL - LVTTL:** Indicates the attempt of a 64-bit transaction on the PCI bus. When the target is 64-bit capable, the target acknowledges the attempt with the assertion of P_ACK64#.
P_RST#	**INPUT - LVTTL Reset:** This signal is used to place PCI-X registers, sequencers, and signals into a consistent state. When P_RST# is asserted, all PCI-X output signals are tri-stated.
P_SERR#	**OUTPUT - Open Drain with Pull-Up Resistor:** System Error. This signal is used to report address parity errors. When an error is detected, P_SERR# is driven LOW for a single PCI-X clock.
P_STOP#	**BIDIRECTIONAL - LVTTL with Pull-Up Resistor:** Stop. This signal is driven by the target to indicate to the initiator that it wishes to stop the current transaction. As a bus slave, P_STOP# is driven by the GD31244 to inform the bus master to stop the current transaction. As a bus master, P_STOP# is received by the GD31244 to stop the current transaction.
P_TRDY#	**BIDIRECTIONAL - LVTTL with Pull-Up Resistor:** Target Ready. This signal indicates the selected device's ability to complete the current data phase and is used in conjunction with P_IRDY#. A data phase is completed on any clock cycle where both P_IRDY# and P_TRDY# are asserted LOW.
TEST0	I**NPUT - LVTTL:** Test input. Set LOW for normal operation.
TOUT	**OUTPUT -** Test pin. Do not use.

Table 5. Configuration Pin Descriptions

Name	Type	Description
32BITPCI#	INPUT	Pin number A2. This pin controls the state of the "64 bit device" status bit 16, in the PCI-X Status Register. When pulled down, reports a 0, a 32-bit bus. When pulled up, reports 1, a 64-bit device.
DPA_MODE#	INPUT	**INPUT - LVTTL:** When HIGH or open, selects Master/Slave Mode for software compatibility. When LOW, selects Master-Master mode for high performance.
SSCEN	INPUT	**Tie this pin to GND.**

Table 6. JTAG Pin Descriptions

Name	Description
TDO	**TEST DATA OUTPUT:** is the serial output pin for the JTAG feature. **TDO** is driven on the falling edge of **TCK** during the SHIFT-IR and SHIFT-DR states of the Test Access Port. At other times, **TDO** floats. The behavior of **TDO** is independent of **P_RST#**.
TDI	**TEST DATA INPUT:** is the serial input pin for the JTAG feature. TDI is sampled on the rising edge of **TCK**, during the SHIFT-IR and SHIFT-DR states of the Test Access Port. This signal has a weak internal pull-up to ensure proper operation when this signal is unconnected.
TCK	**TEST CLOCK:** is an input which provides the clocking function for the IEEE 1149.1 Boundary Scan Testing (JTAG). State information and data are clocked into the component on the rising edge and data is clocked out of the component on the falling edge.
TMS	**TEST MODE SELECT:** is an input sampled at the rising edge of **TCK** to select the operation of the test logic for IEEE 1149.1 Boundary Scan testing. This signal has a weak internal pull-up to ensure proper operation when this signal is unconnected.
TRST#	**TEST RESET:** an input that asynchronously resets the Test Access Port (TAP) controller function of IEEE 1149.1 Boundary Scan Testing (JTAG). This signal has a weak internal pull-up.

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Table 7. Serial ROM Interface Pin Descriptions

Name	Description
SDI	**INPUT - LVTTL with Pull Up:** Connects to the serial data output (SDO) of the Serial ROM. Customers are recommended to add pads for both a pull-up and a pull-down resistor for possible use in the future.
SDO (LED3)	**OUTPUT - LVTTL:** Connects to the serial data input (SDI) of the Serial ROM. This is also the activity LED output for Channel 3 when all four LEDs are activated (active LOW).
SCLK (LED2)	**OUTPUT - LVTTL:** Connects to the clock input (SCLK) of the serial ROM. This is also the activity LED output for Channel 2 when all four LEDs are activated (active LOW).
SCS#	**OUTPUT - LVTTL with Pull Up:** Connects to the chip select input (SCS#) of the Serial ROM.

Table 8. Power Supply Pin Descriptions

Name	Description
V18A, V18B	**OUTPUT:** This is the regulated 1.8 V supply generated internally. Bypass with 0.1 and 10 µF capacitors. V18A and V18B are each outputs of internal voltage regulators. They need to be separately bypassed to ground with 0.1 and 10 µF capacitors separately, they must not be connected together.
V_{CC5REF}	**Voltage Clamp I/O:** In 5 V tolerant systems, this is connected to a 5 V supply. In 3.3 V powered systems this is connected to 3.3 V. In PCI add-in cards, this is normally connected to I/O Power (10 A, 16 A, 19 B, 59 A and 59 B). The user must ensure that the value of V_{CC5REF} is high enough to ensure compliance to the $V_{IH(MAX)}$ specification on every input to the GD31244 not just PCI inputs. For example, when the Serial ROM device is 5 V I/O this pin must be 5 V regardless of the PCI bus.
VA0, VA1	**2.5 V Analog Power Supply:** Separate filtering is recommended. VA0 supplies the PCI PLL. VA1 supplies the CMU.
V_{SS}	Ground.
V_{CC}	2.5 V Digital Logic Power Supply.
V_{IO}	3.3 V PCI I/O Power Supply.
V_{CC0}, V_{CC1}, V_{CC2}, V_{CC3}	2.5 V High-Speed I/O Power Supply for each channel.

3.1.1 VA0, VA1 (V_{CCPLL}) Pin Requirements

To reduce clock skew, the VA0 and VA1 balls for the Phase Lock Loop (PLL) circuit are each isolated on the package. The lowpass filter, as shown in Figure 2, reduces noise induced clock jitter and its effects on timing relationships in system designs. The 22 µF bulk capacitors must be low ESR solid tantalum and the 0.1 µF ceramic capacitor must be of the type X7R. The node connecting VA0 and VA1, must be as short as possible.

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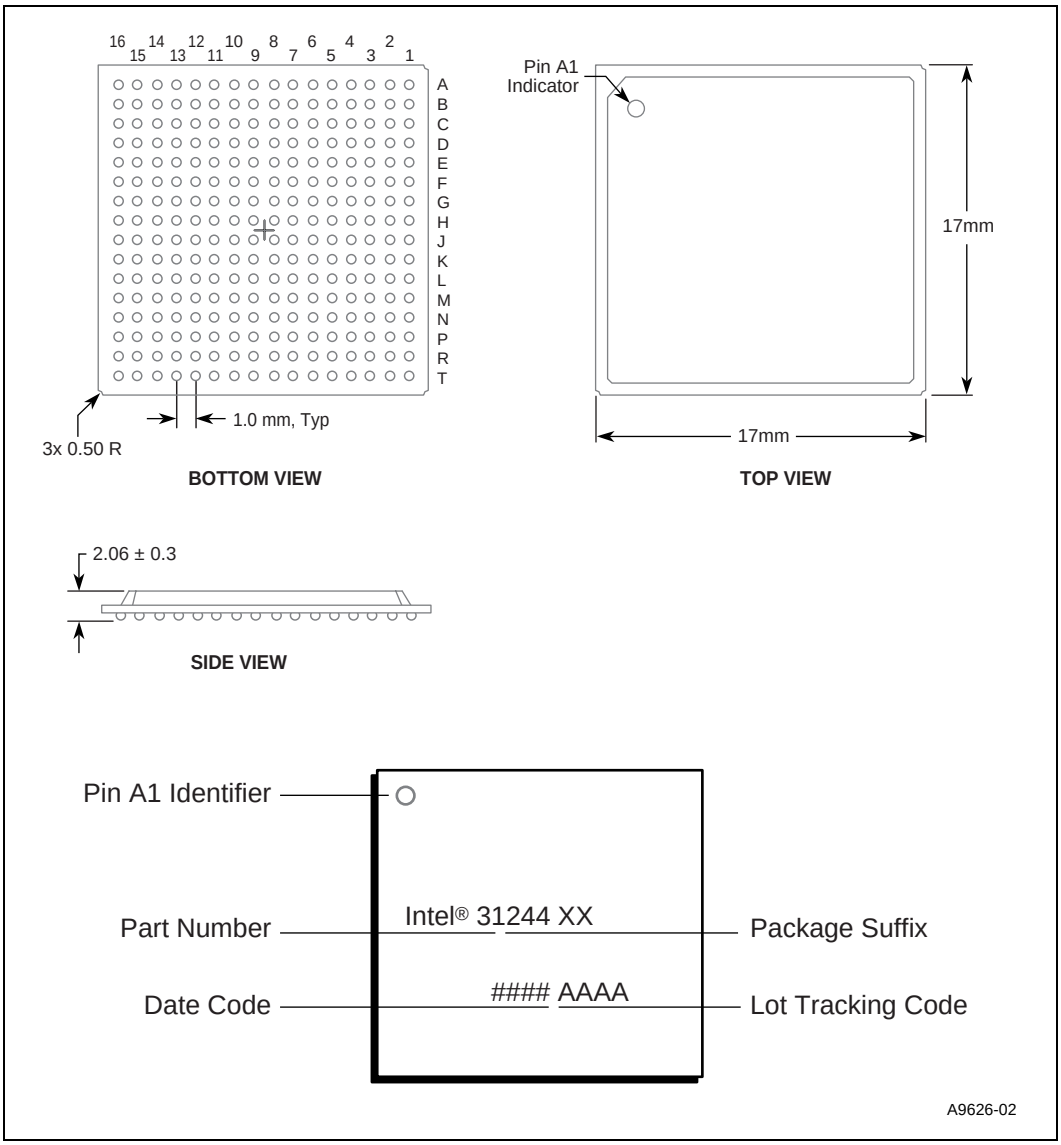
3.2 Package/Marking Information

The package is marked with three lines of text as shown in Figure 4. (The figure is not to scale.)

Figure 4. Package Information: 256-pin PBGA



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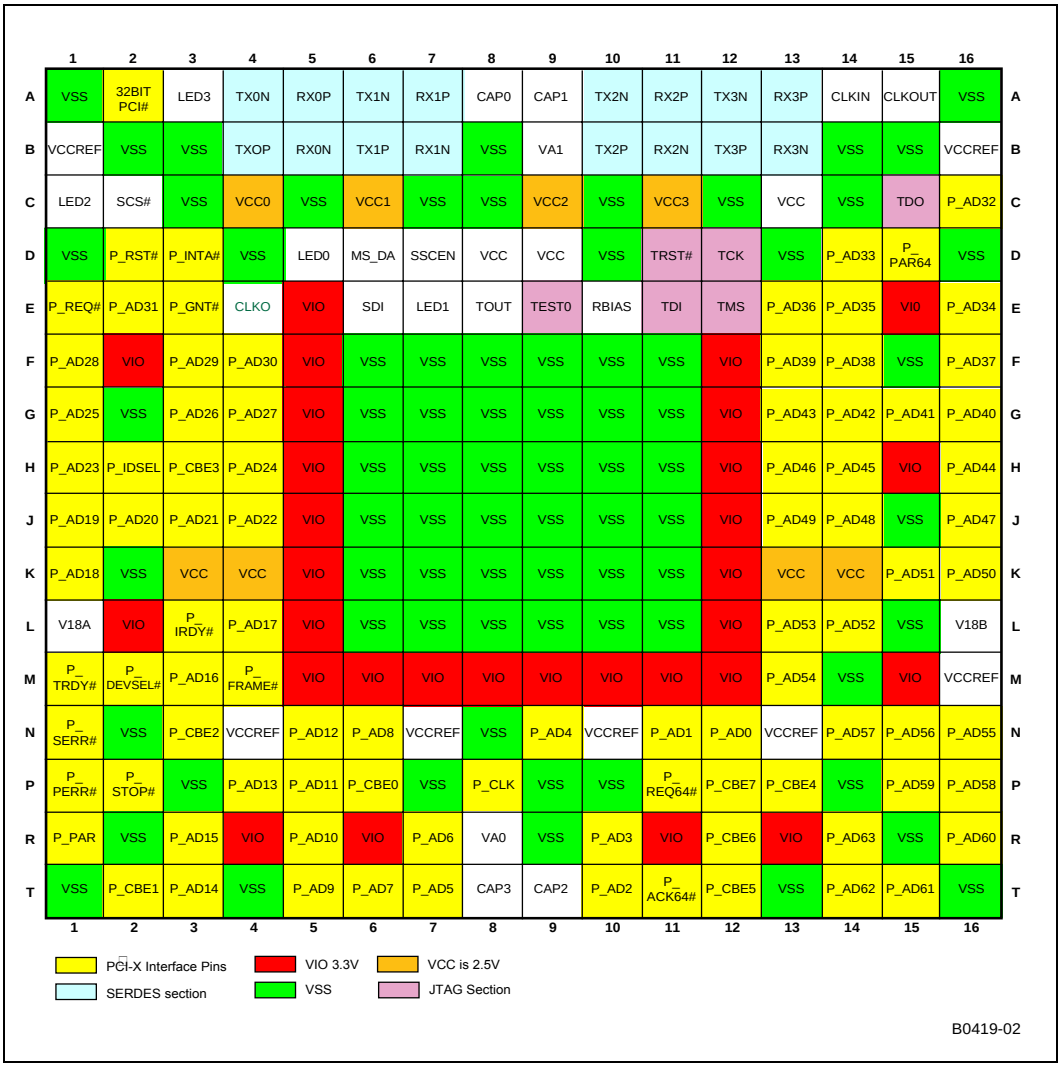
3.3 Ball Map By Function

Figure 5 shows the 544 BGA pins mapped by pin function. This diagram is helpful in placing components around the GD31244 for the layout of a PCB. To simplify routing and minimize the number of cross traces, keep this layout in mind when placing components on your board. Name signals, by design, are located on the PBGA package to simplify signal routing and system implementation.

Figure 5. PBGA Mapped By Pin Function



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Routing Guidelines 4

This chapter provides routing guidelines for layout and design of a printed circuit board using the GD31244. The high-speed clocking required when designing with the GD31244 requires special attention to signal integrity. In fact, it is highly recommended that the board design be simulated to determine optimum layout for signal integrity. The information in this chapter provides guidelines to aid the designer with board layout. Several factors influence the signal integrity of a GD31244 design. These factors include:

- power distribution
- decoupling
- minimizing crosstalk
- layout considerations when routing the SATA bus

4.1 General Routing Guidelines

This section details general routing guidelines for connecting the GD31244. The order in which signals are routed varies from designer to designer. Some designers prefer to route all clock signals first, while others prefer to route all high-speed bus signals first. Either order may be used, provided the guidelines listed here are followed.

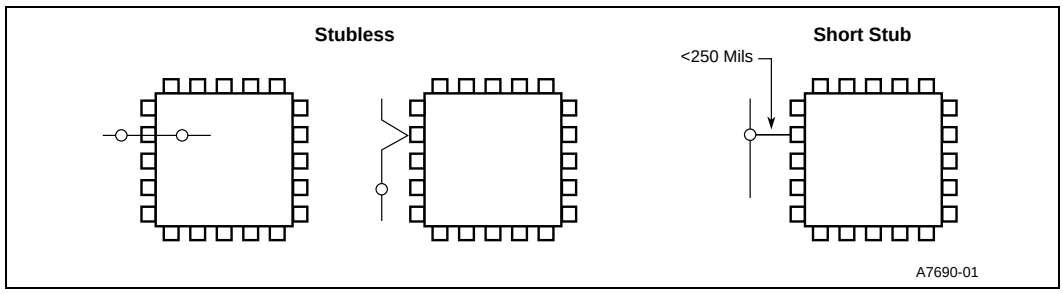
Route the GD31244 address/data and control signals using a daisy chain topology. This topology assumes that no stubs are used to connect any devices on the net. Figure 6, shows two possible techniques to achieve a stubless trace. When it is not possible to apply one of these two techniques due to congestion, a very short stub is allowed - do not exceed 250 mils.

Note: A rule of the thumb for stub trace length is to make sure that the stub length is less than or equal to the one-quarter of the signal transition.

Example:

- Nominal trace velocity To = 190 ps/in
- Typical signal slew rate = 2 V/ns
- Low-to-High Voltage differential (0.3 V_{CC} to 0.5 V_{CC}) =0.66 V
- Rise Time T_R =.66 V *(1 ns/2 V) = 330 ps
- Equivalent Distance = 330 ps/To = 1.74 in
- Stub length less than 1/4 of the length =0.44 in

Figure 6. Examples of Stubless and Short Stub Traces



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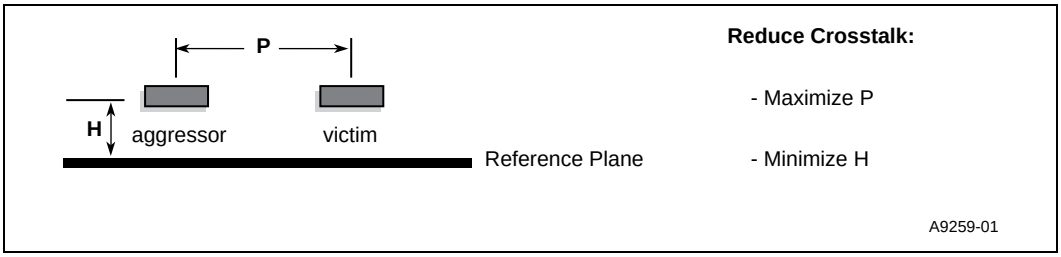
4.2 Crosstalk

Crosstalk is caused by capacitive and inductive coupling between signals. Crosstalk is composed of both backward and forward crosstalk components. Backward crosstalk creates an induced signal on victim network that propagates in the opposite direction of the aggressor signal. Forward crosstalk creates a signal that propagates in the same direction as the aggressor signal.

Circuit board analysis software is used to analyze your board layout for crosstalk problems. Examples of 2D analysis tools include Parasitic Parameters from **ANSOFT*** and XFS from **Quad Design***. Crosstalk problems occur when circuit etch lines run in parallel. When board analysis software is not available, the layout maintains minimum spacing between parallel circuit signals lines.

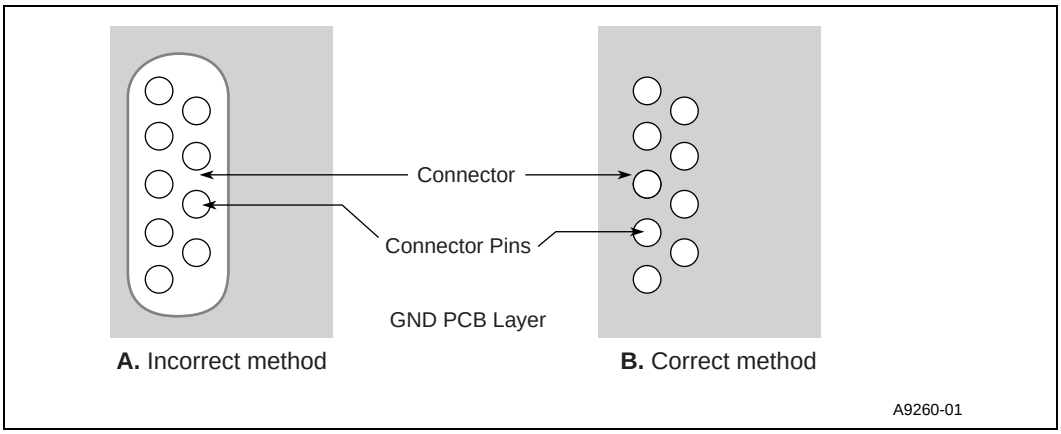
- A general guideline to use is, that space distance between adjacent signals be a least 3.3 times the distance from signal trace to the nearest return plane. The coupled noise between adjacent traces decreases by the square of the distance between the adjacent traces.
- It is also recommended to specify the height of the above reference plane when laying out traces and provide this parameter to the PCB manufacturer. By moving traces closer to the nearest reference plane, the coupled noise decreases by the square of the distance to the reference plane.

Figure 7. Crosstalk Effects on Trace Distance and Height



- Avoid slots in the ground plane. Slots increases mutual inductance thus increasing crosstalk.
- Make sure that ground plane surrounding connector pin fields are not completely cleared out. When this area is completely cleared out, around the connector pins, all the return current must flow together around the pin field increasing crosstalk. The preferred method of laying out a connector in the GND layer is shown in Figure 8B.

Figure 8. PCB Ground Layout Around Connectors



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4.3 EMI Considerations

It is highly recommended that good EMI design practices be followed when designing with the Intel® 31244 PCI-X to serial ATA controller.

- To minimize EMI on your PCB a useful technique is to not extend the power planes to the edge of the board.
- Another technique is to surround the perimeter of your PCB layers with a GND trace. This helps to shield the PCB with grounds minimizing radiation.

The below link may provide some useful general EMI guidelines considerations:

http://developer.intel.com/design/auto/mcs96/applnots/272673.htm

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4.4 Power Distribution and Decoupling

Have ample decoupling to ground, for the power planes, to minimize the effects of the switching currents. Three types of decoupling are: the bulk, the high-frequency ceramic, and the inter-plane capacitors.

- Bulk capacitance consist of electrolytic or tantalum capacitors. These capacitors supply large reservoirs of charge, but they are useful only at lower frequencies due to lead inductance effects. The bulk capacitors may be located anywhere on the board.
- For fast switching currents, high-frequency low-inductance capacitors are most effective. Place these capacitors as close to the device being decoupled as possible. This minimizes the parasitic resistance and inductance associated with board traces and vias.
- Use an inter-plane capacitor between power and ground planes to reduce the effective plane impedance at high frequencies. The general guideline for placing capacitors is to place high-frequency ceramic capacitors as close as possible to the module.

4.4.1 Decoupling

Inadequate high-frequency decoupling results in intermittent and unreliable behavior. A general guideline recommends that you use the largest easily available capacitor in the lowest inductance package.

4.4.1.1 Intel® 31244 PCI-X to Serial ATA Controller Decoupling

It is recommended that to decouple the VCC 2.5 V, use at least twelve 0.1 µF capacitors in as close proximity to the GD31244 VCC pins as possible. When feasible, locate these capacitors on the back of the board, close to the GD31244 VCC ball.

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4.5 Trace Impedance

All signal layers require controlled impedance of 50 Ω +/- 15%, microstrip or stripline where appropriate, unless otherwise specified. Selecting the appropriate board stack-up to minimize impedance variations is very important. When calculating flight times, it is important to consider the minimum and maximum trace impedance based on the switching neighboring traces. Use wider spaces between traces, since this may minimize trace-to-trace coupling, and reduce cross talk.

All recommendations described in this document assume a $\mathbf{T_{wid}}$ 5 mil 50 Ω signal trace, unless otherwise specified. When a different stack up is used the trace widths must be adjusted appropriately. When wider traces are used, the trace spacing must be adjusted accordingly (linearly).

It is highly recommended that a 2D Field Solver be used to design the high-speed traces. The following Impedance Calculator URLs provide approximations for the trace impedance of various topologies. They may be used to generate the starting point for a full 2D Field solver.

http://emclab.umr.edu/pcbtlc/

http://www.westak.com/techcenter/imped/

The following website link provides a useful basic guideline for calculating trace parameters:

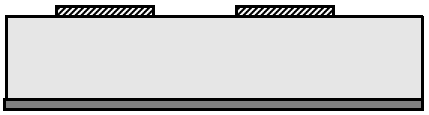
http://www.ultracad.com/calc.htm

Note: Using stripline transmission lines may give better results than microstrip. This is due to the difficulty of precisely controlling the dielectric constant of the solder mask, and the difficulty in limiting the plated thickness of microstrip conductors, which may substantially increase cross-talk.

4.5.1 Differential Impedance

The Serial ATA standard defines a 100 ohms differential impedance. This section provides some basic background information on the differential impedance calculations. In the cross section of Figure 9 shows the cross section of two traces of a differential pair.

Figure 9. Cross Section of Differential Trace



To calculate the coupled impedance requires a 2x2 matrix. The diagonal values in the matrix represent the impedance of the traces to ground and the off-diagonal values provide a measure of how tightly the traces are coupled. The differential impedance is the value of the line-to-line resistor terminator that optimally terminates pure differential signals. The two by two matrix is shown below as:

Example 1. Two-by-two Differential Impedance Matrix

$$Zo = \begin{bmatrix} Z11 & Z12 \\ Z21 & Z22 \end{bmatrix}$$

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For a symmetric trace Z11 = Z22, the differential impedance may be calculated from this equation:

$$Z_{differential} = 2(Z11-Z12)$$

For two traces to be symmetric, they must have the same width, thickness and height above the ground plane.[1] With the traces terminated with the appropriate differential, impedance ringing is minimized.

1. "Terminating Differential Signals on PCBs", Steve Kaufer and Kelee Crisafulli, Printed Circuit Design, March 1999

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Intel® 31244 PCI-X to Serial ATA Controller Interface Ports 5

5.1 Serial ROM Interface

In add-in card applications, firmware may be downloaded to the system from a Serial EEPROM or Serial Flash ROM, through the Serial ROM Interface. This industry standard, 4-pin interface, allows any size of device, up to 128 Kbytes, to be connected to the Intel® GD31244 PCI-X to serial ATA controller. This SPI interface was designed for compatibility with an ST Microelectronics* M25P10-A or Atmel* AT25F1024 device. Two of the pins are dual purpose to support four LED port activity indicators. This four pin interface is defined as follows:

1. **SDI INPUT:** Connects to the serial data output (SO) of the Serial EEPROM. Data is shifted out of the EEPROM on the falling edge of SCLK. Customers are recommended to add pads for both a pull-up and a pull-down resistor for possible use in the future.
2. **SDO OUTPUT:** Connects to the serial data input (SI) of the Serial EEPROM. Data is latched into the Serial EEPROM on the rising edge of SCLK. This is also the activity LED output for Channel 3 when all four LEDs are activated (active LOW).
3. **SCLK OUTPUT:** Connects to the clock input (SCK) of the Serial EEPROM. This is also the activity LED output for Channel 2 when all four LEDs are activated (active LOW).
4. **SCS# OUTPUT:** Connects to the chip select input (CS#) of the Serial EEPROM.

5.2 JTAG Interface

An IEEE 1149.1 compatible JTAG interface and boundary scan functionality is provided to assist on-board testing of the device. A BSDL test file is provided by Intel.

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5.3 PCI-X Interface

The 64-bit, 133 MHz PCI-X interface is fully compliant with the *PCI Local Bus Specification*, Revision 2.2 and the *PCI-X Addendum to the PCI Local Bus Specification*, Revision 1.0a. The PCI-X bus supports up to 1064 Mbytes/s transfer rate of burst data. The GD31244 is backwards compatible with 32-bit/33 MHz, 32-bit/66 MHz and 64-bit/66 MHz operation. The PCI logic supports Plug-n-Play operation, which allows hardware and firmware to resolve all setup conflicts for the user. The GD31244 supports both slave and master data transfers. The devices responds to the following bus cycles as a slave:

- I/O Reads
- I/O Writes
- Memory Read Bus Cycles
- Configuration Read
- Configuration Write

As a master, the GD31244 responds to:

- Single Memory Reads
- Multiple Memory Reads
- Line Memory Reads
- Memory Writes

During system initialization, the Configuration Manager of the host system reads the configuration space of each PCI-X device. After hardware reset, the GD31244 only responds to PCI-X Configuration cycles in anticipation of being initialized by the Configuration Manager. Each PCI-X device is addressable individually by the use of unique **IDSEL#** signals which, when asserted, indicate that a configuration read or write is occurring to this device. The Configuration Manager reads the setup registers of each device on the PCI-X bus and then, based on this information, assigns system resources to each supported function through Type 0 configuration reads and writes. Type 1 configuration cycles are ignored. This scheme allows the GD31244 and its external ROM to be relocated in the memory and I/O space. Interrupts, DMA Channels and other system resources may be reallocated appropriately.

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5.4 Serial ATA Interface

Four 1.5 Gbits/s Serial ATA ports are located on the GD31244, to support point-to-point connectivity to disk drives, CDROMs, DVD ROMs or any other Serial ATA target device. Each port is compliant with the "*Serial ATA: High speed Serialized AT Attachment Specification*, Revision 1.0e. High-speed differential duplex serial lines send 8B/10B encoded data to and from the GD31244 and the target at a maximum raw data rate of 1.2 Gbits/s (150 Mbytes/s). Copies of the targets Task File Registers are maintained on the GD31244 and transferred as needed to the target. The Serial ATA protocol is software compatible with all existing operating systems that support ATA devices, however, performance and reliability are improved since all data is CRC checked.

5.4.1 Direct Port Access (DPA)

The SATA Direct Port Access architecture allows for independent control of the SATA devices. Unlike ATA master/slave configuration where only one drive may operate at a time, DPA allows multiple drivers to be accessed concurrently. In addition, each port supports its own DMA channel allowing each port to transfer data independently (between a device and memory).

The DPA mode does change the register layout from PCI IDE. Therefore, legacy device drivers do not support this mode. DPA requires the registers (including the Command Block, Control Block, DMA, and SATA superset) for each drive is available at all times. Instead of using I/O space, these registers are mapped to a single 4 KB block. Each port has 512 KB; the remaining 2048 KB are for the common port registers. The 4 KB block is mapped using one PCI BAR register.

5.4.2 Extended Voltage Mode

The SATA voltages were designed primarily for a cable connection to the hard drives. In certain applications, such as NAS/SAN enclosures, the hard disk drives (HDD) are connected to a backplane, not a cable (typically in desktop systems). Due to the frequency of the SATA interface, the backplane creates a significant attenuation of the SATA signals. In an effort to simplify system designs, the GD31244 offers an extended voltage range to help alleviate this issue. This extended voltage range allows standard SATA HDD to be used with SATA backplanes.

The firmware may be place into the External Voltage Mode by setting bit 14 in PHY Configuration Register Address 140H to 1. This forces the firmware to operate with this extended voltage range.

Table 9. Normal Voltage Mode

Parameter	Description	Minimum	Maximum	Units
ΔV_{OUT}	TXx output differential peak-to-peak voltage swing	400	600	mVp-p
ΔV_{IN}	RXx input differential peak-to-peak voltage swing	325	600	mVp-p

Table 10. Extended Voltage Mode

Parameter	Description	Minimum	Maximum	Units
ΔV_{OUT}	TXx output differential peak-to-peak voltage swing	800	2000	mVp-p
ΔV_{IN}	RXx input differential peak-to-peak voltage swing	175	2000	mVp-p

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5.4.3 LED Interface

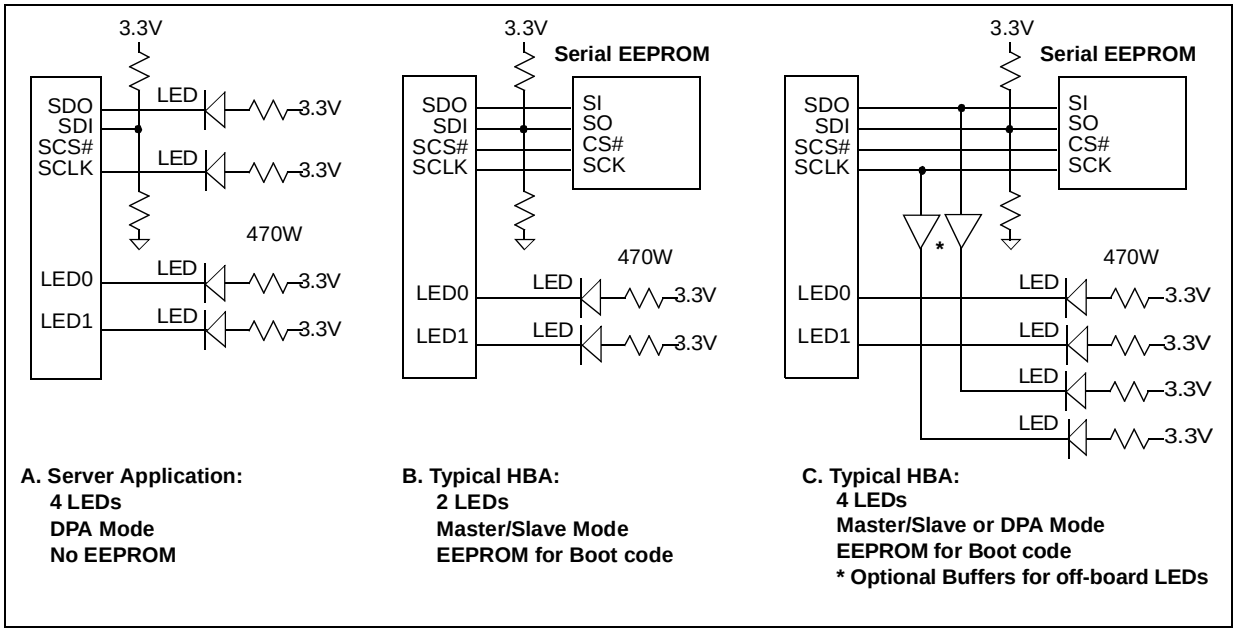
Serial ATA interfaces on disk drives do not include the traditional ATA output, which drives an LED to indicate that the drive is active. The GD31244 compensates for this missing function by adding four LED outputs, which sink 10 mA. In Master/Slave compatibility mode, LED0 goes LOW to turn on an Activity LED, anytime there is activity on either Channel 0 or Channel 1. Likewise, LED1 goes LOW to turn on an Activity LED, anytime there is activity on either Channel 2 or Channel 3. These two outputs may be wire-ORed together to use one LED for all four ports. During EEPROM transfers, the LED function on SCLK and SDO is suspended. A buffer may be required when the LEDs are located off-board and an EEPROM is used.

When GD31244 is configured in Direct Port Access mode (DPA_MODE# is LOW), then each port is assigned its own LED as follows:

- Port 0 on LED0
- Port 1 on LED1
- Port 2 on LED2
- Port 3 on LED3

During EEPROM transfers, the LED function on SCLK and SDO is suspended. A buffer may be required when the LEDs are located off-board and an EEPROM is used. Figure 10 shows a the common configurations of using the serial EEPROM in conjunction with the LEDs.

Figure 10. LED and Serial EEPROM Configurations



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5.4.4 Reference Clock Generation

A 37.5 MHz reference clock with a +/- 100 ppm accuracy is required for proper operation of the GD31244. This is generated from an external oscillator connected directly to the XI input. Optionally, a 37.5 MHz crystal may be connected between the XI and XO pins with a 20 pF capacitor from XI to ground and another from XO to ground. The following are the crystal characteristics:

- **Frequency:** 37.5 MHz +/- 100 ppm
- **Mode:** Fundamental
- **Type:** Parallel resonant
- **ESR:** 30 Ohms maximum
- **Load Capacitance:** 20 pF
- **Shunt Capacitance:** 7 pF
- **Drive Level:** 500 mW maximum
- **Recommended Vendor/Part Number:** Fox Electronics, Part number: 278-37.5-8 (This is an HC-49SD surface mountable package.)

Place the crystal near the GD31244 and isolated from noisy circuits as much as possible.

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Printed Circuit Board (PCB) Methodology 6

This section provides a recommended guidelines for PCB stackup. A considerable part of the SI analysis, is to identify and recommend the backplane stackup recommendations. This guideline section is separated into two recommendations:

- GD31244 in normal mode, refer to Table 9.
- GD31244 in extended voltage mode for backplane designs, refer to Table 10.

The specified impedance range for SATA is differential 100 ± 15% ohms for all components of the SATA path:

- backplane
- cables
- motherboard
- connectors

Table 11 defines the starting point for possible stackups.

The assumption is that GD31244 is implemented with normal 60 ohm guidelines, with the primary application being standard desktop PC.

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6.1 Intel® 31244 PCI-X to Serial ATA Controller Normal Mode (standard SATA driver)

This section provides recommendations for the GD31244 running in the standard SATA mode. Figure 11 shows a standard SATA setup with the GD31244 connected to trace on the motherboard. This trace terminates with a connector. The SATA cable connects to the SATA motherboard cable with the other end connecting to connector on the hard drive. The traces from the SATA hard drive connector connect to the SATA interface IC on the hard drive.

Figure 11. Intel® 31244 PCI-X to Serial ATA Controller Connection Scheme - Normal Mode

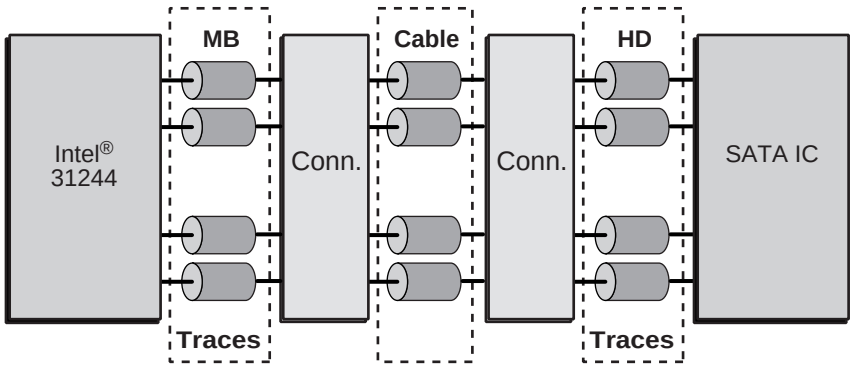

Table 11. Normal Voltage Mode

Parameter	Routing Guideline
Single Ended Trace Impedance	Microstrip stackup
Reference Plane	ground
Impedance	100 ohms differential impedance
Trace Thickness	1.4 mil
Trace Width	5 mil
Intra Pair Trace Spacing	7 mil
Pair to Pair Trace Spacing	20 mil minimum
Trace Length	2” to 5”
Trace Length Matching	100 mils
Cable Length	1 meter
Hard drive PCB Length from connector to SATA interface IC.	1”
Vias	Minimize number of vias (none preferred). Each channel in the pair has an equal number of vias.

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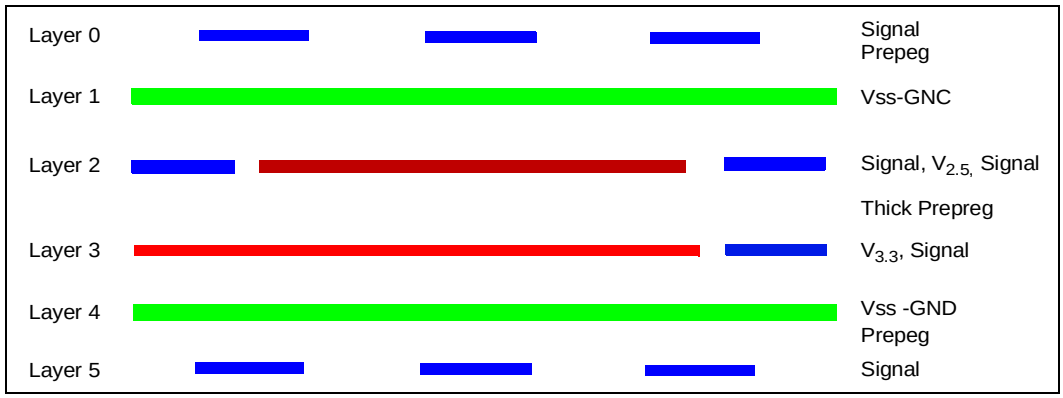
6.1.1 Intel® 31244 PCI-X to Serial ATA Controller HBA Stackup

The below stackup in Figure 12, shows the layer topology that is used in the HBA customer reference board. The first layer, Layer 0 is a signal layer, the second layer, Layer 1 is ground, the third layer, Layer 2 is 2.5 V plane with some traces, the fourth layer, Layer 3 is the 3.3 V plane with some traces, the fifth layer, Layer 4 is ground and the sixth layer Layer 5 may be used for additional signals.

Figure 12. Intel® 31244 PCI-X to Serial ATA Controller HBA Stackup



6.2 Extended Voltage Mode

This section details the recommendation for backplane applications with GD31244. The driver characteristics for this mode are listed in Table 10.

This Extended Voltage Mode was implemented because the as is, the SATA spec driver parameters are insufficient to drive a backplane interconnect. The ‘min’ driver has been modified, and this analysis assumes that the min driver meets this criteria:

Note: All changes have been made to GD31244 only. The SATA hard disk drive has been assumed to conform to the spec.

New ‘min’ corner driver specifications:

- 50 0mV peak-to-peak amplitude vs. 400 mV of spec
- Total jitter must be < 0.35 UI vs. 0.45 UI of spec (@DRV pin)
- Edge rate must be >= 0.3 UI vs. 0.41 UI of spec
- Everything not listed is same as SATA spec
- Attenuation scheme is used only for GD31244 write differential pairs TX lines not on RX lines.

The ‘min’ receiver has been modified, and this solution space is assuming the GD31244 receiver meets this criteria:

New ‘min’ corner receiver specifications:

- 220 mV peak-to-peak amplitude vs. 325 mV of specification

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- Jitter tolerance (TJ) must be >= 0.7 UI vs 0.62 UI of spec (@RCV pin)
- Slowest edge rate assumed
- Used only for GD31244 reads
- Read eye was guardbanded by 10 mV to allow for crosstalk

6.2.1 Backplane Topologies

This analysis looks at two backplane interconnection topologies. These two backplane topologies are divided into the two categories for the read RX lines and write TX lines. These are shown in the figures below. Figure 13a shows the GD31244 motherboard connecting through a connector to a backplane with resistor attenuation for write topologies. Figure 13b shows the GD31244 motherboard connecting through a ribbon cable to a backplane for write topologies with resistor attenuation. The resistor termination for Figure 13 is R1/R2 = 15 ohms/150 ohms 5% resistors provided 50 ohm impedance.

The Figure 14a shows the read topology from the SATA hard drive to a connector to through the backplane connector to the motherboard connecting to the GD31244 RX differential pins. In Figure 14b shows the read topology from the SATA hard drive to a connector to through the backplane connector through a ribbon cable to a motherboard connecting to the GD31244 RX differential pins. Note that reads do not have the extra resistor termination.

This section provides an example target system topology for designing a GD31244-based Serial ATA system. The target system implementation is based on one or more GD31244 chips mounted on the mother board and a backplane supporting 4 to 16 hot-plug SATA drives.

In the proposed example topology covered in this section the backplane is configured mechanically for either 3.5” x 1.0” or 2.5”x 0.75” form factor drives.

Figure 13. Write Backplane Topology

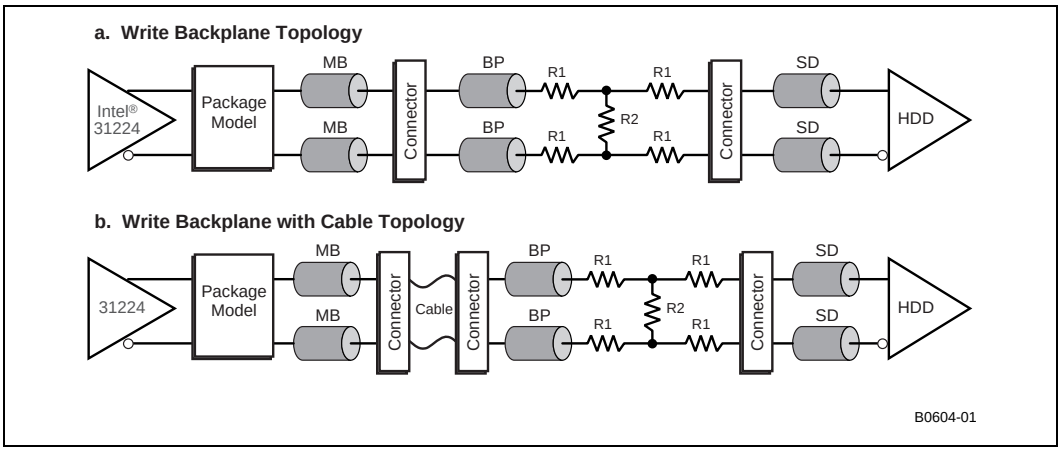

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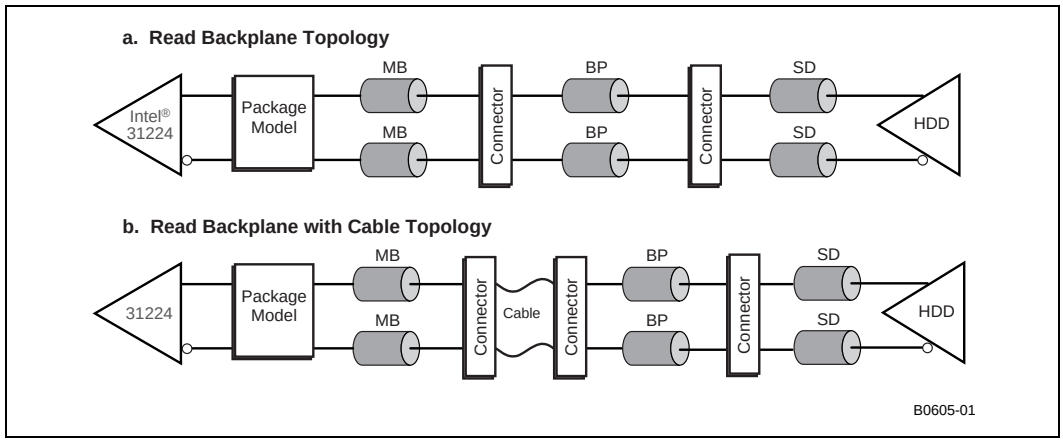
Figure 14. Read Backplane Topology



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6.2.2 Motherboard Stackup for Backplane Designs

The motherboard is supporting components in addition to GD31244, so an assumption is, desktop PC requirements are dominate to assure the processor and memory subsystem may be implemented with normal 60 ohm guidelines.

Table 12. Motherboard Stackup, Microstrip

Variable	Nominal (mil)	Tolerance	Min (mil)	Max (mil)
Mask Thickness	0.8	+/- 0.2	0.6	1.0
Mask Er	3.6		3.6	3.6
Trace Height	4.0	+/- 0.3	3.7	4.3
Preg Er	4.15	+/- 0.55	3.6	4.7
Plane Thickness	1.4	+/- 0.2	1.2	1.6
Trace Thickness	1.4	+/- 0.4	1.0	1.8
Trace Width	5 mil	+/- 1.5	3.5	6.5
Total Thickness	62.0	+/- 6.0	56.0	68.0

Table 13. Motherboard Microstrip Parameters

Parameter	Routing Guideline	Notes
Motherboard Layout	Microstrip	
Single Ended Trace Impedance	55 +/- 12%	
Differential Trace Impedance	100 ohms +/- 15%	
Reference Plane	ground	
Trace Thickness	1.4 mil	
Trace Width	5 mil	
Intra Pair Trace Spacing	15 mil	intra-pair to pair center-to-center
Pair-to-Pair Trace Spacing	55 mil	pair to pair center-to-center
Trace Length	2” to 6”	
Trace Length Matching	10 mil	Intra-pair matching
Vias	0	Minimize number of vias (none preferred). Each channel in the pair has an equal number of vias.

When possible, it is recommended that the designer use stripline for the following reasons:

- Reduced skin effect relative to microstrip
- Reduced forward cross talk
- Reduced jitter through differential stackup and isolated power delivery

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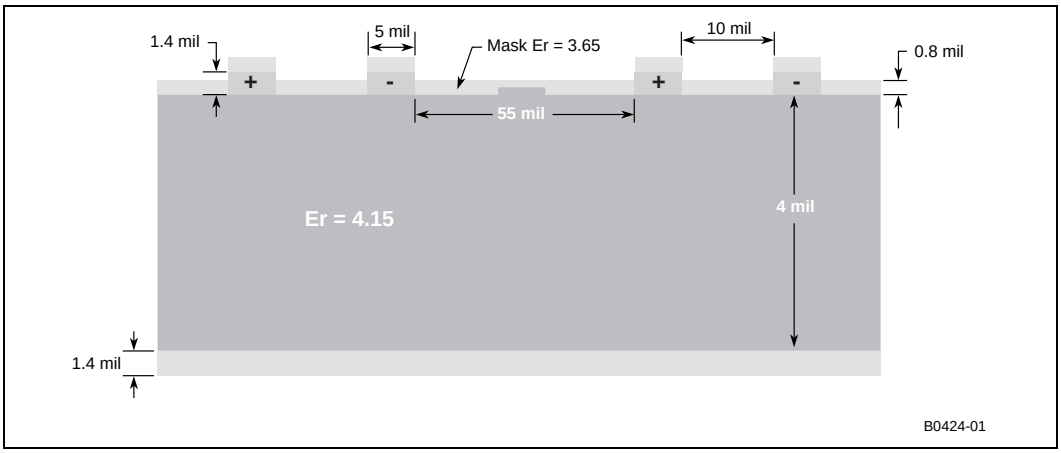
Figure 15. Microstrip Stackup



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6.2.3 Backplane Stripline Stackup

Figure 16 provides an example stackup that may be used to implement the backplane design. The stripline shown in Figure 16 is implemented with ground flood on both component and solder side of the PCB. The differential stripline traces are etched from the power and ground planes. Note that this information is preliminary.

Table 14. Backplane Stripline Stackup

Parameter	Routing Guideline	Notes
Single Ended Trace Impedance	60 +/- 14% ohms	
Differential impedance	100 +/- 15%	
Reference Plane	ground	
Trace Thickness	1.4 mil	
Trace Width	11.5 mil	
Intra Pair Trace Spacing	29.7 mil	intra-pair center-to-center (broadside coupled)
Pair to Pair Trace Spacing	60 mil	pair-to-pair, center-to-center for two adjacent differential pairs
Trace Length	2” to 14”	
Trace Length Matching	10 mils	intra-pair matching
R1	15 +/- 5% ohms	Required only for the write topology shown in Figure 13.
R2	150 +/- 5% ohms	Required only for the write topology shown in Figure 13.

Figure 16. Stripline Stackup

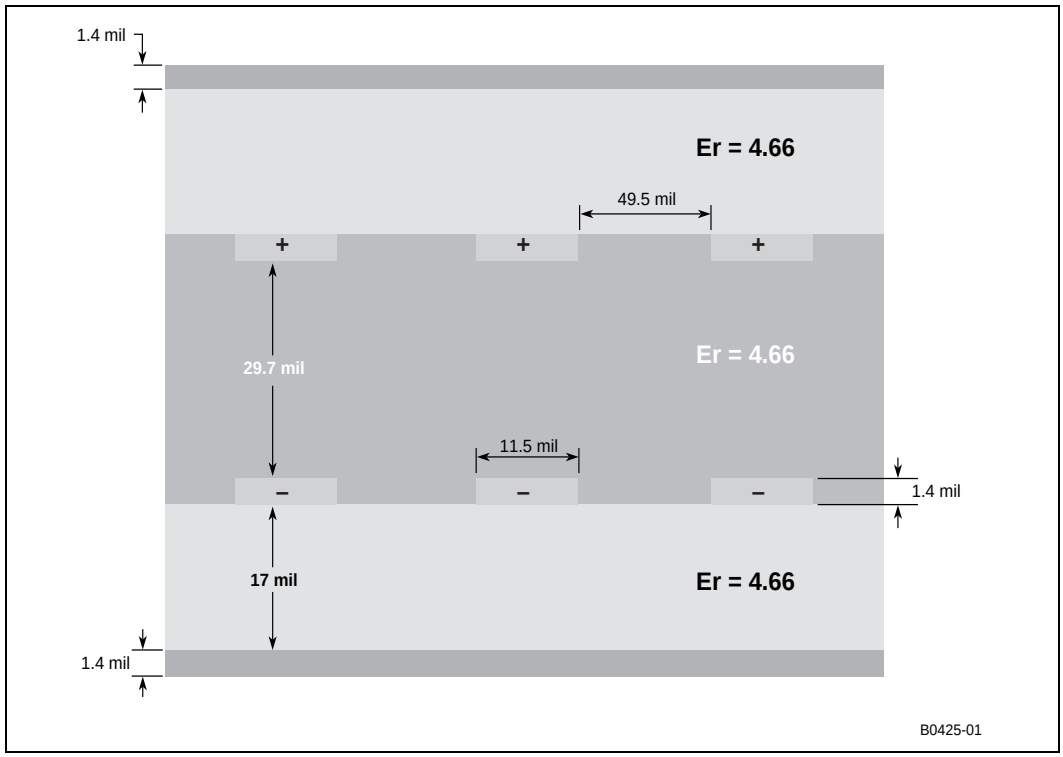

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Table 15. Backplane Stackup, Microstrip

Variable	Nominal (mil)	Tolerance	Min (mil)	Max (mil)
Mask Thickness	0.8	+/- 0.2	0.6	1.0
Mask Er	3.6		3.6	3.6
Trace Height	1.4	+/-0.3	1.1	1.7
Preg Er	4.66	+/-0.55	3.6	4.7
Plane Thickness	1.4	+/-0.2	1.2	1.6
Trace Thickness	1.4	+/-0.4	1.0	1.8
Trace Width	11.5	+/-1.5	10	13
Total Thickness	70.0	+/-7.0	63.0	77.0

Table 16. Backplane Stackup, Offset Stripline

Variable	Nominal (mil)	Tolerance	Min (mil)	Max (mil)
Mask Thickness	0.8	+/- 0.2	0.6	1.0
Mask Er	3.6		3.6	3.6
Trace Height	[1]	+/-0.3		
Preg Er	4.15	+/-0.55	3.6	4.7
Plane Thickness	2.2	+/-0.2	1.2	1.6
Trace Thickness	1.4	+/-0.4	1.8	2.6
Trace Width	11.5	+/-1.5		
Total Thickness	70.0	+/-7.0	63.0	77.0

6.2.4 Cable Interconnect With Backplane

Figure 14 provides the topology which uses a cable as an interconnect between the motherboard and backplane.

Table 17. Cable Specification

Parameter	Routing Guideline	Notes
Characteristic Z - Cable	100 ohms +/- 15%	
Trace Length	1”-6”	
Trace Matching	150 mils	

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PCI-X Layout Guidelines 7

This section provides guidelines for designing with the Intel® 31244 PCI-X to serial ATA controller PCI/PCI-X (PCI/X) bus interface in your application. This chapter is divided as follows:

- PCI/X voltage levels
- clocking modes
- general layout guidelines
- layout guidelines for the different slot configurations using PCI-X

7.1 PCI Voltage Levels

The Intel® 31244 PCI-X to serial ATA controller does not support a 5 V PCI signaling interface, it supports 3.3 V only. Supporting a 5 V PCI interface requires additional I/O level translation circuitry. Table 18 is provided as a reference for the PCI/X signaling levels. A complete *PCI-X Addendum to the PCI Local Bus Specification*, Revision 1.0a may be found on the www.pcisig.com website.

Table 18. PCI/X Voltage Levels

Symbol	Parameter	Minimum	Maximum	Units
V_{IL3}	Input Low Voltage (PCI-X)	-0.5	0.35 V_{CC33}	Voltage
V_{IH3}	Input High Voltage (PCI-X/PCI)	0.5 V_{CC33}	V_{CC33} + 0.5 V	Voltage
V_{IL4}	Input Low Voltage (PCI)	-0.5	0.3 V_{CC33}	Voltage
V_{OL3}	Output Low Voltage (PCI-X)		0.1 V_{CC33}	Voltage
V_{OH3}	Output HIGH Voltage (PCI-X)	0.9 V_{CC33}		Voltage

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7.2 PCI/X Clocking Modes

The Intel® 31244 PCI-X to serial ATA controller clocking modes for PCI-X and PCI bus are shown in Table 19. At PCI bus reset, the Intel® 80321 I/O processor samples the **P_FRAME#, P_IRDY#, P_TRDY#, P_STOP#**, and **P_DEVSEL#** to determine the operating frequency for PCI-X mode. When **P_FRAME#** is deasserted and **P_IRDY#** is deasserted (i.e., the bus is idle) and one or more of **P_DEVSEL#**, **P_STOP#**, and **P_TRDY#** are asserted at the rising edge of **P_RST#**, the device enters PCI-X mode (see Table 19). Otherwise, the device enters conventional PCI mode. With conventional PCI mode, a low on **M66EN** determines the PCI bus is at 66 MHz.

Table 19. PCI-X Clocking Modes

Mode/CLK	PCI/XCAP	M66EN	P_DEVSEL#	P_STOP#	P_TRDY#
PCI 33 MHz	GND	Deasserted	Deasserted	Deasserted	Deasserted
PCI 66 MHz	GND	Asserted	Deasserted	Deasserted	Deasserted
PCI-X 66 MHz	10 KΩ 0.01 µF cap to GND	N/A	Deasserted	Deasserted	Asserted
PCI-X 100 MHz	0.01 µF cap to GND	N/A	Deasserted	Asserted	Deasserted
PCI-X 133 MHz	0.01 µF cap to GND	N/A	Deasserted	Asserted	Asserted

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7.3 PCI General Layout Guidelines

For acceptable signal integrity with bus speeds up to 133 MHz it is important to PCB design layout have controlled impedance.

- Signal traces have an unloaded impedance of 60 +/- 10% Ω.
- Signal trace velocity is roughly 150 – 190 ps/inch

The below list provides general guidelines used when routing your PCI bus signals:

- Avoid routing signals > 8”.
- All clock nets must be on the top layer.
- All 32-bit interface signals from the PCI edge fingers must be no longer than 1.5” and no shorter than 0.75”.
- All 64-bit extension signal from the PCI edge fingers must be no longer than 2.75” and no shorter than 1.75”.
- CLK from the PCI edge finger must be 2.5” +/- 0.1”.
- **P_RST#** from the PCI edge finger must be no longer than 3.0” and no shorter than 0.75”.
- The following signals have no length restrictions: INTA#, INTB#, INTC#, INTD#, **TCK**, **TDI**, **TDO**, **TMS** and **TRST#**

Table 20 provides information on maximum lengths for routing add-on card signals.

Table 20. Add-on Card Routing Parameters

Parameter	PCI-X	
	Minimum	Maximum
CLK	2.4	2.6
P_AD[0 – 31]	0.75	1.5
P_AD[32 – 63]	1.75	2.75
P_RST#	0.75	3.0

Do not use more than one via for the primary PCI bus signals.

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7.4 PCI-X Layout Guidelines For Slot Configurations

The *PCI-X Addendum to the PCI Local Bus Specification*, Revision 1.0a recommends the following guidelines for the number of loads for your PCI-X designs. Any deviation from these maximum values requires close attention to layout with regard to loading and trace lengths.

Table 21. PCI-X Slot Guidelines

Frequency	Maximum Loads	Maximum Number of Slots
66 MHz	8	4
100 MHz	4	2
133 MHz	2	1

The following PCI-X design layout considerations were compiled from the white paper *Design, Modeling and Simulation Methodology for High Frequency PCI-X Subsystems* available on the http://www.pcisig.com website.

The following results were compiled from the simulation of system models that included system board and add-in cards for different slot configurations and bus speeds. This simulation addressed the signal integrity issues including:

- reflective noise
- cross-talk noise
- overshoot/undershoot voltage
- ring-back voltage
- settling time
- inter-symbol interference
- input reference voltage offset
- ground bounce effects

All these results met the required PCI-X timing characteristics and were within appropriate noise margins.

7.4.1 Protection Circuitry for Add-in Cards

Add-in cards designed for 3.3 V may still need to provide protection circuitry on the interrupt lines to prevent damaging the GD31244. This is important in the case where the GD31244-based add-in card (biased to 3.3 V), may potentially plug into a motherboard that has its interrupt lines (**INTA#**) tied to 5 V. To prevent potential damage, it is recommended that Schottky diodes be added to protect the GD31244 input buffer. The anode is connected to the INTA# pin and the cathode is connected to 3.3 V. Schottky diodes are used because of the 0.3 V forward bias voltage.

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7.4.2 PCI Clock Layout Guidelines

The *PCI-X Addendum to the PCI Local Bus Specification*, Revision 1.0a, allows a maximum of 0.5 ns clock skew timing for each of the PCI-X frequencies: 66 MHz, 100 MHz and 133 MHz. A typical PCI-X application may require separate clock point-to-point connections, distributed to each PCI device. Using a low skew clock buffer helps to meet the maximum clock skew requirements. The clock buffer also provides clock fanout to multiple PCI-X devices. The recommended clock buffer layouts are specified as follows:

- Match each of the PCI clock buffers lengths to within 0.1” to help keep the timing within the 0.5 ns maximum budget.
- Use a skew-limited clock buffer with a tight output-to-output skew specification.
- Keep the distance between the clock lines and other signals at least 25 mils from each other.
- Keep the distance between the clock line and itself at a minimum of 25 mils apart (for serpentine clock layout).

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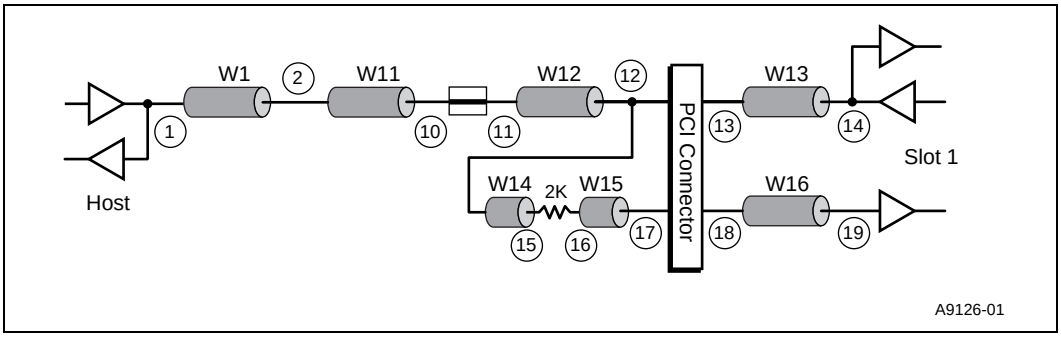
7.4.3 Connecting Intel® 31244 PCI-X to Serial ATA Controller to Single-Slot

Figure 17 shows one of the chipset PCI AD lines connected through W1 and W12 line segments, to a single-slot connector through W13 line segment, to the GD31244. This AD line is also used as an IDSEL line from line segment W14 to a 2K resistor through W15 to the PCI connector. The other end of the PCI connector IDSEL line connects through W16 to GD31244 IDSEL line input buffer. Table 22 shows the wiring lengths for a single slot design. This design layout wiring lengths should support PCI-X speeds. However, prelayout simulation is recommended.

Figure 17. Single-Slot Topology



- Stublengths are represented by W#s

Table 22. Wiring Lengths for Single Slot

Segment	Lower AD Bus		Upper AD Bus		Units
	Minimum Length	Maximum Length	Minimum Length	Maximum Length	
W1	2.0	8	2	7	inches
W12	0.1	0.5	0.1	0.5	inches
W13	0.75	1.5	1.75	2.75	inches
W14	0.1	Note	N/A	N/A	inches
W15	Note	0.6	N/A	N/A	inches
W16	1.125	1.125	N/A	N/A	inches

Note: W14, W15 and W16 represent the IDSEL line. W14 and W15 <= 0.8".

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7.4.4 Embedded Intel® 31244 PCI-X to Serial ATA Controller Single PCI-X Load

Figure 18 shows GD31244 as the PCI-X agent in a standalone embedded application (with no PCI-X slot). This figure shows one of the chipset PCI AD lines connected through W1 to the Intel® 31244 PCI-X to Serial ATA Controller. This AD line is also used as an IDSEL line from line segment W2 to a 2 K resistor through W3 to the GD31244 IDSEL line input buffer. Table 23 shows the corresponding wiring rules. These recommended wire lengths should support all PCI-X frequencies. However, prelayout simulation is recommended.

Figure 18. Embedded Intel® 31244 PCI-X to Serial ATA Controller Design with Single PCI-X Load

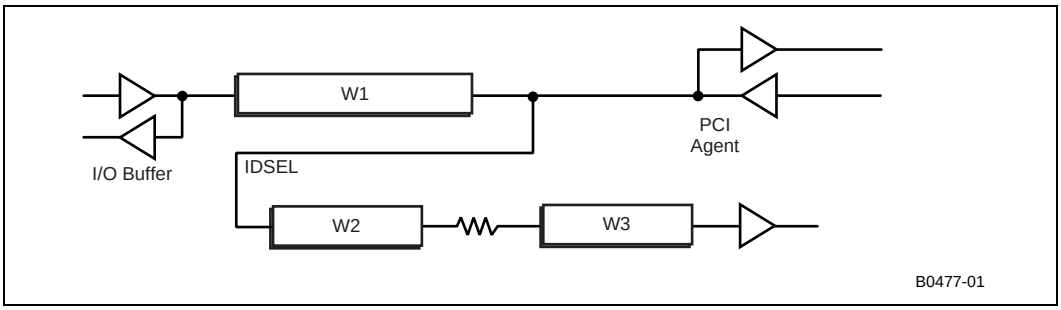

Table 23. Wiring Lengths for Embedded Intel® 31244 PCI-X to Serial ATA Controller with Single PCI-X Load

Segment	Lower AD Bus		Upper AD Bus		Units
	Minimum Length	Maximum Length	Minimum Length	Maximum Length	
W1	2.85	10	3.85	10.25	inches
W2	0.1	0.2	N/A	N/A	inches
W3	1.125	1.725	N/A	N/A	inches

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7.4.5 Embedded Intel® 31244 PCI-X to Serial ATA Controller Design With Multiple PCI-X Loads

Figure 19 shows GD31244 as the PCI-X agent 1 in a standalone embedded application (with no PCI-X slot) with other PCI-X devices shown as agent 2 and agent 3. This figure shows one of the chipset PCI AD lines connected through W1 to the Intel® 31244 PCI-X to Serial ATA Controller. This AD line is also used as an IDSEL line from line segment W2 to a 2K resistor through W3 to the GD31244 IDSEL line input buffer. Table 24 shows the corresponding wiring rules. These recommended wire lengths should support PCI-X frequencies of up to 100 MHz. However, prelayout simulation is recommended.

Figure 19. Embedded PCI-X Design With Multiple Loads

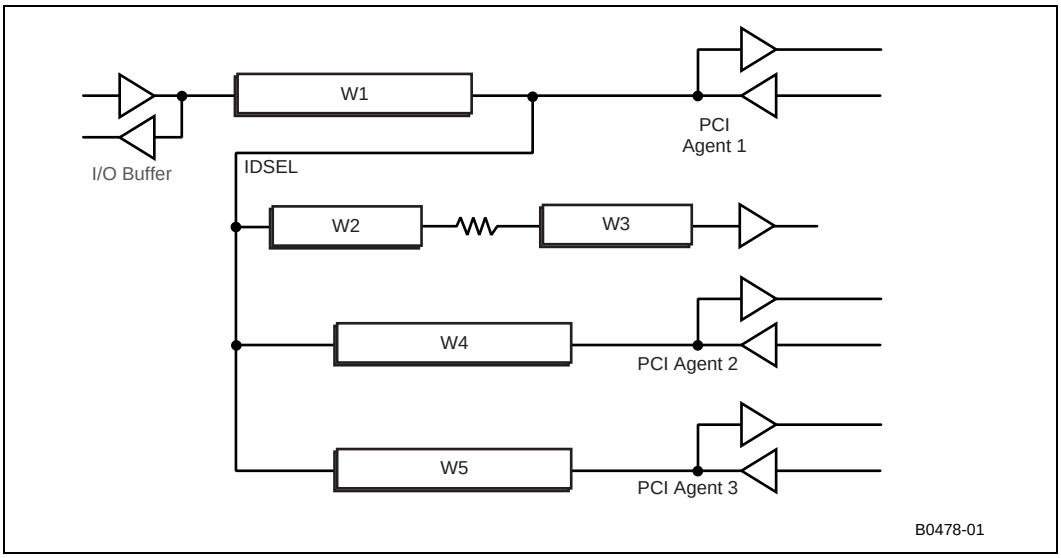

Table 24. Wire Lengths For Multiple PCI-X Load Embedded Intel® 31244 PCI-X to Serial ATA Controller Design

Segment	Lower AD Bus		Upper AD Bus		Units
	Minimum Length	Maximum Length	Minimum Length	Maximum Length	
W1	2.25	9	3.25	10.25	inches
W2	0.1	0.2	N/A	N/A	inches
W3	1.625	1.725	N/A	N/A	inches
W4	1.65	3.2	N/A	N/A	inches
W5	1.65	3.2	N/A	N/A	inches

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Cables and Connectors 8

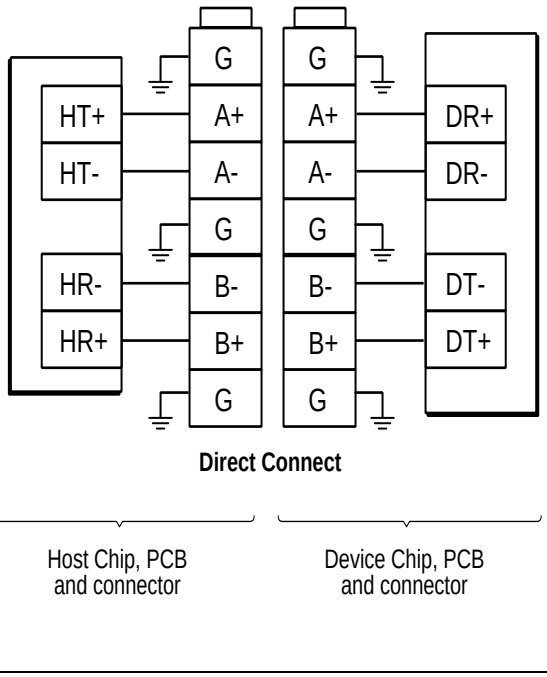
8.1 Cabling

A Serial ATA device is connected to a host through a direct connection or through a cable. For direct connection, the device plug connector, shown as (a) and (b) in Figure 21, is inserted directly into a host receptacle connector, illustrated as (g) in Figure 22. The device plug connector and the host receptacle connector incorporate features that enable the direct connection to be hot pluggable and blind mateable.

Table 25. Serial ATA Signal Definitions

Signals	Definition	Number of pins
G	Ground	1
A+/A-	Serial ATA port A differential signals	2
B+/B-:	Serial ATA port B differential signals	2
HT+/HT-	Host Transmitter differential signals	2
HR+/HR-	Host Receiver differential signals	2
DT+/DT-	Device Transmitter Differential Signals	2
DR+/DR-	Device Receiver Differential Signals	2

Figure 20. Serial ATA Direct Connect



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For connection through a cable, the device signal plug connector, shown as (a) in Figure 21, mates with the signal cable receptacle connector on one end of the cable, illustrated as (c) in Figure 21.

A Serial ATA power cable includes a power cable receptacle connector, shown as (d) in Figure 21 on one end and may be directly connected to the host power supply on the other end, or may include a power cable receptacle on the other end that mates with the device power plug connector, shown as (b) in Figure 21.

The power cable receptacle connector on one end of the power cable mates with the device power plug connector, shown as (b) in Figure 21.

Figure 21. Serial ATA Connectors Cable to Host Connections

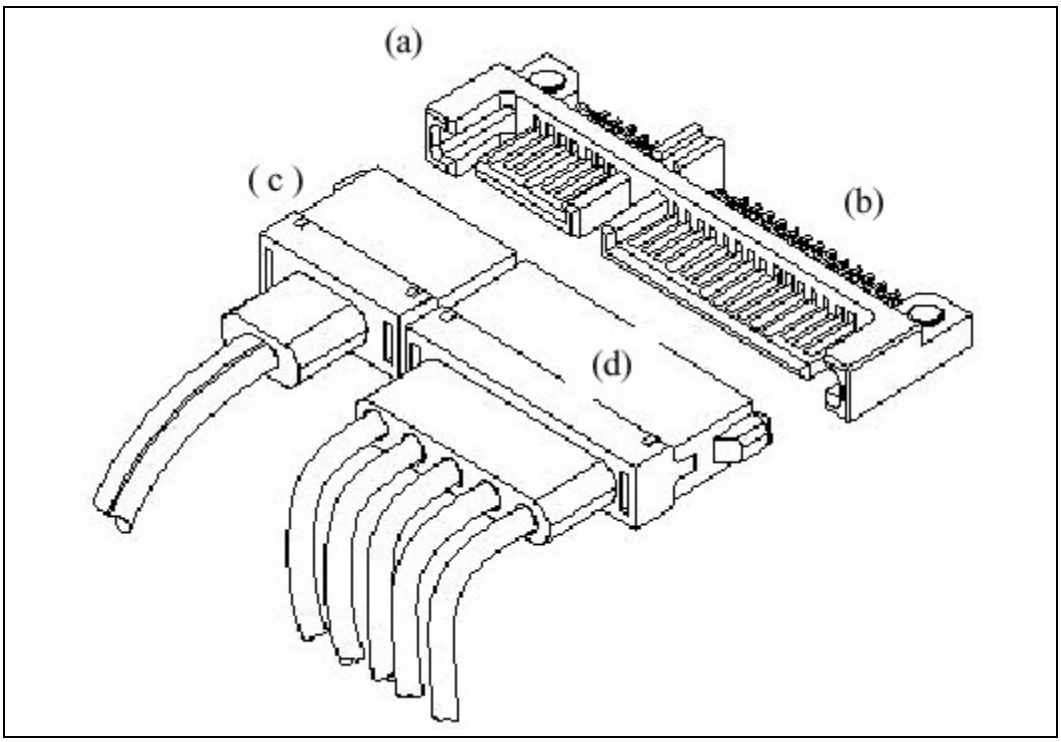

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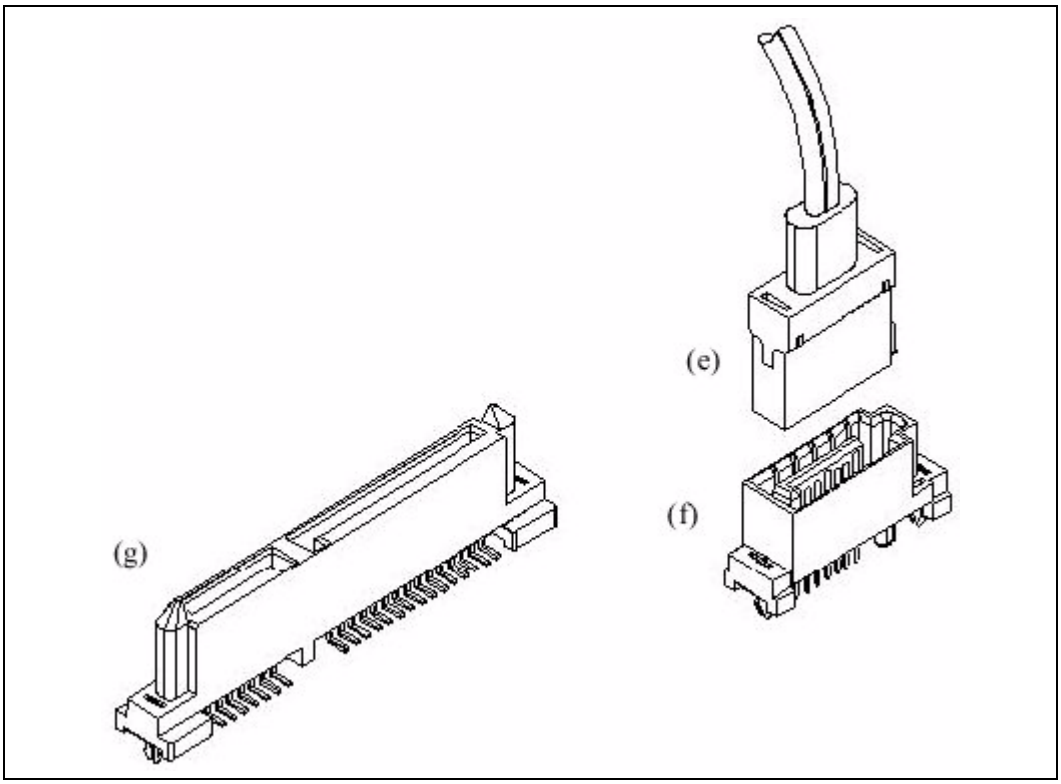
Figure 22. Serial ATA Host Connectors



The signal cable receptacle connector on the other end of the cable is inserted into a host signal plug connector, shown as (f) in Figure 22. The signal cable wire consists of two twinax sections in a common outer sheath.

Besides the signal cable, there is also a separate power cable for the cabled connection.

A Serial ATA power cable includes a power cable receptacle connector, shown as (d) in Figure 21, on one end and may be directly connected to the host power supply on the other end, or may include a power cable receptacle on the other end.

The power cable receptacle connector on one end of the power cable mates with the device power plug connector, shown as (b) in Figure 21. The other end of the power cable is attached to the host.

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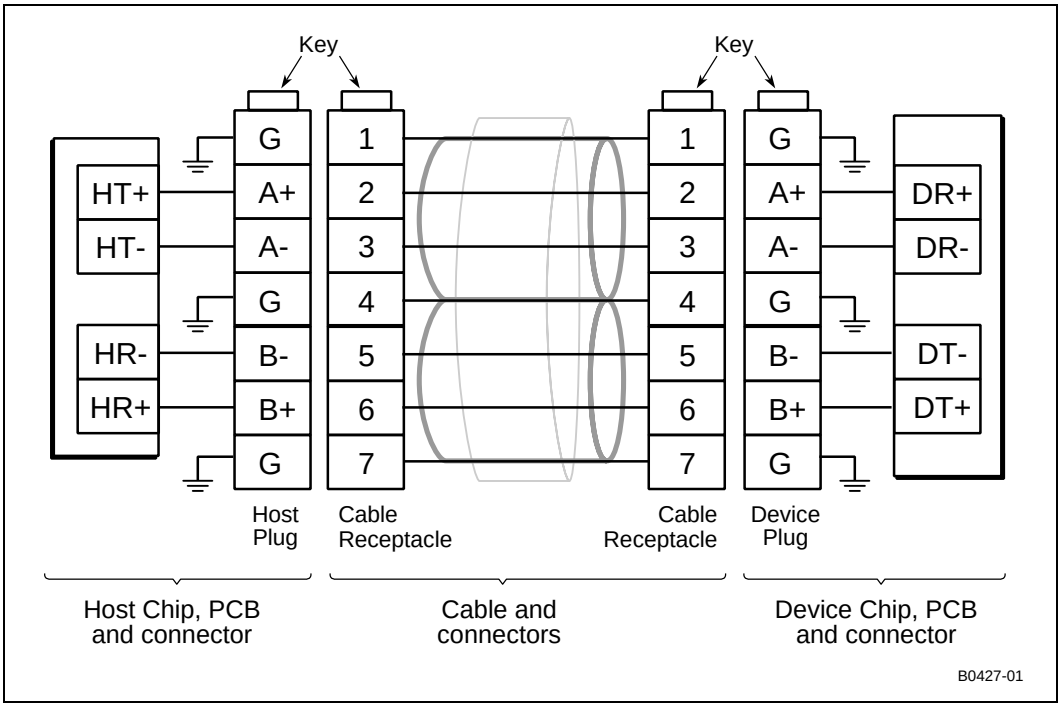
8.1.1 Serial ATA Cable

The Serial ATA cable consists of four conductors in two differential pairs. When necessary, the cable may also include drain wires, to be terminated to the ground pins in the Serial ATA cable receptacle connectors. The cable size may be 30 to 26 AWG. The cable maximum length is one meter.

Figure 23. Serial ATA Cable Signal Connections



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Voltage Power Delivery 9

There are two different voltages needed on the Intel® 31244 PCI-X to serial ATA controller. These are V_{CC} of +2.5 V ±5% and V_{IO} of +3.3 V ±10%. Power sequencing is not required on the GD31244.

9.1 Intel® 31244 PCI-X to Serial ATA Controller Core Supply Voltage: Providing 2.5 V in 3.3 V System

In most system board designs, the 3.3 V system power supply is routed to board components through a dedicated board layer. With the requirements for 2.5 V supplies for the GD31244, it is not necessary to add completely new power supply layers to the circuit board to facilitate this. It is possible to create supply “islands” underneath GD31244 in the existing power supply plane.

Other important considerations are:

- The ‘island’ must be large enough to include the required power supply decoupling capacitance, and the necessary connection to the voltage source.
- To minimize signal degradation, the gap between the supply island and the voltage plane kept to a minimum: typical gap size is about 0.02 inches.
- Minimize the number of traces routed across the power plane gap, since each crossing introduces signal degradation due to the impedance discontinuity that occurs at the gap. For traces that must cross the gap, route them on the side of the board next to the ground plane to reduce or eliminate the signal degradation caused by crossing the gap. When this is not possible, then route the trace to cross the gap at a right angle (90 degrees).
- Use liberal decoupling capacitance between the voltage plane and the supply islands. Decoupling the island reduces impedance discontinuity.

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Test Methodology 10

The signaling requirements of the SATA specification are measured for signal quality, Table 26 details the values from the *SATA Specification*, revision 1.0, 29 August 200, starting on page 76.

Table 26. Interface Timing and SI Requirements

Symbol	Parameter	Min	Max	Units
T,UI	Operating data period	666.43	670.12	ps
t_{rise}	20% to 80% at transmitter	0.2	0.41	UI
t_{fall}	80% to 20% at transmitter	0.2	0.41	UI
$V_{cm,ac}$	Max sinusoidal amplitude of common mode signal measured at receiver connector		100	mV
$T_{settle,CM}$	Maximum time for common-mode transients to settle to within 10% of DC value during transitions to and from the idle bus condition.		10	ns
$V_{diff,tx}$	+/- 250 mV differential nominal. Measured at Serial ATA connector on transmit side	400	600	mV p-p
$V_{diff,rx}$	+/- 200 mV differential nominal. Measured at Serial ATA connector on receive side	325	600	mV p-p
Tx_{Zout}	Tx differential output impedance as seen by a differential TDR with 100 ps (max) edge looking into connector (20%-80%)	85	115	Ohm
Rx_{Zin}	Rx differential input impedance as seen by a differential TDR with 100 ps (max) edge looking into connector (20%-80%)	85	115	Ohms
Tx_{Skew}	TX differential skew		20	ps

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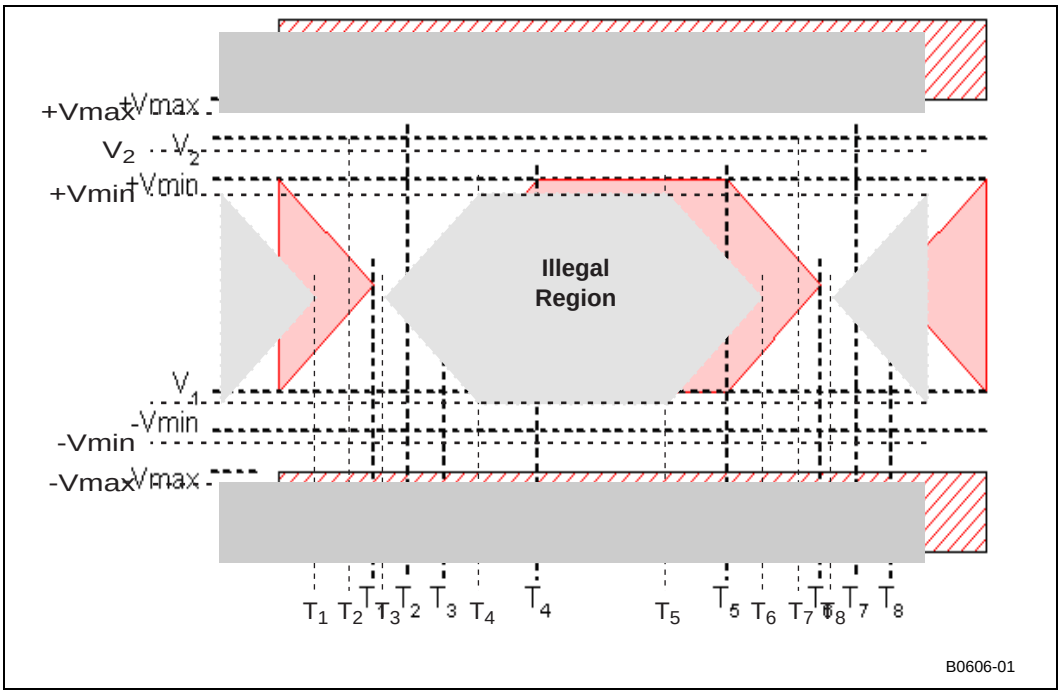
The SATA specification defines Figure 24 using values from Table 26 for the legal signaling levels and jitter.

Figure 24. Serial ATA Eye Diagram



Several of oscilloscopes provide eye pattern masking options to allow the user to set up a mask for serial data streams such as Serial ATA. Automating this measurement through oscilloscope eye mask setup takes a the qualitative guess work out of eye pattern analysis.

Table 27. Timing Requirement

Name	Definition	Notes
Tjitter	t3 -t1	t3 - t1 = t8 - t6
T	t7 - t2	t2 - t1 = t3 - t2 t7 - t6 = t8 - t7
Vdiff	V2 - V1	

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10.1 Extended Voltage Mode

Figure 25, Figure 26, Table 28 and Table 29 describe the extended voltage mode eye diagrams for the modified receiver and driver. These eye diagrams needed to be modified from the original SATA specification to allow for the higher voltage parameters required for a backplane design.

Note: The material in this section is preliminary.

10.1.1 Extended Voltage Mode Receiver Model

For GD31244 reads, the GD31244 receiver must be more sensitive than the SATA specification. The extended voltage mode eye diagram for the receiver shown in Figure 25 is superimposed on the SATA specified eye pattern. Table 28 provides the same parameters in a table format. These parameters are measured at the GD31244 RX pins.

Figure 25. Extended Mode Receiver Example

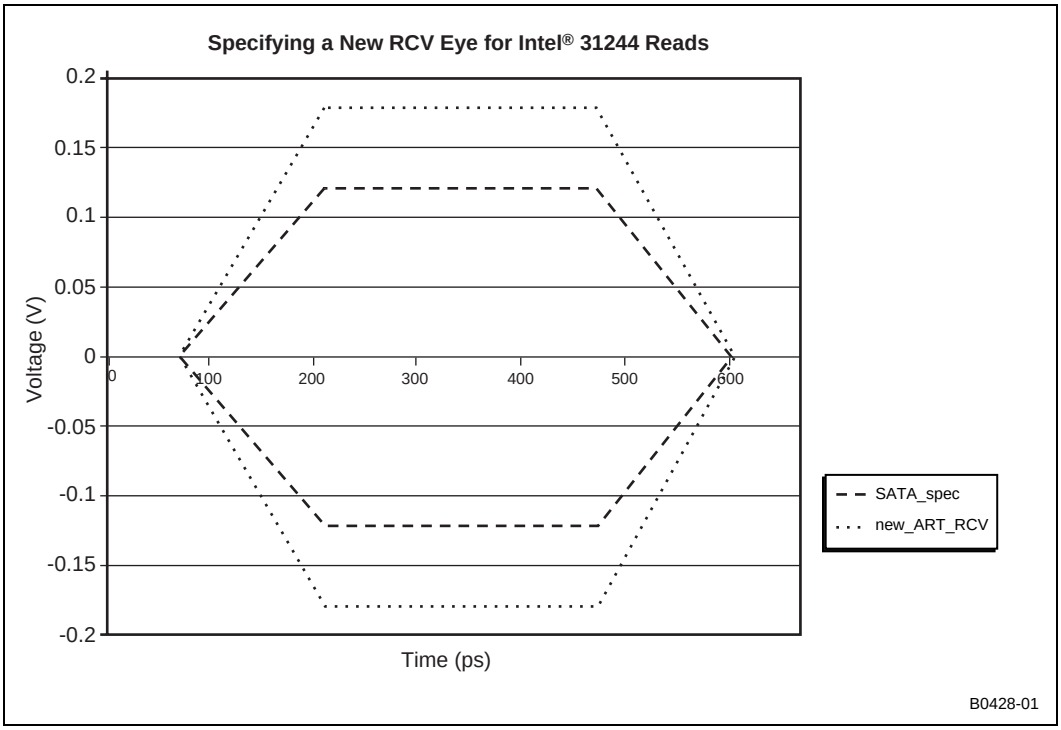

Table 28. Extended Voltage Mode Receiver

Parameter	Value
$V_{diff,rx}$	+/- 110 mV differential nominal. Measured at GD31244 RX pins on receive side.
Tjitter	0 - 7 UI maximum
Trise/fall (20-80%)	0.3 UI - 0.41 UI
Vmax @ backplane	600-650 mV
Vmin @ backplane	500 mV

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10.1.2 Extended Voltage Mode Driver Model

The extended voltage mode eye diagram for the new slow driver is shown in Figure 26 with the SATA driver mode superimposed. The extended voltage mode eye diagram for the driver is also shown in table format in Table 29.

Figure 26. Extended Mode Driver Example

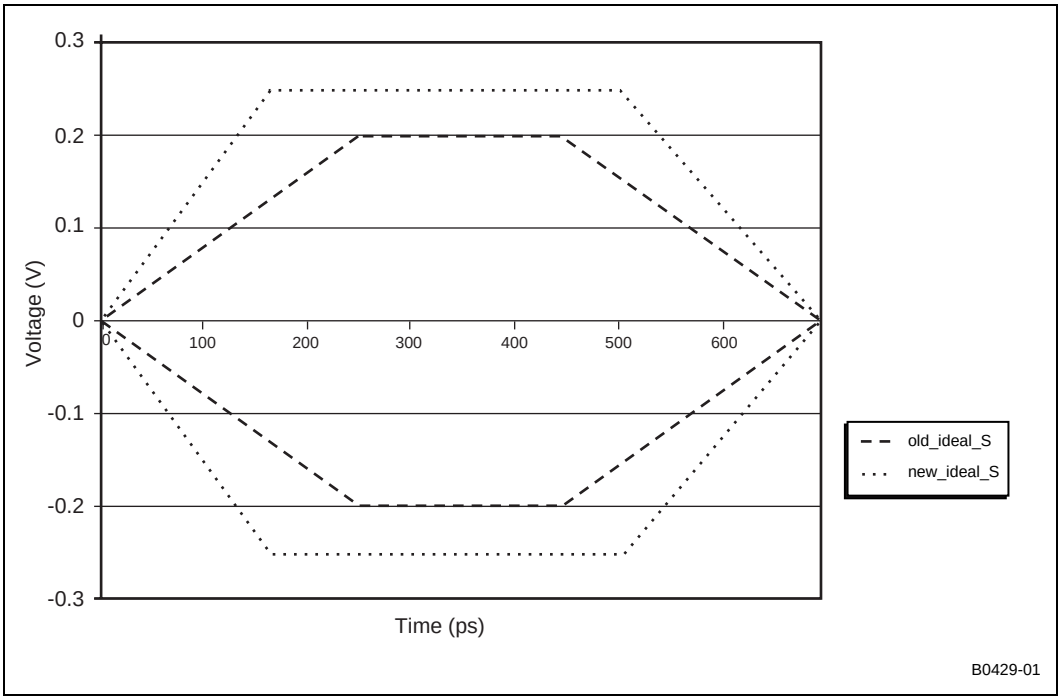

Table 29. Extended Mode Driver

Parameter	Value
$V_{diff,tx}$	+/- 250 mV differential nominal measured at GD31244 TX pins
T,slew	0.3 UI -0.41 UI
Tjitter	0 - 0.35 UI max
Trise/fall (20-80%)	0.3 UI -0.41 UI
Vmin @ GD31244 pin	800 mV
Vmax @ GD31244 pin	1200 mV

Note: The simulation using the maximum driver model with this resistor network shown in Figure 13, resulted in a 50 mV over the specification of 600 mV maximum. It is important to test this overdrive condition and make sure that the actual overdrive condition does not damage the SATA disks.

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Terminations: Pull-down/Pull-ups 11

This chapter provides the requirements for pull-down and pull-up terminations for the Intel® 31244 PCI-X to serial ATA controller.

The PCI-X interface pull-down/pull-up recommendation depends on the application. Table 30 details the termination of these signals when the following factors are true:

1. Embedded or motherboard application (non PCI/X plug-in card) with the GD31244 PCI-X interface as the primary interface.
2. Plug-in card with a PCI/X bridge as the interface into the slot. The GD31244 PCI-X interface is on a non-primary (i.e., secondary side) of the bridge.

When the application is a PCI/X plug-in card into a standard PC-style motherboard, the *PCI Local Bus Specification*, Revision 2.2, requires that the termination of these signals be placed on the motherboard.

The GD31244 uses 10 K pull-ups. The range of values is dependent on the number of loads in the user application. It may be determined from the formula for the pull-ups as stated in the *PCI Local Bus Specification*, Revision 2.2, as follows:

- Rmin = [Vcc(max) - Vol']/[Iol+(16 x Iol)] where 16 is the maximum number of loads
- Rmax = [Vcc(min) - Vx]/[num_loads x Imin] where Vx = 0.7 V_{CC} for 3.3 V signaling:

Table 30. Terminations: Pull-up/Pull-down (Sheet 1 of 2)

Signal Name	Pull-up or Pull-down	Comments
V18A	Refer to Figure 2 and comments	Connect this pin to 10 µF capacitor and 0.1 µF cap in parallel. The opposite end of the caps are connected to GND.
V18B	Refer to Figure 2 and comments	Connect this pin to 10 µF capacitor and 0.1 µF cap in parallel. The opposite end of the caps are connected to GND.
VA0	Refer to Figure 2 and comments	Use low inductance capacitors
VA1	Refer to Figure 2 and comments	Use low inductance capacitors
CAP0	Refer to Figure 2 and comments	This pin is connected to a 0.1 µF cap with the other end connected to the CAP1 pin.
CAP1	Refer to Figure 2 and comments	This pin is connected to a 0.1 µF cap with the other end connected to the CAP0 pin.
CAP2	Refer to Figure 2 and comments	This pin is connected to a 0.015 µF cap with the other end connected to the CAP3 pin.
CAP3	Refer to Figure 2 and comments	This pin is connected to a 0.015 µF cap with the other end connected to the CAP2 pin.
V_{CC5REF}	Refer to comments	In 5 V tolerant systems, this should be connected to a 5 V supply. In 3.3V powered systems this should be connected to 3.3 V. In PCI add-in cards, this would normally be connected to I/O Power (10 A, 16 A, 19 B, 59 A and 59 B).
RBIAS	Refer to Figure 2 and comments	Connect pin to a 1% 1000 ohm resistor to GND.

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Table 30. Terminations: Pull-up/Pull-down (Sheet 2 of 2)

Signal Name	Pull-up or Pull-down	Comments
TEST0	Connect to GND	
TOUT	NC	
32BITPCI#	1K pull-up for 64 bit	Controls status bit 16, in the PCI-X Status Register. When pulled down, reports a 0, for a 32-bit bus. When pulled up, reports 1, a 64-bit device.
DPA_MODE#	GND to enable DPA Mode	1K pull-up to enable legacy mode.
SSCEN	Connect to GND	
TX0P, TX0N, TX1P, TX1N,TX2P,TX2N RX0P, RX0N, RX1P, RX1N,RX2P,RX2N	series 0.01uF capacitor	
TRST#, TDI#, TMS#, TCK	4.7K pull-up	
P_SERR#	10 K pull-up[2]	
P_TRDY#	10 K pull-up[2]	
P_LOCK#	10 K pull-up[2]	
P_PERR#	10 K pull-up[2]	
P_DEVSEL#	10 K pull-up[2]	
P_FRAME#	10 K pull-up[2]	
P_STOP#	10 K pull-up[2]	
P_IRDY#	10 K pull-up[2]	
P_INTA#	10 K pull-up[2]	
P_INTB#	10 K pull-up[2]	
P_INTC#	10 K pull-up[2]	
P_INTD#	10 K pull-up[2]	
P_AD[63:32]	10 K pull-up[2]	
P_C/BE[7:4]#	10 K pull-up[2]	
P_PAR64	10 K pull-up[2]	
P_REQ64#	10 K pull-up[2]	
P_ACK64#	10 K pull-up[2]	

NOTES:
1. Pull-up only when PCI bus is to operate at 66 MHz and not already pulled up by system board. This signal is grounded for 33 MHz operation. It is advisable to connect **M66EN** to a 0.01 µF capacitor located with-in 0.25 inches of the M66EN pin on a add-in connector.
2. Pull-up only when not already pulled up on PCI bus. An add-in card may rely on the motherboard to pull-up these values.
3. PCI/XCAP - The maximum trace length between the resistor (when installed), capacitor, and the connector contact is 0.25 inches. The maximum trace length between the resistor (when installed), capacitor, and ground is 0.1 inches. A PCI-X card is not permitted to connect **PCI/XCAP** to anything else including supply voltages and device input and output pins.

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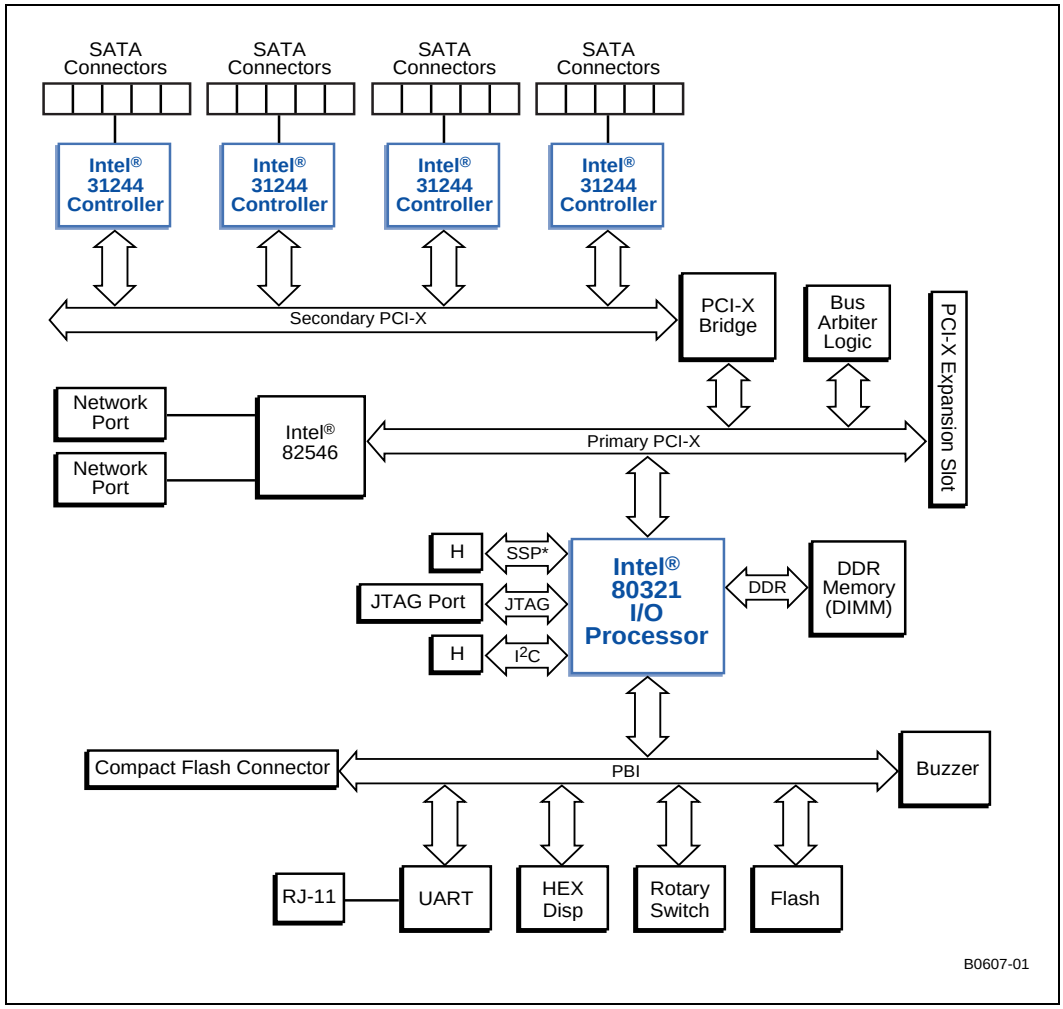
Intel® IQ31244 PCI-X to Serial ATA Controller Evaluation Platform Board 12

The Intel® IQ31244 PCI-X to Serial ATA Controller Evaluation Platform Board (IQ31244) is an Intel® 80321 I/O processor-based design using a PCI-X bridge, four Intel SATA controllers, and Intel® 82546EB Dual-Port Gigabit Ethernet Controller.

The main application for this customer reference board is external storage. The primary function of this system is to translate between a disk or network interconnect and SATA. It will also be used to demonstrate iSCSI and basic NAS functionality.

Figure 27 shows the block diagram of this customer reference board.

Figure 27. Intel® IQ31244 PCI-X to Serial ATA Controller Evaluation Platform Board Block Diagram



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12.1 Features

- Intel® 80321 I/O processor based on Intel® XScale™ microarchitecture
- 256 Mbytes DDR SDRAM in DIMM module16 Mbytes Flash ROM
- Primary PCI-X bus at 100 MHz including discreet arbitration logic (in CPLD)
- Dual 10/100/1000 BaseT Gigabit Ethernet Ports (82546)
- 64-bit/ 100 MHz PCI-X Expansion slot
- PCI-X to PCI-X Bridge to secondary bus (Intel® FW31154 PCI 133 MHz Bridge)
- Four Quad SATA Controllers (GD31244 device)
- UART Port
- Hex Display (two digits)
- Rotary Switch
- Buzzer
- Compact Flash Port
- JTAG Debugger Port
- Red Boot Firmware
- Diagnostic Firmware
- ATX Form Factor
- ATX Power Supply connector

Appendix A, list the preliminary Bill of Materials for the IQ31244.

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Debug Connectors and Logic Analyzer Connectivity 13

13.1 Probing PCI-X Signals

To ease the probing and debug of the PCI-X signals it is recommended to passively probe the PCI-X bus signals with a logic analyzer. This may be accomplished by placing six AMP* Mictor-38 connectors on the board or probing the bus with an interposer card such as the FuturePlus Systems* FS2007 that works with an Agilent Technologies* Logic Analyzer.

For ease of debugging the pin out of the AMP Mictor-38 connectors, the recommended pin-out matches the FuturePlus Systems* configuration setup, which allow ease of viewing the PCI signals on an Agilent Technologies* Logic Analyzer. Refer to the following test equipment that is used for this analysis:

- Two AMP 2-767004-2 surface mount connectors mounted on the target board and routed to the PCI-X Local bus.
- Two Agilent E5346A or E5351A High-Density Adapter Cables from FuturePlus Systems or Agilent Technologies.
- Four logic analyzer PODS.
- FS1104 Software from FuturePlus.

The equivalent for other analyzers may be substituted. A FuturePlus Systems configuration file with the FS1104 product that matches the pinout in Table 31.

Table 31. Logic Analyzer Pod 1 (Sheet 1 of 2)

Mictor-38 #1 Pin Number Odd Pod	Logic Analyzer Channel Number	PCI-X Name
6	CLKC/16	CLK
8	15	C/BE4
10	14	C/BE5
12	13	C/BE6
14	12	C/BE7
16	11	ACK64
18	10	REQ64
20	9	UNUSED
22	8	PME
24	7	C/BEO
26	6	M66EN
28	5	C/BE1
30	4	SERR
32	3	PAR

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Table 31. Logic Analyzer Pod 1 (Sheet 2 of 2)

Mictor-38 #1 Pin Number Odd Pod	Logic Analyzer Channel Number	PCI-X Name
34	2	PERR
36	1	LOCK
38	0	STOP

Table 32. Logic Analyzer Pod 2

Mictor-38 #1 Pin Number Odd Pod	Logic Analyzer Channel Number	PCI-X Signal Name
5	CLK/16	FRAME
7	15	DEVSEL
9	14	TRDY
11	13	C/BE2
13	12	C/BE3
15	11	IDSEL
17	10	REQ
19	9	GNT
21	8	INTD
23	7	INTC
25	6	INTB
27	5	INTA
29	4	UNUSED
31	3	UNUSED
33	2	UNUSED
35	1	UNUSED
37	0	UNUSED

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Table 33. Logic Analyzer Pod 3

Mictor-38 #2 Pin Number Odd Pod	Logic Analyzer Channel Number	PCI-X Signal Name
6	CLK/16	IRDY
8	15	AD15
10	14	AD14
12	13	AD13
14	12	AD12
16	11	AD11
18	10	AD10
20	9	AD09
22	8	AD08
24	7	AD07
26	6	AD06
28	5	AD05
30	4	AD04
32	3	AD03
34	2	AD02
36	1	AD01
38	0	AD00

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Table 34. Logic Analyzer Pod 4

Mictor-38 #2 Pin Number Odd Pod	Logic Analyzer Channel Number	PCI-X Signal Name
5	CLK/16	UNUSED
7	15	AD31
9	14	AD30
11	13	AD29
13	12	AD28
15	11	AD27
17	10	AD26
19	9	AD25
21	8	AD24
23	7	AD23
25	6	AD22
27	5	AD21
29	4	AD20
31	3	AD19
33	2	AD18
35	1	AD17
37	0	AD16

Table 35. Logic Analyzer Pod 5

Mictor-38 #3 Pin Number Odd Pod	Logic Analyzer Channel Number	PCI-X Signal Name
6	CLK/16	PAR64
8	15	AD47
10	14	AD46
12	13	AD45
14	12	AD44
16	11	AD43
18	10	AD42
20	9	AD41
22	8	AD40
24	7	AD39
26	6	AD38
28	5	AD37
30	4	AD36
32	3	AD35
34	2	AD34
36	1	AD33
38	0	AD32

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Table 36. Logic Analyzer Pod 6

Mictor-38 Pin Number Even Pod	Logic Analyzer Channel Number	PCI-X Signal Name
5	CLK/16	Unused
7	15	AD63
9	14	AD62
11	13	AD60
13	12	AD59
15	11	AD58
17	10	AD57
19	9	AD56
21	8	AD55
23	7	AD54
25	6	AD53
27	5	AD52
29	4	AD51
31	3	AD50
33	2	AD49
35	1	AD48
37	0	AD48

The recommended placement of the mictor connectors is at either end of the bus segment. The mictors are placed at the end of, as short a stub as possible, daisy chained off either end of the bus. When there is not enough room to place the mictors **0.5 inches** from the target, then an alternate method may be used. That is, to place the logic analyzer termination circuitry on the target and then extend the etch from the end of the termination circuitry over to the mictor connectors. The connection from the mictors to the logic analyzer must then be done with the **E5351A.** The **E5346A** contains the logic analyzer termination circuitry, the **E5351A** does not.

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Design for Manufacturing 14

The Intel® 31244 PCI-X to Serial ATA Controller is offered in a 256-pin plastic BGA. The construction of this package is shown in Figure 3. PBGA packaging is explained extensively in the *Intel® Packaging Databook* (Order Number 240800).

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Thermal Solutions 15

GD31244 is packaged in a 17 mm, 256-pin Plastic Ball Grid Array (PBGA) in an industry-standard footprint. The package includes a four layer substrate with power and ground planes. The construction of the package is shown below. The device is specified for operation when T_C (case temperature) is within the range of 0^o C to 90^o C, depending on the operating conditions. Refer to Figure 3 for a details on the package.

Table 37. Thermal Resistance

Symbol	Description	Value	Units
T_A	Still air ambient temperature to meet maximum case temperature specifications: [$T_A = T_C - (P_{DMAX}-\theta_{ca})$]	70	^{o}C
θ_{ca}	Thermal resistance from case to ambient in still air including conduction through the leads	20	^{o}C/Watt

Table 38. 544-Lead H-PBGA Package Thermal Characteristics

Thermal Resistance - ^{o}C/Watt					
Parameter	Airflow - ft/min. (M./sec.)				
	0	100	200	400	600
θ_{ca} Thermal Resistance from case to Ambient	20	12.5	11.2	10.2	9.2

15.1 Thermal Recommendations

Based on data Intel gathered while performing thermal validation, the GD31244 does not require a heat sink. The tests were performed in an environment with no airflow, an ambient temperature of 60° C with the processor executing a maximum power test. However, when the case temperature (108° C) is exceeded, a passive heat sink may be used.

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References 16

16.1 Related Documents

The following books and specifications may be helpful for designing with the Intel® 31244 PCI-X to serial ATA controller.

Table 39. Design References

	Design References
1	*Transmission Line Design Handbook*, Brian C. Wadell
2	*Microstrip Lines and Slotlines*, K. C. Gupta. Et al.
3	*PCI-X Addendum to the PCI Local Bus Specification*, Revision 1.0a
4	*PCI-X Electrical Subgroup Report, Version*1.0
5	*Design, Modeling and Simulation Methodology for High Frequency PCI-X Subsystems*, Moises Cases, Nam Pham, Dan Neal. Refer to www.pcisig.com.
6	*PCI Local Bus Specification,* Revision 2.2 PCI Special Interest Group 1-800-433-5177
7	*High-Speed Digital Design "A Handbook of Black Magic"* Howard W. Johnson, Martin Graham
8	Serial ATA: High-Speed Serial AT Attachment Rev. 1.0. Refer to http://www.serialata.org.
9	*"Terminating Differential Signals on PCBs"*, Steve Kaufer and Kelee Crisafulli, Printed Circuit Design, March 1999

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(1-800-548-4725) or visit the Intel website at http://www.intel.com

Table 40. Intel Related Documentation

Document Title	Order #
Intel® 31244 PCI-X to Serial ATA Controller Developer's Manual	273603
Intel® 31244 PCI-X to Serial ATA Controller Datasheet	273595
Intel® Packaging Databook	240800
Intel® 31244 PCI-X to Serial ATA Controller HBA Manual	273792
Intel® 31244 PCI-X to Serial ATA Controller Red Canyon CRB Manual	273801

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16.2 Electronic Information

Table 41. Electronic Information

The Intel World-Wide Web (WWW) Location:	http://www.intel.com
Customer Support (US and Canada):	800-628-8686

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Intel® IQ31244 Controller Evaluation Platform Board Bill of Materials A

The bill of materials (BOM) identifies all components on the Intel® 31244 PCI-X to Serial ATA Controller HBA reference board.

For the most up-to-date BOM, please visit the Intel® website:

http://developer.intel.com/design/storage/serialata/docs/gd31244.htm

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