AP440FX Motherboard

Technical Product Specification

May, 1997

Order Number 281830-002

The AP440FX motherboard may contain design defects or errors known as errata which may cause the product to deviate from published specifications. Current characterized errata are documented in the AP440FX Motherboard Specification Update.

Revision History

Revision	Revision History	Date
-001	Release of the AP440FX Technical Product Specification.	7/96
-002	Second release of the AP440FX Technical Product Specification	5/97

This product specification applies only to standard AP440FX motherboards with BIOS identifier 1.00.0x.CT1.

Changes to this specification will be published in the AP440FX Motherboard Specification Update (Order Number: 281831) before being incorporated into a revision of this document.

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1 Motherboard Description

1.1 Overview

The AP440FX motherboard is a 64-bit, high-performance, mixed-voltage, energy-conscious, highly integrated platform. The AP440FX motherboard supports the following set of features:

- Uses a 9-inch by 13-inch LPX form factor.
- Uses a type 8 Zero Insertion Force (ZIF) socket to house the standard processor, and provides an upgrade path to future OverDrive® processors.
- Accepts Pentium® Pro processors with core clock frequencies of 150 MHz, 166 MHz, 180 MHz, and 200 MHz.
- Supports up to 128 MB of DRAM using four standard 72-pin, tin-lead SIMM† sockets. The modules can use Fast Page Mode (FPM) or Extended Data Out (EDO) memory. Non-parity (32-bit) and parity (36-bit) memory SIMMs are supported. With parity SIMMs, the board can be configured to support Error Checking and Correcting (ECC) memory operation.
- Uses Intel's 82440FX chipset. The Intel 82371SB PCI/ISA IDE Xccelerator (PIIX3) provides an integrated Bus Mastering IDE controller with two high performance IDE interfaces for up to four devices (such as hard drives or CD-ROM).
- Uses a flash BIOS with the following features:
  - Uses both hardware and software Secure Flash features to protect flash contents from corruption.
  - Uses a BIOS that complies with the Desktop Management Interface (DMI-compliant).
- Uses the National Semiconductor Super I/O controller (the PC87307 or the pin-compatible PC87308 device) to integrate the following standard PC I/O functions:
  - floppy interface, two FIFO serial ports and one EPP/ECP capable parallel port
  - real-time clock
  - keyboard controller
  - support for an IrDA† and Consumer Infrared interface at both slow and medium speeds
- Integrates a Crystal audio codec (CS4236) on the motherboard to provide 16-bit stereo, Sound Blaster† Pro compatible audio. Provides an onboard telephony (modem) connector to support the latest telephony applications.
- Integrates an S3† ViRGE/DX† graphics controller onboard to support SVGA graphics at resolutions up to 1600x1200. An enhanced LBP VESA† feature connector supports external multimedia capabilities.
- A hardware monitoring ASIC provides the following monitoring functions:
  - Integrated temperature sensor
  - Fan speed monitoring
  - Power supply voltage monitoring
  - Storage of power-on self test (POST) results and error codes
- PCI and ISA expansion slots are supported by a connector on the motherboard designed to accept a riser card. An onboard jumper supports riser cards with either two or three PCI slots.

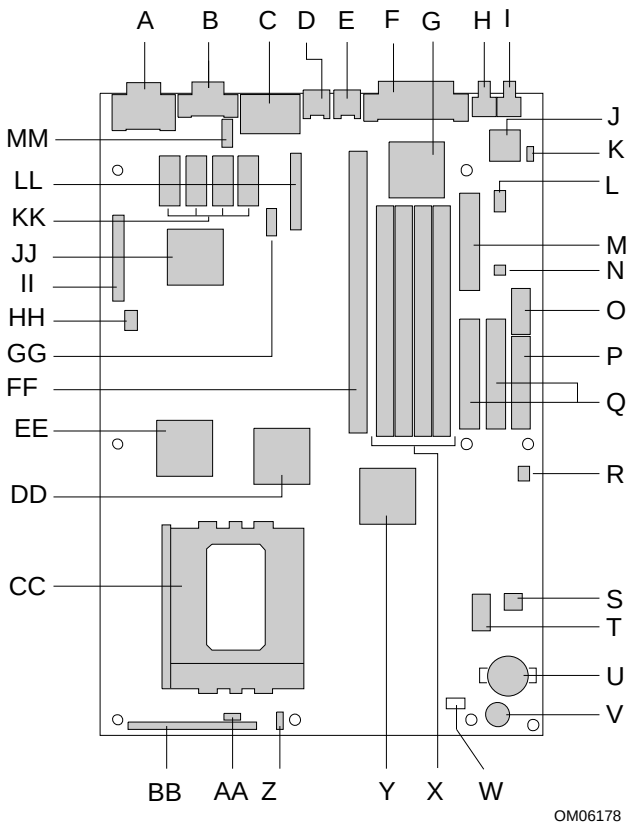

Figure 1. Motherboard Features

Table 1. Key to Motherboard Features

Key	Description	Key	Description	Key	Description
A	VGA† connector	B	Serial port connector	C	Side-by-side USB connectors
D	PS/2† mouse connector	E	PS/2 keyboard connector	F	Parallel port connector
G	I/O Controller (U7M1)	H	Microphone input jack	I	Audio output jack
J	Crystal audio controller (U9M1)	K	CD-ROM header (4x1, J9N1)	L	Wavetable header (2x4, J9L1)
M	Floppy connector (J8L1)	N	Telephony (modem) header (2x2, J9K1)	O	Standard 3.3V power connector (J9J1)
P	Main power connector (J9H1)	Q	IDE connectors (J8H1, J9H2)	R	Soft Off header (3x1, J9F1)
S	Hardware monitor ASIC (U9C1)	T	Flash BIOS (E28F002, U8C1)	U	Real-time clock battery (BT9B1)
V	Onboard speaker (L9A1)	W	3.5 V processor jumper (J8A2)	X	SIMM sockets (J6J1, J7J1, J7J2, J7J3)
Y	Intel SB82371SB (PIIX3, U6E1)	Z	Auxiliary fan header (1x3, J4A1)	AA	Keylock header (3x1, J3A1)
BB	Front panel connector (J2A1)	CC	Processor socket (U3C1)	DD	Intel SB82441FX (PMC, U4F1)
EE	Intel SB82442FX (DBX, U2F1)	FF	ISA/PCI riser socket (J6J2)	GG	Consumer/Fast IR header (5x2, J4L1)
HH	PCI slot Jumper block (2x3, J1J1)	II	LPB VESA header (J1K1)	JJ	S3 ViRGE/DX video controller (U2K1)
KK	2 MB of Video DRAM	LL	Configuration jumper block (J4L2)	MM	COM2H header (5x2, J3N1)

1.2 Motherboard Manufacturing Options

Contact your local Intel Field Sales Office for options and ordering information.

1.3 Form Factor

The motherboard is designed to fit into a standard LPX form factor chassis. Figure 2 illustrates the mechanical form factor for the AP440FX. The AP440FX LPX form factor adheres to the standard LPX guidelines with outer dimensions of 9 inches x 13 inches.

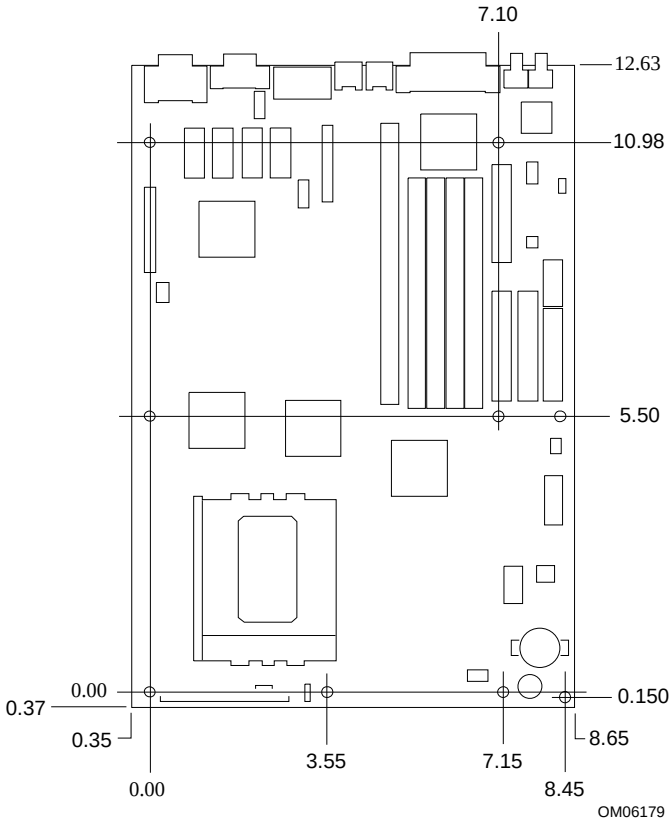

Figure 2. Motherboard Dimensions

1.4 I/O Shield

The back panel I/O shield for the AP440FX motherboard must meet specific dimensional and material requirements. Computers based on the AP440FX motherboard need the back panel I/O shield in order to pass certification testing. Figure 3 shows the critical dimensions for the I/O shield and indicates the position of each cutout.

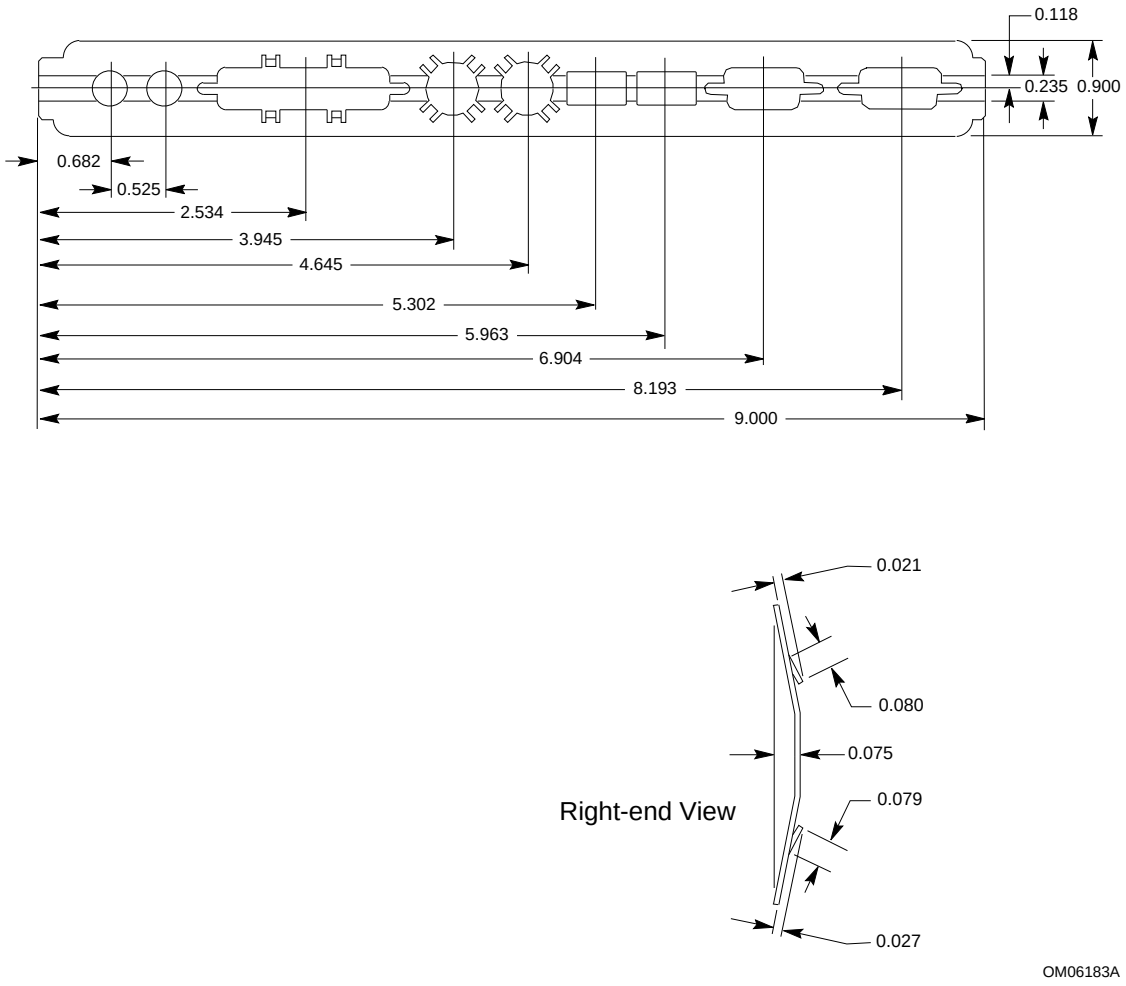

Figure 3. Back Panel I/O Shield Dimensions

1.5 Microprocessor

The AP440FX motherboard operates with 2.1 V to 3.5 V Pentium Pro processors. An onboard voltage regulator circuit provides the required voltages from the 5 V and 3.3 V taps off the power supply. The onboard voltage regulator makes use of the VID capabilities to automatically adjust its voltage output to match that of the installed processor. Pentium Pro processors running at 150, 166, 180, and 200 MHz are supported.

The Pentium Pro processor integrates the second level cache and cache controller that were previously implemented on the motherboard. The internal, non-blocking L2 cache on the 150, 180 and 200 MHz processors is 256 KB, while second versions of the 166 and 200 MHz processors integrate a 512 KB cache. The Pentium Pro processor has an advanced numeric coprocessor that significantly increases the speed of floating point operations, while maintaining backward compatibility with math coprocessors that comply with ANSI/IEEE standard 754-1985.

NOTE

If you are installing a 3.5 V processor, a jumper must be installed on the jumper block located at J8A2. See Section 1.13 for more information.

NOTE

The 200 MHz Pentium Pro processor with 512 KB of cache memory is not supported on the AP440FX motherboard.

1.5.1 Microprocessor Upgrade

Socket 8 is a 387-pin, modified staggered pin grid array (SPGA) zero insertion force (ZIF) socket, along with a programmable voltage regulator for the microprocessor core. It provides users with a performance upgrade path to OverDrive processors. The voltage regulator programming is automatic and controlled by the VID pins of the processor.

1.5.2 Microprocessor Heatsink and Clips

An approved Pentium Pro processor heatsink is necessary for proper thermal dissipation in an LPX compliant chassis. The processor/heatsink assembly must be securely fastened to the Socket 8 ZIF socket by two clips. These clips fit over the heatsink assembly and attach to the outer wide tabs of the Socket 8 assembly.

CAUTION

Do not use the older style of bail-wire clips for securing the heatsink assembly. These clips have been found to damage the motherboard when installed or removed incorrectly.

1.6 Main System Memory

The motherboard has four 72-pin tin-lead SIMM sockets that make it possible to install up to 128 MB of RAM. The sockets support 1M x 32 (4 MB) single-sided modules, 2M x 32 (8 MB), 4M x 32 (16 MB), and 8M x 32 (32 MB) single- or double-sided modules. Minimum memory size is 8 MB and maximum memory size, using four 8M x 32 SIMM modules, is 128 MB. Memory timing requires 60 ns fast page devices or, for optimum performance, 60 ns EDO DRAM. Both parity and non-parity memory modules are supported. With parity SIMMs, the board can be configured to support ECC operation.

The four sockets are arranged in two banks of two sockets each. The sockets are designated Bank 0 and Bank 1. Each bank provides a 64/72-bit wide data path. Both SIMMs in a bank must be of the same memory size and type, although the types and sizes of memory may differ between banks. Bank 0 only, Bank 1 only, or both of the banks may be populated. There are no jumper settings required for the memory size or type, which is automatically detected by the BIOS. Use only tin lead SIMMs when adding DRAM.

1.6.1 DRAM

EDO (or Hyper Page) DRAM is designed to improve the DRAM read performance. EDO DRAM holds the memory data valid until the next memory access cycle, unlike standard fast page mode DRAM that tri-states the memory data when the precharge cycle occurs, prior to the next memory access cycle.

1.6.2 Parity and ECC DRAM

Memory error checking and correction is supported by parity SIMMs. With parity SIMMs, the board can be configured to support ECC memory operation. Parity SIMMs are automatically detected, but the user must enter Setup to configure the SIMMs for either Parity or ECC operation. Parity memory detects single bit errors. ECC memory detects double bit errors and corrects single bit errors. Errors may be generated by a defective memory module, by different speeds of memory modules, or by DMA or memory conflicts.

1.7 Chipset

The Intel 82440FX PCIset consists of the 82441FX PCI Bridge and Memory controller (PMC) and the 82442FX Data Bus Accelerator (DBX). The Intel 82371SB PCI ISA/IDE Xccelerator (PIIX3) bridge, provides the connection between the ISA and PCI buses.

1.7.1 82441FX PCI Bridge and Memory Controller (PMC)

The 82441FX comes in a 208 pin QFP package and provides the following features:

- Microprocessor interface control
  - — Pentium Pro processor host bus up to 66 MHz
  - — 32-bit addressing

- Integrated DRAM controller
  - — 64/72-bit Non-Interleaved path to memory w/ ECC support
  - — Support for EDO and Fast Page DRAM
  - — 8 MB to 256 MB main memory
- Fully synchronous PCI bus interface
  - — PCI Rev. 2.1 - 5 V interface compliant
  - — 25/30/33 MHz
  - — PCI to DRAM > 100 MBps
- Data Buffering
  - — Host-to-DRAM and PCI-to-DRAM write data buffering
  - — Write combining support for host-to-PCI burst writes

1.7.2 82442FX Data Bus Accelerator (DBX)

The DBX connects to the 64 bit Pentium Pro processor data bus, the 64/72 bit memory data bus and the 16 bit PMC private data bus. The DBX works in parallel with the PMC to provide a high performance memory subsystem for Pentium Pro processor based computers. The DBX comes in a 208 pin PQF package.

1.7.3 82371SB PCI/ISA IDE Xccelerator (PIIX3)

The 82371SB provides the interface between the PCI and ISA buses and integrates a dual channel fast IDE interface capable of supporting up to four devices. The 82371SB integrates four 8-bit and three 16-bit DMA channels, three 8-bit timer/counters, two eight-channel interrupt controllers, PCI-to-AT† interrupt mapping circuitry, NMI logic, ISA refresh address generation, and PCI/ISA bus arbitration circuitry together into the same device. The PIIX3 comes in a 208-pin QFP package and provides the following features:

- Interface between the PCI bus and ISA bus
- Universal Serial Bus (USB)
  - — Host/Hub Controller
  - — Support for 2 USB ports
- Integrated fast IDE interface
  - — Support for up to 4 devices with separate Master/Slave mode support
  - — PIO Mode 4 transfers up to 16 MB/sec
  - — Integrated 8 x 32-bit buffer for Bus Master IDE PCI burst transfers
- Enhanced DMA controller with Fast Type-F DMA
- Counters/Timers
- Power Management
  - — Programmable system management interrupt (SMI)

1.7.4 IDE Support

The motherboard provides two independent high performance bus-mastering PCI IDE interfaces capable of supporting PIO Mode 3 and Mode 4 devices. The BIOS supports Logical Block Addressing (LBA) and Extended Cylinder Sector Head (ECHS) translation modes as well as ATAPI (e.g., CD-ROM) devices on both IDE interfaces. Detection of IDE device transfer rate and translation mode capability is automatically determined by the BIOS.

Normally, programmed I/O operations require a substantial amount of microprocessor bandwidth. In true multi-tasking operating systems like Windows† 95, the microprocessor bandwidth freed up by using PCI bus mastering IDE can be used to complete other tasks while disk transfers are occurring. When used in conjunction with the appropriate driver for the Windows 95 environment, the IDE interface can operate as a PCI bus master capable of supporting PIO Mode 4 devices with transfer rates of up to 16 MB/sec.

Detailed information on the PCIset is available in the Intel 82440FX PCISet data sheet.

1.7.5 Secure Flash Support

The AP440FX motherboard uses both onboard hardware and BIOS code support to protect the onboard flash memory device from accidentally or intentionally being corrupted. A general purpose I/O (GPIO) port of the I/O controller is used to control the write enable line of the flash device. By putting the microprocessor in System Management Mode (SMM) whenever the flash write is enabled, the BIOS can ensure that the SMM code is not corrupted and that flash can only be written from within SMM.

1.7.6 USB Support

The AP440FX motherboard has two USB ports. This permits connection of two USB peripheral devices directly to the computer without an external hub. If more devices are required, an external hub can be connected to either of the built-in ports. The motherboard completely supports the standard universal host controller interface (UHCI) and takes advantage of the standard software drivers written to be compatible with UHCI. Features of the USB include:

- Self-identifying peripherals
- Automatic mapping of function to driver and configuration
- Support for isochronous and asynchronous transfer types over the same set of wires
- Support for up to 127 physical devices
- Guaranteed bandwidth and low latencies appropriate for telephony, audio, and other applications
- Error handling and fault recovery mechanisms built into protocol
- Low cost cables and connectors

1.8 PC87307 Super I/O Controller

Control for the integrated serial ports, parallel port, floppy drive, real-time clock, and keyboard controller is incorporated into a single component, the National Semiconductor PC87307. The PC87307 is a fully Plug and Play compatible device which provides:

- Two NS16C550-compatible UARTs with send/receive 16 byte FIFO
  - — Support for an IrDA and Consumer IR compliant Infrared interface
- Multi-mode bi-directional parallel port
  - — Standard mode; IBM† and Centronics† compatible
  - — Enhanced Parallel Port (EPP) with BIOS/Driver support
  - — High Speed mode; Extended Capabilities Port (ECP) compatible
- Industry standard floppy controller with 16 byte data FIFO (2.88 MB floppy support)
- Integrated Real Time Clock with Century calendar functionality
- Integrated 8042 compatible keyboard controller

The PC87307 is normally configured automatically by the BIOS, but configuration of these interfaces also is possible using the CMOS Setup utility that can be invoked during boot. The serial ports can be enabled as COM1, COM2, COM2 as IrDA, or disabled. The parallel port can be configured as compatible, bi-directional, EPP/ECP, or disabled. The floppy interface can be configured for 360 KB or 1.2 MB 5¼" media or for 720 KB, 1.2 MB, 1.44 MB, or 2.88 MB 3½" media.

1.8.1 Floppy Controller

The PC87307 is software compatible with the DP8473 and 82077 floppy disk controllers. The floppy interface can be configured for 360 KB or 1.2 MB 5¼" media or for 720 KB, 1.2 MB, 1.44 MB, or 2.88 MB 3½" media in the BIOS setup. By default, the Floppy A interface is configured for 1.44 MB and Floppy B is disabled. Configuring the floppy interface for 1.2 MB 3½" (3-mode floppy) requires the use of a driver to operate correctly.

1.8.2 Keyboard and Mouse Interface

PS/2 keyboard/mouse connectors are located on the back panel side of the motherboard. The 5V lines to these connectors are protected with a PolySwitch† circuit which acts much like a self-healing fuse, re-establishing the connection after an over-current condition is removed. While this device eliminates the possibility of having to replace a fuse, care should be taken to turn off the power before installing or removing a keyboard or mouse.

The integrated 8042 microcontroller contains the AMI Megakey keyboard/mouse controller code which, besides providing traditional keyboard and mouse control functions, supports Power-On/Reset (POR) password protection. The POR password can be defined by the user in the Setup program. The keyboard controller also provides for the following “hot-key” sequences:

- <CTRL> <ALT> <DEL>: System software reset. This sequence performs a software reset of the computer by jumping to the beginning of the BIOS code and running the POST operation.

- <CTRL> <ALT> <defined in Setup>: Power down and coffee-break key sequences take advantage of the SMM features of the Pentium Pro processor to greatly reduce the computer's power consumption while maintaining the responsiveness necessary to service external interrupts.
- <CTRL> <ALT> <defined in Setup>: Keyboard secure hot keys lock the keyboard until user specified password is given.

1.8.3 Real-Time Clock, CMOS RAM and Battery

The integrated real-time clock is compatible with DS1287 and MC146818 components. It provides a time of day clock, a 100-year calendar with alarm features, and a century register. The real-time clock can be set in the Setup program. The real-time clock also supports 242-byte battery-backed CMOS RAM in two banks which is reserved for BIOS use. The CMOS RAM can be set to specific values or cleared to the default values using the Setup program. Also, the CMOS RAM values can be cleared to the defaults by using a configuration jumper on the motherboard.

An external coin-cell style battery provides power to the real-time clock and CMOS memory. The battery used is a long-life version that is socketed for easy replacement. When the computer is on, the life of the battery is extended by a trickle current from the power supply.

1.8.4 Infrared Support

A 5-pin interface on the front panel I/O connector allows connection to a Hewlett Packard† HSDL-1000 compatible infrared (IrDA) transmitter/receiver. Once the module is connected to the front panel I/O header, Serial port 2 can be redirected to the IrDA module. When configured for IrDA, the user can transfer files to or from portable devices such as laptops, PDAs and printers using application software such as LapLink†. The IrDA specification provides for data transfers at 115kbps from a distance of 1 meter. Support for Consumer Infrared (ASK-IR and DASK-IR options for SHARP-IR) is also included. Consumer infrared is supported at both slow and medium speeds.

1.8.5 Parallel Port

A 25-pin D-Sub header is provided on the back panel for a multi-mode bi-directional parallel port. The parallel port operates in standard mode, Enhanced Parallel Port (EPP) version 1.7 mode, with BIOS and Driver support, and a high speed Extended Capabilities Port (ECP) compatible mode. EPP Mode requires a driver provided by the peripheral manufacturer to operate correctly.

1.9 Graphics Subsystem

The AP440FX motherboard is available with a factory option of an S3 ViRGE† or ViRGE/DX SVGA graphics controller. Both options are supported by 2 MB of 50 ns EDO SOJ DRAM soldered to the motherboard. The AP440FX motherboard also supports the S3 media channel, also known as the Local Peripheral Bus (LBP) or Scenic Highway.

1.9.1 S3 ViRGE Graphics Subsystem

The AP440FX motherboard is available with a factory option of an S3 ViRGE SVGA graphics controller with 2 MB of 50 ns EDO SOJ DRAM. The S3 ViRGE has a high performance 64-bit 2D/3D graphics engine and incorporates the S3 Streams Processor that enables the device to convert YUV formatted video data to RGB and provides acceleration for scaling the video display without compromising picture quality or frame rate. The on-chip RAMDAC/clock synthesizer is capable of output pixel data rates of 135 MHz providing non-interlaced screen resolutions of up to 1280x1024x256 colors at 75 Hz. The 64-bit S3d Engine incorporates the key Windows and other GUI accelerator functions of BitBLT, line draw and polygon fill. 3D features include flat shading, Gouraud shading and texture mapping support. Advanced texture mapping features include perspective correction, bi-linear and tri-linear filtering, MIP-mapping, and Z-buffering. These features provide the most realistic user experience for interactive 3D applications. In addition, a fast linear addressing scheme based upon DCI reduces software overhead by mapping the display memory into the microprocessor's upper memory address space and permitting direct microprocessor access to the display memory.

Table 2. S3 ViRGE Supported Resolutions

Resolution	Refresh rate (Hz)
640 x 480 x 16 colors	60
640 x 480 x 256 colors	60, 72, 75, 85
640 x 480 x 65,536 colors	60, 72, 75
640 x 480 x 16,777,216 colors (non-accelerated mode)	60, 72, 75
800 x 600 x 256	56, 60, 72, 75, 85
800 x 600 x 65,536	60, 72, 75
800 x 600 x 16,777,216 colors (non-accelerated mode)	60, 72, 75
1024 x 768 x 256	43(IL), 60, 70, 75, 85
1024 x 768 x 65,536	43(IL), 60, 70, 75
1280 x 1024 x 256	45(IL), 60, 72, 75

NOTE: IL = Interlaced

The S3 ViRGE graphics controller supports more modes than shown above. The graphics drivers provide options for additional resolutions.

1.9.2 S3 ViRGE/DX Graphics Subsystem

The optional onboard graphics subsystem uses the S3 ViRGE/DX graphics controller, with the following features:

- 64-bit graphics engine with accelerator core
- 24-bit RAMDAC/clock synthesizer
- Dual programmable clock generators
- DCI-based linear addressing scheme
- S3 Streams Processor, which enables the conversion of video data from YUV format to RGB format and accelerates display scaling while maintaining picture quality and frame rate
- 3-D graphics support including flat shading, Gouraud shading, and advanced texture mapping
- S3 Scenic Highway support for hardware MPEG

Table 3. S3 ViRGE/DX Supported Resolutions

	Refresh Rate (Hz) At:				
Resolution	**4-bit Color (16 Colors)**	**8-bit Color (256 Colors)**	**15/16-bit Color (32K/64K Colors)**	**24-bit Color (16M Colors)**	**32-bit Color (16M Colors)**
640 x 480	60	60, 72, 75, 85	60, 72, 75	60, 72, 75 *	60, 72, 75
800 x 600	not supported	56, 60, 72, 75, 85	60, 72, 75	60, 72, 75 *	60, 72, 75
1024 x 768	not supported	43(IL), 60 ,70, 75, 85	43(IL), 60, 70, 75	not supported	not supported
1280 x 1024	43(IL), 45(IL), 60, 72, 75 *	45(IL), 60, 72, 75	not supported	not supported	not supported
1600 x 1200	not supported	48.5(IL)	not supported	not supported	not supported

* Non-accelerated mode only

IL = Interlaced

The S3 ViRGE/DX graphics controller supports more modes than shown above. The graphics drivers provide options for additional resolutions.

1.9.3 LBP VESA Feature Connector

The AP440FX motherboard supports a 34-pin VESA feature connector (which also accepts a 26-pin peripheral plug) for synchronizing graphics output with an external NTSC or PAL signal and a shared frame buffer interface to maximize multimedia performance, as well as the LPB or Scenic Highway that provides a glueless bi-directional interface to a video companion device such as an MPEG/live video decoder. The AP440FX also supports other VESA standards such as the VESA DPMS protocol to put a DPMS compliant monitor into power saving modes and the VESA Display Data Channel (DDC2B) that permits transfer of monitor identification and resolution support data for ease of use.

1.9.4 Graphics Drivers and Utilities

Graphics drivers and utilities may be downloaded from the Intel Applications Support web site at *http://www-cs.intel.com/oem_developer/motherbd*. Once the site is accessed, perform a keyword search for the specific application and its driver. Drivers for SCO† UNIX† are available from SCO.

1.10 Audio Subsystem

The AP440FX motherboard features a 16-bit stereo audio subsystem as a factory installed option. The audio subsystem is based on the Crystal CS4236 multimedia codec. The CS4236 provides all the digital audio and analog mixing functions required for playing and recording of audio on personal computers. These functions include:

- Stereo analog-to-digital and digital-to-analog converters
- Analog mixing
- Anti-aliasing and reconstruction filters
- Line and microphone level inputs
- Digital audio compression using selectable A-law / μlaw
- Full digital control of all mixer and volume control functions

The CS4236 also provides support for four major sound standards including AdLib†, Sound Blaster Pro 2.0, Windows Sound System, and MPU-401. The CS4236 also supports full-duplex operation which ensures support for applications such as video conferencing.

The CS4236 includes a Plug and Play compatible ISA interface and is comprised of seven logical devices including:

- Synthesizer
- Game Port
- Sound Blaster
- Sound System
- MPU-401
- CD-ROM
- CS4236 device

Each logical device is configured into the host environment using the ISA Plug and Play configuration methodologies. The audio subsystem requires up to two DMA channels and one interrupt. The computer can be configured to use either DMA channels 0, 1, or 3. The interrupt can be mapped to use interrupt 5, 7, 9, 11, 12, or 15.

1.11 Management Extension Hardware

The Management Extension hardware provides low-cost instrumentation capabilities designed to reduce the total cost of PC ownership. The Management Extension hardware incorporates features that support the requirements of the Desktop Management Interface (DMI) compliant areas of the BIOS, as well as those of the LANDesk® Client Manager software. The hardware implementation is a single-chip ASIC with the following features:

- An integrated temperature sensor plus support for an external temperature sensor
- Support for one fan speed sensor
- Power supply voltage monitoring to detect levels above or below acceptable values
- Registers for storing POST hardware test results and error codes
- Remote reset capabilities from a remote peer or server through LANDesk Client Manager, Version 3.0 and service layers (when available)
- Hardware compatibility with Windows NT†.

When an out-of-range condition (temperature, fan speed, or voltage) is reached, an interrupt is activated. The Management Extension circuitry connects to the ISA bus as an 8-bit I/O mapped device and uses the I/O addresses identified in the I/O map.

1.12 Motherboard Connectors

The AP440FX motherboard has onboard connectors supporting the following feature areas:

- Front panel features
- Memory (SIMM) and expansion (PCI/ISA riser) sockets
- Video features
- Serial header
- Audio features
- Power connectors
- Floppy and PCI IDE connectors

Figure 4 identifies the connectors on the AP440FX motherboard, and indicates the feature area with which each connector is associated.

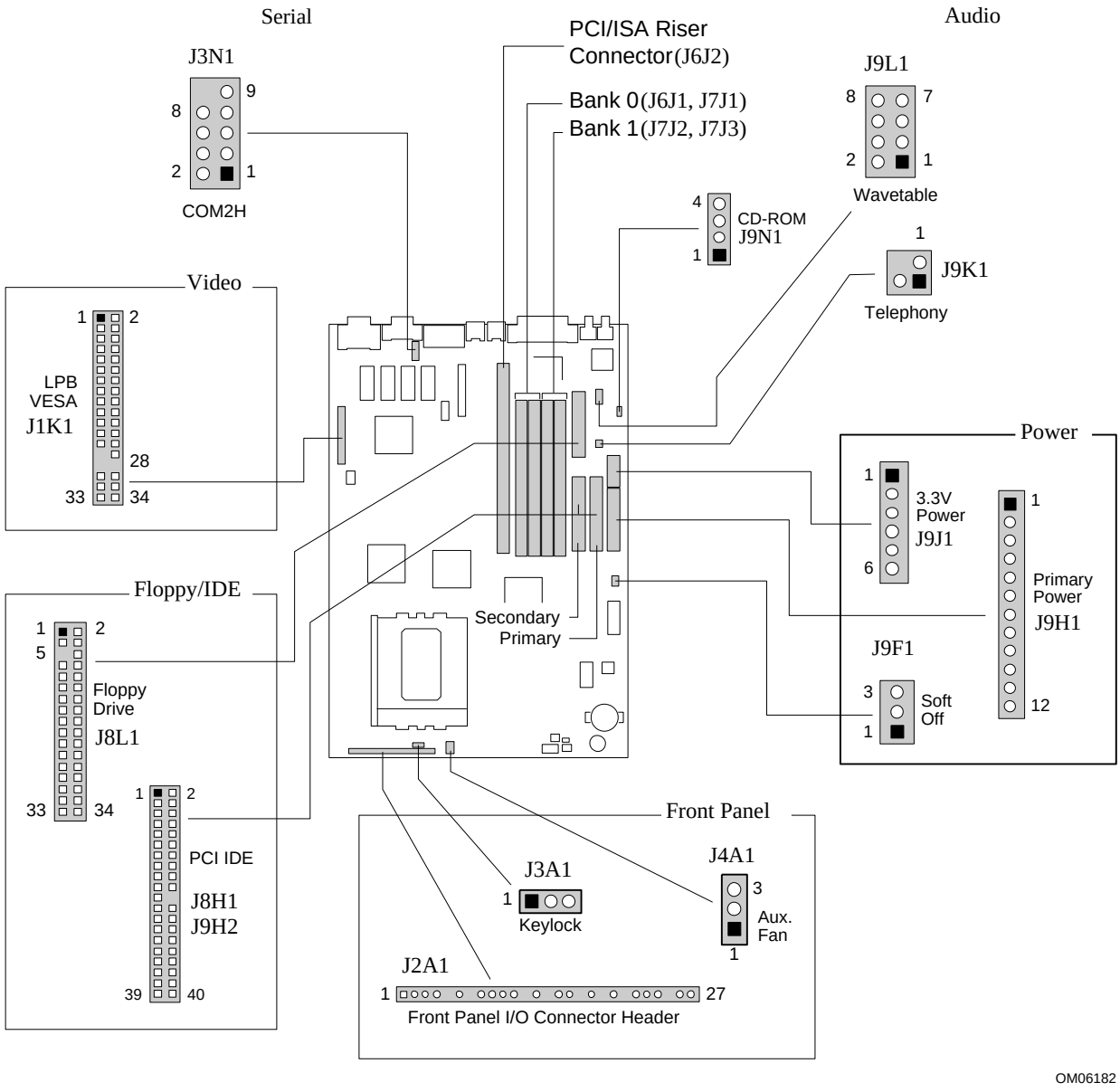

Figure 4. Motherboard Connector Locations

1.12.1 Front Panel Connectors

The AP440FX motherboard provides connectors to support functions typically located on the chassis bezel. In addition, connectors are provided that support a cooling fan and a keyboard lock. Front panel features supported by front panel connectors include:

- Soft Power-On
- Sleep/Resume
- Infrared (IrDA) port
- Hard Drive activity LED
- Power LED
- Reset
- Speaker
- Keyboard lock

Each of the front panel connectors is identified in Figure 4. The front panel I/O connector and keyboard lock connector are shown, in detail, in Figure 5.

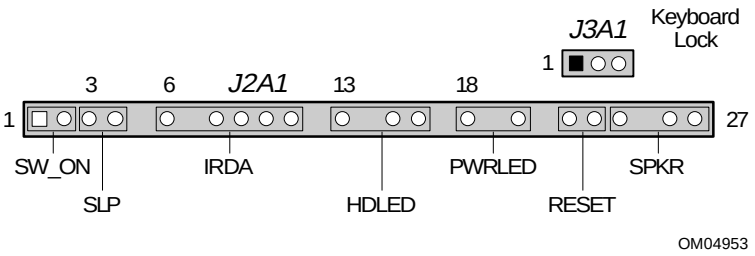

Figure 5. Front Panel I/O Connectors

Table 4 lists the pinout for the front panel I/O connector.

Table 4. Front Panel I/O Connector (J2A1)

Pin	Signal Name	Pin	Signal Name
1	SW_ON	15	HD ACTIVE
2	FPPWR_ON	16	+5V
3	SLEEP_REQ	17	Key
4	FPSLP	18	Ground
5	Key	19	Key
6	+5V	20	PWRDVR
7	Key	21	Key
8	IR_RX	22	Ground
9	Ground	23	FP_RESET
10	IR_TX	24	+5V
11	IR_SL1	25	Key
12	Key	26	SPKR_DAT connect
13	+5V	27	PC_SPKROUT
14	Key		

1.12.1.1 SW_ON

This 2-pin header connects to a front panel power switch. When the switch is closed, the power supply turns on. If a mechanical switch is connected to this header, it must apply a momentary ground to the SW_ON header pin in order to signal the supply to turn on or off. Because of the motherboard's internal debounce circuitry, the ground must be applied for at least 50ms. At least two seconds must pass before the power supply will recognize another on/off signal (to prevent "double clicking").

1.12.1.2 Sleep/Resume

When Advanced Power Management (APM) is activated in the BIOS and the Operating System's APM driver is loaded, Sleep mode (Standby) can be entered in one of three ways:

- An optional front panel "Sleep/Resume" button
- A user defined keyboard hot key
- Prolonged computer inactivity

The Sleep/Resume button is supported by a 2-pin header located on the front panel I/O connector. Closing the "Sleep" switch generates an SMI (System Management Interrupt) to the processor which immediately goes into System Management Mode (SMM).

The front panel "Sleep mode" switch must be a momentary two pin SPST type that is normally open. The function of the Sleep/Resume button can also be achieved by using a keyboard hot-key sequence, or by a time-out of the inactivity timer. Both the keyboard hot key and the inactivity timer are programmable in the BIOS Setup (timer is set to 10 minutes by default). To reactivate the computer, or "Resume", the user must simply press the sleep/resume button again, or use the keyboard or PS/2 mouse. Mouse activity only "wakes up" the computer if a mouse driver is loaded. While the computer is in Standby or "sleep" mode, it is fully capable of responding to and servicing external interrupts (such as in-coming FAX) even though the monitor only turns on if a user interrupt (keyboard/mouse) occurs as mentioned above.

1.12.1.3 Infrared Connector

Serial port 2 can be configured to support an IrDA module with a 5 pin header connector. Once configured for IrDA, the user can transfer files to or from portable devices such as laptops, PDAs and printers using application software such as LapLink. The IrDA specification provides for data transfers at 115 Kbps from a distance of 1 meter. Consumer IR is also supported by the same connector.

1.12.1.4 Hard Drive LED

This 3-pin, keyed header can be connected to a front panel LED to indicate when hard drive activity is taking place. When the hard drive is being accessed, the HDACTIVE pin (J2A1-15) goes low.

1.12.1.5 Power-ON LED

This 2-pin header can be connected to a front panel LED to indicate when power is applied to the motherboard. When the motherboard is powered up, power is applied to the PWRDRV pin (J2A1-20) to light the front panel LED.

1.12.1.6 Reset

This 2-pin header can be connected to a momentary SPST type switch that is normally open. When the switch is closed, the computer performs a hard reset and runs POST.

1.12.1.7 Speaker

The speaker provides error beep code information during the POST, if the computer cannot use the video interface. Jumpering pins 26-27 (the last two pins of J2A1) engage the onboard speaker. To disable the onboard speaker (and allow use of the chassis speaker), remove the jumper from these pins.

1.12.1.8 Keylock Connector (J3A1)

The Keylock connector pinout is listed in Table 5.

Table 5. Keylock Connector (J3A1)

Pin	Signal Name
1	Ground
2	KB_LOCK
3	Ground

1.12.1.9 Fan Connector (J4A1)

The auxiliary fan connector (J4A1) is a 1-by-3 header that can accept either two-position (power and ground) or three-position (power, ground, and fan sense) fan plugs. Figure 6 indicates the required orientation and positioning of the fan plug. Table 6 lists the signals and pinout for the fan connector.

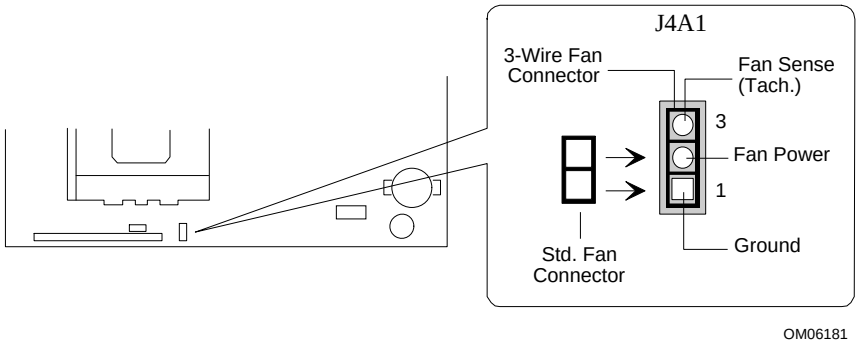

Figure 6. Fan Connector Usage

Table 6. Auxiliary Fan Connector (J4A1)

Pin	Signal Name / Function
1	Ground
2	Fan Power
3	Fan Sense (Tachometer)

1.12.2 Memory/Expansion Connectors

The AP440FX motherboard has four 72-pin SIMM sockets for main memory. These sockets accept standard SIMM 72-pin modules, as long as they satisfy the requirements described in the "Main System Memory" section of this specification, starting on page 12.

The AP440FX motherboard uses a PCI/ISA riser connector (J6J2) to provide for expansion PCI or ISA boards. The associated riser board can support either two or three PCI slots. A pair of jumpers on the AP440FX motherboard must be set to define the number of PCI slots on the riser board. Refer to Figure 8 on page 35 for jumper block details. Table 7 shows the pinout listing for the PCI/ISA riser connector.

Table 7. PCI/ISA Riser Connector (J6J2)

Pin	Signal Name	Pin	Signal Name	Pin	Signal	Pin	Signal Name
A1	IOCHK#	B1	GND	E1	GND	F1	GND
A2	SD7	B2	RSTDRV	E2	GND	F2	GND
A3	SD6	B3	Vcc	E3	PCIINT1#	F3	PCIINT3#
A4	SD5	B4	IRQ9	E4	PCIIINT2#	F4	PCIINT4#
A5	SD4	B5	-5 V	E5	Vcc	F5	Vcc
A6	SD3	B6	DRQ2	E6	Key	F6	Key
A7	SD2	B7	-12 V	E7	Vcc	F7	Vcc
A8	SD1	B8	0WS#	E8	PCIRST#	F8	PCKLF
A9	SD0	B9	+12 V	E9	GNT0#	F9	GND
A10	IOCHRDY	B10	GND	E10	REQ0#	F10	GNT1#
A11	AEN	B11	SMEMW#	E11	GND	F11	GND
A12	SA19	B12	SMEMR#	E12	PCKLE	F12	REQ1#
A13	SA18	B13	IOW#	E13	GND	F13	AD31
A14	SA17	B14	IOR#	E14	AD30	F14	AD29
A15	SA16	B15	DACK3#	E15	3.3 V	F15	3.3 V
A16	SA15	B16	DRQ3	E16	Key	F16	Key
A17	SA14	B17	DACK1#	E17	3.3 V	F17	3.3 V
A18	SA13	B18	DRQ1	E18	AD28	F18	AD27

continued ☛

Table 7. PCI/ISA Riser Connector (J6J2) (continued)

Pin	Signal Name	Pin	Signal Name	Pin	Signal	Pin	Signal Name
A19	SA12	B19	REFRESH#	E19	AD26	F19	AD25
A20	SA11	B20	SYSCLK	E20	AD24	F20	CBE3#
A21	SA10	B21	IRQ7	E21	AD22	F21	AD23
A22	SA9	B22	IRQ6	E22	AD20	F22	AD21
A23	SA8	B23	IRQ5	E23	AD18	F23	AD19
A24	SA7	B24	IRQ4	E24	3.3 V	F24	3.3 V
A25	SA6	B25	IRQ3	E25	Key	F25	Key
A26	SA5	B26	DACK2#	E26	3.3 V	F26	3.3 V
A27	SA4	B27	TC	E27	AD16	F27	AD17
A28	SA3	B28	BALE	E28	FRAME#	F28	IRDY#
A29	SA2	B29	Vcc	E29	CBE2#	F29	DEVSEL#
A30	SA1	B30	OSC	E30	TRDY#	F30	PLOCK#
A31	SA0	B31	GND	E31	STOP#	F31	PERR#
C1	SBHE#	D1	MEMCS16#	G1	SDONE	H1	SERR#
C2	LA23	D2	IOCS16#	G2	SBO#	H2	AD15
C3	LA22	D3	IRQ10	G3	CBE1#	H3	AD14
C4	LA21	D4	IRQ11	G4	PAR	H4	AD12
C5	LA20	D5	IRQ12	G5	GND	H5	GND
C6	LA19	D6	IRQ15	G6	Key	H6	Key
C7	LA18	D7	IRQ14	G7	GND	H7	GND
C8	LA17	D8	DACK0#	G8	AD13	H8	AD10
C9	MEMR#	D9	DRQ0	G9	AD11	H9	AD8
C10	MEMW#	D10	DACK5#	G10	AD9	H10	AD7
C11	SD8	D11	DRQ5	G11	CBE0#	H11	AD5
C12	SD9	D12	DACK6#	G12	AD6	H12	AD3
C13	SD10	D13	DRQ6	G13	AD4	H13	AD1
C14	SD11	D14	DACK7#	G14	AD2	H14	AD0
C15	SD12	D15	DRQ7	G15	Key	H15	Key
C16	SD13	D16	Vcc	G16	Vcc	H16	Vcc
C17	SD14	D17	MASTER#	G17	GNT2	H17	Vcc
C18	SD15	D18	GND	G18	(GND | REQ2) *	H18	(GND | PCCLK2) *
				G19	GND	H19	GND

* These signals are (2 slot | 3 slot) jumpered signal names.

1.12.3 VESA Feature Connector

Table 8 provides the pinout and signal listing for the LBP VESA feature connector.

Table 8. LBP VESA Feature Connector (J1K1)

Pin	Signal Name / Function	Pin	Signal Name / Function
1	Ground	2	Pixel Data 0
3	Ground	4	Pixel Data 1
5	Ground	6	Pixel Data 2
7	Enable External Pixel Data	8	Pixel Data 3
9	Enable External Sync	10	Pixel Data 4
11	Enable External Pixel Clock	12	Pixel Data 5
13	N/C, not used	14	Pixel Data 6
15	Ground	16	Pixel Data 7
17	Ground	18	PCLK, Pixel Clock
19	Ground	20	BLANKING
21	Ground	22	HSYNC, Horizontal Sync
23	N/C, not used	24	VSYNC, Vertical Sync
25	Key (no pin)	26	Ground
27	Key (no pin)	28	Key (no pin)
29	IICCLK	30	Ground
31	IICDAT	32	N/C
33	EN1	34	EN2

1.12.4 Serial Header

The COM2 serial port can be accessed using the COM2H header (J3N1) on the motherboard. Table 9 lists the signals and pinout for the COM2H header.

Table 9. Serial Port (COM2H, J3N1) Pinout

Pin	Signal Name	Description
1	DCD	Carrier Detect
2	DSR	Data Set Ready
3	SIN#	Serial Data In
4	RTS	Request To Send
5	SOUT#	Serial Data Out
6	CTS	Clear To Send
7	DTR	Data Terminal Ready
8	RI	Ring Indicator
9	GND	Chassis Ground
10	Key	Vacant

1.12.5 Audio Connectors

The pinouts and signal listings for the audio connectors are provided in Table 10, Table 11, and Table 12.

Table 10. CD-ROM Connector (J9N1)

Pin	Signal Name
1	Ground
2	CD-Left
3	Ground
4	CD-Right

Table 11. Wavetable Upgrade Connector (J9L1)

Pin	Signal Name
1	Wave Right
2	Ground
3	Wave Left
4	Ground
5	Key
6	Midi_In
7	NC
8	MIDI_Out

Table 12. Telephony Connector (J9K1)

Pin	Signal Name
1	Ground
2	Mono Out
3	Mic In
4	Key

1.12.6 Power Supply Connectors

The AP440FX motherboard must be used with a power supply that supports remote power on/off, so the motherboard can turn off the power under software control. The Powerman utility supplied for Windows 3.1x allows for soft-off as does the shutdown icon in Windows 95 Start menu. The BIOS turns the power off when it receives the proper APM command from the operating system. For example, Windows 95 issues this APM command after the user selects "Shutdown the computer" option. APM must be enabled in the BIOS and operating system in order for the soft-off feature to work correctly. The user has the ability to determine the state of the power supply, so if the computer was turned on when power was disconnected, the computer turns back on when power is reapplied or it remains off, depending on the user setup configuration in CMOS.

Table 13 provides the pinout listing for the primary power supply connector of the AP440FX motherboard.

Table 13. Primary Power Supply Connector (J9H1)

Pin	Name	Function
1	PWRGD	Power good
2	+5 V	+5 volts VCC
3	+12 V	+12 volts
4, key	-12 V	-12 volts
5	Ground	Ground
6	Ground	Ground
7, key	Ground	Ground
8	Ground	Ground
9	-5 V	-5 volts
10	+5 V	+5 volts VCC
11	+5 V	+5 volts VCC
12	+5 V	+5 volts VCC

Table 14 provides the pinout listing for the external 3.3 volt power supply connector of the AP440FX motherboard.

Table 14. External 3.3 V Power Supply Connector (J9J1)

Pin	Name
1	Ground
2	Ground
3	Ground
4	+3.3 V
5	+3.3 V
6 key	+3.3 V

The pinout listing for the soft-off power supply connector of the AP440FX motherboard is shown in Table 15. This 3-pin, keyed position supports a software-controlled power supply shutoff (soft-off). When connected to this position, the power supply follows remote on/off commands.

Table 15. Soft-Off Power Supply Connector (J9F1)

Pin	Name	Function
1	+5 VSB	+5 Volts Standby
2	PS_ON	Remote On/Off
3	PS_COM	Supply presence

1.12.7 Floppy/IDE Connectors

Table 16 lists the pinout and signal names for the floppy drive connector.

Table 16. Floppy Drive Connector (J8L1)

Pin	Signal Name	Pin	Signal Name
1	Ground	2	DENSEL
3	Ground	4	Reserved
5	Key	6	FDEDIN
7	Ground	8	Index#
9	Ground	10	Motor Enable A#
11	Ground	12	Drive Select B#
13	Ground	14	Drive Select A#
15	Ground	16	Motor Enable B#
17	MSEN1	18	DIR#
19	Ground	20	STEP#
21	Ground	22	Write Data#
23	Ground	24	Write Gate#
25	Ground	26	Track 00#
27	MSEN0	28	Write Protect#
29	Ground	30	Read Data#
31	Ground	32	Side 1 Select#
33	Ground	34	Diskette Change#

Table 17 lists the pinout and signal names for the IDE connectors.

Table 17. IDE Connectors (J8H1, J9H2)

Pin	Signal Name	Pin	Signal Name
1	Reset IDE	2	Ground
3	Host Data 7	4	Host Data 8
5	Host Data 6	6	Host Data 9
7	Host Data 5	8	Host Data 10
9	Host Data 4	10	Host Data 11
11	Host Data 3	12	Host Data 12
13	Host Data 2	14	Host Data 13
15	Host Data 1	16	Host Data 14
17	Host Data 0	18	Host Data 15
19	Ground	20	Key
21	DDRQ0 (DDRQ1)	22	Ground
23	I/O Write#	24	Ground
25	I/O Read#	26	Ground
27	IOCHRDY	28	Vcc pull-down
29	DDACK0 (DDACK1)#	30	Ground
31	IRQ14 (IRQ15)	32	Reserved
33	DAG1	34	Reserved
35	DAG0	36	DAG2
37	Chip Select 1P (1S)#	38	Chip Select 3P (3S)#
39	Activity#	40	Ground

1.12.8 Back Panel Connectors

Figure 7 shows the location of the back panel connectors.

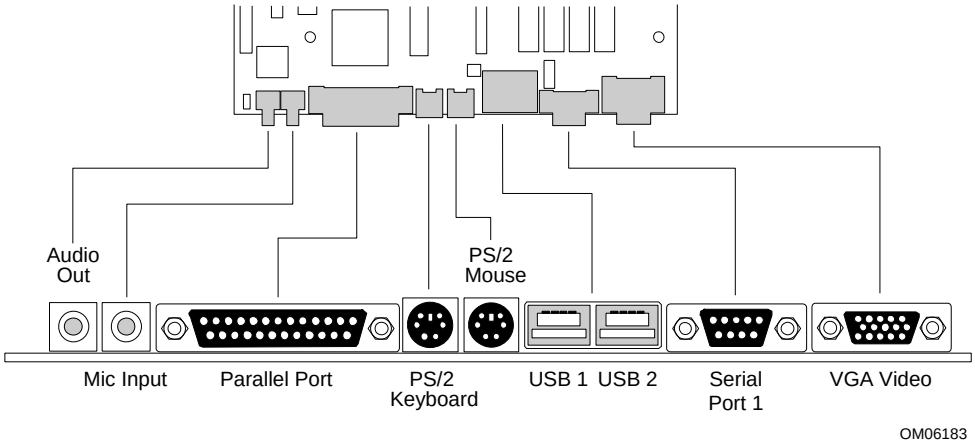

Figure 7. I/O Connections

1.12.8.1 VGA Video Connector

Table 18 lists the pinout and signal names for the VGA video connector.

Table 18. VGA Video Connector (J1N1)

Pin	Signal Name / Function	Pin	Signal Name / Function
1	Red Video	9	Key (no pin)
2	Green Video	10	Sync Return (Ground)
3	Blue Video	11	Monitor ID Bit 0 (not used)
4	Monitor ID Bit 2 (not used)	12	Monitor ID Bit 1 (not used)
5	Chassis Ground	13	Horizontal Sync
6	Red Return (Ground)	14	Vertical Sync
7	Green Return (Ground)	15	Not used
8	Blue Return (Ground)	Shield	Chassis Ground

1.12.8.2 COM1 Serial Port

Table 19 lists the pinout and signal names for the serial connectors.

Table 19. Serial Port Connector Pinout

Pin	Signal Name	Description
1	DCD	Carrier Detect
2	SIN#	Serial Data In
3	SOUT#	Serial Data Out
4	DTR#	Data Terminal Ready
5	GND	Chassis Ground
6	DSR#	Data Set Ready
7	RTS#	Request To Send
8	CTS#	Clear To Send
9	RI	Ring Indicator

1.12.8.3 USB Back Panel Connectors

Table 20 lists the pinout and signal names for the USB back panel connectors.

Table 20. USB Connector Pinout

Pin	Signal Name
1	+5 v (fused)
2	USBP0# [USBP1#] (fused)
3	USBP0 [USBP1] (fused)
4	Ground

1.12.8.4 Keyboard and Mouse Ports

Table 21 lists the pinout and signal names for the PS/2 keyboard and mouse connectors. Although they are labeled as “Keyboard” and “Mouse” on the motherboard and the back panel, the connectors can be used interchangeably for either keyboard or mouse.

Table 21. PS/2 Keyboard/Mouse Connector Pinout

Pin	Signal Name / Function
1	Data
2	No connect
3	Ground
4	+5 VDC (fused)
5	Clock
6	No connect

1.12.8.5 Parallel Port

Table 22 lists the pinout and signal names for the parallel port connector.

Table 22. Parallel Port Connector Pinout

Pin	Signal Name	Description	Pin	Signal Name	Description
1	STB#	Strobe	14	AFD#	Auto Feed
2	PPD0	Data Bit 0	15	ERROR#	Fault
3	PPD1	Data Bit 1	16	INIT#	Initializing printer
4	PPD2	Data Bit 2	17	SLCTIN#	Select input
5	PPD3	Data Bit 3	18	GND	Chassis Ground
6	PPD4	Data Bit 4	19	GND	Chassis Ground
7	PPD5	Data Bit 5	20	GND	Chassis Ground
8	PPD6	Data Bit 6	21	GND	Chassis Ground
9	PPD7	Data Bit 7	22	GND	Chassis Ground
10	ACK#	Acknowledge	23	GND	Chassis Ground
11	BUSY	Port Busy	24	GND	Chassis Ground
12	PE	Paper end	25	GND	Chassis Ground
13	SLCT	Select			

1.13 Jumper Settings

There are three jumper blocks on the AP440FX motherboard. The jumper block at J1J1 defines the number of PCI slots (two or three slots) available on the riser board used with the motherboard. The jumper block at J4L2 defines a range of microprocessor and motherboard configuration parameters. The jumper block at J8A2 is used to provide 3.5 V for processors that require that voltage. Figure 8 shows the jumper block locations on the motherboard, and indicates how jumper placement corresponds to the value defined by the motherboard silk-screening.

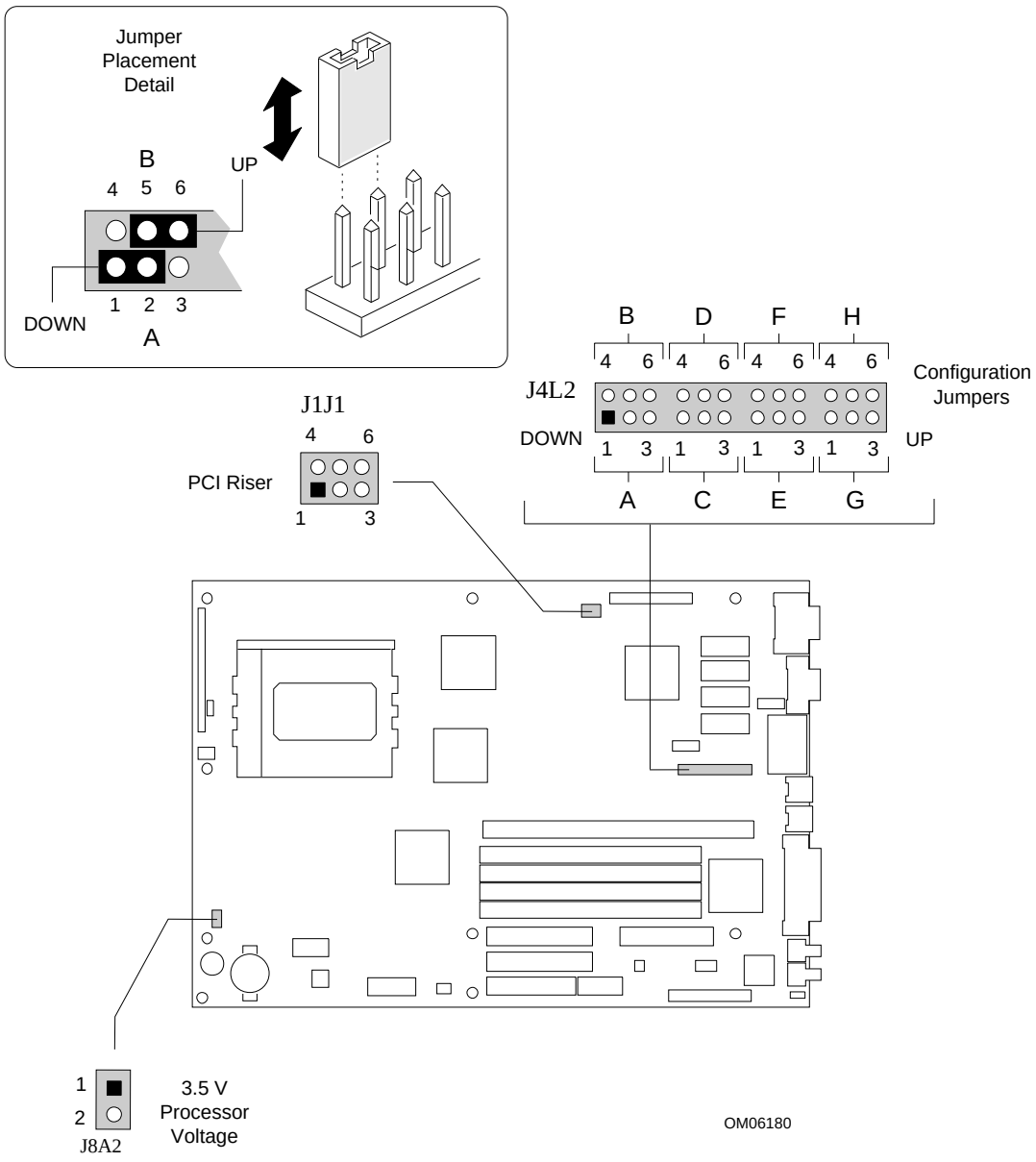

Figure 8. Jumper Locations

1.13.1 Microprocessor Configuration (J4L2)

These allow the motherboard to be switched between different speeds of the Pentium Pro processor. These jumpers also affect the PCI and ISA clock speeds as shown in Table 23.

Table 23. Microprocessor/System Speed Settings

J4L2-A	J4L2-B	J4L2-C	Microprocessor Clock Multiplier	Microprocessor Freq. (MHz)	Host Bus Freq. (MHz)	PCI Bus Freq. (MHz)	ISA Bus Freq. (MHz)
DOWN	DOWN	DOWN	2.5	150	60	30	7.5
DOWN	DOWN	UP	2.5	166	66	33	8.33
DOWN	UP	DOWN	reserved				
DOWN	UP	UP	reserved				
UP	DOWN	DOWN	reserved				
UP	DOWN	UP	reserved				
UP	UP	DOWN	3	180	60	30	7.5
UP	UP	UP	3	200	66	33	8.33

1.13.2 Motherboard Configuration (J4L2, J1J1)

The jumpers for sections D, E, F, G, and H of J4L2 allow the selection of various motherboard features. A second jumper block (J1J1) allows selection of a riser board with either two or three PCI board connectors. A third jumper (J8A2) is used to provide 3.5 V for processors that require that voltage.

⚠ CAUTION

Do not install a jumper on the J8A2 header if you are using a processor that does not require 3.5V. The increased voltage could damage the processor.

Table 24 lists the motherboard configuration jumper positions and indicates the meaning for each position.

Table 24. Configuration Jumper Settings

Function	Jumper	Configuration
FDWPR - Flash Write Protect	J4L2-D, 5-6 J4L2-D, 4-5	UP - ***NOR*** (**Default**), Normal operation DOWN - ***PRT,*** Protect
FLASH - Flash Recover	J4L2-E, 2-3 J4L2-E, 1-2	UP - ***NOR*** (**Default**), Normal operation DOWN - ***REC*** - Enable Top Boot block to recover Flash.
CMOS - Clear CMOS Contents	J4L2-F, 5-6 J4L2-F, 4-5	UP - ***NOR*** (**Default**), Normal operation DOWN - ***CLR***, Clear CMOS content.
PSWCLR - Password Clear Disable/Enable	J4L2-G, 2-3 J4L2-G, 1-2	UP - ***DIS***, Disable DOWN - ***ENA***, Enable system password capability.
SETUP - Setup Enable/Disable	J4L2-H, 5-6 J4L2-H, 4-5	UP - ***ENA***, Enable DOWN - ***DIS***, Disable setup accessibility.
Riser with 2 PCI slots	J1J1, 1-2 and J1J1, 4-5	Enables use of riser card with two (2) PCI slots.
Riser with 3 PCI slots	J1J1, 2-3 and J1J1, 5-6	Enables use of riser card with three (3) PCI slots.
3.5 V Processor Voltage Jumper	J8A2	Installed - 3.5 V Processor. Not Installed - All other processor types.

Note: The text appearing in a ***BOLD-ITALIC*** font duplicates the text of the motherboard silk-screening.

1.14 Reliability

The Mean-Time-Between-Failures (MTBF) data is calculated from predicted data @55 °C in accordance with the *Intel Reliability Policy and Procedures Handbook*.

Motherboard 60239 Hours

1.15 Environmental

Table 25. Motherboard Environmental Specifications

Parameter	Specification
Temperature	
Non-Operating	-40 °C to +70 °C
Operating	+0 °C to +55 °C
DC Voltage	
+3.3 V	±5 %
+5 V	±5 %
-5 V	±5 %
+12 V	±5 %
-12 V	±5 %
Vibration	
Unpackaged	5 Hz to 20 Hz : 0.01g² Hz sloping up to 0.02 g² Hz
	20 Hz to 500 Hz : 0.02g² Hz (flat)
Packaged	10 Hz to 40 Hz : 0.015g² Hz (flat)
	40 Hz to 500 Hz : 0.015g² Hz sloping down to 0.00015 g² Hz

1.16 Power Consumption

Table 26 lists the voltage and current specifications for a hypothetical computer configured with the AP440FX motherboard and the following components: a 200 MHz Pentium Pro processor w/ 256 KB Cache, 16 MB EDO DRAM, 3.5-inch floppy drive, 1.6 GB IDE hard drive, and 4X IDE CD-ROM. The power supply is a 200 watt LPX power supply with at least 65% efficiency. This information is preliminary and is provided only as a guide for calculating **approximate** total power usage with additional resources added.

Table 26. Power Usage

		DC (amps)					
Operating Conditions	**AC (watts)**	**+3.3 V**	**+5 V**	**-5 V**	**+12 V**	**-12 V**	**+5VSB**
APM enabled, idle and running Windows 95 desktop	29.6	400 mA	1.96 A	< 10 mA	240 mA	50 mA	N/A
APM disabled, running Windows 95 SCT AVI test	53.7	410 mA	6.08 A	< 10 mA	240 mA	80 mA	N/A
Computer powered down	N/A	N/A	N/A	N/A	N/A	N/A	< 10 mA

1.16.1 Power Supply Considerations

The AP440FX motherboard is designed to operate with a switching power supply in the PS/2 form-factor with dual line input capability, remote ON/OFF, forced air cooling, standby voltage (VSB), and the following electrical characteristics:

- Power - 200 W maximum peak, 160 W maximum continuous
- Rise time for power supply - 2 ms to 20 ms
- Minimum delay from reset to Powergood - 100ms
- Minimum Powerdown warning - 1 ms

Table 27. DC Voltage

DC Voltage	Acceptable Tolerance	Current Range (amps)	
		Maximum	Minimum
+3.3 V	+5/-3%	14.0	0.3
+5 V	± 5%	18.0	1.0
+5 V SB (standby)	± 5%	0.1	0
-5 V	± 10%	0.3	0
+12 V	± 5%	6.0	0
-12 V	± 10%	0.8	0

1.17 Regulatory Compliance

This printed circuit assembly complies with the following safety and EMI regulations when correctly installed in a compatible host system.

1.17.1 Safety

1.17.1.1 UL 1950 - CSA 950-95, 3rd edition, Dated 07-28-95

The Standard for Safety of Information Technology Equipment including Electrical Business Equipment. (USA & Canada)

1.17.1.2 CSA C22.2 No. 950-93, 3rd Edition

The Standard for Safety of Information Technology Equipment including Electrical Business Equipment. (Canada)

1.17.1.3 EN 60 950, 2nd Edition, 1992 (with Amendments 1, 2 & 3)

The Standard for Safety of Information Technology Equipment including Electrical Business Equipment. (European Union)

1.17.1.4 IEC 950, 2nd edition, 1991 (with Amendments 1, 2 & 3)

The Standard for Safety of Information Technology Equipment including Electrical Business Equipment. (International)

1.17.1.5 EMKO-TSE (74-SEC) 207/94

Summary of Nordic deviations to EN 60 950. (Norway, Sweden, Denmark & Finland)

1.17.2 EMI

1.17.2.1 FCC Class B

Title 47 of the Code of Federal Regulations, Parts 2 & 15, Subpart B, pertaining to unintentional radiators. (USA)

1.17.2.2 CISPR 22, 2nd Edition, 1993

Limits and methods of measurement of Radio Interference Characteristics of Information Technology Equipment. (International)

1.17.2.3 EN 55 022, 1995

Limits and methods of measurement of Radio Interference Characteristics of Information Technology Equipment. (Europe)

1.17.2.4 EN 50 082-1 (1992)

Generic Immunity Standard; Currently compliance is determined via testing to IEC 801-2, -3, and -4. (Europe)

1.17.2.5 VCCI Class 2 (ITE)

Implementation Regulations for Voluntary Control of Radio Interference by Data Processing Equipment and Electronic Office Machines. (Japan)

1.17.2.6 ICES-003, Issue 2

Interference-Causing Equipment Standard, Digital Apparatus. (Canada)

1.17.3 Product Certification Markings

This printed circuit assembly has the following product certification markings:

- European CE Marking: Consists of a marking on the board and shipping container.
- UL Recognition Mark: Consists of the UL File No. E139761 on the component side of the board and the PB No. on the solder side of the board. Board material flammability is 94V-1 or -0.

Canadian Compliance: Consists of small c followed by a stylized backward UR on component side of board.

2 Motherboard Resources

2.1 Memory Map

Table 28. Memory Map

Address Range (Decimal)	Address Range (hex)	Size	Description
1024K-131072K	100000-8000000	127M	Extended Memory
960K-1023K	F0000-FFFFF	64K	AMI BIOS
944K-959K	EC000-EFFFF	16K	Boot Block
936K-943K	EA000-EBFFF	8K	ESCD (Plug and Play configuration area)
932K-935K	E9000-E9FFF	4K	Reserved for BIOS
928K-931K	E8000-E8FFF	4K	OEM LOGO Area
896K-927K	E0000-E7FFF	32K	BIOS Reserved
800-895K	C8000-DFFFF	96K	Available HI DOS memory (open to ISA and PCI bus)
640K-799K	A0000-C7FFF	160K	Video memory and BIOS
639K	9FC00-9FFFF	1K	Extended BIOS Data (moveable by QEMM†, 386MAX†)
512K-638K	80000-9FBFF	127K	Extended conventional
0K-511K	00000-7FFFF	512K	Conventional

2.2 I/O Map

Table 29. I/O Map

Address (hex)	Size	Description	Address (hex)	Size	Description
0000 - 000F	16 bytes	PIIX3 - DMA 1	0376	1 byte	Sec IDE Chan Cmd Port
0020 - 0021	2 bytes	PIIX3 - Interrupt Controller 1	0377	1 byte	Sec IDE Chan Stat Port
002E - 002F	2 bytes	87307 Base Configuration	0378 - 037F	8 bytes	Parallel Port 1
0040 - 0043	4 bytes	PIIX3 - Timer 1	0388 - 038B	4 bytes	CS4236 Audio
0060	1 byte	Keyboard Controller Byte - Reset IRQ	03B0 - 03BB	12 bytes	S3 Virge or Virge/DX
0061	1 byte	PIIX3 - NMI, speaker control	03BC - 03BF	4 bytes	Parallel Port 3
0064	1 byte	Kbd Controller, CMD/STAT Byte	03C0 - 03DF	32 bytes	S3 Virge or Virge/DX
0070, bit 7	1 bit	PIIX3 - Enable NMI	03E8 - 03EF	8 bytes	Serial Port 3
0070, bits 6:0	7 bits	PIIX3 - Real Time Clock, Address	03F0 - 03F5	6 bytes	Floppy Channel 1
0071	1 byte	PIIX3 - Real Time Clock, Data	03F6	1 byte	Pri IDE Chan Cmd Port
0078	1 byte	Reserved - Brd. Config.	03F7 (Write)	1 byte	Floppy Chan 1 Cmd
0079	1 byte	Reserved - Brd. Config.	03F7, bit 7	1 bit	Floppy Disk Chg Chan 1
0080 - 008F	16 bytes	PIIX3 - DMA Page Register	03F7, bits 6:0	7 bits	Pri IDE Chan Status Port
00A0 - 00A1	2 bytes	PIIX3 - Interrupt Controller 2	03F8 - 03FF	8 bytes	Onboard Serial Port 1
00C0 - 00DE	31 bytes	PIIX3 - DMA 2	04D0 - 04D1	2 bytes	Edge/level triggered
00F0-00FF	16 bytes	Math Coprocessor Compatible I/O Registers	LPT + 400h	8 bytes	ECP port, LPT + 400h
0170 - 0177	8 bytes	Secondary IDE Channel	0608 - 060B*	4 bytes	CS4236 Audio
01F0 - 01F7	8 bytes	Primary IDE Channel	0CF8**	1 byte	PCI Config Address Reg.
0200 - 0207	8 bytes	Game Port	0CF9	1 byte	Turbo & Reset control Reg.
0228 - 022F	8 bytes	Parallel Port 3, ECP/EPP Mode	0CFC-0CFF	4 bytes	PCI Config Data Reg
290 - 0297	8 bytes	Management Extension Hardware	0FE0-0FE7	8 bytes	CS4236 Audio
0240-024F	16 bytes	CS4236 Audio	FF00 - FF07	8 bytes	IDE Bus Master Reg.
0278 - 027B	4 bytes	Parallel Port 2	FF80 - FF9F	32 bytes	PCI Universal Serial Bus
02E8-02EF	8 bytes	Serial Port 4	FFA0 - FFA7	8 bytes	IDE primary Channel
02F8 - 02FF	8 bytes	Onboard Serial Port 2	FFA8 - FFAF	8 bytes	IDE secondary channel
0330 - 0331	2 bytes	MPU-401 (MIDI)			

* This is only part of one of the Windows Sound System (WSS) selectable ranges. The defined ranges are 0530-0537, 0604-060B, 0E80-0E87, or 0F40-0F47. Only one of these ranges needs to be used for WSS to work.

** Only by DWORD accesses.

2.3 Soft-Off Control

The motherboard design uses Soft-off control implemented under the SMM code in the BIOS. Any power supply used with the AP440FX motherboard must support the Soft-off feature. The ONCTL# pin of the I/O controller is connected to the Soft-off control line in the power supply circuit. The registers in the I/O controller that set the I/O address and control the ONCTL# pin are not setup until the SMM code is activated.

2.4 PCI Configuration Space Map

Table 30. PCI Configuration Space Map

Bus Number (hex)	Dev Number (hex)	Function Number (hex)	Description
00	00	00	Intel 82440FX (PMC) Host Bridge
00	07	00	Intel 82371SB (PIIX3) ISA bridge
00	07	01	Intel 82371SB (PIIX3) IDE Controller
00	07	02	Intel 82371SB (PIIX3) USB
00	08	00	Video Controller
00	13	00	PCI Expansion Slot: user available
00	11	00	PCI Expansion Slot: user available
00	0B	00	PCI Expansion Slot: Optional PCI Expansion Slot for 3 slot Riser

2.5 DMA Channels

Table 31. DMA Channels

DMA	Data Width	Resource
0	8- or 16-bits	Open
1	8- or 16-bits	Audio
2	8- or 16-bits	Floppy
3	8- or 16-bits	Parallel Port (for ECP/EPP Config.)
4		Reserved - Cascade channel
5	16-bits	Open
6	16-bits	Open
7	16-bits	Open

2.6 Interrupts

Table 32. Interrupts

IRQ	Resource
NMI	I/O Channel Check
0	Reserved, Interval Timer
1	Reserved, Keyboard buffer full
2	Reserved, Cascade interrupt from slave PIC
3	Serial Port 2
4	Serial Port 1
5	Audio - Codec
6	Floppy
7	Parallel Port 1
8	Real Time Clock
9	Audio - FM Synthesis
10	USB
11	Video
12	Onboard Mouse Port if present, else user available
13	Reserved, Math coprocessor
14	Primary IDE if present, else user available
15	Secondary IDE if present, else user available

3 Motherboard BIOS and Setup Utility

3.1 Introduction

The AP440FX motherboard uses an Intel BIOS, which is stored in flash memory and easily upgraded using a floppy disk-based program. In addition to the Intel BIOS, the flash memory also contains the Setup utility, Power-On Self Tests (POST), APM 1.2, the PCI auto-configuration utility, and Windows 95 ready Plug and Play 1.0a. This motherboard also supports BIOS shadowing, allowing the BIOS to execute from 64-bit onboard write-protected DRAM.

The BIOS displays a sign-on message during POST identifying the type of BIOS and a five-digit revision code. The initial production BIOS in the motherboard is identified as 1.00.01.CT1.

3.2 BIOS Flash Memory Organization

The Intel PA28FB002BX 2 MB flash component is organized as 256K x 8 (256 KB). The flash device is divided into seven areas, as described in Table 33.

Table 33. Flash Memory Organization

Address		Flash Memory Area
FFFF0000H	FFFFFFFFH	64 KB Main BIOS
FFFEC000H	FFFEFFFFH	16 KB Boot block (Not flash erasable)
FFFEA000H	FFFEBFFFH	8 KB ESCD Area (Plug and Play data storage area)
FFFE9000H	FFFE9FFFH	4 KB Reserved for BIOS
FFFE8000H	FFFE8FFFH	4 KB OEM Logo Area
FFFE0000H	FFFE7FFFH	32 KB Reserved for BIOS
FFFD0000H	FFFDFFFFH	64 KB Reserved for BIOS
FFFC0000H	FFFCFFFFH	64 KB Reserved for BIOS

3.3 BIOS Upgrades

Flash memory makes distributing BIOS upgrades easy. A new version of the BIOS can be installed from a diskette. BIOS upgrades are available to be down loaded from the Intel Applications Support web site at *http://www-cs.intel.com/oem_developer/motherbd/*, or from Intel's FTP site at *ftp://ftp.intel.com/pub/bios/*. Be sure to have the BIOS identification that applies to this motherboard.

The disk-based Flash upgrade utility, FMUP.EXE, has three options for BIOS upgrades:

- The Flash BIOS can be updated from a file on a disk.
- The current BIOS code can be copied from the Flash EEPROM to a disk file as a backup in the event that an upgrade cannot be successfully completed.
- The BIOS in the Flash device can be compared with a file to ensure the computer has the correct version.

The upgrade utility ensures the upgrade BIOS extension matches the target computer to prevent accidentally installing a BIOS for a different type of computer.

3.4 PCI IDE Support

The two local bus IDE connectors with independent I/O channel support are setup up automatically by the BIOS if the user selects "Autoconfiguration" in Setup. The IDE interface supports PIO Mode 3, and Mode 4 hard drives and recognition of ATAPI CD-ROMs, tape drives, and any other ATAPI devices. The BIOS determines the capabilities of each drive and configures them to optimize capacity and performance. For the high capacity hard drives typically available, the drive is automatically configured for Logical Block Addressing (LBA) for maximum capacity and to PIO Mode 3 or 4 depending on the capability of the drive. The user can override the auto-configuration options by using the manual mode setting. The ATAPI Specification Revision 2.5 recommends that an ATAPI device be configured as shown in Table 34.

Table 34. Recommendations for Configuring an ATAPI Device

Primary Cable		Secondary Cable		
Drive 0	Drive 1	Drive 0	Drive 1	
ATA				Normal, no ATAPI
ATA		ATAPI		Disk and CD-ROM for enhanced IDE systems
ATA	ATAPI			Legacy IDE System with only one cable
ATA		ATAPI	ATAPI	Enhanced IDE with CD-ROM and a tape or two CD-ROMs

3.5 PCI Auto-Configuration

The PCI auto-configuration utility operates in conjunction with the Setup utility to allow the insertion and removal of PCI cards without user intervention (Plug and Play). When the computer is turned on after adding a PCI add-in card, the BIOS automatically configures interrupts, I/O space, and other parameters. PCI interrupts are distributed to available ISA interrupts that have not been assigned to an ISA card, or other resources. Those interrupts left set to "available" in Setup are considered free for PCI add-in card use.

The PCI Auto-Configuration function complies with version 2.10 of the PCI BIOS specification. Configuration information is stored in ESCD format. The ESCD data may be cleared (i.e., "write protection" is removed) by setting the CMOS clear jumper to the DOWN (CLR) position.

PCI specification 2.1 for add-in card auto-configuration is also a part of the Plug and Play BIOS. Peer-to-peer hierarchical PCI Bridge 1.0 is supported, and by using an OEM supplied option ROM or TSR, a PCI-to-PCMCIA bridge capability is possible as well.

3.6 ISA Plug and Play

The BIOS incorporates ISA Plug and Play capabilities as delivered by Plug and Play Release 1.0A (Plug and Play BIOS V.. 1.0A, ESCD V.. 1.03). When used in conjunction with the ISA Configuration Utility (ICU) for DOS or Windows 3.x, the computer allows auto-configuration of Plug and Play ISA cards, PCI cards, and resource management for legacy ISA cards. Because the BIOS supports configuring devices across PCI bridges, release 1.41 or greater of the ICU must be used with the motherboard to properly view and change settings. Configuration information is stored in ESCD format. The ESCD data may be cleared (i.e., "write protection" is removed) by setting the CMOS clear jumper to the DOWN (CLR) position.

The BIOS also has a setup option to support the Windows 95 run time Plug and Play utilities. When this option is selected, only devices critical to booting are assigned resources by the BIOS. Device Node information is available for all devices to ensure compatibility with Windows 95.

Copies of the Intel Architecture Laboratory (IAL) Plug and Play specification may be obtained from the Intel World Wide Web site at *http://www.intel.com/IAL/plugplay/*.

3.7 Desktop Management Interface (DMI)

DMI is a method of managing computers in an enterprise. The main component of DMI is the Management Information Format Database (MIF), which contains information about the computer and its components. Using DMI, a system administrator can obtain the types, capabilities, operational status, installation date and other information about the computer's components. The DMI specification requires that certain information about the motherboard be made available to an applications program. This user-defined information is located in a series of data structures which are accessed in various ways by means of the DMI service layer. Component instrumentation allows the service layer to gain access to the information stored in the GPNV. The included MIF database defines the data and provides the method for accessing the information.

The AP440FX BIOS provides the first stage of DMI v. 2.0 support, including static system configuration information, including motherboard and peripheral data. Future AP440FX product releases will provide event detection and error logging, achieving the maximum benefit of DMI with applications such as LANDesk Client Manager from Intel.

3.8 Advanced Power Management (APM)

This section describes the use of System Management Mode (SMM) by the BIOS. The BIOS supports APM version 1.2. APM is enabled in BIOS by default; however, the computer must be configured with an APM driver to utilize the system power saving features. Windows 95 enables APM automatically upon detecting the presence of the APM BIOS.

The energy saving Standby mode can be initiated by one of the following:

- a keyboard hot-key sequence set by the user
- a time-out period set by the user
- a suspend/resume button tied to the front panel sleep connector.

When in Standby mode, the motherboard reduces power consumption by utilizing the Pentium Pro processor's SMM capabilities and also spinning down hard drives and turning off VESA DPMS compliant monitors. The user may select which DPMS mode (Standby, Suspend, or Off) to send to the monitor in Setup. The ability to respond to external interrupts is fully maintained while in Standby mode allowing the system to service requests such as an in-coming fax or network message while unattended. Any keyboard or mouse activity brings the system out of the energy saving Standby mode. When this occurs the monitor and IDE drives are turned back on immediately.

Because SMM uses its own address space, the pointers to interrupt service routines in protected mode do not necessarily point to the executable interrupt service routines when the processor goes into SMM. Interrupts are disabled upon entry into SMM. Any program that wants to use interrupts during SMM must provide a valid interrupt service routine and place a pointer to it in an interrupt descriptor table before renabling interrupts.

Windows 95 places an Energy Star compliant monitor in video standby mode after a period of system inactivity. Windows 95 uses the motherboard BIOS to put the processor into SMM. The motherboard BIOS in turn invokes the video BIOS to place the monitor into standby mode. Some video BIOSes reenable interrupts when they are called but do not ensure that a valid interrupt service routine is available. If the video BIOS then generates a hardware or software interrupt while the system is in SMM, in most cases the system will lock up.

3.9 Advanced Power Control (APC)

The BIOS supports APC through the National 87307 Super I/O controller. Two features that have been implemented are Auto Start On AC Loss and Power-On COM1 Ring. Auto Start On AC Loss sets the control for returning to the last known state of the computer, or powering down upon AC power loss to the motherboard. Power-On COM1 Ring sets the control for allowing the computer to be powered on upon an incoming POTS call to a telephony device configured for operation on COM1.

3.10 Language Support

The BIOS setup screen and help messages are supported in 32 languages. There are 5 languages available at this time: American English, German, Italian, French, and Spanish. Translation to other languages may become available at a later date.

3.11 Boot Options

Booting from CD-ROM is supported in adherence to the "El Torito" v. 1.0 bootable CD-ROM format specification developed by Phoenix Technologies and IBM. Under the *Boot Options* field in Setup, *CD-ROM* is one of four possible boot devices which are defined in priority order. The default setting is for floppy to be the primary boot device and hard drive to be the secondary boot device. If CD-ROM is selected, it must be the first device. The third and fourth devices are set to *disabled* in the default configuration. The user can add also select *network* as a boot device. The network option allows booting from a network add-in card with a remote boot ROM installed.

NOTE

A copy of "El Torito" v. 1.0 is available on the Phoenix Web page (http://www.ptltd.com/techs/specs.html).

3.12 Flash LOGO Area

The motherboard supports a 4 KB programmable flash user area located at E8000-E8FFF. An OEM may use this area to display a custom logo. The BIOS accesses the user area just after completing POST. A utility is available from Intel to assist with installing a logo into flash for display during POST. Contact your local Intel Sales office or authorized distributor for further information.

3.13 Setup Enable Jumper

A motherboard configuration jumper controls access to the BIOS Setup utility. By setting the jumper to the disable position, the user is prevented from accessing the Setup utility during the POST or at any other time. The message prompting the user to press <F1> to enter Setup is also disabled.

3.14 Overview of the Setup Menu Screens

The Setup program initially displays the Main menu screen. In each screen there are options for modifying the computer's configuration. Select a menu screen by pressing the left <←> or right <→> arrow keys. Use the up <↑> or down <↓> arrow keys to select items in a screen. Use the <Enter> key to select an item for modification. For certain items, pressing <Enter> brings up a subscreen. After you have selected an item, use the arrow keys to modify the setting.

Table 35. Overview of the Setup Menu Screens

Setup Menu Screen	Description
Main	Set up and modify some of the basic options of a PC, such as time, date, diskette drives, hard drives.
Advanced	Modify the more advanced features of a PC, such as peripheral configuration and advanced chipset configuration.
Security	Specify passwords that can be used to limit access to the computer.
Exit	Save or discard changes.
Setup Subscreen	**Description**
Floppy Options	Configure your diskette drives.
IDE Device Configuration	Configure your IDE devices.
Boot Options	Modify options that affect boot up, such as the boot sequence.
Peripheral Configuration	Modify options that affect the serial ports, the parallel port, and the disk drive interfaces.
Advanced Chipset Configuration	Modify options that affect memory and system busses.
Power Management Configuration	Access and modify APM options.
Plug and Play Configuration	Modify options that affect the computer's Plug and Play capabilities.
Event Logging Configuration	Modify options that affect the computer's ability to log events such as parity/ECC errors, POST errors, and system limit errors.

3.14.1 Main BIOS Setup Screen

This section describes the Setup options found on the main menu screen. If you select certain options from the main screen (e.g., Hard Disk), the Setup program switches to a subscreen for the selected option.

3.14.1.1 System Date

Specifies the current date. Select the month from a pop-up menu.

3.14.1.2 System Time

Specifies the current time.

3.14.1.3 Floppy Options

When selected, this brings up the Floppy Options menu.

3.14.1.4 Primary IDE Master

Reports if an IDE device is connected to the computer. When selected, this brings up the IDE Device Configuration subscreen.

3.14.1.5 Primary IDE Slave

Reports if an IDE device is connected to the computer. When selected, this brings up the IDE Device Configuration subscreen.

3.14.1.6 Secondary IDE Master

Reports if an IDE device is connected to the computer. When selected, this brings up the IDE Device Configuration subscreen.

3.14.1.7 Secondary IDE Slave

Reports if an IDE device is connected to the computer. When selected, this brings up the IDE Device Configuration subscreen.

3.14.1.8 Language

Specifies the language of the text strings used in the Setup program and the BIOS. The options are any installed languages.

3.14.1.9 Boot Options

When selected, this brings up the Boot Options subscreen.

3.14.1.10 Video Mode

Reports the video mode. There are no options.

3.14.1.11 Mouse

Reports if a PS/2 mouse is installed or not. There are no options.

3.14.1.12 Base Memory

Reports the amount of base memory. There are no options.

3.14.1.13 Extended Memory

Reports the amount of extended memory. There are no options.

3.14.1.14 BIOS Version

Reports the BIOS identification string. There are no options.

3.14.2 Floppy Options Subscreen

3.14.2.1 Floppy A:

Reports if a floppy drive is connected to the computer. There are no options.

3.14.2.2 Floppy B:

Reports if a second floppy drive is connected to the computer. There are no options.

3.14.2.3 Floppy A: Type

Specifies the physical size and capacity of the floppy drive. The options are:

- Disabled
- 360 KB, 5.25-inch
- 1.2 MB, 5.25-inch
- 720 KB, 3.5-inch
- **1.44/1.25 MB, 3.5-inch (default)**
- 2.88 MB, 3.5-inch.

3.14.2.4 Floppy B: Type

Specifies the physical size and capacity of the floppy drive. The options are:

- **Disabled (default)**
- 360 KB, 5.25-inch
- 1.2 MB, 5.25-inch
- 720 KB, 3.5-inch
- 1.44/1.25 MB, 3.5-inch
- 2.88 MB, 3.5-inch

3.14.3 IDE Device Configuration Subscreen

There are separate configuration subscreens for the Primary IDE Master, Primary IDE Slave, Secondary IDE Master and Secondary IDE Slave devices.

3.14.3.1 IDE Device Configuration

Used to manually configure the IDE device or have the computer auto configure it. The options are:

- **Auto Configured (default)**
- User Definable
- Disabled

If you select User Definable then the Number of Cylinders, Number of Heads, and Number of Sectors items can be modified.

3.14.3.2 Cylinders

If IDE Device Configuration is set to User Definable, you must type the correct number of cylinders for your IDE device.

If IDE Device Configuration is set to Auto Configured, this reports the number of cylinders for your IDE device and cannot be modified.

3.14.3.3 Heads

If IDE Device Configuration is set to User Definable, you must type the correct number of heads for your IDE device.

If IDE Device Configuration is set to Auto Configured, this reports the number of heads for your IDE device and cannot be modified.

3.14.3.4 Sectors

If IDE Device Configuration is set to User Definable, you must type the correct number of sectors for your IDE device.

If IDE Device Configuration is set to Auto Configured, this reports the number of sectors for your IDE device and cannot be modified.

3.14.3.5 Maximum Capacity

Reports the maximum capacity of your IDE device. It is calculated from the number of cylinders, heads, and sectors. There are no options.

3.14.3.6 IDE Translation Mode

Specifies the IDE translation mode. The options are:

- Standard CHS (standard cylinder head sector–less than 1024 cylinders)
- Logical Block
- Extended CHS (extended cylinder head sector–greater than 1024 cylinders)
- **Auto Detected (BIOS detects IDE drive support for LBA) (default)**

⚠ CAUTION

Do not change the IDE Translation Mode from the option selected when the hard drive was formatted. Changing the option can result in corrupted data.

3.14.3.7 Multiple Sector Setting

Sets the number of sectors transferred by an IDE drive per interrupt generated. The options are:

- Disabled
- 4 Sectors/Block
- 8 Sectors/Block
- **Auto Detected (default)**

Check the specifications for your IDE device drive to determine which setting provides optimum performance for your drive.

3.14.3.8 Fast Programmed I/O Modes

Sets how fast transfers on the IDE interface occur. The options are:

- Disabled
- **Auto Detected (default)**

If set to Disabled, transfers occur at a less than optimized speed. If set to Auto Detected, transfers occur at the drive's maximum speed.

3.14.4 Boot Options Subscreen

This section describes the options available on the Boot Options subscreen.

3.14.4.1 First Boot Device

Sets which drive the computer checks first to find a bootable operating system. The options are:

- Disabled
- **Floppy** (**default**)
- Hard Disk
- CD-ROM
- Network

3.14.4.2 Second Boot Device

Sets which drive the computer checks second to find a bootable operating system. The options are:

- Disabled
- Floppy
- **Hard Disk** (**default**)
- Network

3.14.4.3 Third Boot Device

Sets which drive the computer checks third to find a bootable operating system. The options are:

- **Disabled (default)**
- Floppy
- Hard Disk
- Network

3.14.4.4 Fourth Boot Device

Sets which drive the computer checks fourth to find a bootable operating system. The options are:

- **Disabled (default)**
- Floppy
- Hard Disk
- Network

3.14.4.5 System Cache

Enables or disables both the primary and the secondary cache memory. The options are:

- Disabled
- **Enabled (default)**

3.14.4.6 Boot Speed

Sets the boot speed. The options are:

- Deturbo
- **Turbo (default)**

If Turbo is selected, boot-up occurs at full speed. If Deturbo is selected, the board operates at a slower speed.

3.14.4.7 Num Lock

Sets the state of the Num Lock feature on your keyboard when you boot. The options are:

- **Off (default)**
- On

3.14.4.8 Setup Prompt

Turns on (or off) the "Press <F1> Key if you want to run Setup" prompt during the power-up sequence. The options are:

- Disabled
- **Enabled (default)**

NOTE

This option has no effect on your ability to access the Setup program. It only toggles the prompt.

3.14.4.9 Hard Disk Pre-Delay

Sets the hard disk drive pre-delay. The options are:

- **Disabled (default)**
- 3 seconds
- 6 seconds
- 9 seconds
- 12 seconds
- 15 seconds
- 21 seconds
- 30 seconds

When enabled, this option causes the BIOS to wait the specified time before it accesses the first hard drive.

If your computer contains a hard drive, and you don't see the drive type displayed during boot-up, the hard drive may need more time before it is able to communicate with the controller. Setting a pre-delay provides additional time for the hard drive to initialize.

3.14.4.10 Typematic Rate Programming

Sets the typematic rates. The options are:

- **Default (default)**
- Override

Choosing Override enables the Typematic Rate Delay and Typematic Rate setup options.

3.14.4.11 Typematic Rate Delay

Sets how long it takes (in milliseconds) for the key-repeat function to start when you hold down a key on the keyboard. The options are:

- **250 msec (default)**
- 500 msec
- 750 msec
- 1000 msec

If Typematic Rate Programming is set to Default, this option is not visible.

3.14.4.12 Typematic Rate

Sets the speed (in characters per second) at which characters repeat when you hold down a key on the keyboard. The higher the number, the faster the characters repeat. The options are:

- **6 char/sec (default)**
- 8 char/sec
- 10 char/sec
- 12 char/sec
- 15 char/sec
- 20 char/sec
- 24 char/sec
- 30 char/sec

If Typematic Rate Programming is set to Default, this option is not visible.

3.14.4.13 Scan User Flash Area

Scans the user Flash area for ROMs. The options are:

- Disabled
- **Enabled (default)**

3.14.4.14 Quick Mode

Enables the user to speed up the boot process. The options are:

- **Disabled (default**)
- Enabled

3.14.5 Advanced Screen

This section describes the Setup options found on the Advanced menu screen. If you select certain options from the Advanced screen (e.g., Peripheral Configuration), the Setup program switches to a subscreen for the selected option. Subscreens are described in the sections following the description of the Advanced screen options.

3.14.5.1 Processor Type

Reports the microprocessor type. There are no options.

3.14.5.2 Processor Speed

Reports the microprocessor clock speed. There are no options.

3.14.5.3 Cache Size

Reports the size of the secondary cache. There are no options. If your computer contains no L2 cache, this item does not appear.

3.14.5.4 Peripheral Configuration

When selected, this brings up the Peripheral Configuration subscreen.

3.14.5.5 Advanced Chipset Configuration

When selected, this brings up the Advanced Chipset Configuration subscreen.

3.14.5.6 Power Management Configuration

When selected, this brings up the Power Management subscreen.

3.14.5.7 Plug and Play Configuration

When selected, this brings up the Plug and Play Configuration subscreen.

3.14.6 Event Logging Configuration

This section describes the options available in the Event Logging Configuration subscreen.

3.14.7 Peripheral Configuration Subscreen

This section describes the screens for the peripheral configuration subscreen.

3.14.7.1 Primary PCI IDE Interface

Enables or disables the Primary PCI IDE interface. The options are:

- Disabled
- **Auto Configured (default)**

3.14.7.2 Secondary PCI IDE Interface

Enables or disables the Secondary PCI IDE interface. The options are:

- Disabled
- **Auto Configured (default)**

3.14.7.3 Floppy Interface

Enables or disables the diskette drive interface. The options are:

- Disabled
- Enabled
- **Auto Configured (default)**

3.14.7.4 Serial Port 1 Interface

Configures serial port 1. The options are described and listed in Table 36. The default option is Auto Configured.

If the Configuration Mode is set to Auto Configured, the Setup program assigns the first free COM port (normally COM1, 3F8h) to serial port 1.

Table 36. Serial Port Configuration Options

Option	Description
Disable	Port not enabled
COM1, 3F8, IRQ4	Enabled as COM1 at indicated I/O address and IRQ
COM2, 2F8, IRQ3	Enabled as COM2 at indicated I/O address and IRQ
COM3, 3E8, IRQ4	Enabled as COM3 at indicated I/O address and IRQ
COM4, 2E8, IRQ3	Enabled as COM4 at indicated I/O address and IRQ
COM1, 3F8, IRQ3	Enabled as COM1 at indicated I/O address and IRQ
COM2, 2F8, IRQ4	Enabled as COM2 at indicated I/O address and IRQ
COM3, 3E8, IRQ3	Enabled as COM3 at indicated I/O address and IRQ
COM4, 2E8, IRQ4	Enabled as COM4 at indicated I/O address and IRQ
Auto Configured	**Port will be auto configured (Default option)**

3.14.7.5 Serial Port 2 Address

Configures serial port 2. The options are described and listed in Table 36. The default option is Auto Configured. If the Configuration Mode is set to Auto Configured, the Setup program assigns the first free COM port (normally COM2, 2F8h) to serial port 2.

NOTE

If either serial port address is set, the address it is set to does not appear in the options dialog box of the other serial port.

3.14.7.6 Serial Port 2 IR Mode

Makes Serial Port 2 available to infrared applications. The options are:

- **Disabled (default**)
- Enabled

3.14.7.7 Parallel Port Interface

Selects the address and IRQ of the parallel port. The options are described and listed in Table 37.

If the Configuration Mode is set to Auto Configured, the Setup program assigns LPT1, 378h, IRQ7 to the parallel port.

Table 37. Parallel Port Configuration Options

Option	Description
Disabled	Port not enabled
LPT3, 3BC, IRQ7	Enabled as LPT3 at indicated I/O address and IRQ
LPT1, 378, IRQ7	Enabled as LPT1 at indicated I/O address and IRQ
LPT2, 278, IRQ7	Enabled as LPT2 at indicated I/O address and IRQ
LPT3, 3BC, IRQ5	Enabled as LPT3 at indicated I/O address and IRQ
LPT1, 378, IRQ5	Enabled as LPT1 at indicated I/O address and IRQ
LPT2, 278, IRQ5	Enabled as LPT2 at indicated I/O address and IRQ
Auto Configured	**Port will be auto configured (Default option)**

3.14.7.8 Parallel Port Type

Selects the mode for the parallel port. The options are:

- **Compatible (default)**
- Bi-directional
- ECP
- EPP

Compatible means the parallel port operates in AT-compatible mode. Bi-directional means the parallel port operates in bi-directional PS/2-compatible mode. EPP and ECP mean the parallel port operates high-speed, bi-directionally.

Table 38 lists and describes the options that are available if the parallel port mode is ECP.

Table 38. ECP - Compatible Configuration Options

Option	Description
Disable	Port not enabled
LPT1, 378, IRQ7, DMA3	Enabled as LPT1 at indicated I/O address, IRQ, and DMA channel.
LPT2, 278, IRQ7, DMA3	Enabled as LPT2 at indicated I/O address, IRQ, and DMA channel.
LPT1, 378, IRQ5, DMA3	Enabled as LPT1 at indicated I/O address, IRQ, and DMA channel.
LPT2, 278, IRQ5, DMA3	Enabled as LPT2 at indicated I/O address, IRQ, and DMA channel.
LPT1, 378, IRQ7, DMA1	Enabled as LPT1 at indicated I/O address, IRQ, and DMA channel.
LPT2, 278, IRQ7, DMA1	Enabled as LPT2 at indicated I/O address, IRQ, and DMA channel.
LPT1, 378, IRQ5, DMA1	Enabled as LPT1 at indicated I/O address, IRQ, and DMA channel.
LPT2, 278, IRQ5, DMA1	Enabled as LPT2 at indicated I/O address, IRQ, and DMA channel.
LPT3, 228, IRQ7, DMA3	Enabled as LPT3 at indicated I/O address, IRQ, and DMA channel.
LPT3, 228, IRQ5, DMA3	Enabled as LPT3 at indicated I/O address, IRQ, and DMA channel.
LPT3, 228, IRQ7, DMA1	Enabled as LPT3 at indicated I/O address, IRQ, and DMA channel.
LPT3, 228, IRQ5, DMA1	Enabled as LPT3 at indicated I/O address, IRQ, and DMA channel.
Auto Configured	**Port will be auto configured (default option)**

3.14.7.9 USB Interface

Enables or disables the USB interface. The options are:

- Disabled
- **Enabled default)**

3.14.7.10 Audio Interface

Enables or disables the onboard audio subsystem. The options are:

- Disabled
- **Enabled (frees the I/O resources and addresses used to support the audio interface) (default)**

3.14.7.11 Hardware Monitor Interface

Enables or disables the Hardware Monitor Controller. The options are:

- Disabled
- **Enabled (default)**

3.14.7.12 Primary PCI IDE Status

Displays the current status of the Primary PCI IDE Interface from the selectable setting above. This is an informational field and is not accessible.

3.14.7.13 Secondary PCI IDE Status

Displays the current status of the Secondary PCI IDE Interface from the selectable setting above. This is an informational field and is not accessible.

3.14.7.14 Floppy Status

Reports the current status of the floppy drive from the selectable setting above. There are no options.

3.14.7.15 Serial Port 1 Status

Reports the current status of serial port 1 from the selectable setting above. There are no options.

3.14.7.16 Serial Port 2 Status

Reports the current status of serial port 2 from the selectable setting above. There are no options.

3.14.7.17 Parallel Port Status

Reports the current status of the parallel port from the selectable setting above. There are no options.

3.14.8 Advanced Chipset Configuration Subscreen

This section describes the options available on the Advanced Chipset Configuration Subscreen.

3.14.8.1 Base Memory Size

Sets the size of the base memory. The options are:

- 512 KB
- **640 KB (default)**

3.14.8.2 ISA LFB Size

Sets the size of the linear frame buffer. The options are:

- **Disabled (default)**
- 1 MB

If this is set to 1 MB, the ISA LFB Base Address field appears.

3.14.8.3 ISA LFB Base Address

Reports the base address of the LFB. There are no options.

The base address is 16 MB minus the ISA LFB size value. This field does not appear if the ISA LFB Size is set to Disabled.

3.14.8.4 Onboard Video IRQ

Enables or disables the onboard video IRQ. The options are:

- **Disabled (default)**
- Enabled

3.14.8.5 Video Palette Snoop

Controls the ability of a primary PCI graphics controller to share a common palette with an ISA add-in video card. Some add-in cards that use the VESA feature connector might need this feature enabled. The options are:

- **Disabled (default)**
- Enabled

3.14.8.6 ISA VGA Write Combining

Enables or disables the ISA VGA write combining. Enabling this feature provides faster video performance by combining processor writes to video memory. The options are:

- Disabled
- **Enabled (default)**

3.14.8.7 Latency Timer (PCI Clocks)

Sets the length of time (in PCI clocks) an agent on the PCI bus can hold the bus when another agent has requested the bus. The options are:

- **Auto Configured (default)**
- 16
- 24
- 32
- 40
- 48
- 56
- 64
- 72
- 80
- 88
- 96
- 104
- 112
- 120
- 128

3.14.8.8 Memory Error Detection

Sets the type of error detection or correction. The options are:

- **Disabled (default)**
- ECC
- Parity

This field appears if either ECC or Parity SIMMs are detected. Parity and ECC SIMMs can be configured to run either as Parity or ECC (e.g. Parity SIMMs may be configured to run in ECC mode.)

3.14.8.9 Bank 0

Reports the type of memory found in the Bank 0 SIMM slots. There are no options.

3.14.8.10 Bank 1

Reports the type of memory found in the Bank 1 SIMM slots. There are no options.

3.14.9 Power Management Configuration Subscreen

This section describes the options available on the Power Management Subscreen.

3.14.9.1 Advanced Power Management (APM)

Enables or disables the APM support in your computer's BIOS. The options are:

- Disabled
- **Enabled (default)**

Power Management only works with APM-capable operating systems to manage power consumption in your computer.

3.14.9.2 IDE Drive Power Down

Spins down IDE drives when the computer goes into power managed mode. The options are:

- Disabled
- **Enabled (default)**

This field does not appear if APM is disabled.

3.14.9.3 VESA Video Power Down

Sets any VESA compliant monitor to be power managed when the computer goes into power managed mode. The options are:

- Disabled
- Standby
- Suspend
- **Sleep (default)**

This field does not appear if APM is disabled.

3.14.9.4 Inactivity Timer (Minutes)

Sets how long the computer must be inactive before it enters power managed mode. Enter the number of minutes. The range is 0 to 255 minutes. **The default is 10 minutes.**

This field does not appear if APM is disabled.

3.14.9.5 Hot Key (CTRL - ALT-)

Sets the hot key that, when pressed while holding down the <Ctrl> and <Alt> keys, causes the computer to enter power managed mode. All alphanumeric keys are valid.

This field does not appear if APM is disabled.

3.14.9.6 Auto Start On AC Loss

Enables returning to the last known state of the computer, or powering down upon AC power loss to the motherboard. The options are:

- Disabled
- **Enabled (default)**

3.14.9.7 Power-On COM1 Ring

Enables the computer to power on upon an incoming POTS call to a telephony device configured for operation on COM1. The options are:

- **Disabled (default)**
- Enabled

3.14.10 Plug and Play Configuration Subscreen

This section describes the options found on the Plug and Play configuration subscreen.

3.14.10.1 Configuration Mode

Sets how the BIOS gets information about ISA cards that do not have Plug and Play capabilities. The options are:

- Use BIOS Setup
- **Use PnP OS (default)**

If Use PnP OS is selected, the BIOS will depend on run-time software to ensure that there are no conflicts between ISA boards with Plug and Play capabilities and those without. Only the Boot With PnP OS will be visible.

3.14.10.2 PnP OS

Enables the computer to select the type of PnP OS to boot from. The options are:

- Disabled
- Other PnP OS
- **Windows 95 (default)**

3.14.10.3 ISA Shared Memory Size

Sets a range of memory addresses that will be directed to the ISA bus rather than on-board memory. The options are:

- **Disabled (default)**
- 16 KB
- 32 KB
- 48 KB
- 64 KB
- 80 KB
- 96 KB

If this is set to Disabled, the ISA Shared Memory Base Address (described below) will not be visible.

This field should be set to Enabled only when a non Plug and Play ISA card (legacy card) that requires non-ROM memory space is used. LAN cards that have on-board memory buffers are one example of this; video capture cards that have video buffer memory are another.

By default, allocation of upper memory is as follows: memory from C0000-C7FFF is automatically shadowed. (This memory range is typically reserved for video BIOS.) Memory from C8000-DFFFFh is initially unshadowed. The BIOS scans this range for any ISA expansion card BIOS that may be present and notes the location and size. The BIOS will then autoconfigure the PCI and Plug and Play devices, shadowing the ROM requirements (other than video) into the area above E0000h until that area is full. It will then assign additional PCI and Plug and Play expansion cards to the area between C8000h and DFFFFh. If an ISA legacy card has non-ROM memory requirements, the autoconfigure routine may write into an area that is needed by the ISA expansion card. The ISA Shared Memory Size parameter signifies the autoconfigure routine that this block of memory is reserved and should not be shadowed.

Shadowing is a technique that copies a block of memory from an add-in card's ROM to the same address in system memory. This provides faster access and achieves higher performance. By default, all upper memory is shadowed.

3.14.10.4 ISA Shared Memory Base Address

Sets the base address for the ISA Shared Memory. The options are:

- **C8000h (default)**
- CC000h
- D0000h
- D4000h
- D8000h
- DC000h

This setting could affect the ISA Shared Memory Size item. The value entered in the ISA Shared Memory Size item cannot extend to the E0000h address.

For example, if a size of 64K is selected, options D4000h, D8000h, and DC000h are not available. If the ISA Shared Memory Size is set to Disabled, this field will not appear.

3.14.10.5 IRQ 3, 4, 5, 7, 9, 10, 11, 12, 14, 15

Sets the status of the IRQ. The options are:

- **Available (default)**
- Used By ISA Card

The PCI auto-configuration code looks here to see if these interrupts are available for use by a PCI or Plug and Play device.

If an interrupt is available, the PCI auto-configuration code or the PnP configuration agent can assign the interrupt to be used by the PCI or PnP device.

If your computer contains a legacy ISA agent that uses one of these interrupts, select Used By ISA Card for that interrupt. This lets PCI and PnP cards know that the marked interrupts are not available for their use.

NOTE

IRQ 3, 4, 5, and 7 may not be available in this option, depending on the setting chosen for the COM1, COM2 and parallel ports in the Peripheral Configuration Subscreen. IRQ 14 and 15 may not be available if the Primary and Secondary IDE ports are enabled.

3.14.11 Event Logging Configuration

This section describes the options available in the Event Logging Configuration subscreen.

3.14.11.1 Event Log Capacity

This information field tells whether the log is full.

3.14.11.2 Event Count Granularity

Defines the number of log events that must occur before the event log is updated. The default is 10 events.

3.14.11.3 Event Time Granularity (Minutes)

Defines the amount of time that must pass before the event log is updated. The default is 30 minutes.

3.14.11.4 Event Log Control

Allows users to enable or disable event logging. The options are:

- **All Events Enabled (default)**
- ECC Events Disabled
- All Events Disabled

3.14.11.5 Clear Event Log

Sets a flag that clears the event log on the next pass through the POST. The options are:

- **Keep (default)**
- On Next Boot

3.14.11.6 Mark Existing Events as Read

Marks all events already in the log as having been not read (Do Not Mark) or read (Mark). The options are:

- **Do Not Mark (default)**
- Mark

3.14.11.7 Event Log Subscreens

The bottom of the Event Log screen includes several information fields that display information about the date and time of the last event of a specific type, as well as a count of how many events of that type are logged. Selecting a field and pressing <Enter> brings up a subscreen that shows information specific to that event type. Event types for which subscreens are available include:

- Single Bit ECC Events
- Multiple Bit ECC Events
- Pre-Boot Events

The subscreens presented for each of these event types are described in Table 39. Note that the initial three lines of information for all screens cover the same information.

Table 39. Event Log Subscreens

Event Type	Subscreen Detail	
Single Bit ECC Events	Date of Last Occurrence	None *(initial value)*
	Time of Last Occurrence	None *(initial value)*
	Total Count of Events/Errors	None *(initial value)*
	Memory Bank with Errors	None *(initial value)*
Multiple Bit ECC Events *	Date of Last Occurrence	None *(initial value)*
	Time of Last Occurrence	None *(initial value)*
	Total Count of Events/Errors	None *(initial value)*
	Memory Bank with Errors	None *(initial value)*
Pre-Boot Events *	Date of Last Occurrence	None *(initial value)*
	Time of Last Occurrence	None *(initial value)*
	Total Count of Events/Errors	None *(initial value)*
	POST ERRORS FOUND:	None *(initial value)*

3.14.12 Security Screen

This section describes the two access modes that can be set using the options found on the Security screen, and then describes the Security screen options themselves.

3.14.12.1 Administrative and User Access Modes

The options on the Security screen menu enable you to restrict access to the Setup program by enabling you to set passwords for two different access modes: Administrative mode and User mode.

In general, Administrative mode has full access to the Setup fields, whereas User mode has restricted access to the options. Thus, by setting separate Administrative and User passwords, a system administrator can limit who can change critical Setup values. The actual limitations depend on whether either the Administrative or User passwords or both are set.

To limit access to who can boot the computer, set the User password. This is the password that the computer asks for before booting. If only the Administrative password is set, the computer boots up without asking for a password. If both passwords are set, you can enter either password to boot the computer.

Table 40 shows the effects of setting the Administrative and User passwords. (The table is for reference only, and is not shown on the Security screen.) In the table, the statement "Can change a limited number of options" means you can change the date and time, the power management hot key, the User password, the security hot key, and unattended start.

Table 40. Administrative and User Password Functions

Password Set	Administrative mode can . . .	User mode can . . .	Password Required During Boot Process
Neither	Can change all options*	Can change all options*	None
Administrative only	Can change all options	Can change a limited number of options	None
User only	N/A	Can change all options	User
Both	Can change all options	Can change a limited number of options	Administrative or User

* If no password is set, any user can change all Setup options.

3.14.13 Security Screen Options

3.14.13.1 User Password

Reports if there is a User password set. There are no options.

3.14.13.2 Administrative Password

Reports if there is an Administrative password set. There are no options.

3.14.13.3 Enter Password

Sets the User password. The password can be up to seven alphanumeric characters.

3.14.13.4 Set Administrative Password

Sets the Administrative password. The password can be up to seven alphanumeric characters.

3.14.14 Exit Screen

This section describes the different ways to exit and save or not save changes made in the Setup program.

3.14.14.1 Exit Saving Changes

Saves the changes to CMOS RAM and exits the Setup program. You can also press the <F10> key anywhere in the Setup program to initiate this.

3.14.14.2 Exit Discarding Changes

Exits the Setup program without saving any changes. This means that any changes made while in the Setup program are discarded and NOT SAVED. Pressing the <Esc> key in any of the four main screens initiates this activity.

3.14.14.3 Load Setup Defaults

Resets all of the Setup options to their defaults. You can also press the <F5> key anywhere in the Setup program to initiate this.

This selection loads the default Setup values from the ROM table.

3.14.14.4 Discard Changes

Discards any changes you made during the current Setup session without exiting the program. You can also press the <F6> key anywhere in the Setup program to initiate this.

This selection loads the CMOS RAM values that were present when the computer was turned on.

4 Error Messages and Beep Codes

4.1 BIOS Beep Codes

Table 41. BIOS Beep Codes

Beeps	Error Message	Description
1	Refresh Failure	The memory refresh circuitry on the motherboard is faulty.
2	Parity Error	A parity error has been detected.
3	Base 64 KB Memory Failure	Memory failure in the first 64 KB.
4	Timer Not Operational	Memory failure in the first 64 KB of memory, or Timer 1 on the motherboard is not functioning.
5	Processor Error	The microprocessor on the motherboard generated an error.
6	Gate A20 Failure	The keyboard controller might be bad. The BIOS cannot switch to protected mode.
7	Processor Exception Interrupt Error	The microprocessor generated an exception interrupt.
8	Display Memory Read/Write Error	The video adapter is either missing or its memory is faulty. This is not a fatal error.
9	ROM Checksum Error	ROM checksum value does not match the value encoded in BIOS.
10	CMOS Shutdown Register Read/Write Error	The shutdown register for CMOS RAM failed.

4.2 PCI Configuration Error Messages

The following PCI messages are displayed as a group with bus, device and function information.

Table 42. PCI Configuration Error Messages

Error Message	Explanation
NVRAM Checksum Error, NVRAM Cleared	The ESCD data was reinitialized because of an NVRAM checksum error. Try rerunning the ICU.
System Board Device Resource Conflict	A non Plug and Play ISA card has requested a resource that is already in use.
Primary Output Device Not Found	The designated primary output device (printer, modem, or other, if output is redirected) could not be found.
Primary Input Device Not Found	The designated primary input device (keyboard, mouse, or other, if input is redirected) could not be found.
Primary Boot Device Not Found	The designated primary boot device (hard disk drive, diskette drive, or CD-ROM drive) could not be found.

continued ☛

Table42. PCI Configuration Error Messages (continued)

Error Message	Explanation
NVRAM Cleared By Jumper	The “Clear CMOS” jumper has been moved to the “CLR” position and CMOS RAM has been cleared.
NVRAM Data Invalid, NVRAM Cleared	Invalid entry in the ESCD.
Static Device Resource Conflict	A non Plug and Play ISA card has requested a resource that is already in use.
PCI Error Log is Full	If and when more than 15 PCI conflict errors are detected the log full message is displayed. If this message displays, no additional PCI errors can be logged.
Floppy Disk Controller Resource Conflict	The floppy disk controller has requested a resource that is already in use.
Primary IDE Controller Resource Conflict	The primary IDE controller has requested a resource that is already in use.
Secondary IDE Controller Resource Conflict	The secondary IDE controller has requested a resource that is already in use.
Parallel Port Resource Conflict	The parallel port has requested a resource that is already in use.
Serial Port 1 Resource Conflict	Serial port 1 has requested a resource that is already in use.
Serial Port 2 Resource Conflict	Serial port 2 has requested a resource that is already in use.

The following PCI messages are chained together to give an error message.

Table 43. Chained PCI Error Messages

Error Message		Explanation
PCI *resource name* Conflict: Bus: *aa*, Device *bb*, Function: *cc* where:		A PCI resource conflict has been detected. The full message Is formed by chaining the fixed text with the variable text indicated by italics. Each message variation provides details on the type of resource conflict, and detailed information on the bus, device, and function associated with the resource conflict.
	PCI *I/O Port* Conflict:	Two devices requested the same I/O port, resulting in a conflict.
	PCI *Memory* Conflict:	Two devices requested the same memory address, resulting in a conflict.
	PCI *IRQ* Conflict:	Two devices requested the same IRQ address, resulting in a conflict.
	Bus: *aa*	Is a hexadecimal number corresponding to the PCI bus number. For desktop motherboards, the bus number is 00.
	Device: *bb*	Is a hexadecimal number corresponding to the PCI device.
	Function: *cc*	Is a hexadecimal number corresponding to the active PCI function within a device.

4.3 BIOS Error Messages

Table 44. BIOS Error Messages

Error Message	Explanation
Gate A20 Error	Gate A20 on the keyboard controller is not working.
Address Line Short!	Error in the address decoding circuitry on the motherboard.
Cache Memory Bad, Do Not Enable Cache!	Cache memory is defective. Replace it.
CH-2 Timer Error	There is an error in timer 2.
CMOS Battery State Low	CMOS RAM is powered by a battery. The battery power is low. Replace the battery.
CMOS Checksum Failure	After CMOS RAM values are saved, a checksum value is generated for error checking. The previous value is different from the current value. Run Setup.
CMOS System Options Not Set	The values stored in CMOS RAM are either corrupt or nonexistent. Run Setup.
CMOS Display Type Mismatch	The video type in CMOS RAM does not match the type detected by the BIOS. Run Setup.
CMOS Memory Size Mismatch	The amount of memory on the motherboard is different than the amount in CMOS RAM. Run AMIBIOS Setup.
CMOS Time and Date Not Set	Run Setup to set the date and time in CMOS RAM.
Diskette Boot Failure	The boot disk in floppy drive A: is corrupt. It cannot be used to boot the computer. Use another boot disk and follow the screen instructions.
Display Switch Not Proper	The display jumper is not implemented on this product. This error should not occur.
DMA Error	Error in the DMA controller.
DMA #1 Error	Error in the first DMA channel.
DMA #2 Error	Error in the second DMA channel.
FDD Controller Failure	The BIOS cannot communicate with the floppy disk drive controller. Check all appropriate connections after the computer is powered down.
HDD Controller Failure	The BIOS cannot communicate with the hard disk drive controller. Check all appropriate connections after the computer is powered down.
INTR #1 Error	Interrupt channel 1 failed POST.
INTR #2 Error	Interrupt channel 2 failed POST.
Invalid Boot Diskette	The BIOS can read the disk in floppy drive A:, but cannot boot the computer. Use another boot disk.
Keyboard Is Locked...Unlock It	The keyboard lock on the computer is engaged. The computer must be unlocked to continue.
KB/Interface Error	There is an error in the keyboard connector.
On Board Parity Error	Parity error detected in memory.

4.4 ISA NMI Messages

Table 45. ISA NMI Messages

ISA NMI Message	Explanation
Memory Parity Error at xxxxx	Memory failed. If the memory location can be determined, it is displayed as xxxxx. If not, the message is Memory Parity Error ????.
I/O Card Parity Error at xxxxx	An expansion card failed. If the address can be determined, it is displayed as xxxxx. If not, the message is I/O Card Parity Error ????.
DMA Bus Time-out	A device has driven the bus signal for more than 7.8 microseconds.