Intel® LXD972M Transceiver Demo Board (Board Rev A1)

Preliminary User's Guide

October 2004

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Contents

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Revision History

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Page	**Description**
5	Section 1.1, “About this Demo Board Kit”. Text added.
6	Section 1.3, “Features of Intel® LXD972M Demo Board”. Text changed.
7	Section 2.1, “Equipment Requirements”. Text changed.
9	Section 2.3, “Quick-Start Checklists”. Text changed. Text changed in Table 2 “Quick-Start Checklist for Jumper Settings”. Text changed in Table 3 “Quick-Start Checklist for Switch Settings”. Figure 2 “Intel® LXD972M Transceiver Demo Board” changed.
12	Section 2.4.2, “Power Supply Voltage Source and Clock Options”. Text changed in Table 4 “Power Supply Voltage Source Connector Options” changed.
13	Section 2.4.3, “MDIO Configuration Options”. Text changed. Text changed in Table 4 “Power Supply Voltage Source Connector Options” changed.
13	Section 2.4.4, “LED Configuration Options”. Text changed.
14	Section 2.4.5, “CFG Pin Configuration Options”. Text changed and new table added.
15	Section 3.0, “Intel® LXD972M Demo Board Schematics”. Schematics changed.
20	Section 4.0, “Bill of Materials”. Text in Table 11 “Bill of Materials” changed.

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Page	**Description**
	Initial release.

1.0 Introduction

This document describes the typical hardware set-up procedures for the Intel® LXD972M Transceiver Demo Board (called hereafter the LXD972M Demo Board). The LXD972M Demo Board is a platform for evaluation of the Intel LXT972M Single-Port 10/100 Mbps PHY Transceiver (called hereafter the LXT972M Transceiver).

The LXD972M Demo Board allows system designers to test the following:

- 10 Mbps and 100 Mbps link performance
- Auto-negotiation
- Register functionality

The LXD972M Demo Board requires only a single 3.3V power supply.

1.1 About this Demo Board Kit

This Demo Board kit includes the following:

- LXD972M Demo Board
- Intel® LXD972M Transceiver Demo Board (Board Rev A1) User's Guide

1.2 Related Documents

Table 1 lists related documentation.

Table 1. Related Documents

Document	Document Number
Intel® LXT972M Single-Port 10/100 Mbps PHY Transceiver Datasheet	302875
Intel® LXT971A, LXT972A, LXT972M Single-Port 10/100 Mbps PHY Transceivers Specification Update	249354

1.3 Features of Intel® LXD972M Demo Board

- 3.3V operation, with option for 2.5V I/O voltage
- Low power consumption (300 mW typical)
- Quick setup and clear visibility of application settings for complete system demonstration
- Auto-negotiation protocol compliant. Compatible with systems not supporting auto-negotiation.
- LED indicators for major functions
- JTAG boundary scan port
- Configurable through MDIO port or hardware jumpers
- Standard half-duplex or full-duplex operation at 10 Mbps or 100 Mbps

2.0 Using the Intel® LXD972M Demo Board

This document includes information on the following items concerning using the LXD972M Demo Board:

2.1 Equipment Requirements

The LXD972M Demo Board is populated with all components needed for twisted-pair evaluation. However, the following additional equipment is also required:

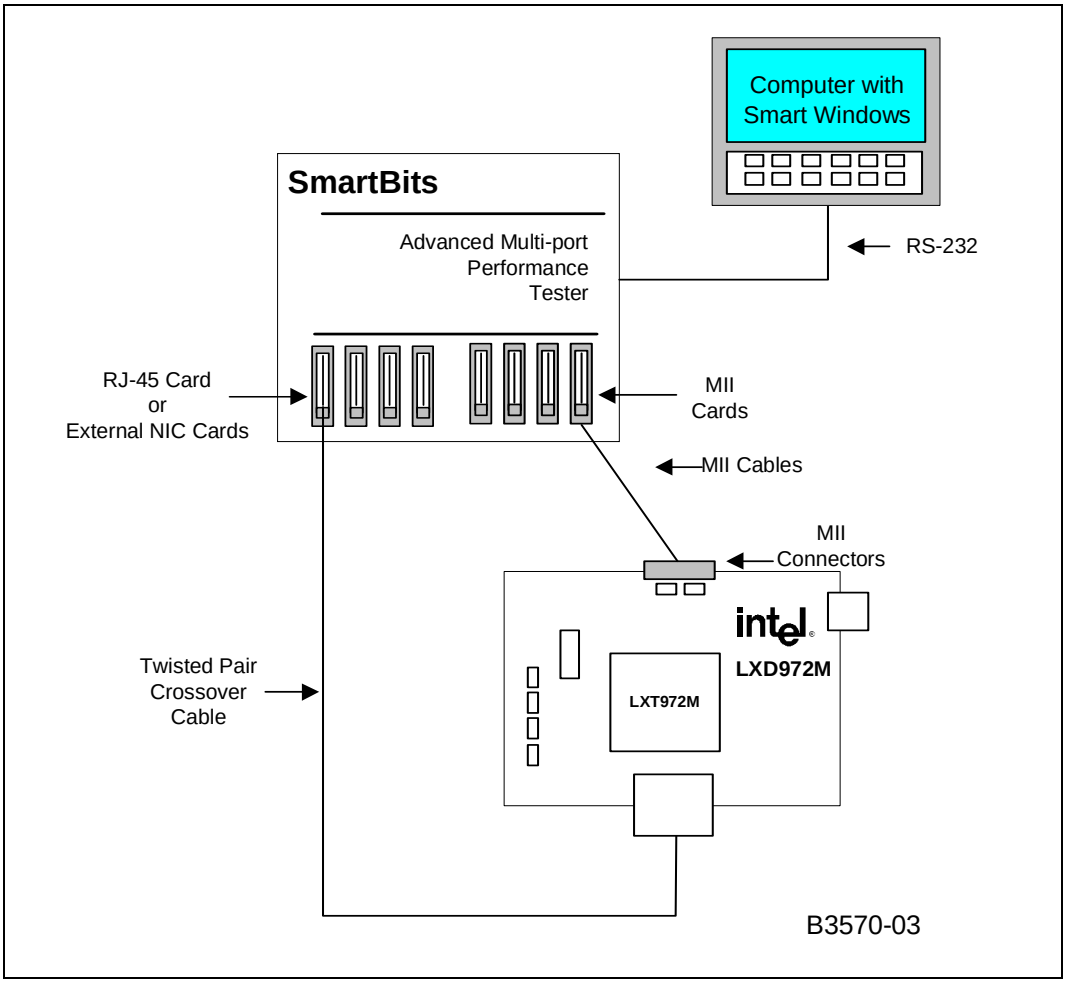
- SmartBits Advanced Multi-port Performance Test Box configured with firmware version 4.39 or newer
- PC with Smart Windows (version 6.0 or newer) installed
- One MII Cable (male to male)
- One external NIC card
- One Category 5 Unshielded Twisted-Pair (UTP) crossover cable
- External power supply

2.2 Typical Test Setup

Figure 1 shows a typical test setup for standard operation of the LXD972M Demo Board.

The LXD972M Demo Board plugs into a SmartBits Advanced Performance Test Box through a standard 40-pin MII cable (not included with the LXD972M Demo Board). The LXD972M Demo Board RJ-45 jack connects to the RJ-45 card in the SmartBits test box through a Twisted-Pair cable. Operation can be set for evaluation of 10 Mbps, 100 Mbps, and auto-negotiation capabilities.

Figure 1. Typical Test Setup



2.3 Quick-Start Checklists

Use the quick-start checklists in this section to set up the LXD972M Demo Board, shown in Figure 2, "Intel® LXD972M Transceiver Demo Board" on page 10.

The following quick-start setup procedure sets all ports to the default condition, which includes Auto-Negotiation enabled, advertising dual-speed, and full-duplex/half-duplex capabilities.

1. Set the jumpers as listed in Table 2.

   The following jumpers are defined as follows: LED1 has the functionality of LED/CFG1, LED2 has the functionality of LED/CFG2, and CFG has the functionality of LED/CFG3 as defined by the LXT972M Transceiver datasheet.
2. Set SW1 switches as listed in Table 3.
3. Connect the MII port of the LXD972M Demo Board to the Smartbits test box through the MII connector/cable. A male-to-male cable is required to interface the Smartbits test box to the LXD972M Demo Board and is available from Newark* (.5m cable - Newark 91F9746).
4. Connect the twisted-pair port through a Twisted-Pair crossover cable to the RJ-45 card in the SmartBits test box.
5. Power up the Smartbits test box.
6. When the LXD972M Demo Board is configured according to desired test settings, apply the desired power connections per Table 4 options in Section 2.4.2, "Power Supply Voltage Source and Clock Options" on page 12 and press Reset switch S2.
7. Proceed with testing.

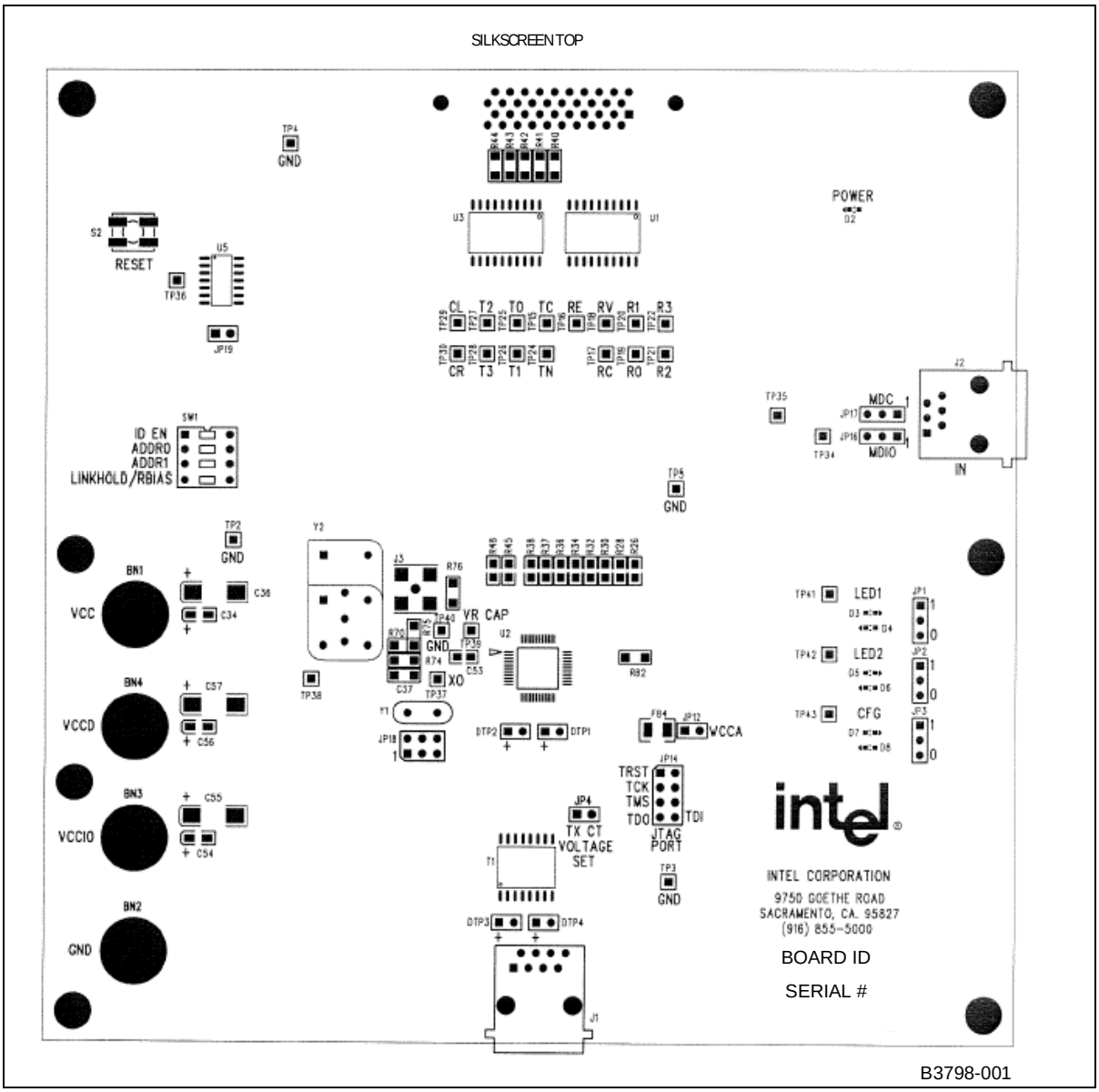
Table 2. Quick-Start Checklist for Jumper Settings

Jumper	Label	Setting		Configuration
JP1, JP2, JP3	LED1, LED2, CFG	Pins 1, 2	Jumper	"Sets Port Configuration to 111 for Auto-Negotiation, 10/100 Mbps, Full-Duplex. For details, see Section 2.4.5, "CFG Pin Configuration Options" on page 14.
JP12	VCCA	Jumpered		Routes power from VCCD connector (BN4) through JP12 to the VCCA input.
JP16	MDIO	Pins 2, 3	Jumper	Routes MDIO through MII 40-pin Connector P1.
JP17	MDC	Pins 2, 3	Jumper	Routes MDC through MII 40-pin Connector P1.
JP18	Clock Select	Pins 1, 2	Open	Disables output of clock oscillator Y2.
		Pins 3, 4 Pins 5, 6	Jumper Jumper	Connects crystal across XI and XO to enable Y1.
JP19	Reset	Pins 1,2	Jumper	Connects reset button

Table 3. Quick-Start Checklist for Switch Settings

Switch / Label	Setting	Configuration
SW1-1 / ID EN	Off	Not applicable for LXT972M Transceiver.
SW1-2 / ADDR0	Off	Sets ADDR0 = 0 ("Off" position)
SW1-3 / ADDR1	Off	Sets ADDR1 = 0 ("Off" position)
SW1-4 / LINKHOLD / RBIAS	Off	Not applicable for LXT972M Transceiver.

Figure 2. Intel® LXD972M Transceiver Demo Board



Note: In Figure 2, the format of the Board ID on the LXD972M Transceiver Demo Board can be either one of the following:

- For leaded: LXD972M Rev.A1
- For lead-free: LXD972MLF Rev.A1

In Figure 2, the format of the Serial Number on the LXD972M Transceiver Demo Board can be either one of the following:

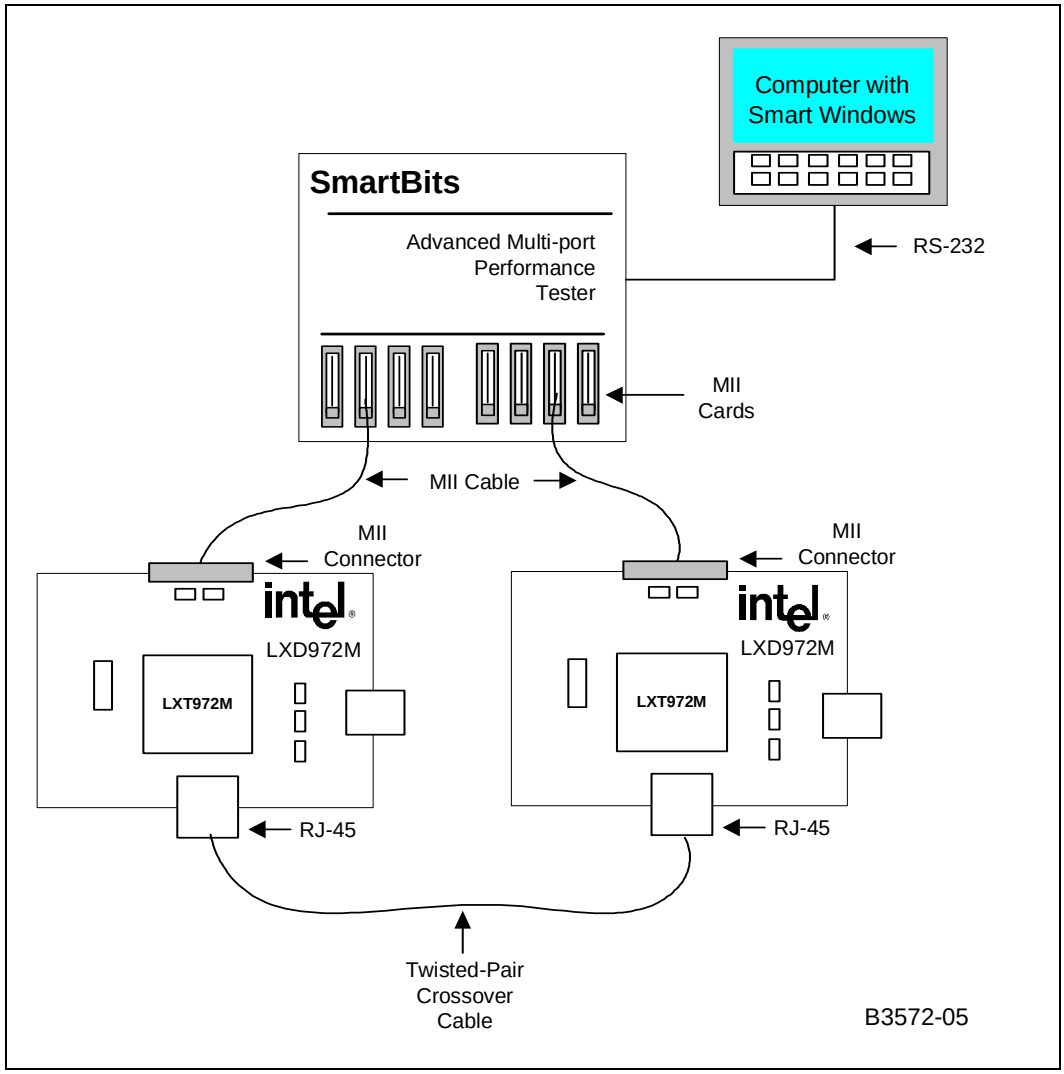
- For leaded: 972M-xxxx-A1
- For lead-free: 972MLF-xxxx-A1

2.4 Configurations

2.4.1 Optional Test Setup, Using Two Intel® LXD972M Demo Boards

Figure 3 shows an optional test setup using two LXD972M Demo Boards. Each Demo Board plugs into a SmartBits Advanced Performance Test Box through standard 40-pin MII cables. The two LXD972M Demo Boards are linked through a Twisted-Pair crossover cable connected to the RJ-45 jack on each board. Operation can be set for evaluation of 10 Mbps, 100 Mbps, and auto-negotiation capabilities.

Figure 3. Optional Test Setup



2.4.2 Power Supply Voltage Source and Clock Options

Table 4 lists banana lead power connectors (BNn) for the LXD972M Demo Board. For details on the power supplies, see the schematic in Chapter 3.0, "Intel® LXD972M Demo Board Schematics".

Table 4. Power Supply Voltage Source Connector Options

Reference Designators	Signal	Supply Description
BN1	VCC	+3.3V. For components on the LXD972M Demo Board other than LXT972M Transceiver.
BN2	GND	Ground
BN3	VCCIO	+3.3V or +2.5V. I/O voltage for the LXT972M Transceiver.
BN4	VCCD	+3.3V. LXT972M digital power. If JP12 jumper is on, analog power is provided for the LXT972M Transceiver.

Table 5 lists internal and external jumper settings to configure the power supply source for the transmit magnetic center-tap voltage.

Table 5. Magnetic Center-Tap Voltage Source Configuration Options

Desired Power Supply Source	Setting	Description
3.3V Power Supply from VCCA	Jumper JP4	Use Jumper JP4 to apply 3.3V power from VCCA for center-tap operation.
Alternate Power Supply	Open JP4	Use Jumper JP4 to supply either 2.5V or 3.3V power supply for center-tap operation. Connect the power supply to pin 2 of JP4.

Table 6 lists the LXT972M Demo Board analog power supply (VCCA) configuration options.

Table 6. Analog Power Supply (VCCA) Configuration Options

Desired Configuration		Setting	Description
Analog	3.3V Power Supply to VCCA	Jumper JP12	Use Jumper JP12 to route power from the VCCD Power Connector (BN4) through JP12 to the VCCA input of the LXT972M Transceiver.
	External Power Supply to VCCA	Open JP12	1. Remove jumper from JP12 to disable for VCCA input. 2. Apply external power from an alternate power supply through pin 2 of JP12. For power supply requirements, see the LXT972M Transceiver datasheet.

Table 7 lists clock configuration options.

Table 7. Clock Configuration Options

Desired Configuration	JP18 Settings		Description
Enable Crystal Oscillator Y1	Pins 1[1], 2	Open	Remove jumper from pins 1 and 2 to disable the clock oscillator Y2 output.
	Pins 3, 4	Jumper	Place a jumper on pins 3 and 4 and pins 5 and 6, which connects a crystal across XI and XO to enable Y1.
	Pins 5, 6		
Enable Clock Oscillator Y2	Pins 1, 2	Jumper	Place a jumper on pins 1 and 2, which enables the output of clock oscillator Y2.
	Pins 3, 4	Open	Remove jumper from pins 3 and 4, and remove jumper from pins 5 and 6, which disables a crystal connection across XI and XO to Y1.
	Pins 5, 6		
1. Pin 1 is located on the lower-right corner of JP18.			

2.4.3 MDIO Configuration Options

The default configuration of the MDIO and MDC signals is to route the MDIO through the MII connector to the SmartBits Test Box by installing jumpers JP16 and JP17.

Note: The RJ-11 feature is not supported. As a result, do not jumper the MDIO and MDC signals to the RJ-11 connector.

Table 8 lists the desired MDIO configuration settings.

Table 8. MDIO Configuration Options

Desired Configuration	Jumper	Setting		Description
Route MDIO and MDC through MII	JP16	Jumper	Pins 2, 3	Routes MDIO through 40-pin MII Connector P1
	JP17	Jumper	Pins 2, 3	Routes MDC through 40-pin MII Connector P1
Route MDIO and MDC through RJ-11	JP16	Jumper	Pins 1, 2	Routes MDIO through RJ-11 Connector J2
	JP17	Jumper	Pins 1, 2	Routes MDC through RJ-11 Connector J2

2.4.4 LED Configuration Options

The LXD972M Demo Board provides three programmable LEDs. Each LED can display one of several available status conditions as selected by the LED Configuration Register (Address 20). Programmable LEDs (LED/CFG1, LED/CFG2, LED/CFG3) are set in default mode and are programmable with the MDIO pin. Register address 20 also provides optional LED pulse stretching up to 100 ms. Register bits 20.3:2 select one of three possible stretch times. (For details, see the LXT972M Transceiver datasheet.)

Note: The active LED state is determined by the CFG pin function. When the LED/CFG pin is pulled High, the LED becomes active Low. When the LED/CFG pin is pulled Low, the LED becomes active High.

2.4.5 CFG Pin Configuration Options

Three control jumpers pull the associated port configuration pins High or Low to select the desired mode (auto-negotiation, speed, and duplex). When auto-negotiation is enabled with LED/CFG1 (JP1) = 1, then LED/CFG2 (JP2), and LED/CFG3 (JP3) are used to configure default advertising characteristics of the LXD972M Demo Board. The desired modes and jumper configuration settings are listed in Table 9. For specific register definitions and functions, see the LXT972M Transceiver datasheet.

Table 9. Jumper Configuration Settings for LED/CFG Pins

Mode			Jumper Settings					
Auto-Negotiation	Speed	Duplex	JP1 LED/CFG1 Setting		JP2 LED/CFG2 Setting		JP3 LED/CFG3 Setting	
Disabled	10	Half	Jumper	Pins 2 & 3	Jumper	Pins 2 & 3	Jumper	Pins 2 & 3
		Full		Pins 2 & 3		Pins 2 & 3		Pins 1 & 2
	100	Half		Pins 2 & 3		Pins 1 & 2		Pins 2 & 3
		Full		Pins 2 & 3		Pins 1 & 2		Pins 1 & 2
Enabled	100	Half		Pins 1 & 2		Pins 2 & 3		Pins 2 & 3
		Full / Half		Pins 1 & 2		Pins 2 & 3		Pins 1 & 2
	10/100	Half		Pins 1 & 2		Pins 1 & 2		Pins 2 & 3
		Full / Half		Pins 1 & 2		Pins 1 & 2		Pins 1 & 2

2.5 JTAG Test Signals

The boundary scan test port is accessed through JP14 for board level testing. Table 10 lists the JTAG test signal descriptions.

Table 10. JTAG Test Signal Descriptions

JP14 Pin Number	Symbol	Description
1	TRST_L	**Test Reset.** Test reset input sourced by testing device.
3	TCK	**Test Clock.** Test clock input sourced by testing device.
5	TMS	**Test Mode Select.**
7	TDO	**Test Data Output.** Test data driven with respect to the falling edge of TCK.
8	TDI	**Test Data Input.** Test data sampled with respect to the rising edge of TCK.

3.0 Intel® LXD972M Demo Board Schematics

This section includes schematics for the LXD972M Demo Board:

- Figure 4, “Schematic: Intel® LXD972M Transceiver Demo Board Power Control” on page 16
- Figure 5, “Schematic: Intel® LXD972M Transceiver Demo Board MII Port” on page 17
- Figure 6, “Schematic: Intel® LXD972M Transceiver Demo Board Twisted-Pair Port” on page 18
- Figure 7, “Schematic: Intel® LXD972M Transceiver Demo Board Configuration” on page 19

Note: Page 1 of 5 of the schematics is not included (the title page of the schematics).

Figure 4. Schematic: Intel® LXD972M Transceiver Demo Board Power Control

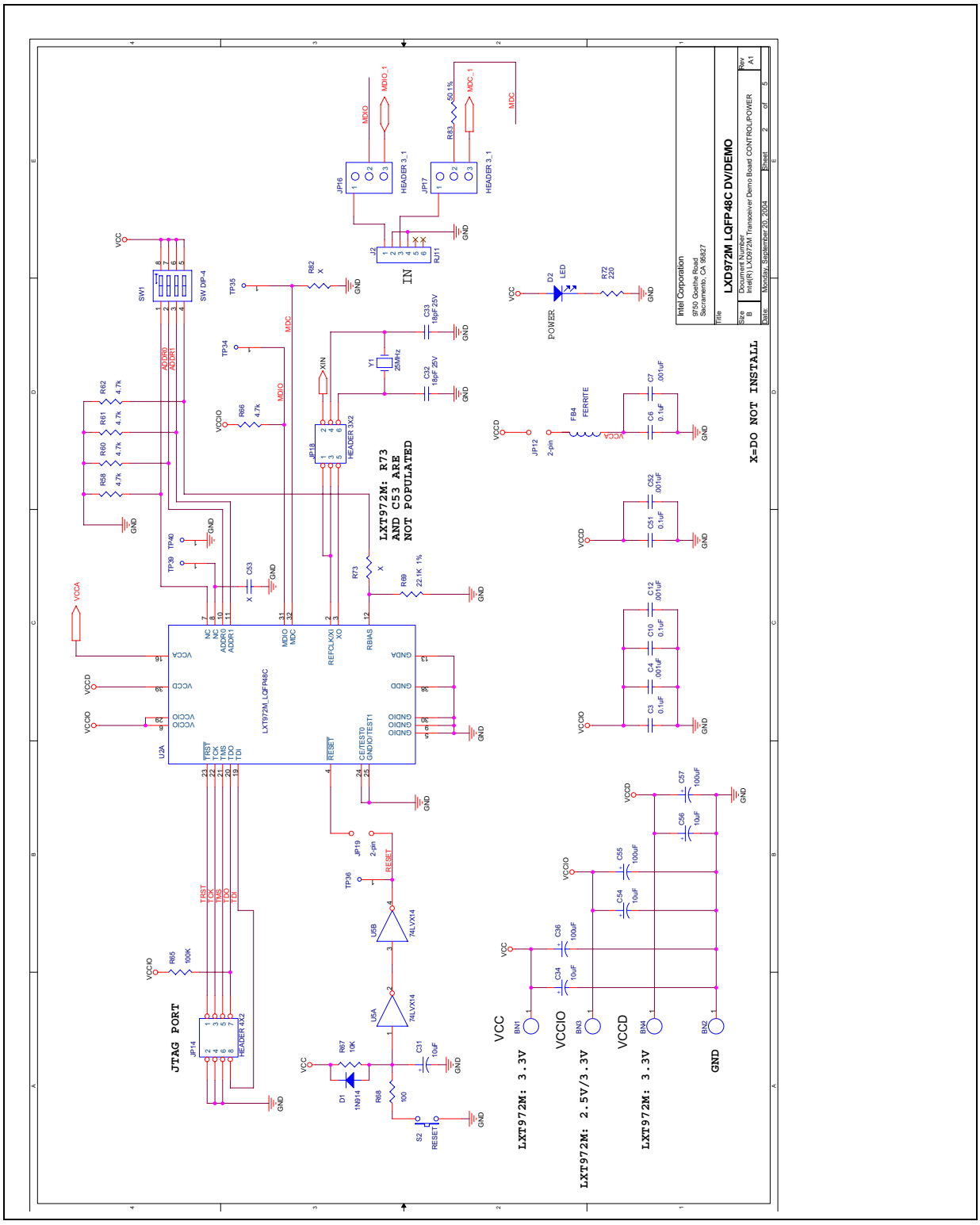


Figure 5. Schematic: Intel® LXD972M Transceiver Demo Board MII Port

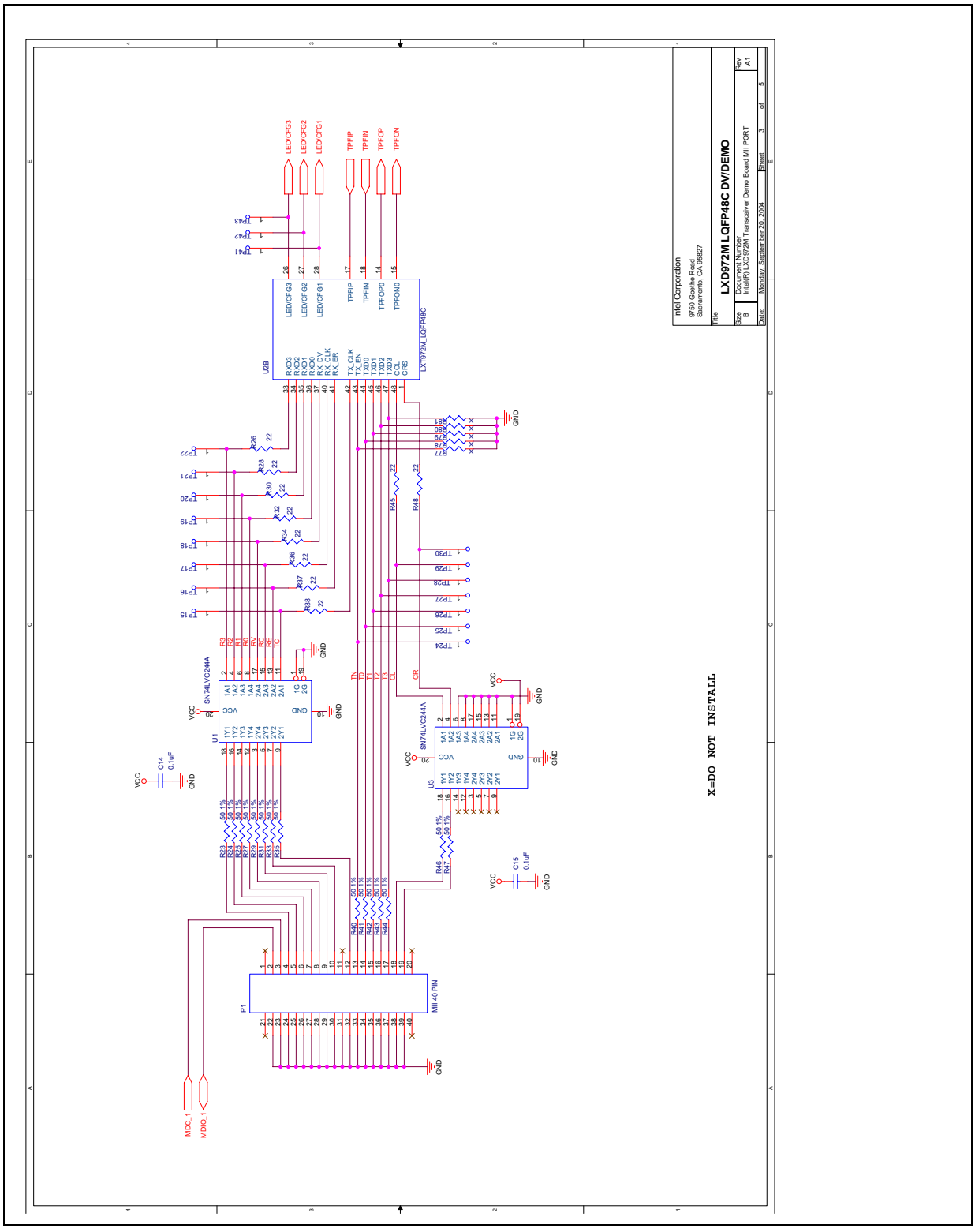


Figure 6. Schematic: Intel® LXD972M Transceiver Demo Board Twisted-Pair Port

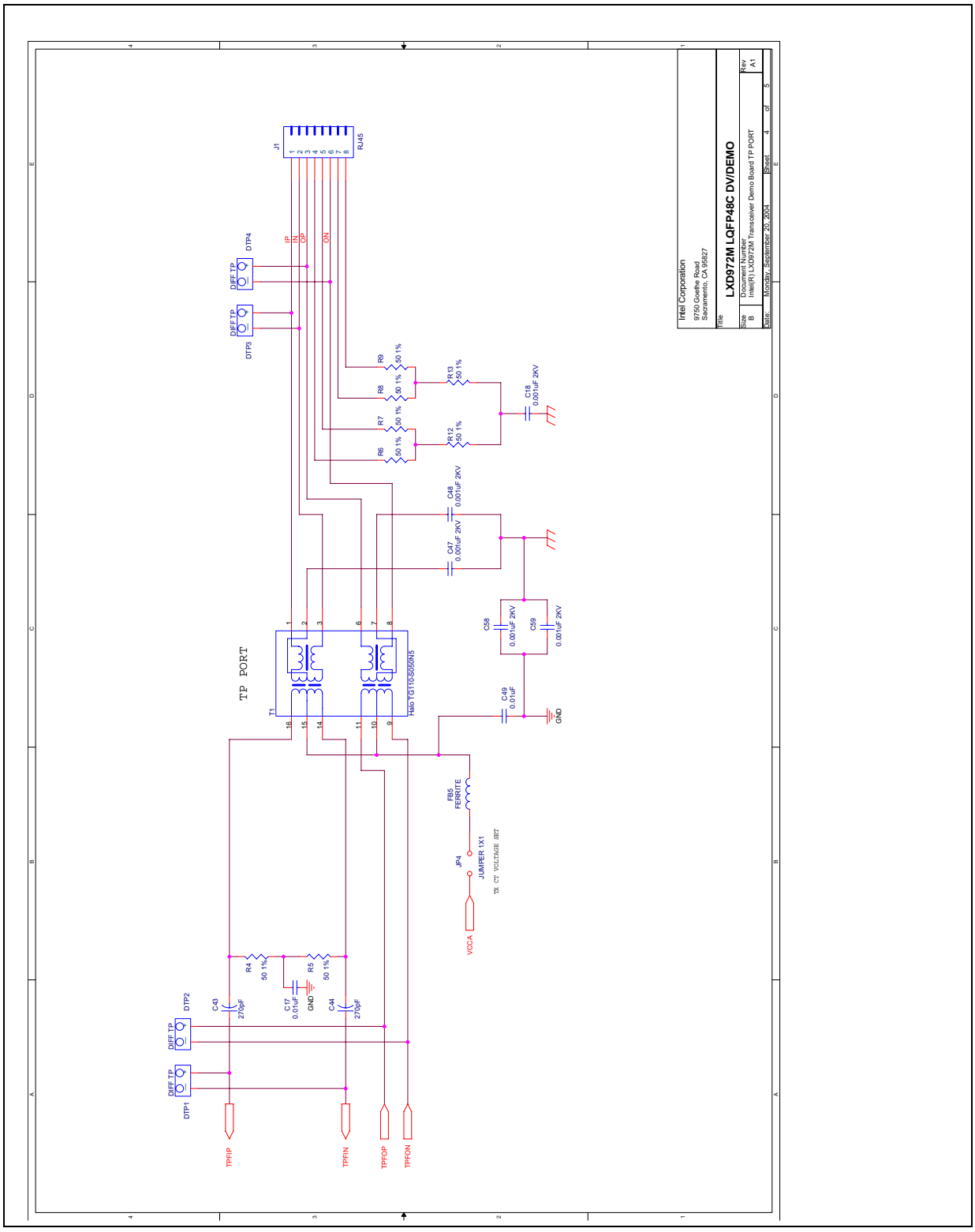
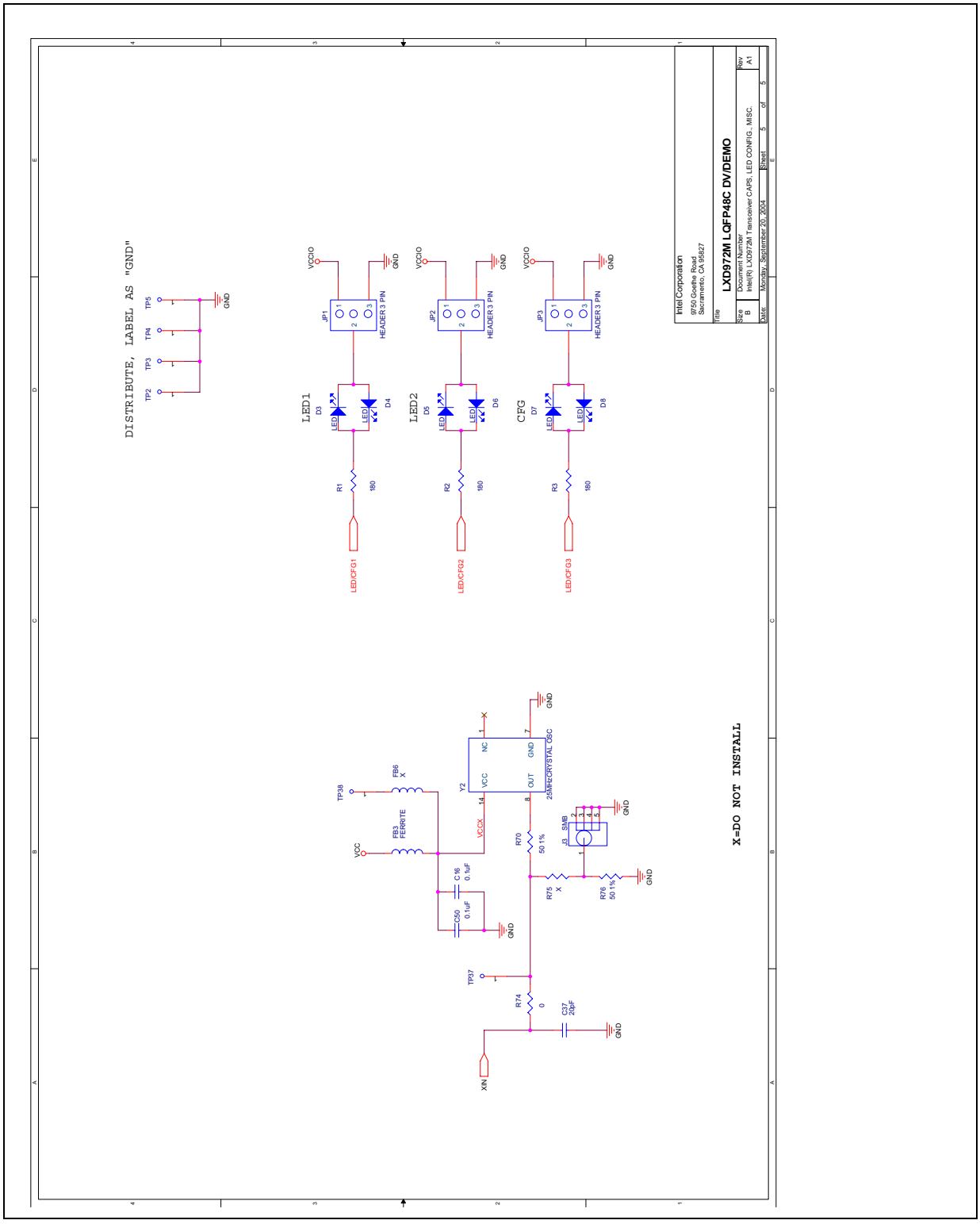


Figure 7. Schematic: Intel® LXD972M Transceiver Demo Board Configuration



4.0 Bill of Materials

Table 11 lists the bill of materials for the LXD972M Demo Board Rev A1.

Table 11. Bill of Materials (Sheet 1 of 3)

Board Reference Designator	Description	Manufacturer	Part Number	Quantity
BN1-4	CONN BANANA NUT SILVER (BANANA_NUT)	EF JOHNSON	108-0740-001	4
C1, C2, C5, C8, C9, C11, C13, C38-C42, C45, C46	LABELS NOT USED IN SCHEMATIC.			
C3, C6, C10, C14-16, C50-51	HEADER 3X1 (SIP\3P)	BERG	08055C104KATMA	8
C4, C7, C12, C52	HEADER 4X2 (HEADER2X4)	BERG	ECU-V1H102JCX	4
C17, C49	CAP 0.01uF X7R 10% (0805)	AVX	08055C103KATMA	2
C53 (NOT INSTALLED)	NOT INSTALLED		X	1
C18, C47-48, C58-59	CAP 1000pF 20% 2KV X7R (1812)	AVX	1812GC102KAT1A	5
C31, C34, C54, C56	CAP 10uF 6.3V TANT (CASEA)	PANASONIC	ECS-TOJY106R	4
C32-33	CAP 18pF 50V 5% (0805)	PANASONIC	ECU-V1H180JCN	2
C36, C55, C57	CAP 100uF 6.3V (CASED)	PANASONIC	ECE-V0JA101P	3
C37	CAP 20PF 50V 5% (1206)	PANASONIC	ECU-V1H200JCM	1
C43-44	CAP 270pF NPO (1206)	AVX	12061A271JATTA	2
D1	DIODE RECTIFIER DL4001 1A 50V MELF SMD	DIODES INC.	DL4001-13	1
D2-D8	DIODE LED GREEN SS TYPE LOW CUR SMD (LED\SMD\SS)	PANASONIC	LNJ308G8LRA	7
DTP1-4, JP4, JP12, JP19	HEADER 2X1 (SIP\2P)	BERG	68000-240-2	7
FB1, FB2	LABELS NOT USED IN SCHEMATIC.			
FB3-5	FBEAD 60 OHM@100MHZ 0.10OHM@DC 1.5A (1210) (BEAD3225)	STEWARD	MI1210K600R-00	3
FB6 (NOT INSTALLED)	NOT INSTALLED		X	1
J1	CONN MOD JACK 8-8 LOW PROFILE	AMP	555164-1	1
J2	CONN MOD JACK 6-6 RJ11 UNSHIELDED BLOCK RJ11-6L-B	CORCOM	RJ11-6L-B	1
J3	CONN SMB VERTICAL PC MOUNT (SMB\SM)	JOHNSON COMPONENTS	131-3711-201	1

Table 11. Bill of Materials (Sheet 2 of 3)

Board Reference Designator	Description	Manufacturer	Part Number	Quantity
JP5-JP11, JP13, JP15	LABELS NOT USED IN SCHEMATIC.			
JP1-3, JP16-17	HEADER 3X1 (SIP\3P)	BERG	68000-240-3	5
JP14	HEADER 4X2 (HEADER2X4)	BERG	C9192-280-4	1
JP18	HEADER 3X2	BERG	C9192-280-3	1
P1	CONN MII 40 PIN FEMALE R/A (CON40F\RT\4ROW)	AMP	787171-4	1
R1-3	RES 182 OHM 1/8W 1% (1206) SMD	PANASONIC	ERJ-8ENF1820V	3
R4-9, R12-13, R23-25, R27, R29, R31, R33, R35, R40-44, R46-47, R70, R76, R82, R83	RES 49.9 1/8W 1% (1206)	PANASONIC	ERJ-8ENF49R9V	27
R26, R28, R30, R32, R34, R36-38, R45, R48	RES 22 OHM 1/8W 1% (0805)	YAGEO AMERICA	9C08052A22R0FK HFT	10
R58, R60-62, R66	RES 4.7K 1/8W 5% (1206)	PANASONIC	ERJ-8GEYJ472V	5
R65	RES 100K 1/8W 1% (1206) SMD	PANASONIC	ERJ-8ENF1003V	1
R67	RES 10K 1/8W 1% (1206) **NOTE:** R3 is shown as 180 Ohm resistor in schematic.	PANASONIC	ERJ-8ENF1002V	1
R68	RES 100 OHM 1/8W 1% (1206)	PANASONIC	ERJ-8ENF1000V	1
R69	RES 22.1K 1/8W 1% (1206)	PANASONIC	ERJ-8ENF2212V	1
R72	RES 220 OHM 1/8W 5% (1206)	PANASONIC	ERJ-8GEYJ221V	1
R73, R75, R77-R82 (NOT INSTALLED)	NOT INSTALLED		X	8
R10, R11, R14-22, R39, R49-57, R59, R63-64, R71	LABELS NOT USED IN SCHEMATIC.			
R74	RES 0 OHM 1/8W 5% (1206) SMD	PANASONIC	ERJ-8GEY0R00V	1
S2	SWITCH PB MOM KEY J-LEAD SMD (SWITCH\RESET\SM)	C&K COMPONENTS	KT11P2JM	1
SW1	SWITCH DIP 4 POS THRU HOLE SEALED BLACK (SWITCH\8)	AMP	4-435166-9	1
T1	IC XFMR TG110-S050N2 16 PIN SOIC	HALO	TG110-S050N2	1
TP2-5, TP15-22, TP24-30, TP34-43	HEADER 1X1	BERG	68000-240-1	29

Table 11. Bill of Materials (Sheet 3 of 3)

Board Reference Designator	Description	Manufacturer	Part Number	Quantity
TP1, TP6-14, TP23, TP31-33	LABELS NOT USED IN SCHEMATIC.			
U1, U3	IC LOGIC 74LVC244 LOW VOLTAGE BUFFER 20 PIN SOIC	TEXAS INSTRUMENTS	SN74LVC244ADW	2
U2	IC PHY LXT977/LXT972M DUAL PORT (LQFP48C)	INTEL	LXT977/LXT972M	1
U4	LABELS NOT USED IN SCHEMATIC.			
U5	IC LOGIC 74LVX14 HEX SCHMITT TRIG INV 14 PIN SOIC	TOSHIBA	TC74LVX14FN	1
Y1	CRYSTAL 25.000MHZ (HC49)	CTS	MP250	1
Y2	OSC 25.000MHZ FULL SIZE ( )	CTS	MX045-25.0000	1