

Intel[®] Solid-State Drive 530 Series (mSATA)

Product Specification

- Capacities: 80 GB, 120 GB, 180 GB, 240 GB
- Components:
 - Intel[®] 20 nm NAND Flash Memory
 - Multi-Level Cell (MLC)
- Form Factors: mSATA full size
- Thickness: up to 3.8 mm
- Weight: < 10 grams
- SATA 6Gb/s Bandwidth Performance¹
 (Iometer* Queue Depth 32)
 - Sustained Sequential Read: up to 540 MB/s
 - Sustained Sequential Write: up to 490 MB/s
- Read and Write IOPS¹
 (Iometer Queue Depth 32)
 - Random 4 KB Reads: up to 41,000 IOPS
 - Random 4 KB Writes: up to 80,000 IOPS²
- Data Compression
- AES 256-bit Encryption
- End-to-End Data Protection
- Compatibility
 - Intel[®] SSD Toolbox with Intel[®] SSD Optimizer
 - Intel[®] Data Migration Software
 - Intel[®] Rapid Storage Technology
 - SATA Revision 3.0
 - ACS-2 (ATA/ATAPI Command Set 2)
 - SSD Enhanced SMART ATA feature set

- Power Management
 - 3.3 V SATA Supply Rail
 - SATA Link Power Management (LPM)
 - Device Sleep (DevSleep)
- Power
 - Active (BAPCo MobileMark* 2007 Workload): 140 mW
 - Idle³: 55 mW
 - DevSleep: 200 μW
- Temperature
 - Operating⁴: 0° C to 70° C
 - Non-Operating: -55° C to 95° C
- Reliability
 - Uncorrectable Bit Error Rate (UBER):
 <1 sector per 10¹⁶ bits read
 - Mean Time Between Failure (MTBF):
 1,200,000 hours
 - Shock (operating and non-operating): 1,000 G/0.5 msec
- Vibration
 - Operating: 2.17 G_{RMS} (5-700 Hz)
 - Non-operating: 3.13 G_{RMS} (5-800 Hz)
- Certifications and Declarations:
 - UL*
 - CE*
 - C-Tick*
 - BSMI*
 - KCC*
 - Microsoft* WHCK (Windows* 7 and 8)
 - VCCI*
 - SATA-IO*
- Product Ecological Compliance
 - RoHS*

NOTES:

- 1. Performance values vary by capacity.
- 2. Random 4 KB writes measured using out-of-box SSD
- 3. Non-DevSleep idle power with SATA Link Power Management (LPM) enabled
- 4. As measured by temperature sensor, SMART Attribute BEh. Active airflow is recommended within the system for maintaining proper device operating temperatures on heavier workloads.



Ordering Information

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Product Specification

September 2013



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Revision History

Document Number	Revision Number	Description	Revision Date
329280	001US	Initial Release	July 2013
329280	002US	Added 120 GB Capacity	September 2013



1 Introduction

This document describes the specifications and capabilities of the Intel® Solid-State Drive 530 Series (Intel® SSD 530 Series).

The Intel® SSD 530 Series is a case-less mSATA (mini-SATA) design that is designed for Ultrabook™ and small form factor compute platforms. This form factor allows ultra-compact solutions which deliver leading performance for Serial Advanced Technology Attachment (SATA)-based computers in capacities ranging up to 240GB.

The latest feature addition is the DevSleep functionality, a low power drive state controlled by the host via the DevSleep pin. The drive will consume a mere 200 μ W while in this state.

As compared to standard SATA HDDs, Intel SSD 530 Series offers these key features:

- High I/O and throughput performance
- Lower power consumption
- Increased system responsiveness
- Higher reliability
- Enhanced ruggedness
- Small form-factor
- Minimum weight

The Intel SSD 530 Series also offers additional key features such as:

• Advanced Encryption Standard (AES) 256-bit Encryption

AES 256-bit encryption is an industry standard in data security, providing a hardware-based mechanism for encryption and decryption of user data. Utilizing a 256-bit encryption key, AES encryption—when combined with an ATA drive password—helps protect user data.

End-to-End Data Protection

End-to-end data protection helps protect data from being corrupted across the data path by using cyclic redundancy check (CRC), parity, and error correction code (ECC) checks in the data path from the host interface to the NAND, and back.

Data Compression

Data compression helps improve performance and endurance by automatically compressing information sent to the SSD so that less data has to be processed and stored on the NAND. The amount of data that can be compressed depends on the type of data.



1.1 Terminology

Term	Description
ATA	Advanced Technology Attachment
DAS	Device Activity Signal
DevSleep	Device Sleep, a power feature that allows the host to initiate ultra-low power consumption by the drive.
DIPM	Device Initiated Power Management
DMA	Direct Memory Access
EXT	Extended
FPDMA	First Party Direct Memory Access
GB	Gigabyte (1,000,000,000 bytes) Note: The total usable capacity of the SSD may be less than the total physical capacity because a small portion of the capacity is used for NAND flash management and maintenance purposes.
HDD	Hard Disk Drive
HIPM	Host Initiated Power Management
1/0	Input/Output
IOPS	Input/Output Operations Per Second
КВ	Kilobyte (1,024 bytes)
LBA	Logical Block Address
LPM	Link Power Management
MB	Megabyte (1,000,000 bytes)
MLC	Multi-level Cell
MTBF	Mean Time Between Failures
NCQ	Native Command Queuing
NOP	No Operation
PIO	Programmed Input/Output
RDT	Reliability Demonstration Test
RMS	Root Mean Squared
SATA	Serial Advanced Technology Attachment
SMART	Self-Monitoring, Analysis and Reporting Technology
SSD	Solid-State Drive
TYP	Typical
UBER	Uncorrectable Bit Error Rate



1.2 Reference Documents

Table 2: Standard References

Date or Rev. #	Title	Location
Sept 2008	IEC 55022 Information Technology Equipment — Radio disturbance Characteristics— Limits and methods of measurement CISPR22:2008 (Modified)	http://www.iec.ch/
Dec 2008	VCCI	http://www.vcci.jp/vcci_e/
June 2009	RoHS	http://qdms.intel.com/ Click Search MDDS Database and search for material description datasheet
June 2009	Serial ATA Revision 3.0	http://www.sata-io.org/
August 2009	ACS-2 Specification	http://www.t13.org/
August 2010	IEC 55024 Information Technology Equipment — Immunity characteristics— Limits and methods of measurement CISPR24:2010	http://www.iec.ch/
Sept 2010	Solid-State Drive (SSD) Requirements and Endurance Test Method (JESD218)	http://www.jedec.org/standards- documents/docs/jesd218/
Oct 2010	JEDEC Solid-State Product Outline – mSATA SSD Assembly	http://www.jedec.org/
July 2011	Serial ATA Revision 3.1 (mSATA definition)	http://www.sata-io.org/



2 Product Specifications

2.1 Capacity

Table 3: User Addressable Sectors

Intel® SSD 530 Series	Unformatted Capacity (Total User Addressable Sectors in LBA mode)
80 GB	156,301,488
120 GB	234,441,648
180 GB	351,651,888
240 GB	468,862,128

2.2 Performance

Table 4: Compressible Performance

Specification	Unit	Intel® SSD 530 Series			
		80 GB	120 GB	180 GB	240 GB
Random 4 KB Read (up to) ¹	IOPS	24,000	24,000	41,000	41,000
Random 4 KB Write (up to) ²	IOPS	80,000	80,000	80,000	80,000
Random 4 KB Write (TYP) 1	IOPS	33,000	37,500	49,000	49,000
Sequential 128 KB Read (SATA 6 Gb/s) 1	MB/s	540	540	540	540
Sequential 128 KB Write (SATA 6 Gb/s) 1	MB/s	480	480	490	490

Note:

- Performance measured using Iometer* with Queue Depth 32. Measurements are performed on 8 GB of Logical Block Address (LBA) range on a full SSD
- 2. Random 4 KB writes measured using out-of-box SSD

Table 5: Incompressible Performance

Specification	Unit	Intel® SSD 530 Series			
		80 GB	120 GB	180 GB	240 GB
Random 4 KB Read (up to) ¹	IOPS	20,500	18,000	37,500	37,500
Random 4 KB Write (up to) 1	IOPS	9,200	15,000	17,000	23,000
Sequential 128 KB Read (SATA 6Gb/s) 1	MB/s	430	450	470	510
Sequential 128 KB Write (SATA 6Gb/s) ¹	MB/s	100	130	170	230

Note:

1. Performance measured using Iometer* with Queue Depth 32

Product Specification

September 2013 Order Number: 329280-002US

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Intel® Solid-State Drive 530 Series (mSATA)



Table 6: Latency

Specification	Intel® SSD 530 Series			
	80 GB	120 GB	180 GB	240 GB
Read ¹	80 μs (TYP)			
Write ¹	85 μs (TYP)			
Power On To Ready ²	1 s (TYP)			

Note:

- 1. Based on sequential 4 KB using Iometer with Queue Depth 1 workload with compressible (non-random) data pattern. Write Cache enabled.
- 2. Power On To Ready time assumes proper shutdown

2.3 Electrical Characteristics

Table 7: Operating Voltage and Power Consumption

Electrical Characteristics Value		lue		
	80 GB	120 GB	180 GB	240 GB
Operating Voltage for 3.3 V (±5%) Min Max Rise Time (Max/Min) Fall Time (Max/Min) Noise Tolerance Min Off Time ¹	3.14 V 3.47 V 100 ms / 0.1 ms 5 s / 1 ms 70 mV pp (10 Hz – 30 MHz) 1 s			
Power Consumption (TYP) Active ² Idle ³ DevSleep ⁴ Thermal Power ⁵	2.7 W	55	mW mW μW 3.8 W	4.5 W
Regulator Power ⁶	3 W	3.4 W	4.1 W	4.9 W

Note:

- 1. Minimum time from when power removed from drive (Vcc < 100 mV) to when power can be reapplied to drive
- Active power measured during execution of MobileMark* 2007 with SATA Link Power Management (LPM) enabled.
- 3. Non-DevSleep idle power with SATA Link Power Management (LPM) enabled.
- 4. Power consumption during DevSleep state.
- 5. Power measured during 128 KB sequential writes with Queue Depth 32 workload using 100 ms sample period. This represents power that would be thermal load on system during heavy workloads.
- Power measured during 128 KB sequential writes with Queue Depth 32 workload using 500 µs sample period. This represents power that system power supply would have to regulate for proper device operation.



2.4 Environmental Conditions

2.4.1 Temperature, Shock, Vibration

Table 8: Temperature, Shock, Vibration

Table 6: Temperature, Snock, Vibration				
Electrical Characteristics	Range			
Module Temperature				
Operating ¹	0° C - 70° C			
Non-operating ²	-55° C - 95° C			
Temperature Gradient ³				
Operating	30 (TYP) °C /hr			
Non-operating	30 (TYP) °C /hr			
Humidity				
Operating	5 – 95 %			
Non-operating	5 – 95 %			
Shock and Vibration	Range			
Shock ⁴				
Operating	1,000 G (Max) at 0.5 msec			
Non-operating	1,000 G (Max) at 0.5 msec			
Vibration ⁵				
Operating	2.17 GRMS (5-700 Hz) Max			
Non-operating	3.13 GRMS (5-800 Hz) Max			

Note:

- 1. As measured by temperature sensor, SMART Attribute BEh. Active airflow is recommended within the system for maintaining proper device operating temperature on heavier workloads.
- 2. Please contact your Intel representative for details on the non-operating temperature range.
- 3. Temperature gradient measured without condensation.
- 4. Shock specifications assume the SSD is mounted securely with the input vibration applied to the drive-mounting screws. Stimulus may be applied in the X, Y or Z axis. Shock specification is measured using peak acceleration and pulse width value.
- 5. Vibration specifications assume the SSD is mounted securely with the input vibration applied to the drive-mounting screws. Stimulus may be applied in the X, Y or Z axis. Vibration specification is measured using Root Mean Squared (RMS) value.

2.4.2 Altitude

The drive is not sensitive to changes in atmospheric pressure because it has no moving parts. Drive tested under non-operational conditions to pressures representative of -1 K and +40 K feet.



2.5 **Product Regulatory Compliance**

The Intel® SSD 530 Series meets or exceeds the regulatory or certification requirements in the table below.

Table 9: Product Regulatory Compliance Specifications

Title	Description	Region For Which Conformity Declared
TITLE 47-Telecommunications CHAPTER 1— FEDERAL COMMUNMICATIONS COMMISSION PART 15 — RADIO FREQUENCY DEVICES	FCC Part 15B Class B	USA
ICES-003, Issue 4 Interference-Causing Equipment Standard Digital Apparatus	CA/CSA - CEI/IEC CISPR 22-10 (Ref. CISPR 22: 2008)	Canada
IEC 55024 Information Technology Equipment — Immunity characteristics— Limits and methods of measurement CISPR24:2010	EN-55024: 2010 and its amendments	European Union
IEC 55022 Information Technology Equipment — Radio disturbance Characteristics— Limits and methods of measurement CISPR24:2008 (Modified)	EN-55022: 2010 and its amendments	European Union
EN-60950-1 2 nd Edition	Information Technology Equipment — Safety — Part 1: General Requirements	USA/Canada
UL/CSA EN-60950-1 2 nd Edition	Information Technology Equipment — Safety — Part 1: General Requirements	USA/Canada



2.6 Reliability

The Intel® SSD 530 Series meets or exceeds SSD endurance and data retention requirements as specified in the JESD218 specification.

Table 10: Reliability Specifications

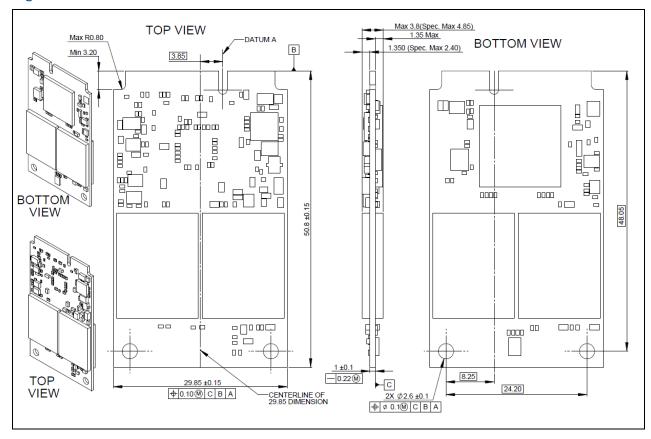
Parameter	Value
Uncorrectable Bit Error Rate (UBER)	
Uncorrectable bit error rate will not exceed one sector in the specified number of bits read. In the unlikely event of a non-recoverable read error, the SSD will report it as a read failure to the host; the sector in error is considered corrupt and is not returned to the host.	< 1 sector per 10 ¹⁶ bits read
Mean Time Between Failures (MTBF)	
Mean Time Between Failures is estimated based on Telcordia* methodology and demonstrated through Reliability Demonstration Test (RDT).	≥ 1.2 million hours
Minimum Useful Life/Endurance Rating	
The SSD will have a minimum useful life based on a typical client workload assuming up to 20 GB of host writes per day.	5 years
Insertion Cycles	
Maximum insertion/removal cycles on mSATA port	250 insertion/removal cycles



3 Mechanical Information

The figure below shows the mechanical information for the mSATA full size Intel\$ SSD 530 Series SSD. All dimensions are in millimeters.

Figure 1: Dimensions for Full Size mSATA Drives

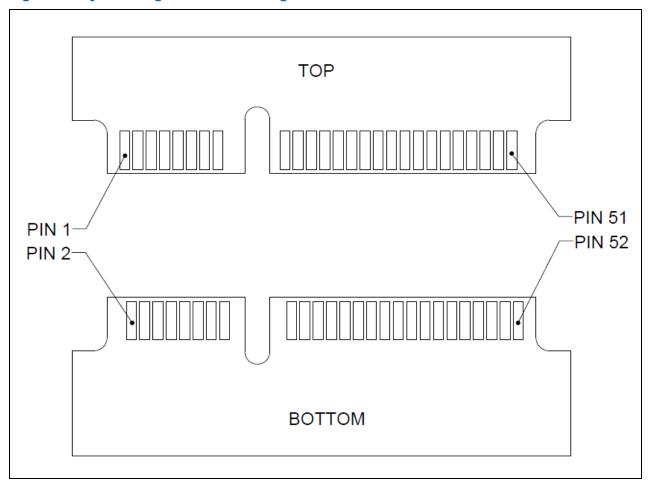




4 Pin and Signal Descriptions

4.1 Pin Locations

Figure 2: Layout of Signal and Power Segment Pins





4.2 Signal Descriptions

Table 11. Serial ATA Power Pin Definitions

Pin Reserved No Connect P2	Table 11	I. Serial ATA Power I	PIN DETINITIONS	
P2 +3.3 V 3.3 V Source P3 Reserved No Connect P4 GND Ground P5 Reserved No Connect P6¹ +1.5 V 1.5 V Source P7 Reserved No Connect P8 Reserved No Connect P9 GND Ground P10 Reserved No Connect P11 Reserved No Connect P12 Reserved No Connect P13 Reserved No Connect P14 Reserved No Connect P15 GND Ground P16 Reserved No Connect P17 Reserved No Connect P18 GND Ground P19 Reserved No Connect P19 GND Ground P10 Reserved No Connect P11 Reserved No Connect P12 Reserved No Connect P13 Reserved No Connect P14 Reserved No Connect P15 GND Ground P16 Reserved No Connect P17 Reserved No Connect P18 GND Ground P19 Reserved No Connect P20 Reserved No Connect P21 GND Ground P22 Reserved No Connect P23 +B Host Receiver Differential Signal Pair (This is an output of the SSD) P24 +3.3 V 3.3 V Source P25 -B Host Receiver Differential Signal Pair (This is an output of the SSD) P26 GND Ground P27 GND Ground P28¹ +1.5 V 1.5 V Source P29 GND Ground P30² Two Wire Interface Two Wire Interface Clock P31 -A Host Transmitter Differential Signal Pair (This is an input of the SSD)	Pin ¹	Function	Definition	
P3 Reserved No Connect P4 GND Ground P5 Reserved No Connect P6¹ +1.5 V 1.5 V Source P7 Reserved No Connect P8 Reserved No Connect P9 GND Ground P10 Reserved No Connect P11 Reserved No Connect P12 Reserved No Connect P13 Reserved No Connect P14 Reserved No Connect P15 GND Ground P16 Reserved No Connect P17 Reserved No Connect P18 GND Ground P19 Reserved No Connect P19 GND Ground P10 Reserved No Connect P11 Reserved No Connect P12 Reserved No Connect P13 Reserved No Connect P14 Reserved No Connect P15 GND Ground P16 Reserved No Connect P17 Reserved No Connect P18 GND Ground P19 Reserved No Connect P19 Reserved No Connect P20 Reserved No Connect P21 GND Ground P22 Reserved No Connect P23 +B Host Receiver Differential Signal Pair (This is an output of the SSD) P24 +3.3 V 3.3 V Source P25 -B Host Receiver Differential Signal Pair (This is an output of the SSD) P26 GND Ground P27 GND Ground P28¹ +1.5 V 1.5 V Source P29 GND Ground P30² Two Wire Interface Two Wire Interface Clock P31 -A Host Transmitter Differential Signal Pair (This is an input of the SSD)	P1	Reserved	No Connect	
P4 GND Ground P5 Reserved No Connect P6¹ +1.5 V 1.5 V Source P7 Reserved No Connect P8 Reserved No Connect P9 GND Ground P10 Reserved No Connect P11 Reserved No Connect P12 Reserved No Connect P13 Reserved No Connect P14 Reserved No Connect P15 GND Ground P16 Reserved No Connect P17 Reserved No Connect P18 GND Ground P19 Reserved No Connect P19 Reserved No Connect P10 Reserved No Connect P11 Reserved No Connect P12 Reserved No Connect P13 Reserved No Connect P14 Reserved No Connect P15 GND Ground P16 Reserved No Connect P17 Reserved No Connect P18 GND Ground P19 Reserved No Connect P20 Reserved No Connect P20 Reserved No Connect P21 GND Ground P22 Reserved No Connect P23 +B Host Receiver Differential Signal Pair (This is an output of the SSD) P24 +3.3 V 3.3 V Source P25 -B Host Receiver Differential Signal Pair (This is an output of the SSD) P26 GND Ground P27 GND Ground P28¹ +1.5 V 1.5 V Source P29 GND Ground P30² Two Wire Interface Two Wire Interface Clock P31 -A Host Transmitter Differential Signal Pair (This is an input of the SSD)	P2	+3.3 V	3.3 V Source	
P5 Reserved No Connect P6¹ +1.5 V 1.5 V Source P7 Reserved No Connect P8 Reserved No Connect P9 GND Ground P10 Reserved No Connect P11 Reserved No Connect P12 Reserved No Connect P13 Reserved No Connect P14 Reserved No Connect P15 GND Ground P16 Reserved No Connect P17 Reserved No Connect P18 GND Ground P19 Reserved No Connect P19 Reserved No Connect P19 Reserved No Connect P10 Reserved No Connect P11 Reserved No Connect P12 Reserved No Connect P13 Reserved No Connect P14 Reserved No Connect P15 GND Ground P16 Reserved No Connect P17 Reserved No Connect P18 GND Ground P19 Reserved No Connect P20 Reserved No Connect P20 Reserved No Connect P21 GND Ground P22 Reserved No Connect P23 +B Host Receiver Differential Signal Pair (This is an output of the SSD) P24 +3.3 V 3.3 V Source P25 -B Host Receiver Differential Signal Pair (This is an output of the SSD) P26 GND Ground P27 GND Ground P28¹ +1.5 V 1.5 V Source P29 GND Ground P30² Two Wire Interface Two Wire Interface Clock P31 -A Host Transmitter Differential Signal Pair (This is an input of the SSD)	P3	Reserved	No Connect	
P6¹ +1.5 V 1.5 V Source P7 Reserved No Connect P8 Reserved No Connect P9 GND Ground P10 Reserved No Connect P11 Reserved No Connect P12 Reserved No Connect P13 Reserved No Connect P14 Reserved No Connect P15 GND Ground P16 Reserved No Connect P17 Reserved No Connect P18 GND Ground P19 Reserved No Connect P20 Reserved No Connect P21 GND Ground P22 Reserved No Connect P21 GND Ground P22 Reserved No Connect P23 +B Host Receiver Differential Signal Pair (This is an output of the SSD) P24 +3.3 V 3.3 V Source P25 -B Hos	P4	GND	Ground	
P7 Reserved No Connect P8 Reserved No Connect P9 GND Ground P10 Reserved No Connect P11 Reserved No Connect P12 Reserved No Connect P13 Reserved No Connect P14 Reserved No Connect P15 GND Ground P16 Reserved No Connect P17 Reserved No Connect P18 GND Ground P19 Reserved No Connect P20 Reserved No Connect P21 GND Ground P22 Reserved No Connect P23 +B Host Receiver Differential Signal Pair (This is an output of the SSD) P24 +3.3 V 3.3 V Source P25 -B Host Receiver Differential Signal Pair (This is an output of the SSD) P26 GND Ground P27 GND Ground P28 +1.5 V 1.5 V Source P29 GND Ground P302 Two Wire Interface Two Wire Interface Clock P31 -A Host Transmitter Differential Signal Pair (This is an input of the SSD)	P5	Reserved	No Connect	
P8 Reserved No Connect P9 GND Ground P10 Reserved No Connect P11 Reserved No Connect P12 Reserved No Connect P13 Reserved No Connect P14 Reserved No Connect P15 GND Ground P16 Reserved No Connect P17 Reserved No Connect P18 GND Ground P19 Reserved No Connect P20 Reserved No Connect P20 Reserved No Connect P21 GND Ground P22 Reserved No Connect P23 +B Host Receiver Differential Signal Pair (This is an output of the SSD) P24 +3.3 V 3.3 V Source P25 B Host Receiver Differential Signal Pair (This is an output of the SSD) P26 GND Ground P27 GND Ground P28 +1.5 V 1.5 V Source P29 GND Ground P302 Two Wire Interface Two Wire Interface Clock P31 -A Host Transmitter Differential Signal Pair (This is an input of the SSD)	P6 ¹	+1.5 V	1.5 V Source	
P9 GND Ground P10 Reserved No Connect P11 Reserved No Connect P12 Reserved No Connect P13 Reserved No Connect P14 Reserved No Connect P15 GND Ground P16 Reserved No Connect P17 Reserved No Connect P18 GND Ground P19 Reserved No Connect P20 Reserved No Connect P21 GND Ground P22 Reserved No Connect P23 +B Host Receiver Differential Signal Pair (This is an output of the SSD) P24 +3.3 V 3.3 V Source P25 B Host Receiver Differential Signal Pair (This is an output of the SSD) P26 GND Ground P27 GND Ground P28 +1.5 V 1.5 V Source P29 GND Ground P30 Two Wire Interface Two Wire Interface Clock P31 -A Host Transmitter Differential Signal Pair (This is an input of the SSD)	P7	Reserved	No Connect	
P10 Reserved No Connect P11 Reserved No Connect P12 Reserved No Connect P13 Reserved No Connect P14 Reserved No Connect P15 GND Ground P16 Reserved No Connect P17 Reserved No Connect P18 GND Ground P19 Reserved No Connect P19 Reserved No Connect P19 Reserved No Connect P20 Reserved No Connect P21 GND Ground P22 Reserved No Connect P23 +B Host Receiver Differential Signal Pair (This is an output of the SSD) P24 +3.3 V 3.3 V Source P25 -B Host Receiver Differential Signal Pair (This is an output of the SSD) P26 GND Ground P27 GND Ground P28 +1.5 V 1.5 V Source P29 GND Ground P29 GND Ground P30 Two Wire Interface Two Wire Interface Clock P31 -A Host Transmitter Differential Signal Pair (This is an input of the SSD)	P8	Reserved	No Connect	
P11 Reserved No Connect P12 Reserved No Connect P13 Reserved No Connect P14 Reserved No Connect P15 GND Ground P16 Reserved No Connect P17 Reserved No Connect P18 GND Ground P19 Reserved No Connect P19 Reserved No Connect P19 Reserved No Connect P20 Reserved No Connect P21 GND Ground P22 Reserved No Connect P23 +B Host Receiver Differential Signal Pair (This is an output of the SSD) P24 +3.3 V 3.3 V Source P25 -B Host Receiver Differential Signal Pair (This is an output of the SSD) P26 GND Ground P27 GND Ground P28 Host Receiver Differential Signal Pair (This is an output of the SSD) P26 GND Ground P27 GND Ground P28 H.5 V 1.5 V Source P29 GND Ground P302 Two Wire Interface Two Wire Interface Clock P31 -A Host Transmitter Differential Signal Pair (This is an input of the SSD)	P9	GND	Ground	
P12 Reserved No Connect P13 Reserved No Connect P14 Reserved No Connect P15 GND Ground P16 Reserved No Connect P17 Reserved No Connect P18 GND Ground P19 Reserved No Connect P19 Reserved No Connect P19 Reserved No Connect P20 Reserved No Connect P21 GND Ground P22 Reserved No Connect P23 +B Host Receiver Differential Signal Pair (This is an output of the SSD) P24 +3.3 V 3.3 V Source P25 -B Host Receiver Differential Signal Pair (This is an output of the SSD) P26 GND Ground P27 GND Ground P28 +1.5 V 1.5 V Source P29 GND Ground P302 Two Wire Interface Two Wire Interface Clock P31 -A Host Transmitter Differential Signal Pair (This is an input of the SSD)	P10	Reserved	No Connect	
P13 Reserved No Connect P14 Reserved No Connect P15 GND Ground P16 Reserved No Connect P17 Reserved No Connect P18 GND Ground P19 Reserved No Connect P20 Reserved No Connect P21 GND Ground P22 Reserved No Connect P23 +B Host Receiver Differential Signal Pair (This is an output of the SSD) P24 +3.3 V 3.3 V Source P25 -B Host Receiver Differential Signal Pair (This is an output of the SSD) P26 GND Ground P27 GND Ground P28 +1.5 V 1.5 V Source P29 GND Ground P302 Two Wire Interface Two Wire Interface Clock P31 -A Host Transmitter Differential Signal Pair (This is an input of the SSD)	P11	Reserved	No Connect	
P14 Reserved No Connect P15 GND Ground P16 Reserved No Connect P17 Reserved No Connect P18 GND Ground P19 Reserved No Connect P20 Reserved No Connect P21 GND Ground P22 Reserved No Connect P23 +B Host Receiver Differential Signal Pair (This is an output of the SSD) P24 +3.3 V 3.3 V Source P25 -B Host Receiver Differential Signal Pair (This is an output of the SSD) P26 GND Ground P27 GND Ground P28 +1.5 V 1.5 V Source P29 GND Ground P30² Two Wire Interface Two Wire Interface Clock P31 -A Host Transmitter Differential Signal Pair (This is an input of the SSD)	P12	Reserved	No Connect	
P15 GND Ground P16 Reserved No Connect P17 Reserved No Connect P18 GND Ground P19 Reserved No Connect P20 Reserved No Connect P21 GND Ground P22 Reserved No Connect P23 +B Host Receiver Differential Signal Pair (This is an output of the SSD) P24 +3.3 V 3.3 V Source P25 -B Host Receiver Differential Signal Pair (This is an output of the SSD) P26 GND Ground P27 GND Ground P28 +1.5 V 1.5 V Source P29 GND Ground P302 Two Wire Interface Two Wire Interface Clock P31 -A Host Transmitter Differential Signal Pair (This is an input of the SSD)	P13	Reserved	No Connect	
P16 Reserved No Connect P17 Reserved No Connect P18 GND Ground P19 Reserved No Connect P20 Reserved No Connect P21 GND Ground P22 Reserved No Connect P23 +B Host Receiver Differential Signal Pair (This is an output of the SSD) P24 +3.3 V 3.3 V Source P25 -B Host Receiver Differential Signal Pair (This is an output of the SSD) P26 GND Ground P27 GND Ground P28 +1.5 V 1.5 V Source P29 GND Ground P302 Two Wire Interface Two Wire Interface Clock P31 -A Host Transmitter Differential Signal Pair (This is an input of the SSD)	P14	Reserved	No Connect	
P17 Reserved No Connect P18 GND Ground P19 Reserved No Connect P20 Reserved No Connect P21 GND Ground P22 Reserved No Connect P23 +B Host Receiver Differential Signal Pair (This is an output of the SSD) P24 +3.3 V 3.3 V Source P25 -B Host Receiver Differential Signal Pair (This is an output of the SSD) P26 GND Ground P27 GND Ground P28 +1.5 V 1.5 V Source P29 GND Ground P302 Two Wire Interface Two Wire Interface Clock P31 -A Host Transmitter Differential Signal Pair (This is an input of the SSD)	P15	GND	Ground	
P18 GND Ground P19 Reserved No Connect P20 Reserved No Connect P21 GND Ground P22 Reserved No Connect P23 +B Host Receiver Differential Signal Pair (This is an output of the SSD) P24 +3.3 V 3.3 V Source P25 -B Host Receiver Differential Signal Pair (This is an output of the SSD) P26 GND Ground P27 GND Ground P281 +1.5 V 1.5 V Source P29 GND Ground P302 Two Wire Interface Two Wire Interface Clock P31 -A Host Transmitter Differential Signal Pair (This is an input of the SSD)	P16	Reserved	No Connect	
P19 Reserved No Connect P20 Reserved No Connect P21 GND Ground P22 Reserved No Connect P23 +B Host Receiver Differential Signal Pair (This is an output of the SSD) P24 +3.3 V 3.3 V Source P25 -B Host Receiver Differential Signal Pair (This is an output of the SSD) P26 GND Ground P27 GND Ground P281 +1.5 V 1.5 V Source P29 GND Ground P302 Two Wire Interface Two Wire Interface Clock P31 -A Host Transmitter Differential Signal Pair (This is an input of the SSD)	P17	Reserved	No Connect	
P20 Reserved No Connect P21 GND Ground P22 Reserved No Connect P23 +B Host Receiver Differential Signal Pair (This is an output of the SSD) P24 +3.3 V 3.3 V Source P25 -B Host Receiver Differential Signal Pair (This is an output of the SSD) P26 GND Ground P27 GND Ground P281 +1.5 V 1.5 V Source P29 GND Ground P302 Two Wire Interface Two Wire Interface Clock P31 -A Host Transmitter Differential Signal Pair (This is an input of the SSD)	P18	GND	Ground	
P21 GND Ground P22 Reserved No Connect P23 +B Host Receiver Differential Signal Pair (This is an output of the SSD) P24 +3.3 V 3.3 V Source P25 -B Host Receiver Differential Signal Pair (This is an output of the SSD) P26 GND Ground P27 GND Ground P281 +1.5 V 1.5 V Source P29 GND Ground P302 Two Wire Interface Two Wire Interface Clock P31 -A Host Transmitter Differential Signal Pair (This is an input of the SSD)	P19	Reserved	No Connect	
P22 Reserved No Connect P23 +B Host Receiver Differential Signal Pair (This is an output of the SSD) P24 +3.3 V 3.3 V Source P25 -B Host Receiver Differential Signal Pair (This is an output of the SSD) P26 GND Ground P27 GND Ground P28¹ +1.5 V 1.5 V Source P29 GND Ground P30² Two Wire Interface Two Wire Interface Clock P31 -A Host Transmitter Differential Signal Pair (This is an input of the SSD)	P20	Reserved	No Connect	
P23 +B Host Receiver Differential Signal Pair (This is an output of the SSD) P24 +3.3 V 3.3 V Source P25 -B Host Receiver Differential Signal Pair (This is an output of the SSD) P26 GND Ground P27 GND Ground P28 ¹ +1.5 V 1.5 V Source P29 GND Ground P30 ² Two Wire Interface Two Wire Interface Clock P31 -A Host Transmitter Differential Signal Pair (This is an input of the SSD)	P21	GND	Ground	
P24 +3.3 V 3.3 V Source P25 -B Host Receiver Differential Signal Pair (This is an output of the SSD) P26 GND Ground P27 GND Ground P28¹ +1.5 V 1.5 V Source P29 GND Ground P30² Two Wire Interface Two Wire Interface Clock P31 -A Host Transmitter Differential Signal Pair (This is an input of the SSD)	P22	Reserved	No Connect	
P25 -B Host Receiver Differential Signal Pair (This is an output of the SSD) P26 GND Ground P27 GND Ground P281 +1.5 V 1.5 V Source P29 GND Ground P302 Two Wire Interface Two Wire Interface Clock P31 -A Host Transmitter Differential Signal Pair (This is an input of the SSD)	P23	+B	Host Receiver Differential Signal Pair (This is an output of the SSD)	
P26 GND Ground P27 GND Ground P281 +1.5 V 1.5 V Source P29 GND Ground P302 Two Wire Interface Two Wire Interface Clock P31 -A Host Transmitter Differential Signal Pair (This is an input of the SSD)	P24	+3.3 V	3.3 V Source	
P27 GND Ground P28 ¹ +1.5 V 1.5 V Source P29 GND Ground P30 ² Two Wire Interface Two Wire Interface Clock P31 -A Host Transmitter Differential Signal Pair (This is an input of the SSD)	P25	-В	Host Receiver Differential Signal Pair (This is an output of the SSD)	
P28 ¹ +1.5 V 1.5 V Source P29 GND Ground P30 ² Two Wire Interface Two Wire Interface Clock P31 -A Host Transmitter Differential Signal Pair (This is an input of the SSD)	P26	GND	Ground	
P29 GND Ground P30 ² Two Wire Interface Two Wire Interface Clock P31 -A Host Transmitter Differential Signal Pair (This is an input of the SSD)	P27	GND	Ground	
P30 ² Two Wire Interface Two Wire Interface Clock P31 -A Host Transmitter Differential Signal Pair (This is an input of the SSD)	P28 ¹	+1.5 V	1.5 V Source	
P31 -A Host Transmitter Differential Signal Pair (This is an input of the SSD)	P29	GND	Ground	
	P30 ²	Two Wire Interface	Two Wire Interface Clock	
P32 ² Two Wire Interface Two Wire Interface Data	P31	-A	Host Transmitter Differential Signal Pair (This is an input of the SSD)	
	P32 ²	Two Wire Interface	Two Wire Interface Data	

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Table 11. Serial ATA Power Pin Definitions

Pin ¹	Function	Definition
P33	+A	Host Transmitter Differential Signal Pair (This is an input of the SSD)
P34	GND	Ground
P35	GND	Ground
P36	Reserved	No Connect
P37	GND	Ground
P38	Reserved	No Connect
P39	+3.3 V	3.3 V Source
P40	GND	Ground
P41	+3.3 V	3.3 V Source
P42	Reserved	No Connect
P43	Device Type	No Connect
P44	DevSleep	Device Sleep pin
P45 ³	Vendor	Vendor Specific / Manufacturing Pin
P46	Reserved	No Connect
P47 ³	Vendor	Vendor Specific / Manufacturing Pin
P48 ¹	+1.5 V	1.5 V Source
P49	DAS/DSS	Device Activity Signal / Disable Staggered Spin-up
P50	GND	Ground
P51 ⁴	Presence Detection	Shall be pulled to GND by device
P52	+3.3 V	3.3 V Source

Note:

- 1. 1.5 V rail is not used on the Intel SSD 530 Series. No connect on the host side. Pin 6, 28, and 48 shall be unconnected on the device side to avoid conflicts with wireless coexistence pins as specified in PCI Express Mini Card Specification.
- 3. Pins 30 and 32 are intended for use as a two-wire interface to read a memory device to determine device information (an example of this would be for use as SMB bus pins). These pins are not designed to be active in conjunction with the SATA signal differential pairs. Not used on the Intel SSD 530 Series. No connect on the host side.
- 3. Vendor-specific pins are not used in the Intel SSD 530 Series. No connect on the host side.
- 4. Presence detection pin indicates presence of an mSATA device.

4.3 Device Sleep Feature

Device Sleep (or DevSleep/DEVSLP) is a new platform feature aligned with the mobile Intel® 4th Generation Core™ Processor. Many new mobile computing platforms, such as Ultrabooks™, have stringent power requirements for SSDs and require an ability to put the drive in a low power state. Although Link Power Management allows some control over power consumption, both methods still require the SATA link to remain online. The DevSleep pin is an enable high pin.

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5 Supported Command Sets

The Intel SSD 530 Series supports all mandatory Advanced Technology Attachment (ATA) and Serial ATA (SATA) commands defined in the ACS-2 and SATA Revision 3.0 specifications. The mandatory and optional commands are defined in this section.

5.1 ATA General Feature Command Set

General Feature command set (non-PACKET), which consists of:

- EXECUTE DEVICE DIAGNOSTIC
- FLUSH CACHE
- IDENTIFY DEVICE ¹
- READ DMA
- READ SECTOR(S)
- READ VERIFY SECTOR(S)
- SEEK
- SET FEATURES
- WRITE DMA
- WRITE SECTOR(S)
- READ MULTIPLE
- SET MULTIPLE MODE
- WRITE MULTIPLE

The Intel SSD 530 Series also supports the following optional commands:

- READ BUFFFER
- WRITE BUFFER
- NOP
- DOWNLOAD MICROCODE

Note:

1. See the Appendix for details on the sector data returned after issuing an IDENTIFY DEVICE command.



5.2 Power Management

The Intel SSD 530 Series supports several power management feature sets as defined by the ATA specification: general Power Management feature set, Advanced Power Management feature set, and Power-Up in Standby (PUIS) feature set.

The Advanced Power Management and PUIS features can be enabled or disabled using the SET FEATURES command.

The Power Management feature set includes the following commands:

- CHECK POWER MODE
- IDLE
- IDLE IMMEDIATE
- SLEEP
- STANDBY
- STANDBY IMMEDIATE

5.3 Security Mode Feature Set

The Intel SSD 530 Series supports the Security Mode command set, which consists of:

- SECURITY SET PASSWORD
- SECURITY UNLOCK
- SECURITY ERASE PREPARE
- SECURITY ERASE UNIT
 - Normal Mode Full NAND erase of user available space and spare area
 - Enhanced Mode Cryptographically erase data
- SECURITY FREEZE LOCK
- SECURITY DISABLE PASSWORD



5.4 SMART Command Set

The Intel SSD 530 Series supports the SMART command set, which consists of:

- SMART READ DATA
- SMART READ ATTRIBUTE THRESHOLDS
- SMART ENABLE/DISABLE ATTRIBUTE AUTOSAVE
- SMART SAVE ATTRIBUTE VALUES
- SMART EXECUTE OFF-LINE IMMEDIATE
- SMART READ LOG SECTOR
- SMART WRITE LOG SECTOR
- SMART ENABLE OPERATIONS
- SMART DISABLE OPERATIONS
- SMART RETURN STATUS

5.4.1 SMART Attributes

Table 12 lists the SMART attributes supported by the Intel SSD 530 Series; Table 13 lists the corresponding status flags and threshold settings.

Table 12: SMART Attributes

ID	Attribute			Threshold				
		SP	EC	ER	PE	ОС	PW	
05h	Re-allocated Sector Count The raw value of this attribute shows the number of retired blocks since leaving the factory (grown defect count).		1	0	0	1	0	0 (none)
09h	Power-On Hours Count The raw value reports two values: the first 4 bytes report the cumulative number of power-on hours over the life of the device, the remaining bytes report the number of milliseconds since the last hour increment. The On/Off status of the Device Initiated Power Management (DIPM) feature will affect the number of hours reported. If DIPM is turned On, the recorded value for power-on hours does not include the time that the device is in a "slumber" state. If DIPM is turned Off, the recorded value for power-on hours should match the clock time, as all three device states are counted: active, idle and slumber.	1	1	0	0	1	0	0 (none)
0Ch	Power Cycle Count The raw value of this attribute reports the cumulative number of power cycle events over the life of the device.	1	1	0	0	1	0	0 (none)
AAh	Available Reserved Space	1	1	0	0	1	1	10



ID	Attribute			Statu	s Flag	s		Threshold
		SP	EC	ER	PE	ОС	PW	
ABh	Program Fail Count The raw value of this attribute shows total count of program fails and the normalized value, beginning at 100, shows the percent remaining of allowable program fails.	1	1	0	0	1	0	0 (none)
ACh	Erase Fail Count The raw value of this attribute shows total count of erase fails and the normalized value, beginning at 100, shows the percent remaining of allowable erase fails.	1	1	0	0	1	0	0 (none)
AEh	Unexpected Power Loss The raw value of this attribute reports the cumulative number of unsafe (unclean) shutdown events over the life of the device. An unsafe shutdown occurs whenever the device is powered off without STANDBY IMMEDIATE being the last command		1	0	0	1	0	0 (none)
B7h	SATA Downshift Count The count of the number of times SATA interface selected lower signaling rate due to error.	1	1	0	0	1	0	0 (none)
B8h	End-to-End Error Detection Count Reports number of errors encountered during end-to-end error detection within the SSD data path.	1	1	0	0	1	1	90
BBh	Uncorrectable Error Count The raw value shows the count of errors that could not be recovered using Error Correction Code (ECC).	1	1	0	0	1	0	0 (none)
BEh	Temperature Reports real-time temperature of drive as measured by temperature sensor on drive PCB. The normalized value reports the current temperature value. The raw value shows current, lifetime highest and lifetime lowest temperatures. Byte 1:0 = current temp Celsius; Byte 3:2 = lifetime highest temp Celsius; Byte 5:4 = lifetime lowest temp Celsius.	1	1	0	0	1	0	0 (none)
COh	Power-Off Retract Count (Unsafe Shutdown Count) The raw value of this attribute reports the cumulative number of unsafe (unclean) shutdown events over the life of the device. An unsafe shutdown occurs whenever the device is powered off without STANDBY IMMEDIATE being the last command.	1	1	0	0	1	0	0 (none)
C7h	CRC Error Count The total number of encountered SATA interface cyclic redundancy check (CRC) errors.	1	1	0	0	1	0	0 (none)

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ID	Attribute			Threshold				
		SP	EC	ER	PE	ОС	PW	
E1h	Host Writes The raw value of this attribute reports the total number of sectors written by the host system. The raw value is increased by 1 for every 65,536 sectors (32 MB) written by the host.		1	0	0	1	0	0 (none)
E2h	Timed Workload Media Wear Measures the wear seen by the SSD (since reset of the workload timer, attribute E4h), as a percentage of the maximum rated cycles.	1	1	0	0	1	0	0 (none)
E3h	Timed Workload Host Read/Write Ratio Shows the percentage of I/O operations that are read operations (since reset of the workload timer, attribute E4h).	1	1	0	0	1	0	0 (none)
E4h	Timed Workload Timer Measures the elapsed time (number of minutes since starting this workload timer).	1	1	0	0	1	0	0 (none)
E8h	Available Reserved Space This attribute reports the number of reserve blocks remaining. The normalized value begins at 100 (64h), which corresponds to 100 percent availability of the reserved space. The threshold value for this attribute is 10 percent availability.	1	1	0	0	1	1	10
E9h	Media Wearout Indicator This attribute reports the number of cycles the NAND media has undergone. The normalized value declines linearly from 100 to 1 as the average erase cycle count increases from 0 to the maximum rated cycles. Once the normalized value reaches 1, the number will not decrease, although it is likely that significant additional wear can be put on the device.	1	1	0	0	1	0	0 (none)
F1h	Total LBAs Written The raw value of this attribute reports the total number of sectors written by the host system. The raw value is increased by 1 for every 65,536 sectors (32 MB) written by the host.	1	1	0	0	1	0	0 (none)
F2h	Total LBAs Read The raw value of this attribute reports the total number of sectors read by the host system. The raw value is increased by 1 for every 65,536 sectors (32 MB) read by the host.	1	1	0	0	1	0	0 (none)
F9h	Total NAND Writes Raw value reports the number of writes to NAND in 1 GB increments.	1	1	0	0	1	0	0 (none)



Table 13: SMART Attribute Status Flags

Status Flag	Description	Value = 0	Value = 1
SP	Self-preserving attribute	Not a self-preserving attribute	Self-preserving attribute
EC	Event count attribute	Not an event count attribute	Event count attribute
ER	Error rate attribute	Not an error rate attribute	Error rate attribute
PE	Performance attribute	Not a performance attribute	Performance attribute
OC	Online collection attribute	Collected only during offline	Collected during both
00	Offilitie collection attribute	activity	offline and online activity
PW	Pre-fail warranty attribute	Advisory	Pre-fail

5.4.2 SMART Logs

The Intel SSD 530 Series implements the following Log Addresses: 00h, 02h, 03h, 06h, and 07h.

The Intel SSD 530 Series implements host vendor specific logs (addresses 80h-9Fh) as read and write scratchpads, where the default value is zero (0). Intel SSD 530 Series does not write any specific values to these logs unless directed by the host through the appropriate commands.

The Intel SSD 530 Series also implements a device vendor specific log at address A9h as a read-only log area with a default value of zero (0).

5.5 Device Statistics

In addition to the SMART attribute structure, statistics pertaining to the operation and health of the Intel SSD 530 Series can be reported to the host on request through the Device Statistics log as defined in the ATA specification.

The Device Statistics log is a read-only GPL/SMART log located at read log address 0x04 and is accessible using READ LOG EXT, READ LOG DMA EXT or SMART READ LOG commands.

The table below lists the Device Statistics supported by the Intel SSD 530 Series.

Table 14: Device Statistics Log

Page	Offset	Description	Equivalent SMART attribute if applicable
0x00	-	List of Supported Pages	-
	0x08	Power Cycle Count	0Ch
0x01 - General	0x10	Power-On Hours	09h
Statistics	0x18	Logical Sectors Written	E1h
	0x28	Logical Sectors Read	F2h
0x04 - General	0x08	Num Reported Uncorrectable Errors	BBh
Errors Statistics	0x10	Num Resets Between Command Acceptance and Completion	-
0x06 -	0x08	Num Hardware Resets	-
Transport	0x10	Num ASR Events	-
Statistics	0x18	Num Interface CRC Errors	-
0x07 - Solid State Device Statistics	0x08	Percentage Used Endurance Indicator	E9h This statistic counts up from 0 rather than down from 100, and may go beyond 100 for drives that exceed their expected lifetime.

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5.6 SMART Command Transport

With SMART Command Transport (SCT), a host can send commands and data to an SSD and receive status and data from an SSD using standard write/read commands to manipulate two SMART Logs:

- Log Address E0h ("SCT Command/Status") used to send commands and retrieve status
- Log Address E1h ("SCT Data Transfer") used to transport data

5.7 Data Set Management Command Set

The Intel SSD 530 Series supports the Data Set Management command set Trim attribute, which consists of:

DATA SET MANAGEMENT

5.8 Host Protected Area Command Set

- READ NATIVE MAX ADDRESS
- SET MAX ADDRESS
- READ NATIVE MAX ADDRESS EXT
- SET MAX ADDRESS EXT

5.9 48-Bit Address Command Set

The Intel SSD 530 Series supports the 48-bit Address command set, which consists of:

- FLUSH CACHE EXT
- READ DMA EXT
- READ NATIVE MAX ADDRESS
- READ NATIVE MAX ADDRESS EXT
- READ SECTOR(S) EXT
- READ VERIFY SECTOR(S) EXT
- SET MAX ADDRESS EXT
- WRITE DMA EXT
- WRITE MULTIPLE EXT
- WRITE SECTOR(S) EXT

5.10 General Purpose Log Command Set

The Intel SSD 530 Series supports the General Purpose Log command set, which consists of:

- READ LOG EXT
- WRITE LOG EXT
- READ LOG DMA EXT
- WRITE LOG DMA EXT

5.11 Native Command Queuing

- READ FPDMA QUEUED
- WRITE FPDMA QUEUED



5.12 Software Settings Preservation

The Intel SSD 530 Series supports the SET FEATURES parameter to enable/disable the preservation of software settings.

5.13 SATA Link Power Management (LPM)

The Intel SSD 530 Series supports the SET FEATURES parameter to enable Device Initiated Power Management (DIPM). The SSD also supports Host Initiated Power Management (HIPM).



6 Certifications and Declarations

The table below describes the Device Certifications supported by the Intel SSD 530 Series.

Table 15: Device Certifications and Declarations

Certification	Description
CE Compliant	European Economic Area (EEA): Compliance with the essential requirements of EC Council Directives Low Voltage Directive (LVD) 2006/95/EC, EMC Directive 2004/108/EC and Directive 2011/65/EU.
UL Certified	Certified Underwriters Laboratories, Inc. Bi-National Component Recognition; UL 60950-1, 2nd Edition, 2007-03-27 (Information Technology Equipment - Safety - Part 1: General Requirements) CSA C22.2 No. 60950-1-07, 2nd Edition, 2007-03 (Information Technology
C-Tick Compliant	Equipment - Safety - Part 1: General Requirements) Compliance with the Australia/New Zealand Standard AS/NZS3548 and Electromagnetic Compatibility (EMC) Framework requirements of the Australian Communication Authority (ACA).
BSMI Compliant	Compliance to the Taiwan EMC standard CNS 13438: Information technology equipment - Radio disturbance Characteristics - limits and methods of measurement, as amended on June 1, 2006, is harmonized with CISPR 22: 2005.04.
ксс	Compliance with paragraph 1 of Article 11 of the Electromagnetic Compatibility Control Regulation and meets the Electromagnetic Compatibility (EMC) Framework requirements of the Radio Research Laboratory (RRL) Ministry of Information and Communication Republic of Korea.
Microsoft WHCK	Microsoft Windows Hardware Certification Kit
RoHS Compliant	Restriction of Hazardous Substance Directive
VCCI	Voluntary Control Council for Interface to cope with disturbance problems caused by personal computers or facsimile.
SATA-IO	Indicates certified logo program from Serial ATA International Organization.
Low Halogen	Applies only to brominated and chlorinated flame retardants (BFRs/CFRs) and PVC in the final product. Intel components as well as purchased components on the finished assembly meet JS-709 requirements, and the PCB/substrate meet IEC 61249-2-21 requirements. The replacement of halogenated flame retardants and/or PVC may not be better for the environment.



7 Appendix

The table below describes the sector data returned from an identify device command

Table 16: Identify Device Returned Sector Data

Word	F = Fixed V = Variable X = Both	Default Value	Description
0	F	0040h	General configuration bit-significant information
1	Х	3FFFh	Obsolete - Number of logical cylinders (16,383)
2	V	C837h	Specific configuration
3	Х	0010h	Obsolete - Number of logical heads (16)
4-5	Х	0h	Retired
6	Х	003Fh	Obsolete - Number of logical sectors per logical track (63)
7-8	V	0h	Reserved for assignment by the CompactFlash* Association (CFA)
9	Х	0h	Retired
10-19	F	varies	Serial number (20 ASCII characters)
20-21	Х	0h	Retired
22	Х	0h	Obsolete
23-26	F	varies	Firmware revision (8 ASCII characters)
27-46	F	varies	Model number (Intel® Solid-State Drive)
47	F	8010h	7:0—Maximum number of sectors transferred per interrupt on multiple commands
48	F	4000h	Reserved
49	F	2F00h	Capabilities
50	F	4000h	Capabilities
51-52	Х	0h	Obsolete
53	F	0007h	Words 88 and 70:64 valid
54	Х	3FFFh	Obsolete - Number of logical cylinders (16,383)
55	Х	0010h	Obsolete - Number of logical heads (16)
56	Х	003Fh	Obsolete - Number of logical sectors per logical track (63)
57-58	Х	00FBFC10h	Obsolete
59	V	0110h	Number of sectors transferred per interrupt on multiple commands
60-61	F	varies	Total number of user-addressable sectors
62	Х	0h	Obsolete
63	F	0007h	Multi-word DMA modes supported/selected
64	F	0003h	PIO modes supported
65	F	0078h	Minimum multiword DMA transfer cycle time per word
66	F	0078h	Manufacturer's recommended multiword DMA transfer cycle time
67	F	0078h	Minimum PIO transfer cycle time without flow control

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Word	F = Fixed V = Variable X = Both	Default Value	Description
69	F	4010h	Additional Supported
70	F	Oh	Reserved
71-74	F	0h	Reserved for IDENTIFY PACKET DEVICE command
75	F	001Fh	Queue depth
76	F	270Eh	Serial ATA capabilities
77	F	0086h	Reserved for future Serial ATA definition
78	F	054Ch	Serial ATA features supported
79	V	0040h	Serial ATA features enabled
80	F	03FCh	Major version number
81	F	FFFFh	Minor version number
82	F	746Bh	Command set supported
83	F	7429h	Command sets supported
84	F	6163h	Command set/feature supported extension
85	V	7469h	Command set/feature enabled
86	V	B409h	Command set/feature enabled
87	V	6163h	Command set/feature default
88	V	407Fh	Ultra DMA Modes
89	F	0002h	Time required for security erase unit completion
90	F	0001h	Time required for enhanced security erase completion
91	V	00FEh	Current advanced power management value
92	V	FFFEh	Master Password Revision Code
93	F	Oh	Hardware reset result: the contents of bits (12:0) of this word shall change only during the execution of a hardware reset
94	V	Oh	Vendor's recommended and actual acoustic management value
95	F	0h	Stream minimum request size
96	V	0h	Streaming transfer time - DMA
97	V	0h	Streaming access latency - DMA and PIO
98-99	F	0h	Streaming performance granularity
100-103	V	varies	Maximum user LBA for 48-bit address feature set
104	V	0h	Streaming transfer time - PIO
105	F	0001h	Reserved
106	F	4000h	Physical sector size / logical sector size
107	F	Oh	Inter-seek delay for ISO-7779 acoustic testing in microseconds
108-111	F	varies	Unique ID
112-115	F	0h	Reserved for world wide name extension to 128 bits
116	V	0h	Reserved for technical report
117-118	F	0h	Words per logical sector
119	F	401Ch	Supported settings
120	F	401Ch	Command set/feature enabled/supported



Word	F = Fixed V = Variable X = Both	Default Value	Description
121-126	F	0h	Reserved
127	F	0h	Removable Media Status Notification feature set support
128	V	0021h	Security status
129-159	Х	varies	Vendor-specific
160	F	0h	CompactFlash Association (CFA) power mode 1
161-168	Х	0h	Reserved for assignment by the CFA
169	Х	0001h	Data set management Trim attribute support
170-173	F	0h	Additional Product Identifier
174-175	F	0h	Reserved
176-205	V	0h	Current media serial number
206	Х	0025h	SCT Command Transport
207-208	Х	0h	Reserved
209	Х	4000h	Alignment of logical blocks within a physical block
210-211	Х	0h	Write-Read-Verify Sector Count Mode 3 (DWord)
212-213	Х	0h	Write-Read-Verify Sector Count Mode 2 (DWord)
214	Х	0h	NV Cache Capabilities
215-216	Х	0h	NV Cache Size in Logical Blocks (DWord)
217	Х	0001h	Nominal media rotation rate
218	Х	0h	Reserved
219	Х	0h	NV Cache Options
220	Х	0h	Write-Read-Verify feature set
221	Х	0h	Reserved
222	Х	103Fh	Transport major version number
223	Х	0h	Transport minor version number
224-229	Х	0h	Reserved
230-233	Х	Oh	Extended Number of User Addressable Sectors (QWord)
234	Х	0002h	Minimum number of 512-byte data blocks per DOWNLOAD MICROCODE command for mode 03h
235	Х	0400h	Maximum number of 512-byte data blocks per DOWNLOAD MICROCODE command for mode 03h
236-254	X	0h	Reserved
255	Х	varies	Integrity word

Note:

F = **Fixed**. The content of the word is fixed and does not change. For removable media devices, these values may change when media is removed or changed.

V = Variable. The state of at least one bit in a word is variable and may change depending on the state of the device or the commands executed by the device.

 $\mathbf{X} = \mathbf{F} \mathbf{or} \mathbf{V}$. The content of the word may be fixed or variable.

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