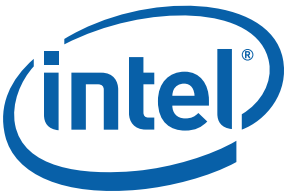

Intel® Core™ 2 Duo processor with the Mobile Intel® 945GME Express Chipset

Development Kit User's Manual

May 2007

Order Number: 317443-001US

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Revision History

Date	Revision	Description
May 2007	001	Initial release

1.0 About This Manual

This user's manual describes the use of the Intel® Core™ 2 Duo processor with the Mobile Intel® 945GME Express Chipset. This manual has been written for OEMs, system evaluators, and embedded system developers. This document defines all jumpers, headers, LED functions, and their locations on the board, along with subsystem features and POST codes. This manual assumes basic familiarity in the fundamental concepts involved with installing and configuring hardware for a personal computer system.

For the latest information about the Intel® 945GME Express Chipset Development Kit, visit:

http://developer.intel.com/design/intarch/devkits/index.htm

For design documents related to this platform please contact http://developer.intel.com/design/intarch/core2duo/tech_docs.htm.

Note: The Intel® 945GME Express Chipset supports both Intel® Core™ Duo processors and Intel® Core™ 2 Duo processors. For the Intel® 945GME Express Chipset with Intel® Core™ Duo Processors Development Kit User's Manual, visit http://download.intel.com

1.1 Content Overview

Chapter 1.0, "About This Manual" — This chapter contains a description of conventions used in this manual. The last few sections explain how to obtain literature and contact customer support.

Chapter 2.0, "Getting Started"— Provides complete instructions on how to configure the evaluation board and processor assembly by setting jumpers, connecting peripherals, providing power, and configuring the BIOS.

Chapter 3.0, "Theory of Operation" — This chapter provides information on the system design.

Chapter 4.0, "Hardware Reference"— This chapter provides a description of jumper settings and functions, board debug capabilities, and pinout information for connectors.

Appendix A, "Heat Sink Installation Instructions" gives detailed installation instructions for the Intel® Core™ 2 Duo processor heat sink.

1.2 Text Conventions

The following notations may be used throughout this manual.

#	The pound symbol (#) appended to a signal name indicates that the signal is active low. (e.g., PRSNT1#)
Variables	Variables are shown in italics. Variables must be replaced with correct values.

Instructions

Instruction mnemonics are shown in uppercase. When you are programming, instructions are not case-sensitive. You may use either uppercase or lowercase.

Numbers

Hexadecimal numbers are represented by a string of hexadecimal digits followed by the character *H*. A zero prefix is added to numbers that begin with *A* through *F*. (For example, *FF* is shown as *0FFH*.) Decimal and binary numbers are represented by their customary notations. (That is, 255 is a decimal number and 1111 1111 is a binary number. In some cases, the letter *B* is added for clarity.)

Units of Measure

The following abbreviations are used to represent units of measure:

A	amps, amperes
GByte	gigabytes
KByte	kilobytes
KΩ	kilo-ohms
mA	milliamps, milliamperes
MByte	megabytes
MHz	megahertz
ms	milliseconds
mW	milliwatts
ns	nanoseconds
pF	picofarads
W	watts
V	volts
µA	microamps, microamperes
µF	microfarads
µs	microseconds
µW	microwatts

Signal Names

Signal names are shown in uppercase. When several signals share a common name, an individual signal is represented by the signal name followed by a number, while the group is represented by the signal name followed by a variable (*n*). For example, the lower chip-select signals are named CS0#, CS1#, CS2#, and so on; they are collectively called CS*n*#. A pound symbol (#) appended to a signal name identifies an active-low signal. Port pins are represented by the port abbreviation, a period, and the pin number (e.g., P1.0).

1.3 Glossary of Terms and Acronyms

This section defines conventions and terminology used throughout this document.

Aggressor A network that transmits a coupled signal to another network.

Anti-etch Any plane-split, void or cutout in a VCC or GND plane.

Assisted Gunning Transceiver Logic+

The front-side bus uses a bus technology called AGTL+, or Assisted Gunning Transceiver Logic. AGTL+ buffers are open-drain, and require pull-up resistors to provide the high logic level and termination. AGTL+ output buffers differ from GTL+ buffers with the addition of an active pMOS pull-up transistor to assist the pull-up resistors during the first clock of a low-to-high voltage transition.

Asynchronous GTL+ The processor does not utilize CMOS voltage levels on any signals that connect to the processor. As a result, legacy input signals such as A20M#, IGNNE#, INIT#, LINT0/INTR, LINT1/NMI, PWRGOOD, SMI#, SLP#, and STPCLK# utilize GTL+ input buffers. Legacy output signals (FERR# and IERR#) and non-AGTL+ signals (THERMTRIP# and PROCHOT#) also utilize GTL+ output buffers. All of these signals follow the same DC requirements as AGTL+ signals, however the outputs are not actively driven high (during a logical 0 to 1 transition) by the processor (the major difference between GTL+ and AGTL+). These signals do not have setup or hold time specifications in relation to BCLK[1:0], and are therefore referred to as "Asynchronous GTL+ Signals". However, all of the Asynchronous GTL+ signals are required to be asserted for at least two BCLKs in order for the processor to recognize them.

Bus Agent A component or group of components that, when combined, represent a single load on the AGTL+ bus.

Crosstalk The reception on a victim network of a signal imposed by aggressor network(s) through inductive and capacitive coupling between the networks.

- Backward Crosstalk - Coupling that creates a signal in a victim network that travels in the opposite direction as the aggressor's signal.
- Forward Crosstalk - Coupling that creates a signal in a victim network that travels in the same direction as the aggressor's signal.
- Even Mode Crosstalk - Coupling from a signal or multiple aggressors when all the aggressors switch in the same direction that the victim is switching.
- Odd Mode Crosstalk - Coupling from a signal or multiple aggressors when all the aggressors switch in the opposite direction that the victim is switching.

Flight Time Flight time is a term in the timing equation that includes the signal propagation delay, any effects the system has on the TCO of the driver, plus any adjustments to the signal at the receiver

needed to ensure the setup time of the receiver. More precisely, flight time is defined as:

- The time difference between a signal at the input pin of a receiving agent crossing the switching voltage (adjusted to meet the receiver manufacturer's conditions required for AC timing specifications; i.e., ringback, etc.) and the output pin of the driving agent crossing the switching voltage when the driver is driving a test load used to specify the driver's AC timings.
- Maximum and Minimum Flight Time - Flight time variations are caused by many different parameters. The more obvious causes include variation of the board dielectric constant, changes in load condition, crosstalk, power noise, variation in termination resistance, and differences in I/O buffer performance as a function of temperature, voltage, and manufacturing process. Some less obvious causes include effects of Simultaneous Switching Output (SSO) and packaging effects.
- Maximum flight time is the largest acceptable flight time a network will experience under all conditions.
- Minimum flight time is the smallest acceptable flight time a network will experience under all conditions.

Infrared Data Assoc. The Infrared Data Association (IrDA) has outlined a specification for serial communication between two devices via a bi-directional infrared data port. The 945GME platform has such a port and it is located on the rear of the platform between the two USB connectors.

IMVP6 The Intel Mobile Voltage Positioning specification for the Intel® Core™ 2 Duo Processor. It is a DC-DC converter module that supplies the required voltage and current to a single processor.

Inter-Symbol Interference

Inter-symbol interference is the effect of a previous signal (or transition) on the interconnect delay. For example, when a signal is transmitted down a line and the reflections due to the transition have not completely dissipated, the following data transition launched onto the bus is affected. ISI is dependent upon frequency, time delay of the line, and the reflection coefficient at the driver and receiver. ISI may impact both timing and signal integrity.

Media Expansion Card

The Media Expansion Card (MEC) provides digital display options through the SDVO interface. The MEC card also incorporates video-in.

Network The network is the trace of a Printed Circuit Board (PCB) that completes an electrical connection between two or more components.

Overshoot The maximum voltage observed for a signal at the device pad, measured with respect to VCC.

Pad The electrical contact point of a semiconductor die to the package substrate. A pad is only observable in simulations.

Pin The contact point of a component package to the traces on a substrate, such as the motherboard. Signal quality and timings may be measured at the pin.

Power-Good — "Power-Good," "PWRGOOD," or "CPUPWRGOOD" (an active high signal) indicates that all of the system power supplies and clocks are stable. PWRGOOD should go active a predetermined time after system voltages are stable and should go inactive as soon as any of these voltages fail their specifications.

Ringback — The voltage to which a signal changes after reaching its maximum absolute value. Ringback may be caused by reflections, driver oscillations, or other transmission line phenomena.

System Bus — The System Bus is the microprocessor bus of the processor.

Setup Window — The time between the beginning of Setup to Clock (TSU_MIN) and the arrival of a valid clock edge. This window may be different for each type of bus agent in the system.

Simultaneous Switching Output — Simultaneous Switching Output (SSO) effects are differences in electrical timing parameters and degradation in signal quality caused by multiple signal outputs simultaneously switching voltage levels in the opposite direction from a single signal or in the same direction. These are called odd mode and even mode switching, respectively. This simultaneous switching of multiple outputs creates higher current swings that may cause additional propagation delay ("push-out") or a decrease in propagation delay ("pull-in"). These SSO effects may impact the setup and/or hold times and are not always taken into account by simulations. System timing budgets should include margin for SSO effects.

Stub — The branch from the bus trunk terminating at the pad of an agent.

Trunk — The main connection, excluding interconnect branches, from one end

System Management Bus — A two-wire interface through which various system components may communicate.

Undershoot — The minimum voltage extending below VSS observed for a signal at the device pad.

V_{CC} (CPU core) — V_{CC} (CPU core) is the core power for the processor. The system bus is terminated to V_{CC} (CPU core).

Victim — A network that receives a coupled crosstalk signal from another network is called the victim network.

Table 1 defines the acronyms used throughout this document.

Table 1. Acronyms (Sheet 1 of 3)

Acronym	Definition
AC	Audio Codec
ACPI	Advanced Configuration and Power Interface
AGTL	Assisted Gunning Transceiver Logic
AMC	Audio/Modem Codec.
ASF	Alert Standard Format
AMI	American Megatrends Inc. (BIOS developer)

Table 1. Acronyms (Sheet 2 of 3)

Acronym	Definition
ATA	Advanced Technology Attachment (disk drive interface)
ATX	Advance Technology Extended (motherboard form factor)
BGA	Ball Grid Array
BIOS	Built-In Self Test
CK-SSCD	Spread Spectrum Differential Clock
CMC	Common Mode Choke
CMOS	Configuration Memory Operating System
CPU	Central Processing Unit (processor)
DDR	Double Data Rate
DMI	Direct Memory Interface
ECC	Error Correcting Code
EEPROM	Electrically Erasable Programmable Read-Only Memory
EHCI	Enhanced Host Controller Interface
EMA	Extended Media Access
EMI	Electro Magnetic Interference
ESD	Electrostatic Discharge
EV	Engineering Validation
EVMC	Electrical Validation Margining Card
FIFO	First In First Out - describes a type of buffer
FS	Full-speed. Refers to USB
FSB	Front Side Bus
FWH	Firmware Hub
GMCH	Graphics Memory Controller Hub
HS	High-speed. Refers to USB
ICH	I/O Controller Hub
IDE	Integrated Drive Electronics
IMVP	Intel Mobile Voltage Positioning
IP/IPv6	Internet Protocol/Internet Protocol version 6
IrDA	Infrared Data Association
ISI	Inter-Symbol Interference
KBC	Keyboard Controller
LAI	Logic Analyzer Interface
LAN	Local Area Network
LED	Light Emitting Diode
LOM	LAN on Motherboard
LPC	Low Pin Count
LS	Low-speed. Refers to USB
LVDS	Low Voltage Differential Signalling
MC	Modem Codec
MEC	Media Expansion Card

Table 1. Acronyms (Sheet 3 of 3)

Acronym	Definition
MHz	Mega-Hertz
OEM	Original Equipment Manufacturer
PCIe	PCI Express*
PCM	Pulse Code Modulation
POST	Power On Self Test
PLC	Platform LAN Connect
RAID	Redundant Array of Inexpensive Disks
RTC	Real Time Clock
SATA	Serial ATA
SIO	Super Input/Output
SMBus	System Management Bus
SODIMM	Small Outline Dual In-line Memory Module
SPD	Serial Presence Detect
SPI	Serial Peripheral Interface
SSO	Simultaneous Switching Output
STR	Suspend To RAM
TCO	Total Cost of Ownership
TCP	Transmission Control Protocol
TDM	Time Division Multiplexed
TDR	Time Domain Reflectometry
µBGA	Micro Ball Grid Array
UDP	User Datagram Protocol
UHCI	Universal Host Controller Interface
USB	Universal Serial Bus
VGA	Video Graphics Adapter
VID	Voltage Identification
VREG	Voltage Regulator
XDP	eXtended Debug Port

1.4 Support Options

1.4.1 Electronic Support Systems

Intel's web site (http://www.intel.com/) provides up-to-date technical information and product support. This information is available 24 hours per day, 7 days per week, providing technical information whenever you need it.

Product documentation is provided online in a variety of web-friendly formats at:

http://www3.hibbertgroup.com/intel/main

1.4.2 Additional Technical Support

If you require additional technical support, please contact your Intel Representative or local distributor.

1.5 Product Literature

You can order product literature from the following Intel literature centers:

Table 2. Intel Literature Centers

Location	Telephone Number
U.S. and Canada	1-800-548-4725
U.S. (from overseas)	708-296-9333
Europe (U.K.)	44(0)1793-431155
Germany	44(0)1793-421333
France	44(0)1793-421777
Japan (fax only)	81(0)120-47-88-32

1.6 Related Documents

The table below provides a summary of publicly available documents related to this development kit. For additional documentation, please contact your Intel Representative.

Table 3. Related Documents

Document Title	Location
Mobile Intel® 945 Express Chipset Family Datasheet	http://www.intel.com/design/mobile/datashts/309219.htm
Intel® I/O Controller Hub 7 (ICH7) Family Datasheet	http://www.intel.com/design/chipsets/datashts/307013.htm
Mobile Intel® 945 Express Chipset Family Specification Update	http://www.intel.com/design/mobile/specupdt/309220.htm
Intel® Centrino® Duo Processor Technology Design Guide	Order Number 654938[1]

Note:
1. Contact your Intel representative for access to this document.

2.0 Getting Started

This chapter identifies the evaluation kit's key components, features and specifications. It also details basic board setup and operation.

2.1 Overview

The evaluation board consists of a baseboard populated with the Intel® Core™ 2 Duo processor and the Intel® 945GME Express Chipset, other system board components, and peripheral connectors.

Note: The evaluation board is shipped as an open system allowing for maximum flexibility in changing hardware configuration and peripherals. Since the board is not in a protective chassis, take extra precaution when handling and operating the system.

2.1.1 Intel® 945GME Express Chipset Development Kit Features

Features of the development kit board are summarized below:

Processor

- Intel® Core™ 2 Duo processor with 4 MByte L2 Cache on 65nm process in the 478 pin Flip Chip Pin Grid Array (Micro-FCPGA) package

Mobile Intel® 945GME Express Graphics Memory Controller Hub (945GME Express GMCH)

- 1466 pin Micro-FCBGA Package
- Supports a 533/667 MHz front side bus
- Supports dual-Channel DDR2 at 400/533/667 MHz
- Two SODIMM slots (one per channel) support DDR2 SODIMMS (unbuffered, non-ECC) modules
- Supports 128 MBytes to 4 GBytes using 256 Mbit, 512 Mbit, or 1 Gbit technology
- x16 PCI Express* Graphics or Serial Digital Video Out (SDVO) port
- 18 bpp LVDS, VGA & TV-D connector support

I/O Controller Hub 7 (ICH7-M)

- 652 pin plastic BGA package
- DMI (x4) interface with GMCH
- Two SATA and one IDE (40 pin) Hard Drive interface
- Two PCI 2.3 compliant desktop slots
- 82802AC8 Firmware Hub (FWH)
- 82573E Gigabit Ethernet Controller

- Two x1 PCI Express* slots.

Note: There are actually three x1 PCI Express* slots but slot 2 was used for validation purposes. Only slots 0 and 1 are supported.

Clocking

- CK-410M and CK-SSCD
- Battery-backed real time clock

Connector Interface Summary

- One x16 PCI Express* Video Interface, doubles as an MEC connector to provide access to dual SDVO ports if PCI Express* is unused
- Two SATA ports
- One Ultra ATA (33/66/100) IDE connector supporting up to two IDE devices
- Eight Universal Serial Bus (USB) 2.0 ports (Five ports provided on rear-panel, three provided via headers (J6H2, J7E2)
- Two PCI 2.3 compliant 33 MHz interface connectors
- PS/2-style keyboard and PS/2 mouse (6-pin mini-DIN) connectors
- TV Out D-connector at back panel interface
- LVDS connector on top of circuit board near GMCH (J5F1)
- One VGA connector provides access to integrated graphics
- One LAN connector providing 10/100/1000 Mbps connectivity from the Intel 82573E Gigabit Ethernet Controller
- One 9-pin serial port connector.
- One IrDA port (U4A1)
- Two PCI Express* slots (x1)
- Two SODIMM connectors on rear side of circuit board

Debug Features

- Extended Debug Port (XDP) connector
- On-board Port 80h display

Miscellaneous Features

- Configurable for ATX 1.1 Power Supply in desktop mode or AC Mobile Brick/Battery Pack for Mobile Mode
- ATX Form Factor eight layer PCB
- AMI* system BIOS
- Two built-in fan power connectors: Chassis Fan and CPU Fan
- Power/Reset buttons
- CMOS clear jumper
- BIOS recovery jumper
- Boot Block protection jumper
- Support for Serial, IrDA, serial mouse, and keyboard

2.2 Included Hardware and Documentation

The following hardware and documentation is included in the development kit:

- One Intel® 945GME Express Chipset Development Kit board
- One Intel® Core™ 2 Duo processor with 4 MB L2 Cache on 65nm process in the 478 pin Flip-Chip Pin Grid Array (Micro-FCPGA) package (Installed)
- One Intel® Core™ Duo processor with 2 MByte L2 Cache on 65 nm process in the 478 pin Flip Chip Pin Grid Array (Micro-FCPGA) package (included in kit box for evaluation– not populated on board)
- One Firmware Hub (FWH) (Installed)
- One GMCH (945GME) heat sink (Installed)
- One Type 2032, socketed 3 V lithium coin cell battery (Installed)
- One DDR2 SODIMM (200 Pin)
- One CPU thermal solution and CPU back plate (included in kit box – not populated on board)
- One hard drive
- One cable kit

2.3 Software Key Features

The driver CD included in the kit contains all of the software drivers necessary for basic system functionality under the following operating systems: Windows* 2000/XP/XP Embedded, and Linux*.

Note: While every care was taken to ensure the latest versions of drivers were provided on the enclosed CD at time of publication, newer revisions may be available. Updated drivers for Intel components can be found at: http://developer.intel.com/design/intarch/software/index.htm

For all third-party components, please contact the appropriate vendor for updated drivers.

Note: Software in the kit is provided free by the vendor and is only licensed for evaluation purposes. Refer to the documentation in your evaluation kit for further details on any terms and conditions that may be applicable to the granted licenses. Customers using the tools that work with Microsoft* products must license those products. Any targets created by those tools should also have appropriate licenses. Software included in the kit is subject to change.

Refer to http://developer.intel.com/design/intarch/devkits for details on additional software from other third-party vendors.

2.3.1 AMI* BIOS

This development kit ships pre-installed with AMI* BIOS pre-boot firmware from AMI*. AMI* BIOS provides an industry-standard BIOS platform to run most standard operating systems, including Windows* 2000/XP/XP Embedded, Linux*, and others.

The AMI* BIOS Application Kit (available through AMI*) includes complete source code, a reference manual, and a Windows-based expert system, BIOStart*, to enable easy and rapid configuration of customized firmware for your Intel® 945GME Express Chipset.

The following features of AMI* BIOS are enabled in the Intel® 945GME Express Chipset:

- DDR2 SDRAM detection, configuration, and initialization
- Intel® 945GME Express Chipset configuration
- POST codes displayed to port 80h
- PCI/PCI Express* device enumeration and configuration
- Integrated video configuration and initialization
- Super I/O configuration
- CPU microcode update
- Active Management Technology
- RAID 0/1 Support

2.4 Before You Begin

Additional hardware may be necessary to successfully set up and operate the evaluation board.

VGA Monitor: Any standard VGA or multi-resolution monitor may be used. The setup instructions in this chapter assume the use of a standard VGA monitor, TV, or flat panel monitor.

Keyboard: The evaluation board can support either a PS/2 or USB style keyboard.

Mouse: The evaluation board can support either a PS/2 or USB style mouse.

Hard Drives and Optical Disc Drives: Up to two SATA drives and two IDE devices (master and slave) may be connected to the evaluation board. An optical disc drive may be used to load the OS. All these storage devices may be attached to the board simultaneously.

Video Adapter: Integrated video is provided on the back panel of the evaluation board. Alternately, a standard PCI Express* video adapter or an MEC video adapter may be used for additional display flexibility. Please contact the respective vendors for drivers and necessary software for adapters not provided with this development kit. Check the BIOS for the proper video settings. See Section 2.6, “Configuring the BIOS” on page 21 for more information.

Note: The enclosed driver CD includes drivers necessary for LAN, Integrated graphics, and system INF utilities.

Network Adapter: A Gigabit network interface is provided on the evaluation board. The network interface will not be operational until after all the necessary drivers have been installed. A standard PCI/PCI Express* adapter may be used in conjunction with, or in place of, the onboard network adapter. Please contact the respective vendors for drivers and necessary software for adapters not provided with this development kit.

You must supply appropriate network cables to utilize the LAN connector or any other installed network cards.

Power Supply: The Intel® **945GME Express Chipset** has the option to be powered from two different power sources: an ATX power supply, or ‘Mobile Brick’. The Intel® **945GME Express Chipset** contains all of the voltage regulators necessary to power the system.

There are two main supported power supply configurations, Desktop and Mobile. The Desktop solution consists of only using the ATX power supply. The Mobile solution consists of only using the AC Brick.

Note: Desktop peripherals, including add-in cards, will not work in mobile power mode. If desktop peripherals are used, the platform must be powered using desktop power mode. The AC Brick power supply configuration does not provide the 12 V supply required by most desktop peripherals.

Note: Select a power supply that complies with the "ATX12V" 1.1 specification. For more information, refer to http://www.formfactors.org.

Note: If the power button on the ATX power supply is used to shut down the system, wait at least five seconds before turning the system on again to avoid damaging the system.

Other Devices and Adapters: The evaluation board functions much like a standard desktop computer motherboard. Most PC-compatible peripherals can be attached and configured to work with the evaluation board.

2.5 Setting Up the Evaluation Board

Once the necessary hardware (described in Section 2.4) has been gathered, follow the steps below to set up the Intel® 945GME Express Chipset evaluation board.

Note: To locate items discussed in the procedure below, please refer to Section 4.0.

1. Create a safe work environment.
   Ensure a static-free work environment before removing any components from their anti-static packaging. The evaluation board is susceptible to electrostatic discharge (ESD) damage, and such damage may cause product failure or unpredictable operation. A flame retardant work surface must also be used.

Caution: ***Because of this susceptibility, it is recommended that an ESD wrist strap be used when handling the board.***

2. Inspect the contents of your kit.
   Check for damage that may have occurred during shipment. Contact your sales representative if any items are missing or damaged.

Caution: ***Since the board is not in a protective chassis, use caution when connecting cables to this product.***

Caution: ***Standby voltage is constantly applied to the board. Therefore, do not insert or remove any hardware unless the system is unplugged.***

Note: The evaluation board is a standard ATX form factor. An ATX chassis may be used if a protected environment is desired. If a chassis is not used, standoffs must be used to elevate the board off the working surface to protect the memory and to protect from any accidental contact to metal objects.

3. Check the jumper default position setting. Refer to Figure 4 for jumper location. Jumper J6H1 is used to clear the CMOS memory. Make sure this jumper is set for normal operation.
4. Be sure to populate the following hardware on your evaluation board:
   — One Intel® Core™ 2 Duo processor
   — One processor thermal solution
   — One DDR2 SODIMM (200-pin)

Note: Ensure that the processor has been locked into the socket by turning the socket screw fully clockwise.

Note: For proper installation of the CPU thermal solution, please refer to Appendix A, "Heat Sink Installation Instructions"

5. Connect a SATA or IDE hard disk drive.
6. Connect any additional storage devices to the evaluation board.
7. Connect the keyboard and mouse.
   Connect a PS/2-style or USB mouse and keyboard (see Figure 3 on page 38 for connector locations).

Note: J1A1 (on the baseboard) is a stacked PS/2 connector. The bottom connector is for the keyboard and the top is for the mouse.

8. Connect an Ethernet cable (optional).
9. Connect the monitor through the VGA connector.
10. Connect the power supply.
    Connect an appropriate power supply to the evaluation board. Make sure the power supply is not plugged into an electrical outlet (turned off). After connecting the power supply board connectors, plug the power supply cord into an electrical outlet.
11. Power up the board.
    Power and Reset are implemented on the evaluation board through buttons located on SW1C1and SW1C2, respectively. See Figure 5 on page 42 for switch locations.
    Turn on the power to the monitor and evaluation board. Ensure that the fansink on the processor is operating.

Note: Note that the power button may have to be pressed twice to turn the power on.

12. Install operating system and necessary drivers
    Depending on the operating system chosen, all necessary drivers for components included in this development kit can be found on the enclosed CD. Please see Section 2.3 for information on obtaining updated drivers.

2.6 Configuring the BIOS

AMI* BIOS is pre-loaded on the evaluation board. The default BIOS settings may need to be modified to enable/disable various features of the evaluation board. The setup program can be used to modify BIOS settings and can be accessed during the Power On Self Test (POST). Setup options are configured through a menu-driven user interface. For AMI BIOS POST codes, visit:

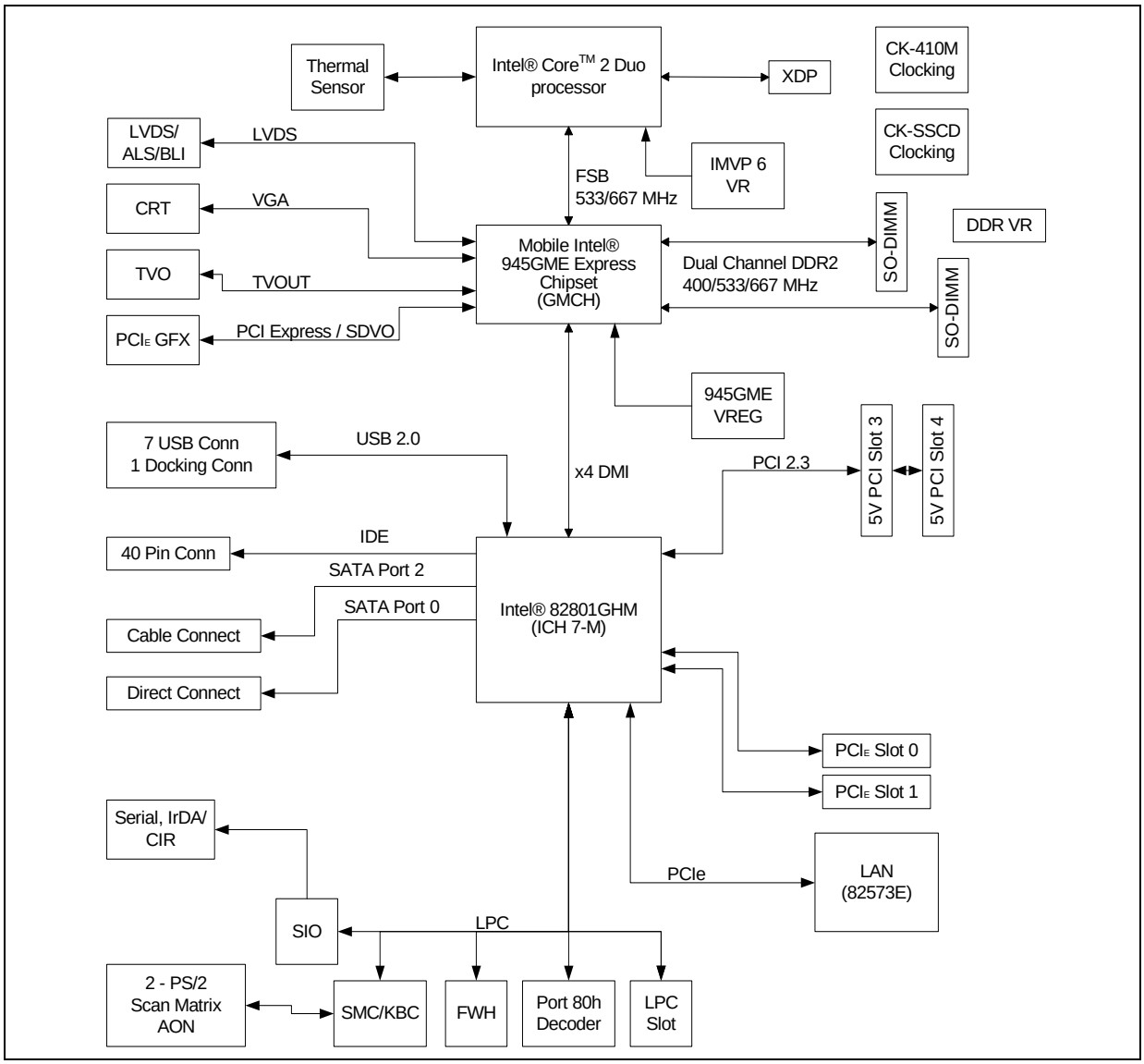
http://www.ami.com

For BIOS Updates please contact your Intel Sales Representative.

3.0 Theory of Operation

3.1 Block Diagram

Figure 1. Intel® 945GME Express Chipset Development Kit Block Diagram



3.2 Mechanical Form Factor

The evaluation board conforms to the ATX form factor. For extra protection in a development environment, you may want to install the evaluation board in an ATX chassis. Internal and rear panel system I/O connectors are described in Section 3.4.3. An overview of connector and slot locations is provided in Section 4.0.

3.3 Thermal Management

The objective of thermal management is to ensure that the temperature of each component is maintained within specified functional limits. The functional temperature limit is the range within which the electrical circuits can be expected to meet their specified performance requirements. Operation outside the functional limit can degrade system performance and cause reliability problems.

The development kit is shipped with a fansink thermal solution for installation on the processor. This thermal solution has been tested in an open-air environment at room temperature and is sufficient for evaluation purposes. The designer must ensure that adequate thermal management is provided for any customer-derived designs.

3.4 System Features and Operation

The following sections provide a detailed view of system features and operation. Refer to Figure 2 and Table 7 for the location of the major components of the platform.

The Intel® 945GME Express Chipset features the 82945GM Graphics Memory Controller Hub and the Intel® I/O Controller Hub (ICH7-M).

3.4.1 Intel(R) 945GME GMCH

The Intel® 945GME Express Chipset GMCH provides the processor interface optimized for Intel® Core™ 2 Duo processors, system memory interface, DMI and internal graphics. It provides flexibility and scalability in graphics and memory subsystem performance. The following list describes the reference board's implementation of the Intel® 945GME Express Chipset GMCH features.

A list of features follows:

- 1466 Micro-FCBGA package
- 533/667 MHz Front Side Bus
- 36-bit host bus addressing
- System memory controller (DDR2 implemented)
  - — Supports Dual Channel and Single Channel operation
  - — Two 200-pin SODIMM slots
  - — DDR2 400/533/667
- Direct Media Interface (DMI)
- Integrated graphics based on Intel's Graphics Media Accelerator 950
  - — Directly supports on-board VGA, S-Video and LVDS interfaces.
  - — Supports resolutions up to 2048 x 1536 @ 75 Hz.
- SDVO interface via PCI Express* x16 connector provides maximum display flexibility
  - — Can drive up to two display outputs

3.4.1.1 System Memory

The evaluation board supports DDR2 400/533/667 main memory. Two 200-pin SODIMM connectors (one per channel) on the board support unbuffered, non-ECC, single and double-sided DDR2 400/533/667 MHz SODIMMs. These SODIMMs provide the ability to use up to 1 Gbit technology for a maximum of 4 GBytes system memory.

Note: Memory that utilizes 128 MBit technology is not supported on the Intel® 945GME Express Chipset.

Note: The SODIMM connectors are on the back side of the board.

Caution: Standby voltage is applied to the SODIMM sockets when the system is in the S3 state. Therefore, do not insert or remove SODIMMs unless the system is unplugged.

3.4.1.2 DMI

The Intel® 945GME Express Chipset GMCH's Direct Media Interface (DMI) provides high-speed bi-directional chip-to-chip interconnect for communication with the ICH7-M.

3.4.1.3 Advanced Graphics and Display Interface

The reference board has five options for displaying video, VGA, LVDS, TVOUT, SDVO, or PCI Express* Graphics. SDVO (MEC) and PCI Express* Graphics are multiplexed on the same pins within the Intel® 945GME Express Chipset. The Intel® 945GME Express Chipset contains one SDVO/PCI Express* Graphics Slot (J6C1) for a PCI Express* compatible graphics card or an SDVO compatible graphics card, one LVDS connector (J5F1), one TVOUT connector (J2A1), and one 15-pin VGA connector (J2A2B).

3.4.2 ICH7-M

The ICH7-M is a highly integrated multifunctional I/O controller hub that provides the interface to the system peripherals and integrates many of the functions needed in today's PC platforms. The following sections describe the reference board implementation of the ICH7-M features, which are listed below:

- Two PCI Express* (x1) connectors
- Two PCI connectors
- LPC interface
- System management
- ACPI* 2.0 compliant
- Real Time Clock
- 652 mBGA package
- Two SATA drive connectors
- One IDE connector
- Eight Universal Serial Bus (USB) 2.0 ports (five ports provided on rear-panel, three provided via headers (J6H2, J7E2)

3.4.2.1 PCI Express* Slots

The reference board has two x1 PCI Express* slots for add-in cards. The PCI Express* interface is compliant to the *PCI Express* Rev. 1.0a Specification*.

3.4.2.2 PCI Slots

The reference board has two PCI slots for add-in cards. The PCI bus is compliant to the PCI Rev. 2.3 Specification at 33 MHz.

3.4.2.3 On-Board LAN

The 82573E provides the LAN connectivity for this platform. It provides Gigabit ethernet as well as Intel® Active Management Technology functions. It is connected to the ICH7-M through a PCIe interface and to an RJ45 connector at J5A1A with built in magnetic decoupling. Access to this interface is provided on the rear I/O panel (See Figure 3 on page 38).

Features of the 82573E are as follows:

- x1 PCIe Interface
- 2 Gbps peak bandwidth per direction
- Wide, pipelined internal data path architecture
- 32 KB configurable Receive (Rx) and Transmit (Tx) FIFO
- IEEE 802.3x compliant flow control support with software controllable pause times and threshold values
- Programmable host memory Rx buffers (256 B- 16 KB)
- Descriptor ring management hardware for Tx and Rx
- Tx/Rx IP, TCP, and UDP checksum offloading
- Tx TCP Segmentation
- IPv6 offloading
- Intel® Active Management Technology
- Wake on LAN (WoL) support

Note: The 82573E is only powered in S3-S0 and will not support AMT or WoL support from S4 or S5.

- SPI or EEPROM support
- Optional on-die voltage regulator

Information on Intel® Active Management Technology can be found at:

http://www.intel.com/technology/manage/iamt/

3.4.2.4 AC'97 and High Definition Audio

AC'97 and Intel® High Definition Audio are not supported on the board.

3.4.2.5 ATA / Storage

The Intel® 945GME Express Chipset provides one parallel ATA IDE connector and two serial ATA connectors. The parallel ATA IDE Connector is a standard 40-pin connector at J7J1 for a desktop IDE drive. A power connector is supplied on the platform to power a parallel ATA hard disk drive at J4J2. One of the two serial ATA connectors on the Intel® 945GME Express Chipset is a direct connect connector; located at J8J2. The other serial ATA connector is broken up into two connectors. One connector is for the serial data signals, and the other is to power the serial ATA hard disk drive. These connectors are located at J7H1 and J6H3. A green LED at location CR7J1 indicates activity on the ATA channel.

The Intel® 945GME Express Chipset also supports 'ATA swap' capability for both the parallel IDE channel and the serial ATA channels. A device can be powered down by software and the port can then be disabled, allowing removal and insertion of a new device. The parallel IDE device should be powered from the power connector, J4J2, on the Intel® 945GME Express Chipset to utilize the hot swap feature. This feature requires customer-developed software support.

Desktop hard drives must be powered using the external ATX power supply, not the onboard power supply.

The Intel® 945GME Express Chipset includes Intel® Matrix Storage Technology, providing greater performance and reliability through features such as Native Command Queuing (NCQ) and RAID 0/1. For more information about Intel® Matrix Storage Technology, refer to Intel's website at:

http://www.intel.com/design/chipsets/matrixstorage_sb.htm

3.4.2.6 USB Connectors

The ICH7-M provides a total of eight USB 2.0 ports. Three ports are routed to a triple-stack USB connector at J3A1. Two ports are routed to a combination RJ-45/dual USB connector at J5A1B. Three ports are routed to USB front panel headers at J6H2 and J7E2.

3.4.2.7 LPC Super I/O (SIO)/LPC Slot

An SMSC LPC47N207 serves as the SIO on the Intel® 945GME Express Chipset platform. Shunting the jumper at J7E3 to the 2-3 positions can disable the SIO by holding it in reset. This allows other SIO solutions to be tested in the LPC slot at J8F1. A sideband header is provided at J9G2 for this purpose. This sideband header also has signals for LPC power management. Information on this header is on sheet 35 of the Intel® 945GME Express Chipset schematics and is detailed in the "LPC Slot and Sideband Header Specification" (refer to Table 3, "Related Documents" on page 15).

3.4.2.8 Serial, IrDA

The SMSC SIO incorporates a serial port, and IrDA (Infrared), as well as general purpose IOs (GPIO). The serial port connector is provided at J2A2A, and the IrDA transceiver is located at U4A1. The IrDA transceiver on Intel® 945GME Express Chipset supports both SIR (slow IR) and CIR (Consumer IR). The option to select between the two is supported through software and GPIO pin on the SIO.

3.4.2.9 BIOS Firmware Hub (FWH)

The 8 Mbit Flash device used on the Intel® 945GME Express Chipset to store system and video BIOS as well as an Intel Random Number Generator (RNG) is a socketed E82802AC8 a 32-pin PLCC package. The reference designator location of the FWH device is U8G1. The BIOS can be upgraded using an MS-DOS* based utility and is addressable on the LPC bus off of the ICH7-M.

3.4.2.10 System Management Controller (SMC)/Keyboard Controller

The Hitachi* H8S/2104V serves as both SMC and KBC for the platform. The SMC/KBC controller supports two PS/2 ports, battery monitoring and charging, EMA support, wake/runtime SCI events, and power sequencing control. The two PS/2 ports on the Intel® 945GME Express Chipset are for legacy keyboard and mouse. The keyboard plugs into the bottom jack and the mouse plugs into the top jack at J1A1. Scan matrix keyboards can be supported via an optional connector at J9E1.

3.4.2.11 Clocks

The Intel® 945GME Express Chipset board uses a CK-410M and CK-SSCD compatible solution. The CK-SSCD solution offers improved EMI performance by spreading the radiated clock emissions over a wider spectrum than a single frequency. This is accomplished while controlling the clock frequency deviation such that system performance is not compromised. The FSB frequency is determined from decoding the processor BSEL[2:0] pin settings.

3.4.2.12 Real Time Clock

An on-board battery at BT5H1 maintains power to the real time clock (RTC) when in a mechanical off state. A CR2032 battery is installed on the Intel® 945GME Express Chipset development kit.

3.4.2.13 Thermal Monitoring

The processor has a thermal diode for temperature monitoring. The SMC thermal monitoring device will throttle the processor if it becomes hot. If the temperature of the processor rises too high, the SMC will alternately blink the CAPS lock and NUM lock LEDs on the board, and the board will shut down.

3.4.3 System I/O and Connector Summary

The evaluation board provides extensive I/O capability in the form of internal connectors and headers as detailed by the following list. For detailed information on these connectors and headers, please refer to "Hardware Reference" on page 35.

- One (x16) PCI Express* connector
- Two (x1) PCI Express* connectors
- Two PCI connectors
- One IDE connector (supports two drives)
- Two SATA connectors
- Two USB ports via front panel header (J8J1)
- One LVDS video connector

In addition to the internal I/O connections listed above, the evaluation board also contains the following I/O on the rear panel (as illustrated in Figure 3 on page 38).

- Five USB ports on back panel.
- VGA connector
- PS/2-style keyboard and mouse ports
- LAN connector
- One 9-pin serial connector
- One IrDA port
- One TV D-connector

3.4.3.1 PCI Express* Support

The evaluation board provides access to one x16 PCI Express* connector. Any industry standard x16 PCI Express* video adapter may be used with this interface. The evaluation board also provides access to two x1 PCI Express* connectors. Any industry standard x1 PCI Express* adapter may be used with these interfaces.

3.4.3.2 SATA Support

The evaluation board provides support for up to two SATA disk drives. The SATA controllers are software compatible with IDE interfaces, while providing lower pin counts and higher performance.

These are two SATA connectors on the evaluation board. The SATA Cable connect provides both signalling and power white the SATA Direct connect only provides signals (the user typically uses an ATX power supply for the drive power).

3.4.3.3 IDE Support

The evaluation board has a 40-pin connector for the ICH7-M's integrated IDE controller. This connector supports up to two Ultra ATA/100 hard drives; one master and one slave.

Note: Desktop hard drives must be powered by an external ATX power supply.

3.4.3.4 USB Ports

The evaluation board provides five USB (2.0) ports on the rear panel and three additional ports through headers (J6H2 and J7E2).

There are four UHCI Host Controllers and an EHCI Host Controller. Each UHCI Host Controller includes a root hub with two separate USB ports each, for a total of eight legacy USB ports.

The EHCI Host Controller includes a root hub that supports up to eight USB 2.0 ports. The connection to either the UHCI or EHCI controllers is dynamic and dependant on the particular USB device. As such, all ports support High Speed, Full Speed, and Low Speed (HS/FS/LS).

3.4.3.5 VGA Connector

A standard 15 pin D-Sub connector on the rear panel provides access to the analog output of the Intel® 945GME Express Chipset. The integrated graphics supports a maximum resolution of 2048 x 1536 @ 75Hz. This can be connected to any capable analog CRT or flat panel display with analog input.

When used in conjunction with the other display options, the displays can operate in Dual Independent mode. This allows unique content to appear on each display at unique refresh rates and timings.

3.4.3.6 Keyboard / Mouse

The keyboard and mouse connectors are PS/2 style, six-pin stacked miniature D-Sub connectors. The top connector is for the mouse and the bottom connector is for the keyboard.

3.4.3.7 32 bit / 33 MHz PCI Connectors

Two industry standard 32 bit/33 MHz PCI connectors are provided on the evaluation board. These slots support 5 V devices.

3.4.3.8 Ethernet Gigabit LAN Interface connector

The evaluation board provides one industry standard Gigabit RJ45 LAN Interface Connector (Integrated with the dual USB connector).

3.4.3.9 LVDS Flat Panel Display Interface

The evaluation board provides one forty-four pin LVDS video interface connector. The provided LVDS connects to most 18 bits per pixel (bpp) flat panel display assemblies. 24 bpp LVDS is not supported.

3.4.4 POST Code Debugger

A port 80-83 display at CR6A1, CR6A2, CR6A3, and CR6A4 show the POST codes and can be used for debug information during POST. The evaluation board uses an AMI* BIOS.

For AMI* BIOS POST codes, please visit: http://www.ami.com

3.5 Clock Generation

The Intel® 945GME Express Chipset board uses a CK-410M and CK-SSCD compatible solution. The FSB frequency is determined from decoding the processor BSEL[2:0] pin settings.

The clock generator provides Processor, GMCH, ICH7-M, PCI, PCI Express*, SATA, and USB reference clocks. Clocking for DDR2 is provided by the GMCH.

Table 4. Primary System Clocks

Clock Name	Speed
CPU	133 MHz @ 533 FSB Speed 166 MHz @ 667 FSB Speed
DDR2	100 MHz @ 400 Memory Speed 133 MHz @ 533 Memory Speed 166 MHz @ 667 Memory Speed
PCI Express* and DMI	100 MHz
SATA	100 MHz
PCI	33 MHz
USB	48 MHz

3.6 Power Management States

The evaluation board supports the following ACPI System states: S0 (Full On), S3 (Suspend to RAM), S4 (Suspend to disk), and S5 (Soft-off), ACPI CPU states: C0 (Full On), C1 (Auto Halt), C2 (Stop Grant), C3 (Deep Sleep), and C4 (Deeper Sleep), and ACPI Global Power States: G0 (Working), G1 (Sleeping), G2 (Soft Off), and G3 (Mechanical Off). Transition requirements are detailed below.

Table 5 lists the power management states that have been identified for the Intel® 945GME Express Chipset Platform.

Table 5. Intel® 945GME Express Chipset Development Kit Power Management States

State	Description
G0/S0/C0	Full On
G0/S0/C2	STPCLK# signal active
G0/S0/C3	Deep Sleep: DPSLP# signal active
G0/S0/C4	Deeper Sleep: DPRSLP# signal active
G1/S3	Suspend to RAM
G1/S4	Suspend to Disk
G2/S5	Soft Off
G3	Mechanical Off

3.6.1 Transition to S3

If enabled, the transition to S3 from the full-on state can be accomplished in the following ways:

- The OS performs the transition through software.
- Press the front panel power button for less than four seconds (assuming the OS power management support has been enabled).

Note: The power button is accessed by adding a switch to the pins 5 and 6 on the front panel header J8J1.

3.6.2 Transition to S4

"Wake on S4" (Suspend to disk) is controlled by the operating system.

3.6.3 Transition to S5

The transition to S5 is accomplished by the following means:

- Press the front panel power button for less than four seconds (if enabled through the OS).
- Press the front panel power button for more than four seconds to activate power button override.

3.6.4 Transition to Full-On

The transition to the Full-On state can be from S3 or S5. The transition from S3 is a low latency transition that is triggered by one of the following wake events:

- Power management timer expiration
- Real Time Clock (RTC) triggered alarm
- Power button activation
- USB device interrupt
- ICH7M pin PME# assertion
- AC power loss

For AC power loss, the system operation is defined by register settings in the Intel ICH7-M. Upon the return of power, a BIOS option, set prior to the power loss, allows the system to either go immediately to the S5 state, or reboot to the Full-On state, no matter what the state was before the power loss. External logic for this functionality is not necessary. If the BIOS remains in the S5 state after AC power loss, only the power button or the RTC alarm can bring the system out of the S5 state. The status of enabled wake events will be lost.

3.7 Power Measurement Support

Power measurement resistors are provided on the platform to measure the power of most subsystems. All power measurement resistors have a tolerance of 1%. The value of these power measurement resistors are 2 mΩ by default. Power on a particular subsystem is calculated using the following formula:

$$P = \frac{V^2}{R}$$

R is the value of the sense resistor (typically 0.002 Ω)

V is the voltage measured across the sense resistor.

It is recommended that the user use an oscilloscope or high precision digital multi-meter tool such as the Agilent* 34401A digital multi-meter. Such a meter has 6½ digits of accuracy and can provide a much greater accuracy in power measurement than a common 3½ digit multimeter.

Table 6 summarizes the voltage rails and power measurement sense resistors located on the Intel® 945GME Express Chipset platform. All sense resistors are 0.002 Ω unless otherwise noted. Please note that many voltage rails do not have sense resistors.

Table 6. Intel® 945GME Express Chipset Development Kit Voltage Rails (Sheet 1 of 3)

Voltage Groups	Voltage Rail	Sense Resistor	Powered during System States
0.9V	+V0.9	R4N4	S0,S3
1.05V Switched	+V1.05S	R4V4	S0
1.2V	+V1.2_LAN	R8A2	S0,S3
1.5V Always	+V1.5A_AZ_IO		S0,S3,S4,S5
	+V1.5A_PWRGD		S0,S3,S4,S5
1.5V Switched	+V1.5S	R5F4	S0
	+V1.5S_3GPLL	R6D8	S0
	+V1.5S_AUX	R6D6	S0
	+V1.5S_DPLLA		S0
	+V1.5S_DPLLB		S0
	+V1.5S_HPLL		S0
	+V1.5S_MPLL		S0
	+V1.5S_PCIE	R5E2	S0
	+V1.5S_PCIE_ICH		S0
	+V1.5S_QTVDAC and +V1.5S_TVDAC	R5F3	S0
1.8V	+V1.8	R5N2	S0,S3
2.5V	+V2.5_LAN	R7M2	S0,S3
	+VLAN_2.5-3.3		S0,S3
2.5V Switched	+V2.5S		S0
	+V2.5S_CRTDAC		S0
	+V2.5S_PWRGD		S0
3.3V	+V3.3		S0,S3
3.3V Always	+V3.3A		S0,S3,S4,S5
	+V3.3A/1.5A_AZ_IO		S0,S3,S4,S5
	+V3.3A_MBL		S0,S3,S4,S5
	+V3.3A_RTC		S0,S3,S4,S5
3.3V Switched	+V3.3S		S0
	+V3.3_PCISLT3	R9B3	S0
	+V3.3S/1.5S_AZ_IO	R8F8	S0
	+V3.3S_DB800_VDDA		S0

Table 6. Intel® 945GME Express Chipset Development Kit Voltage Rails (Sheet 2 of 3)

Voltage Groups	Voltage Rail	Sense Resistor	Powered during System States
	+V3.3S_PEG	R6C2	S0
	+V3.3S_PWRGD		S0
	+V3.3S_SATA_P0		S0
	+V3.3S_SATA_P2		S0
	+V3.3S_TVDAC		S0
	+V3.3S_TVDAC_LDO	R4F2	S0
	+V3.3S_TVDACA		S0
	+V3.3S_TVDACB		S0
	+V3.3S_TVDACC		S0
	+VCCA_TVDAC		S0
5V	+V5		S0,S3
5V Always	+V5A		S0,S3,S4,S5
	+V5A_MBL	R3V4	S0,S3,S4,S5
5V Switched	+V5S		S0
	+V5_PCISLT3	R8B5	S0
	+V5S_F_DAC		S0
	+V5S_IMVP6	R1B2	S0
	+V5S_L_DAC		S0
	+V5S_PATA		S0
	+V5S_PWRGD		S0
	+V5S_SATA_P0		S0
	+V5S_SATA_P2		S0
	+V5SB_ATXA		S0
	V5S_FAN		S0
-12V Always	-V12A		S0,S3,S4,S5
-12V Switched	-V12S		S0
+12V SWITCHED	+V12S		S0
	+V12S_PATA		S0
	+V12S_PEG	R6N6	S0
	+V12S_SATA_P0		S0
	+V12S_SATA_P2		S0
AC Power Brick	+V_BC_OUT		S0,S3,S4,S5
	+VAC_IN		S0,S3,S4,S5
	+VAC_IN_L		S0,S3,S4,S5
	+VCHGR_OUT		S0,S3,S4,S5
Battery Voltage	+VBAT		S0,S3,S4,S5
	+VBAT_S4		S0,S3,S4,S5
	+VDC_PHASE	R1B3	S0,S3,S4,S5
Battery Voltage Always	+VBATA		S0,S3,S4,S5

Table 6. Intel® 945GME Express Chipset Development Kit Voltage Rails (Sheet 3 of 3)

Voltage Groups	Voltage Rail	Sense Resistor	Powered during System States
Battery Voltage Switched	+VBATS		S0
	+VBS		S0
Processor Core	+VCC_CORE		S0

4.0 Hardware Reference

This section provides reference information on the hardware, including locations of evaluation board components, connector pinout information and jumper settings. Figure 2 provides an overview of basic board layout.

4.1 Primary Features

Figure 2 shows the major components of the Intel® 945GME Express Chipset board and Table 7 gives a brief description of each component.

Figure 2. Intel® 945GME Express Chipset Component Locations

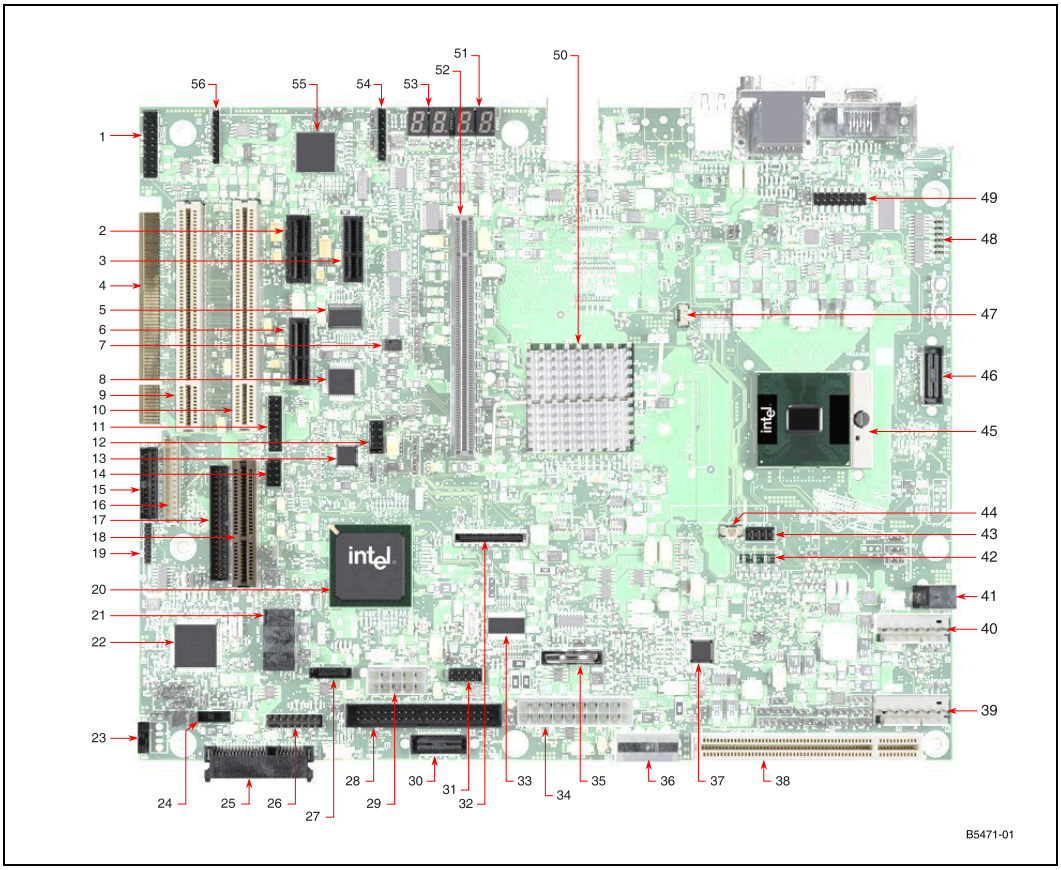


Table 7. Intel® 945GME Express Chipset Component Location Legend (Sheet 1 of 2)

No.	Default Setting	Reference Designator
1	Reserved	J9A2
2	PCI Express* Slot 0	J8C1
3	PCI Express* Slot 1	J7C1
4	Reserved	S9C1
5	DB800 Clock Buffer	U7D1
6	Reserved	J8D1
7	CK-SSCD	U7D3
8	Port 80 Controller	U7D10
9	PCI Slot 4	J9B1
10	PCI Slot 3	J8B1
11	Reserved	J8E1
12	Reserved	J7E2
13	SMSC SIO	U7E4
14	Reserved	J8E2
15	Reserved	J9E2
16	Keyboard Scan Matrix	J9E1
17	LPC Sideband Header	J9G2
18	LPC Slot	J8F1
19	Reserved	J9G1
20	Intel® ICH7-M Digital Home	U7G1
21	Firmware Hub (FWH)	U8G1
22	KBC	U9H1
23	LID Switch	SW9J2
24	Virtual Battery Switch	SW9J1
25	SATA Direct Connect	J8J2
26	Front Panel Header	J8J1
27	SATA Cable Connect	J7H1
28	IDE (Parallel ATA)	J7J1
29	SATA Power Connector	J6H3
30	Reserved	J6J1
31	Front Panel USB	J6H2
32	LVDS Connector	J5F1
33	CK410M	U6H1
34	ATX Power Supply	J4J1
35	Battery	BT5H1
36	Parallel ATA Power	J4J2
37	4-in-1 VREG Controller	U3H1
38	Reserved	J3J3
39	Reserved	J1J1

Table 7. Intel® 945GME Express Chipset Component Location Legend (Sheet 2 of 2)

No.	Default Setting	Reference Designator
40	Reserved	J1H1
41	AC Brick Power Connector	J1G3
42	System Power State LEDs	CR2G1, CR3G1-3
43	Reserved	J3F2
44	LAI Fan Header	J3F1
45	Intel Processor	U2E1
46	XDP Connector	J1E1
47	CPU Fan Header	J3C1
48	VID LEDs	CR1B1-6, CR1C1
49	Reserved	J2B1
50	945GME GMCH	U5E1
51	Port 82-83 Display	CR6A3,4
52	PCI Express* Graphics Slot	J6C1
53	Port 80-81 Display	CR6A1,2
54	Reserved	J7A1
55	82573E Gb LAN	U8A2
56	Reserved	J9A1

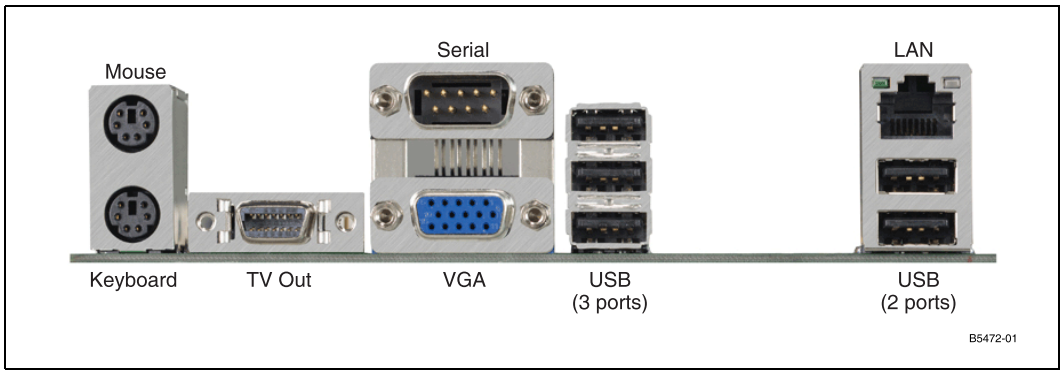
4.2 Back Panel Connectors

This section describes the Intel® 945GME Express Chipset panel connectors on the Intel® 945GME Express Chipset platform.

Note: Many of the connectors provide operating voltage (for example, +5 V DC and +12 V DC) to devices inside the computer chassis, such as fans and internal peripherals. Most of these connectors are not over-current protected. Do not use these connectors for powering devices external to the computer chassis. A fault in the load presented by the external devices could cause damage to the computer, the interconnecting cable, and the external devices themselves.

Figure 3 shows the back panel connectors to the Intel® 945GME Express Chipset platform.

Figure 3. Back Panel Connector Locations



4.3 Configuration Settings

Note: Do not move jumpers with the power on. Always turn off the power and unplug the power cord from the computer before changing jumper settings. Failure to do so may cause damage to the board.

Figure 4 shows the location of the configuration jumpers and switches.

Table 8 summarizes the jumpers and switches and gives their default and optional settings.

The unsupported jumpers must remain in their default position or the operation of the platform is unpredictable. The Intel® 945GME Express Chipset board is shipped with the jumpers and switches shunted in the default locations.

Figure 4. Configuration Jumper and Switch Locations

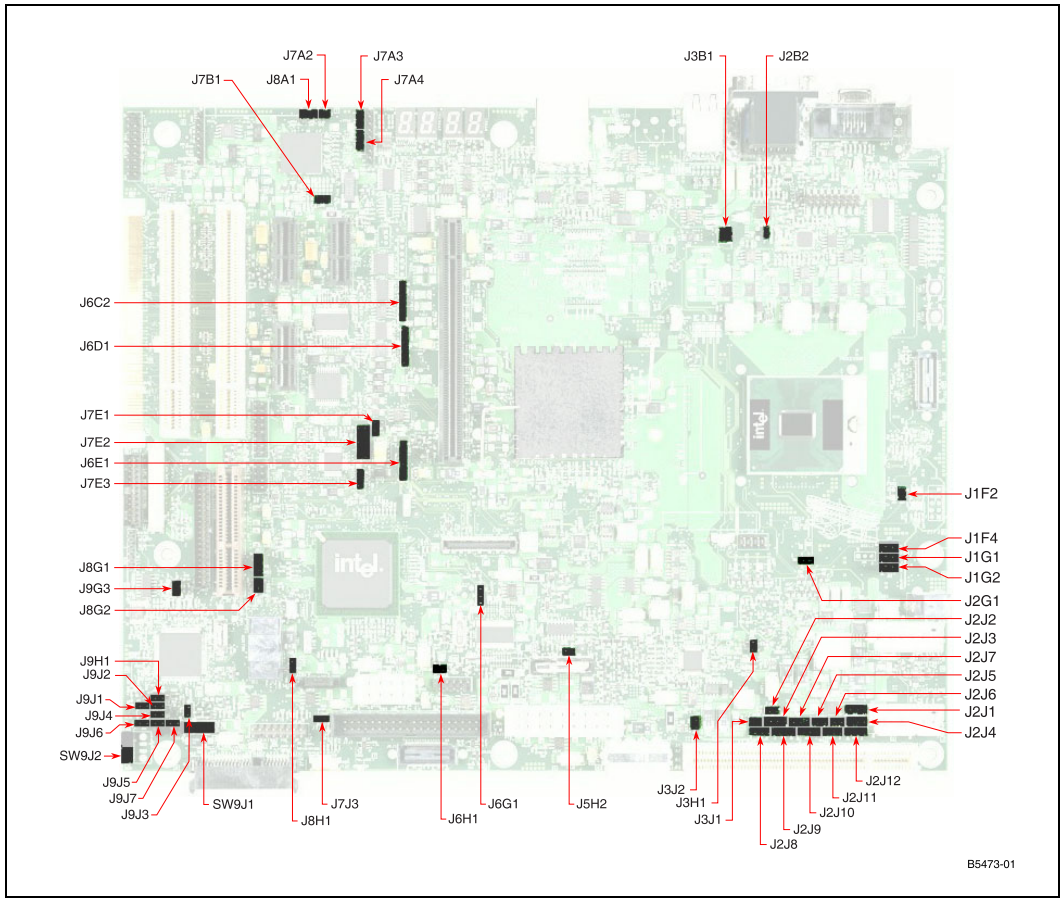


Table 8. Supported Configuration Jumper/Switch Settings (Sheet 1 of 2)

Ref Des	Function	Default Setting	Optional Setting
J1F2	Enginnering Validation (EV) Support	Out - Normal Operation	Not supported
J1F4	BSEL2	1-2 CPU Driven FSB Frequency	2-3 Force FSB Frequency - See schematic for valid combinations
J1G1	BSEL1	1-2 CPU Driven FSB Frequency	2-3 Force FSB Frequency - See schematic for valid combinations
J1G2	BSEL0	1-2 CPU Driven FSB Frequency	2-3 Force FSB Frequency - See schematic for valid combinations
J2B2	IMVP-6 Test	Out - Normal Operation	Not supported
J2G1	CPU Clock Test	Out - Normal Operation	Not supported
J2J1	EV Support	Out - Normal Operation	Not supported
J2J10	CRB/System Validation (SV) Detect	2-3 - Normal Operation	Not supported
J2J11	EV Support	Out - Normal Operation	Not supported
J2J12	EV Support	Out - Normal Operation	Not supported
J2J2	EV Support	Out - Normal Operation	Not supported
J2J3	EV Support	Out - Normal Operation	Not supported
J2J4	EV Support	Out - Normal Operation	Not supported
J2J5	EV Support	Out - Normal Operation	Not supported
J2J6	EV Support	Out - Normal Operation	Not supported
J2J7	EV Support	Out - Normal Operation	Not supported
J2J8	EV Support	Out - Normal Operation	Not supported
J2J9	EV Support	Out - Normal Operation	Not supported
J3B1	Thermal Diode Connection	1-2 Connect CPU THERMDA to Sensor 3-4 Connect CPU THERMDC to Sensor	Out - Disconnect CPU from Thermal Sensor Out - Disconnect CPU from Thermal Sensor
J3H1	Shutdown	Out - Normal Operation	In - Force the board to shut down
J3J1	EV Support	Out - Normal Operation	Not supported
J3J2	EV Support	Out - Normal Operation	Not supported
J5H2	SATA HotSwap	In - Normal Operation	Out - Disable SATA Hotswap
J6C2	EVMC Schmoo Header	Out - Normal Operation	Not supported
J6D1	EVMC Schmoo Header	Out - Normal Operation	Not supported
J6E1	LVDS Panel Power Jumper	2-3 and 5-6 - Normal Operation	Not supported
J6G1	EVMC Schmoo Header	Out - Normal Operation	Not supported
J6H1	CMOS Clear	Out - Normal Operation	In - Clear the CMOS
J7A2	82573E PHY Test	Out - Normal Operation	Not supported
J7A3	KBC Program	1-2 Normal Operation	2-3 Connect RxD to KBC for programming
J7A4	KBC Program	1-2 Normal Operation	2-3 Connect TxD to KBC for programming
J7B1	82573E Clock View	Out - Normal Operation	Not supported
J7E1	Port80 Select	Out - Normal Operation	Not supported
J7E2	Enable SPI Boot BIOS	Out - Normal Operation	Not supported
J7E3	SuperIO Reset	1-2 Normal Operation	2-3 to hold the SIO in reset

Table 8. Supported Configuration Jumper/Switch Settings (Sheet 2 of 2)

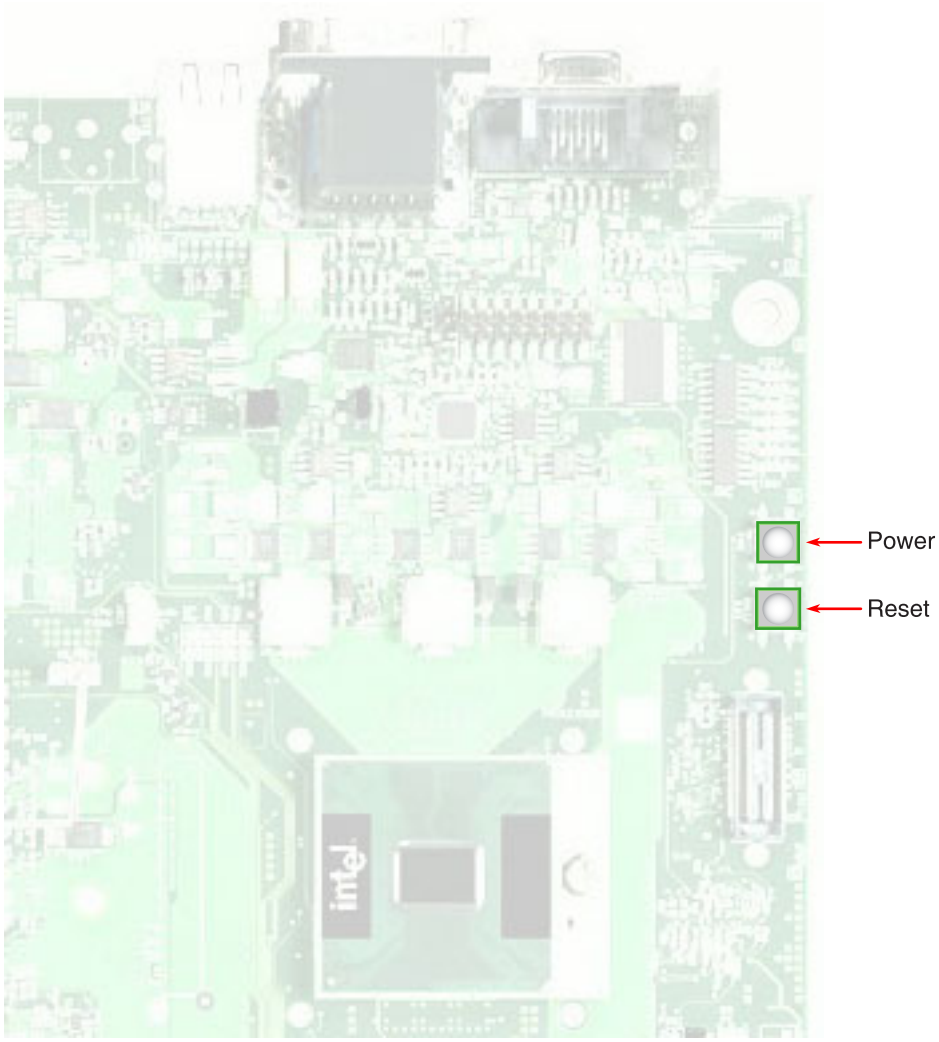
Ref Des	Function	Default Setting	Optional Setting
J7J3	PATA Hotswap	In - Normal Operation	Out - Disable PATA Hotswap
J8A1	LAN Non-volatile Memory Protect	Out - Normal Operation	Not supported
J8G1	KBC Reset	1-2 Normal Operation	2-3 to hold the KBC in reset
J8G2	SV Set Up	Out - Normal Operation	Not supported
J8H1	BIOS Recovery	Out - Normal Operation	In - Recover the BIOS
J9G3	Boot Block Program	In - Normal Operation	Not supported
J9H1	Non-Maskable Interrupt Jumper (1 Hz Clock)	Out - Normal Operation	In - Enable KBC programming
J9J1	KBC Disable	Out - Normal Operation	In - KBC Disabled
J9J2	Mode Type (MD) 0	In - Normal Operation	Not supported
J9J3	SATA Device Status	In - Normal Operation	Not supported
J9J4	MD2	Out - Normal Operation	Not supported
J9J5	LID Jumper	Out - Normal Operation	In - LID Jumper closed
J9J6	MD1	In - Normal Operation	Not supported
J9J7	Virtual Battery Jumper	Out - Normal Operation	Not supported
SW9J1	Virtual Battery Switch	1-2 Normal Operation	Not supported
SW9J2	Lid Switch	1-2 Normal Operation	2-3 LID Switch closed

4.4 Power On and Reset Buttons

The Intel® 945GME Express Chipset board has two push buttons, POWER and RESET. The POWER button releases power to the entire board, causing the board to boot. The RESET button will force all systems to warm reset. The two buttons are located near the CPU close to the edge of the board. The POWER button is located at SW1C2 and the RESET button is located at SW1C1.

Note: If the board is powered from an external ATX power supply (not a power brick), the Power button must be pressed twice to turn on the system.

Figure 5. Intel® 945GME Express Chipset Development Kit Power On and Reset Buttons



4.5 LEDs

The following LEDs provide status for various functions on the Intel® 945GME Express Chipset board.

Table 9. Intel® 945GME Express Chipset LED Function Legend

Function	LED
Keyboard Number Lock	CR9G1
Keyboard Scroll Lock	CR9G2
Keyboard Caps Lock	CR9G3
System State S0	CR3G1
System State S3	CR3G2
System State S4	CR3G3
System State S5	CR2G1
ATA Activity	CR7J1
VID 0	CR1B1
VID 1	CR1B2
VID 2	CR1B3
VID 3	CR1B4
VID 4	CR1B5
VID 5	CR1B6
VID 6	CR1C1

4.6 Other Headers, Slots, and Sockets

4.6.1 H8 Programming Headers

The microcontroller for system management/keyboard/mouse control can be upgraded in two ways. The user can either use a special MS-DOS* utility or use an external computer connected to the system via the serial port on the board.

Caution: Make sure the motherboard is not powered on and the power supply is disconnected before moving any of the jumpers.

To program the microcontroller via the utility, the user must ensure that jumper J9H1 is populated. Once the programming is complete, jumper J9H1 should be unpopulated.

If the user chooses to use an external computer connected to the system via the serial port, there are five jumpers that have to be set correctly first. Please refer to Table 10 for a summary of these jumpers and see Figure 4 for the location of each jumper.

Here is the sequence of events necessary to program the H8.

1. With the board powered off, move the five jumpers listed in Table 10 to the programming stuffing option.
2. Power the S5 voltage rails by attaching an AC brick or an ATX power supply to the system.

3. Program the H8 via the serial port.
4. Disconnect the power supply from the system.
5. With the board powered off, move the five jumpers listed in Table 10 back to the default stuffing option.

Table 10. H8 Programming Jumpers

Jumper	Reference Designator	Default Stuffing Option	Programming Stuffing Option
1Hz Clock	J9H1	Out - normal operation - clock enabled	IN - clock disabled - enable H8 programming
H8 Programming	J9J2 and J9J6	IN - normal operation and enable external H8 programming	Leave in for programming
Tx Select	J7A4	1-2 Normal Operation	2-3 connect TxD to H8 for programming
Rx Select	J7A3	1-2 normal operation (SIO)	2-3 connect RxD to H8 for programming

4.6.2 Expansion Slots and Sockets

Following is a list of the slots and sockets available for attaching additional devices. Refer to Figure 2 for locations.

Table 11. Expansion Slots and Sockets

Reference Designator	Slot/Socket Description	Detail
U2E1	478 Pin Grid Array (Micro-FCPGA) Processor Socket	
J5N1	DDR2 - Channel A - SODIMM slot	
J5P1	DDR2 - Channel B - SODIMM slot	
J5F1	LVDS Graphics Interface	
J6C1	PCI Express* (x16)	Table 12
J6C1	Media Expansion Card Slot	Table 13
J7C1	PCI Express* (x1) Slot 1	Table 14
J8C1	PCI Express* (x1) Slot 0	Table 14
J8B1	PCI 2.3 Slot 3	
J9B1	PCI 2.3 Slot 4	
J7J1	IDE Interface Connector	Table 15
J8J2	Mobile SATA Hard Drive Interface Connector	Table 18
J7H1	Desk Top SATA Hard Drive Interface Connector	Table 16
J6H3	SATA Desk Top Power Connector	Table 17
U8G1	Intel Firmware Hub Socket	
BT5H1	Battery	

4.6.2.1 478 Pin Grid Array (Micro-FCPGA) Socket

The pin locking mechanism on the CPU socket is released by rotating the screw on the socket 180 degrees counter-clockwise. CPU pins are keyed so as to only allow insertion in one orientation. DO NOT FORCE CPU into socket. Once the CPU is properly seated

into the socket, turn the screw 180 degrees clock-wise to secure the CPU in the socket. Note that the slot on the screw aligns with the lock and unlock legend on the case of the CPU socket.

Caution: Please refer to the CPU installation instruction in Appendix A prior to inserting the CPU as the CPU and socket can be easily damaged.

4.6.2.2 PCI Express* (x16)

The platform has one x16 lane PCI Express* Graphics slot and supports either x1 or x16 modes. The slot is wired "lane reversed" which connects the Intel® 945GME Express Chipset lanes 0 through 15 to lanes 15 through 0 on the slot. The Intel® 945GME Express Chipset will internally un-reverse this wiring since its CFG9 power-on strap is tied low.

Table 12. PCI Express* (x16) Pinout (J6C1) (Sheet 1 of 3)

Pin	Description	Pin	Description
A1	PRSNT1#	B1	+12 V
A2	+12 V	B2	+12 V
A3	+12 V	B3	+12 V
A4	GND	B4	GND
A5	(JTAG) TCK	B5	SMCLK
A6	(JTAG) TDI	B6	SMDAT
A7	(JTAG) TDO	B7	GND
A8	(JTAG) TMS	B8	+3.3 V
A9	+3.3 V	B9	(JTAG) TRST#
A10	+3.3 V	B10	+3.3 VAUX
A11	PERST#	B11	WAKE#
A12	GND	B12	RSVD
A13	REFCLK+	B13	GND
A14	REFCLK-	B14	LANE 0 (T+)
A15	GND	B15	LANE 0 (T-)
A16	LANE 0 (R+)	B16	GND
A17	LANE 0 (R-)	B17	PRSNT2*
A18	GND	B18	GND
A19	RSVD	B19	LANE 1 (T+)
A20	GND	B20	LANE 1 (T-)
A21	LANE 1 (R+)	B21	GND
A22	LANE 1 (R-)	B22	GND
A23	GND	B23	LANE 2 (T+)
A24	GND	B24	LANE 2 (T-)
A25	LANE 2 (R+)	B25	GND
A26	LANE 2 (R-)	B26	GND
A27	GND	B27	LANE 3 (T+)
A28	GND	B28	LANE 3 (T-)
A29	LANE 3 (R+)	B29	GND

Table 12. PCI Express* (x16) Pinout (J6C1) (Sheet 2 of 3)

Pin	Description	Pin	Description
A30	LANE 3 (R-)	B30	RSVD
A31	GND	B31	PRSNT2#
A32	RSVD	B32	GND
A33	RSVD	B33	LANE 4 (T+)
A34	GND	B34	LANE 4 (T-)
A35	LANE 4 (R+)	B35	GND
A36	LANE 4 (R-)	B36	GND
A37	GND	B37	LANE 5 (T+)
A38	GND	B38	LANE 5 (T-)
A39	LANE 5 (R+)	B39	GND
A40	LANE 5 (R-)	B40	GND
A41	GND	B41	LANE 6 (T+)
A42	GND	B42	LANE 6 (T-)
A43	LANE 6 (R+)	B43	GND
A44	LANE 6 (R-)	B44	GND
A45	GND	B45	LANE 7 (T+)
A46	GND	B46	LANE 7 (T-)
A47	LANE 7 (R+)	B47	GND
A48	LANE 7 (R-)	B48	PRSNT#2
A49	GND	B49	GND
A50	RSVD	B50	LANE 8 (T+)
A51	GND	B51	LANE 8 (T-)
A52	LANE 8 (R+)	B52	GND
A53	LANE 8 (R-)	B53	GND
A54	GND	B54	LANE 9 (T+)
A55	GND	B55	LANE 9 (T-)
A56	LANE 9 (R+)	B56	GND
A57	LANE 9 (R-)	B57	GND
A58	GND	B58	LANE 10 (T+)
A59	GND	B59	LANE 10 (T-)
A60	LANE 10 (R+)	B60	GND
A61	LANE 10 (R-)	B61	GND
A62	GND	B62	LANE 11 (T+)
A63	GND	B63	LANE 11 (T-)
A64	LANE 11 (R+)	B64	GND
A65	LANE 11 (R-)	B65	GND
A66	GND	B66	LANE 12 (T+)
A67	GND	B67	LANE 12 (T-)
A68	LANE 12 (R+)	B68	GND
A69	LANE 12 (R-)	B69	GND

Table 12. PCI Express* (x16) Pinout (J6C1) (Sheet 3 of 3)

Pin	Description	Pin	Description
A70	GND	B70	LANE 13 (T+)
A71	GND	B71	LANE 13 (T-)
A72	LANE 13 (R+)	B72	GND
A73	LANE 13 (R-)	B73	GND
A74	GND	B74	LANE 14 (T+)
A75	GND	B75	LANE 14 (T-)
A76	LANE 14 (R+)	B76	GND
A77	LANE 14 (R-)	B77	GND
A78	GND	B78	LANE 15 (T+)
A79	GND	B79	LANE 15 (T-)
A80	LANE 15 (R+)	B80	GND
A81	LANE 15 (R-)	B81	PRST2#
A82	GND	B82	RSVD

4.6.2.3 Media Expansion Card (MEC) Slot

When not being used for PCI Express*, the x16 slots can be used for Serial Digital Video Out (SDVO). SDVO cards provide for a third party vendor secondary graphics add-on such as a digital panel interface.

The SDVO interface will also support a Media Expansion Card (MEC), which provide TV Capture over the PCI Express* x1 port in addition to the standard SDVO card video out capabilities.

Table 13. MEC Slot (J6C1) (Sheet 1 of 3)

Pin Number	A	B
1	N/C	12 V
2	12 V	12 V
3	12 V	Reserved
4	GND	GND
5	N/C	N/C
6	N/C	N/C
7	N/C	GND
8	N/C	3.3 V
9	3.3 V	N/C
10	3.3 V	+3.3VA
11	RESET	WAKE#
Key		
12	GND	Reserved
13	REFCLK+	GND
14	REFCLK-	Lane 0 (T+)
15	GND	Lane 0 (T-)
16	Lane 0 (R+)	GND

Table 13. MEC Slot (J6C1) (Sheet 2 of 3)

Pin Number	A	B
17	Lane 0 (R-)	SDVO_CtrlClk
18	GND	GND
End of x1 Connector		
19	Reserved	N/C
20	GND	N/C
21	N/C	GND
22	N/C	GND
23	GND	N/C
24	GND	N/C
25	N/C	GND
26	N/C	GND
27	GND	N/C
28	GND	N/C
29	N/C	GND
30	N/C	Reserved
31	GND	SDVOB_CtrlData
32	Reserved	GND
End of x4 Connector		
33	Reserved	N/C
34	GND	N/C
35	N/C	GND
36	N/C	GND
37	GND	N/C
38	GND	N/C
39	N/C	GND
40	N/C	GND
41	GND	N/C
42	GND	N/C
43	N/C	GND
44	N/C	GND
45	GND	N/C
46	GND	N/C
47	N/C	GND
48	N/C	MEC_Enable
49	GND	GND
End of x8 Connector		
50	Reserved	SDVOC_CLK+
51	GND	SDVOC_CLK-
52	N/C	GND
53	N/C	GND

Table 13. MEC Slot (J6C1) (Sheet 3 of 3)

Pin Number	A	B
54	GND	SDVOC_Blue+
55	GND	SDVOC_Blue-
56	N/C	GND
57	N/C	GND
58	GND	SDVOC_Green+
59	GND	SDVOC_Green-
60	SDVOC_Int+	GND
61	SDVOC_Int-	GND
62	GND	SDVOC_Red+
63	GND	SDVOC_Red-
64	N/C	GND
65	N/C	GND
66	GND	SDVOB_Clk+
67	GND	SDVOB_Clk-
68	N/C	GND
69	N/C	GND
70	GND	SDVOB_Blue+
71	GND	SDVOB_Blue-
72	SDVO_Stall+	GND
73	SDVO_Stall-	GND
74	GND	SDVOB_Green+
75	GND	SDVOB_Green-
76	SDVOB_Int+	GND
77	SDVOB_Int-	GND
78	GND	SDVOB_Red+
79	GND	SDVOB_Red-
80	SDVO_TVClkIn+	GND
81	SDVO_TVClkIn-	N/C
82	GND	Reserved

4.6.2.4 PCI Express* (x1)

The two PCI Express* x1 connectors allow the use of any industry standard PCI Express* device. The pin configuration of the connectors is given below.

Table 14. PCI Express* (x1) Pinout (J7C1, J8C1) (Sheet 1 of 2)

Pin	Description	Pin	Description
A1	PRSNT1#	B1	+12 V
A2	+12 V	B2	+12 V
A3	+12 V	B3	RSVD
A4	GND	B4	GND

Table 14. PCI Express* (x1) Pinout (J7C1, J8C1) (Sheet 2 of 2)

A5	(JTAG) TCK	B5	SMCLK
A6	(JTAG) TDI	B6	SMDAT
A7	(JTAG) TDO	B7	GND
A8	(JTAG) TMS	B8	+3.3 V
A9	+3.3 V	B9	(JTAG) TRST#
A10	+3.3 V	B10	+3.3 VAUX
A11	PERST#	B11	WAKE#
A12	GND	B12	RSVD
A13	REFCLK+	B13	GND
A14	REFCLK-	B14	LANE 0 (T+)
A15	GND	B15	LANE 0 (T-)
A16	LANE 0 (R+)	B16	GND
A17	LANE 0 (R-)	B17	PRSNT2*
A18	GND	B18	GND

4.6.2.5 IDE Connector

The IDE interface can support up to two devices, a master and a slave. Ensure that the jumpers on the drives are properly selected for the given configuration. Mobile drives with an IDE interface will require an adapter to connect to this port. This adapter is included in the Development Kit.

Table 15. IDE Connector (J7J1)

Pin	Signal	Pin	Signal
1	Reset IDE	2	Ground
3	Host Data 7	4	Host Data 8
5	Host Data 6	6	Host Data 9
7	Host Data 5	8	Host Data 10
9	Host Data 4	10	Host Data 11
11	Host Data 3	12	Host Data 12
13	Host Data 2	14	Host Data 13
15	Host Data 1	16	Host Data 14
17	Host Data 0	18	Host Data 15
19	Ground	20	Key
21	DRQ3	22	Ground
23	I/O Write	24	Ground
25	I/O Read	26	Ground
27	I/O Ch Ready	28	CSEL
29	DACK 3	30	Ground
31	IRQ 14	32	NC
33	Address 1	34	DATA Detect
35	Address 0	36	Address 2
37	Chip Select 0	38	Chip Select 1
39	Activity	40	Ground

4.6.2.6 SATA Pinout

Table 16. SATA Port 0 Data Connector Pinout (J7H1)

Pin	Signal
1	GND
2	TXP
3	TXN
4	GND
5	RXN
6	RXP
7	GND

Table 17. SATA Port 0 Power Connector Pinout (J6H3)

Pin	Signal
1, 2	+3.3 V
3, 4	+5 V
5	+12 V
6, 7, 8, 9, 10	GND

Table 18. SATA Port 2 Mobile Drive Connector Pinout (J8J2)

Pin	Signal
2	TX
3	TX#
5	RX#
6	RX
8, 9, 10	+3.3 V
14, 15, 16	+5 V
20, 21, 22	+12 V
1, 4, 7, 11	GND
12, 13, 17, 19	GND

4.6.2.7 Fan Connectors

Table 19. Fan Connectors (J3F1 and J3C1)

Pin	Signal
1	+5V
2	GND

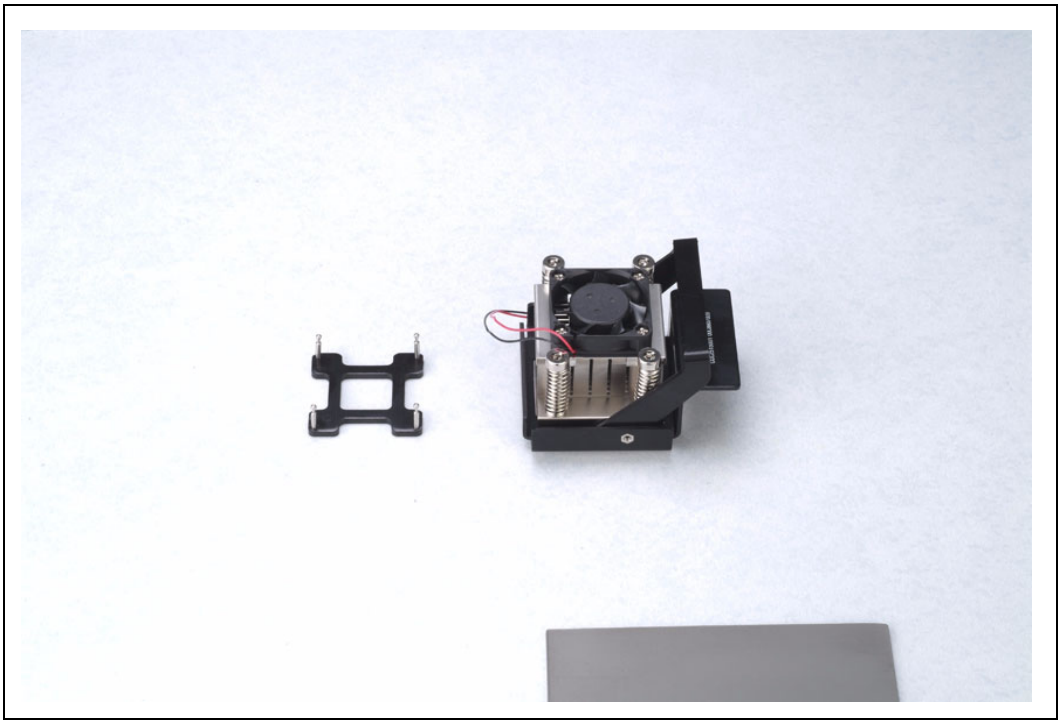
Appendix A Heat Sink Installation Instructions

It is necessary for the Intel® Core™ 2 Duo processor to have a thermal solution attached to it in order to keep it within its operating temperature.

A heat sink is included in the kit. To install the heat sink:

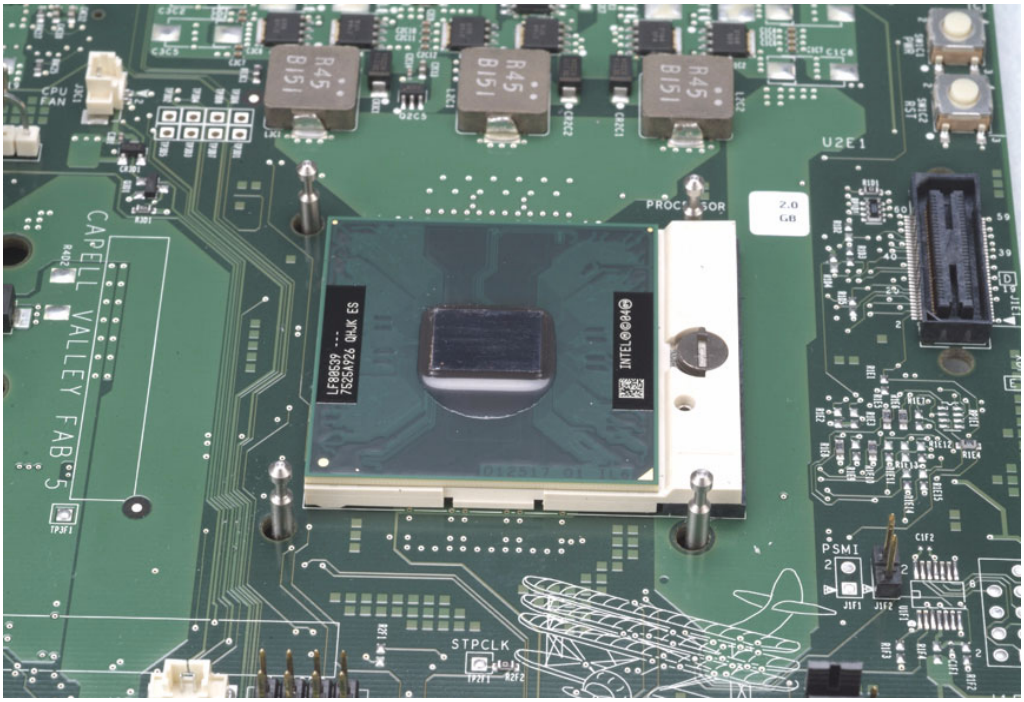
1. Remove the heatsink from its package and separate the fan heatsink portion from the heatsink backplate.

Figure 6. Heatsink and Backplate



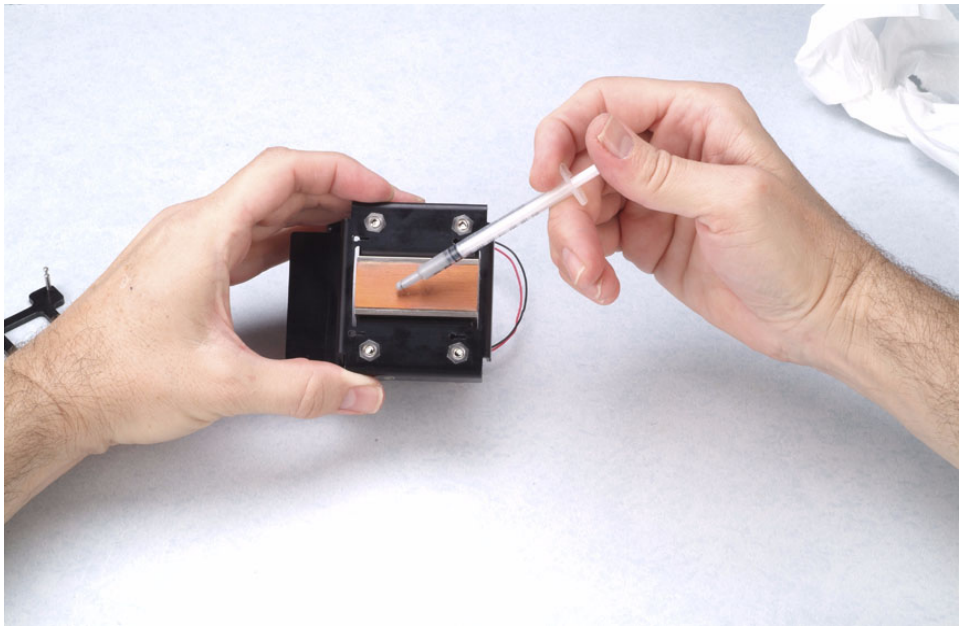
2. Examine the base of the heatsink, where contact with the processor die is made. This surface should be clean of all materials and greases. Wipe the bottom surface clean with isopropyl alcohol.
3. Place the backplate on the underside of the board so that the pins protrude through the holes in the system board around the processor.

Figure 7. Backplate Pins



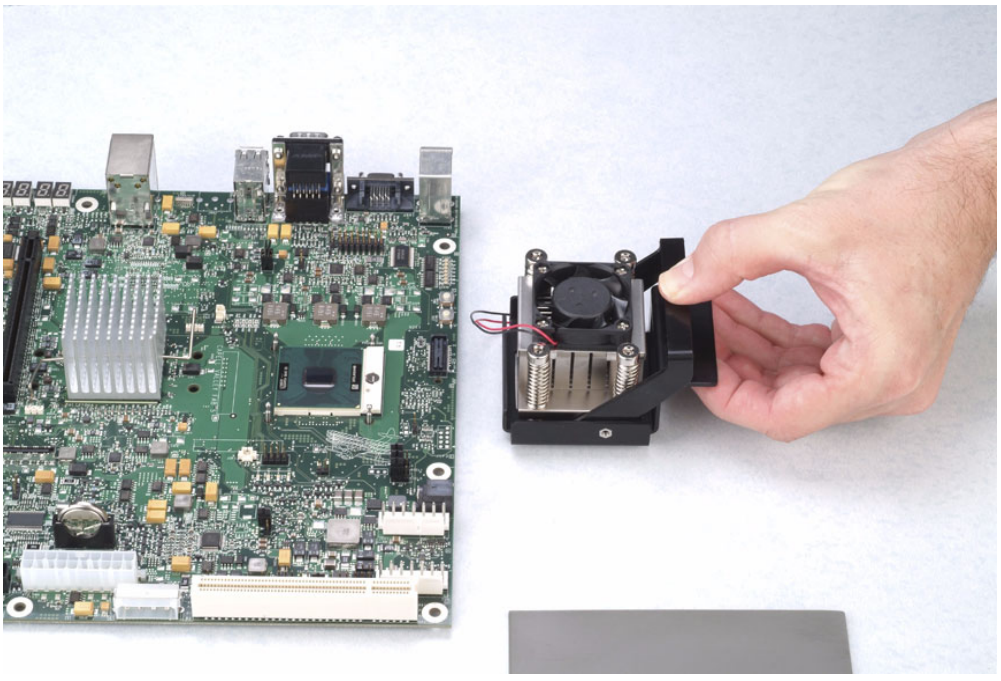
4. Clean the die of the processor with isopropyl alcohol before the heatsink is attached to the processor. This ensures that the surface of the die is clean.
5. Remove the tube of thermal grease from the package and use it to coat the bottom of the heatsink thermal plate with the thermal grease.

Figure 8. Applying the Thermal Grease



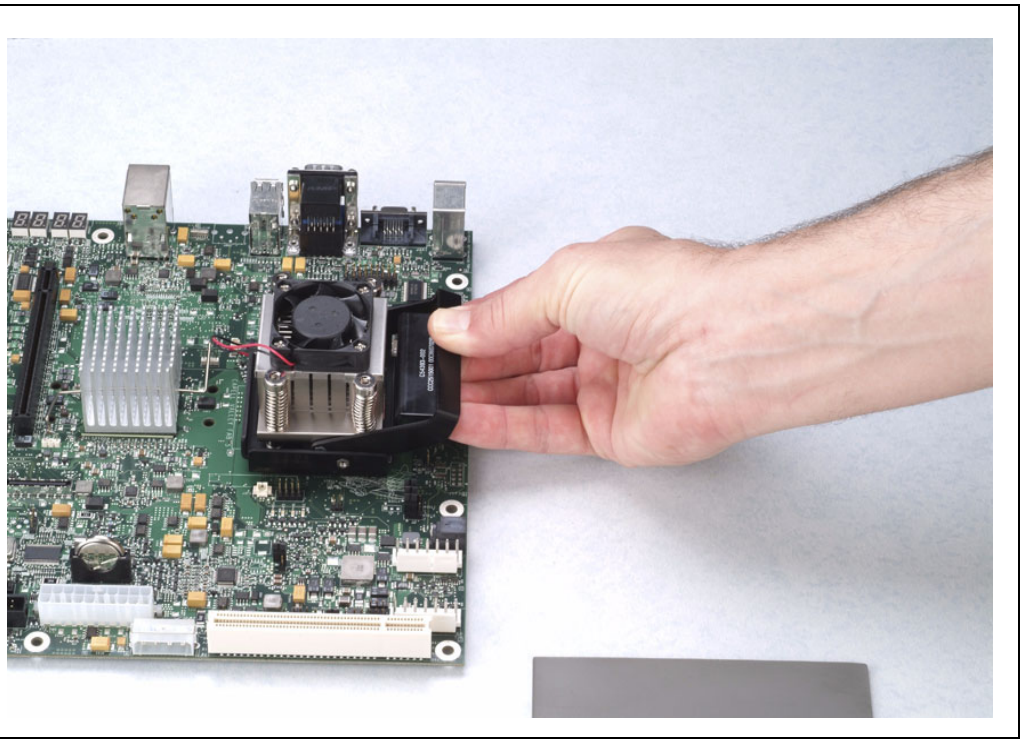
6. Pick up the heatsink and squeeze the activation arm until it comes in contact with the base plate that is attached to the heatsink base. This will cause the springs on the heatsink attachment mechanism to compress.

Figure 9. Squeezing Activation Arm



7. While keeping the activation arm compressed, place the heatsink over the pins of the heatsink backplate. Lower the heatsink until the lugs have inserted into the base of the heatsink. Slide the heatsink over the lugs on the backplate pins so that the base is directly over the processor die and the pins on the backplate have traveled the entire length of the channel in the heatsink base. Slowly let go of the activation arm until the base of the heatsink makes contact with the processor die. The heatsink base should be flat on top of the processor die.

Figure 10. Installing the Heatsink



8. Plug the fan connector for the heatsink onto the CPU fan header (J3C1) on the motherboard.

Figure 11. Plugging in the Fan

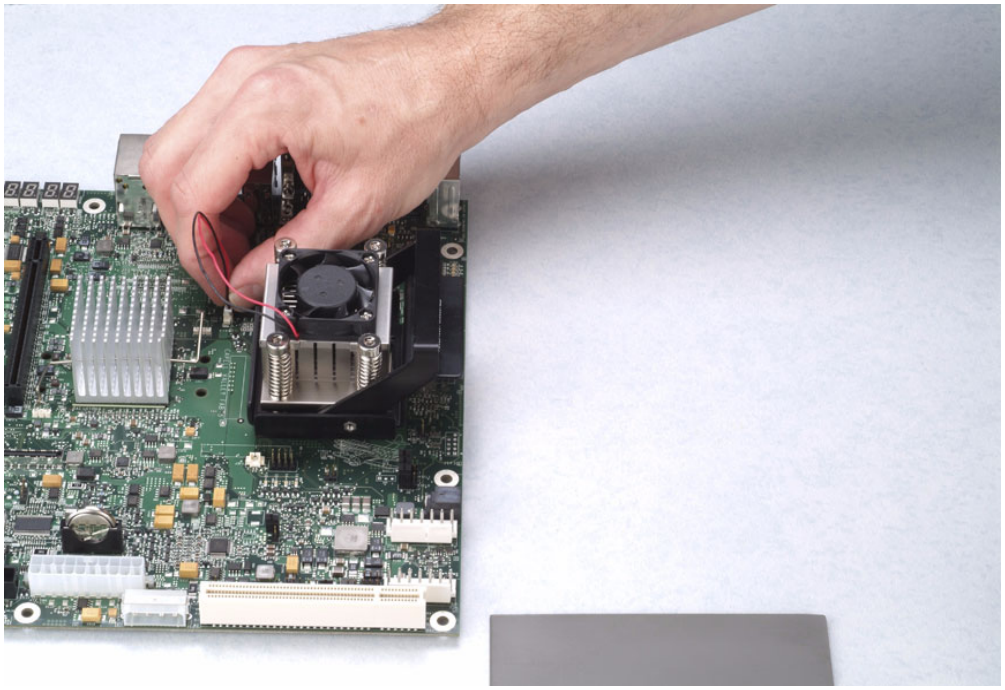


Figure 12. Completed Assembly