



LXD386 — Evaluation Board for Quad T1/E1 Applications

Developer Manual

January 2001

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LXD386 — Evaluation Board for Quad T1/E1 Applications User Guide.

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1.0 General Description

The LXD386 evaluation board is a versatile tool for engineers designing T1/E1 short haul applications using the LXT386.

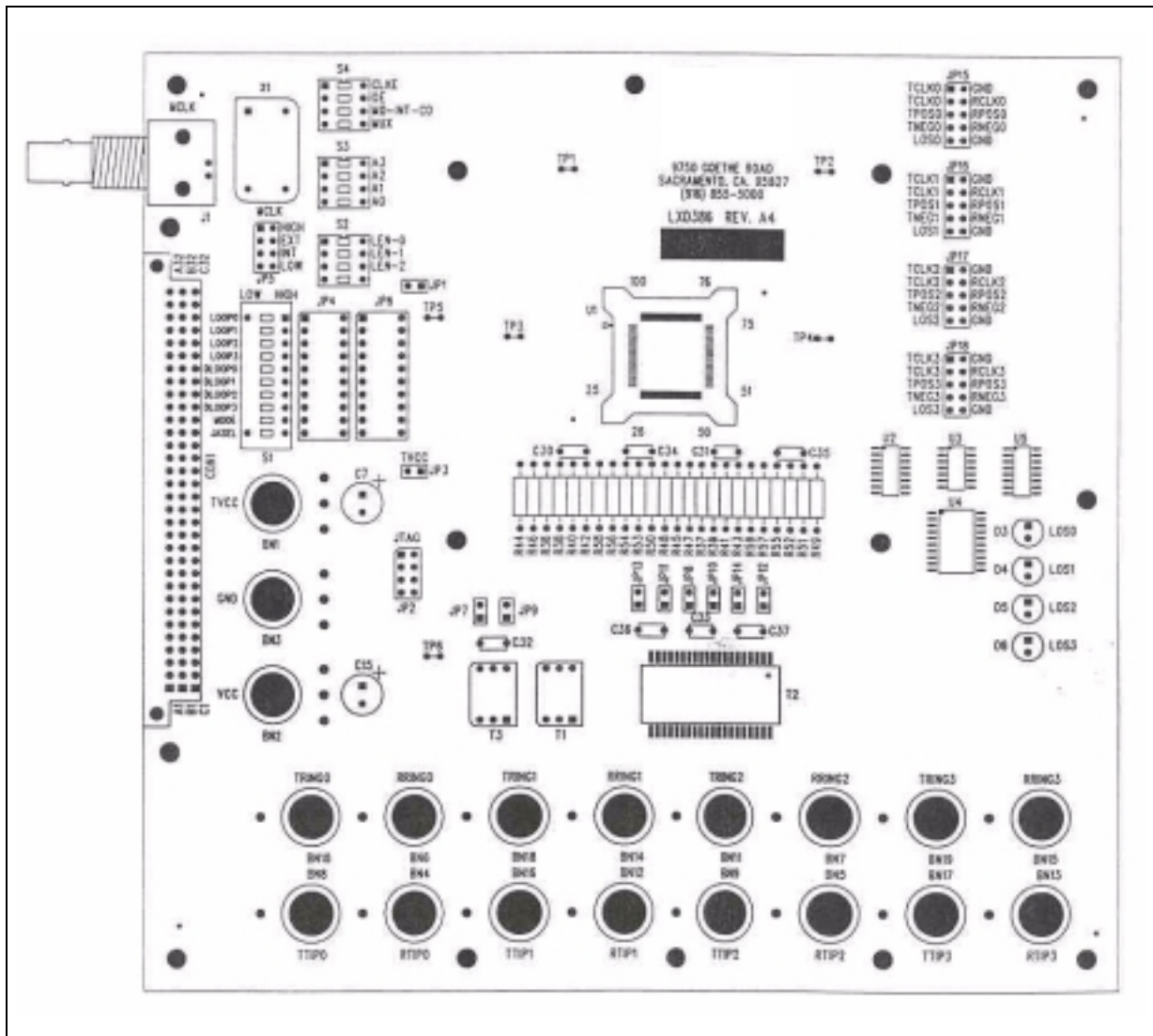
The evaluation board operates in one of two modes: Software (Host) mode or Hardware mode. In Software mode, the device is controlled with the PC based configuration and monitoring software through an i8051 microcontroller interface. In Hardware mode, the device and channel controls are set using shorting blocks and DIP switches located on the LXD386 evaluation board.

The evaluation board provides banana jacks for each channel's line interface to allow connection of a T1/E1 pattern generator/analyzer. A connector is also provided for each channel's framer or back-end ASIC interface.

1.1 Features

- Software and Hardware controllable
- ZIF LQFP socket for easy swapping of LXT386
- Banana jacks for power and line interfaces
- 10-pin connectors for framer/ASIC interface
- 8-pin connector for IEEE 1149.1 compliant JTAG boundary scan port
- LED indicators for LOS alarm
- On-board 2.048/1.544 MHz reference clock oscillator
- Switches and shorting blocks for Hardware mode operation
- Compatible with Intel external i8051 microcontroller board
- PC-based software for ease of use
- Socketed transformer and termination components for easy experimentation
- Built-in overvoltage protection for line interface and power supply

Figure 1. LXD386 Evaluation Board



2.0 Overview

Caution: CMOS devices are static (ESD) sensitive. Take all industry standard precautions when handling the evaluation board, LXT386 chip, and other sensitive electronic components.

Before proceeding with any evaluation board operations, review the specifications for the LXT386 transceiver.

2.1 LXD386 Packing List

The evaluation board kit contains the following components:

- LXD386 evaluation board with the LXT386 installed.
- 2.048 MHz oscillator installed, additional 1.544 MHz oscillator supplied.
- i8051 microcontroller interface board and PC serial port cable.
- PC compatible diskettes containing software for using the evaluation board in Software mode.
- Shorting block kit for selecting Hardware mode.
- LXD386 user guide.
- LXT386 data sheet.

2.2 Equipment Requirements

The evaluation board kit includes all the circuit components needed for a successful evaluation. However, the following lab equipment is required:

- Power Supply +3.3V DC (+5VDC for TVCC optional)
- Telecom cable or cable simulator (optional).
- T1/E1 pattern generator/analyzer.
- 1.544/2.048 MHz clock source (optional).
- For Software mode: an IBM compatible PC with minimum 386 40 MHz processor, available serial port, mouse, VGA monitor, DOS 5.0+, and Microsoft Windows[®] 3.1 or later version, Windows 9x is recommended.

2.3 Control Modes

The LXT386 has two basic operating modes: Hardware mode or Software (Host) mode. In Hardware mode, operation of the LXT386 is established by hard-wiring the pins. In Software mode, operation of the LXT386 is controlled by an external microprocessor that communicates with the LXT386's internal registers via either a serial or parallel interface.

The LXD386 evaluation board supports both hardware and software modes.



2.4 Factory Settings

When shipped from the factory, the LXD386 evaluation board's switches and jumpers are set for software mode and parallel microprocessor interface.

3.0 Hardware Mode Set-Up and Operation

3.1 Power Connections

The evaluation board has two power planes (VCC and TVCC) each of which is tied to a separate red colored banana jack.

1. Connect the +3.3 VDC power supply to the VCC jack.
2. Connect either a +3.3 VDC or +5.0 VDC power supply to the TVCC jack.
3. Connect the power supply ground lead(s) to the black (GND) banana jack.

Jumper JP1 is provided to allow LXT386 current consumption measurements and must be installed for normal board operation. Jumper JP3 allows measurement of the current in the TVCC power supply only. It must also be installed for normal operation.

3.2 Hardware Mode Selection

To enable the Hardware mode of operation:

1. Set the MODE switch in switch block S1 to the LOW position.
2. Insert the two shorting blocks, provided with the evaluation board kit, into 20-pin sockets JP4 and JP6.

3.3 Loopback Mode Selection

The LXT386 LOOP/DLOOP signals are set by switches in switch block S1. Depending on the LOOPn/DLOOPn combination selected for a particular channel, a different operation or loopback mode is selected. Please refer to [Table 1](#).

Table 1. LOOP/DLOOP Switch Settings

| LOOPn | DLOOPn | Channel #n Operation |
|---------------------------|--------|------------------------|
| Open | x | Normal Mode |
| LOW | x | Remote Loopback |
| HIGH | LOW | Analog Local Loopback |
| HIGH | HIGH | Digital Local Loopback |
| 1. "x" means "don't care" | | |

3.4 Clock Edge Selection

The phase relation between RCLK and RPOS/RNEG is set by the CLKE switch in switch block S4. Please refer to the "CLKE" signal pin in the LXT386 data sheet for details.

3.5 Output Enable Selection

The OE switch in switch block S4 controls the operation of the LXT386 output drivers. For normal operation (driver outputs enabled), set the OE switch to the ON position. Setting the OE switch to OFF forces the output drivers to the high impedance state.

3.6 Code Selection

In Hardware mode, the MO-INT-CO switch in switch block S4 selects the line encode/decode. To select AMI encode/decode set to the ON position. To select B8ZS/HDB3 encode/decode set to the OFF position.

3.7 Monitoring Address Selection

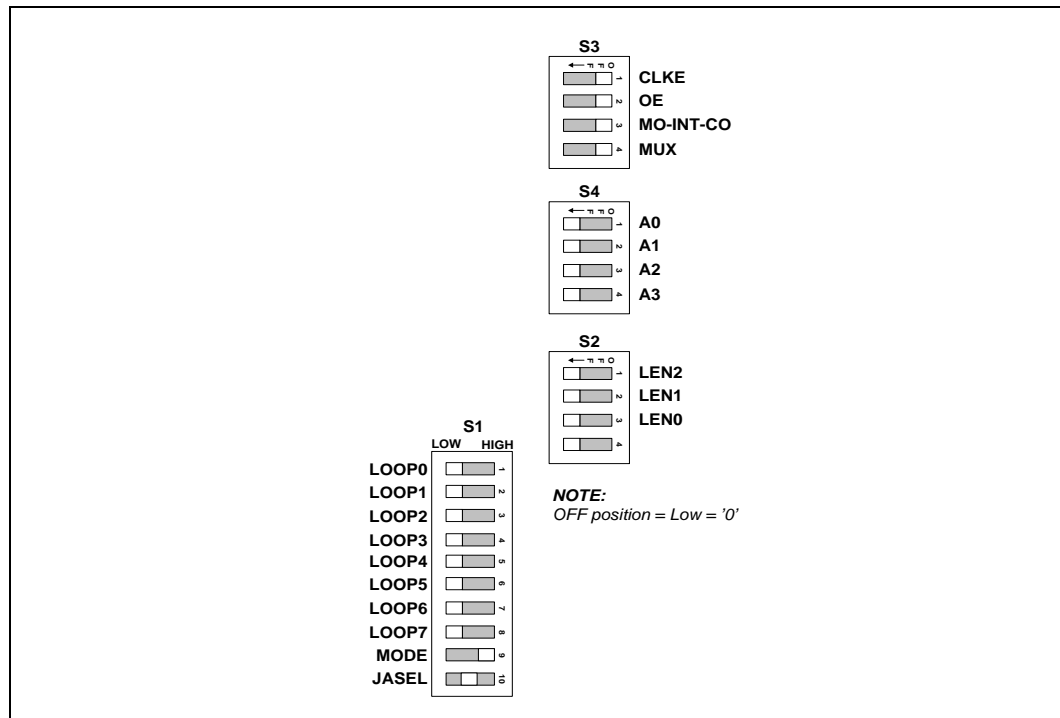
Switch block S3 sets the Protected Monitoring Addresses A0 through A3. The factory default setting is 0000 (no monitoring). See the LXT386 data sheet for details.

3.8 Jitter Attenuator Selection

In Hardware mode, the JASEL switch in switch block S1 selects the position of the Jitter Attenuator in the data path:

- Transmit path = LOW
- Receive path = HIGH
- JA disabled = center

Figure 2. Default Switch Settings



3.9 Line Buildout Selection

Switch block S2 is used to select the transmit pulse shaping for T1 mode operation, as well as T1/E1 mode selection. The factory default is 000 (E1 mode). Refer to the LXT386 data sheet for T1 pulse shape details.

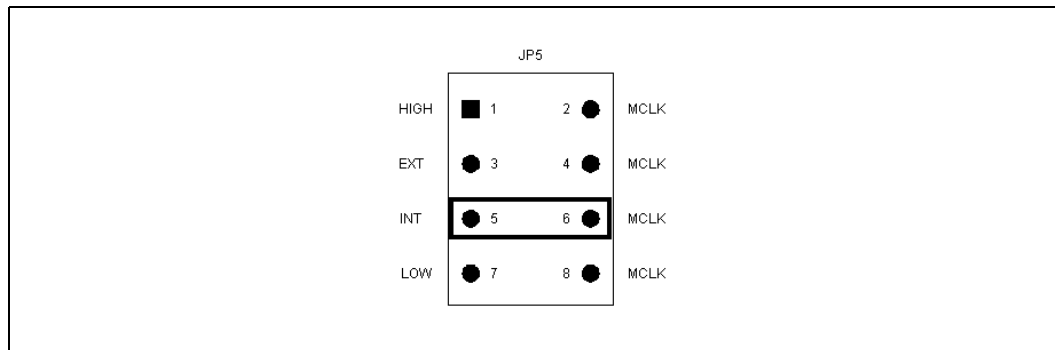
3.10 Master Clock Setup

The on-board 2.048 MHz oscillator can be used for MCLK source. An additional 1.544 MHz oscillator is included for use in T1 operation mode. A BNC connector (J1) is provided to allow use of an external MCLK source. J1 is internally terminated into 50Ω. Jumper block JP5 is used to configure MCLK. Table 2 describes the options available with JP5. The factory setup for JP5 sets internal oscillator timing as illustrated in Figure 3.

Table 2. JP5 Jumper Settings

| JP5 Setting | Operation |
|-------------|----------------------------------|
| HIGH | Data recovery mode |
| EXT | External MCLK source at BNC (J1) |
| INT | Internal oscillator |
| LOW | Receiver power-down |

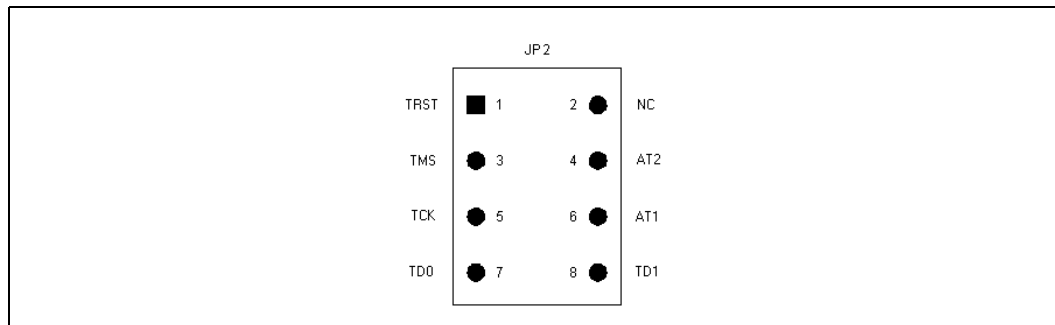
Figure 3. Jumper Block JP5



3.11 JTAG Boundary Scan Port

The eight pin connector JP2 shown in Figure 4 provides access to the IEEE 1149.1 compliant JTAG boundary scan port for board testing purposes.

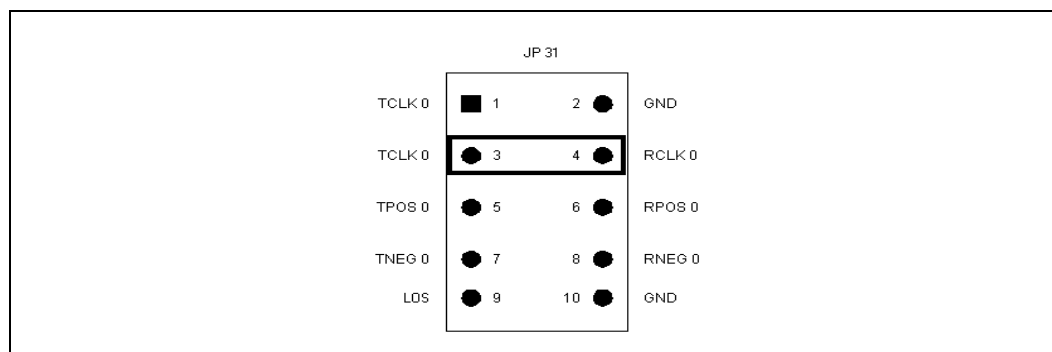
Figure 4. Jumper Block JP2



3.12 Framer/ASIC Connection

Ten pin connectors provide access to the digital signals necessary for interfacing with the back-end Framer/Mapper or ASIC. Figure 5 represents one of the four connectors with the factory jumper connecting RCLK to TCLK.

Figure 5. Jumper Block JP 31



3.13 LED Indicators

Loss of Signal (LOS) status for each channel is indicated by four LEDs, labeled D3 through D6. If the board is being used in the Software mode, the state of these LEDs will also be displayed on the registers display screen.

3.14 Line Interface

Access to the line interface is provided through the green and white banana jacks. The TIP signal is routed to the white jacks for both transmit and receive directions. The RING signal is routed to the green jacks for both directions.

An octal transformer is used for channels 1 to 3 (one transformer port is unused). Transformers in channel 0 and line resistors /capacitors for channels 0 to 3 are socketed for easy swapping. Jumpers JP7 to JP14 can be used to bypass the transmit series resistors for T1 applications with TVCC=3.3V. See the LXT386 Data Sheet for details on transmit interface options.

3.15 Board Protection

The LXD386 evaluation board is equipped with both power supply and line surge protection. Two Transient Voltage Suppressors (TVS) are included for power supply protection (5V/3.3V). For the T1/E1 line interface, the transmitters are protected with Schottky diodes and the receivers are protected by series 1KΩ input resistors. This protection is sufficient for G.703 Annex B compliance.

4.0 Software Mode Set-Up and Operation

4.1 i8051 Microcontroller Board

An i8051 microcontroller interface board is provided with the evaluation board kit. Connect the i8051 microcontroller board to the evaluation board at the 96 pin header labeled CON1. Connect the microcontroller board to an available serial (COM) port on your PC using the cable provided in the evaluation board kit.

Instead of the i8051, a user supplied microcontroller board may also be used to control the LXT386. Evaluation board connector CON1 provides access to all the relevant LXT386 microprocessor interface signals.

4.2 Evaluation Board Set-up

The evaluation board contains switches and jumpers to select various operating parameters. All other parameters are controlled through the evaluation board software. When using the i8051 microcontroller provided with the kit, set the evaluation board switches and jumpers as follows:

1. Select software mode by removing the shorting blocks from sockets JP4 and JP6.
2. Set the MODE switch (in switch block S1) to select serial or parallel mode:
 - HIGH for parallel mode (factory default)
 - Center position for serial mode
3. Set the JASEL switch (in switch block S1) to the center position.
4. Set MO-INT-CO switch (in switch block S3) to HIGH (Intel microprocessor).
5. Set MUX switch (in switch block S3) to HIGH (Multiplexed microprocessor address/data bus).
6. Set CLKE switch (in switch block S3). Refer to “CLKE” signal pin in LXT386 data sheet for details.
7. Set OE switch (in switch block S3) as described in “Output Enable Selection” on page 10.
8. Set the jumper on JP5 as described in “Master Clock Setup” on page 11.

4.3 Test Equipment Connections

The evaluation board contains connectors to interface an external pattern generator and other test equipment. See [page 9](#) for details.

4.4 Power Connections

Connect power supply as described in “Power Connections” on [page 9](#).

4.5 Evaluation Board Software

When operating the evaluation board in the software mode, the software provided with the kit will be used to configure the LXT386 and to monitor its operation. This software provides a point-and-click, user friendly interface with on-line help screens. Refer to the data sheet for detailed information about the LXT386 transceiver.

4.6 Software Installation and Start-Up

The minimum PC system requirements are:

- IBM compatible PC
- 386/40 MHz CPU (Pentium class recommended)
- Available serial port
- Mouse
- VGA monitor
- DOS version 5.0 or higher and Microsoft Windows 3.1 (Windows 9x recommended)

Begin the installation procedure by running the Setup.exe file on the installation diskette #1. Follow the on-screen prompts to complete the software installation.

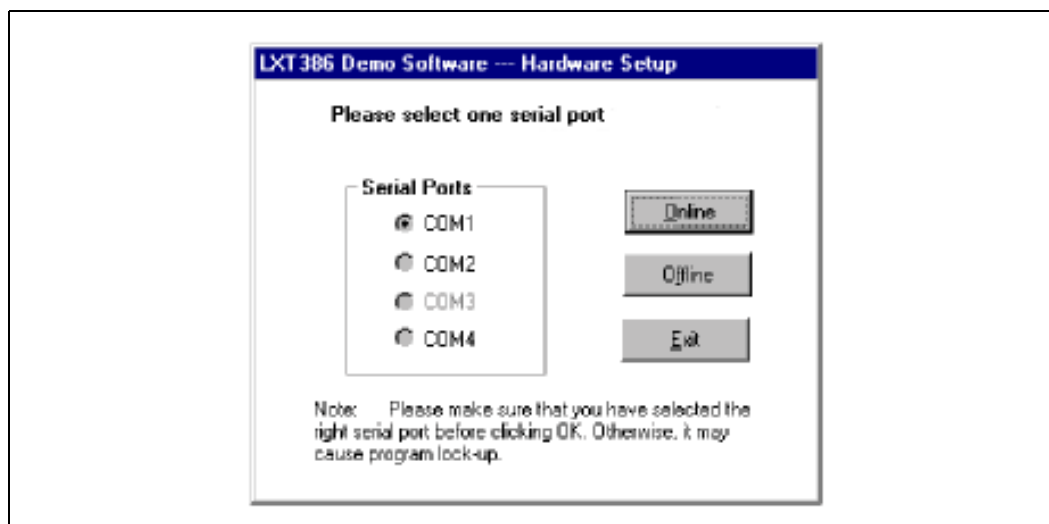
4.7 Hardware Set-up Screen

Whenever the LXT386 software is run, the Hardware Set-up screen will appear first on the monitor (see [Figure 6](#)). This screen is used to select the PC serial port to be used. Select an available serial port and click the OK button.

4.8 Quitting the Program

The program can be terminated at any time by clicking the “Exit” control button, located at the right side of the screen.

Figure 6. Hardware Set-up Screen



4.9 Configuration Screen

The configuration screen shown in [Figure 7](#) is the next screen to appear on the monitor. It is the primary control interface with the evaluation board. A graphical representation of each channel is shown in a tabbed display box, along with the control buttons described in the following paragraphs.

4.9.1 Communications Modes

The option buttons located in the communications modes box are used to set the microprocessor interface mode to parallel interface or serial interface.

Note: The selected communication mode must match the evaluation board MODE switch setting (see [“Evaluation Board Set-up”](#) on page 14). The factory default setting is parallel mode.

4.9.2 Registers

Clicking the Registers control button will select the Registers screen, enabling read/write access to all the LXT386 registers. See [“Registers”](#) on page 16.

4.9.3 Setting Individual Transceiver Operating Modes

Select the transceiver channel you wish to configure by clicking on the corresponding tab symbol. Once a channel has been selected, set the operating mode by clicking on one of the three loopback modes.

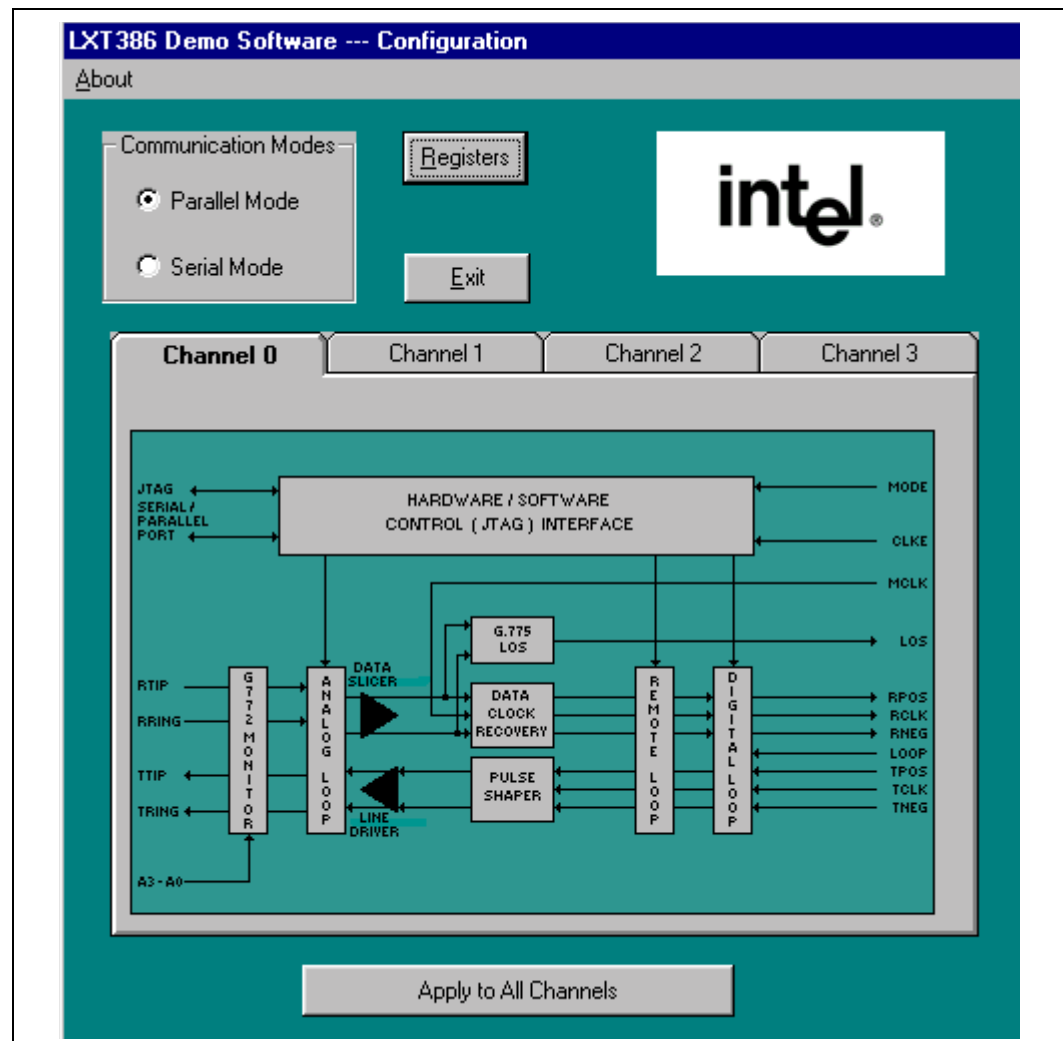
4.9.4 Apply to all Channels

Clicking the “Apply to All Channels” control button will configure the other three channels to the settings displayed for the currently selected channel.

4.9.5 Exit

The exit control button can be used at any time to close the software.

Figure 7. Configuration Screen



4.10 Registers Screen

4.10.1 Setting Registers

The Registers screen (see in [Figure 8](#)) allows direct control of all the LXT386 registers. Each register is labeled by its functional name and hex address. Right click on a register name for on-line help.

4.10.2 Status Indicators

Display boxes within the Registers screen show the state settings for individual bit positions of each register. Each of the 4 least significant bits of these registers control the corresponding transceiver channel, except where otherwise noted in the LXT386 specifications. The check boxes beside the “Mode” column denote enabling of read/write step modes.

4.10.3 Control Buttons

Clicking on the “Read All” button will initiate a global read of all LXT386 registers. Clicking on the “Read Step” and “Write Step” buttons performs the indicated action only on registers that have the enable box checked. The “Back” button is used to return to the configuration screen, and the “Exit” control button can be used at any time to close the software.

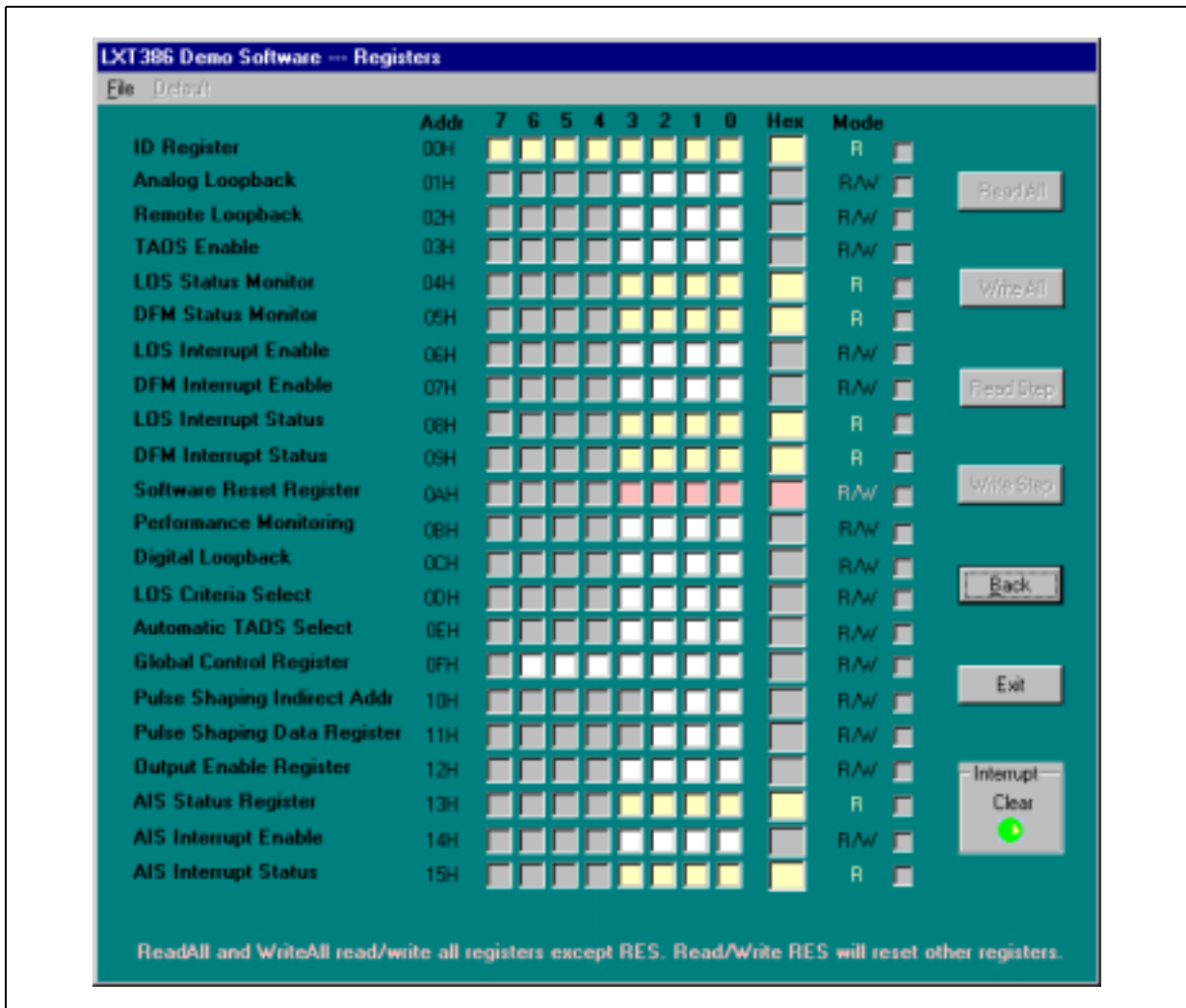
4.10.4 Interrupts

The Interrupt indicator is located in the lower right corner. This indicator will turn red whenever there are pending interrupts in the LXT386. Interrupts are cleared by reading the corresponding Status Monitor register. When all interrupts are cleared, the Interrupt indicator will turn Green. See [Figure 8](#).

4.10.5 Reset

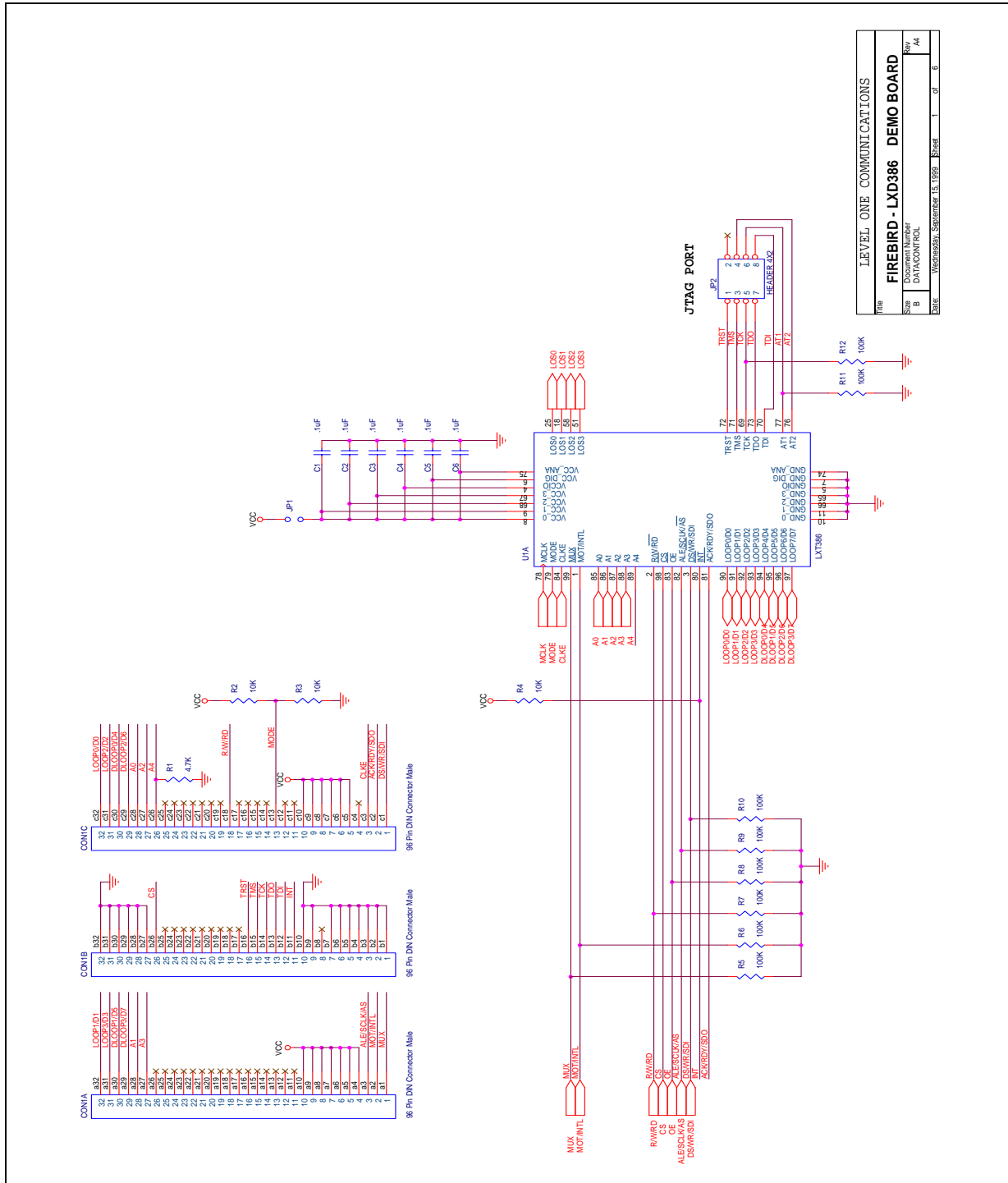
While operating the evaluation board in Software mode, reset is accomplished by using the write step function to write to the software reset register address 0Ah.

Figure 8. Registers Screen



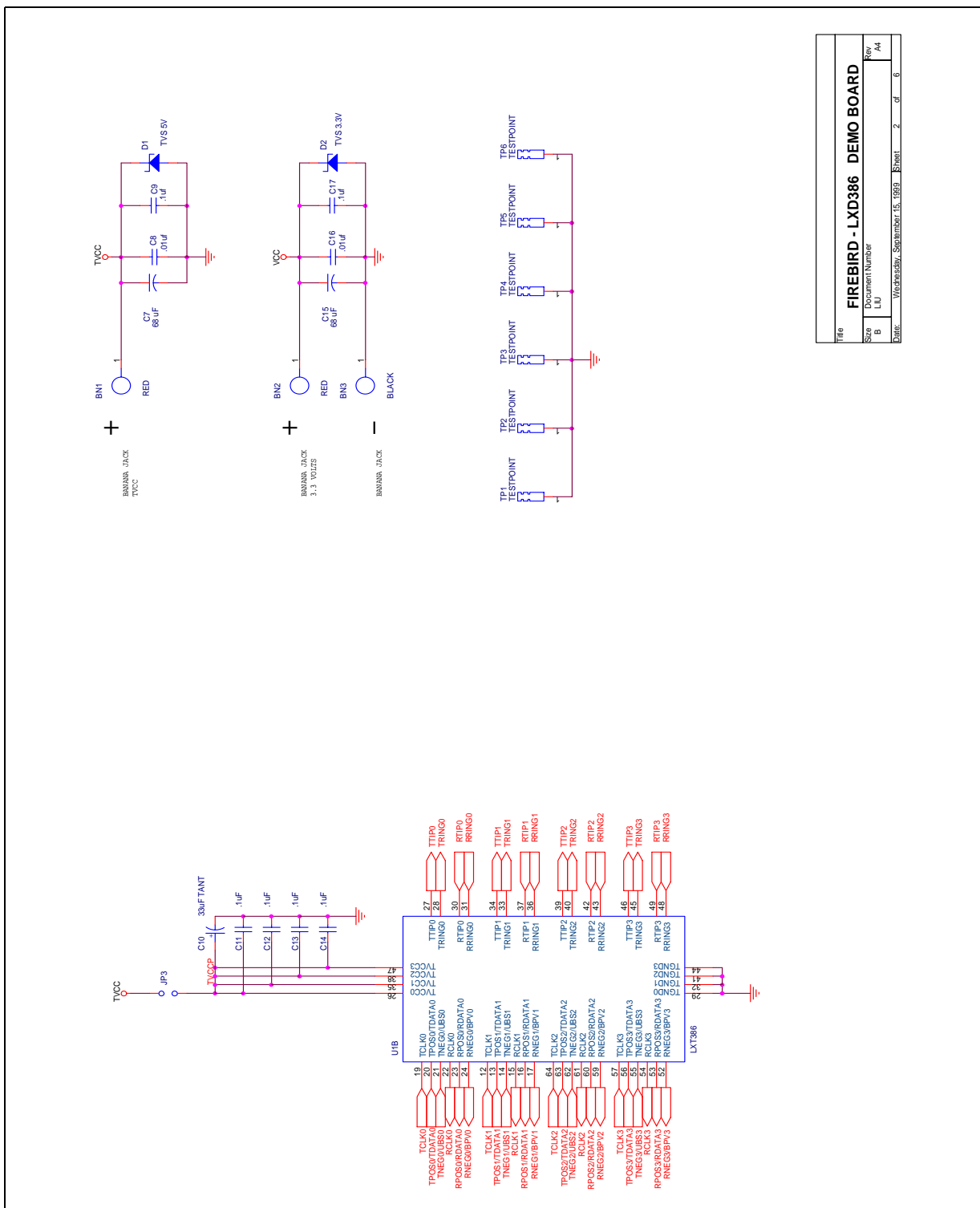
5.0 Evaluation Board Schematics

Figure 9. Evaluation Board Schematic — Data/Control



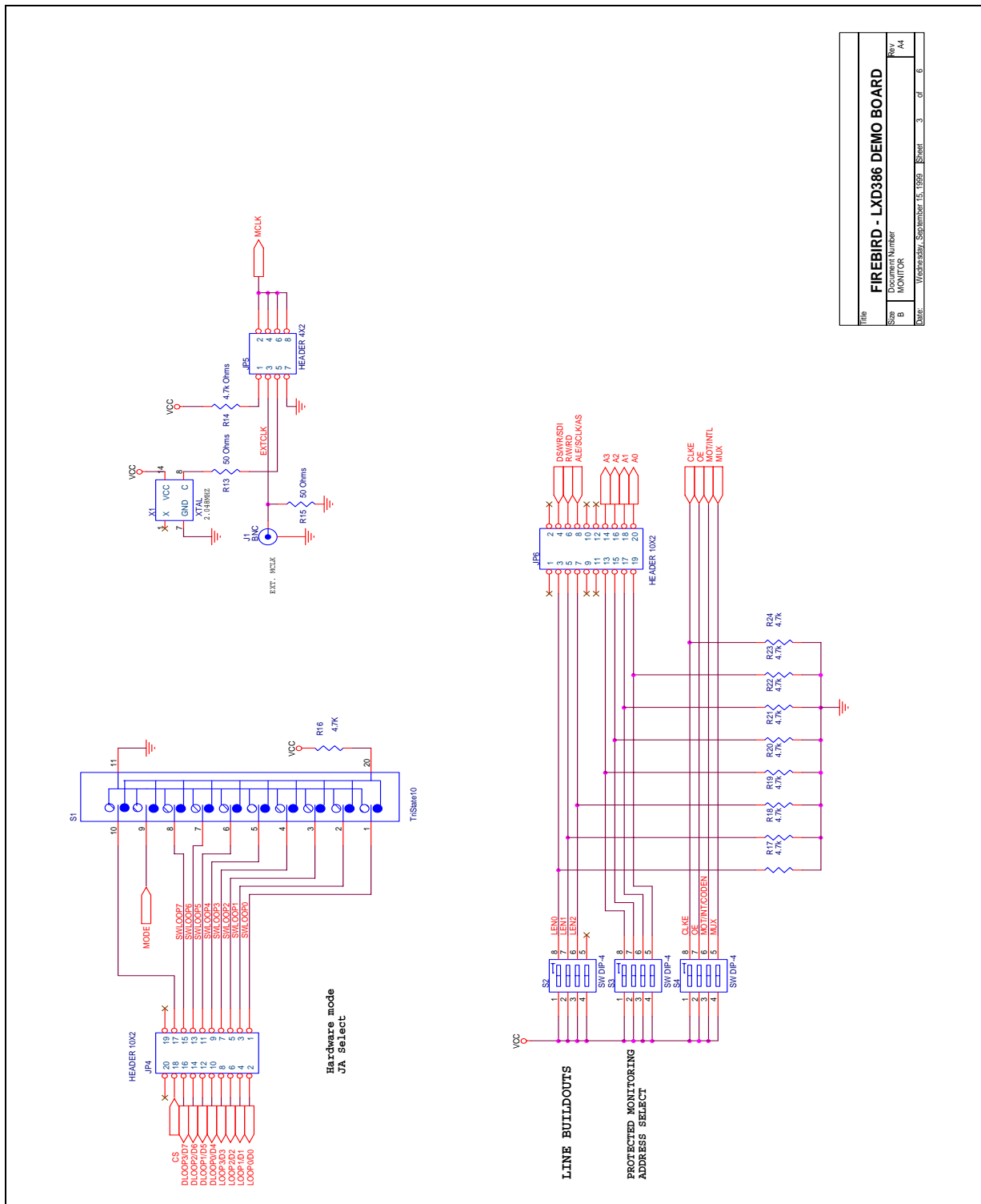
| | | | |
|--------------------------|-------------------------------|-------|--------|
| LEVEL ONE COMMUNICATIONS | | | |
| File | FIREBIRD - LXD386 DEMO BOARD | | |
| Size | Document Number | Rev | AM |
| B | DATA CONTROL | | |
| Date | Wednesday, September 15, 1999 | Sheet | 1 of 6 |

Figure 10. Evaluation Board Schematic — Line Interface Unit



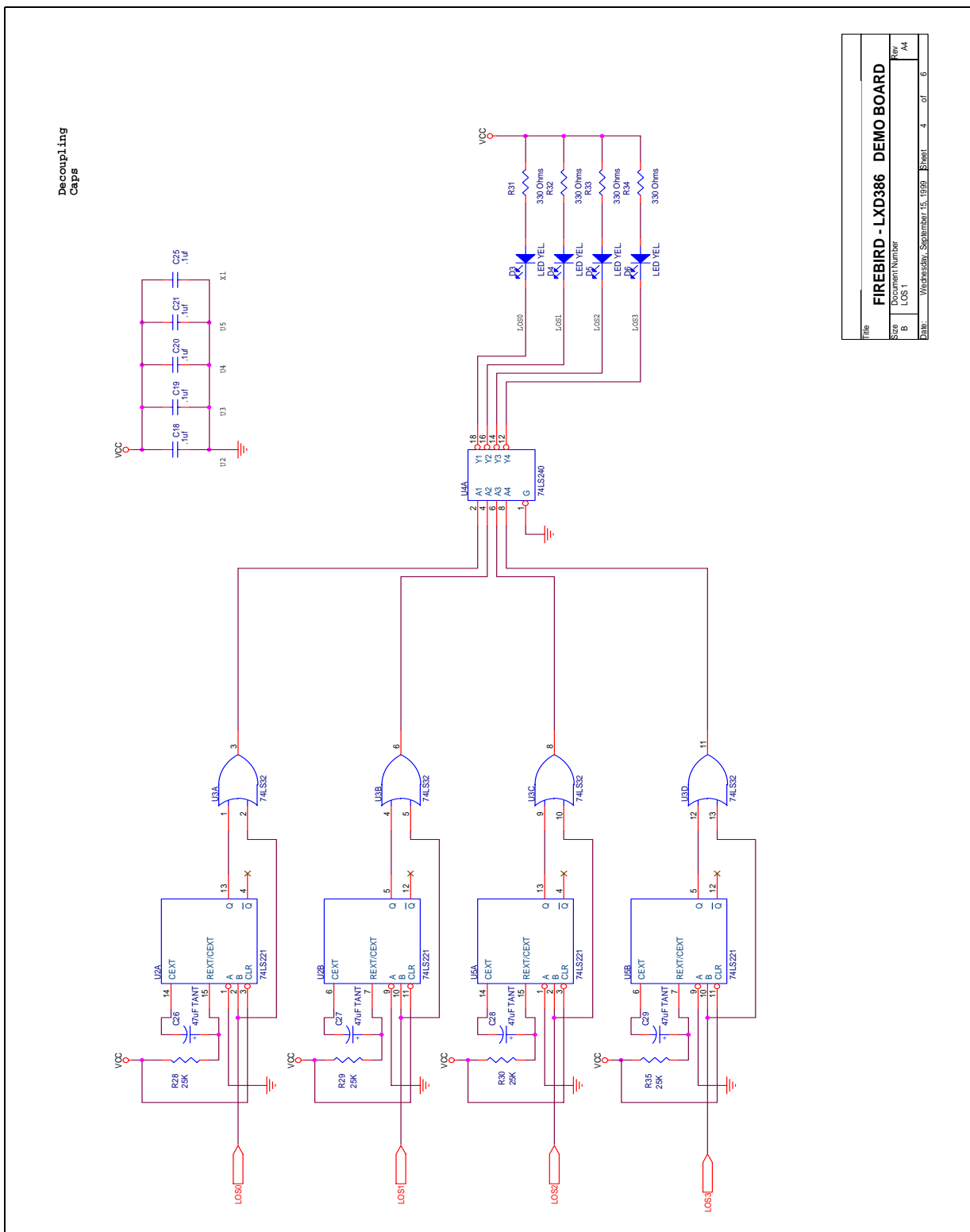
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| Size | Document Number | Rev | A4 |
| B | LIU | | |
| Date: | Wednesday, September 15, 1999 | Sheet | 2 of 6 |

Figure 11. Evaluation Board Schematic — Monitoring



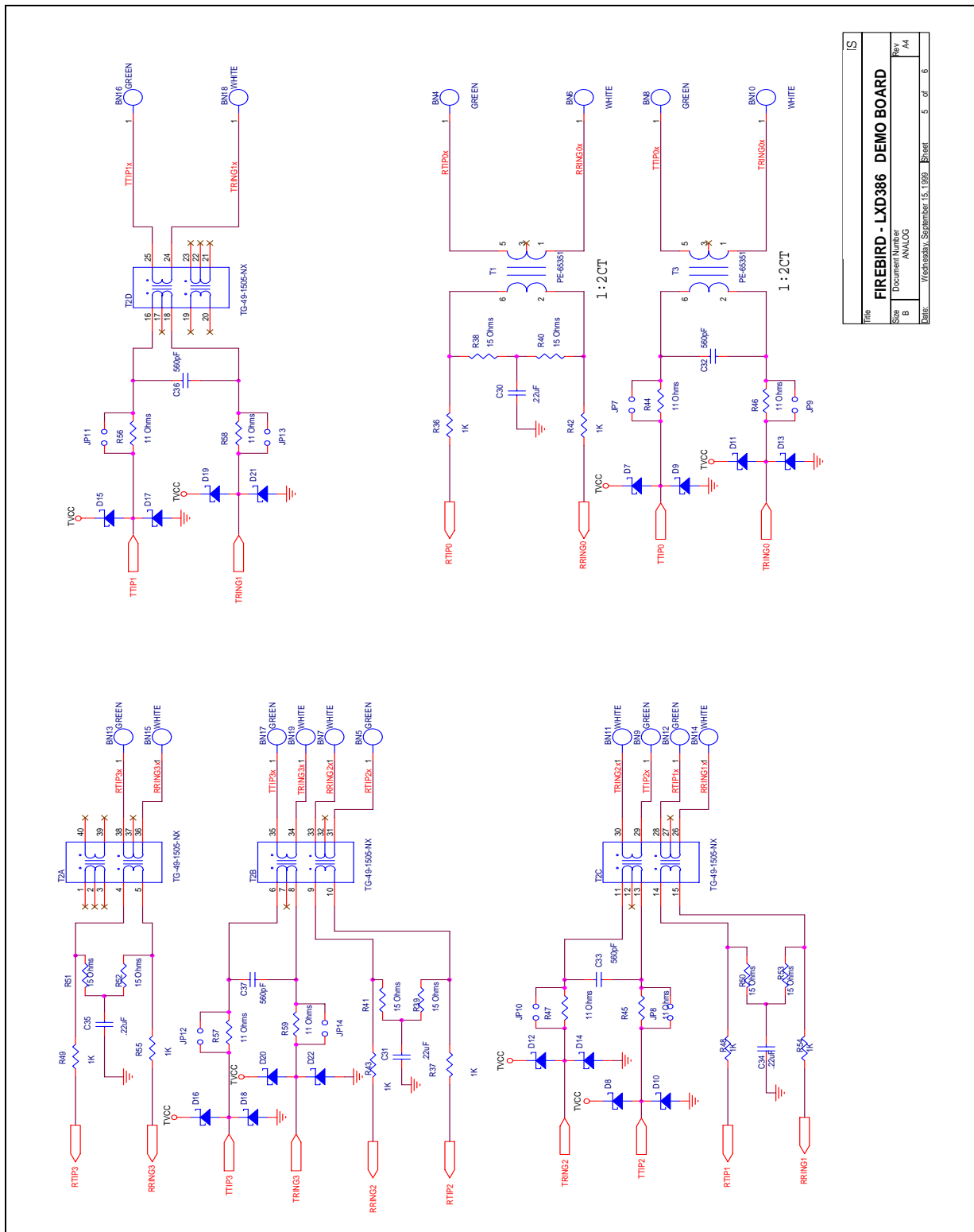
| | |
|------------------|--|
| Title | FIREBIRD - LXD386 DEMO BOARD |
| Docuement Number | Rev. 1/94 |
| Sub | MONITOR |
| Date | Wednesday, September 15, 1993 Sheet 3 of 6 |

Figure 12. Evaluation Board Schematic — LOS Detector



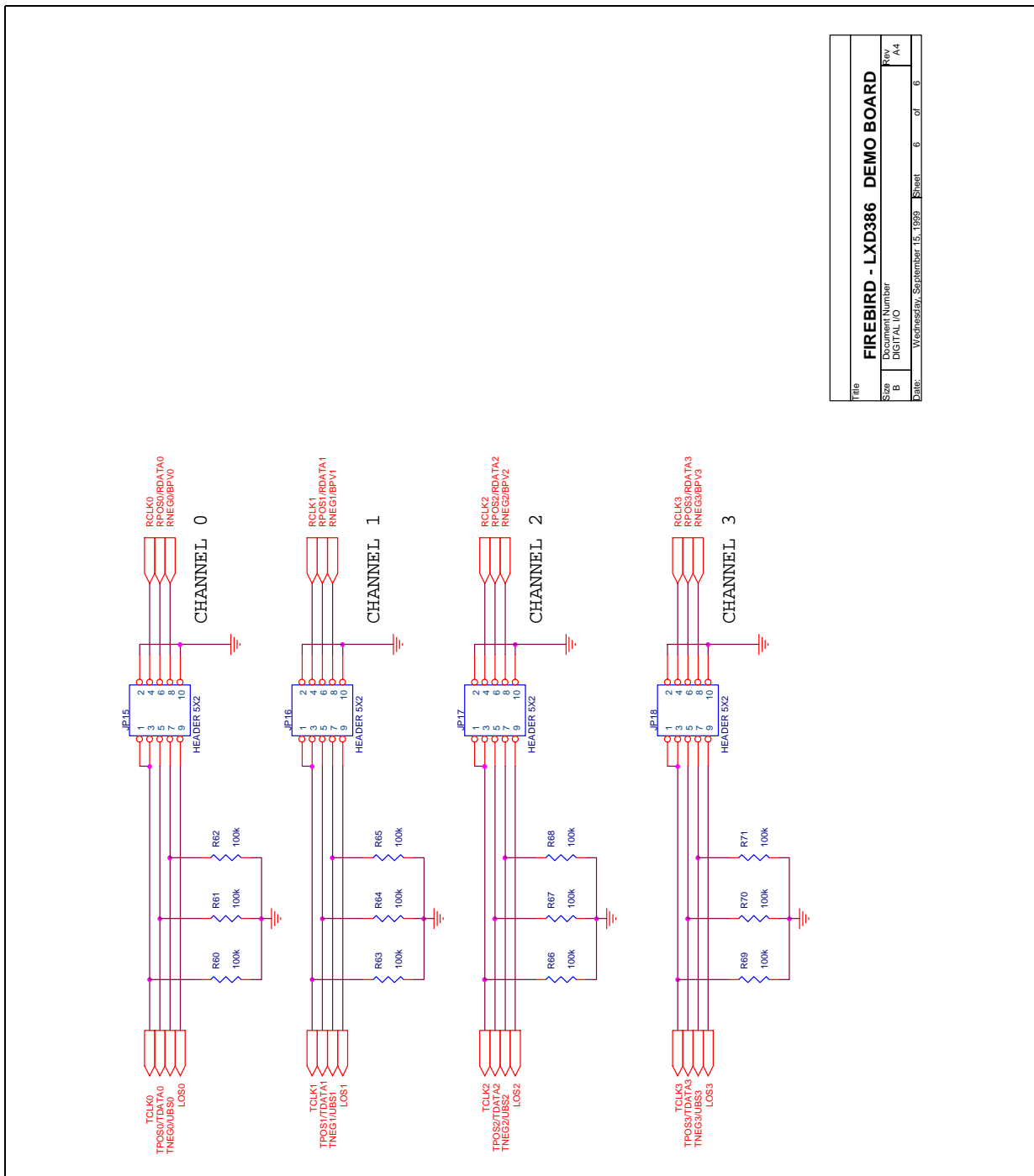
| | | | |
|-------|-------------------------------|-------|--------|
| File | FIREBIRD - LX386 DEMO BOARD | | |
| Size | Document Number | Rev. | A4 |
| B | LOS 1 | | |
| Date: | Wednesday, September 15, 1999 | Sheet | 4 of 6 |

Figure 13. Evaluation Board Schematic — Analog



| | |
|-------|--------------------------------------|
| File | IS |
| Title | FIREBIRD - LXD386 DEMO BOARD |
| Size | Document |
| Rev | A4 |
| Doc | ANALOG |
| Date | Wednesday, September 15, 1999 5 of 6 |

Figure 14. Evaluation Board Schematic — Digital I/O



| | | | |
|-------|-------------------------------|-----------------------------|--------|
| Title | | FIREBIRD - LX386 DEMO BOARD | |
| Size | Document Number | Rev | |
| B | DIGITAL I/O | A4 | |
| Date: | Wednesday, September 15, 1999 | Sheet | 6 of 6 |

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