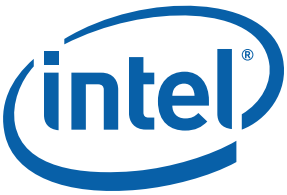

Intel NetStructure® MPCBL0010 Single Board Computer

Technical Product Specification

October 2006

Order Number: 304120

Contents

Figures

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Revision History

Date	Revision	Description
September 2006	002	Updated to include the following: -- new Chapter 11, “Serial over LAN” -- CMOS_CLR jumper change -- new sensor threshold data -- change to sensor name, Temp CPLD Area -- new section 3.8.2.1 for other flashInx command options -- new information about using ipmitool in section 3.8.3 -- corrected duplicate section names in 4.3.2 and 4.3.3 -- new note in section 6.7 to clarify additional boot options -- new sysfs interface subsection 12.4.15 in Chapter 12, “Telecom Clock”
March 2006	001	Intial release of this document.

1.0 Introduction

1.1 Document Organization

This document provides technical specifications related to the Intel NetStructure® MPCBL0010 Single Board Computer (SBC). The MPCBL0010 SBC is designed following the standards of the Advanced Telecommunications Compute Architecture (AdvancedTCA*) Design Guide for high availability, switched network computing. This document is intended for support during system product development and while sustaining a product. It specifies the architecture, design requirements, external requirements, board functionality, and design limitations of the MPCBL0010 Single Board Computer (SBC).

The focus of each section in this document can be summarized as follows:

Chapter 1.0, "Introduction" gives an overview of the information contained in this document as well as a glossary of acronyms and important terms.

Chapter 2.0, "Feature Overview" introduces the key features of the MPCBL0010.

Chapter 3.0, "Operating the Unit" provides basic instructions for configuring and upgrading the MPCBL0010.

Chapter 4.0, "Specifications" contains the mechanical, environmental, and reliability specifications for the MPCBL0010.

Chapter 5.0, "Connectors and LEDs" includes an illustration of LEDs, connector locations, connector descriptions, and pinout tables.

Chapter 6.0, "BIOS Features" provides an introduction to the Intel/AMI BIOS, and the System Management BIOS, stored in flash memory on the MPCBL0010.

Chapter 7.0, "BIOS Setup" describes the interactive menu system of the BIOS setup program.

Chapter 8.0, "Error Messages" lists BIOS error messages, Port 80h POST codes, and provides a brief description of each.

Chapter 9.0, "Addressing" lists the PCI devices and the buses on which they reside, as well as FPGA registers.

Chapter 10.0, "Hardware Management Overview" provides a detailed overview of the IPMI implementation based on PICMG* 3.0 and IPMI v1.5 specifications in the MPCBL0010.

Chapter 11.0, "Serial Over LAN (SOL)"provides detailed information about Serial over LAN (SOL), including architecture, theory of operations, use cases, configuration, and installation.

Chapter 12.0, "Telecom Clock" describes the operations of the telecom clock, its various interfaces, and the API used by the telecom clock module.

Chapter 13.0, “Maintenance” includes supervision and diagnostics information.

Chapter 14.0, “Thermals” describes pressure drop curves versus the flow rate in accordance with PICMG 3.0 Specification..

Chapter 15.0, “Component Technology” lists the major components used on the MPCBL0010.

Chapter 16.0, “Warranty Information” provides warranty information for Intel NetStructure® products.

Chapter 17.0, “Customer Support” provides information on how to contact customer support.

Chapter 18.0, “Certifications” and Chapter 19.0, “Agency Information—Class B” document the regulatory requirements the MPCBL0010 is designed to meet.

Chapter 19.0, “Agency Information—Class B” contains precautions to avoid personal injury and prevent damage to this product or products to which it is connected.

Appendix A, “Reference Documents” provides a list of datasheets, standards, and specifications for the technology designed into the MPCBL0010.

Appendix B, “List of Supported Commands (IPMI v1.5 and PICMG 3.0)” provides lists of commands supported by IPMI v1.5 and PICMG Specification 3.0.

1.2 Glossary

ACPI	Advanced Configuration and Power Interface.
AdvancedMC*	Advanced Mezzanine Card. The AdvancedMC is a modular add-on card that extends the functionality of the SBC.
AdvancedTCA	Advanced Telecommunications Compute Architecture
AMC	Advanced Mezzanine Card. See AdvancedMC.
BIOS	Basic Input/Output Subsystem. ROM code that initializes the computer and performs some basic functions.
Blade	An assembled PCB card that plugs into a chassis.
DIMM	Dual Inline Memory Module. A small card with memory on it that is used with the MPCBL0010.
EEPROM	Electrically Erasable Programmable Read-Only Memory.
Fabric Board	A board capable of moving packet data between Node Boards via the ports of the backplane. This is sometimes referred to as a switch.
Fabric Slot	A slot supporting a link port connection to/from each Node Slot and/or out of the chassis.
FRED	Field Recovery Device
FWUM	Firmware Upgrade Manager used for upgrading IPMI firmware.
Hyper-Threading Technology† (HT Technology)	Allows a single physical processor, to appear as two logical processors to a HT Technology-aware operating system.
I^2C*	Inter-IC (Integrated Circuit). Two-wire interface commonly used to carry management data.

IBA	Intel® Boot Agent. The Intel Boot Agent is a software product that allows your networked client computer to boot using a program code image supplied by a remote server.
IDE	Integrated Device Electronics. Common, low-cost disk interface.
IPMB	Intelligent Platform Management Bus. Physical two-wire medium to carry IPMI.
IPMC	Intelligent Platform Management Controller. ASIC on baseboard responsible for low-level system management.
IPMI	Intelligent Platform Management Interface. Programming model for system management.
KCS	Keyboard Controller Style interface.
LPC Bus	Low Pin Count Bus. Legacy I/O bus that replaces ISA and X-bus. See the Low Pin Count (LPC) Interface specification.
MTBF	Mean Time Between Failure. A reliability measure based on the probability of failure.
NEBS	National Equipment Building Standards. Telco standards for equipment emissions, thermal, shock, contaminants, and fire suppression requirements.
NMI	Non-Maskable Interrupt. Low-level PC interrupt.
Node Board	A board capable of providing and/or receiving packet data to/ from a Fabric Board via the ports of the networks. The term is used interchangeably with SBC.
MPCBL0010	Single Board Computer.
Node Slot	A slot supporting port connections to/from Fabric Slot(s). A Node slot is intended to accept a Node Board.
PCB	Printed Circuit Board.
Physical Port	A port that physically exists. It is supported by one of many physical (PHY) type components.
PLL	Phase-locked Loop.
ROM	Read-Only Memory.
SATA	Serial ATA (Advanced Technology Attachment). A physical storage interface.
SBC	Single Board Computer. This term is used interchangeably with Node Board.
SEL	System Event Log. Action logged by management controller.
ShMC	Shelf Management Controller.
SMBus	System Management Bus. Similar to I^2C.
SMI	System Management Interrupt. Low-level PC interrupt which can be initiated by chipset or management controller. Used to service IPMC or handle things like memory errors.
SMS, SMSC	Standard Microsystems Corporation*.
SOL	Serial over LAN
USB	Universal Serial Bus. General-purpose peripheral interconnect, operating at 1-12 Mbps.

2.0 Feature Overview

2.1 Application

The Advanced Telecommunications Compute Architecture (AdvancedTCA*) standards define open architecture modular computing components for a carrier-grade, communications network infrastructure. The goals of the standards are to enable blade-based modular platforms to be:

- cost effective
- high-density
- high-availability
- scalable

These systems use a fabric I/O network for connecting multiple, independent processor boards, I/O nodes (e.g., line cards), and I/O devices (e.g., storage subsystem).

The MPCBL0010 Single Board Computer (SBC) is designed according to the AdvancedTCA Design Guide for High Availability, Switched Network Computing.

2.2 Functional Description

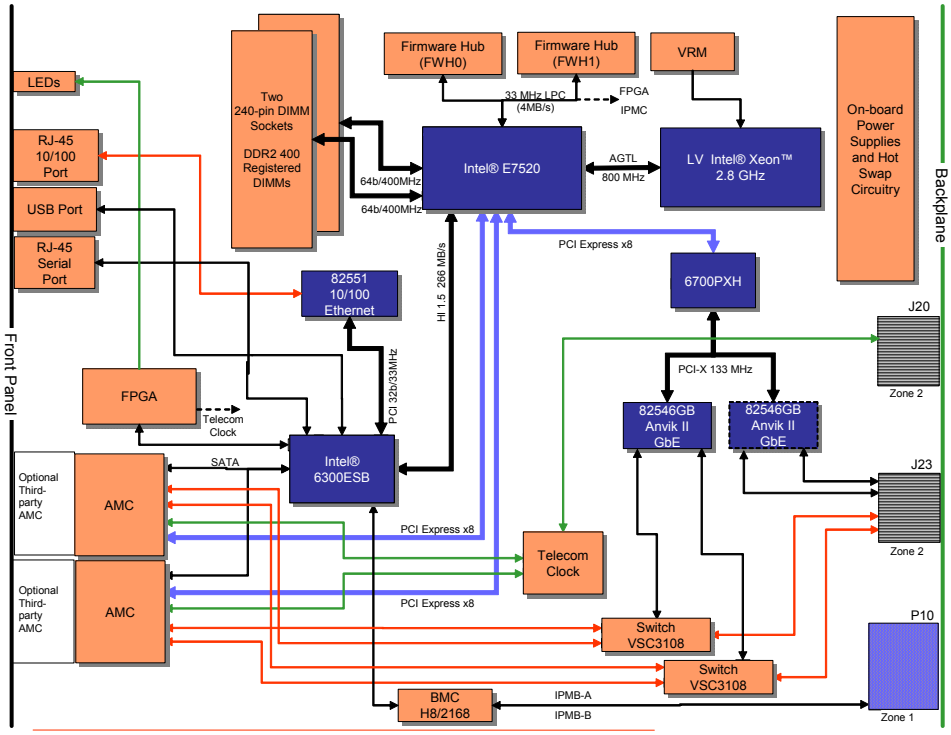
This topic defines the architecture of the MPCBL0010 SBC through descriptions of functional blocks. Figure 1 shows the functional blocks of the MPCBL0010 SBC. The MPCBL0010 SBC is a hot-swappable SBC with backplane connections to gigabit Ethernet networks.

The SBC incorporates an Intelligent Platform Management Controller that monitors critical functions of the board, responds to commands from the shelf manager, and reports events.

Power is supplied to the MPCBL0010 SBC through two redundant -48 V power supply connections. Power for on-board hardware management circuitry is provided through a standby converter. This converter is fed by the diode OR'd -48 V supply from the backplane.

The SBC has provision for the addition of two AdvancedMC* devices and also offers one USB port and one service terminal interface (serial port). An overview of each block is shown in Figure 1.

Figure 1. MPCBL0010 Block Diagram



2.2.1 Low Voltage Intel® Xeon™ Processor

The MPCBL0010 SBC supports a single Low Voltage Intel® Xeon™ processor. This LV Xeon processor with 800 MHz system bus is designed for high-performance. Based on the Intel® NetBurst™ microarchitecture and Hyper-Threading Technology† (HT Technology), it is binary-compatible with previous Intel® Architecture (IA-32) processors.

Low Voltage Xeon processors require their package case temperatures to be operated below an absolute maximum specification. If the chassis ambient temperature exceeds a level whereby the processor thermal cooling subsystem can no longer maintain the specified case temperature, the processor will automatically enter a mode called Thermal Monitor to reduce its case temperature. Thermal Monitor controls the processor temperature by modulating the internal processor core clocks and reducing internal power dissipation and it does not require any interaction by the operating system or application. Once the case temperature has reached a safe operating level, the processor will return to its non-modulated operating frequency.

See the Low Voltage Xeon processor datasheet, referenced in Appendix A, “Reference Documents”, for further details.

2.2.2 Chipset

The MPCBL0010 SBC uses the Intel® E7520 chipset, which consists of the following major components:

- Intel® E7520 Memory Controller Hub (MCH)
- Intel® 6300ESB I/O Controller Hub (ICH)

- Intel® 6700PXH 64-bit PCI Hub

A brief overview is provided here and detailed component information can be found in each device's respective documentation.

2.2.2.1 Memory Controller Hub

The architecture of the Intel® E7520 MCH provides the performance and feature set required for performance servers, with configuration options facilitating optimization of the platform for workloads characteristic of communication, presentation, storage, performance computation, or database applications. To accomplish this optimization, the MCH has numerous Reliability, Availability, Serviceability, Usability, and Manageability (RASUM) features on multiple interfaces.

The front side bus supports a base system bus frequency of 200 MHz. The address and request interface is double-pumped to 400 MHz while the 64-bit data interface (+ parity) is quad-pumped to 800 MHz. This arrangement provides a matched system bus address and data bandwidths of 6.4 GBytes/s. The MCH provides an integrated memory controller for direct connection to registered DDR2-400 memory.

The MCH is compatible with PCI Express* *Interface Specification, Rev 1.0a*. The MCH provides three configurable x8 PCI Express interfaces, each with a max theoretical bandwidth of 4 GBytes. The MCH supports PCI Express Hot Swap. The MCH is a root class component as defined in the PCI Express Interface Specification, Rev1.0a.

The MCH connects with the 6300ESB ICH through a dedicated Hub Interface 1.5 that supports a peak bandwidth of 266 MByte/s using a x4 base clock of 66 MHz.

2.2.2.2 I/O Controller Hub

The Intel®6300ESB ICH provides legacy function support similar to that of previous ICH-family devices, but with extensions in Serial ATA technology and 32-bit/33 MHz PCI-X support. The 6300ESB ICH also includes integrated USB 2.0 and USB 1.0 support, an LPC interface, a system management interface, a power management interface, integrated IOxAPIC and 8259 interrupt controllers, and an integrated DMA controller.

2.2.2.3 64-Bit PCI Hub

The Intel® 6700PXH PCI Hub provides the connection between a PCI Express interface and two independent PCI bus interfaces configurable for standard PCI 2.3 protocol, as well as the enhanced high-frequency PCI-X 1.0b protocol. The 6700PXH provides configurable support for 32- or 64-bit PCI devices.

The MPCBL0010 SBC implements four gigabit Ethernet interfaces by means of two high-speed Intel® 82546GB Dual Port Gigabit Ethernet controllers. These controllers are connected to the 6700PXH through a shared PCI-X interface. One controller is connected to the base interface and the other to the fabric interface on the AdvancedTCA backplane to support PICMG 3.0 and 3.1 specifications.

2.2.3 Memory (J10, J12)

The memory subsystem is designed to support Double Data Rate2 (DDR2) Synchronous Dynamic Random Access Memory (SDRAM) using the E7520 MCH. The MCH provides two independent DDR channels, which support DDR2-400 DIMMs. The peak bandwidth of each DDR2 branch channel is 3.2 GByte/s (8 bytes x 400 MT/s) with DDR2-400. The two DDR2 channels from the MCH operate in lock step; the effective overall peak bandwidth of the DDR2 memory subsystem is 6.4 GByte/s for DDR2 400.

Note: Two 25-degree 240-pin DIMMs theoretically support memory configurations up to 8 GBytes of PC2-3200 registered DDR2-400 SDRAM, but only memory configurations of 2 GBytes and 4 GBytes have been validated.

Table 1. Supported Memory Configurations

Total Memory	J10	J12
2 GBytes	1 GByte DDR2-400 DIMM	1 GByte DDR2-400 DIMM
4 GBytes	2 GBytes DDR2-400 DIMM	2 GBytes DDR2-400 DIMM

Note: See the *Intel NetStructure® MPCBL0010 High-Performance Single Board Computer Compatibility Report*, available on the Intel web site, for a complete list of validated memory.

Memory scrubbing is supported and enabled on the MPCBL0010 SBC as described in the Intel E7520 chipset datasheet. There is no additional configuration or driver support required. The memory subsystem is periodically checked and cleansed as the scrubbing process repeats itself over and over. If a correctable memory error is found it is fixed automatically and a "Correctable ECC" event is sent to the SEL. If uncorrectable memory errors are found, an "Uncorrectable ECC" event is sent to the SEL.

2.2.4 I/O

2.2.4.1 I/O Controller Hub

The 6300ESB ICH includes integrated USB 2.0 and USB Classic support, SATA, an LPC interface, a system management interface, a power management interface, integrated IOxAPIC and 8259 interrupt controllers, and an integrated DMA controller.

See the 6300ESB ICH product-specific documentation as noted in Appendix A, “Reference Documents”for further details.

2.2.4.2 Real-Time Clock

The MPCBL0010 SBC real-time clock is integrated into the ICH. It is derived from a 32.768 kHz crystal with the following specifications:

- Frequency tolerance @ 25 ºC: ±20 ppm
- Frequency stability: maximum of -0.04ppm/$(\Delta ºC)^2$
- Aging $\Delta F/f$ (1^{st} year @ 25º C): ±3 ppm
- ±20ppm from 0-55º C and aging 1 ppm/year

The real-time clock is powered by a 0.22 F SuperCap capacitor when main power is not applied to the board. This capacitor powers the real-time clock for a minimum of two hours while external power is removed from the MPCBL0010 SBC.

2.2.4.3 Timers

The 6300ESB ICH provides three timers. Each is implemented as a single counter with its own comparator and value register. Each timer’s counter increases monotonically. Each individual timer can generate an interrupt when the value in its value register matches the value in the main counter. Some of the timers can be enabled to generate a periodic interrupt.

The registers associated with these timers are mapped to a memory space (much like the I/O APIC). However, this memory space is not implemented as a standard PCI function. The BIOS reports to the operating system the location of the register space.

The hardware may support an assignable decode space; however, the BIOS will set this space prior to handing it over to the OS. It is not expected that the OS will move the location of these timers once the space is set by the BIOS.

In the 6300ESB ICH, one timer block is implemented. The timer block has one counter and three timers (comparators). Various capabilities registers indicate the number of timers and the capabilities of each.

2.2.4.3.1 Timer Accuracy

The timers are accurate over any 1 ms period to within 0.005% of the time specified in the timer resolution fields. Within any 100 ms period, the timer will report a time that is up to two ticks too early or too late. Each tick is less than or equal to 100 ns, so this represents an error of less than 0.2%. The timer is monotonic. It will not return the same value on two consecutive reads (unless the counter has rolled over and reached the same value). The main counter will be clocked by the 14.31818 MHz clock, synchronized into the 66.666 MHz domain. This method results in a non-uniform duty cycle on the synchronized clock, but it does have the correct average period. The main counter will be as accurate as the 14.3818 MHz clock.

2.2.4.4 Gigabit Ethernet

The MPCBL0010 SBC implements four gigabit Ethernet interfaces. Two of these interfaces are routed to the AdvancedTCA base interface and operate in copper mode, and the other two are optionally routed to the AdvancedTCA fabric interface in SERDES mode on the AdvancedTCA backplane to support PICMG 3.0 and 3.1 specifications. These four GbE interfaces are connected through the Intel 6700PXH and use the Intel® 82546GB Dual Port Gigabit Ethernet Controller.

2.2.4.5 10/100 Fast Ethernet

A single 10/100 Fast Ethernet port is routed to the front panel of the SBC and may be used as a debug Ethernet port. This Ethernet interface is connected to the 6300ESB ICH through the Intel® 82551ER 10BASE-T/100BASE-TX Ethernet Controller.

2.2.4.6 USB 2.0

The MPCBL0010 SBC has one USB connector that supports USB 2.0 and 1.1. This connector enables the daisy chaining of as many as 127 devices per interface. USB supports Plug and Play and Hot Swapping operations (OS level) which allows USB devices to be automatically attached, configured, and detached, without rebooting. USB devices such as a floppy drive or a CD-ROM drive can be used as boot devices for the MPCBL0010 SBC.

2.2.4.7 Serial Ports

The MPCBL0010 SBC supports two serial ports and is software compatible with NS16C550. Serial port 1 is routed to the front panel RJ-45 connector for normal operation. Serial port 2 is routed to the IPMC.

2.2.5 AdvancedMC (AMC) Connector (J18, J19)

The MPCBL0010 SBC has two single-width, full-height AdvancedMC* slots. The AdvancedMC slots are connected to the E7520 MCH with PCI Express x8 to each slot. Each AdvancedMC slot has an opening in the front panel of the SBC that exposes the I/O connectors of the add-in AdvancedMCs.

The MPCBL0010 SBC does not support double-width, half-height, or stacked half-height AdvancedMC modules.

In addition to the PCI Express connections to the AdvancedMC slots, SATA and AdvancedTCA zone 2 telecom clock signals are also connected to each AdvancedMC slot. The MPCBL0010 SBC features a two-channel bus master PCI SATA interface through the 6300ESB ICH. Each channel supports one device and is available through the AdvancedMC module slots.

Each of these x8 PCI Express ports routed to the AdvancedMC connectors can train with a link width of x8, x4, or x1. The PCI Express raw bit-rate on the data pins of 2.5 Gbit/s results in the bandwidth per pair of 250 MBytes/s given the 8/10 encoding used to transmit data across this interface. The result is a maximum theoretical realized bandwidth on an x8 PCI Express port of 2 GBytes/s in each direction or an aggregate of 4 GBytes/s.

The MPCBL0010 SBC supports AdvancedMC modules with a maximum power consumption of 20 watts for each AdvancedMC slot, and it has independent hot swap circuitry for +12 V and +3.3 V connections.

Note: Do not operate the MPCBL0010 SBC without filler panels or AdvancedMC modules installed. The AdvancedMC module slots should not be left open or uncovered when the MPCBL0010 SBC is in use. The two slot filler panels included with the SBC are provided to optimize cooling and radiated emissions for the SBC.

Note: Shipping the MPCBL0010 SBC with third party AdvancedMC modules installed may cause damage to the SBC or AdvancedMCs. Shipping damage that occurs to the MPCBL0010 SBC due to AdvancedMC modules installed during shipment may not be covered by the SBC product warranty.

2.2.6 Firmware Hubs

The MPCBL0010 SBC supports two 8 Mbit (1 MByte) BIOS flash ROMs (Firmware Hubs):

- Primary BIOS flash ROM (FWH0)
- Recovery BIOS flash ROM (FWH1)

The flash is allocated for BIOS and firmware use.

The SBC boots from the primary flash ROM under normal circumstances. During the boot process, if the BIOS (or IPMC) determines that the contents of the primary flash ROM are corrupted, a hardware mechanismautomatically changes the flash device select logic to the recovery flash ROM and restarts the boot process.

Each flash component has a separately write-protected boot block that prevents erasure when the device is upgraded.

Flash ROM BIOS updates can be performed by an end user locally, or a network administrator over the LAN via telnet. The SBC should have a local copy of the flash update utility and the BIOS data files, or have the capability to copy the flash update utility and BIOS data files onto a local drive from the network. The flash update utility has a command line interface to specify the path and the file name of the BIOS data files. After completing the BIOS ROM update, users should shutdown and reset the SBC for the new BIOS ROM to take effect.

2.2.6.1 FWH0 (Main BIOS)

The BIOS executes code off of the flash ROM and performs checksum validation of its operational code. This checksum occurs in the BIOS boot block. The BIOS image is also stored in FWH0 firmware hub. During a BIOS update, the BIOS image is stored in FWH0 only. FWH0 also stores the factory default CMOS settings and user-configured CMOS settings.

2.2.6.2 FWH1 (Backup/Recovery BIOS)

The FWH1 firmware hub stores the recovery BIOS. In the event of a checksum failure on the main BIOS operational code, the BIOS requests the BMC to switch firmware hubs, so that the board can boot up from FWH1 for recovery.

2.2.6.3 Flash ROM Backup Mechanism

The on-board Intelligent Platform Management Controller (IPMC) manages which of the two BIOS flash ROMs is used during the boot process. The IPMC monitors the boot progress and can change the flash ROM selection and reset the processor.

The Intelligent Platform Management Controller sets the ID for both firmware hub (FWH) devices. The default state is to configure the main firmware hub (FWH) ROM device ID to be the boot device; the backup FWH is assigned the next ID. The backup FWH responds to the address range just below the main FWH ROM in high memory.

Boot accesses are directed to the FWH with ID = 0; unconnected ID pins are pulled low by the FWH device. In this way the IPMC can select which flash ROM is used for the boot process.

2.2.7 Onboard Power Supplies

The main power supply rails on the MPCBL0010 SBC are powered from dual-redundant -48 V power supply inputs from the AdvancedTCA backplane power connector (P10). There are also dual redundant, limited current, make-last-break-first (MLBF) power connections.

2.2.7.1 Power Feed Fuses

As required by the PICMG 3.0 specification, the MPCBL0010 SBC provides fuses on each -48 V power feed and on the RTN connections as well. The fuses on the return feeds are critical to preventing overcurrent situations if an ORing diode in the return path fails and there is a voltage potential difference between the A and B return paths.

2.2.7.2 ORing Diodes and Circuit Breaker Protection

The two -48 V power sources are ORed together. A current limiting FET switch is connected between the ORed -48 V sources and the primary DC-DC converters. The FET switch provides three functions:

- A mechanism to electrically connect/disconnect the SBC to/from the two -48 V inputs.
- A soft-on function.
- An electronic over-current circuit breaker feature.

2.2.7.3 Isolated -48 V to +12 V, 12 V Suspend, 5 V, 3.3 V Suspend, 1.8 V, and 1.5 V Converters

These converters provide DC isolation between the -48 V and -48 V return connections and all of the derived DC power on the MPCBL0010 SBC. A 12 V rail provides up to 10 A of current mainly for processor VRM and the two AdvancedMC slots. A 5 V output provides up to 2 A of current mainly for USB. The 3.3 V suspend provides the main 3.3 V when back end power is enabled. Up to 6 A of 3.3 V is provided when board is full on. The converter's 1.8 V output provides up to 25 A of current, and the 1.5 V provides up to 18 A of current. The 12 V suspend and 3.3 V suspend outputs are always enabled. When the board is in the suspend state, no more than 10 W is drawn from the -48 V input (as specified in PICMG 3.0). All other outputs are enabled under IPMC control.

Current values here indicate the maximum that can be delivered by design and do not reflect the current actually provided on the MPCBL0010 SBC. Additionally, each converter has design margin. The maximum current that can be drawn by the SBC in operation is 200 Watts, conforming with the AdvancedTCA 3.0 specification.

2.2.7.4 Processor Voltage Regulator Module (VRM)

The Voltage Regulator Module (VRM) provides core power to the Low Voltage Xeon processor. The input to the VRM is connected to the +12 V power rail.

The VRM controller is designed to support the processor core voltages selected by the voltage identification (VID) pins on the processor. The VRM is disabled until all other voltage converters indicate “power good.” The voltage regulator module is designed to support one Low Voltage Xeon at up to 60 A of current.

2.2.7.5 IPMC Subsystem Standby Power

The IPMC subsystem standby power is 3.3 V suspend, as described in Section 2.2.7.3.

2.2.7.6 Other On-board Supplies

The 2.5 V power rail is derived from the 3.3 V rail using a standard buck converter. This rail is limited to 3 A of current. Vtt for the CPU is derived from the 1.5 V rail using a linear regulator.

2.2.7.7 Other Suspend Power

The 5 V suspend is derived from the 12 V suspend using a linear regulator at < 1 A. The 1.8 VSB and 1.5 VSB are derived from the 3.3 V suspend using linear regulators all at < 1 A.

2.2.8 IPMC

The MPCBL0010 SBC uses the Renesas* H8S/2168 for the Intelligent Platform Management Controller (IPMC). The IPMC provides a management subsystem for monitoring, event logging, and recovery control. The IPMC serves as the gateway for management applications to access the platform hardware. Some of the key features are:

- Compliant with PICMG 3.0 and IPMI v1.5 rev 1.1
- Automatic rollback capability if an upgrade fails
- Upgradeable from the IPMI KCS interface
- Support for AdvancedMC via IPMB-L
- Supports initiation of a graceful shutdown on the host CPU and ShMC notification insertion and removal.

2.2.9 Telecom Clock

The MPCBL0010 SBC supports a telecom clock synchronization circuit. This circuit uses the Zarlink* ZL30410 Multi-Service Line Card PLL and a PLD that act as a clock multiplexer on inputs and outputs. The clock can be synchronized to any of the AdvancedTCA backplane clocks, CLK1A/B and CLK2A/B. Any of the output clocks can be routed to the AdvancedMC CLKA and CLKB signals.

Control and status registers are implemented in the FPGA. States are synchronized between the FPGA and the PLD through a 33MHz full-duplex synchronous serial link. The FPGA being attached to the main processor as well as the IPMC allows for flexibility, and accesses to the control/status registers are simple and fast.

The PLL and clock buffers are not powered in the suspend well and stop working when the SBC is powered down.

The following frequencies can be selected individually for an AdvancedMC module:

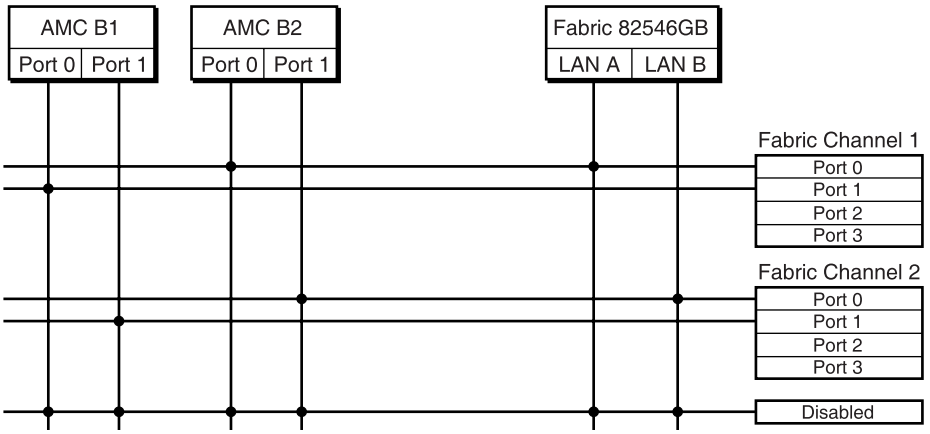
- 8 kHz
- 1.544 MHz
- 2.048 MHz
- 4.096 MHz
- 6.312 MHz
- 8.192 MHz
- 8.592 MHz
- 11.184 MHz
- 19.44 MHz
- 34.368 MHz
- 44.735 MHz

For more information on the telecom clock, see Section 12.0, “Telecom Clock”.

2.2.10 AdvancedMC Direct Connect

The AdvancedMC Direct Connect feature on the MPCBL0010 SBC enables connections from the AdvancedMC module directly to the AdvancedTCA backplane zone 2 fabric interface through a cross-point switch. This connection can be used instead of the on-board gigabit Ethernet connection that is normally routed to the AdvancedTCA fabric interface. Figure 2 displays the possible connection paths. Each intersecting dot in the diagram represents a programmable switch setting that can be set using IPMI OEM commands or through the BIOS configuration. This feature is compatible with the AdvancedMC .2 R1.0 specification.

Figure 2. AdvancedMCA Direct Connect Switch Block Diagram



2.2.11 AdvancedTCA Compliance

The MPCBL0010 SBC conforms to the following specifications:

- PICMG 3.0 R2.0
- PICMG 3.1 R1.0 (Ethernet/Fiber Channel over AdvancedTCA)
- AdvancedMC.0 R1.0
- AdvancedMC.1 R1.0
- AdvancedMC.2 R1.0
- AdvancedMC.3 R1.0
- ACPI R1.0

3.0 Operating the Unit

3.1 Jumpers

The MPCBL0010 SBC contains several jumper posts that allow the user to configure certain options not configurable through the BIOS setup utility. Figure 3 shows the placement of the MPCBL0010 SBC jumpers. The MPCBL0010 SBC is shipped pre-configured and jumper positions do not generally need to be altered.

Figure 3. Jumpers

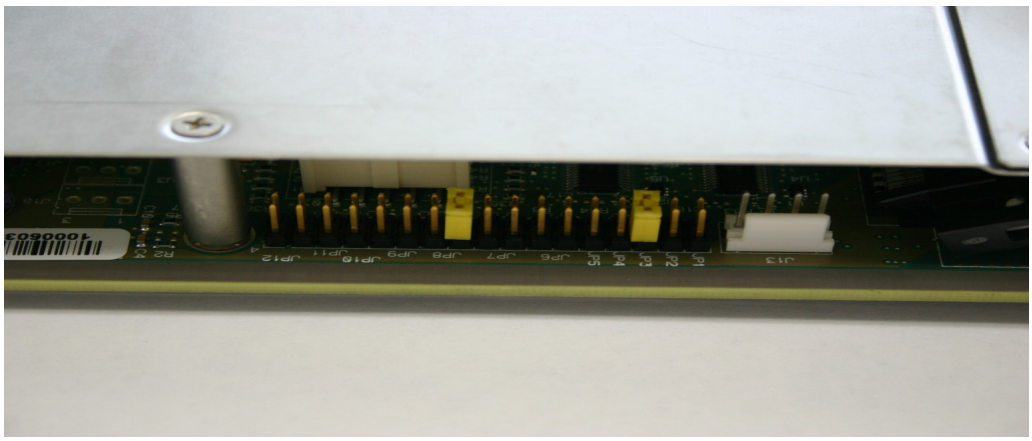


Figure 4 shows the jumper locations on the SBC. Table 2 gives definitions for each of these jumpers.

Figure 4. Jumper/Connector Locations

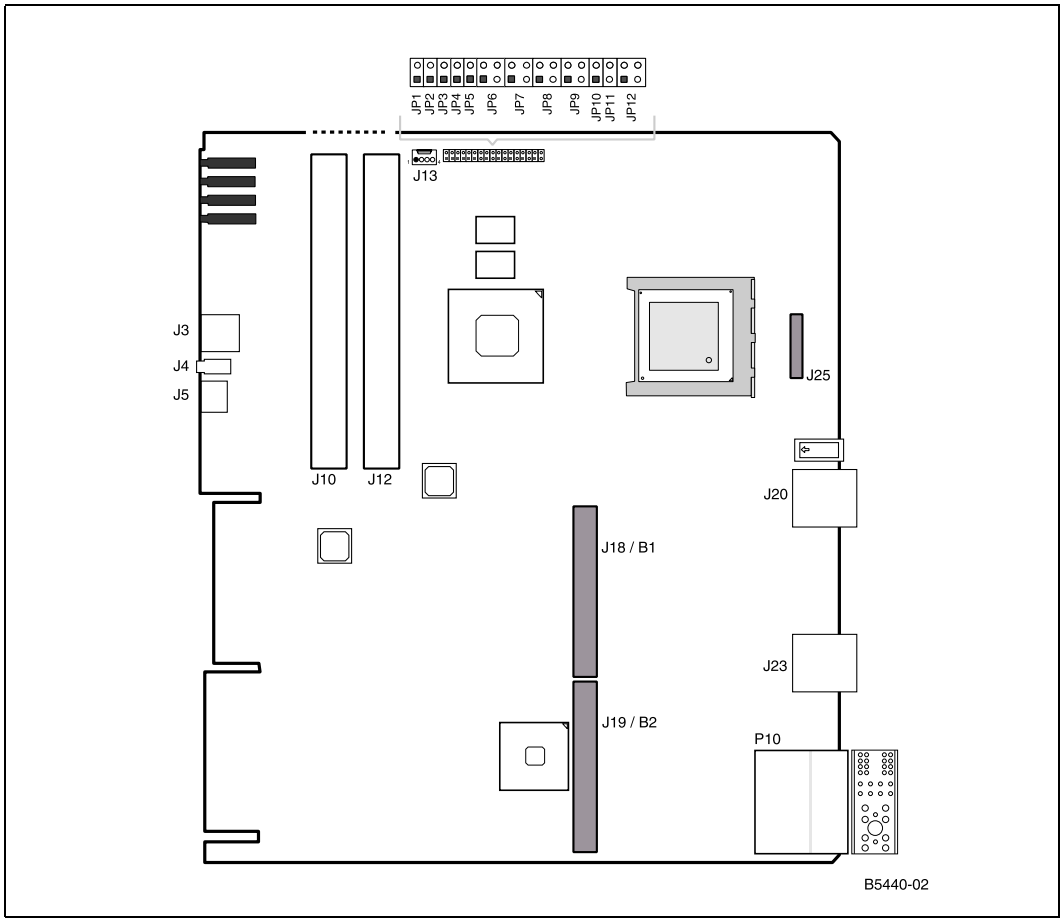


Table 2. Jumper Definitions

Name	Function with Jumper Present (On)	Function with Jumper Removed (Off)
JP3 VT100 Mode	Enabled (default)	Disabled
JP5 Clear CMOS	Clear CMOS	Normal operation (default)
JP6 IPMC Override for MPCBL0010 SBC (posts 1-2)	SBC Activation Override. This setting is used when there is not an AdvancedTCA shelf manager to activate the MPCBL0010 SBC. Setting this jumper allows the SBC to power up without a shelf manager.	Require AdvancedTCA shelf manager to activate MPCBL0010 SBC (default).
JP6 IPMC Override for AdvancedMC (posts 3-4)	AdvancedMC Activation Override. This setting is used when there is not an AdvancedTCA shelf manager capable of activating the AdvancedMC modules installed in the MPCBL0010 SBC. Setting this jumper allows the AdvancedMCs to power up without shelf manager support.	Require AdvancedTCA shelf manager to activate AdvancedMC modules installed in the MPCBL0010 SBC (default).
JP7 POST code (posts 1-2)	POST code to IPMC	POST code to BIOS (default)

Table 2. Jumper Definitions (Continued)

Name	Function with Jumper Present (On)	Function with Jumper Removed (Off)
JP7 IPMC Override (posts 3-4)	IPMC is completely disabled and always in RESET mode. This setting can be used to allow the MPCBL0010 SBC to boot if the IPMC firmware is corrupted or non-functional.	Normal IPMC operation (default)
JP8 FPGA Config	User PROM (default)	Factory PROM (for manufacturing purposes only)
JP10 Test Mode	Test Mode (for manufacturing purposes only).	Normal (default)
JP11 AdvancedMC PCI-Express Reference Clock Override	Override AdvancedMC E-Keying and provide PCI-Express Reference Clock to the AdvancedMC connectors.	Use normal AdvancedMC E-keying (default)

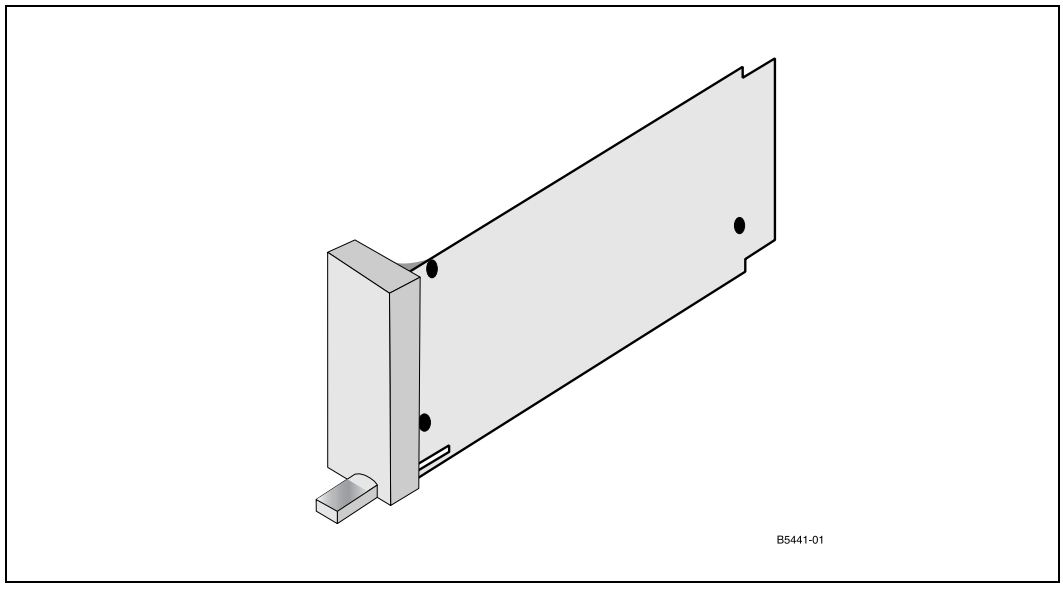
Note: Jumpers JP2, JP1, JP4, JP9, and JP12 are reserved for future use.

3.2 AdvancedMC Filler Panels

AdvancedMC* filler panels are used to optimize cooling and reduce radiated emissions when AdvancedMC modules are not installed in theMPCBL0010 SBC AdvancedMC module slots. Do not operate the MPCBL0010 SBC without filler panels or AdvancedMC modules installed. AdvancedMC module slots should not be left open or uncovered when the MPCBL0010 SBC is in use.

The MPCBL0010 SBC uses full-height, half-width AdvancedMC filler panels such as Schroff* part number # 20849-024 (http://www.schroff.us/).

Figure 5. AdvancedMC Filler Panel



3.3 Installing Memory

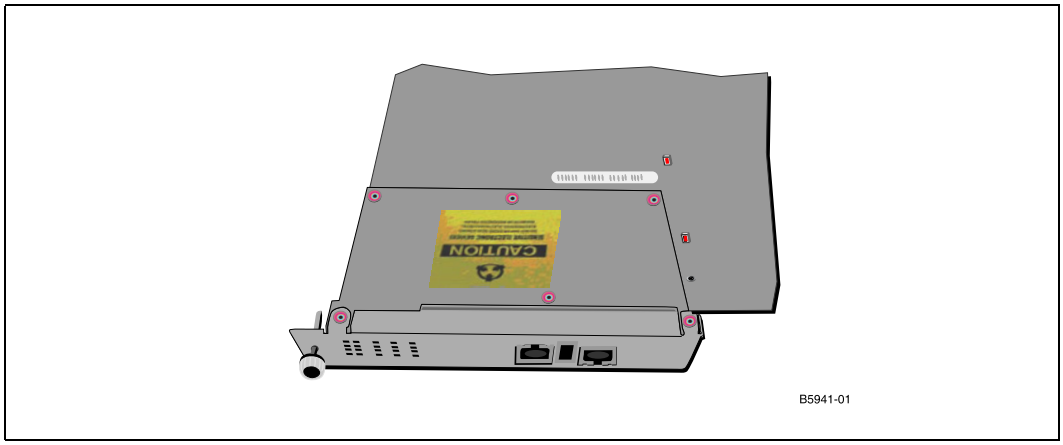
DDR2-400 DIMMs must be installed in matched pairs. Memory DIMMs of 1 GBytes or 2 GBytes are supported for a total of 2 Gbytes (2x1 Gbyte) or 4 Gbytes (2x2 Gbytes) of system memory. Matched pairs in this case means a pair of DIMMs equal in speed, density, and technology. Preferably, the same vendor and part number for both pairs. See the *MPCBL0010 SBC Compatibility Report* on the Intel web site for a list of approved memory part numbers and vendors.

To install memory:

Caution: Electrostatic discharge (ESD) can damage components. Install the memory in an ESD-controlled area. If such an area is not available, wear an antistatic wrist strap or touch the surface of the antistatic package before handling the SBC and memory.

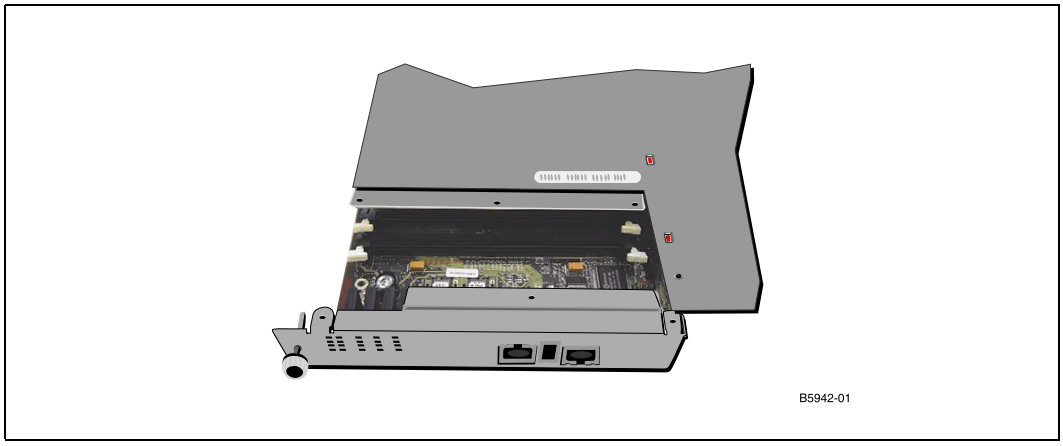
1. Remove all six screws pictured in Figure 6 from the memory access panel on the MPCBL0010 SBC top cover.

Figure 6. Memory Top Cover Installed



2. Remove the cover.

Figure 7. Empty DIMM Sockets



3. Insert two matched pair DIMMs.

Warning: Using excessive force to install memory can damage the DIMM socket and/or circuit board.

Figure 8. Memory Installed

4. Reinstall the cover.
5. Reinstall the six cover screws.

Note: Should any of the cover screws get lost in this process, the specifcations for them are:

- Flat head Phillips screws countersunk M2.5 x 3.4
- Steel with Precote* 80 (pink) coating all around

3.4 Installing and Extracting the SBC

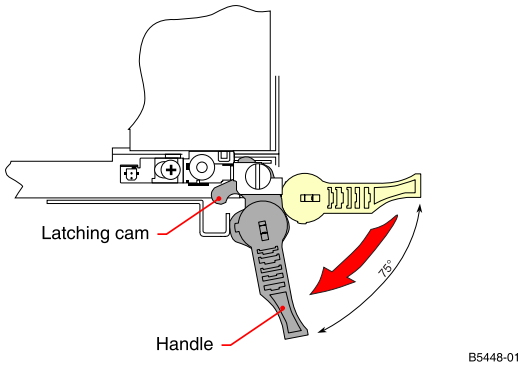
The ability to replace SBCs without affecting the operation of the chassis is a major element of the PICMG AdvancedTCA standard. This Hot Swap functionality requires a faceplate ejector handle designed to the PICMG specifications. The new handle has two important functions:

- **Activate the Hot Swap microswitch on the chassis.** The handle does this by sliding inward at the start of the extraction procedure.
- **Operate within a narrow range of motion.** The handle is designed to provide clearance from other chassis components (cables, cable trays, PEMs, etc.) that would otherwise interfere with handle movement in some installations. It also allows clearance for AdvancedMCs to be installed or removed while the SBC is operating in the chassis. This is accomplished through a ratcheting mechanism where the handle is connected to the latching cam (See the illustration in Section 3.4.1, “Chassis Installation”).

Please review the procedures below before attempting to install or remove the MPCBL0010 SBC from an AdvancedTCA chassis.

3.4.1 Chassis Installation

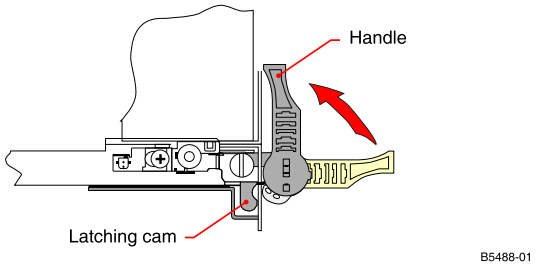
1. Insert the MPCBL0010 SBC into the chassis with the latching cams at a 75º angle. This will set the latching cams into the installation position. Move the latching cam by pressing the handle inward to free the latching cam for rotation.



2. While holding inward pressure on the handle, slide the MPCBL0010 SBC into the chassis. Begin rotating the latching cam back to 0º allowing the cam to assist with insertion. As the SBC is inserted, the AdvancedTCA backplane connectors are mated to the SBC. If necessary, use your thumbs to apply pressure to the SBC faceplate near the handles to make sure the SBC is fully inserted.

Caution: Do not apply pressure to the AdvancedMC faceplate, as this could damage the connectors at the rear of the AdvancedMC module.

3. Once the SBC is installed, rotate the handles into the vertical position.



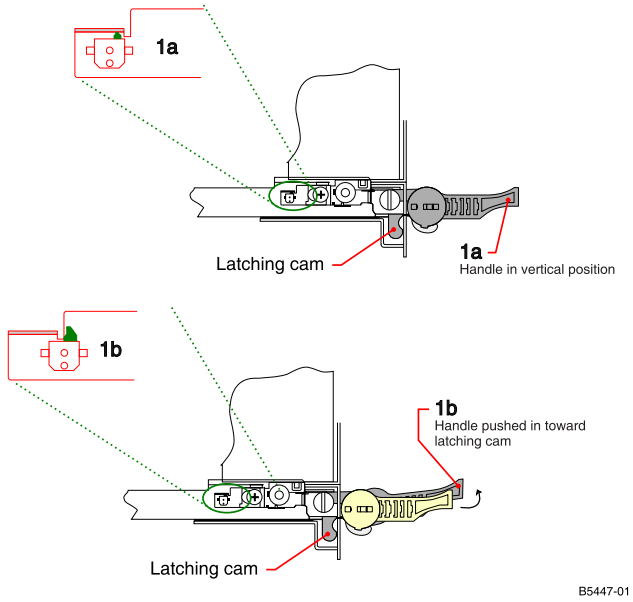
3.4.2 Chassis Extraction

The AdvancedTCA Hot Swap switch is activated by pushing in the lower handle (or the left handle when the SBC is mounted in the horizontal position). When the handle is pushed inward, a small metal slider will activate the Hot Swap switch.

Note: The ratcheting function of the handle allows the handle to be moved without affecting the position of the latching cam that holds the SBC in the chassis (see illustration in

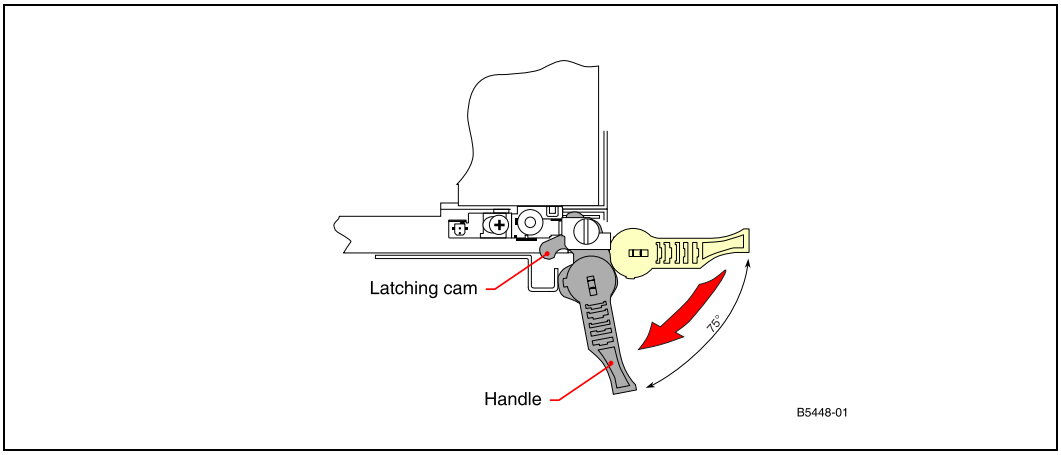
Section 3.4.1). To rotate the cam, the handle must be pushed in towards the SBC when moving the handle up or down.

1. Rotate the lower handle to the horizontal position, and push in to disengage the Hot Swap switch (position 1a to 1b). Wait for the Hot Swap LED on the faceplate to turn solid blue.

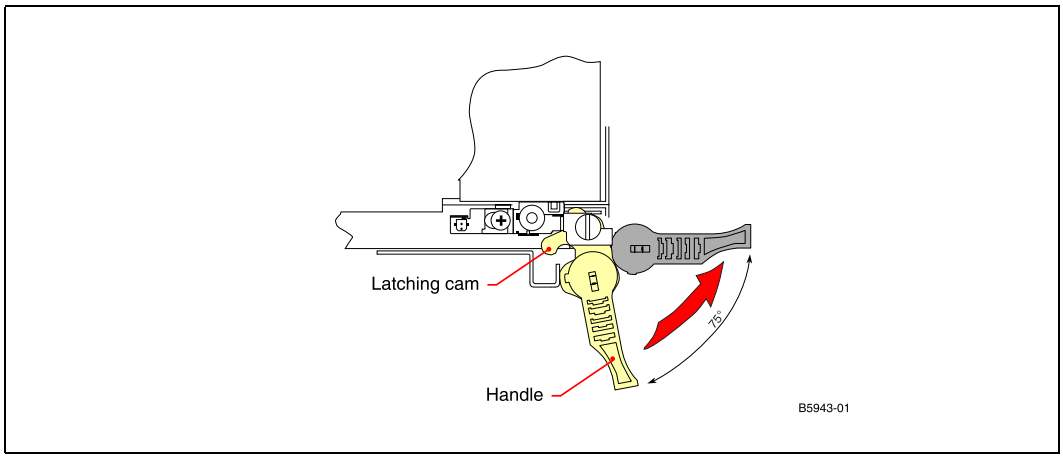


2. With the handles pushed in, simultaneously pivot the top handle up and the bottom handle down. Using the handles, rotate the latching cam to their farthest point of travel. This is the pitch line— the farthest the handles can be moved without hitting the cable tray or other chassis component.

Note: The handles must be pushed in for the latching cam rotation to occur.



3. Release the handles to allow the ratchet mechanisms to disengage from the cams, and reposition the handles to the horizontal position (the cams will remain at an angle to the horizontal).



4. Simultaneously push both handles in again and rotate until the handles are at their farthest point of travel. Repeat this process until the SBC faceplate is clear of the chassis. At this point the SBC can be removed from the chassis.

3.5 AdvancedMC Module Installation and Extraction

To install or remove an AdvancedMC* module into the MPCBL0010 SBC, simply move the SBC handle from the vertical to the horizontal position. This will move the handle out of the way of the AdvancedMC slot and allow modules to be inserted or removed.

Note: Do not push the SBC handle inward because this will activate the Hot Swap switch.

Refer to the AdvancedMC manufacturer user manual for other considerations specific to the AdvancedMC module you are using.

3.6 BIOS Configuration

In most cases, the BIOS defaults will provide the correct configuration to use the board. See Chapter 7.0, “BIOS Setup” for a complete list of BIOS options.

3.7 Remote Access Configuration

Console redirection to the serial port is enabled by default. This setting will redirect the text output of the BIOS and operating system to the RJ-45 serial port on the MPCBL0010 SBC. Remote access using serial console redirection allows users to monitor the boot process and run the BIOS setup from a remote serial terminal. The default settings used for console redirection to the serial port are 115,200, n, 8, 1, and no flow control. See Chapter 5.0, “Connectors and LEDs” for the pin connection of this interface.

3.8 Software Updates

It is important to use compatible BIOS, FPGA, and IPMC firmware versions. Since all the software and hardware versions are exchanging specific information, they must be in synch. Always follow the documentation instructions included with the software updates.

You can download software updates for the MPCBL0010 SBC from this Intel web site:

http://www.intel.com/design/telecom/products/cbp/atca/9445/overview.htm

3.8.1 BIOS Updates

At times, new BIOS images will be released to the Intel web site which may add additional features to the SBC. The BIOS update release package contains the BIOS ROM image, as well as the flash update utilities. The BIOS update release package also contains detailed instructions about how to update the BIOS.

3.8.2 Loading\Saving Custom BIOS Configuration

The CMOS settings, together with the BIOS binary image, can be copied to a file with a file name specified by the user. This allows the user to save BIOS settings from one SBC and then load the settings onto several other SBCs. The **flashlnx** utility used to perform this function is included in the BIOS update release package on the Intel web site.

3.8.2.1 Synchronizing BIOS Image and Settings from FWH0 (Main) to FWH1 (Backup)

Prior to upgrading the main BIOS (FWH0), a user can create a mirror image where all the operational codes and CMOS settings will be copied to a redundant BIOS Flash device. Preserving a copy of the old BIOS image prior to updating the main BIOS is suggested in case the FWH0 update fails.

The syntax `./flashlnx -m` can be used to initiate this transfer. See the suggested method in Table 3.

Table 3. Suggested Method of BIOS Image Synchronization prior to BIOS Upgrade

BIOS Image	Command	Behavior
FWH0 Image N FWH1 Image N-1		• This is the original FWH images before an upgrade. • FWH0 has Image N installed, which is a newer image than what is installed in FWH1, which is Image N-1.
FWH0 Image N FWH1 Image N	./flashlnx –m	• The user can initiate a BIOS update while the OS is running. • When this command is executed, the Image N in FWH0 (BIOS codes + CMOS settings) is synchronized to FWH1. Image N has now been copied to the backup FWH1 BIOS image. • No reboot is needed for this operation.
Note: N = BIOS version		

Table 3. Suggested Method of BIOS Image Synchronization prior to BIOS Upgrade

FWH0 Image N+1 FWH1 Image N	./flashlnx –b Pxx-xxxx	• When this command is initiated, the FWH0 image will be updated to the latest version (Image N+1). • The latest version of the BIOS will take effect after the user initiates a reset. • If a checksum error is detected on FWH0 after a reboot, it will automatically switch to FWH1 and regain normal operation.
Note: N = BIOS version		

3.8.2.2 Copying BIOS.bin from the SBC

1. Copy the **flashlnx** utility to an SBC running Linux with custom BIOS CMOS settings that will be used to update other SBCs.

2. Issue the command "`./flashlnx -r -afff00000 -s1048576 BIOS.bin`" to copy the BIOS with the customized CMOS settings to the same directory from which **flashlnx** is executed. All user-preferred settings (including the BIOS image) will be saved in the file named ***BIOS.bin***.

Note: "***BIOS.bin***" is a generic file name used here to illustrate the command line used to perform the operation. You may wish to use the BIOS version as the file name instead of ***BIOS.bin***.

3.8.2.3 Saving BIOS.bin to the SBC

1. Copy the **flashlnx** utility and ***BIOS.bin*** to the SBC running Linux.
2. Execute "`chmod +x flashlnx`" to change the file attribute to an executable form.
3. Execute "`./flashlnx -b -zc BIOS.bin`" to copy the ***BIOS.bin*** file to the firmware hub (FWH) and CMOS.
4. Upon completion, perform a reset to ensure the new CMOS settings and BIOS are loaded.

Note: To ensure that the ***BIOS.bin*** file is not corrupted, Intel strongly suggests performing these steps before major deployment of any SBCs running in a live network environment.

3.8.2.4 flashInx Command Line Options

Table 4 lists the command line parameter switches and features supported by the BIOS flash utility.

Table 4. FlashInx Utility Command Line Options

Command Line Parameter	Description
-b [option] bios_image where possible [option] values are: • -z - do not clear the CMOS • -zc - update the CMOS from image	Program a BIOS image to primary fimware hub (FWH0)
-i [bios_image]	Display BIOS system information
-r [options] bin_image where possible [option] values are: • -aAddress - physical address in hex • -pPage - page number in decimal • -sSize - image size in decimal	Read the flash image and store to a file
-m	Mirror image where all the operational codes and CMOS settings are copied from FWH0 to FHW1 (redundant BIOS flash device)
-b cmos_image	Backup current CMOS settings to a file
-r cmos_image	Restore CMOS settings from a file
-q	Force non-interactive mode (assumes “yes” for all prompts)

3.8.3 IPMC Firmware Updates

Periodically, new IPMC firmware with additional features will be released to the Intel web site. The IPMC firmware is upgraded using the KCS interface. The IPMC firmware update release package contains the IPMC firmware as well as the update utility. The update release package also contains detailed instructions about how to update the IPMC firmware.

3.8.3.1 IPMC Firmware Upgrade Using the KCS Interface

The KCS interface is the communication mechanism between the host processor on the MPCBL0010 SBC and the IPMC controller. A firmware update utility is available. It takes a hex file to be updated as input from the command line. It can also verify that updates are completed successfully by reading back data written to the flash memory.

The utility typically takes around two minutes to complete the update over the KCS interface. After the firmware update is completed, the controller goes through a reset and boots up with the new firmware. IPMC communication is temporarily lost during the update, but the host processor is not reset when going through a firmware update, so the operating system and applications running on the host processor are not interrupted.

Updating the IPMC firmware requires using *ipmitool 1.8.8* or later. Download ipmitool from http://ipmitool.sourceforge.net/

1. Download and compile *ipmitool 1.8.8* or later for your Linux system.
2. Download the IPMC firmware file from the MPCBL0010 SBC product web site specified in Section 3.8, “Software Updates”
3. Run the following commands to update the IPMC firmware to the newly downloaded version:

```
# ipmitool fwum download <IPMI FW file>.bin
# ipmitool fwum upgrade <IPMI FW file>.bin
```

4. To verify that the upgrade worked properly, run the following command:

```
# ipmitool fwum status
```

The output of this command should show the "last known good" version to be the same as the version just upgraded to. The "previous good" version should show the previous version before the upgrade.

5. To roll back the lat upgraded version, run the following command:

```
# ipmitool fwum rollback
```

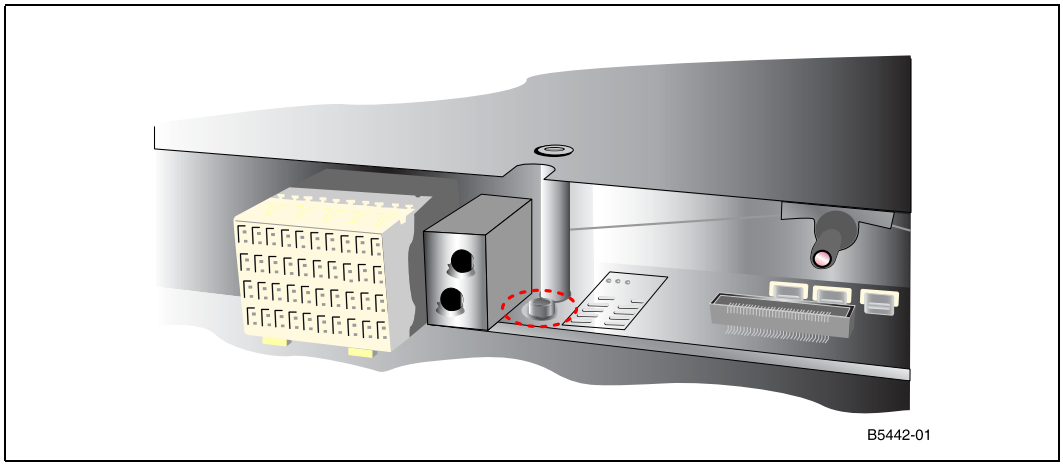
Note: You can also use **Get Device ID IPMI** to verify the current reported version of the IPMI firmware.

3.9 Digital Ground to Chassis Ground Connectivity

The default grounding for the MPCBL0010 SBC is that digital ground is isolated from the chassis ground. To connect the digital ground to the chassis ground, install a stainless steel M2.5 x 6 Phillips pan head screw into the hole next to the AdvancedTCA K1 alignment block (circled in red in Figure 9) on the MPCBL0010 SBC. The screw must be tightened to 4 lb. per in.

Note: Digital ground is also called logic ground. Chassis ground is also known as shelf ground.

Figure 9. Digital Ground and Chassis Ground Isolated (Default)



4.0 Specifications

This section defines the Intel NetStructure® MPCBL0010 Single Board Computer operating and storage environments. It also documents the procedures followed to determine the reliability of the MPCBL0010 SBC.

4.1 Mechanical Specifications

4.1.1 Board Outline

The MPCBL0010 SBC form factor is mechanically compliant to PICMG 3.0 specification of 322.25 mm x 280.00 mm (12.687" x 11.024"). The board pitch is 6HP, and the PCB thickness is 2.0 mm (+/-0.2 mm).

4.1.2 Backing Plate and Top Cover

The MPCBL0010 SBC has a rugged metal backing plate that forms a single-piece faceplate. This backing plate is made of stainless steel (SS304) and is approximately 0.65 mm thick on bottom, and 1.0 mm thick at the faceplate. The top cover is made from stainless steel (SS304) and is approximately 0.65 mm thick. A removable cutout is provided in the top cover for easy access to memory modules.The solid backing plate and top cover provides PCB stiffening, enhanced EMI protection from adjacent boards, and protection during flame tests.

Caution: Removing the backing plate can damage the components on the board and may void the warranty. No user-serviceable parts are available under the PCB. Do not remove the face plate/backing plate.

4.2 Environmental Specifications

The MPCBL0010 SBC meets the board-level specifications as specified in the *Intel Environmental Standards Handbook – Telco Specification,* Document #A78805-01. The test methodology is a combination of Intel and NEBs test requirements with the intent that the product will pass pure system-level NEBs testing. Intel will not be completing NEBs testing on the SBC. The following table summarizes environmental limits, both operating and nonoperating.

Table 5. Environmental Specifications (Sheet 1 of 2)

Parameter	Conditions	Detailed Specification
Temperature (Ambient)	Operating	0 to 55° C
	Storage	-40 to 70° C
Airflow	Operating	30 cubic feet per minute (CFM) minimum
Humidity	Operating	15%-90% (non-condensing) at 55° C
	Storage	5%-95% (non-condensing) at 40° C

Table 5. Environmental Specifications (Sheet 2 of 2)

Altitude	Operating	4000 m (13123 ft.) ***Note:*** May require additional cooling above 1800 m (5905 ft.)
	Storage	15000 m (49212 ft.)
Unpackaged Vibration	Operating	Sine sweep: • 5 to 100 Hz: 1G @ 0.25 Octave/minute • 100 to 500 Hz: 1G @ 1 Octave/minute Random profile: • 5 Hz @ 0.01 g2 /Hz to 20 Hz @ 0.02 g2 /Hz (slope up) • 20 Hz to 500 Hz @ 0.02 g2 /Hz (flat) • 3.13 g RMS, 10 minutes per axis for all 3 axes
	Storage	5 to 50 Hz: 0.5G @ 0.1 Octave/minute 50 to 500 Hz: 3G @ 0.25 Octave/minute.
Shock	Operating	30G/11 ms half sine
	Storage	50G, 170 inches/second trapezoidal

4.3 Reliability Specifications

4.3.1 Mean Time Between Failure (MTBF) Specifications

Calculation Type: MTBF/FIT Rate

Standard: Telcordia* Standard SR-332 Issue 1

Methods: Method I, Case I, Quality Level II

The calculation results were generated using the references and assumptions listed. This report and its associated calculations supersede all other released MTBF and Failure in Time (FIT) calculations of earlier report dates. The reported failure rates do not represent catastrophic failure. Catastrophic failure rates will vary based on application environment and features critical to the intended function.

Table 6. Reliability Estimate Data

Reliability Measure	Value
Failure Rate (FIT)	8967 failures in 10^9 hours
MTBF	111,513 hours

4.3.1.1 Environmental Assumptions

- Failure rates are based on a 40° C ambient temperature.
- Applied component stress levels are 50 percent (voltage, current, and/or power).
- Ground, fixed, controlled environment with an environmental adjustment factor equal to 1.0.

4.3.1.2 General Assumptions

- Component failure rates are constant.
- Board-to-system interconnects included within estimates.
- Non-electrical components (screws, mechanical latches, labels, covers, etc.) are not included within estimations.
- Printed circuit board is considered to have a 0 FIT rate.

4.3.1.3 General Notes

- Method I, Case I = Based on parts count. Equipment failure is estimated by totaling device failures rates and quantities used.
- Quality Level II = Devices purchased to specifications, qualified devices, vendor lot-to-lot controls for AQLs and DPMs.
- Where available, direct component supplier predictions or actual FIT rates have been used.
- The SBC MTBF does not include addition of the AdvancedMC cards. The product MTBF could be significantly impacted by adding AdvancedMC cards. Please contact the AdvancedMC card manufacturer for specific component and relevant operational MTBF information.

4.3.2 Power Requirements

The power consumed by the MPCBL0010 SBC is dependent on the configuration. Table 7 shows typical consumption values.

Table 7. Power Requirements

Operating Modes	Voltage
Normal	-43 VDC to -72 VDC
Degraded	-38 VDC to < -43 VDC
Non-Operating	0 VDC to < -38 VDC, -72 VDC to -75 VDC

Note: These voltages assume a 1 V round trip drop on power signals between shelf power input terminals and board/module slots.

Note: IPMC is powered with input voltage as low as -36 V.

4.3.3 Power Consumption

Table 8. Total Measured Power

Memory	Power
4 Gbytes (two 2 Gbyte DIMMs)	Max power = < 160 watts

4.4 Weight

Table 9 shows packaged and unpackaged weight.

Table 9. Weight

Configuration	Weight	Comments
Packaged	7 lb 6 0z 3.35 kg	Includes MPCBL0010 SBC, AMC filler panels, and packaging material. Does not include DIMMs.
Unpackaged	5 lb 6 oz 2.44 kg	Includes MPCBL0010 SBC and AMC filler panels. Does not include DIMMs.

5.0 Connectors and LEDs

Connectors along the rear edge of AdvancedTCA* server blades are divided into three distinct zones, as described in Section 2.3 of the PICMG 3.0 specification:

- Zone 1 for system management and power distribution
- Zone 2 for data fabric
- Zone 3 for the rear transition module (not used on the MPCBL0010 SBC)

As shown in Figure 10, the MPCBL0010 SBC includes several connectors to interface with application-specific devices. Some of the connectors are available at the front panel as shown in Figure 11. A detailed description and pinout for each connector is found in the following sections.

Figure 10. Connector Locations

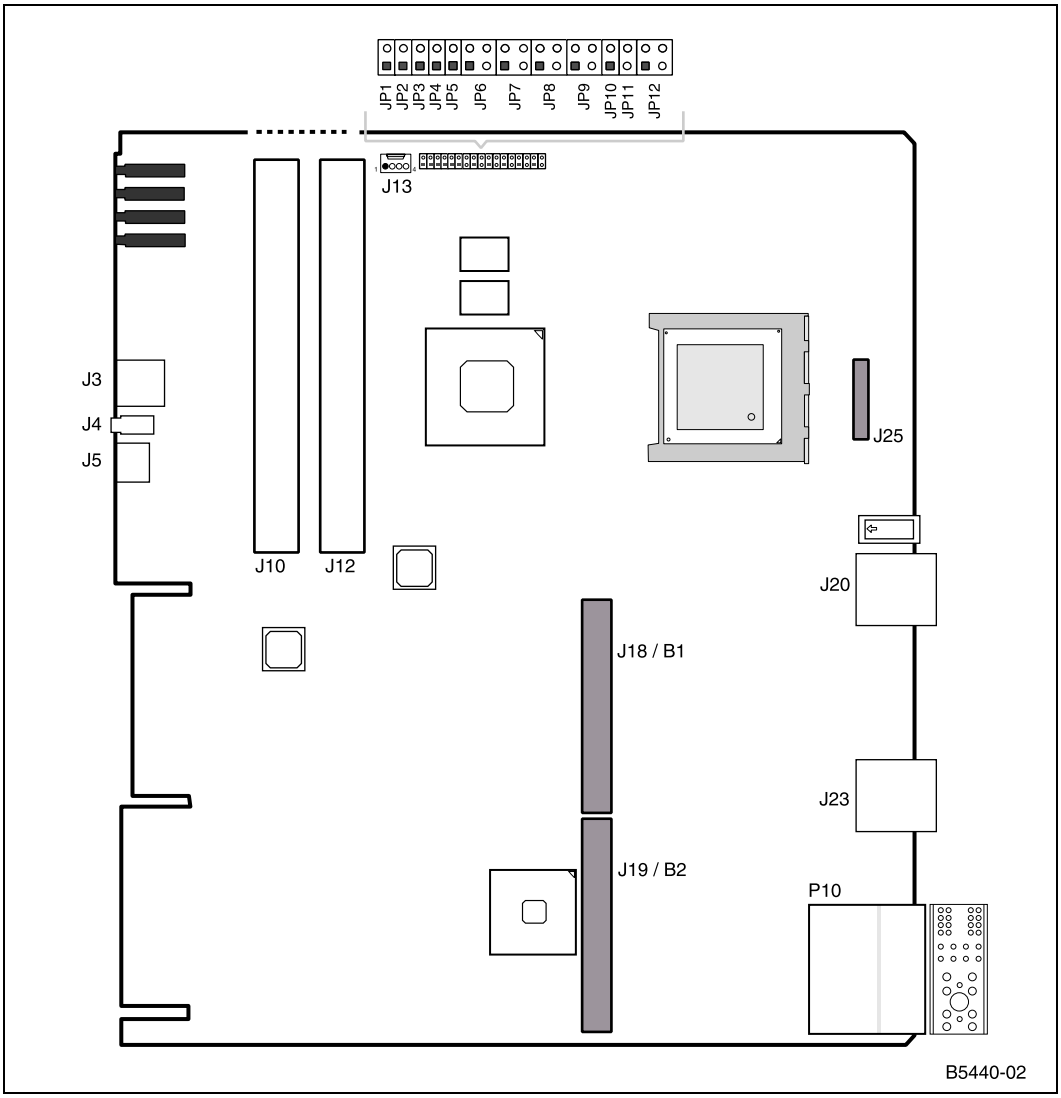


Table 10. On-board and Backplane Connector Assignments

Backplane Connectors	Description
J10, J12	Memory Socket
J13	POST Code (factory use only)
J25	Extend ITP700 (see Chapter 12 Maintenance)
J20	AdvancedTCA Telecom Clockz (Zone 2)
J23	AdvancedTCA Base and Fabric Interfaces (Zone 2)
P10	AdvancedTCA Power and IPMB

Figure 11. Front Panel

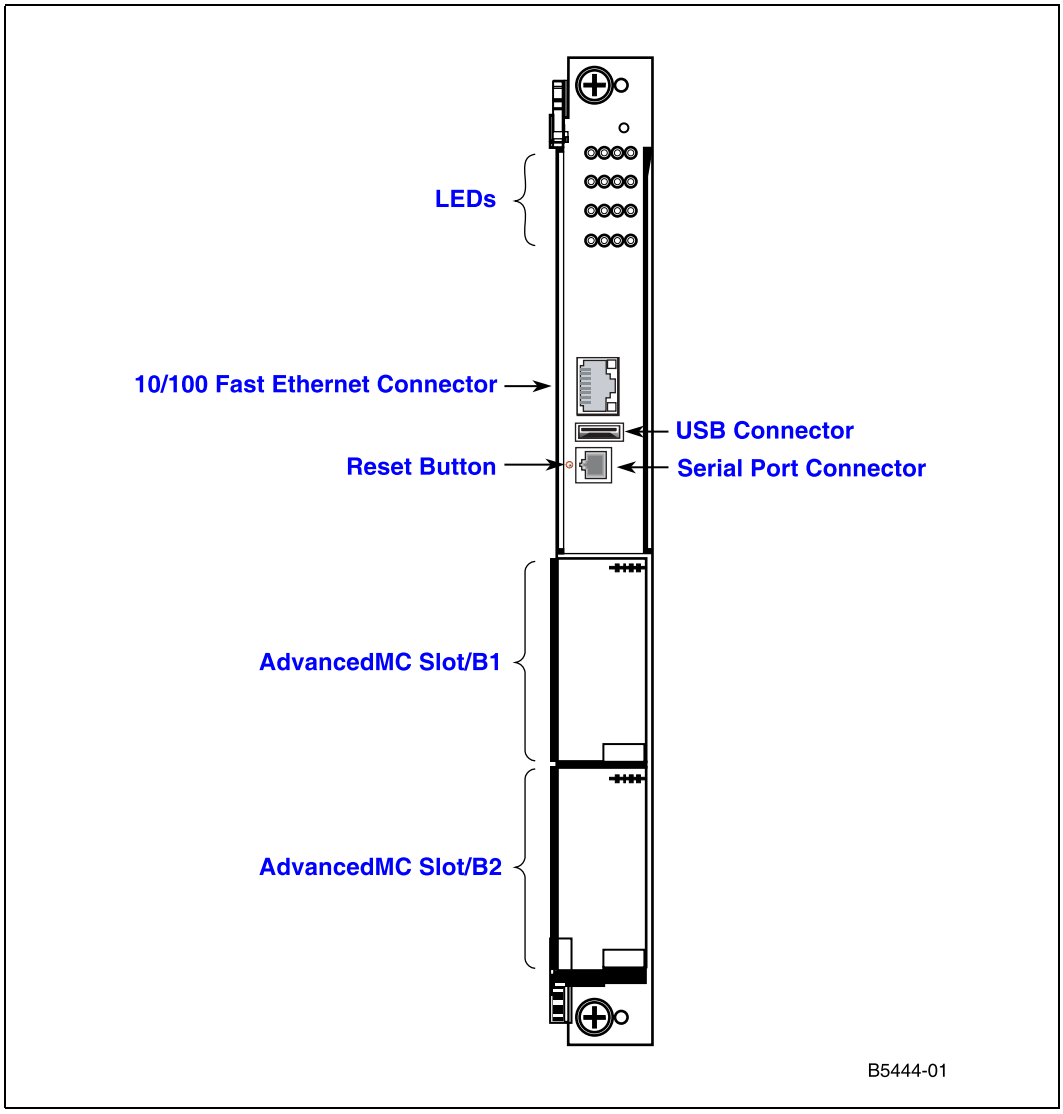


Table 11. Front Panel Connector Assignments

Front Panel Connectors	Description
J3	10/100 Ethernet Debug Port
J4	USB 2.0
J5	Serial Port (RJ-45)
J18, J19	AdvancedMC Connectors

5.1 Backplane Connectors

5.1.1 Power Distribution Connector (P10)

Zone 1 consists of P10, a blue 34-pin Positronic* header connector that provides the following signals:

- Two -48 VDC power feeds (four signals each; eight signals total)
- Two IPMB ports (two signals each, four signals total)
- Geographic address (eight signals)
- 5.55 A allocated to the MPCBL0010 SBC on the -48 VDC redundant power feeds -- this is equivalent to 200 Watts at the minimum input voltage (-36 VDC)

The connector used is Positronic* part number VPB30W8M6200A1. Figure 12 shows the mechanical drawing of the connector. The pin assignments are given in Table 12.

Figure 12. Power Distribution Connector (Zone 1) P10

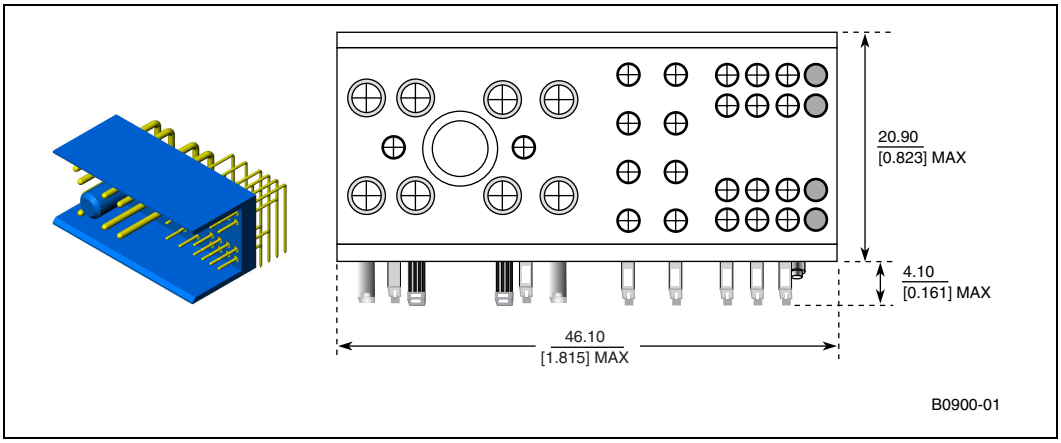


Table 12. Power Distribution Connector (Zone 1) P10 Pin Assignments

Pin	Signal	Description	Pin	Signal	Description
1	NCt	No Connection	18	Unused	No Connection
2	NC	No Connection	19	Unused	No Connectiont
3	NC	No Connectiont	20	Unused	No Connection
4	NC	No Connection	21	Unused	No Connection
5	GA0	Geographic Addr Bit 0	22	Unused	No Connection
6	GA1	Geographic Addr Bit 1	23	Unused	No Connection
7	GA2	Geographic Addr Bit 2	24	Unused	No Connection
8	GA3	Geographic Addr Bit 3	25	EMI_GND	EMI Chassis Ground
9	GA4	Geographic Addr Bit 4	26	LOGIC_GND	Gnd Ref for Card Logic
10	GA5	Geographic Addr Bit 5	27	ENABLE_B	Enb DC-DC conv, B Feed
11	GA6	Geographic Addr Bit 6	28	VRTN_A	-48 V Return, Feed A
12	GA7/P	Geo Adr Bit 7 (Odd Parity)	29	VRTN_B	-48 V Return, Feed B
13	IPMB_CLK_A	IPMB Bus A Clock	30	- 48 V_EARLY_A	-48 V In, Feed A Precharge
14	IPMB_DAT_A	IPMB Bus A Data	31	-48 V_EARLY_B	-48 V In, Feed B Precharge
15	IPMB_CLK_B	IPMB Bus B Clock	32	ENABLE_A	Enb DC-DC conv, A Feed
16	IPMB_DAT_B	IPMB Bus B Data	33	-48V_A	-48 V Input, Feed A
17	Unused	No Connection	34	-48V_B	-48 V Input, Feed B

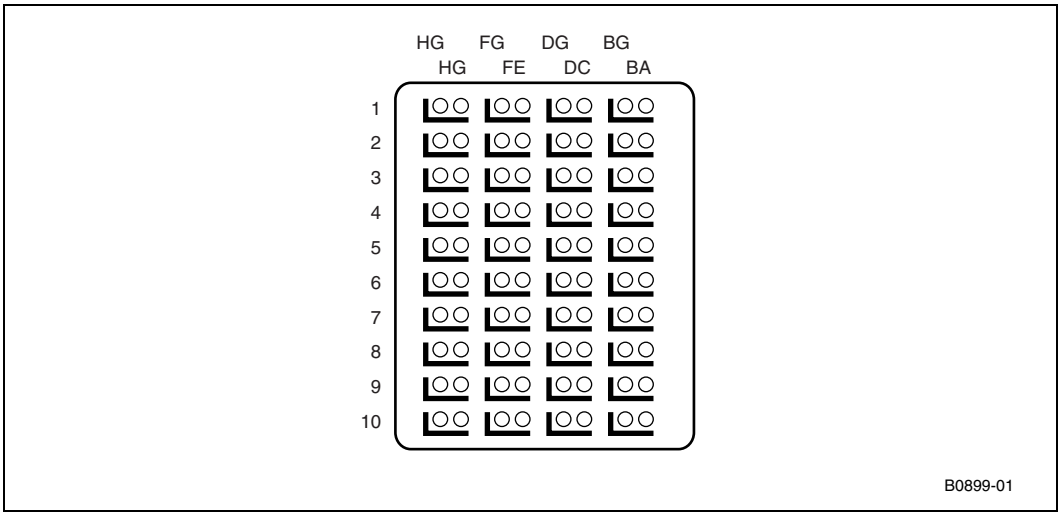
5.1.2 AdvancedTCA Data Transport Connector (J23)

Zone 2 includes one 120-pin HM-ZD connector, labeled J23, with 40 differential pairs. This data transport connector provides the following signals:

- Two 10/100/1000BASE-T/TX Ethernet base channels (four differential signal pairs each, 16 signals total).
- Two 1000BASE-BX Ethernet fabric channels (four differential signal pairs each, eight signals total).

The connector used is AMP*/Tyco* part number 1469001-1. Figure 13 shows a face view of the connector. The pinout of this connector complies with the AdvancedTCA 3.0 specification.

Figure 13. Data Transport Connector (Zone 2) J23



The following naming convention describes the signals on this connector. Signal direction is defined from the perspective of the MPCBL0010 SBC.

P[C]dxp

Where:
P = Prefix (B=Base interface [Gigabit Ethernet], F= Fabric interface [Gigabit Ethernet])
C = Channel (1-2)
d = direction (Tx = Transmit, Rx = Receive)
x = port number (0-1)
p = polarity (+, -)

Note: A port is two differential pairs, one Tx and one Rx.

The BG, DG, FG, and HG (G for Ground) columns contain the ground shields for the four columns of differential pairs. They have been omitted from the pinout tables below for simplification. All pins in the BG, DG, FG, and HG columns are connected to logic ground.

Table 13. AdvancedTCA Data Transport Connector (Zone 2) J23 Pin Assignments

Pin	A	B	C	D	E	F	G	H
1	No Connect	No Connect	No Connect	No Connect	No Connect	No Connect	No Connect	No Connect
2	F[2]Tx0+	F[2]Tx0-	F[2]Rx0+	F[2]Rx0-	F[2]Tx1+	F[2]Tx1-	F[2]Rx1+	F[2]Rx1-
3	No Connect	No Connect	No Connect	No Connect	No Connect	No Connect	No Connect	No Connect
4	F[1]Tx0+	F[1]Tx0-	F[1]Rx0+	F[1]Rx0-	F[1]Tx1+	F[1]Tx1-	F[1]Rx1+	F[1]Rx1-
5	B[1]Tx0+	B[1]Tx0-	B[1]Rx0+	B[1]Rx0-	B[1]Tx1+	B[1]Tx1-	B[1]Rx1+	B[1]Rx1-
6	B[2]Tx0+	B[2]Tx0-	B[2]Rx0+	B[2]Rx0-	B[2]Tx1+	B[2]Tx1-	B[2]Rx1+	B[2]Rx1-
7	No Connect	No Connect	No Connect	No Connect	No Connect	No Connect	No Connect	No Connect
8	No Connect	No Connect	No Connect	No Connect	No Connect	No Connect	No Connect	No Connect
9	No Connect	No Connect	No Connect	No Connect	No Connect	No Connect	No Connect	No Connect
10	No Connect	No Connect	No Connect	No Connect	No Connect	No Connect	No Connect	No Connect

Indicates used extended fabric (Gigabit Ethernet) ports
Indicates used base (Gigabit Ethernet) channels

5.1.3 AdvancedTCA Data Transport Connector (J20)

The MPCBL0010 SBC implementation of the telecom clock uses the J20 connector to connect to the three separate and redundant clock buses on the AdvancedTCA backplane. The Zone 2 J20 connector consists of one 120-pin HM-ZD connector with 40 differential pairs.

Table 14. AdvancedTCA* Data Transport Connector (Zone 2) J20 Pin

Pin	A	B	C	D	E	F	G	H
1	CLK1A+	CLK1A-	CLK1B+	CLK1B-	CLK2A+	CLK2A-	CLK2B+	CLK2B-
2	No Connect	No Connect	No Connect	No Connect	CLK3A+	CLK3A-	CLK3B+	CLK3B-
3	No Connect	No Connect	No Connect	No Connect	No Connect	No Connect	No Connect	No Connect
4	No Connect	No Connect	No Connect	No Connect	No Connect	No Connect	No Connect	No Connect
5	No Connect	No Connect	No Connect	No Connect	No Connect	No Connect	No Connect	No Connect
6	No Connect	No Connect	No Connect	No Connect	No Connect	No Connect	No Connect	No Connect
7	No Connect	No Connect	No Connect	No Connect	No Connect	No Connect	No Connect	No Connect
8	No Connect	No Connect	No Connect	No Connect	No Connect	No Connect	No Connect	No Connect
9	No Connect	No Connect	No Connect	No Connect	No Connect	No Connect	No Connect	No Connect
10	No Connect	No Connect	No Connect	No Connect	No Connect	No Connect	No Connect	No Connect

5.1.4 Alignment Blocks

The MPCBL0010 SBC implements the K1 and K2 alignment blocks at the top of Zone 2 and Zone 3, as required in Section 2.4.4 of the PICMG 3.0 specification. The Zone 2 alignment block is assigned a keying value of 11, and uses a Tyco* 1469373 or a Tyco 1469268 component (or equivalent). The Zone 3 alignment block has a solid face and is used to ensure that rear transition modules (RTMs) with protruding connectors are not plugged into the MPCBL0010 SBC or vice versa; the component used for this is either a Tyco 1469374 or a Tyco 1469275-2 (or equivalent).

5.2 On-Board Connectors

5.2.1 POST Code Connector (J13)

The 8-bit content of I/O address 80h is serialized into a proprietary protocol and the output sent to the J13 connector. In manufacturing, a display board is used to deserialize and display the POST code value on 7-segment LEDs modules.

Table 15. POST Code Connector Pin Assignments

Pin	Signal
1	VCC3
2	Post:Data
3	Post:Clock
4	GND

5.2.2 Extended IPT700 Debug Port Connector (J25)

An Extended ITP700 port connection is included to facilitate debug and BIOS/software development efforts. This JTAG connection to the processors utilizes voltage signaling levels that are specific to the Low Voltage Intel® Xeon™ Processor family. These levels must not be exceeded or processor damage may occur. See the *Debug Port Design Guide* listed in Appendix A, “Reference Documents” for more information.

5.3 Front Panel Connectors

5.3.1 Ethernet 10/100 Debug Connector (J3)

A single Ethernet port interface is provided on the front edge of the card using an RJ-45 style shielded connector (Tyco* RJ714-CL2). This port can be used for debug or management. See Figure 10 for its position on the board.

Note: When using the Ethernet 10/100 Debug Connector, you must use shielded category 5 cabling.

Figure 14. Ethernet 10/100 Debug Connector

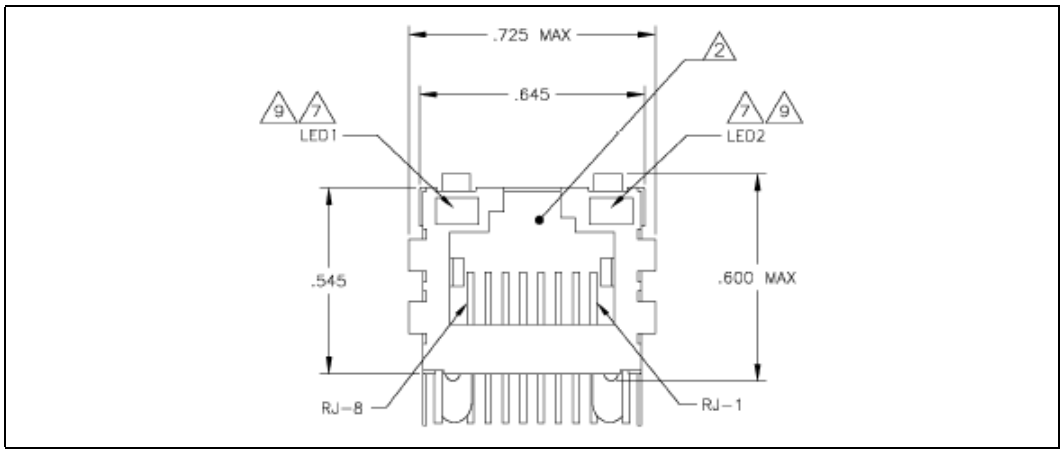


Table 16. Ethernet 10/100 Debug Connector Pin Assignments

Pin	Signal
1	TX+
2	TX-
3	RX+
4	No Connect
5	No Connect
6	RX-
7	No Connect
8	No Connect

Table 17. Ethernet 10/100 Debug Connector LED Operation

LED	Function
LNK	Off: No Link Amber: Link Amber-blink: Link & Activity
SPD	Off: 10Mb/s Green: 100Mb/s

5.3.2 USB Connector (J4)

The MPCBL0010 SBC has one USB connector that supports 2.0 and 1.1 USB. USB connector J4 is available at the front panel. See Figure 10for its position on the board.

Figure 15. USB Connector (J4)

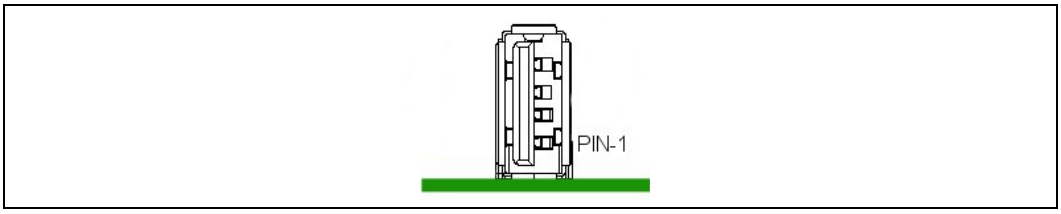


Table 18. USB Connector (J4) Pin Assignments

Pin	Signal
1	+5 V
2	-DATA
3	+DATA
4	GND

5.3.3 Serial Port Connector (J5)

A single serial port interface is provided on the front edge of the card using an RJ-45 style shielded connector. See Figure 10 for its position on the board. This connector is an 8-pin RJ-45.

Figure 16. Serial Port Connector (J5)

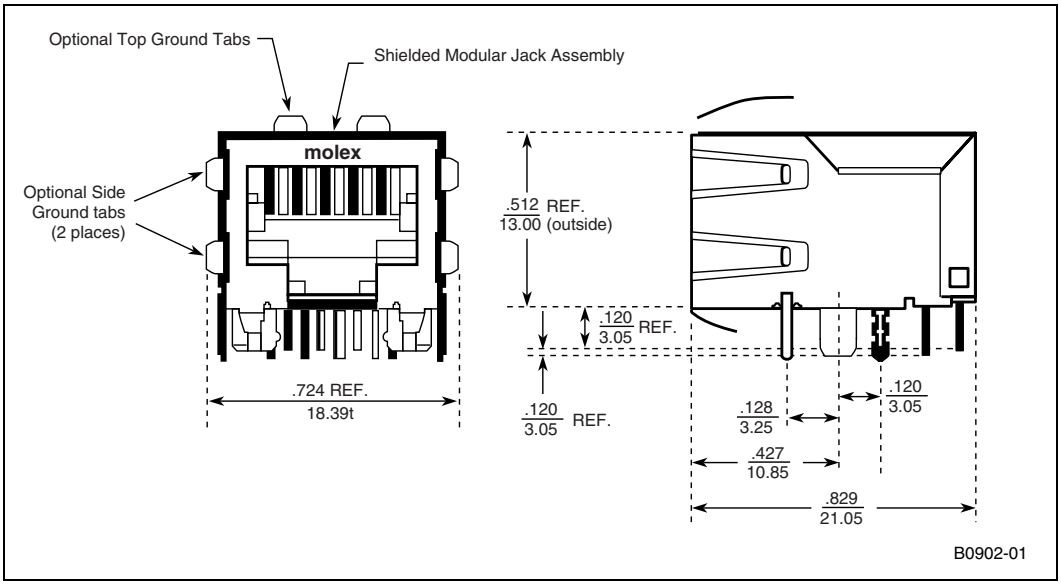
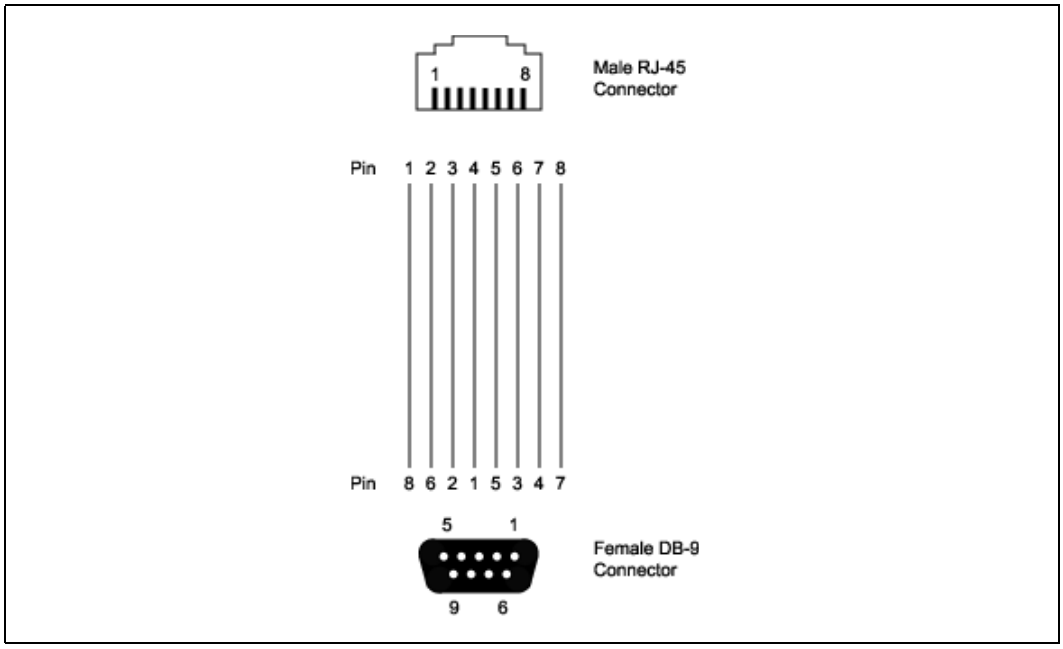


Table 19. Serial Port Connector (J5) Pin Assignments

Pin	Signal
1	RTS
2	DTR
3	TXD
4	GND
5	GND
6	RXD
7	DSR
8	CTS

Figure 17. DB-9 to RJ-45 Pin Translation



5.3.4 AdvancedMC* Connectors (J18, J19)

There is a single AMC B+ connector for each AdvancedMC slot. Connector J18 corresponds to AMC designator B1. Connector J19 corresponds to AMC designator B2. The connectors and pinouts are defined by the industry standard specifications AMC.0 R1.0, AMC.1 R1.0, AMC.2 R1.0, and AMC.3 R1.0. The AdvancedMC slots are available from the front panel. See Figure 10 for their positions on the board.

Note: Do not operate the MPCBL0010 SBC without AdvancedMC module filler panels or AdvancedMC modules installed. The AdvancedMC module slots should not be open or uncovered when the MPCBL0010 SBC is in use in order to meet cooling and radiated emmission requirements.

Table 20 on the following page lists the AdvancedMC connector pin assignments.

Table 20. AdvancedMC* Connector Pin Assignments

Pin	Signal
1	GND
2	PWR1
3	PS1#
4	MP_3V3
5	GA0
6	NC
7	GND
8	NC
9	PWR2
10	GND
11	PORT0_RXP
12	PORT0_RXN
13	GND
14	PORT0_TXP
15	PORT0_TXN
16	GND
17	GA1
18	PWR3
19	GND
20	PORT1_RXP
21	PORT1_RXN
22	GND
23	PORT1_TXP
24	PORT1_TXN
25	GND
26	GA2
27	PWR4
28	GND
29	MB_Rx2+ (SATA)
30	MB_Rx2- (SATA)
31	GND
32	MB_Tx2+ (SATA)
33	MB_Tx2- (SATA)
34	GND
35	NC
36	NC
37	GND
38	NC
39	NC

Pin	Signal
40	GND
41	ENABLE
42	PWR5
43	GND
44	MB_Rx4+
45	MB_Rx4-
46	GND
47	MB_Tx4+
48	MB_Tx4-
49	GND
50	MB_Rx5+
51	MB_Rx5-
52	GND
53	MB_Tx5+
54	MB_Tx5-
55	GND
56	IPMI_CLK
57	PWR6
58	GND
59	MB_Rx6+
60	MB_Rx6-
61	GND
62	MB_Tx6+
63	MB_Tx6-
64	GND
65	MB_Rx7+
66	MB_Rx7-
67	GND
68	MB_Tx7+
69	MB_Tx7-
70	GND
71	IPMI_DATA
72	PWR7
73	GND
74	+CLKA
75	-CLKA
76	GND
77	+CLKB
78	-CLKB
79	GND
80	+CLKC

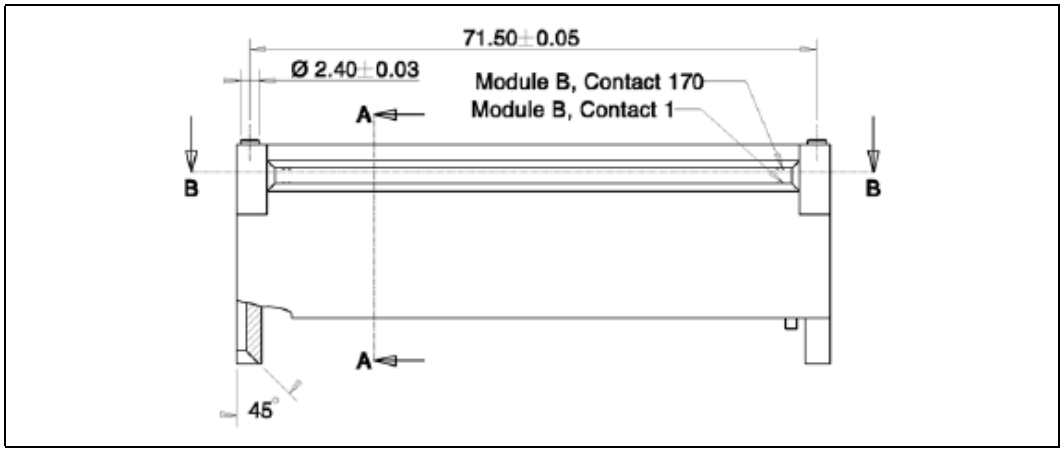
Pin	Signal
81	-CLKC
82	GND
83	GND
84	PWR8
85	GND
86	GND
87	MB_Tx8-
88	MB_Tx8+
89	GND
90	MB_Rx8-
91	MB_Rx8+
92	GND
93	MB_Tx9-
94	MB_Tx9+
95	GND
96	MB_Rx9-
97	MB_Rx9+
98	GND
99	MB_Tx10-
100	MB_Tx10+
101	GND
102	MB_Rx10-
103	MB_Rx10+
104	GND
105	NC
106	NC
107	GND
108	MB_Rx11-
109	MB_Rx11+
110	GND
111	MB_Tx12-
112	MB_Tx12+
113	GND
114	MB_Rx12-
115	MB_Rx12+
116	GND
117	NC
118	NC
119	GND
120	NC
121	NC

Pin	Signal
122	GND
123	NC
124	NC
125	GND
126	NC
127	NC
128	GND
129	NC
130	NC
131	GND
132	NC
133	NC
134	GND
135	NC
136	NC
137	GND
138	NC
139	NC
140	GND
141	NC
142	NC
143	GND
144	NC
145	NC
146	GND
147	NC
148	NC
149	GND
150	NC
151	NC
152	GND
153	NC
154	NC
155	GND
156	NC
157	NC
158	GND
159	NC
160	NC
161	GND
162	NC

Pin	Signal
163	NC
164	GND
165	TCLK
166	TMS
167	RST
168	TDO
169	TDI
170	GND
NC	NC
NC	NC

Note:
NC = No Connection

Figure 18. AdvancedMC* Connector



Caution: Do not ship the MPCBL0010 SBC with third party AdvancedMC modules installed. Damage that occurs to the MPCBL0010 SBC during shipment from AdvancedMC modules installed is not covered by the MPCBL0010 SBC product warranty.

5.4 LEDs

The MPCBL0010 SBC provides several LEDs to indicate status. The LEDs can be driven to display red, green or amber color. There are two different possible MPCBL0010 faceplates as shown in Figure 19 and Figure 20. The LEDs are labeled slightly differenly on each, but the fucntionality is the same on both. The status for each LED when lit is defined in Table 21.

Figure 19. Front Panel LEDs (Option 1)

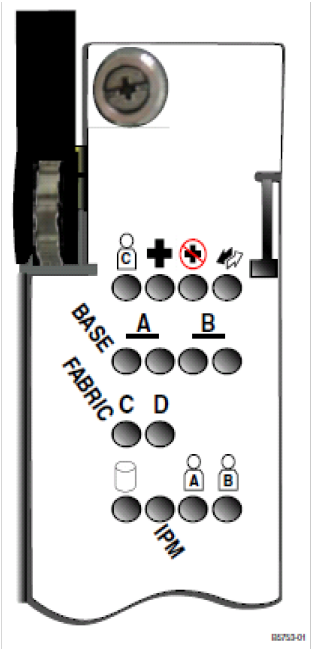


Figure 20. Front Panel B LEDs (Option 2)

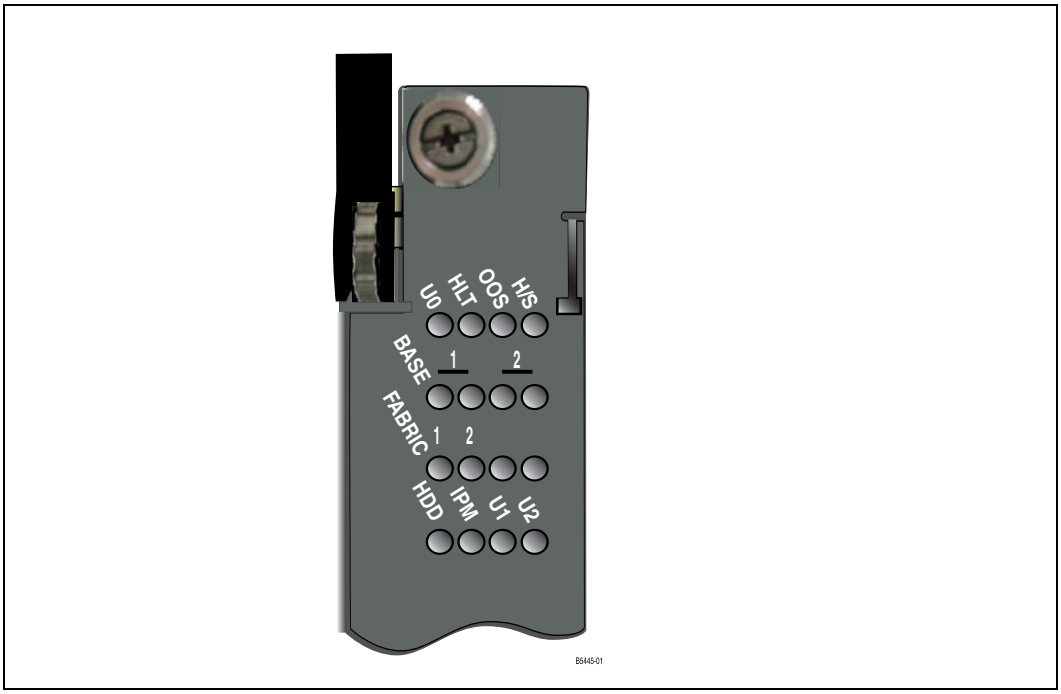


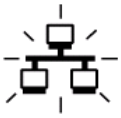
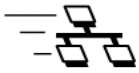
Table 21. Front Panel LED Descriptions (Sheet 1 of 2)

LED	Function
H/S 	Hot Swap (AdvancedTCA-Blue). The LED's default IPMC behavior can be overridden with AdvancedTCA FRU LED Control commands. Off / Blue
OOS 	Out of Service (AdvancedTCA-LED1). Amber: The IPMC is not responding. Amber-blink: The IPMC firmware is being upgraded. Off: The IPMC is running OK. The LED's default IPMC behavior can be overridden with AdvancedTCA FRU LED Control commands. Off / Red / Amber
HLT 	Health (AdvancedTCA-LED2). The SBC health is based on an aggregation of IPMI sensors, like board temperature and voltage. Green - The SBC is healthy. Red - The SBC is not healthy. The LED's default IPMC behavior can be overridden with AdvancedTCA FRU LED Control commands. Off / Green / Red / Amber
U0 	Hearbeat / User Defined 0 (AdvancedTCA-LED3). This LED is user-defined and off by default. The LED's default IPMC behavior can be overridden with AdvancedTCA FRU LED Control commands. Off / Amber
Base 1 GbE Link	Gigabit Ethernet Base Interface 1 Activity and Status. Off: No Link Green: Link Green-blink: Link & Activity
Base 1 GbE Speed	Gigabit Ethernet Base Interface 1 Speed. Off: 10Mb/s Green: 100Mb/s Amber: 1000Mb/s
Base 2 GbE Link	Gigabit Ethernet Base Interface 2 Activity and Status. Off: No Link Green: Link Green-blink: Link & Activity
Base 2 GbE Speed	Gigabit Ethernet Base Interface 2 Speed. Off: 10Mb/s Green: 100Mb/s Amber: 1000Mb/s
Fabric 1 GbE Link	Gigabit Ethernet Fabric Interface 1 Activity and Status. Off: No Link Green: Link Green-blink: Link & Activity
Fabric 2 GbE Link	Gigabit Ethernet Fabric Interface 2 Activity and Status. Off: No Link Green: Link Green-blink: Link & Activity

Table 21. Front Panel LED Descriptions (Sheet 2 of 2)

LED	Function
HDD 	This LED has two functions. The LED will display POST codes in the event the SBC fails to boot. Once the SBC has booted and passed BIOS POST, this LED will indicate hard disk activity. Hard Disk activity Green-blink: Activity POST Codes. Off / Green / Red / Amber See Section , "" on page 55 for more detail.
IPM	IPMC Status. Slow Blink Green: IPMC Heartbeat. Fast Blink Green: There is traffic on the KCS interface of the IPMC. Slow Blink Red: The KCS interface request attention from the SMS or SMM. Fast Blink Red: There is traffic on the IPMB interface of the IPMC. It is not possible to override the behavior of this LED. Off / Green / Red / Amber
U1 	User Defined (AdvancedTCA USER1). By default this LED is off. The LED's default IPMC behavior can be overridden with AdvancedTCA FRU LED Control commands. Off / Green / Red / Amber
U2 	User Defined (AdvancedTCA USER2). By default this LED is off. The LED's default IPMC behavior can be overridden with AdvancedTCA FRU LED Control commands. Off / Green / Red / Amber

Table 22. Ethernet 10/100 Debug Connector LED Operation

LED	Function
LNK 	Off: No Link Amber: Link Amber-blink: Link & Activity
SPD 	Off: 10Mb/s Green: 100Mb/s

5.4.1 POST LED Codes

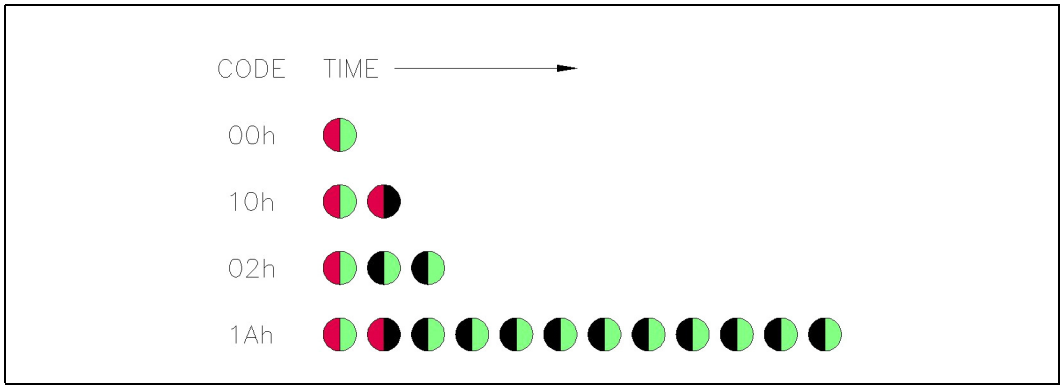
The HDD LED uses a blinking sequence to display the current POST (Power On Self Test) code value. If the boot process succeeds, the POST code is irrelevant and the BIOS will change the state of the HDD LED to display hard disk activity just before the

operating system launches. If the boot sequence fails or the CPU hangs, the HDD (POST) LED will remain operational in POST code mode and repeat indefinitely the last POST code blink sequence as defined below:

1. Blink simultaneously amber and green one time: start of the sequence.
2. Blink amber 0-15 times while green stays off.
3. Blink green 0-15 times while amber stays off.
4. Repeat the sequence (see step 1).

Amber (A) is the first or most significant digit of the POST code value in hexadecimal, while green (G) is the second digit (i.e., POST code value is AGh). Some examples are shown in Figure 21.

Figure 21. Example POST LED Codes



Note: See Section 8.2, "Port 80h POST Codes" for explanations of the codes.

5.5 Reset Button

The Reset button is located in a small recessed hole near the serial port connector on the front panel. The Reset button is an input to the IPMC to request a cold reset. There are IPMI commands to reset the board and change power states through the software.

The Reset button is a last resort because someone must be physically present at the chassis to reset the board. The Reset button location on the front panel is shown in Figure 11.

6.0 BIOS Features

6.1 Introduction

The MPCBL0010 SBC uses an Intel/AMI* BIOS, which is stored in flash memory and updated using a disk-based program. In addition to the BIOS and BIOS setup program, the flash memory contains POST and Plug and Play support.

The BIOS displays a message during POST identifying the type of BIOS and a revision code. Refer to the *Specification Update* on the Documentation tab of the MPCBL0010 SBC web site at http://www.intel.com/design/telecom/products/cbp/atca/9445/overview.htm for the latest default settings.

6.2 BIOS Flash Memory Organization

The MPCBL0010 SBC contains two firmware hub (FWH) devices . (See Figure 1) The first is the Primary FWH, which holds the BIOS code that executes during POST. The second is the Backup FWH, which recovers the system when the Primary FWH is corrupted. The N82802AC FWH includes an 8 Mbit (1024 KByte) symmetrical flash memory device. Internally, the device is grouped into sixteen 64-KByte blocks that are individually erasable, lockable, and unlockable.

6.3 Complementary Metal-Oxide Semiconductor (CMOS)

CMOS RAM is a nonvolatile storage that stores data needed by the BIOS. The data consists of certain onboard configurable settings, including time and date. CMOS resides in the 6300ESB ICH and is powered by the Supercap when the blade is power off. The settings in the BIOS setup menu are stored in the CMOS RAM and are often called CMOS settings.

6.4 Redundant BIOS Functionality

MPCBL0010 SBC hardware has two flash banks for BIOS where redundant copies are stored. BIOS bank selection logic is connected to the IPMC, and the IPMC firmware allows selection of the BIOS bank.

By default, firmware selects BIOS bank 0. BIOS executes code off this flash and performs checksum validation of its operational code. This checksum occurs in the boot block of the BIOS. If the boot block detects a checksum failure in the remainder of the BIOS, it notifies the IPMC of the failure.

In case of failure, the IPMC firmware:

1. Asserts the RESET pin on the processor
2. Switches the flash bank
3. De-asserts the RESET pin on the processor, allowing BIOS to execute off the second flash bank

An application running on a non-Plug and Play operating system can obtain the SMBIOS information.

6.5 Legacy USB Support

Legacy USB support enables USB devices such as keyboards, mice, and hubs to be used even when the operating system's USB drivers are not yet available. Legacy USB support is used to access the BIOS Setup program and install an operating system that supports USB. Legacy USB support is set to **Enabled** by default.

Note: Legacy USB support is for keyboards, mice and hubs only. Other USB devices are not supported in legacy mode except bootable devices like CD-ROM drives and floppy disk drives.

Legacy USB support operates as follows:

1. When you apply power to the computer, legacy support is disabled.
2. POST begins.
3. Legacy USB support is enabled by the BIOS, allowing you to use a USB keyboard.
4. POST completes.
5. The operating system loads. USB keyboards and mice are recognized and may be used to configure the operating system. Keyboards and mice are not recognized during this period if Legacy USB support was set to **Disabled** in the BIOS Setup program.
6. After the operating system loads the USB drivers, all legacy and non-legacy USB devices are recognized by the operating system. Legacy USB support from the BIOS is no longer used.

To install an operating system that supports USB, verify that Legacy USB support in the BIOS Setup program is set to **Enabled** and follow the operating system's installation instructions.

6.5.1 Language Support

English is the only supported language.

6.6 Recovering BIOS Data

Some types of failure can destroy the BIOS. For example, the data can be lost if a power outage occurs while the BIOS is being updated in flash memory. The BIOS can be recovered from the backup BIOS FWH. Recovery mode is active when BIOS checksum fails and notifies the IPMC to failover to the backup BIOS automatically.

6.7 Boot Options

In the BIOS Setup program, the user can choose to boot from available boot devices, with each boot device having options for removable media, CD-ROM, AdvancedMC* hard drive, or by a network boot through any of the four Gigabit Ethernet (GbE) adapters. In every POST, the BIOS detects all available boot devices, then displays them on the boot order screen, with the exception of the IBA, which displays even if the LAN cable is not connected.

The default settings are:

- 1st Boot Device: removable media
- 2nd Boot Device: CD-ROM
- 3rd Boot Device: hard drive
- 4th Boot Device: IBA2 - Intel® Boot Agent (IBA) 0309

- 5th Boot Device: IBA1 - Intel® Boot Agent (IBA) 0308
- 6th Boot Device: IBA2 - Intel® Boot Agent (IBA) 0311
- 7th Boot Device: IBA2 - Intel® Boot Agent (IBA) 0310

Note: Additional boot devices may appear in the above list if there are other bootable devices connected to the board (for example, USB devices or AdvancedMC devices).

6.7.1 CD-ROM and Network Boot

Booting from CD-ROM is supported in compliance with the "El Torito" bootable CD-ROM format specification. Under the Boot menu in the BIOS setup program, USB CD-ROM is listed as a boot device (removable media). Boot devices are defined in priority order.

Accordingly, if there is not a bootable CD in the CD-ROM drive, the system attempts to boot from the next defined drive.

The network can be selected as a boot device. This Intel® Boot Agent (IBA) selection allows booting from the onboard LANs if connected to a network.

6.7.2 Booting without Attached Devices

For use in embedded applications, the BIOS has been designed so that after passing the POST, the operating system loader is invoked even if a video adapter (via AdvancedMC), keyboard, or mouse are not present:

6.8 Fast Booting Systems

6.8.1 Quick Boot

Use of the following BIOS setup program settings reduces the POST execution time.

In the Boot Menu:

- Disable Option - ROM(s) if customer configuration does not use IBA(PXE) boot
- Enable Quick Boot - bypasses memory count and the search for a removable drive

Note: Quick Boot is enabled by default. The boot time may be so fast that some drives might not be initialized at all. If this occurs, it is possible to introduce a programmable delay ranging from 0 to 35 seconds using the BIOS setup program, IDE Configuration Submenu, Advanced Menu, IDE Detect Time Out feature.

6.9 BIOS Security Features

The BIOS includes security features that restrict access to the BIOS Setup program and booting the computer. A supervisor password and a user password can be set for the BIOS setup program and for booting the computer, with the following restrictions:

- The supervisor password gives unrestricted access to view and change all the setup options in the BIOS setup program. This is the supervisor mode.
- The user password gives restricted access to view and change setup options in the BIOS setup program. This is the user mode.
- If only the supervisor password is set, pressing the **Enter** key at the password prompt of the BIOS setup program allows the user restricted access to setup.

- If both the supervisor and user passwords are set, users can enter either the supervisor password or the user password to access setup. Access to setup corresponds to which password is entered.
- Setting the user password restricts who can boot the computer. The password prompt is displayed before the computer is booted. If only the supervisor password is set, the computer boots without asking for a password. If both passwords are set, the user can enter either password to boot the computer.

Table 23 shows the effects of setting the supervisor password and user password. This table is for reference only and is not displayed on the screen.

Table 23. Supervisor and User Password Functions

Password Set	Supervisor Mode	User Mode	Password to Enter Setup	Password During Boot
None	Any user can change all options	Any user can change all options	None	None
Supervisor and user	Can change all options	Based on user access level: No Access, View Only, Limited, Full Access	Supervisor or user	If password check option is set to Setup then no password required. Otherwise requires either supervisor or user password.
Supervisor only	Can change all options	Based on user access level: No Access, View Only, Limited, Full Access.	Supervisor (for supervisor mode) or enter only (for user mode)	If password check option is set to Setup then no password required. Otherwise requires either supervisor password or enter only.
User only	Can't get into supervisor mode until user password is cleared.	Can change all options	User	If password check option is set to Setup then no password required. Otherwise requires user password.

6.10 Remote Access Configuration

Remote access using serial console redirection allows users to monitor the MPCBL0010 SBC boot process and run the MPCBL0010 SBC BIOS setup from a remote serial terminal. Connection is made directly through a serial port.

The console redirection feature is useful in cases where it is necessary to communicate with a processor board in an embedded application without video support.

Note: The default settings used for console redirection to the serial port are 115,200, n, 8, 1, and no flow control.

Table 24 shows the escape code sequences that may be useful for things like BIOS setup if function keys cannot be sent directly from a terminal application:

Table 24. Function Key Escape Code Equivalents (Sheet 1 of 2)

Key	Escape Sequence	Note
F1	ESC OP	
F2	ESC OQ	
F3	ESC OR	
F4	ESC OS	To enter BIOS Setup
F5	ESC OT	
F6	ESC OU	
F7	ESC OV	

Table 24. Function Key Escape Code Equivalents (Sheet 2 of 2)

Key	Escape Sequence	Note
F8	ESC OW	
F9	ESC OX	
F10	ESC OY	To save and exit Setup
F11	ESC OZ	
F12	ESC OI	PXE boot

7.0 BIOS Setup

7.1 Introduction

The MPCBL0010 SBC BIOS is based on AMIBIOS8*. The BIOS Setup program can be used to view and change the BIOS settings for the SBC. The BIOS Setup program is accessed by pressing the <**DEL**> key (or **F4** on a remote keyboard) after the Power-On Self-Test (POST) begins and before the operating system boot begins. Table 25 lists the BIOS Setup program menu features.

Table 25. BIOS Setup Program Menu Bar

Main	Advanced	PCIPnP	Boot	Security	Chipset	Exit
Allocates resources for hardware components.	Configures advanced features available through the chipset.	Configures PCI Plug and Play features.	Selects boot options and power supply controls.	Sets passwords and security features.	Configures MCH and ICH features.	Saves or discards changes to Setup program options.

Table 26 lists the function keys available for menu screens.

Table 26. BIOS Setup Program Function Keys

BIOS Setup Program Function Key	Description
<←> or <→>	Selects a different menu screen (moves the cursor left or right).
<↑ > or <↓>	Selects an item (moves the cursor up or down).
<Tab>	Selects a field (not implemented).
<Enter>	Executes command or selects the sub-menu.
<F10>	Saves the current values and exits the BIOS Setup program.
<Esc>	Exits the menu.

7.2 Main Menu

To access this menu, select **Main** on the menu bar at the top of the screen.

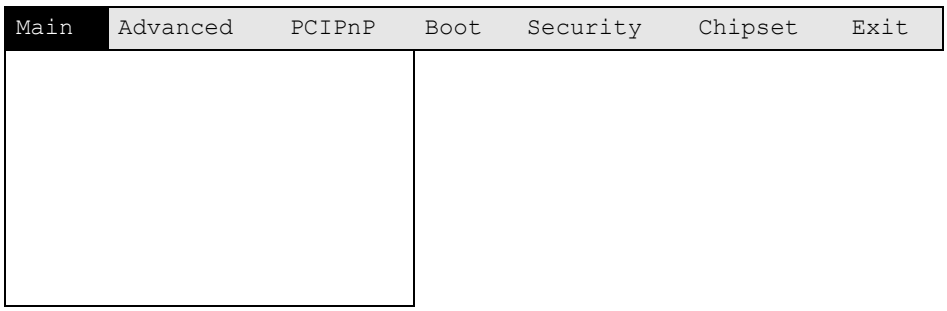


Table 27 describes the Main menu. This menu reports processor and memory information and is used for configuring the system date and system time.

Table 27. Main Menu

Feature	Options	Description
BIOS ID	Version Build Date ID	Displays the BIOS version, build date, and ID.
PLD Information	FPGA Version	Programmable Logic Device Version Information.
Processor	Type Speed Count	Reports processor type, speed, and count.
System Memory Size	Size	Displays installed memory size.
System Time	Hour/minute/second	Specifies the current time.
System Date	Day of week Month/day/year	Specifies the current date.

7.3 Advanced Menu

To access this menu, select **Advanced** on the menu bar at the top of the screen.

Main	Advanced	PCIPnP	Boot	Security	Chipset	Exit

CPU Configuration
IDE Configuration
SuperIO Configuration
ACPI Configuration
System Management
Event Log Configuration
MPS Configuration
ATCA Channel Routing (PICMG)
On-board Devices Configuration
PCI Express Configuration
Remote Access Configuration
IPMI Configuration
USB Configuration

Warning: Setting the wrong values in the sections that follow may cause the system to malfunction.

Do not modify the settings unless you are familiar with the items. To restore factory defaults, go to "`Exit > Load Optimal Defaults`".

Table 28 describes the Advanced menu. This menu sets advanced features that are available through the chipset.

Table 28. Advanced Menu

Feature	Options	Description
CPU Configuration	Select to display sub-menu	Display CPU details, Enable/Disable Hyper-Threading** technology.
IDE Configuration	Select to display sub-menu	Display the primary IDE master and primary IDE slave drive.
SuperIO Configuration	Select to display sub-menu	Set parallel port address/interrupt.
ACPI Configuration	Select to display sub-menu	Enable/Disable ACPI support for OS, Enable/Disable additional ACPI 2.0 tables.
System Management	Select to display sub-menu	Displays FRU, board, product, IPMI device, and firmware information.
Event Log Configuration	Select to display sub-menu	Enable/Disable error logging.
MPS Configuration	Select to display sub-menu	Configure Multi-Processor Table.
ATCA Channel Routing (PICMG)	Select to display sub-menu	Select either the on-board GbE Fabric port, or the AdvancedMC port for routing to AdvancedTCA backplane.
On-Board Device Configuration	Select to display sub-menu	Enable / Disable On-board devices.
PCI Express Configuration	Select to display sub-menu	Configure PCI Express support.
Remote Access Configuration	Select to display sub-menu	Enable/Disable remote access.
IPMI Configuration	Select to display sub-menu	IPMI configuration including server monitoring and event log.
USB Configuration	Select to display sub-menu	Enable/Disable USB devices.

7.3.1 CPU Configuration Sub-Menu

To access this sub-menu, select **Advanced** on the menu bar, then **CPU Configuration**.

Main	Advanced	PCIPnP	Boot	Security	Chipset	Exit

CPU Configuration
IDE Configuration
SuperIO Configuration
ACPI Configuration
System Management
Event Log Configuration
MPS Configuration
ATCA Channel Routing (PICMG)
On-board Devices Configuration
PCI Express Configuration

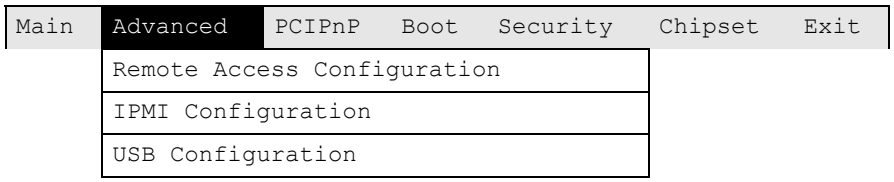


Table 29 shows the sub-menu options for configuring the CPU.

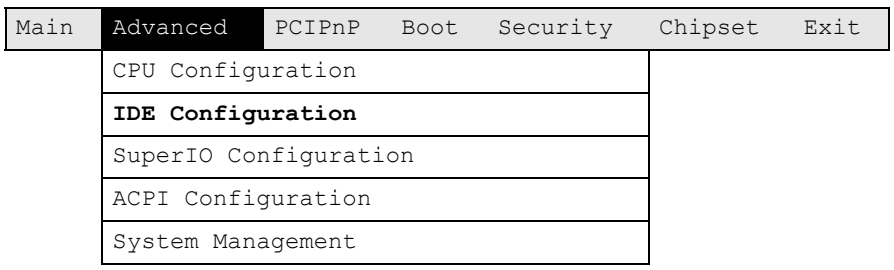
Table 29. CPU Configuration Sub-Menu

Feature	Options	Description
Manufacturer		Display CPU Manufacturer.
Brand String		Display CPU Brand String.
Frequency		Display CPU Frequency.
FSB Speed		Displays Front Side Bus Speed.
Cache L1		Displays L1 Cache size.
Cache L2		Displays L2 Cache size.
Ratio Status		Displays Ratio Status (14=2.8 Ghz).
Ratio Actual Value		Displays Ratio Value.
Max CPUIP Value Limit	**Disabled** Enabled	This should be enabled to boot legacy operating systems that do not support extended CPUID functions.
Thermal Monitor	Disabled **TM1**	CPU Thermal Monitor. Modulates clock to compensate for high temperature condition. ***Note:*** Failures that occur due to Thermal Monitor Disabled may void warranty.
Execute Disable Bit	Disabled **Enabled**	When disabled, force XD feature flag to return 0.
Hardware Prefetcher	Disabled **Enabled**	Enable/Disable Hardware Prefetcher.
Adjacent Cache Line Prefetcher	Disabled **Enabled**	Enable/Disable Adjacent Cache Line Prefetcher.
Hyper-Threading Technology	Disabled **Enabled**	Enable/Disable Hyper-Threading.

Note: **Bold** text indicates default setting.

7.3.2 IDE Configuration Sub-Menu

To access this sub-menu, select **Advanced** on the menu bar, then **IDE Configuration**.



Main	Advanced	PCIPnP	Boot	Security	Chipset	Exit

Event Log Configuration
MPS Configuration
ATCA Channel Routing (PICMG)
On-board Devices Configuration
PCI Express Configuration
Remote Access Configuration
IPMI Configuration
USB Configuration

Table 30 shows the IDE configuration options.

Table 30. IDE Configuration Sub-Menu

Feature	Options	Description
IDE Configuration	Disabled **P-ATA Only** S-ATA Only P-ATA & S-ATA	Selects IDE mode.
S-ATA Running Enhanced Mode	**Yes** No	Sets S-ATA Running Enhanced Mode.
P-ATA Channel Selection	Primary Secondary **Both**	Selects P-ATA Channel.
S-ATA Ports Definition	**P0-3rd./P1-4th** P0-4th./P1-3rd	Selects S-ATA Ports.
Primary IDE Master		Display the primary IDE master drive.While entering setup, BIOS auto detects the presence of IDE devices. This displays the status of the auto detection of IDE devices.
Primary IDE Slave		Display the primary IDE slave drive.While entering setup, BIOS auto detects the presence of IDE devices. This displays the status of the auto detection of IDE devices.
Secondary IDE Master		Display the primary IDE master drive.While entering setup, BIOS auto detects the presence of IDE devices. This displays the status of the auto detection of IDE devices.
Secondary IDE Slave		Display the primary IDE master drive.While entering setup, BIOS auto detects the presence of IDE devices. This displays the status of the auto detection of IDE devices.
Third IDE Master		Display the primary IDE master drive.While entering setup, BIOS auto detects the presence of IDE devices. This displays the status of the auto detection of IDE devices.
Fourth IDE Master		Display the primary IDE master drive.While entering setup, BIOS auto detects the presence of IDE devices. This displays the status of the auto detection of IDE devices.

Table 30. IDE Configuration Sub-Menu (Continued)

Feature	Options	Description
Hard Disk Write Protect	**Disabled** Enabled	Enable/Disable Hard Disk device write protection. This is effective only if the device is accessed through BIOS.
IDE Detect Time Out	0 5 10 15 20 25 30 **35**	Select the time out value for detecting ATA/ATAPI device(s).

Note: **Bold** text indicates default setting.

7.3.2.1 Primary IDE Master/Slave Configuration Options

Table 31 shows the IDE Master/Slave configuration options.

Table 31. IDE Master/Slave Sub-Menu

Feature	Options	Description
Device		Display IDE device.
Vendor		Display IDE vendor name.
Size		Display IDE device size.
LBA Mode		Display IDE LBA Mode status.
Block Mode		Display IDE Block Mode status.
PIO Mode		Display PIO Mode status.
Async DMA		Display Async DMA status.
Ultra DMA		Display Ultra DMA-5 status.
S.M.A.R.T		Display S.M.A.R.T status.
Type	Not installed **Auto** CDROM ARMD	Select the type of IDE device connected.
LBA/Large Mode	Disabled **Auto**	Disable: Disable LBA ModeAuto: Enable the LBA Mode if the device supports it and the devices is not already formatted with LBA Mode disable.
Block (Multi-Sector Transfer)	Disabled **Auto**	Disable: The data transfer from and to the device occurs one sector at a time. Auto: The data transfer from and to the device occurs multiple sectors at a time if the device supports it.
PIO Mode	**Auto** 0/1/2/3/4	Select PIO Mode.

Table 31. IDE Master/Slave Sub-Menu (Continued)

Feature	Options	Description
DMA Mode	**Auto** SWDMA0 SWDMA1 SWDMA2 MWDMA0 MWDMA1 MWDMA2 UDMA0 UDMA1 UDMA2 UDMA3 UDMA4	Select DMA Mode: Auto: Auto detected SWDMAn: SingleWordDMAn MWDMAn: MultiWordDMAn UDMAn: UltraDMAn
32 Data Transfer	Disabled **Enabled**	Enable/Disable 32-bit Data Transfer.

Note: **Bold** text indicates default setting.

7.3.3 SuperIO Configuration Sub-Menu

To access this sub-menu, select **Advanced** on the menu bar, then **SuperIO Configuration**.

Main	Advanced	PCIPnP	Boot	Security	Chipset	Exit

CPU Configuration
IDE Configuration
SuperIO Configuration
ACPI Configuration
System Management
Event Log Configuration
MPS Configuration
ATCA Channel Routing (PICMG)
On-board Devices Configuration
PCI Express Configuration
Remote Access Configuration
IPMI Configuration
USB Configuration

Table 32 shows SuperIO configuration options.

Table 32. SuperIO Configuration Sub-Menu

Feature	Options	Description
ICH Serial Port1 Address	Disabled **3F8/IRQ4** 2F8/IRQ3 3E8/IRQ4 2E8/IRQ3	Set serial port 1 address and interrupt.
ICH Serial Port2 Address	Disabled 3F8/IRQ4 **2F8/IRQ3** 3E8/IRQ4 2E8/IRQ3	Set serial port 2 address and interrupt.
PLD POD Devicer	**Disabled** Enabled	Enable to use on-board LPT port to program PLD with POD device.
Parallel Port Address	Disabled **378** 278 3BC	Select Parallel Port Address
Parallel Port Mode	**Normal** Bi-Directional ECP EPP ECP & EPP	Set the parallel port mode.
Parallel Port IRQ	IRQ5 **IRQ7**	Set parallel port interrupt.

Note: **Bold** text indicates default setting.

7.3.4 ACPI Configuration Sub-Menu

To access this sub-menu, select **Advanced** on the menu bar, then **ACPI Configuration**.

Main	Advanced	PCIPnP	Boot	Security	Chipset	Exit

CPU Configuration
IDE Configuration
SuperIO Configuration
ACPI Configuration
System Management
Event Log Configuration
MPS Configuration
ATCA Channel Routing (PICMG)
On-board Devices Configuration
PCI Express Configuration

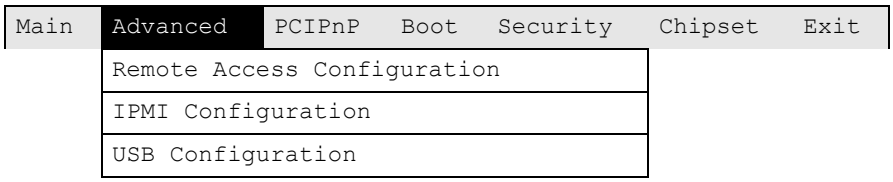


Table 33 shows ACPI configuration options.

Table 33. ACPI Configuration Sub-Menu

Feature	Options	Description
Advanced ACPI Configuration		Configure advanced ACPI options.
Chipset ACPI Configuration		Configure ACPI chipset options.

7.3.4.1 Advanced ACPI Configuration Sub-Menu

To access this sub-menu, select **Advanced** on the menu bar, select **ACPI Configuration**, then **Advanced ACPI Configuration**.

Table 34 shows Advanced ACPI configuration options.

Table 34. Advanced ACPI Configuration Sub-Menu

Feature	Options	Description
ACPI 2.0 Support	**No** Yes	Enable RSDP pointers to 64-bit fixed system description tables.
ACPI APIC support	Disabled **Enabled**	Include ACPI APIC table pointer to RSDT pointer list.
AMI OEMB table	Disabled **Enabled**	Include OEMB table to R(X)SDT pointer lists.
Headless Mode	**Disabled** Enabled	Enable/Disable Headless operation mode through ACPI.

Note: **Bold** text indicates default setting.

7.3.4.2 Chipset ACPI Configuration Sub-Menu

To access this sub-menu, select **Advanced** on the menu bar, select **ACPI Configuration**, then **Chipset ACPI Configuration**.

Table 35 shows ACPI configuration options.

Table 35. Chipset ACPI Configuration Sub-Menu

Feature	Options	Description
APIC ACPI SCI IRQ	**Disabled** Enabled	Enable/Disable APIC ACPI SCI interrupt.

Note: **Bold** text indicates default setting.

7.3.5 System Management Sub-Menu

To access this sub-menu, select **Advanced** on the menu bar, then **System Management**.

Main	Advanced	PCIPnP	Boot	Security	Chipset	Exit

CPU Configuration
IDE Configuration
SuperIO Configuration
ACPI Configuration
System Management
Event Log Configuration
MPS Configuration
ATCA Channel Routing (PICMG)
On-board Devices Configuration
PCI Express Configuration
Remote Access Configuration
IPMI Configuration
USB Configuration

Table 36 shows the System Management information.

Table 36. System Management Sub-Menu

Feature	Options	Description
Board Product Name		Displays Board Product Name.
Board Serial Number		Displays Board Serial Number.
Board Part Number		Displays Board Part Number.
Product Name		Displays Product Name.
Product Part/Model		Displays Product Part/Model.
Product Version Number		Displays Product Version Number.
Product Serial Number		Displays Product Serial Number.
IPMI Version		Displays IPMI Version.
Device ID		Displays Device ID.
Device Revision		Displays Device Revision.
Firmware Revision		Displays Firmware Revision.
SDR Revision		Displays Sensor Data Record Revision.
FWUM Firmware Version		Displays Firmware Update Manager Version.

7.3.6 Event Log Configuration Sub-Menu

To access this sub-menu, select **Advanced** on the menu bar, then **Event Log Configuration**.

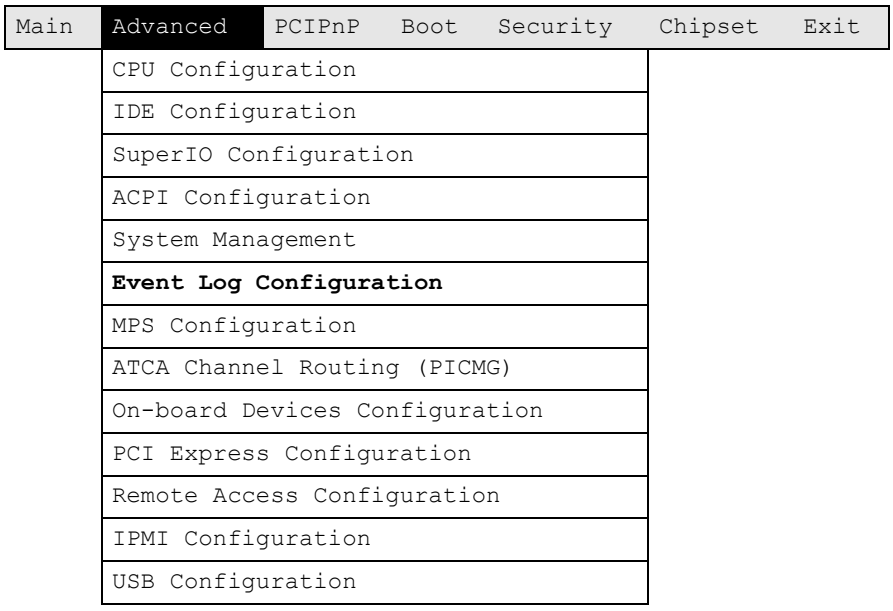


Table 37 shows event log configuration options.

Table 37. Event Log Configuration Sub-Menu

Feature	Options	Description
View Event Log		View all unread events.
Mark all events as read		Option to Mark all events as read.
Clear Event Log		Discard all events in the log.
ECC Event Logging	Disabled **Enabled**	Enable/Disable fatal error event logging.
Hub Interface Event Logging	Disabled **Enabled**	Enable/Disable Hub Interface error logging.
System Bus Event Logging	Disabled **Enabled**	Enable/Disable System Bus error logging.
Memory Buffer Event Logging	Disabled **Enabled**	Enable/Disable Memory Buffer error logging.
PCI Error Logging	Disabled **Enabled**	Enable/Disable PCI error events.
PCI Express Error Logging	Disabled **Enabled**	Enable/Disable PCI Express error events.
PCI Express Error Masking		Selects sub-menu
Machine-Check Exception Action	**Restart Execution** Reboot System	Specifies what the machine-check exception handler should do when program execution cannot be restarted reliably.

Note: **Bold** text indicates default setting.

Note: The event log reports both correctable memory errors (single bit) and uncorrectable memory errors (double-bit or multi-bit). However, some double-bit errors are correctable and some are not. If a double-bit error occurs that is correctable, it will be logged as a correctable error (single bit).

7.3.6.1 PCI Express Error Masking Configuration Sub-Menu

To access this sub-menu, select **Advanced** on the menu bar, select **Event Log Configuration**, then **PCI Express Error Masking**.

Table 38 shows PCI Express Error Masking options.

Table 38. PCI Express Error Masking Configuration Sub-Menu

Feature	Options	Description
Mask Duplicate Errors	No **Yes**	Mask same errors if they are found in successive SMI interrupts.
Mask Unsupported Request	No **Yes**	Unsupported Request Errors can be masked when set to ‘yes’. If set to ‘no’, the default mask used is based on chipset recommendations.

Note: **Bold** text indicates default setting.

7.3.7 MPS Configuration Sub-Menu

To access this sub-menu, select **Advanced** on the menu bar, then **MPS Configuration**.

Main	Advanced	PCIPnP	Boot	Security	Chipset	Exit

CPU Configuration
IDE Configuration
SuperIO Configuration
ACPI Configuration
System Management
Event Log Configuration
MPS Configuration
ATCA Channel Routing (PICMG)
On-board Devices Configuration
PCI Express Configuration
Remote Access Configuration
IPMI Configuration
USB Configuration

Table 39 shows MPS Configuration options.

Table 39. MPS Configuration Sub-Menu

Feature	Options	Description
MPS Revision	1.1 **1.4**	Configures the Multiprocessor Specification revision level. Some operating systems will require 1.1 for compatibility reasons.

Note: **Bold** text indicates default setting.

7.3.8 AdvancedTCA* Channel Routing (PICMG*) Sub-Menu

To access this sub-menu, select **Advanced** on the menu bar, then **AdvancedTCA Channel Routing** (PCMIG).

Main	Advanced	PCIPnP	Boot	Security	Chipset	Exit

CPU Configuration
IDE Configuration
SuperIO Configuration
ACPI Configuration
System Management
Event Log Configuration

MPS Configuration
ATCA Channel Routing (PICMG)
On-board Devices Configuration
PCI Express Configuration
Remote Access Configuration
IPMI Configuration
USB Configuration

Table 40 shows MPS Configuration options.

Table 40. AdvancedTCA Channel Routing (PICMG) Sub-Menu

Feature	Options	Description
Actual LAN A Port State		Displays port state based on E-key granting from the AdvancedTCA shelf manager.
Fabric LAN A Port Setting	Disabled **Fabric Ch1 Port 0**	Select built-in GbE LAN port A to go to AdvancedTCA backplane Fabric Channel 1, Port 0.
Actual LAN B Port State		Displays port state based on E-key granting from the AdvancedTCA shelf manager.
Fabric LAN B Port Setting	Disabled **Fabric Ch2 Port 0**	Select built-in GbE LAN port B to go to AdvancedTCA backplane Fabric Channel 2, Port 0.
Actual AdvancedMC B1 Port 0 State		Displays port state based on E-key granting from the AdvancedTCA shelf manager.
AdvancedMC B1 Port 0 Setting	**Disabled** Fabric Ch1 Port 1	Select AdvancedMC B1 GbE LAN port 0 to go to AdvancedTCA backplane Fabric Channel 1, Port 1.
Actual AdvancedMC B1 Port 1 State		Displays port state based on E-key granting from the AdvancedTCA shelf manager.
AdvancedMC B1 Port 1 Setting	**Disabled** Fabric Ch2 Port 1	Select AdvancedMC B1 GbE LAN port 1 to go to AdvancedTCA backplane Fabric Channel 2, Port 1.
Actual AMC B2 Port 0 State		Displays port state based on E-key granting from the AdvancedTCA shelf manager.
AMC B2 Port 0 Setting	**Disabled** Fabric Ch1 Port 0	Select AdvancedMC B2 GbE LAN port 0 to go to AdvancedTCA backplane Fabric Channel 1, Port 0.
Actual AMC B2 Port 1 State		Displays port state based on E-key granting from the AdvancedTCA shelf manager.
AMC B2 Port 1 Setting	**Disabled** Fabric Ch2 Port 0	Select AdvancedMC B2 GbE LAN port 1 to go to AdvancedTCA backplane Fabric Channel 2, Port 0.

Note: **Bold** text indicates default setting.
Note: To enable ports to the AdvancedTCA backplane, you need E-key granting from the AdvancedTCA shelf manager. If the shelf manager rejects the request, the ports will not be enabled even though the BIOS has configured them.

7.3.9 On-board Devices Configuration Sub-Menu

To access this sub-menu, select **Advanced** on the menu bar, then **On-board Devices Configuration**.

Main	Advanced	PCIPnP	Boot	Security	Chipset	Exit

CPU Configuration
IDE Configuration
SuperIO Configuration
ACPI Configuration
System Management
Event Log Configuration
MPS Configuration
ATCA Channel Routing (PICMG)
On-board Devices Configuration
PCI Express Configuration
Remote Access Configuration
IPMI Configuration
USB Configuration

Table 41 shows On-board Devices Configuration options.

Table 41. On-board Devices Configuration Sub-Menu

Feature	Options	Description
On-board Dual-Ethernet 1		Select Dual-Ethernet 1 for configuration (Base).
On-board Dual-Ethernet 2		Select Dual-Ethernet 2 for configuration (Fabric).

Note: **Bold** text indicates default settings.

Table 42. Option ROM Configuration Options

Feature	Options	Description
On-board Dual-Ethernet 1 Option ROM Function A	Disabled **Enabled**	Enable/Disable ROM option for IBA GE Slot 0308 AdvancedTCA Base Channel 1.
On-board Dual-Ethernet 1 Option ROM Function B	Disabled **Enabled**	Enable/Disable ROM option for IBA GE Slot 0309 AdvancedTCA Base Channel 2.
On-board Dual-Ethernet 2 Option ROM Function A	Disabled **Enabled**	Enable/Disable ROM option for IBA GE Slot 0310 AdvancedTCA Fabric Port 0.
On-board Dual-Ethernet 2 Option ROM Function B	Disabled **Enabled**	Enable/Disable ROM option for IBA GE Slot 0311 AdvancedTCA Fabric Port 1.

Note: **Bold** text indicates default settings.

7.3.10 PCI Express* Configuration Sub-Menu

To access this sub-menu, select **Advanced** on the menu bar, then **PCI Express Configuration**.

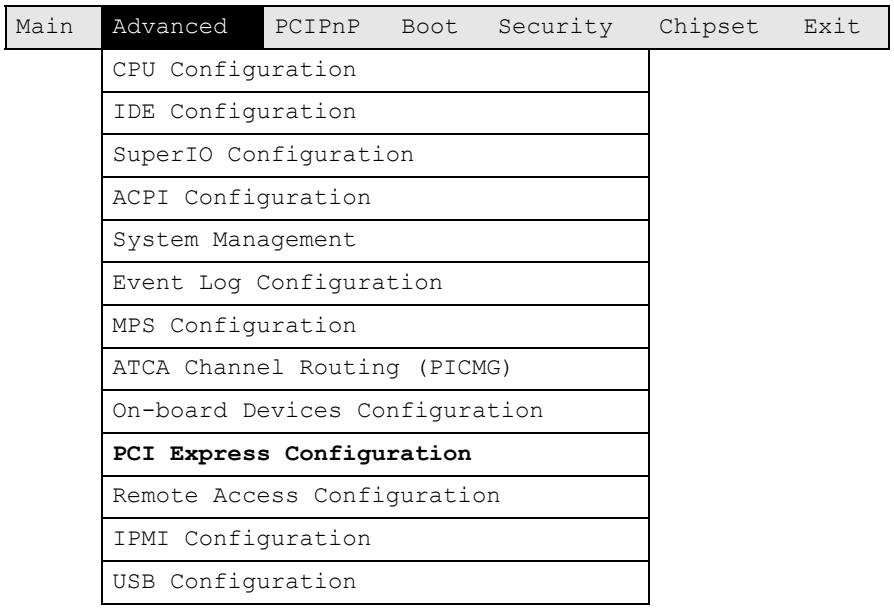


Table 43 shows PCI Express configuration options.

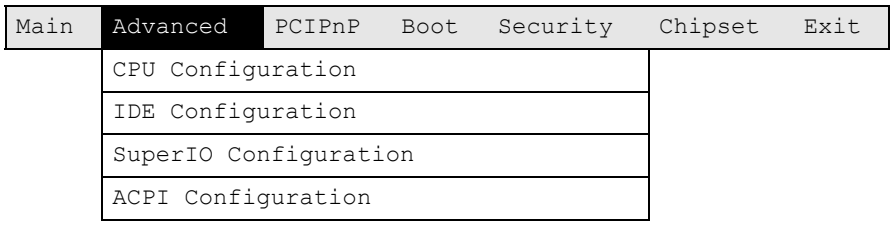
Table 43. PCI Express* Configuration Sub-Menu

Feature	Options	Description
PCI Express Port 4 - AMC B2	Disabled **Enabled**	Enable/Disable PCI Express port 4 for AMC B2.
Hot Plug Support - AMC B2	Disabled **Enabled**	Enable/Disable Hot Plug support for AMC B2.
PCI Express Port 6 - AMC B1	Disabled **Enabled**	Enable/Disable PCI Express port 6 for AMC B1.
Hot Plug Support - AMC B1	Disabled **Enabled**	Enable/Disable Hot Plug support for AMC B1.

Note: **Bold** text indicates default setting.
Note: SATA AdvancedMC hard disk drive modules do not support Hot Add or Hot Swap, even if it is enabled in the BIOS.

7.3.11 Remote Access Configuration Sub-Menu

To access this sub-menu, select **Advanced** on the menu bar, then **Remote Access Configuration**.



Main	Advanced	PCIPnP	Boot	Security	Chipset	Exit

System Management
Event Log Configuration
MPS Configuration
ATCA Channel Routing (PICMG)
On-board Devices Configuration
PCI Express Configuration
Remote Access Configuration
IPMI Configuration
USB Configuration

Table 44 shows remote access configuration options.

Table 44. Remote Access Configuration Sub-Menu

Feature	Options	Description
Remote Access	Disabled **Enabled**	Enable / Disable Remote Access function.
Serial Port Number	**COM1** COM2	Selects serial port for remote access.
Serial Port Base Address		Displays selected serial port base address.
Serial Port Mode	**115200 8,N,1** 57600 8,N,1 38400 8,N,1 19200 8,N,1 9600 8,N,1	Configures the serial port bits per second, data bits, parity, stop bits, and flow control.
Flow Control	**None** Hardware Software	Enables and configures flow control type.
Redirection after BIOS POST	**Always** Disabled Boot Loader	Specifies when redirection should occur.
Terminal Type	**ANSI** VT-100 VT-UTF8	Specifies the target terminal type.
VT-UTF8 Combo Key Support	Disabled **Enabled**	Enabled VT-UTF8 combination key support for ANSI and VT-100 terminals.

Notes:
1. Bold text indicates the default setting.
2. To use the Serial over LAN (SOL) feature described in Chapter 11.0, "Serial Over LAN (SOL)", the following settings must be used:
   - Remote Access = Enabled
   - Serial Port Number = COM2
   - Flow Control = Hardware
   - Redirection after BIOS POST = Always

7.3.12 IPMI Configuration Sub-Menu

To access this sub-menu, select **Advanced** on the menu bar, then **IPMI Configuration**.

Main	Advanced	PCIPnP	Boot	Security	Chipset	Exit

CPU Configuration
IDE Configuration
SuperIO Configuration
ACPI Configuration
System Management
Event Log Configuration
MPS Configuration
ATCA Channel Routing (PICMG)
On-board Devices Configuration
PCI Express Configuration
Remote Access Configuration
IPMI Configuration
USB Configuration

Table 45 shows the IPMI configuration options.

Table 45. IPMI Configuration Sub-Menu

Feature	Options	Description
Set LAN Configuration		Use this sub-menu to configrue LAN settings used by the SOL feature as described in Chapter 11.0, "Serial Over LAN (SOL)". For more details, see Table 46
Status of IPMC		Displays IPMI device status.
KCS-SMS IRQ	Disabled **IRQ11**	Selects the Management Controller IRQ for the System Management Software (SMS).
BIOS Watch Dog TImer Action	No Action Reset System **Power Cycle**	Configures the IPMC to reset or power down if the BIOS/POST fails.
Disable BIOS Watchdog Timer		Disables the BIOS/POST watchdog timer (for current session only).

Note: **Bold** text indicates default setting.

Table 46 shows the LAN configuration options.

Table 46. LAN Configuration Sub-Menu

Feature	Options	Description
Active LAN Channel	**01** 02	To use the SOL feature, channel 01 must be used
IP Address		IP address used by SOL
Subnet Mask		Subnet Mask used by SOL

Table 46. LAN Configuration Sub-Menu

Feature	Options	Description
Gateway Address		Gateway address used by SOL
MAC Address		This is a read-only field that displays the MAC address of the network interface that will be used for SOL

Note: **Bold** text indicates default setting.

7.3.13 USB Configuration Sub-Menu

To access this sub-menu, select **Advanced** on the menu bar, then **USB Configuration**.

Main	Advanced	PCIPnP	Boot	Security	Chipset	Exit

CPU Configuration
IDE Configuration
SuperIO Configuration
ACPI Configuration
System Management
Event Log Configuration
MPS Configuration
ATCA Channel Routing (PICMG)
On-board Devices Configuration
PCI Express Configuration
Remote Access Configuration
IPMI Configuration
USB Configuration

Table 47 shows USB configuration options.

Table 47. USB Configuration Sub-Menu

Feature	Options	Description
USB Devices Enabled		Displays currently attached USB devices that have been detected.
USB Function	Disabled 2 USB Ports **All USB Ports**	Enables USB controllers.
Legacy USB Support	Disabled **Enabled**	Enable legacy USB support. Auto option disables legacy support if no USB devices are detected.
USB 2.0 Controller	Disabled **Enabled**	Enable USB 2.0 Controller.

Table 47. USB Configuration Sub-Menu (Continued)

Feature	Options	Description
USB 2.0 Controller Mode	FullSpeed **HiSpeed**	Configures USB 2.0 for HiSpeed (480 Mbps), or FullSpeed (12 Mbps).
BIOS EHCI Hand-Off	Disabled **Enabled**	Enables work-around for operating systems without EHCI hand-off support.

Note: **Bold** text indicates default setting.

7.3.13.1 USB Mass Storage Device Configuration

Table 48 shows USB Mass Storage Device Configuration options.

Table 48. USB Mass Storage Device Configuration

Feature	Options	Description
Device #		Display USB Mass Storage device(s) Name.
Emulation Type	**Auto** Floppy Forced FDD Hard Disk CDROM	If Auto, USB devices less than 530 MByte are emulated as floppy and remaining as hard drive. Forced FDD option can be used to force a HDD formatted drive to boot as FDD (Ex. ZIP drive).

Note: **Bold** text indicates default setting.

7.4 PCIPnP Menu

To access this menu, select **PCIPnP** from the menu bar at the top of the screen.

Main	Advanced	PCIPnP	Boot	Security	Chipset	Exit

Table 49 shows PCI Plug and Play* options.

Table 49. PCIPnP Menu

Feature	Options	Description
Clear NVRAM	**No** Yes	Clear NVRAM during system boot.
PCI Latency TImer	**32** 64 96 128 160 192 224 248	Value in units of PCI clocks for the PCI device latency timer.
Allocate IRQ to PCI VGA	No **Yes**	No = Does not assign PCI request to VGA even if VGA request IRQ. Yes = Assigns IRQ to VGA.

Note: **Bold** text indicates default setting.

7.5 Boot Menu

To access this menu, select **Boot** from the menu bar at the top of the screen.

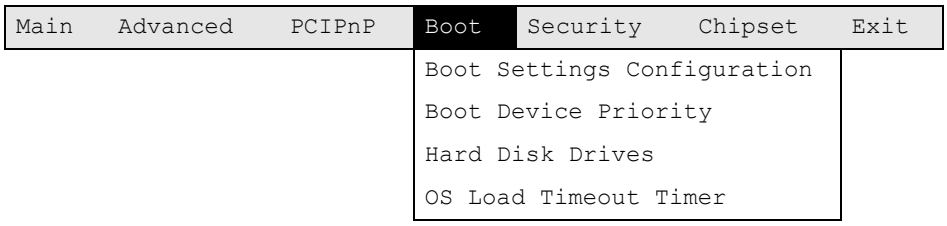


Table 50 shows options for setting the boot features and boot sequence.

Table 50. Boot Menu

Feature	Options	Description
Boot Settings Configuration	Select to display sub-menu	Set boot options.
Boot Device Priority	Select to display sub-menu	Specifies boot device priority.
Hard Disk Drives	Select to display sub-menu	Displays detected hard disk drives.
OS Load Timeout Timer	Select to display sub-menu	Specifies OS Load Action.

7.5.1 Boot Settings Configuration Sub-Menu

To access this sub-menu, select **Boot** on the menu bar, then **Boot Settings Configuration**.

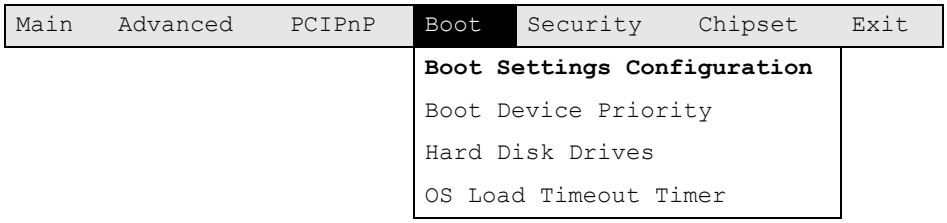


Table 51 shows Boot Settings Configuration options.

Table 51. Boot Settings Configuration Sub-Menu (Sheet 1 of 2)

Feature	Options	Description
Quick Boot	Disabled **Enabled**	Disable/Enable the BIOS to skip certain tests while booting, to decrease the time needed to boot the system.
Quiet Boot	**Disabled** Enabled	Enabled = Display normal POST messages. Disabled = Displays OEM logo.
AddOn ROM Display Mode	**Force BIOS** Keep Current	Set display mode for Option ROM.

Table 51. Boot Settings Configuration Sub-Menu (Sheet 2 of 2)

Feature	Options	Description
Bootup Num-Lock	Off **On**	Set power-on state for num-lock.
PS/2 Mouse Support	Disabled Enabled **Auto**	Set support for PS/2 mouse.
Wait For 'F1' If Error	**Disabled** Enabled	Disable/enable waiting for F1 key to be pressed if error occurs.
Hit 'DEL' Message Display	Disabled **Enabled**	Display "Press DEL to run Setup" in POST.
Interrupt 19 Capture	**Disabled** Enabled	Disable/enable the ability for option ROMs to trap interrupt 19.
Soft Reset	Disabled **Enabled**	Enable/Disable soft reset support
Retry Boot Sequence	Disabled **Enabled**	Retries boot sequence until a successful boot occurs.
Save CMOS in Flash	Disabled **Enabled**	Saves CMOS contents into flash memory

Note: **Bold** text indicates default setting.

7.5.2 Boot Device Priority Sub-Menu

To access this sub-menu, select Boot on the menu bar, then Boot Device Priority.

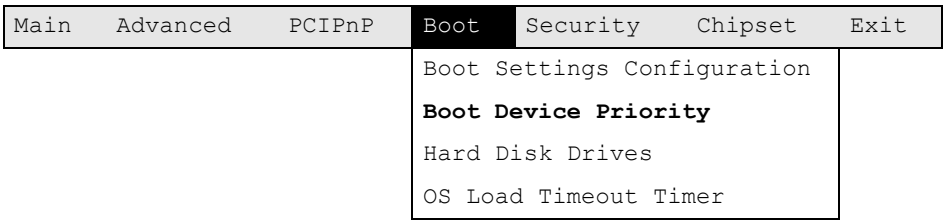


Table 52 shows Boot Device Priority options.

Table 52. Boot Device Priority Sub-Menu

Feature	Options	Description
1st Boot Device	Displays detected boot devices	Set the first boot device.
2nd Boot Device	Displays detected boot devices	Set the second boot device.
3rd Boot Device	Displays detected boot devices	Set the third boot device.

Table 52. Boot Device Priority Sub-Menu (Continued)

Feature	Options	Description
4th Boot Device	Displays detected boot devices	Set the fourth boot device.
5th Boot Device	Displays detected boot devices	Set the fifth boot device.

Note: **A device only shows as an option if it is installed and detected by the BIOS during boot. The factory default for boot device priority is as follows:**

1. USB device
2. SATA hard disk on AdvancedMC
3. PXE on GbE 1
4. PXE on GbE 2
5. PXE on GbE 3
6. PXE on GbE 4

7.5.3 Hard Disk Drives Sub-menu

To access this sub-menu, select Boot on the menu bar, then Hard Disk Drives.

```
Main   Advanced   PCIPnP   Boot   Security   Chipset   Exit
                            Boot Settings Configuration
                            Boot Device Priority
                            Hard Disk Drives
                            OS Load Timeout Timer
```

Table 53 shows Hard Disk Drives options.

Table 53. Hard Disk Drive Sub-Menu

Feature	Options	Description
1st Drive	Displays detected hard drives	Set the first hard drive.
2nd Drive	Displays detected hard drives	Set the second hard drive.

Note: **A device only shows as an option if it is installed and detected by the BIOS during boot**.

7.5.4 OS Load Timeout Timer Sub-Menu

To access this sub-menu, select **Boot** on the menu bar, then **OS Load Timeout Timer**.

```
Main   Advanced   PCIPnP   Boot   Security   Chipset   Exit
                            Boot Settings Configuration
                            Boot Device Priority
                            Hard Disk Drives
                            OS Load Timeout Timer
```

Table 54 shows OS Load Timeout Timer options.

Table 54

Table 54. OS Load Timeout Timer Sub-Menu

Feature	Options	Description
OS Load Action	**Disabled** Reset System Power Down Power Cycle	Specifies the action to take upon timeout.

Note: **Bold** text indicates default setting.

7.6 Security Menu

To access this menu, select **Security** from the menu bar at the top of the screen.

Main	Advanced	PCIPnP	Boot	Security	Chipset	Exit
				Supervisor Password		
				User Password		
				Change Supervisor Password		
				Change User Password		
				Boot Sector Virus Protection		

Table 55 shows passwords and security features.

Table 55. Security Menu

Feature	Options	Description
Supervisor Password		Display the Supervisor Password status. Installed/Not Installed.
User Password		Display the Supervisor Password status. Installed/Not Installed.
Change Supervisor Password		Set the supervisor password.
Change User Password		Set the user password.
Boot Sector Virus Protection	**Disabled** Enabled	Disable/enable boot sector virus protection.

Note: **Bold** text indicates default setting.

7.7 Chipset Menu

To access this menu, select **Chipset** from the menu bar at the top of the screen.

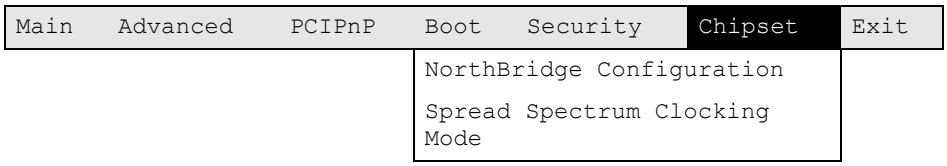


Table 56 describes the sub-menus used to select chipset features.

Table 56. Chipset Menu

Feature	Options	Description
Northbridge Configuration	Select to display sub-menu	Set Northbridge options.
Spread Spectrum Clocking Mode	Enabled **Disabled**	Enables / Disables Spread Spectrum Clocking for EMI control.

Note: **Bold** text indicates default setting.

7.7.1 Northbridge Configuration Sub-Menu

To access this menu, select **Chipset** from the menu bar and then **NorthBridge Configuration**.

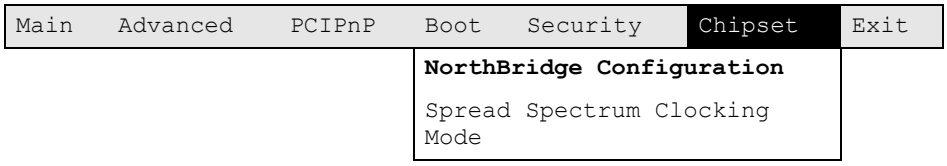


Table 57 shows the sub-menu used for configuring the Northbridge options.

Table 57. Northbridge Chipset Configuration

Feature	Options	Description
Memory Remap Feature	Disabled **Enabled**	Enables / Disables remapping of overlapped PCI memory above the total physical limit.
Memory Mirroring/Sparring	**Disabled**	Disables Memory Mirroring.
DMA Controller	**Disabled** Enabled	Enable / Disable DMA Controller.
DDR2 Refresh	**Auto** 7.8uS 3.9uS	Specifies DDR2 refresh rate. A higher refresh rate (7.8uS) may be required when operating in high temperature environments with certain types of DIMMs. The default Auto setting uses the memory SEEPROM (SPD) byte 12 Refresh Rate/Type to determine the appropriate setting.

Note: **Bold** text indicates default setting.

7.7.2 Spread Spectrum Clocking Mode Sub-Menu

To access this menu, select **Chipset** from the menu bar and then **Spread Spectrum Clocking Mode**.

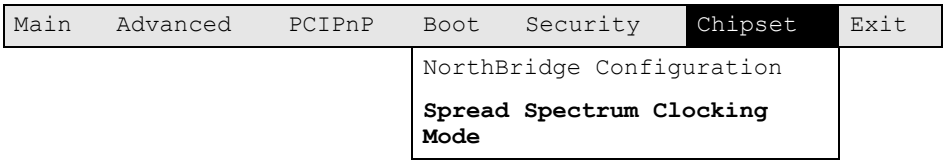


Table 58 describes the Spread Spectrum Clocking Mode options.

Table 58. Spread Spectrum Clocking Mode Configuration

Feature	Options	Description
Spread Spectrum Clocking Mode	**Disabled** Enabled	Enables / Disables Spread Spectrum Clocking for EMI control.

Note: **Bold** text indicates default setting.

7.8 Exit Menu

To access this menu, select **Exit** from the menu bar at the top of the screen.

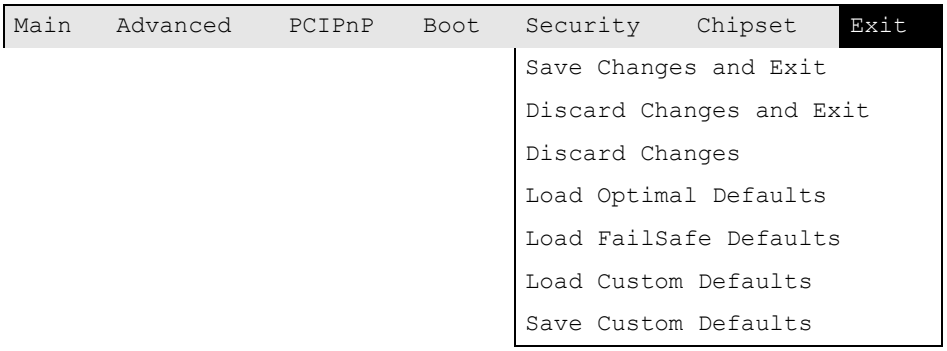


Table 59 describes the options under the Exit menu.

Table 59. Exit Menu

Feature	Options	Description
Save Changes and Exit		Exit system setup after saving changes.
Discard Changes and Exit		Exit system setup without saving changes.
Discard Changes		Discard changes without exiting.
Load Optimal Defaults		Load optimal default values.

Table 59. Exit Menu (Continued)

Feature	Options	Description
Load FailSafe Defaults		Load failsafe default values.
Load Custom Defaults		Load custom BIOS configuration
Save Custom Defaults		Save custom BIOS configuration

8.0 Error Messages

8.1 BIOS Error Messages

Table 60 lists BIOS error messages and gives an explanation of the message.

Table 60. BIOS Error Messages

Error Message	Explanation
Timer Error	This timer resides in ICH. Error message indicates an error while programming the count register of the timer. This may indicate a problem with the timer in ICH.
CMOS Battery Low	BIOS will report this error message when status bit (RTC_REGD.Bit7) in ICH is low. This bit is hard-wired to RTC power, so it will be low when the voltage in SuperCAP is low.
CMOS Settings Wrong	BIOS will load default value after it detects CMOS corruption. Error message is triggered if BIOS fails to load the default value to CMOS.
CMOS Checksum Bad	CMOS contents failed the checksum check. Error message indicates that the CMOS data has been changed by a program other than the BIOS or the CMOS is not retaining data due to hardware malfunction.
RAM R/W test failed	Error message indicates BIOS fail to read/write to memory content during RAM R/W test. RAM R/W test is executed during POST.
CMOS Date/Time Not Set	Error message indicates BIOS has detected an invalid value in date & time register. (e.g., Invalid date = 50h or invalid month = 13h).
System Event Log is Full	Error message indicates the System Event Log storage is full.
Refresh timer test failed	This timer is a counter based on 82C54 which provides memory refresh request signal periodically. Memory content need to be refreshed to compensate for the gradual leakage of charge from the capacitors which stores the data.
KBC BAT Test failed	Error message indicates that Keyboard controller BAT test has failed.

Notes: If “Wait for F1 Error” was enabled under the BIOS setup screen and any of the above error messages are displayed, the BIOS will wait for user input before proceeding with the boot up. The only exceptions are:

— CMOS Checksum BAD

— Clear CMOS Jumper enabled

BIOS setting “Wait for F1 Error” is not enabled by default.

8.2 Port 80h POST Codes

During the POST, the BIOS generates diagnostic progress codes (POST-codes) to I/O port 80h. If the POST fails, execution stops and the last POST code generated is left at port 80h. This code is useful for determining the point where an error occurred.

Table 61 through Table 64 give descriptions of the POST codes generated by the BIOS. They define the uncompressed INIT code checkpoints, the boot block recovery code checkpoints, and the runtime code uncompressed in F000 shadow RAM.

Note: Some codes are repeated in the tables because they apply to more than one operation.

Table 61. Bootblock Initialization Code Checkpoints

Checkpoint	Description
Before D1	Early chipset initialization is done. Early super I/O initialization is done, including RTC and keyboard controller. NMI is disabled.
D1	Perform keyboard controller BAT test. Check if waking up from power management suspend state. Save power-on CPUID value in scratch CMOS.
D0	Go to flat mode with 4 GByte limit and GA20 enabled. Verify the bootblock checksum.
D2	Disable CACHE before memory detection. Execute full memory sizing module. Verify that flat mode is enabled.
D3	If memory sizing module not executed, start memory refresh and do memory sizing in Bootblock code. Do additional chipset initialization. Re-enable CACHE. Verify that flat mode is enabled.
D4	Test base 512 KByte memory. Adjust policies and cache first 8 GBytes. Set stack.
D5	Bootblock code is copied from ROM to lower system memory and control is given to it. BIOS now executes out of RAM.
D6	Both key sequence and OEM-specific methods are checked to determine if BIOS recovery is forced. Main BIOS checksum is tested. If BIOS recovery is necessary, control flows to checkpoint E0.
D7	Restore CPUID value back into register. The Bootblock-Runtime interface module is moved to system memory and control is given to it. Determine whether to execute serial flash.
D8	The Runtime module is uncompressed into memory. CPUID information is stored in memory.
D9	Store the Uncompressed pointer for future use in PMM. Copying Main BIOS into memory. Leaves all RAM below 1 MByte Read-Write including E000 and F000 shadow areas but closing SMRAM.
DA	Restore CPUID value back into register. Give control to BIOS POST (ExecutePOSTKernel). See Table 62, “POST Code Checkpoints” on page 90 for more information.
E1-E8 EC-EE	OEM memory detection/configuration error. This range is reserved for chipset vendors and system manufacturers. The error associated with this value may different from one platform to the next.

Table 62. POST Code Checkpoints

Checkpoint	Description
03	Disable NMI, parity, video for EGA, and DMA controllers. Initialize BIOS, POST, runtime data area. Also initialize BIOS modules on POST entry and GPNV area. Initialized CMOS as mentioned in the kernel variable.
04	Check CMOS diagnostic byte to determine if battery power is OK and CMOS checksum is OK. Verify CMOS checksum manually by reading storage area. If the CMOS checksum is bad, update CMOS with power-on default values and clear passwords. Initialize status register A. Initializes data variables that are based on CMOS setup questions. Initializes both the 8259 compatible PICs in the system.
05	Initializes the interrupt controlling hardware (generally PIC) and interrupt vector table.
06	Do R/W test to CH-2 count reg. Initialize CH-0 as system timer. Install the POSTINT1Ch handler. Enable IRQ-0 in PIC for system timer interrupt. Traps INT1Ch vector to “POSTINT1ChHandlerBlock.”
08	Initializes the CPU. The BAT test is being done on KBC. Program the keyboard controller command byte is being done after Auto detection of KB/MS using AMI KB-5.
C0	Early CPU Init Start -- Disable Cache - Init Local APIC.
C1	Set up bootstrap processor information.
C2	Set up bootstrap processor for POST.
C5	Enumerate and set up application predecessors.
C6	Re-enable cache for bootstrap processor.

Table 62. POST Code Checkpoints (Continued)

Checkpoint	Description
C7	Early CPU Init Exit.
0A	Initializes the 8042-compatible Keyboard Controller.
0B	Detects the presence of PS/2 mouse.
0C	Detects the presence of Keyboard in KBC port.
0E	Testing and initialization of different Input Devices. Also, update the Kernel Variables. Traps the INT09h vector, so that the POST INT09h handler gets control for IRQ1. Uncompress all available language, BIOS logo, and Silent logo modules.
13	Early POST initialization of chipset registers.
24	Uncompress and initialize any platform specific BIOS modules.
30	Initialize System Management Interrupt.
2A	Initializes different devices through DIM.
2C	Initializes different devices. Detects and initializes the video adapter installed in the system that have optional ROMs.
2E	Initializes all the output devices.
31	Allocate memory for ADM module and uncompress it. Give control to ADM module for initialization. Initialize language and font modules for ADM. Activate ADM module.
33	Initializes the silent boot module. Set the window for displaying text information.
37	Displaying sign-on message, CPU information, setup key message, and any OEM-specific information.
38	Initializes different devices through DIM.
39	Initializes DMAC-1 & DMAC-2.
3A	Initialize RTC date/time.
3B	Test for total memory installed in the system. Also, check for DEL or ESC keys to limit memory test. Display total memory in the system.
3C	Mid POST initialization of chipset registers.
40	Detect different devices (Parallel ports, serial ports, and coprocessor in CPU, etc.) successfully installed in the system and update the BDA, EBDA, etc.
50	Programming the memory hole or any kind of implementation that needs an adjustment in system RAM size if needed.
52	Updates CMOS memory size from memory found in memory test. Allocates memory for Extended BIOS Data Area from base memory.
60	Initializes NUM-LOCK status and programs the KBD typematic rate.
75	Initialize Int-13 and prepare for IPL detection.
78	Initializes IPL devices controlled by BIOS and option ROMs.
7A	Initializes remaining option ROMs.
7C	Generate and write contents of ESCD in NVRam.
84	Log errors encountered during POST.
85	Display errors to the user and gets the user response for error.
87	Execute BIOS setup if needed.
8C	Late POST initialization of chipset registers.
8D	Build ACPI tables (if ACPI is supported).
8E	Program the peripheral parameters. Enable/Disable NMI as selected.
90	Late POST initialization of system management interrupt.
A0	Check boot password if installed.

Table 62. POST Code Checkpoints (Continued)

Checkpoint	Description
A1	Clean-up work needed before booting to OS.
A2	Takes care of runtime image preparation for different BIOS modules. Fill the free area in F000h segment with 0FFh. Initializes the Microsoft IRQ Routing Table. Prepares the runtime language module. Disables the system configuration display if needed.
A4	Initialize runtime language module.
A7	Displays the system configuration screen if enabled. Initialize the CPUs before boot, which includes the programming of the MTRRs.
A8	Prepares CPU for OS boot, including final MTRR values.
A9	Waits for user input at config display if needed.
AA	Uninstalls POST INT1Ch vector and INT09h vector. Deinitializes the ADM module.
AB	Prepares BBS for Int 19 boot.
AC	End of POST initialization of chipset registers.
B1	Saves system context for ACPI.
00	Passes control to OS Loader (typically INT19h).
61-70	OEM POST Error. This range is reserved for chipset vendors & system manufacturers. The error associated with this value may be different from one platform to the next.

Table 63. DIM Code Checkpoints

Checkpoint	Description
2A	Initializes different buses and performs the following functions: • **Function 0: Reset, Detect, and Disable** - Disables all device nodes, PCI devices, and PnP ISA cards. Assigns PCI bus numbers. • **Function 1: Static Device Initialization** - initializes all static devices that include manual configured onboard peripherals, memory and I/O decode windows in PCI-PCI bridges, and noncompliant PCI devices. Reserves static resources. • **Function 2: Boot Output Device Initialization** - Searches for and initializes any PnP, PCI, or AGP video devices.
38	Initializes different buses and performs the following functions: • **Function 3: Boot Input Device Initialization** - Searches for and configures PCI input devices and detects if system has standard keyboard controller. • **Function 4: IPL Device Initialization** - searches for and configures all PnP and PCI boot devices. • **Function 5: General Device Initialization** - Configures all onboard peripherals that are set to automatic configuration and configures all remaining PnP and PCI devices.

Table 64. ACPI Runtime Checkpoints

Checkpoint	Description
AC	First ASL check point. Indicates the system is running in ACPI mode.
AA	System is running in APIC mode.
01, 02, 03, 04, 05	Entering sleep state S1, S2, S3, S4, or S5.
10, 20, 30, 40, 50	Waking from sleep state S1, S2, S3, S4, or S5.

9.0 Addressing

9.1 PCI Configuration Map

Table 65 lists the PCI devices and the bus on which they reside.

Table 65. PCI Configuration Map

ID SEL#	BUS #	DEV #	V. ID	D. ID	Funct #	Description	PCI Description
	0	0	8086h	3590h	0	E7520 – Memory Controller Hub	Bridge, host-bridge, multi-function
	0	1	8086h	3591h	0	E7520 – Memory Error Reporting	Bridge, host-bridge, multi-function
	0	1	8086h	3594h	0	E7520 – DMA Controller	System peripheral, non-specific, single-function
	0	2	8086h	3595h	0	E7520 – Host-to-PCI Express A Bridge (x8 or x4)	Bridge, PCI-to-PCI, single-function, type 1 header
	0	3	8086h	3596h	0	E7520 – Host-to-PCI Express A1 Bridge (x4 only)	Bridge, PCI-to-PCI, single-function, type 1 header
	0	4	8086h	3597h	0	E7520 – Host-to-PCI Express B Bridge (x8 or x4) – (Support Hot-Plug)	Bridge, PCI-to-PCI, single-function, type 1 header
	0	5	8086h	3598h	0	E7520 – Host-to-PCI Express B1 Bridge (x4 only)	Bridge, PCI-to-PCI, single-function, type 1 header
	0	6	8086h	3599h	0	E7520 – Host-to-PCI Express C Bridge (x8 or x4) – (Support Hot-Plug)	Bridge, PCI-to-PCI, single-function, type 1 header
	0	7	8086h	359Ah	0	E7520 – Host-to-PCI Express C1 Bridge (x4 only)	Bridge, PCI-to-PCI, single-function, type 1 header
	0	7	8086h	359Bh	0	E7520 – Extended Configuration Registers	
	0	28	8086h	25Aeh	0	i6300ESB ICH – HUB Interface to PCI-X Bridge	
	0	29	8086h	25A9h	0	i6300ESB ICH – USB UHCI Controller #1	
	0	29	8086h	25Aah	1	i6300ESB ICH – USB UHCI Controller #2	
	0	29	8086h	25Abh	4	i6300ESB ICH – Watchdog Controller	
	0	29	8086h	25Ach	5	i6300ESB ICH – IOAPIC bus B	
	0	29	8086h	25Adh	7	i6300ESB ICH – USB EHCI Controller	
	0	30	8086h	25A1h	0	i6300ESB ICH – HUB Interface to PCI Bridge	
	0	31	8086h	25A2h	0	i6300ESB ICH – LPC Interface	
	0	31	8086h	25A1h	1	i6300ESB ICH – IDE Controller	

Table 65. PCI Configuration Map (Continued)

ID SEL#	BUS #	DEV #	V. ID	D. ID	Funct #	Description	PCI Description
	0	31	8086h	25A3h	2	i6300ESB ICH – Serial-ATA Controller	
	0	31	8086h	25A4h	3	i6300ESB ICH – SMBus Controller	
AD17	1	1	8086h	1229h	0	i82551er	
	2	0	8086h	0329h	0	i6700PXH – PCI-Express to PCI Bridge (P2P-A)	
	2	0	8086h	0326h	1	i6700PXH – I/OxAPIC-A	
	2	0	8086h	032Ah	2	i6700PXH – PCI-Express to PCI Bridge (P2P-B)	
	2	0	8086h	0327h	3	i6700PXH – I/OxAPIC-B	
AD17	3	1	8086h	1079h	0	I82546GB	
AD17	3	1	8086h	1079h	1	I82546GB	
AD18	3	2	8086h	1079h	0	I82546GB	
AD18	3	2	8086h	1079h	1	I82546GB	
	4 [0f-17]					AMC B2	
	6 [06-Oe]					AMC B1	

The AdvancedMC* configuration as it relates to the PCI Configuration Map can be confusing. The following additional information regarding the AMC configuration should help clarify the configuration:

- BUS 0 is the internal MCH and ICH device.
- BUS 1 is assigned to the secondary side of the PCI-to-PCI bridge 0:1e.0 (ICH bus 32bit/33MHz).
- BUS 2 to 4 is assigned to the secondary side of the PCI Express Port A of the MCH (PCI to PCI bridge 0:2.0). (Connected to PXH).
- BUS 5 is assigned to the secondary side of the PCI-to-PCI bridge 0:1c.0 (ICH bus PCI-X, no connect on MPCBL0010 SBC).
- BUS 6 to 0Eh is assigned to the secondary side of the PCI Express Port C of the MCH (PCI to PCI bridge 0:6.0). (Connected to AMC B1)
- BUS 0Fh to 17h is assigned to the secondary side of the PCI Express Port B of the MCH (PCI to PCI bridge 0:4.0). (Connected to AMC B2)

The hot plug devices (which can be added after the system has booted) will have a bus number based on the PCI BUS 0 scan order. At boot-up, Linux uses the bus number assigned by the BIOS while in POST. The PCI-Express Hot Plug driver uses the resource (BUS, IO, MEM) configured by the BIOS on the PCI Express root port.

The tree listing from Linux, with some comments, is:

```
# lspci -t
-[00]-+-00.0
      +-00.1
      +-02.0-[02-04]--+-00.0-[04]--
      |               \-00.2-[03]--+-01.0 (i82546GB, base ch 1)
      |                            +-01.1 (i82546GB, base ch 2)
      |                            +-02.0 (i82546GB, fabric port 0)
      |                             \-02.1 (i82546GB, fabric port 1)
      +-04.0-[0f-17]--                    (AMC B2)
      +-06.0-[06-0e]--                   (AMC B1)
      +-1c.0-[05]--
      +-1d.0
      +-1d.1
      +-1d.4
      +-1d.5
      +-1d.7
      +-1e.0-[01]----01.0              (i82551 Debug LAN)
      +-1f.0
      +-1f.1
      \-1f.3
```

9.2 FPGA Registers

This section describes the Field Programmable Gate Array (FPGA) register settings.

Note: Unused bits are reserved. To ensure compatibility with other products and upgrades to this product, do not modify unused bits.

Table 66. FPGA Register Legend

Symbol	Description
U	Unchanged (stays unchanged after reset)
X	Not Defined
NU	Not Used

Table 67. FPGA Register Overview

80h	POST Code low byte
81h	POST Code high byte
A00h	FPGA Version
A01h	Debug LED Control
A02h	Firmware Update Manager (manufacturing use only)
A03h	Reserved for IPMI Controller
A04h	Development Features
A05-A07h	Reserved
A08h	Telecom Clock Register 0: Configuration
A09h	Telecom Clock Register 1: Configuration
A0Ah	Telecom Clock Register 2: Configuration & Status
A0Bh	Telecom Clock Register 3: Configuration
A0Ch	Telecom Clock Register 4: Reset and Test Modes
A0Dh	Telecom Clock Register 5: PLD Version
A0Eh	Telecom Clock Register 6: Alarms
A0Fh	Telecom Clock Register 7: Interrupt Number
A10-A12h	Telecom Clock Extensions
A13-A1Fh	Reserved

Table 68. POST Codes 00:80h

Address	Action	D7	D6	D5	D4	D3	D2	D1	D0
0x080	Read	POST Code							
	Write	POST Code							
	Reset	00h							

POST codes are captured in this register as they are written.

Table 69. Extended POST Codes 0081h

Address	Action	D7	D6	D5	D4	D3	D2	D1	D0
0x081	Read	POST Code							
	Write	POST Code							
	Reset	00h							

POST codes are captured in this register as they are written.

Note: POST codes are not always 16-bit and the high byte in register 81h could be unrelated to the content of register 80h. Also, only a 16-bit Write to I/O 80h will write to I/O 81h. An 8-bit Write to I/O 81h is ignored.

Table 70. FPGA Version 0A00h

Address	Action	D7	D6	D5	D4	D3	D2	D1	D0
0xA00	Read	Reserved			Version				
	Write				NU				
	Reset				Version				

Version: Programmable logic version.

Table 71. Debug LED 0A01h

Address	Action	D7	D6	D5	D4	D3	D2	D1	D0
0xA01	Read	MfgFlag	RJ45	EnHD	EnPost	EnClk	Green0	Amber0	Red0
	Write	MfgFlag	RJ45	EnHD	EnPost	EnClk	Green0	Amber0	Red0
	Reset	0/NA	1	0	1	0	0	0	0

EnHD: Setting this bit uses LED Amber0 for displaying hard disk activity.

EnPost: Enables using the debug LED to display the last POST code of the boot. The BIOS clears this bit prior to the operating system launch.

EnClk: Enables telecom clock monitoring on the debug LED. EnHD and EnPost must be cleared. When the LED is green, both clocks are present. When the LED is amber, only one clock is present. When the LED is red, no clock is present or the Telco Clock PLD is not initialized. This is a debug mode.

Green0/Red0/Amber0: Debug LED 0. Used as a debug LED or to display POST codes (default during boot) or hard disk activity (default following boot) or as an end-user status/debug LED.

RJ45: This bit tells the FPGA which LEDs should reflect LAN activity; RJ-45 LEDs or grouped LEDs. The BIOS should set this bit as soon as possible to reflect the configuration of the fabric LAN. This should be set to 0 if the LAN goes to the fabric.

MfgFlag: A memory element used by the BIOS and test software in manufacturing.

Note: Tthis bit is cleared on a power-up, but is not affected by a reset

The Debug LED is amber/green when in Reset (this is hardware). As soon as the FPGA is programmed, the LED is amber and is enabled for POST code display. If the BIOS fails, it is possible to read the POST code. If the BIOS succeeds, it disables the POST code and enables HD activity on the green LED. If needed, the application software can then disable hard disk activity reporting and directly control the bi-color LED for status reporting.

To read the 8-bit POST code:

- Both colors: Start of POST sequence.
- Amber blink: This is the high nibble. 0 to 15 blinks represent hexadecimal 0 to F.
- Green blink: This is the low nibble. 0 to 15 blinks represent hexadecimal 0 to F.

Table 72. FWUM 0A02h

Address	Action	D7	D6	D5	D4	D3	D2	D1	D0
0xA02	Read	NU	NU	Status	DoProg	Roll-back	UART	Mode	Reset
	Write	NU	NU	NU	DoProg	Roll-back	UART	Mode	Reset
	Reset	NU	NU	NU	0	0	0	1	0

Reset: FWUM reset -- the power-up state of this bit will be 0 under normal operating conditions

Mode: FWUM mode pin

UART: Set this bit to connect UART1 to the FWUM for programing.

RollBack: Set to 1 for manual rollback (in conjunction with DoProg); Leave at 0 for normal operation.

DoProg: Set to 1 then to 0 to start programming the IPMC with the new code.

Status:

1: FWUM Ready

0: FWUM Busy

Table 73. Development Features 0A04h

Address	Action	D7	D6	D5	D4	D3	D2	D1	D0
0xA04	Read	Minor Version				NU	PCB	SSC1	SSC0
	Write	NU	NU	NU	NU	NU	NU	SSC1	SSC0
	Reset	NU	NU	NU	NU	NU	NU	1	1

Minor Version: Minor version with no impact on the IPMC -- for development minor version tracking.

SSC0: Special Serial Connection bit 0

SSC1: Special Serial Connection bit 1

SSC1 / SSC0:

01: Float the **FW_RXD** pin; use this to program the FWUM.

10: Connect **FW_RX**D and **FW_TXD** to an RJ-45 RS-232 port

00: Connect **B1** to **ICH UART1**

PCB: PCB version.

These bits define a special connections between serial devices that are meaningless under normal operation. They are for development and/or manufacturing facilities. Leave these bits in their default state for normal operation.

Minor Version: Minor version with no impact on the IPMC; for development minor version tracking.

SSC0: Special Serial Connection bit 0

SSC1: Special Serial Connection bit 1

SSC1/SSC0:

01: Float the **FW_RXD** pin -- use this to program the FWUM

10: Connect **FW_RXD** and **FW_TXD** to an RJ-45 RS-232 port

00: Connect B1 to ICH UART1

PCB: PCB version.

These bits define special connections between serial devices that are meaningless under normal operation. They are for development and/or manufacturing facilities. Leave these bits in their default state for normal operation.

Table 74. Telecom Clock Register 0 0A08h

Address	Action	D7	D6	D5	D4	D3	D2	D1	D0
0xA08	Read	HWMODE	HO_LOS	MS2	MS1	REFALIGN	FCS	E3DS3	E3DS30C3
	Write	HWMODE	HO_LOS	MS2	MS1	REFALIGN	FCS	E3DS3	E3DS30C3
	Reset	0	0	0	0	0	0	0	0

HWMODE: Enables automatic switching by hardware

HO_LOS: Switch criteria in hardware (HW) mode.When set, use PLL holdover detection as the switch criteria.When cleared, use loss of clock (internal to PLD) as the switch criteria.

MS2/MS1: PLL Mode selection:

MS[2..1] = 00: Normal operation

MS[2..1] = 01: Holdover mode

MS[2..1] = 10: Free-run mode

MS[2..1] = 11: Reserved

REFALIGN: Reference clock phase alignment; changing this bit from 0 to 1 starts the alignment.

FCS: Filter characteristics of the PLL:

0: 12 Hz filter without phase slope limitation

1: 6 Hz filter with phase slope limited to 41 ns per 1.326 ms.

E3DS3/E3DS3OC3: These bits select the transmission clock frequency when `TXREFx_SEL[2..0]=111` in telecom clock register 3.

```
E3DS3OC3 = 0, E3DS3 = 1:  8.592 MHz

E3DS3OC3 = 0, E3DS3 = 0:  11.184 MHz

E3DS3OC3 = 1, E3DS3 = 1:  34.368 MHz

E3DS3OC3 = 1, E3DS3 = 0:  44.736 MHz
```

Table 75. Telecom Clock Register 1 0A09h

Address	Action	D7	D6	D5	D4	D3	D2	D1	D0
0xA09	Read	RSV1	RSV0	SELCLK3B	SELCLK3A	REFSEL	8K_16M	SEL_REFFRQ	SEL_RDNCLK
	Write	NU	NU	SELCLK3B	SELCLK3A	NU	8K_16M	SEL_REFFRQ	SEL_RDNCLK
	Reset	X	X	0	0	X	0	0	0

SELCLK3B: Select the clock to send to the backplane CLK3B:

0: from the first AdvancedMC (AMC B1, CLKC)

1: from the second AdvancedMC (AMC B2, CLKC).

SELCLK3A: Select clock to send to backplane CLK3A:

0: from the first AdvancedMC (AMC B1, CLKC)

1: from the second AdvancedMC (AMC B2, CLKC).

8K_16M: This bit is valid only when the transmission clock is selected by setting TXREFx_SEL[2..0]=101 in TelClock3 register. Setting this bit selects the transmission clock frequency as 16.384 MHz, while clearing it select 8.0 kHz.

SEL_REFFRQ: Select reference frequency (8 k or 19.44 M): 0 = 8 kHz, 1=19.44 MHz. This bit controls the multiplexer that feeds clocks to the PLL:

0: PLL input clocks = CLK1A & CLK1B (8kHz per AdvancedTCA spec)

1: PLL input clocks = CLK2A & CLK2B (19.44MHz per AdvancedTCA spec)

SEL_RDNCLK: Setting this bit to the value of the formerly read **REFSEL** enables the switch-over to the actual unused reference in the case of LOS of the actual reference.

REFSEL: Show the reference that is currently selected:

0: Primary reference

1: Secondary reference

RSV1 / RSV0: Reserved.

Table 76. Telecom Clock Register 2 0A0Ah

Address	Action	D7	D6	D5	D4	D3	D2	D1	D0
0xA0A	Read	PRI_LOS	SEC_LOS	HOLDOVER	UNLOCK	NU	DRVCLKA1	NU	DRVCLKA0
	Write	NU	NU	NU	NU	NU	DRVCLKA1	NU	DRVCLKA0
	Reset	X	X	X	X	X	0	X	0

PRI_LOS: Loss of primary reference clock detected. This bit is high when the primary clock at the input of the PLL (i.e., after PLD mux) is lost.

SEC_LOS: Loss of secondary reference clock detected. This bit is high when the primary clock at the input of the PLL (i.e. after PLD mux) is lost.

HOLDOVER: Holdover detected by the PLL

UNLOCK: Unlock detected by the PLL

DRVCLKA1: Drives transmission clock **CLKA** for AdvancedMC B2. This bit is forced to 0 when AdvancedMC B2 is absent or unpowered.

DRVCLKA0: Drives transmission clock **CLKA** for AdvancedMC B1. This bit is forced to 0 when AdvancedMC B1 is absent or unpowered.

Table 77. Telecom Clock Register 3 0A0Bh

Address	Action	D7	D6	D5	D4	D3	D2	D1	D0
0xA0B	Read	DRVCLK3B	DRVCLK3A	TXREF1_SEL[2..0]			TXREF0_SEL[2..0]		
	Write	DRVCLK3B	DRVCLK3A	TXREF1_SEL[2..0]			TXREF0_SEL[2..0]		
	Reset	0	0	000			000		

DRVCLK3B: Enables **MLVDS** buffer to drive **CLK3B** to the backplane. This bit is forced to 0 until the IPMC authorizes it.

DRVCLK3A: Enables **MLVDS** buffer to drive **CLK3A** to the backplane. This bit is forced to 0 until the IPMC authorizes it.

TXREF1_SEL[2..0]: Transmission reference clock for AdvancedMC B2 selection (See Table 78)

TXREF0_SEL[2..0]: Transmission reference clock for AdvancedMC B1 selection (See Table 78) The transmission frequency is selected according to Table 78:

Table 78. Transmission Frequency Selection

TXREFx_SEL[2..0]	Transmission Clock Frequency
000	1.544 MHz (T1, J1)
001	2.048 MHz (E1)
010	4.096 MHz (E1)
011	6.312 MHz (J2)
100	8.192 MHz (E1)
101	8 kHz / 16.384 MHz† (E1, T1, J1, J2)
110	19.44 MHz (OC3, 12/STM-1, 4)
111	34.368 / 44.736 MHz‡ (E3, T3) or 8.592 / 11.184 MHz

Notes:

† 8 kHz or 16 MHz can be selected by bit 8K_16M in telecom clock register 1.

‡ One frequency can be selected by bits E3DS3 and E3DS3OC3 in telecom clock register 0.

Table 79. Telecom Clock Register 4 0A0Ch

Address	Action	D7	D6	D5	D4	D3	D2	D1	D0
0xA0C	Read	NU	NU	NU	NU	NU	IRQTST	RESET	TEST
	Write	NU	NU	NU	NU	NU	IRQTST	RESET	TEST
	Reset	X	X	X	X	X	0	1	0

IRQTST: Interrupt test -- the state of this bit is ORed with the real interrupt.

Note: This bit is for software testing. Ignore it in normal operation. A "**1**" asserts the interrupt request.

TEST: Ignores IPMC and shelf manager authorization.

Note: Use this bit for testing only. In normal operation, leave this bit set to 0. Otherwise, the MPCBL0010 SBC will not be compliant with the AdvancedTCA* specification.

RESET: Hardware reset of the PLL

Table 80. Telecom Clock Register 5 0A0Dh

Address	Action	D7	D6	D5	D4	D3	D2	D1	D0
0xA0D	Read	PCB	Version						
	Write	NU	NU						
	Reset	PCB	Version						

PCB: Set to 1 to indicate that the compilation switch is properly set in the source code and that the PLD is compiled for PCB revision 1.

VERSION: PLD code version. Values:

PCB&Version: FF: indicates a test PLD to make a clock generator

PCB&Version: FE: indicates a test PLD used during manufacturing tests

Table 81. Telecom Clock Register 6 0A0Eh

Address	Action	D7	D6	D5	D4	D3	D2	D1	D0
0xA0E	Read	UNLOCK10	UNLOCK01	HLDOVR10	HLDOVR01	SEC10	SEC01	PRI10	PRI01
	Write	NU	NU	NU	NU	NU	NU	NU	NU
	Reset	X	X	X	X	X	X	X	X

PRI01: Bit PRI_LOS in telecom clock register 2 switched from 0 to 1

PRI10: Bit PRI_LOS in telecom clock register 2 switched from 1 to 0

SEC01: Bit SEC_LOS in telecom clock register 2 switched from 0 to 1

SEC10: Bit SEC_LOS in telecom clock register 2 switched from 1 to 0

HLDOVR01: Bit HOLDOVER in telecom clock register 2 switched from 0 to 1

HLDOVR10: Bit HOLDOVER in telecom clock register 2 switched from 1 to 0

UNLOCK01: Bit UNLOCK in telecom clock register 2 switched from 0 to 1

UNLOCK10: Bit UNLOCK in telecom clock register 2 switched from 1 to 0

This register reports changes since the last time it was read. A legacy ISA interrupt is generated when any of these bits are set. The actual interrupt used is assigned by the BIOS at boot time and can be read from telecom clock register 7.

Reading this register clears all bits that were '1' prior to reading. Bits that turned to '1' during the reading are not affected.

Table 82. Telecom Clock Register 7 0A0Fh

Address	Action	D7	D6	D5	D4	D3	D2	D1	D0
0xA0F	Read	NU	NU	NU	NU	Interrupt Number			
	Write	NU	NU	NU	NU	Interrupt Number			
	Reset	X	X	X	X	0101b			

The content of this register is the number of the legacy ISA interrupt used for events. (See telecom clock register 6). It is initialized at boot time by the BIOS.

The interrupt is acknowledged by a Read of telecom clock register 6. Always perform a Read to this register before enabling the interrupt in the chipset to remove any pending interrupt.

Note: A value of '**2**' hooks the interrupt to an SMI.

See Chapter 12.0, "Telecom Clock" for a complete list of telecom clock register and API settings.

9.3 IPMC Addresses

The IPMI controller has a parallel interface (bit bang) defined as follows:

AD[7:0]: Address/Data multiplexed

Ads#: Address strobe

Read: Read/Write#

Ds#: Data strobe

The bits are GPIOs on the IPMI controller and are toggled by software. This interface provides up to 256 8-bit locations that are both readable and writable. Pull-ups on Read and Clk signals guarantee that the interface is idle while the IPMC is in reset.

The IPMC should leave the data port in input by default. Pull-up resistors are used to avoid floating the input of the FPGA and IPMC.

To access data through this interface, proceed as follows:

1. For **Idle** state: AD[7:0] in input, Ads# high, Read high, Strobe# high
2. Select register: Read low, then AD[7:0] = register address, then ADS# high-to-low-to-high pulse
3. Write a register: Read low, then AD[7:0] = data, Strobe# high-to-low-to-high pulse.
4. Read selected register: AD[7:0] = inputs, Read = high

Table 83. IPMC Register Legend

Address	Function
00h	SBC Control
01h	SBC Status
02h	PostCodeLow (I/O 80)

Table 83. IPMC Register Legend (Continued)

Address	Function
03h	PostCodeHigh (I/O 81)
04h-05h	Reserved
06h	LED Color Control
07h	LED Control
08-0Fh	Reserved
10-11h	AMC B1
12-13h	AMC B2
14-17h	Reserved
18h	CPU 0 VIDs
19h	CPU 0 Status
1A-1Fh	Reserved
20h	ADCs Grab Control
21h	ADC1 Reading
22h	ADC2 Reading
23h	Reserved
24h	Fabric Control 1
25h	Fabric Control 2
26h	Reserved
27h	Reset Source
28h	Frimware Hub Control
29h	Reset Events
2Ah	Crosspoint Switch Control
2Bh	Crosspoint Switch Data
2Ch	Reserved
2Dh	Miscellaneous Control and Status
2E-FDh	Reserved
FEh	POST Code Register (if enabled)
1FFh	Version

Table 84. SBC Control 00h

Address	Action	D7	D6	D5	D4	D3	D2	D1	D0
00h	Read	0	BoardON	TurnX	PwrBtn	LTYPE	LTEST	UART	BRST
	Write	HT0	NU	NU	PwrBtn(1)	LTYPE	LTEST	UART	BRST
	PowerUp	0	0	0	0	1	0	0	0

BRST: Board Reset; set this bit for a minimum of 16ms to reset the SBC.

LTEST: Lamp test; set this bit to perform a global lamp test on all the front panel LEDs.

UART: UART override;
when set, the serial port to the IPMC will take-over the SBC serial port.
when cleared, the IPMC will receive the data (RX) for monitoring purposes but will not be able to transmit

LTYPE: LED type.
when cleared, whenever possible, amber LEDs are used instead of red.
when set, red is used instead of amber.
Applicable LEDs: Postcode/HardDisk/Debug LED.

PwrBtn: ICH Power Button Control. This bit can be set, but it cannot be cleared. It will clear itself when the power sequencing requested is completed (i.e. **TurnX**=0).

Note: This bit should only be set when TurnX is 0. This bit will not work when a test-jig is inserted and its **TEST_ON#** signal is asserted (Override power-on in absence of firmware in IPMC).

TurnX: Turn **ON** or turn **OFF** in progress.

BoardON: Power status of the board
1 = Board **ON**

HTU: Hard Turn-Off. Turns off power supplies regardless of the chipset state.
Writing a 1 to this bit will turn off the power supply immediately.
On a Read, this will always return **0**.

9.3.0.1 PwrBtn usage

For a power up:

1. IPMC sets bit **PowerBtn**
2. FPGA asserts **PowerBtn** ICH input and waits for the ICH to de-assert its "**suspend**" output
3. When "**suspend**" is de-asserted, the FPGA de-asserts the power button and turns off all supplies.

For a power down:

1. IPMC sets bit **PowerBtn**
2. FPGA asserts **PowerBtn** for 33 ms (ICH debouncer delay is 16 ms)
3. FPGA waits for the ICH "**suspend**" output to be de-asserted. Then it turns off all supplies.

Note: There is no timeout and if the operating system does not shut down, the board remains stuck in this condition.

The IPMC must implement a timeout of reasonable length (i.e. seconds) and perform a hard turn-off (i.e. HTO=1) in the case of a timeout.

Quick power-down:

1. IPMC sets bit **HTO**.
2. FPGA turns off all supplies.

Note: The "**suspend**" information from the chipset does not reflect the state of the power supply.

Table 85. SBC Status 01h

Address	Action	D7	D6	D5	D4	D3	D2	D1	D0
01h	Read	Vcore	1.2V	1.5V	1.8V	2.5V	3.3V	5V	12V
	Write	NU	NU	NU	NU	NU	NU	NU	NU
	PowerUp	NU	NU	NU	NU	NU	NU	NU	NU

Table 86. POST Code Low 02h

Address	Action	D7	D6	D5	D4	D3	D2	D1	D0
02h	Read	Last access to I/O 80 in the BIOS address space							
	Write	NU	NU	NU	NU	NU	NU	NU	NU
	PowerUp	NU	NU	NU	NU	NU	NU	NU	NU

Table 87. POST Code High 03h

Address	Action	D7	D6	D5	D4	D3	D2	D1	D0
03h	Read	Last access to I/O 81 in the BIOS address space							
	Write	NU	NU	NU	NU	NU	NU	NU	NU
	PowerUp	NU	NU	NU	NU	NU	NU	NU	NU

Table 88. LED Color Control 06h

Address	Action	D7	D6	D5	D4	D3	D2	D1	D0
06h	Read	U2COL1	U2COL0	U1COL1	U1COL0	L2COL1	L2COL0	L1COL1	L1COL0
	Write	U2COL1	U2COL0	U1COL1	U1COL0	L2COL1	L2COL0	L1COL1	L1COL0
	PowerUp	0	0	0	0	0	0	0	0

L1COL[1:0]: ATCA LED 1 color control: 00 = amber, 10 = red, others = off

L2COL[1:0]: ATCA LED 2 color control: 00 = amber, 10 = red, 01 = green, others = off

U1COL[1:0]: User LED 1 color control: 00 = amber, 10 = red, 01 = green, others =off

U2COL[1:0]: User LED 1 color control: 00 = amber, 10 = red, 01= green, others = off

Table 89. LED Control 07h

Address	Action	D7	D6	D5	D4	D3	D2	D1	D0
07h	Read	0LED1		ULED2	ULED1	LED3	LED2	LED1	LED0
	Write	0LED1		ULED2	ULED1	LED3	LED2	LED1	LED0
	PowerUp	0		0	0	0	0	0	1

LED0: Standard ATCA0 LED control: Hotswap LED, color is blue

LED1: Standard ATCA1 LED control: Out of service LED, color from LED color control register. This bit only works if bit OLED1 is set

LED2: Standard ATCA2 LED control: Health LED, color from LED color control register

LED3: Standard ATCA3 LED control: Heart beat LED, color is amber

ULED1: User LED 1, color from LED color control register

ULED2: User LED 2, color from LED color control register

OLED1: Override LED1. In this implementation, LED1 is controlled by the FWUM. Setting this bit will override the FWUM LED control signal and activate bit LED1

Table 90. AdvancedMC B1 Control & Status 10h

Address	Action	D7	D6	D5	D4	D3	D2	D1	D0
10h	Read	MRLSw	Fault#	AttSw	Present#	EnAMC	EnIPMB	En12V	En3V
	Write	MRLSw	Fault#	AttSw	Present#	EnAMC	EnIPMB	En12V	En3V
	PowerUp	0	1	0	1	0	0	0	0

MRLSw: Mechanical retention latch status for MCH (IPMC must write this bit)

Fault#: Fault indication for MCH (IPMC must write this bit)

AttSw: Attention switch for MCH (IPMC must write this bit)

Present#: AdvancedMC presence for MCH (IPMC must write 0 for presence)

En3V: Enables 3.3V power: bit is locked in "**0**" state if no AdvancedMC module is present

En12V: Enables 12V power: bit is locked in "**0**" state if no AdvancedMC module is present

EnIPMCB: Enables I^2C link on AdvancedMC. module: bit is locked in "**0**" state if no AdvancedMC module is present

EnAMC: Enables AdvancedMC module: bit is locked in "**0**" state if no AdvandedMC is present

Table 91. AdvancedMC B1 Control & Status 11h

Address	Action	D7	D6	D5	D4	D3	D2	D1	D0
11h	Read	ClkCEn		ClkAEn	12V0k	12VFault	3V0k	3VFault	Present
	Write	ClkCEn		ClkAEn					
	PowerUp	0		0					

Present: Indicates that an AdvancedMC module is present

3VFault: Fault on 3.3V voltage from an overcurrent

3V0k: Valid 3.3V voltage

12VFault: Fault on 12V

12V0k: Valid 12V voltage

ClkAEn: Authorizes the telecom clock circuit to drive synchronization clock **CLKA**

ClkCEn: Authorizes the 100 MHz PCI-Express clock driver for this AdvancedMC module

Even though authorization is given by the IPMC to drive the clocks to the AdvancedMC module, no actual clocks are driven if the module is not present, unpowered, or illpowered. These bits can be set prior to turning on the AdvancedMC module's power.

A readback returns the state of the bit, but does not reflect the actual clock. In the case of bad power (**12VFault**=1 for example), the clock is not driven even if the authorization bit is set. On an AdvancedMC extraction, these bits are automatically cleared.

Table 92. AMC B2 Control & Status 12h

Address	Action	D7	D6	D5	D4	D3	D2	D1	D0
12h	Read	MRLSw	Fault#	AttSw	Present#	EnAMC	EnIPMB	En12V	En3V
	Write	MRLSw	Fault#	AttSw	Present#	EnAMC	EnIPMB	En12V	En3V
	PowerUp	0	1	0	1	0	0	0	0

MRLSw: Mechanical retention latch status for MCH (IPMC must write this bit)

Fault#: Fault indication for MCH (IPMC must write this bit)

AttSw: Attention switch for MCH (IPMC must write this bit)

Present#: AdvancedMC presence for MCH (IPMC must write 0 for presence)

En3V: Enables 3.3V power: bit is locked in "**0**" state if no AdvancedMC module is present

En12V: Enables 12V power: bit is locked in "**0**" state if no AdvancedMC module is present

EnIPMCB: Enables I^2C link on AdvancedMC module: bit is locked in "**0**" state if no AdvancedMC module is present

EnAMC: Enables AdvancedMC module: bit is locked in "**0**" state if no AdvancedMC module is present

Table 93. AdvancedMC B2 Control & Status 13h

Address	Action	D7	D6	D5	D4	D3	D2	D1	D0
13h	Read	ClkCEn		ClkAEn	12V0k	12VFault	3V0k	3VFault	Present
	Write	ClkCEn		ClkAEn					
	PowerUp	0		0					

Present: Indicates that an AdvancedMC module is present

3VFault: Fault on 3.3V voltage from an overcurrent

3V0k: Valid 3.3V voltage

12VFault: Fault on 12V voltage

12V0k: Valid 12V voltage

ClkAEn: Authorizes the telecom clock circuit to drive synchronization clock **CLKA**

ClkCEn: Authorizes the 100 MHz PCI-Express clock driver for this AdvancedMC module.

Even though authorization is given by the IPMC to drive the clocks to the AdvancedMC module, no actual clocks are driven if the module is not present, unpowered, or illpowered. These bits can be set prior to turning on the AdvancedMC module's power. A readback will return the state of the bit, but does not reflect the actual clock. In the case of bad power (**12VFault** = 1, for example), the clock is not driven even if the authorization bit is set. On an AdvancedMC module extraction, these bits are automatically cleared.

Table 94. CPU 0 VIDs 18h

Address	Action	D7	D6	D5	D4	D3	D2	D1	D0
18h	Read	NU	NU	VID5	VID4	VID3	VID2	VID1	VID0
	Write	NU	NU	NU	NU	NU	NU	NU	NU
	PowerUp	NU	NU	NU	NU	NU	NU	NU	NU

Table 95. CPU 0 Status 19h

Address	Action	D7	D6	D5	D4	D3	D2	D1	D0
19h	Read	NU	NU	MCERR	HOT	TRIP	VTT	IERR	PR
	Write	NU	NU	NU	NU	NU	NU	NU	NU
	PowerUp	NU	NU	NU	NU	NU	NU	NU	NU

PR: CPU present

IERR: CPU internal error

VTT: CPU type required VTT

TRIP: Indicates a thermal trip was detected and the CPU switcher was turned off. This bit retains its value when the board is turned off, but it is cleared at power-up time. Prior to the first power up, this bit is always cleared (no special treatment needed for the first powerup).

HOT: Indicates the CPU pin **PROCHOT#** is asserted.

MCERR: CPU Machine Check Error. Asserted on various conditions that are BIOS-dependant

Table 96. ADC Grab Control 20h

Address	Action	D7	D6	D5	D4	D3	D2	D1	D0
20h	Read	NU	NU	NU	NU	NU	NU	NU	NU
	Write	NU	NU	NU	NU	NU	NU	NU	NU
	PowerUp	NU	NU	NU	NU	NU	NU	NU	NU

Any Bit: Writing any value to the grab register arms the grab circuit. The grab circuit captures the next conversion result in about 1 ms.

The analog to digital conversion is a continuous process in the sense that conversion occurs regardless of the IPMC. Valid data is available every millisecond or so. The IPMC tells the FPGA in advance that wants a fresh copy of the ADCs reading. Unless the IPMC requests a fresh copy, the ADC values returned by the FPGA never change.

Table 97. ADC1 and ADC2 Grab Data 21-22h

Address	Action	D7	D6	D5	D4	D3	D2	D1	D0
21-22h	Read	ADC1 or ADC2 data							
	Write	NU	NU	NU	NU	NU	NU	NU	NU
	PowerUp	NU	NU	NU	NU	NU	NU	NU	NU

Address 21h returns **ADC1;** address 22h returns ADC2

ADC1 measures the current on the main 48V input power

ADC1 = (256/4.096)(50K/499)$R_s I_{in}$,
Where R_s is the sense resistor set to 0.0033ohm

Or, to get the current from the reading:
I_{in} = (4.096/256))(499/50K)ADC/0.0033 = 0.0479ADC1
with **ADC1** in [0, 255] and I_{in} in [0, 12.2A]

ADC2 measures the main input voltage (48V nominal)

The reading is as follows:

ADC2 = (256/4.096V)(15K/295K)V_{in},

or, to get the voltage from the reading:
V_{in} = (4.096V/256)(295K/15K)ADC2 = 0.315ADC2
with **ADC2** in [0, 255] and V_{in} in [0, 80V]

Note: To find the power of the entire board, the input diodes need to be taken into account.

The drop in the two diodes is as follows:
Vd = I_{in} 0.1 + 0.7V

Add this value to the actual measurement to estimate the input voltage.

Table 98. Fabric Control 1 24h

Address	Action	D7	D6	D5	D4	D3	D2	D1	D0
24h	Read	PCB	3VOC	NU	EnClk3B	EnClk3A	Reserved	Reserved	Reserved
	Write	NU	NU	NU	EnClk3B	EnClk3A	Reserved	Reserved	Reserved
	PowerUp	NU	NU	NU	0	0	0	0	0

EnClk3A: Authorizes the telecom clock circuit to drive clock 3A to the backplane. Must also be enabled in the Telco register.

EnClk3B: Authorizes the telecom clock circuit to drive clock 3B to the backplane. Must also be enabled in the Telco register.

3VOC: 3.3V overcurrent status.
1: overcurrent
0: normal.

PCB: PCB revision.

Table 99. Fabric Control 2 25h

Address	Action	D7	D6	D5	D4	D3	D2	D1	D0
25h	Read	NU	NU	NU	ReqClk3B	ReqClk3A	NU	NU	NU
	Write	NU	NU	NU	NU	NU	NU	NU	NU
	PowerUp	NU	NU	NU	NU	NU	NU	NU	NU

ReqClk3A: A copy of bit **DRVCLK3A** of register **TelClock3**: when this bit is set, the application that configures the TelClock module requests to drive **CLK3A** in the backplane.

ReqClk3B: A copy of bit **DRVCLK3B** of register **TelClock3**. When this bit is set, the application that configures the TelClock module requests to drive **CLK3A** in the backplane.

Table 100. Reset Source 27h

Address	Action	D7	D6	D5	D4	D3	D2	D1	D0
27h	Read	Vcore	1.2V	1.5V	1.8V	2.5V	3.3V	5V	12V
	Write	NU	NU	NU	NU	NU	NU	NU	NU
	PowerUp	0	0	0	0	0	0	0	0

On a power fail (i.e. that causes a reset), the content of register **SBC Status** (register 01h) is captured here. See the **SBC Status** register for the detailed bit definition.

Table 101. Firmware Hub Control 28h

Address	Action	D7	D6	D5	D4	D3	D2	D1	D0
28h	Read	NU	NU	NU	NU	NU	FWHID	FWH1	FWH0
	Write	NU	NU	NU	NU	NU	FWHID	FWH1	FWH0
	PowerUp	NU	NU	NU	NU	NU	0	0	0

FWH0: 1 = connect **FWH0** to IPMC; 0 = connect **FWH0** to ICH

FWH1: 1 = connect **FWH1** to IPMC; 0 = connect **FWH1** to ICH

FWHID: Value of ID[0] of **FWH0** matches this bit; **FWH1** has the inverted value

If the main processor needs to change the ID of the **FWH**, it has to ask the IPMC to do it.

Note: The default configuration connects **FWH0** and **FWH1** to the ICH.

Table 102. Reset Events 29h

Address	Action	D7	D6	D5	D4	D3	D2	D1	D0
29h	Read	NU	PwGd	PFRE	NU	PCIREv	PCIR	SWEv	SW
	Write	NU	NU	Clear	NU	Clear	FWHID	Clear	NU
	PowerUp	NU	X	1	NU	X	0	X	0

SW: Direct reading of the reset switch: 1 = switch pressed; 0 = switch released

SWEv: Switch Event: this bit turns to **1** when the reset switch is pressed and stays at '**1**' until a **1** is written at this bit position. This bit is used to capture a short pulse on the switch.

PCIR: Direct reading of the PCI reset: **1** = PCI reset asserted; **0** = no PCI reset

PCIEv: PCI Reset Event: this bit turns to **1** when a PCI reset occurs and stays in this state until a 1 is written at this bit position. This bit is used to capture a short pulse on **PCI_RESET**.

SwHw: When set, the reset switch performs a hardware reset independent of the IPMC. When cleared, the IPMC deals with hard/warm resets.

PFREv: Power fail reset event: this bit turns to **1** when a Power Fail occurs and stays in this state until a **1** is written at this bit position. This bit is used to capture a short pulse on the power source. Since power supplies are not valid during a normal power-up, this bit is always set following a normal power-up. It is not possible to clear this bit when the power supplies are not stable. Make sure **PwrgGd** (see below) is active before clearing **PFREv**.

PwrGd: Directs reading of the power good signal that goes to the ICH (and resets everything)

On a power-up (i.e. SBC inserted in the chassis), some false events may be reported. The IPMC must ignore these first events. When the IPMC leave its reset state, its has to write **0Ah** in register 29h. Also, a "read-modify-write" on this register should not be done since this could result in clearing an event. Unless an event need to be cleared, write **0**.

Table 103. Crosspoint Switch Control 2Ah

Address	Action	D7	D6	D5	D4	D3	D2	D1	D0
2Ah	Read	Reset	Chip	A5	A4	A3	A2	A1	A0
	Write	Reset	Chip	A5	A4	A3	A2	A1	A0
	PowerUp	1	0	0	0	0	0	0	0

A[5..0]: Address of a VSC3108 (See the Vitesse* VSC3108 datasheet)

Chip: Specifies which VSC3108 crosspoint switch to talk to (See Table 104)

Reset: Send a Reset pulse to the crosspoint switch -- must be 0 in normal operation

To write a nibble in a crosspoint switch, proceed in this exact order:

1. Wait for bit "**Busy**" to be **0** (register 2Bh).
2. Write the data nibble in the crosspoint data register (2Bh).
3. Write the address and chip identification in the crosspoint control register (2Ah).

Note: If the board is not fully powered, this register is locked.

Assignment of the crosspoints switches ports is defined in Table 104:

Table 104. Crosspoint Switch Ports Register

Chip	Port	Input Signal Source	Port	Output Signal Designation
0	A0	AMC B1 port 0	Y0	AMC B1 port 0
	A1	AMC B2 port 0	Y1	AMC B2 port 0
	A2	Fabric Channel 1 port 0	Y2	Fabric Channel 1 port 0
	A3	Fabric Channel 1 port 1	Y3	Fabric Channel 1 port 1
1	A0	AMC B1 port 1	Y0	AMC B1 port 1
	A1	AMC B2 port 1	Y1	AMC B2 port 1
	A2	Fabric Channel 2 port 0	Y2	Fabric Channel 2 port 0
	A3	Fabric Channel 2 port 1	Y3	Fabric Channel 2 port 1

Table 105. Crosspoint Switch Data 2Bh

Address	Action	D7	D6	D5	D4	D3	D2	D1	D0
2Bh	Read	Busy	NU	NU	NU	D3	D2	D1	D0
	Write	NU	NU	NU	NU	D3	D2	D1	D0
	PowerUp	NU	NU	NU	NU	0	0	0	0

D[3..0]: Data to write in the crosspoint chip. (See the crosspoint control register.)

Busy: When set, the interface is busy; wait for this bit to be 0 before writing in registers 2A-2Bh. The time for the complete transfer is less than 8 ms.

Table 106. Miscellaneous Controls and Status 2Dh

Address	Action	D7	D6	D5	D4	D3	D2	D1	D0
2Dh	Read	NU	NU	NU	SwHw	NU	NU	JMP1	JMP0
	Write	NU	NU	NU	SwHw	NU	NU	NU	NU
	PowerUp	NU	NU	NU	1	NU	NU	NU	NU

SwHw: When set, the reset switch performs a hardware reset independent of the IPMC. When cleared, the IPMC handles the hard/warm reset.

JMPO: Status of jumper 0: **0** = In, **1** = Out

JMP1: Status of jumper 1: **0** = In, **1** = Out

Table 107. IPMC POST Codes FEh

Address	Action	D7	D6	D5	D4	D3	D2	D1	D0
FEh	Read	POST Codes							
	Write	POST Codes							
	PowerUp	00h							

POST Codes: POST codes are captured in this register as they are written. The content of this register is serialized and transmitted off-board to a display module if bit **IPOST** (register 2Ah) is set. Otherwise, the register is functional but the display module will show the CPU POST codes.

Table 108. Version FFh

Address	Action	D7	D6	D5	D4	D3	D2	D1	D0
FFh	Read	Reserved			Version				
	Write	Reserved			NU				
	PowerUp	Reserved			Version				

Version: Programmable logic version: for the IPMC to track the FPGA version -- this register returns the save value as the other version register on LPC

10.0 Hardware Management Overview

10.1 Intelligent Platform Management Controller (IPMC)

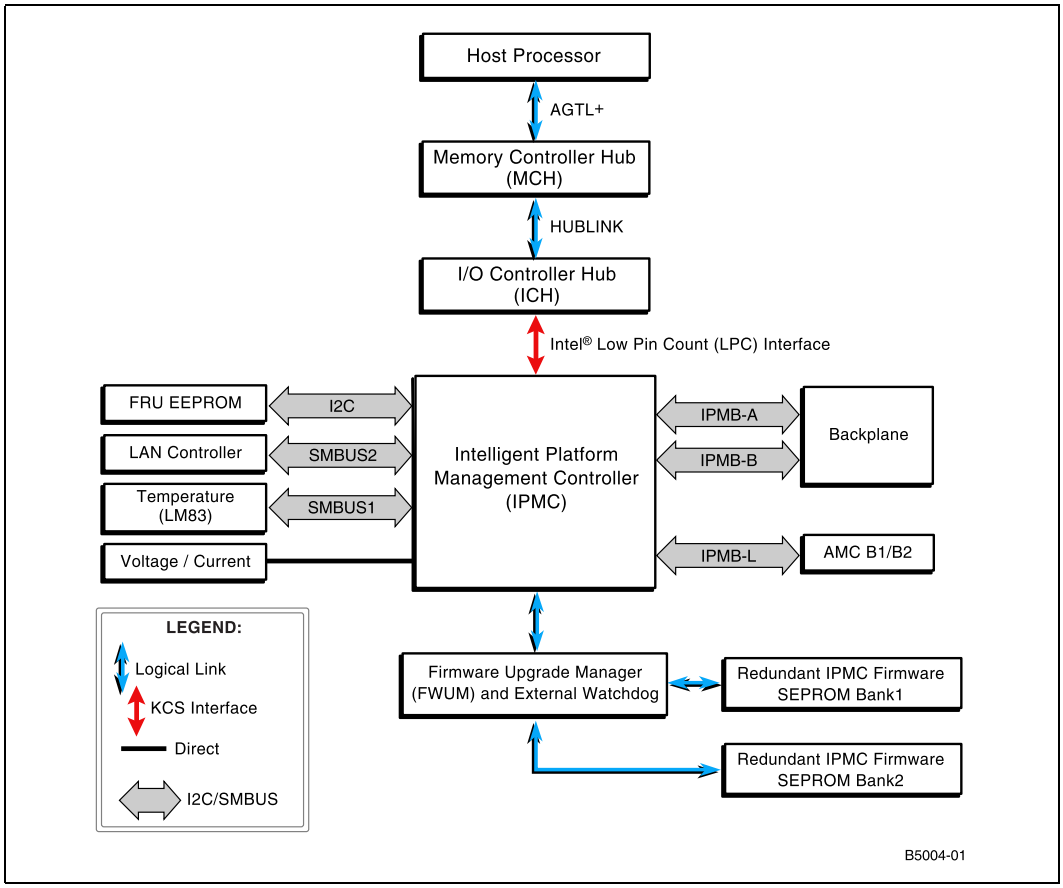
The MPCBL0010 SBC uses the Renesas* H8S/2168 for the Intelligent Platform Management Controller (IPMC). The IPMC management subsystem provides monitoring, event logging, and recovery control. The IPMC serves as the gateway for management applications to access the platform hardware.

The main processors communicate with the IPMC using the Keyboard Controller Style (KCS) interface. BIOS uses the SMM interface. The base address of the LPC interface for SMS is 0xCA2 and 0xCA4 for SMM operation. The BIOS is also able to communicate with the IPMC for POST error logging purposes and fault resilient purposes.

The memory subsystem of the IPMC consists of integrated flash memory to hold the IPMC operation code, and integrated RAM for data. The field replacement unit (FRU) inventory information is stored in the nonvolatile memory on an EEPROM connected via a local I^2C interface to the IPMC microcontroller. It is possible to store up to 4 KB within the FRU inventory information stored in the EEPROM. Events are generated over the IPMB to the Shelf Manager (ShMC), which maintains a SEL for each device in the chassis. This ensures that 'postmortem' logging information is available even if the main processor for the MPCBL0010 SBC becomes disabled or non-functional.

The IPMC provides six I^2C bus connections. Two are used as the redundant IPMB connections to the backplane, one is used for IPMB-L bus with AdvancedMC* modules, two are used for the LAN connections for IPMI Over LAN, and the last one is for local EEPROM storage.

Figure 22. IPMC Block Diagram



If an IPMB bus fault or IPMC failure occurs, IPMB isolators are used to switch and isolate the backplane/system IPMB bus from the faulted SBC board. Where possible, the IPMC activates the redundant IPMB bus to re-establish system management communication to report the fault.

The onboard DC voltages, currents, and temperature are monitored by the IPMC microcontroller. The IPMC will log an event into the ShMC SEL if any of the thresholds are exceeded.

To increase the reliability of the MPCBL0010 SBC management subsystem, an external watchdog supervisor is implemented only for the IPMC . The IPMC strobes the external watchdog at two-second intervals to ensure continuity of operation of the board's management subsystem. If the IPMC ceases to strobe the watchdog supervisor, the watchdog isolates the IPMC from the IPMBs and resets the IPMC. The watchdog supervisor does not reset the payload power and the restart of the IPMC does not affect the payload. It restores the previous hot swap state and power level negotiated with the shelf manager. The watchdog timeout expires after six seconds if strobes are not generated. The external watchdog supervisor is not configurable and should not be confused with the IPMI v1.5 watchdog timer commands.

This external watchdog of the IPMC is implemented in a second microcontroller called the Firmware Upgrade Manager (FWUM). This microcontroller is responsible for monitoring the IPMC and for managing the IPMC fail safe firmware upgrade process.

The FWUM can handle two firmware codes that are stored in two external SEPROMs. If a failure occurs during a firmware upgrade, the FWUM automatically rolls back to the redundant IPMC firmware image.

10.2 Sensor Data Record (SDR)

Sensor Data Records contain information about the type and number of sensors in the baseboard, sensor threshold support, event generation capabilities, and the types of sensor readings handled by system management firmware. SDRs also contain the configuration of a specific sensor such as threshold/hystheresis, and event generation capabilities that specifies sensor behavior. Some fields of the sensor SDR are configurable through IPMI v1.5 commands and are set to built-in default values.

The MPCBL0010 SBC management controller is set up as a satellite management controller (SMC). It supports sensor devices, and uses the IPMI dynamic sensor population feature of IPMI v1.5 to merge the hot-swapped AdvancedMC sensors with the MPCBL0010 SBC sensor population. Normally, the AdvancedTCA* ShMC is informed about an AdvancedMC insertion is through the AdvancedMC carrier hot swap sensor. However, to remain compliant to IPMI v1.5, the IPMC updates the sensor population change indicator timestamp accessible through the Get Device SDR Info command. All SDRs can be queried using Device SDR commands to the firmware. Baseboard sensors that have been implemented are listed in the following table.

Table 109. Hardware Sensors (Sheet 1 of 4)

Sensor Number	Sensor Type	Sensor Name (Signal Monitored)	Monitored Via	Scanning Enabled in Power-Off State (M1)	Health LED (Green to Red)
0x00	Platform Alert	IPMC Reboot	IPMC	Yes	N/A
0x01	Watchdog 2	IPMI Watchdog	IPMC	Yes	On watchdog expiration
0x02	Management Subsystem Health	IPMC Storage Err	IPMC	Yes	N/A
0x03	System Event	FRU0 Reconfig	IPMC	Yes	N/A
0x04	Cable/Interconnect	EventRCV ComLost	IPMC	Yes	N/A
0x05	System SCPI Power State	ACPI State	IPMC	Yes	N/A
0x06	OEM Firmware Info (1) (OEM reading type)	IPMI Info-1	IPMC	Yes	N/A
0x07	OEM Firmware Info (2) (OEM reading type)	IPMI Info-2	IPMC	Yes	N/A
0x08	IPMB Link Sensor	IPMB0 Link State	IPMC	Yes	N/A
0x09	OEM IPMB-L Link Sensor	FRU0 IPMBL State	IPMC	Yes	N/A
0x0A	OEM IPMB-L Link Sensor	FRU1 IPMBL State	IPMC	Yes	N/A
0x0B	OEM IPMB-L Link Sensor	FRU2 IPMBL State	IPMC	Yes	N/A
0x0C	OAh DMI-based availability with OEM data 2, 3	FRU0 FRU Agent	IPMC	Yes	N/A
0x0D	OAh DMI-based availability with OEM data 2, 3	FRU1 FRU Agent	IPMC	Yes	N/A
0x0E	OAh DMI-based availability with OEM data 2, 3	FRU2 FRU Agent	IPMC	Yes	N/A
0x0F	ATCA FRU hot swap	FRU0 HotSwap	IPMC	Yes	N/A
0x10	ATCA FRU hot swap	FRU1 HotSwap	IPMC	Yes	N/A

Table 109. Hardware Sensors (Sheet 2 of 4)

Sensor Number	Sensor Type	Sensor Name (Signal Monitored)	Monitored Via	Scanning Enabled in Power-Off State (M1)	Health LED (Green to Red)
0x11	ATCA FRU hot swap	FRU2 HotSwap	LM83	Yes	N/A
0x12	OEM FWUM Status	Firmware Upg Mng	FWUM	Yes	N/A
0x13	Platform Alert	Health Error	IPMC (Aggregate)	No	Reflects current LED status
0x14	Temperature	Temp Air Inlet	LM83	Yes	Exceeds critical threshold
0x15	Temperature	Temp BoardA Area	LM83	Yes	Exceeds critical threshold
Ox16	Temperature	Temp CPU	LM83	No	Exceeds critical threshold
0x17	Temperature	Temp MCH	LM83	No	Exceeds critical threshold
0x18	Temperature	Temp Vcore	LM83	No	Exceeds critical threshold
0x19	Temperature	Temp BoardB Area	LM83	Yes	Exceeds critical threshold
0x1A	Temperature	Temp PXH	LM83	No	Exceeds critical threshold
0x1B	Temperature	Temp CPLD Area	LM83	No	Exceeds critical threshold
0x1C	Temperature	Temp 12vPS Area	LM83	No	Exceeds critical threshold
0x1D	Current	FRU2 Icc +12V	IPMC	No	Exceeds critical threshold
0x1E	Current	FRU1 Icc +12V	IPMC	No	Exceeds critical threshold
0x1F	Current	Icc +12V	IPMC	No	Exceeds critical threshold
0x20	Voltage	Vcc +12V	IPMC	No	Exceeds critical threshold
0x21	Current	Icc +5V	IPMC	No	Exceeds critical threshold
0x22	Voltage	Vcc +5V	IPMC	No	Exceeds critical threshold
0x23	Current	Icc +3.3VSB	IPMC	Yes	Exceeds critical threshold
0x24	Voltage	Vcc +3.3VSB	IPMC	Yes	Exceeds critical threshold
0x25	Current	Icc +1.8V	IPMC	No	Exceeds critical threshold
0x26	Voltage	Vcc +1.8V	IPMC	No	Exceeds critical threshold
0x27	Current	Icc +1.5V	IPMC	No	Exceeds critical threshold
0x28	Voltage	Vcc +1.5V	IPMC	No	Exceeds critical threshold
0x29	Voltage	Vcc +3.3V	IPMC	No	Exceeds critical threshold

Table 109. Hardware Sensors (Sheet 3 of 4)

Sensor Number	Sensor Type	Sensor Name (Signal Monitored)	Monitored Via	Scanning Enabled in Power-Off State (M1)	Health LED (Green to Red)
0x2A	Voltage	Vcc +2.5V	IPMC	No	Exceeds critical threshold
0x2B	Voltage	Vcc Vtt DDR	IPMC	No	Exceeds critical threshold
0x2C	Voltage	Vcc Core Voltage	IPMC	No	Loss of critical power
0x2D	Current	Icc -48V	IPMC	No	Exceeds critical threshold
0x2E	Voltage	Vcc -48V	IPMC	No	Exceeds critical threshold
0x2F	Current	3.3V Over Icc	IPMC	No	Exceeds critical threshold
0x30	Power Supply (OEM Power Good reading type)	Power Good	IPMC	Yes	N/A
0x31	Power Supply (OEM Power Good reading type)	Power Good Event	IPMC	No	Loss of critical power (allow detection of first supply)
0x32	Unit Based	FRU0 Power	IPMC	No	Exceeds critical threshold
0x33	Unit Based	FRU1 Power	IPMC	No	Exceeds critical threshold
0x34	Unit Based	FRU2 Power	IPMC	No	Exceeds critical threshold
0x35	OEM ATCA Board Reset Sensor	Board Reset	IPMC	No	When SBC is reset
0x36	System Firmware Progress	POST Error	BIOS	No	When POST hang is detected
0x37	OEM POST value sensor	POST value	BIOS	No	N/A
0x38	CPU Critical Interrupt	Critical Int	BIOS	No	Therm trip and CPU errors
0x39	Memory	Memory	BIOS	No	Uncorrectable memory error
0x3A	POST Memory Resize	CmosMemorySize	BIOS	No	On assertion
0x3B	Platform Security Violation Attempt	Preboot Password	BIOS	No	On violation attempt
0x3C	Processor	CPU 0 Status	IPMC	No	Proc Hot (throttle)
0x3D	Processor	CPU 0 ThermalTrip	IPMC	No	Thermal Trip
0x3E	Boot Error	FWH 0 Boot Error	IPMC	No	Invalid boot sector
0x3F	Boot Error	FWH 1Boot Error	IPMC	No	Invalid boot sector
0x40	Power Supply	RTN A Pres-Fuse	IPMC	Yes	N/A
0x41	Power Supply	RTN B Pres-Fuse	IPMC	Yes	N/A
0x42	Power Supply	-48V A Pres-Fuse	IPMC	Yes	N/A
0x43	Power Supply	-48V B Pres-Fuse	IPMC	Yes	N/A
0x44	Power Supply	FRU1 Mp Over Icc	FPGA	Yes	N/A
0x45	Power Supply	FRU1 Over Icc	FPGA	Yes	N/A

Table 109. Hardware Sensors (Sheet 4 of 4)

Sensor Number	Sensor Type	Sensor Name (Signal Monitored)	Monitored Via	Scanning Enabled in Power-Off State (M1)	Health LED (Green to Red)
0x46	Management Subsystem Health	FRU1 Sensor Err	IPMC	Yes	N/A
0x47	Power Supply	FRU2 Mp Over Icc	FPGA	Yes	N/A
0x48	Power Supply	FRU2 Over Icc	FPGA	Yes	N/A
0x49	Management Subsystem Health	FRU2 Sensor Err	IPMC	Yes	N/A
0x4A	Platform Alert	FRU0 Pwr Denied	IPMC	Yes	N/a
0x4B	Platform Alert	FRU1 Pwr Denied	IPMC	Yes	N/A
0x4C	Platform Alert	FRU2 Pwr Denied	IPMC	Yes	N/a

Table 110. OEM Sensor Types

OEM Name	OEM Number	Description
OEM Firmware Information	COh	Sensor indicates information about firmware state. According to the Event/Reading Type, the 2 first bits will have assertion mask set. Associated event/reading type code: • 0x70-OEM Firmware Info 1 • 0x71-OEM Firmware Info 2 • 0x75-OEM Firmware Info 2
Init Agent Sensor	C2h	Display the last error that occur in the RunInitAgent. Associated event/reading type code: • 03h - IPMI Digital discrete
IPMBL Link State	C3h	Sensor indicates the status of the 3rd IPMB link named L. This sensor matches the AdvancedTCA defined type F1h (SDR_SENSTYPE_ATCA_PHYSICAL_IPMB0). See AdvancedTCA specification ECN 3.0 1.0 001 section 3.8.4 for details related to this sensor. An OEM sensor type is used because the type is reserved for Port Link A & B. Sensor Port Link L do not include a port B and Port L is placed at the same location as IPMB A. All bytes related to IPMB B are set to "enable-working" state. The sensor will only move from state (byte 4 in Get Sensor reading command): [3] 1b = IPMB A enabled, IPMB-B enabled to [2] 1b = IPMB A disabled, IPMB-B enabled A value of 1 and 0 is not possible. This sensor matches the AdvancedTCA defined type F1h.
AdvancedTCA Reset Sensor	C4h	Sensor indicates board reset source. All defined bits will have assertion event mask set. Associated event/reading type code: • 6Fh IPMI Sensor Specific
FIA Error Sensor	C5h	Sensor indicates if there as been an error during the FRU Information Agent scan (used for E-Keying). Associated event/reading type code: 0Ah - DMI-based availability
POST Value Sensor	C6h	Sensor indicates BIOS POST error code. Associated event/reading type code: • 6Fh - IPMI Sensor Specific
FWUM Status	C7h	Sensor indicates the state of the Firmware Update Manager (for rollback). Associated event/reading type code: • 6Fh OEM FWUM Status

Table 111. OEM Event/Reading Type

OEM Name	OEM Number	Description
OEM Firmware Information 1	70h	Internal diagnostic data.
OEM Firmware Information 2	75h	Internal diagnostic data.
OEM Power Good	77h	Discrete sensor indicates power good status.

10.3 System Event Log (SEL)

MPCBL0010 SBC IPMC events are logged and stored in non-volatile memory on the AdvancedTCA shelf manager. There is no local SEL on the MPCBL0010 SBC. The SBC IPMC sends events to the AdvancedTCA shelf manager to ensure that post-mortem logging information is available should a failure occur that disables the SBCs processor. Events are forwarded to the shelf manager and logged to the SEL as required in the AdvancedTCA specification.

Table 112. SEL Events Supported (Sheet 1 of 5)

Sensor Type	Sensor Type Code	Sensor Specific Offset	Event	Description
Reserved	00h	-	Reserved	Reserved
Temperature	01h	-	Temperature	Temperature reading exceeds thresholds.
Voltage	02h	-	Voltage	Voltage reading exceeds thresholds.
Current	03h	-	Current	Current reading exceeds supported thresholds.
Platform Security Violation Attempt	06h	01h	Pre-boot password violation - user password	Password check failed.
		04h	Other pre-boot password violation	Password check failed.
Processor	07h	00h	IERR	Processor IERR has occurred.
		01h	Thermal Trip	Processor thermal trip has occurred.
		04h	Initialization Failure	Processor did not start.
		06h	SM BIOS uncorrectable CPU-complex error	Uncorrectable error.
		07h	Processor Presence Detected	Indicates processor is present.
		0Ah	Processor Automatically Throttled	Processor started throttling due to excessive temperature.
Power Supply	08h	00h	Presence Detected	Power feed presence (not enabled by default).
		01h	Power Supply Failure Detected	Fuse failure detected.
Unit Based (Power)	0Bh	-	Power (Watts)	Power (watts) reading exceeds supported threshold.
Memory	0Ch	00h	Correctable ECC	Correctable ECC memory error has occurred.
		01h	Uncorrectable ECC	Uncorrectable ECC memory error has occurred.
POST Memory Resize	0Eh	-	Generic Discreet Reading Type	Indicates if CMOS memory size is wrong.

Table 112. SEL Events Supported (Sheet 2 of 5)

Sensor Type	Sensor Type Code	Sensor Specific Offset	Event	Description
System Firmware Progress	0Fh	00h	Unspecified	CMOS Settings Wrong, CMOS Checksum Bad, CMOS Date/Time Not Set. Event Data2 = 00h
			No Usable System Memory	Raw R/W test failed. Event Data2 = 02h
			Unrecoverable Hard-disk/ATAPI/ IDE Device Failure	Primary Master Hard Disk Error, Primary Slave Hard Disk Error, Secondary Master Hard Disk Error, Secondary Slave Hard Disk Error, Primary Master Drive - ATAPI Incompatible, Primary Slave Drive - ATAPI Incompatible, Secondary Master Drive - ATAPI Incompatible, Secondary Slave Drive - ATAPI Incompatible, SMART error. Event Data2 = 03h
			Unrecoverable System Board Failure	Refresh timer test failed, DMA Controller Error, DMA-1 Error, DMA-2 Error, Timer Error. Event Data2 = 04h
			Unrecoverable PS/2 or USB Keyboard Failure	KBC BAT Test failed ~<INS> Pressed, Unlock Keyboard. Event Data2 = 07h
System Event	12h	00h	System Reconfigured	Indicates change in AdvancedMC population or sensor population change.
CPU Critical Interrupt	13h	04h	PCI SERR	System Bus Error.
		05h	PCI PERR	PCi Parity Error.
Cable / Interconnect	1Bh	-	Generic Discreet Reading Type	Indicates if link is available or not.
Boot Error	1Eh	03h	Invalid Boot Sector	Indicates the firmware hub boot failed.
Slot Connector	21h	00h	Fault Status	Indicates SFP device fault.
		02h	Connector Device Installed	Indicates SFP device present.
System ACPI Power States	22h	00h	SO/GO	Board is running.
		06h	S4/S5	Soft off.
		07h	Soft Off Any	Can not determine precise soft off state.
		0Bh	Legacy On State	Board is on, but ACPI state cannot be determined.
		0Ch	Legacy Off State	Board is in unknown ACPI state.
		0Eh	Unknown	Board is unknown ACPI state.
Platform Alert	24h	-	Generic Discrete Reading	Indicates if the alert is on of off.
Watchdog	23h	00h	Timer Expired, Status Only	WDT expired, no effect on board.
		01h	Hard Reset	WDT reset after the monitor timeout.
		02h	Power Down	WDT shutdown after the monitor timeout.
		03h	Power Cycle	WDt power cycle after the monitor timeout.
		08h	Timer Interrupt	WDT pre-timeout (first stage) reached.

Table 112. SEL Events Supported (Sheet 3 of 5)

Sensor Type	Sensor Type Code	Sensor Specific Offset	Event	Description
Management Subsystem Health	28h	01h	Controller Access Degraded or Unavailable	The storage area used by the IPMC is potentially damaged or some data might have been lost.
		00h	Sensor Access Degraded	The FRUx sensor population could not be entirely merged in.
OEM Firmware Information (1)	COh	-	OEM Reserved	For development use.
OEM Firmware Information (2)	COh	-	OEM Reserved	For development use.
OEM IPMB-L Link Sensor	C3h	00h		Based on IPMB Link Sensor for single channel IPMB link Refer to PICMG 3.0 Specification.
		01h		Based on IPMB Link Sensor for single channel IPMB link Refer to PICMG 3.0 Specification.
		02h	IPMB-L Disabled	IPMB-L link is currently disabled.
		03h	IPMB-L Enabled	IPMB-L link is enabled.
OEM AdvancedTCA Board Reset Sensor	C4h	00h	Push Button	OEM event.
		01h	HW Power	Power error.
		02h	Unknown	Unknown PCI reset.
		03h	HW Watchdog	Hardware Watchdog or IPMC Watchdog.
		04h	Soft Reset	Soft reset.
		05h	Warm Reset	Warm Reset.
		06h	Reserved	Reserved
		07h	IPMI Command	Reset triggered by IPMI command: - chassis command -FRU command
		08h	Setup Reset	CMOS setup generated request.

Table 112. SEL Events Supported (Sheet 4 of 5)

Sensor Type	Sensor Type Code	Sensor Specific Offset	Event	Description
OEM Extended Data 2-3 Sensor	C5h	-	Generic Discreet Reading Type	OEM Extended Data 2-3. When name is "FIA" (FRU Initialization Agent). Sensor used to give the last error that occurred in the FRU InitAgent (FIA). In Event Byte 2: Error details on section: • Bit 7: unspecifiedError • Bit 6: notPresentError • Bit 5: multirecHeaderError • Bit 4: multirecDataError • Bit 3: timeout error • Bit 2: ipmcError • Bit 1: fruDataError • Bit 0: commonHeaderError In Event Byte 3: Error details on section: • Bit 7: reserved • Bit 6: reserved • Bit 5: SetPortState Not Supported • Bit 4: SetPortState Error • Bit 3: reserved • Bit 2: reserved • Bit 1: reserved • Bit 0: Match Error Not in single link matches.
OEM POST Value Sensor	C6h	00h-07h	POST Value Low Byte	OEM Event/Reading Type 0x78. On "System Firmware Progress" events current POST code is available through this sensor. Event data 2 = POST Low Nibble Event data 3 = POST High Nibble
		14h	Error Trig	Error trigger.
OEM FWUM Status	C7h	00h	First Boot After Upgrade	OEM Event/Reading Type 0x79. The IPMC has been updated and reset.
		01h	First Boot After Roll-back	The FWUM automatically rolled back the IPMC and the IPMC has been reset.
		02h	First Boot After Error (watchdog)s	The FWUM watchdog has expired and the IPMC has been reset.
		03h	First Boot After Manual Roll-back	The FWUM has rolled back the IPMC at the users's request and the IPMC has been reset.
		08h	Firmware Watchdog Bite, Reset Occurred	The FWUM has detected an IPMC internal watchdog reset.
		14h	Debug Mode Activated	Indicates the FWUM has entered debug mode.

Table 112. SEL Events Supported (Sheet 5 of 5)

Sensor Type	Sensor Type Code	Sensor Specific Offset	Event	Description
Power Supply OEM Power Good reading type	08h OEM Event/ Reading 0x77	00h	VCC Good 12V	When this bit is asserted, it means that Power Good is normal.
		01h	VCC Todd 5V	
		02h	VCC Good 3.3V	
		03h	VCC Good 2.5V	
		04h	VCC Good 1.8V	
		05h	VCC Core 1.5V	
		06h	VCC Good 1.2VV	
		07h	VCC Good Core	
AdvancedTCA FRU Hot Swap	F0h	07h	M7 FRU Inactive	Refer to PICMG 3.0 Specification.
		06h	M6 FRU Activation Request	
		05h	M5 FRU Activation In Progress	
		04h	M4 FRU Active	
		03h	M3 FRU Deactivation Request	
		02h	M2 FRU Deactivation In Progress	
		01h	M1 Communication Lost	
		00h	M0 FRU Not Installed	
IPMB Link Sensor	F1h	00h	IPMB A & B Disabled	Refer to PICMG 3.0 Specification.
		01h	IPMB A Enabled IPMB B Disabled	
		02h	IPMB A Disabled IPMB B Enabled	
		03h	IPMB A & B Enabled	

Note: The event log reports both correctable memory errors (single-bit) and uncorrectable memory errors (double-bit or multi-bit). However, some double-bit errors are correctable and some are not. If a double-bit error occurs that is correctable, it will be logged as a correctable error (single-bit).

Note: This IERR detection scheme differs in implementation on the MPCBL0010 SBC from “traditional” PC architecture. On the MPCBL0010 SBC, IERR is reported as part of SERR. When IERR occurs, the CPUis not automatically reset as on a traditional PC. You must use a BIOS or IPMC watchdog if your preference is to have the SBC reset itself automatically when this occurs.

10.4 IPMB Link Sensor

The MPCBL0010 SBC provides two IPMB links to increase communication reliability to the shelf manager and other IPM devices on the IPMB bus. These IPMB links work together for increased throughput where both buses are actively used for communication at any point. A request might be received over IPMB Bus A, and the response sent over IPMB Bus B. Any requests that time out are retried on the redundant IPMB bus. In the event of any link state changes, the events are written to the MPCBL0010 SBC SEL. IPMC monitors the bus for any link failure and isolates itself from the bus if it detects that it is causing errors on the bus. Events are sent to signify the failure of a bus or, conversely, the recovery of a bus.

10.5 Field Replaceable Unit (FRU) Information

The FRU information provides inventory data about the boards where the FRU information device is located. The part number or version number can be read through software.

FRU information on the MPCBL0010 SBC includes data describing the SBC as specified in the PICMG 3.0 requirements. Additional multi-records are added for the BIOS to write CPU information, BIOS version number, and PMC information to the FRU data correctly. This information is retrieved by the AdvancedTCA shelf manager (ShMC), enabling reporting of board-specific information through an out-of-band mechanism. Table 113 lists the definitions for the multi-record implemented by the firmware as part of the FRU data.

Note: The MPCBL0010 SBC provides 512 bytes of space to store custom FRU information. See Section 10.6, “Customizable FRU Area” for more information.

Table 113. FRU Multi-Record Data for CPU/RAM/PMC/BIOS Version Information

Variable	Size (bytes)	Data	Type
Manufacturer ID (Intel IANA number)	3	0x000157 (LSB first, MSB next)	Binary
Record Version	1	1	Binary
Type/Length	1	1	Binary
CPU Numbers	1	1	Binary
Type/Length	1	2	Binary
RAM Info	2	X (in units of 1 MByte)	Binary
Type/Length	1	(4 * XXX) + 1	Binary
Number of PMCs	1	0	Binary
Type/Length	1	0xFF	Binary
BIOS Version	63	yyyyyyyy	ASC-II
End of fields	1	0xC1	Binary

10.6 Customizable FRU Area

The **LinuxCustFru** utility is a Linux utility that runs directly on the MPCBL0010 SBC and is available on the Intel web site. This utility can be used to read data from a file and write it to the existing Field Replaceable Unit (FRU) information storage area on the MPCBL0010 SBC, or it can be used to purge any existing customer area in the FRU. The MPCBL0010 SBC provides 512 bytes of space for users to store custom FRU information. The FRU file complies with the IPMI Platform Management FRU Information Storage Definition v1.0.

10.6.1 LinuxCustFru Utility Usage

Running the **LinuxCustFru** utility with a FRU filename argument causes it to read in the customer area MRA record from the FRU file and write it to the FRU of the blade. If there is no valid customer area MRA record in the FRU file, nothing is written to the FRU (FRU is unchanged):

```
LinuxCustFru filename.fru
```

Running the **LinuxCustFru** utility with the "**-p**" argument, without a FRU filename, causes it to purge any existing customer area MRA record in the FRU area of the blade. If there is no valid customer area MRA record within the FRU on the blade, the FRU is left unchanged:

```
LinuxCustFru -p
```

Running the utility without arguments shows usage information and some examples of usage:

```
LinuxCustFru

Usage: ./LinuxCustFru [-p | fileName]
```

Where:

`fileName` = FRU file containing customer record (writes to the SBC). Omitting the filename clears the customer area of the FRU.

`-p`: purge / write customer area of FRU.

`-v`: verbose - show read/write data.

Examples:

```
./LinuxCustFru filename.fru
```

Reads customer area MRA record from filename.fru, writes it into the FRU of the SBC.

```
./LinuxCustFru -p
```

Purges customer area MRA record from the MPCBL0010 SBC FRU, if present.

10.6.2 FRU Customer Area

The FRU customer area consists of one or more OEM MRA records with a **Record Type ID** of '**0xC1'**. Platform Management FRU Information Storage Definition v1 provides more information about the format of the MRA records.

Multiple C1 records are needed to program more than 252 bytes of customer data into the FRU. The specification limits the size of the OEM records in the MRA to 255 bytes. Of these 255 bytes, the first three bytes are reserved by the specification for a three-byte manufacturer's ID, as described in the FRU Storage Definition.

The example FRU input file below implements the Customer Information Area with two Type-C1 OEM MRA records (in **FruCreate** format). These two records contain 313 bytes of customer data.

The headings **_SEE_COMMON** and **_SEE_MULTIREC** are required delimiters in the file. The common area is the FRU Common Header and the Multirec heading delineates the beginning of the MRA data.

The first byte of data is the Common Header Format version, which is version 1. Byte 6 is the MRA offset into the FRU. This value is calculated when the data is written to the FRU, but must be set to a non-zero value to indicate that MRA data is present. The checksum is in byte 8 and is '**0x100'** minus the modulus 256 summation of the first seven bytes and must be correct or the data will not be written to the FRU.

The MRA header is the first five bytes following the Multirec heading. Byte one is the record type and must be '**0xC1'**. The second byte is the record version and EOL indicator. This value is '**0x02**' for all records except the last record in the list. The Version/EOL byte must be set to '**0x82**' for the last MRA record in the input file. Failure to terminate the list causes the utility to abort the FRU update. Byte three is the length of the data record including the 3-byte Manufacturer ID, but not including the 5-byte record header. Bytes 4 and 5 are checksums of the record and the header respectively. The header checksum is '**0x100**' minus the modulus 256 summation of the first four bytes including the record checksum. The record checksum is '**0x100**' minus the modulus 256 summation of all the data bytes in the record, including the Manufacturer ID. In this example, 255 bytes of data follow the header in the first record.

Example 1. Input File:

```
_SEE_COMMON

   01  // Common Header Format Version

   00 // Internal Use Area Starting Offset (in multiples of 8 bytes)

   00  // Chassis Info Area Starting Offset (in multiples of 8 bytes)

   00  // Board Info Area Starting Offset (in multiples of 8 bytes)

   00  // Product Info Area Starting Offset (in multiples of 8 bytes)

   01  // MultiRecord Area Starting Offset (in multiples of 8 bytes)

   00  // Pad

   FE  // Common Header Checksum


_SEE_MULTIREC

   C1       // Record Type ID == 0xC1 == customer area OEM record

   02       // Version Information/EOL

   FF       // Record Length

   2E       // Record Checksum (zero checksum)

   10       // Header Checksum (zero checksum)
```

```
   51 31 00 // Manufacturer ID - 255 byte record length includes
Manufacture ID

   00 01 02 03 04 05 06 07// 252 bytes of data

   08 09 0A 0B 0C 0D 0E 0F

   10 11 12 13 14 15 16 17

   18 19 1A 1B 1C 1D 1E 1F

   20 21 22 23 24 25 26 27

   28 29 2A 2B 2C 2D 2E 2F

   30 31 32 33 34 35 36 37

   38 39 3A 3B 3C 3D 3E 3F

   40 41 42 43 44 45 46 47

   48 49 4A 4B 4C 4D 4E 4F

   50 51 52 53 54 55 56 57

   58 59 5A 5B 5C 5D 5E 5F

   60 61 62 63 64 65 66 67

   68 69 6A 6B 6C 6D 6E 6F

   70 71 72 73 74 75 76 77

   78 79 7A 7B 7C 7D 7E 7F

   80 81 82 83 84 85 86 87

   88 89 8A 8B 8C 8D 8E 8F

   90 91 92 93 94 95 96 97

   98 99 9A 9B 9C 9D 9E 9F

   A0 A1 A2 A3 A4 A5 A6 A7

   A8 A9 AA AB AC AD AE AF

   B0 B1 B2 B3 B4 B5 B6 B7

   B8 B9 BA BB BC BD BE BF

   C0 C1 C2 C3 C4 C5 C6 C7

   C8 C9 CA CB CC CD CE CF

   D0 D1 D2 D3 D4 D5 D6 D7

   D8 D9 DA DB DC DD DE DF

   E0 E1 E2 E3 E4 E5 E6 E7
```

```
E8 E9 EA EB EC ED EE EF

F0 F1 F2 F3 F4 F5 F6 F7

F8 F9 FA c1


C1              // Record Type ID == 0xC1 == customer area OEM record

82              // Version Information

40              // Record Length

60              // Record Checksum (zero checksum)

1D              // Header Checksum (zero checksum)

5A 31 00        // Manufacturer ID - 64 byte record length includes

                // Manufacture ID

40 41 42 43 44 45 46 47// 61 bytes of data

30 31 32 33 34 35 36 37

38 39 30 31 32 33 34 35

5A 59 58 57 56 55 54 53

52 51 50 4F 4E 4D 4C 4B

4A 49 48 47 46 45 44 43

42 41 40 39 38 37 36 35

34 33 32 31 C1
```

10.7 E-Keying

E-Keying is specified in the PICMG 3.0 requirements to prevent board damage, prevent mis-operation, and to verify fabric compatibility. The FRU data contains the board point-to-point connectivity record as described in Section 3.7.2.3 of the PICMG 3.0 specification.

Additional E-Keying is provided for connectivity between the AdvancedMC carrier and the AdvancedMC slots as described the in Section 3.9 and 3.7 of the AdvancedMC.0 RC.1.1 specification. The Set/Get AdvancedMC Port State IPMI commands defined by the AdvancedMC.0 specification are used for either granting or rejecting E-keys.

10.8 OEM IPMI Commands

This section documents the OEM-style IPMI commands implemented and supported on the MPCBL0010 SBC.

Command Name	NetFunction	Command
Reset BIOS Flash Type	3A	01h
SetBoardDeviceChannelPortSelection	3A	10h
GetBoardDeviceChannelPortSelection	3A	11h
GetBoardDevicePossibleSelection	3A	13h
Set Control State	3E	20h
Get Control State	3E	21h

10.8.1 Reset BIOS Flash Type

This command resets the processor and changes the BIOS bank select signal so the CPU boots using the redundant BIOS bank.

Table 114. Reset BIOS Flash Type

Request Data	1	BIOS checksum success/failure indication 00h - Checksum success 01h - Checksum failure
Response Data	1	Completion Code

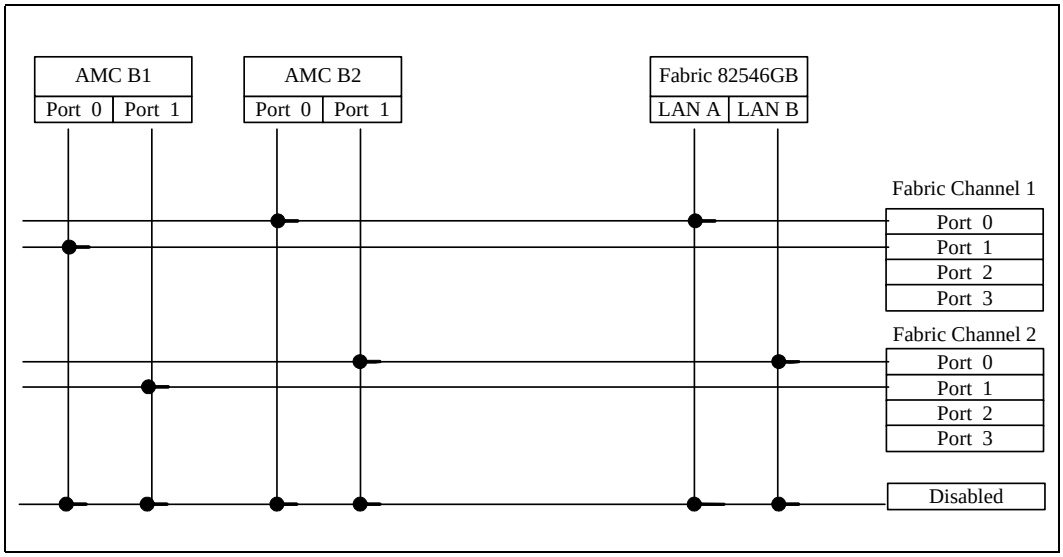
10.8.2 Board Device Channel Port Selection Identifiers

Table 115 lists the control identifiers that can be used in conjunction with Set/Get (HW) Board Device Channel Selection IPMI commands to query or set port connectivity on certain controls in the firmware for the AdvancedTCA channel routing.

Table 115. Channel Port Selection Identifiers

Control Description	Control Number
Base 82546 Gigabit Ethernet Lan A	0
Base 82546 Gigabit Ethernet Lan B	1
Fabric 82546 Gigabit Ethernet Lan A	2
Fabric 82546 Gigabit Ethernet Lan B	3
Fabric AdvancedMC B1 Port 0	6
Fabric AdvancedMC B1 Port 1	7
Fabric AdvancedMC B2 Port 0	8
Fabric AdvancedMC B2 Port 1	9
Reserved	0A-FFh

Figure 23. AdvancedMC Direct Connect Switch Block Diagram



10.8.2.1 SetBoardDeviceChannelPortSelection

This command selects the AdvancedTCA channel routing for the installed devices.

Table 116. SetBoardDeviceChannelPortSelection

Request Data	1–3	Intel IANA number (0x000157) LSB first, MSB last
	4	Device to select port (See Table 115, "Channel Port Selection Identifiers")
	5	Device channel/port selection 00h - Disabled (03h) - Reserved 04h - Back plane Base Channel 1 Port 0 05h - Back plane Base Channel 2 Port 0 (06h-07h) - Reserved 08h - Back plane Fabric Channel 1 Port 0 09h - Back plane Fabric Channel 1 Port 1 0Ah - Reserved 0Bh - Back plane Fabric Channel 1 Port 3 0Ch - Back plane Fabric Channel 2 Port 0 0Dh - Back plane Fabric Channel 2 Port 1 0Eh - Reserved 0Fh - Back plane Fabric Channel 2 Port 3 (10h - FFh) - Reserved
Response Data	1	Completion Code
	2–4	Intel IANA number (0x000157) LSB first, MSB last

10.8.2.2 GetBoardDeviceChannelPortSelection

This command returns the current device AdvancedTCA channel routing selection.

Table 117. GetBoardDeviceChannelPortSelection

Request Data	1-3	Intel IANA number (0x000157) LSB first, MSB last
	4	Device to select port (See Table 115, "Channel Port Selection Identifiers")
Response Data	1	Completion Code
	2-4	Intel IANA number (0x000157) LSB first, MSB last
	5	Device channel/port selection 00h - Disabled (03h) - Reserved 04h - Backplane Base Channel 1 Port 0 05h - Backplane Base Channel 2 Port 0 (06h-07h) - Reserved 08h - Backplane Fabric Channel 1 Port 0 09h - Backplane Fabric Channel 1 Port 1 0Ah - Reserved 0Bh - Backplane Fabric Channel 1 Port 3 0Ch - Backplane Fabric Channel 2 Port 0 0Dh - Backplane Fabric Channel 2 Port 1 0Eh - Reserved 0Fh - Back plane Fabric Channel 2 Port 3 (10h - FFh) - Reserved
	6	Device channel/port HW setting 00h - Disabled (03h) - Reserved 04h - Backplane Base Channel 1 Port 0 05h - Backplane Base Channel 2 Port 0 (06h-07h) - Reserved 08h - Backplane Fabric Channel 1 Port 0 09h - Backplane Fabric Channel 1 Port 1 0Ah - Reserved 0Bh - Backplane Fabric Channel 1 Port 3 0Ch - Backplane Fabric Channel 2 Port 0 0Dh - Backplane Fabric Channel 2 Port 1 0Eh - Reserved 0Fh - Backplane Fabric Channel 2 Port 3 (10h - FFh) - Reserved

10.8.2.3 GetBoardDevicePossibleSelection

This command returns the possible selections for the device received in parameters.

Table 118. GetBoardDevicePossibleSelection

Request Data	1-3	Intel IANA number (0x000157) LSB first, MSB last
	4	Device to select port (See Table 115, "Channel Port Selection Identifiers")

Table 118. GetBoardDevicePossibleSelection (Continued)

Response Data	1	Completion Code
	2-4	Intel IANA number (0x000157) LSB first, MSB last
	5-8	Device channel/port selection. Many connections can be set per device. - Bit Offset - (16-31) - Reserved 15 - Back plane Fabric Channel 2 Port 3 14 - Reserved 13 - Back plane Fabric Channel 2 Port 1 12 - Back plane Fabric Channel 2 Port 0 11 - Back plane Fabric Channel 1 Port 3 10 - Reserved 09 - Back plane Fabric Channel 1 Port 1 08 - Back plane Fabric Channel 1 Port 0 (06-07) - Reserved 05 - Back plane Base Channel 2 Port 0 04 - Back plane Base Channel 1 Port 0 (03) - Reserved 00 - Disable

10.8.3 Set Control State

This command sets the state of a control pin and overrides the control pin's auto state.

Table 119. Set Control State

Request Data	1	Control Number
	2	Control State 00h - De-assert 01h - Assert FFh - Don't change setting 03h - FEh - Reserved
Response Data	1	Completion Code

10.8.4 Get Control State

This command gets the state of a control pin.

Table 120. Get Control State

Request Data	1	Control Number
Response Data	1	Completion Code

10.8.5 Controls Identifier Table

The Controls Identifier Table lists the control identifiers that can be used with Set/Get Control State IPMI commands to query or set information on certain controls in the firmware.

Table 121. Controls Identifier

Control Description	Control Number
FWH Hub (for BIOS bank information)0	0
FWH 0 Write Protect	1
FWH 1 Write Protect	2
FWH 0 Top Block Lock	3
FWH 1 Top Block Lock4	4

10.9 Hot Swap Process

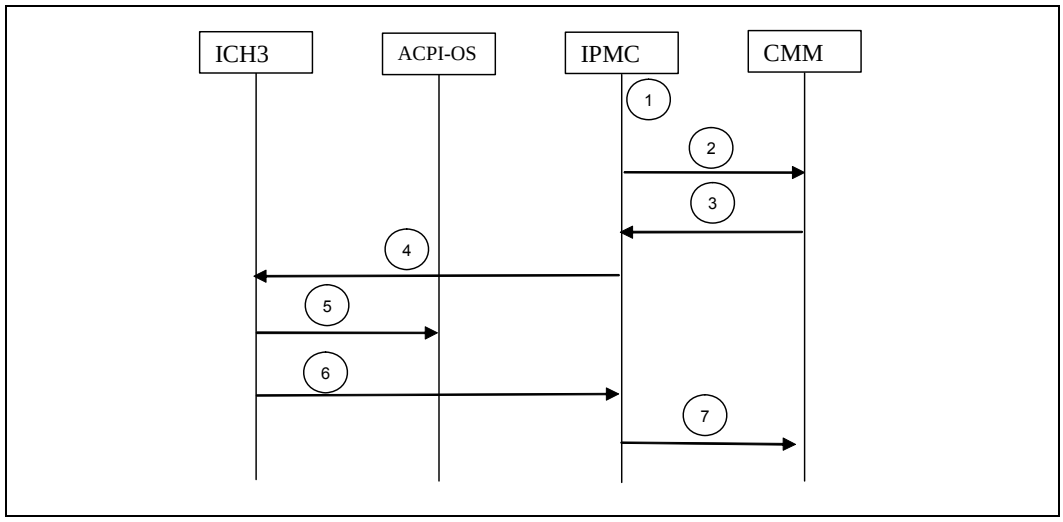
The MPCBL0010 SBC can be hot-swapped in and out of a chassis as defined in the AdvancedTCA specification. The onboard IPMC manages the SBC's power-up and power-down transitions.

The steps below illustrates this process:

1. The ejector latch is opened. The IPMC firmware detects the assertion of this signal.
2. IPMC sends a **Deactivation Request** message to the CMM or shelf manager. The M state moves from M4 to M5.
3. The board moves from M5 to M6 if the shelf manager grants the request.
4. The IPMC's ACPI timer starts if an ACPI-enabled operating system is loaded. Otherwise, it goes to Step 6 below.
5. The 'Power Button Status' register is set. It then asserts **SCI/SMI#** to the operating system.
   If the ACPI operating system is enabled, the SCI interrupt handler on the operating system is called. The interrupt handler clears the **PWRBTN_STS** bit. The operating system starts to perform a graceful shutdown.
6. The firmware de-asserts payload power and sets the IPMI locked bit before it transitions from the M6 to M1 state.

Note: If upper-level software moves the IPMC to M6, the same procedure is followed, starting with Step 4.

Figure 24. Hot Swap Process



10.9.1 Hot Swap LED

The MPCBL0010 SBC supports one blue Hot Swap LED, mounted on the front panel. This LED indicates when it is safe to remove the SBC from the chassis. The on-board IPMC drives this LED to indicate the hot swap state.

When the lower ejector handle is press inward, the hot swap switch embedded in the PCB l asserts a **HOT_SWAP_PB#** signal to the IPMC, and the IPMC moves from the M4 state to the M5 state. At the M5 state, the IPMC asks the AdvancedTCA shelf manager for permission to move to the M6 state. The Hot Swap LED indicates this state by blinking **ON** for about 100 milliseconds, followed by 900 milliseconds in the **OFF** state. This occurs as long as the SBC remains in the M5 state. Once permission is received from the AdvancedTCA shelf manager or higher-level software, the SBC moves to the M6 state.

The AdvancedTCA shelf manager or higher level software can reject the request to move to the M6 state. If this occurs, the hot swap LED returns to a solid **OFF** condition, indicating that the SBC has returned to the M4 state.

If the SBC reaches the M6 state, either through an extraction request through the lower ejector handle or a direct command from higher-level software, and an ACPI-enabled operating system is loaded on the SBC, the IPMC communicates to the operating system that the module must discontinue operation in preparation for removal. The Hot Swap LED continues to flash during this preparation time, just like it does at the M5 state. When main board power is successfully removed from the SBC, the Hot Swap LED remains lit, indicating it is safe to remove the SBC from the chassis.

Table 122. Hot Swap LED Signals

LED Status	Meaning
Off	Normal status
Blinking blue	Preparing for removal/insertion: Long blink indicates activation is in progress, short blink when deactivation is in progress
Solid blue	Ready for hot swap

10.10 AdvancedMC Module Activation

The MPCBL0010 SBC is configured to avoid activation of an AdvancedMC module during the BIOS POST or operating system boot sequence. The AdvancedMC module should be installed before BIOS POST, or after the operating system has completed loading. Within an ATCA chassis, there is often no defined order that the ShMC grants power to the FRU (SBC) and sub-FRU (AdvancedMC module) for an SBC. The MPCBL0010 SBC has a built in delay mechanism that prevents the activation process of the FRU and inserted sub-FRU into M3 state, which is **activation in progress** until the ShMC has granted power to all FRUs. This allows all FRUs to go to M4 at the same time, at which point the SBC BIOS will scan its devices. There is a timeout (30 second) if for some reason the ShMC does not power up an AdvancedMC module to ensure the SBC will still boot.

After the sychronization occurs, there is a "dead time" (2 seconds) where if a PCI-Express or SATA AdvancedMC module insertion is performed, the payload is reset. This "dead time" has been added to ensure the BIOS will see the AdvancedMC device at boot time.

The MPCBL0010 SBC also has a second "dead time" (45 seconds) used to avoid PCI - Express hot plug signaling during the operating system load. This delay is applied from the time the SBC goes to M4 state. There is no hot plug "attention button" during that delay. The IPMC asserts the "attention button" only after the delay to notify the operating system that a new device is ready to power.

10.10.1 Pre-Defined Resources for AdvancedMC Modules

In order to support AdvancedMC hot add, the SBC has to reserve resources that are not being used by a device when the SBC is booted. It is not possible for the SBC to know exactly what resources an AdvancedMC module that is hot-added may require before it is inserted. If the resources reserved by the SBC for the AdvancedMC module are adequate, then the AdvancedMC hot add will be successful. If an AdvancedMC module needs more resources (memory, IRQs, etc) than the SBC has reserved, then the AdvancedMC module will not work properly until the SBC is rebooted. If the hot-added AdvancedMC module does not use all of the resources that are reserved by the SBC, the reserved resources are left unused and cannot be used by any other component because they are still reserved.

For each AdvancedMC module slot, the following resources are reserved:

- 8 PCI buses
- IO: 8K
- Memory: 4000000h ;(64MB)
- Pre-fetch Memory: 8000000h ;(128MB)advanced

10.11 Temperature and Voltage Sensors

Temperature and voltage sensors are monitored by the MPCBL0010 SBC. These sensors are used to ensure that the MPCBL0010 SBC is operating at its pre-defined threshold limits. The sensors are categorized as follows:

- Lower Non-Critical
- Lower Critical
- Upper Non-Critical
- Upper Critical

If the lower critical or upper critical threshold is exceeded, it raises a major alarm. If the lower non-critical or upper non-critical threshold is exceeded, it raises a minor alarm.

Only critical thresholds which are exceeded turn on the solid red LED. However, for any events above, the IPMC forwards the events to the AdvancedTCA shelf manager to log into the SEL.

Table 123 lists the sensor numbers, normal values, and thresholds for all voltage and temperature sensors.

Table 123. Sensors and Thresholds (Version SDR 040)

Sensor Name	Description	Sensor Number	Normal Value	Lower Critical	Lower Non-Critical	Upper Non-Critical	Upper Critical
Temp Air Inlet		14h	19 C	-	-	50 C	55 C
Temp BoardA Area		15h	34 C	-	-	80 C	85 C
Temp CPU		16h	35 C	-	-	97C	102 C
Temp MCH		17h	37 C	-	-	80 C	85 C
Temp Vcore		18h	32 C	-	-	80 C	85 C
Temp BoardB Area		19h	27 C	-	-	70 C	85 C
Temp PXH		1Ah	33 C	-	-	70 C	85 C
Temp CPLD Area		1Bh	28 C	-	-	70 C	85 C
Temp 12vPS Area		1Ch	36 C	-	-	80 C	90 C
AMC DS75 Temp 1		51h	22 C				
AMC DSK DS75 Temp		50h	21 C				
Vcc +12V		20h	11.86 V	10.856 V	11.686 V	12.449 V	13.275 V
VCC +5V		22h	4.95 V	4.758 V	4.831 V	5.172 V	5.246 V
Vcc +3.3VSB		24h	3.33 V	3.136 V	3.200 V	3.424 V	3.472 V
Vcc +1.8V		26h	1.83 V	1.773 V	1.803 V	1.920 V	1.950 V
Vcc +1.5V		28h	1.50 V	1.421 V	1.450V	1.558 V	1.577V
Vcc +3.3V		29h	3.31 V	3.136 V	3.200 V	3.408 V	3.472 V
Vcc +2.5V		2Ah	2.48 V	2.373 V	2.410 V	2.583 V	2.619 V
Vcc VTT DDR		2Bh	1.19 V	1.137 V	1.161 V	1.234 V	1.244 V
Vcc Core Voltage		2Ch	1.07 V	0.872 V	0.891 V	1.156 V	1.176 V
Vcc -48V		2Eh	-51.34	-74.970 V	-72.135 V	-43.785 V	-37.800 V
+AMC DSK 12V		4Fh	10.94				
AMC DSK +3.3V		4Eh	3.38 V				

10.11.1 Processor Events

The processor asserts IERR as the result of an internal error. A thermal trip error indicates the processor junction temperature has reached a level where permanent silicon damage may occur. Upon **THERMTRIP** assertion, the IPMC powers down the boards. This event is logged in the SEL.

10.11.2 DIMM Memory Events

The MCH instructs the ICH to report memory parity errors via **SMI#**. The SMI handler extracts the error information (address) from the DRAM error registers in the MCH and logs it into the SEL on the shelf manager. The KCS interface performs error reporting to the IPMC. The BIOS sends a platform event message with the appropriate data to the IPMC, which logs the event to the SEL on the shelf manager. Correctable memory errors generate an SMI and are logged into the SEL. Normally, a board with non-correctable errors is likely to hang since the multi-bit error can cause the CPU to execute corrupted instructions. If the CPU executes corrupted instructions before executing the code to log the event, the event is not logged in the SEL.

10.11.3 System Firmware Progress (POST Error)

The BIOS is able to log both POST and critical events to the IPMC error log.

10.11.4 Critical Interrupts

In general, the system BIOS is capable of generating requests on the KCS interface to communicate with the IPMC for error logging, fault resilience, critical interrupts, and reading/writing inventory of CPU and RAM information to the IPMC. Two LPC interfaces are available for the BIOS to communicate with the IPMC. The BIOS uses the SMS interface for normal communication with the IPMC and the SMM interface when executing code under SMM mode.

PCI error handling is implemented in the MPCBL0010 SBC as follows:

1. The MCH sends a parity error/system error (**PERR/SERR**) message over the hub interface to the ICH notifying it that an error occurred.
2. The ICH generates an **SMI#** interrupt when it receives a **PERR/SERR** message.
3. The SMI handler checks the error status registers of the CPU/MCH until it identifies the source and type of the error.
4. The handler sends a message to the IPMC via the KCS interface, causing it to log the error in the IPMC and then forward the event to the shelf manager to log it into the SEL.

10.11.5 System ACPI Power State

The MPCBL0010 SBC supports ACPI functionality with support for the sleep states S0, S4, and S5. The IPMC sends out a hot swap event message to the shelf manager requesting deactivation. On successful reception of a deactivation message from the shelf manager, the FRU enters M1 power state and remains in this state.

Under conditions where an ACPI enabled operating system is in S4/S5 sleep state, the chipset could de-assert, requiring the IPMC to attempt an AdvancedTCA power state transition to the M4 state (through M2, M3).

The ACPI capabilities of an operating system are communicated by the BIOS to the IPMC at initialization. An OEM-style IPMI command is sent by the BIOS for this purpose. This command is sent by the BIOS every time an operating system is

initialized. The IPMC firmware defaults to no ACPI until this command is received with proper data in the request to indicate the operating system is either ACPI-enabled or -disabled. This command is only executable over the SMS channel.

10.11.6 IPMB Link Sensor

The MPCBL0010 SBC provides two IPMB links to increase communication reliability to the shelf manager and other IPMI devices on the IPMB bus. These IPMB links work together for increased throughput where both buses are actively used for communication at any point. A request might be received over IPMB Bus A, and the response is sent over IPMB Bus B. Any requests that time out are retried on the redundant IPMB bus. In the event of any link state changes, the events are written to the SEL. The IPMC monitors the bus for any link failure and isolates itself from the bus if it detects that it is causing errors on the bus. Events are sent to signify the failure of a bus or, conversely, the recovery of a bus.

10.11.7 FRU Hot Swap

The hot swap event message conveys the current state of the FRU, the previous state, and a cause of the state change as can be determined by the IPMC. Refer to the *PICMG 3.0 specifications* for further information about the hot swap state.

10.12 Reset

The following sections describe the two types of reset requests and the boot relationships among them. The two types of reset requests available on the MPCBL0010 SBC are:

- Hard reset request (always results in a cold boot)
- Warm reset request (can result in either a warm or cold boot)

A hard reset request occurs whenever the processor Reset line is asserted and then deasserted. A soft reset occurs whenever an assertion occurs on the processor Init line. Whenever a soft reset request occurs, the BIOS checks two memory locations to determine whether to initiate a warm boot while leaving main memory intact or a cold boot that clears memory.

The reset button on the front panel is an input to the IPMC. There are also IPMI commands to reset the board and change power states through the software. However, the reset button is a last resort because the user must be physically present at the chassis to reset the board.

Table 124. Reset Actions

Reset Action	System Function	Memory Status
Warm boot	Partial restart	Preserves memory above 8MB boundary.
Cold boot	Full restart	Functionally equivalent to a hard reset.

The type of reset also affects the BIOS POST. There are two possibilities:

- A hard reset (or power-up) does a full BIOS POST.
- In warm reset, the memory count/test/clear is skipped. Also, check-point 0D0h to 0D4h boot block is skipped.

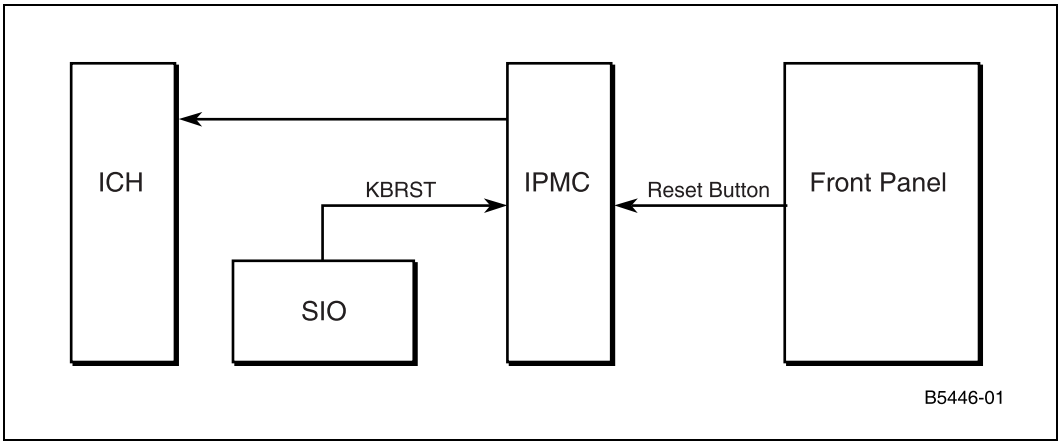
10.12.1 Warm Reset

A warm reset occurs when the processor boots after a soft reset request. To qualify as a warm boot, the reset counter located at 40h:D0h must be non-zero (by default, the reset counter and reset flag are initialized to 10 and 1234h by the BIOS after a cold boot). Execution starts at the reset vector. The BIOS initializes and configures all devices except for memory. Memory contents remain intact except for the first 8 MB. The BIOS uses the first 8 MB during POST, but does not modify the reset flag or the reset counter. MCH is not reset, allowing DRAM refresh to continue during the warm boot.

On every warm boot, the BIOS automatically decrements the reset counter by one. When the reset counter reaches zero and the soft reset is initiated, a cold boot occurs instead of a warm boot

The front panel reset button is connected to IPMC. If the button is pushed, the IPMC outputs an active signal to the ICH's RCIN to perform CPU init as the warm reset.

Figure 25. Warm Reset Block Diagram



Note: The KBRST (keyboard reset) can be used to cause a warm reset and will be detected by the IPMC.

10.12.2 Hard Reset

Any reset that does not meet the configuration described in Section 10.12.1, "Warm Reset" is classified as a cold boot. Execution starts at the reset vector, and the BIOS initializes and configures all devices, including memory subsystem, as if a hard reset had occurred. During a cold boot the BIOS initializes the warm reset counter to 10h and clears the reset flag to 1234h. Software can then read the Reset flag to determine the type of reset.

10.13 Field Replaceable Unit (FRU) Information

The FRU information provides inventory data about the boards where the FRU Information Device is located. The part number or version number can be read through software.

FRU information in the MPCBL0010 SBC includes data describing the MPCBL0010 SBC board as specified in the PICMG 3.0 requirements. Additional multi-records are added for the BIOS to write CPU information, and the BIOS version number to FRU data correctly. This information is retrieved by the shelf manager (AdvancedTCA ShMC), enabling reporting of board-specific information through an out-of-band mechanism.

Below is example of MPCBL0010 SBC FRU information as reported by the Intel CMM:

```
bash-2.04# cmmget -l blade5 -t fru -d all

FRU NAME: IPM Controller

FRU TYPE: Board

DESCRIPTION: MPCBL0010xxx

MANUFACTURER: Intel Corporation

PART #: C68372-100

SERIAL #: 1000603009

MANUFACTUREDATE: Tue Sep 27 02:19:04 2005


FRU File ID: FRUWR752BLA-04-14

FRU NAME: IPM Controller

FRU TYPE: Product

DESCRIPTION: MPCBL0010xxx

MANUFACTURER: Intel Corporation

MODEL: MPCBL0010xxx

PART #: C90917-001

SERIAL #: 1000603009

REV. LEVEL:

MANUFACTUREDATE:
```

10.14 IPMC Firmware Code

IPMC firmware code is organized into boot code and operational code, both of which are stored in a flash module. Upon an IPMC reset, the IPMC executes the boot code and does the following:

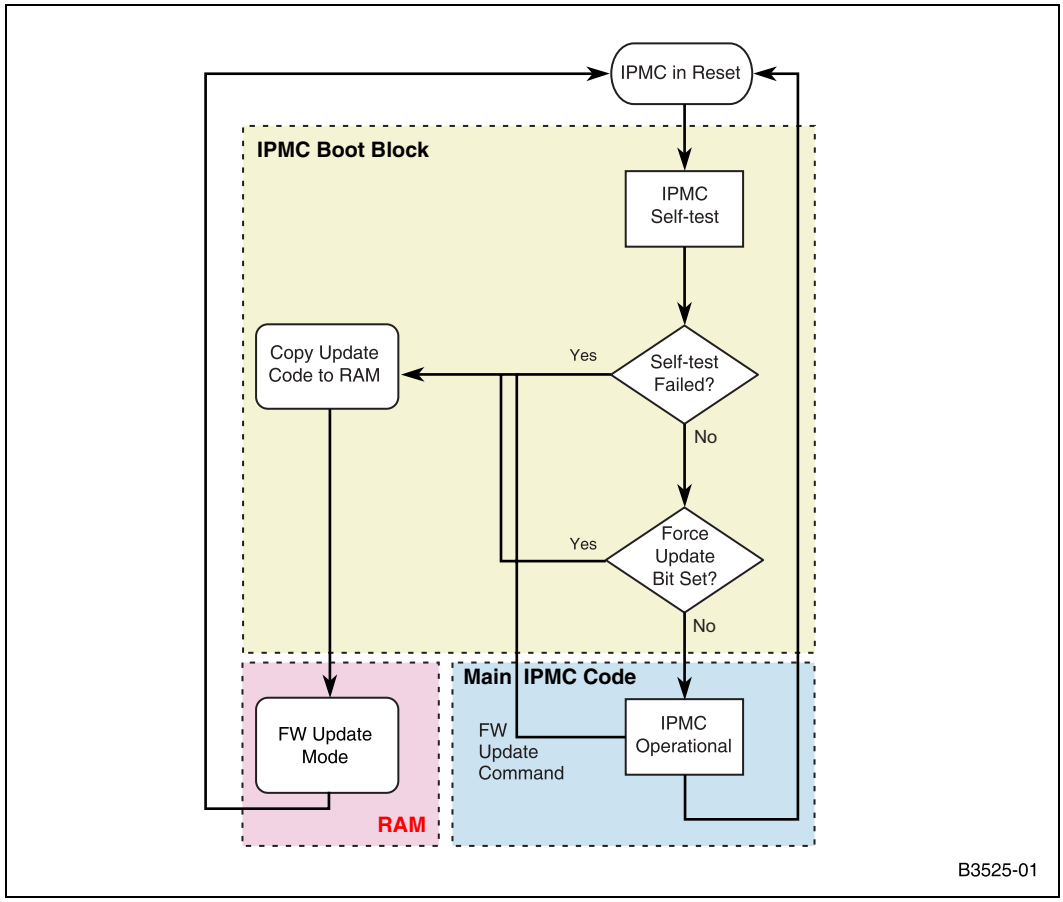
1. Performs self tests to verify the status of its hardware and memory
2. Sets up the internal real-time operating system (RTOS)
3. Performs a checksum of the operational code

Upon successful verification of the operational code checksum, the firmware jumps to the operational code.

When the firmware enters firmware (FW) update mode, the operational code uses a special branch, Software Interrupt, to jump to the FW update code in the boot block. Once in FW update mode, the update code is copied into RAM, then the firmware jumps to the code in RAM to execute. The firmware update code cannot execute out of flash while the flash is being updated.

Figure 26 illustrates the firmware code process.

Figure 26. IPMC Firmware Code Process



11.0 Serial Over LAN (SOL)

Serial over LAN (SOL) is a packet format and protocol defined in the IPMI v2.0 specification for transmitting serial port data over Ethernet using IPMI over LAN (RMCP+) messages. This two-way redirection of a blade's serial port data over Ethernet is independent of the operating system or any applications executing on it. The BIOS also supports redirection of its console over serial port, which can be redirected over the network for remote access.

The SOL mechanism, coupled with a SOL client utility executing on a remote node, enables viewing of serial port data from any IPMI v2.0-based, SOL-enabled blade, and thus provides a virtual remote terminal server for accessing a blade's serial port character stream.

11.1 References

- *Intelligent Platform Management Interface Specification v2.0*. dated June 1, 2004
- *AES - Advanced Encryption Standard.* http://csrc.nist.gov/publications/fips/fips197/fips-197.pdf

11.2 SOL Architecture

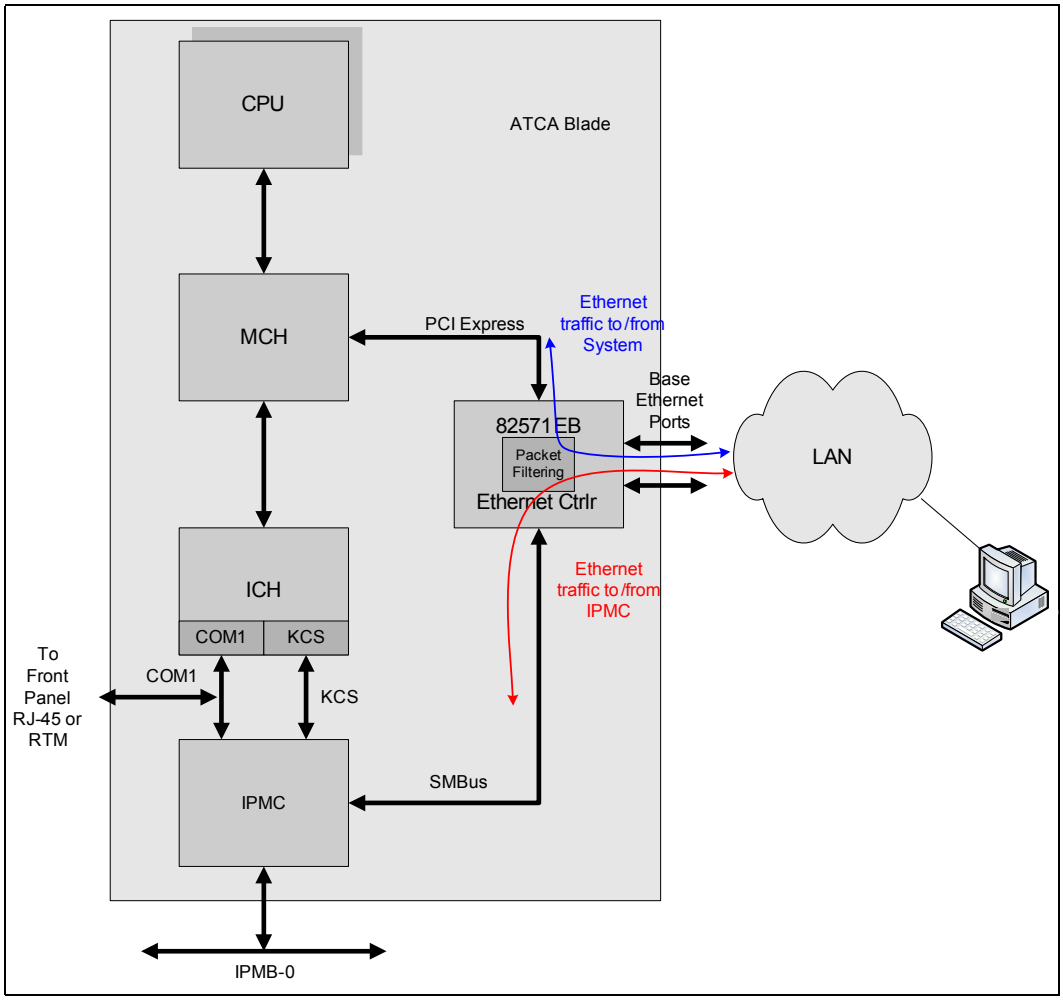
The SOL implementation on the MPCBL0010 Single Board Computer is based on the definition in Section 15 of the IPMI v2.0 specification.

11.2.1 SOL Implementation

Serial over LAN (SOL) enables suitably designed blades and servers to transparently redirect a serial character stream of a baseboard UART to/from a remote client via LAN over RMCP+ sessions. This capability enables users at remote consoles to access the serial port of a blade/server and interact with a text-based BIOS console, operating system, command line interfaces, and serial text-based applications.

Figure 27 is a block diagram of the SOL implementation on the blade:

Figure 27. SOL Block Diagram



This architecture requires the following three components to perform Serial over LAN operations.

1. SOL-capable firmware executing on the Intelligent Platform Management Controller (IPMC)
   The IPMC also provides a dedicated SMBus connection to the base interface Ethernet controller. This connectivity is not shared with IPMB-0 or any other I^2C/SMBus/IPMB connections that the IPMC may provide on the blade for hardware management.
2. The base interface Ethernet controller, which provides a sideband interface port to the IPMC over which SOL traffic is redirected
   The Ethernet controller also filters packets based on MAC address, RMCP port number, or IP address and forwards the packets to the IPMC over the sideband interface.
3. Client software running on any remote node that has LAN access to the blade whose serial port data is to be accessed
   The IPMC is responsible for controlling the serial hardware MUX, the transformation

of serial data to and from network packets, and the transmission and reception of SOL network packets through the Ethernet controller sideband interface port.

11.2.2 Architectural Components

11.2.2.1 IPMC

As shown in the block diagram in Figure 27, the IPMI controller on the blade provides a UART interface to the blade's serial port (COM1). This interface is used by the IPMC firmware to write data to the blade's serial port or to receive the blade's serial port data written by the BIOS or the operating system. The serial port can be connected to either the IPMI controller or to RJ-45 connector(s) on the front panel or rear transition module. Switching the serial port between the front panel/rear transition module and the IPMC UART port is controlled by the IPMC firmware.

The IPMC also provides a dedicated SMBus connection to the Ethernet controller, whose ports are connected to the base Ethernet interface.

The Keyboard Controller Style (KCS) interface is used for interaction between the IPMC firmware and software executing on the OS (for example, OpenIPMI or OpenHPI) by sending/receiving IPMI messages, and does not play a role during SOL communication. The KCS interface, however, can be used for SOL-related IPMC configuration, as described below.

11.2.2.2 Ethernet Controller

The Ethernet controller provides an advanced pass-through mode of operation where the controller allows the on-board IPMC to communicate over the Ethernet ports using a sideband interface port.

The Ethernet controller is available with standby (management) power, so that it is possible to view the initial serial port data written by the BIOS or the OS.

11.3 Theory of Operation

11.3.1 Front Panel Serial Port or Rear Transition Module

By default, the serial console is connected to the serial port connector(s) on the front panel and rear transition module (if available).

If serial cables are connected to both the front panel and the rear transition module connectors, both connections will be active. However, only one user is allowed to use the serial session.

11.3.2 Serial Over LAN

The IPMC firmware is pre-configured at manufacturing time with default serial port settings (baud rate, parity bits, data bits, stop bits, flow control), user name and password for RMCP+ sessions. The SOL feature, however, is disabled by default.

The IP address to be used by IPMC can be configured during initial setup of the blade in the system.

The IP address, once configured by the reference script provided, is stored in a non-volatile memory and is persistent across IPMC update and payload resets. The IP addresses are assigned to the IPMC independently of the host (OS) IP addresses and they need not match. The IP addresses used by the OS are not visible to the IPMC.

To start SOL communication, the user invokes the SOL client utility with the IP address of the blade and a series of authentication parameters (username, password, privilege level, cipher suite, etc). The IPMI v2.0 specification allows for AES encryption algorithms for encryption of payload data sent over the network, including AES-128, which uses 128-bit cipher keys.

The SOL client utility initializes the RMCP+ session with the blade and activates SOL. When authentication is successfully completed, the IPMC firmware collects serial port data from the blade's serial port, formats it into network packets, and forwards it to the SOL client utility over the SOL session. The SMBus sideband interface port between the IPMC and base interface Ethernet controller is used for this purpose. The SOL client utility receives the packets, extracts the serial port data, and displays it on the screen. The IPMC extracts the serial port data received from the SOL client utility and writes it to the serial port of the blade. This allows network redirection of the blade's serial port data stream that is independent of the host OS or BIOS. The Ethernet controller plays a critical role in redirecting the packets meant for the IPMC, based on receive filters.

The maximum baud rate supported by the IPMC for SOL is 38.4 kbps. The default SOL baud rate is 9.6 kbps.

Note: The BIOS default baud rate is 9.6 kbps. If SOL is configured for a different baud rate, the BIOS output is not seen using the SOL client until the BIOS baud rate is set to match the SOL client baud rate.

11.4 Serial Over LAN Client

The SOL client establishes an IPMI-over-LAN connection with the IPMC on the blade. It then activates SOL, which switches the board hardware to redirect serial traffic to the IPMC instead of the serial port. Any outbound characters from the UART now are packetized by the IPMC and sent over the network to the SOL client via the sideband interface port. Conversely, any input on the SOL client is packetized by the client and sent over the network to the IPMC, which is responsible for conveying it to the UART.

SOL data is carried over the network in UDP datagrams. IPMI 2.0 defines the specification of packet formats and protocols for SOL. As per the IPMI 2.0 specification, RMCP+ is the packet format when the Payload Type is set to "SOL". Authentication, integrity, and encryption for SOL are part of the RMCP+ specification.

The ipmitool client (version 1.8.7 or higher) is required. The ipmitool is open source. For more information, refer to Section 11.8, "Setting up a Serial Over LAN Session"

This client needs to be downloaded and compiled on the Linux* operating system of your choice.

11.5 Reference Configuration Script

Intel provides an SOL reference script (***reference_cfg***) that sets up the various parameters required for SOL operation.

The SOL configuration reference script (***reference_cfg***) sends a sequence of IPMI commands to configure an SBC to enable the SOL feature. This script can be executed on a payload CPU for local configuration or on a node that has network connectivity to the target SBC. Without this IPMC configuration, the SOL client utility is not be able to communicate with the SBC. This script is provided to customers as an example of a semi-automated method of configuring systems and is not meant for use in production environments.

The ipmitool utility enables a user to establish an RMCP+ session with the SBC's management controller and activate two-way SOL packet communication.

Note: While ipmitool is a supported utility, *reference_cfg* is provided as an unsupported reference to be modified by customers to suit their specific environments and integration needs.

11.6 Supported Usage Model

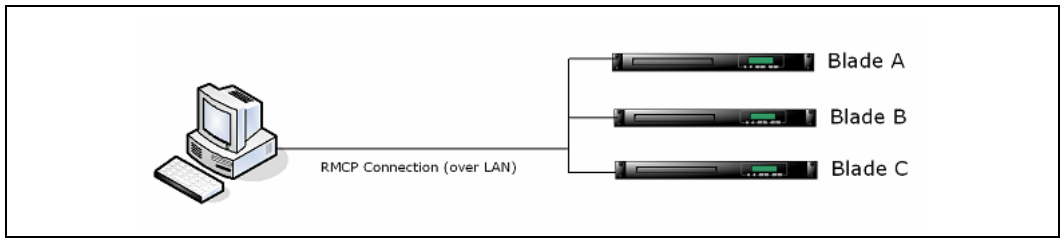
Customers are expected to use SOL to accomplish the following:

- BIOS console redirection
- Remote terminal access for OS setup and viewing text console output

The ipmitool utility runs on a remote network node and communicates over the LAN interface. The remote node and the target SBC may be on the same subnet or on different subnets.

The reference script can be run on the remote node.

Figure 28. Reference Script Running on a Remote Node, Communicating over the LAN



Note: The machine or “remote node” running ipmitool may also be an MPCBL0010 SBC within the same chassis.

11.6.1 Configuring the Blade for SOL

In order to configure a blade for SOL, the system on which the configurator is installed (typically the remote node) needs to establish an RMCP connection with the SBC. The configurator sends commands and configuration settings to the SBC in order to configure and enable SOL operation. In order to configure a blade for SOL, *reference_cfg* must run either on the same blade as the IPMC and communicate via the KCS interface, or on a remote node. In the latter case, the script sends IPMI messages over the LAN to the SBC shelf manager, which in turn bridges data to the IPMC’s IPMB-0 interface.

The minimal per-blade configuration that must be set up includes the following:

- an IP/MAC address, subnet mask, default gateway
- ARP configuration
- user ID and password to authenticate access
- channel, user, payload, and SOL privilege levels

The configuration utility is referring to the ***reference_cfg*** script described above.

11.7 Reference Script (reference_cfg)

11.7.1 SOL Configuration Reference Script (*reference_cfg*)

The reference script can run with no special setup. The script uses built-in bash commands as well as `grep` and `awk`. The environment in which the script runs must have bash installed at `/bin/bash` (or a symbolic link at that location), and must include `grep` and `awk` in the path.

The reference script is implemented as two separate bash files: ***reference_cfg***, which contains the necessary IPMI commands, and *reference_func*, a library of supporting functions. When ***reference_cfg*** runs, it looks for the library in the following paths in the order listed:

1. the current working directory
2. `/usr/lib/sbcutils`
3. `/home/scripts`

If ***reference_cfg*** cannot find the library in any of these locations, it terminates with an error message.

When running the reference script on a remote node over RMCP via a shelf manager RMCP to IPMB, bridging must be enabled on the shelf manager. In the case of the Intel NetStructure MPCMM0001/0002 Chassis Management Module, the following command enables RMCP:

```
# cmmset -d rmcpenable -v 1
```

RMCP and KCS communication requires the OpenIPMI application library, version 1.4 or later. KCS communication further requires the OpenIPMI driver.

11.7.2 Default Behavior

To configure a blade for SOL communications, many configuration parameters are required (for example, user information, channel parameters, LAN parameters, SOL parameters). Most of the values used for configuration appear as hard-coded default values.

11.7.3 SOL User Information

SBCs from Intel implement four different users, User1 through User4. User1 has a null username that is not editable. The script configures User2 as specifically enabled for SOL payloads.

The user name is “solusername”, zero-padded to a length of 16 bytes as per the IPMI 2.0 specification. The password is “soluserpassword”, zero-padded to 20 bytes as per the IPMI 2.0 extension.

11.7.4 LAN Parameters

The reference script configures IPMI channel 1. The IPMI channel number used by *reference_cfg* can be changed to any IPMI LAN channel supported by the target SBC.

The configured channel must be a base interface, not a fabric interface. On the MPCBL0010 SBC, IPMC channel 1 corresponds to the Ethernet interface eth1.

Since *reference_cfg* uses IPMI channel 1, for any SBC, eth0 will be routed to a switch in slot 7 (This may vary with different chassis implementations.)

IP and MAC addresses supplied to the IPMC are specified on the command-line as shown in Table 125. The IP source is set to "***static***" and the subnet mask is set for a class C subnet. Gateway IP and MAC addresses should be specified with the command to enable RMCP communication across subnets. If the IP or MAC address options are missing from the command line, these parameters are not be changed on the IPMC.

The IP, MAC, gateway, and gateway MAC parameters are optional. If these settings have been previously configured and have not changed, it is not necessary to supply them on the command line every time the script is executed.

The IP and MAC address for an IPMC can be obtained from the operating system running on the SBC with the "ifconfig" command. In the output from this command, the field "***inet addr***" contains the IP address; the field "***HWaddr***" contains the MAC address.

The IP and MAC address of the subnet's gateway can be obtained from the operating system running on the SBC by executing the "**route**" command to obtain the host name of the gateway, then by executing the command "arp -a gateway_hostname" to obtain the gateway's IP address and MAC address. (If needed, execute the command "**ping gateway_hostname**", then re-execute the "**arp**" command to obtain the IP and MAC addresses.)

Gratuitous ARPs generated by the BMC are enabled and sent every three seconds.

The md5 authentication type is enabled for all privilege levels.

11.7.5 SOL Parameters

The SOL payload type is enabled with a privilege level of operator. Neither payload encryption nor payload authentication is forced. Serial characters are accumulated for as long as 40 milliseconds or as many as 50 characters. SOL packets are retried every 100 milliseconds, up to seven times. The default SOL baud rate is 9600 bps.

11.7.6 Channel Parameters

Channel 1 is configured as "always available", meaning that all RMCP traffic to the SBC LAN adaptor is routed exclusively to the IPMC and not to system software.

For channel 1, User2 is enabled for general IPMI messaging (as opposed to SOL-only messaging). User2 has a privilege level of operator on channel 1.

11.7.7 Command Line Options

Table 125 lists the available command-line options for the reference script.

Table 125. SOL Configuration Reference Script Command-line Options

Option	Meaning
-h	"help" - display usage, version number and a list of options. When this option is specified, all other options are ignored.
-l	"location" - specifies what blade to configure. When running on an Intel NetStructure MPCMM0001 Chassis Management Module (CMM), this value should be one of ["blade1"..."blade14"]. When running on a remote node, this value should be the IPMB address. When running on the local processor, this option is ignored.
-i	"IP" - specifies what IP address should be used to configure the blade. The IP address should be given in the form ###.###.###.### where "###" is a decimal number from 0 to 255
-j	Specifies the IP address of the subnet's gateway.

Table 125. SOL Configuration Reference Script Command-line Options

Option	Meaning
-n	Specifies the MAC address of the subnet's gateway.
-g	"Gratuitous ARPs" - Turns on gratuitous ARPs. If this switch is not supplied, then IPMC-generated ARP responses are enabled instead.
-v	"Version" - displays the version and quits
-I	"Interface" - specifies the interface used to commuicate to the IPMC. Must be one of kcs, lan, or ipmb.
-m	"MAC" - specifies what MAC address should be used to configure the blade. The MAC address is given in the form of `##:##:##:##:##:##`
-H	RMCP-IP - IP address or host name fo the shelf manager used to bridge RMCP messages to IPMB
-U	"User" - specifies the username for establishing the RMCP sessions. If not specifed, the default value `root` is used.
-P	"Password" - password for establishing RMCP sessions. If not specified, the default value `cmmrootpass` is used.
-A	"Authorization" - authorization type for establishing the RMCP sessions. One of {`none|straight|md2|md5`}
-?	Print the message and quit

11.8 Setting up a Serial Over LAN Session

11.8.1 Target Blade Setup

The target blade is the SOL blade that sends the serial data to the client.

Ensure that the MPCBL0010 SBC has the following firmware/OS versions loaded:

- IPMC Firmware 4.56_R006 or later
- BIOS 045.P04 or later
- sbcutilities 1.2.0.10 or later
- MontaVista 4.0 LSP, RHEL 4.0 U3

11.8.1.1 BIOS Configuration

Configure the target blade BIOS baud rate so that it is set to 9600.

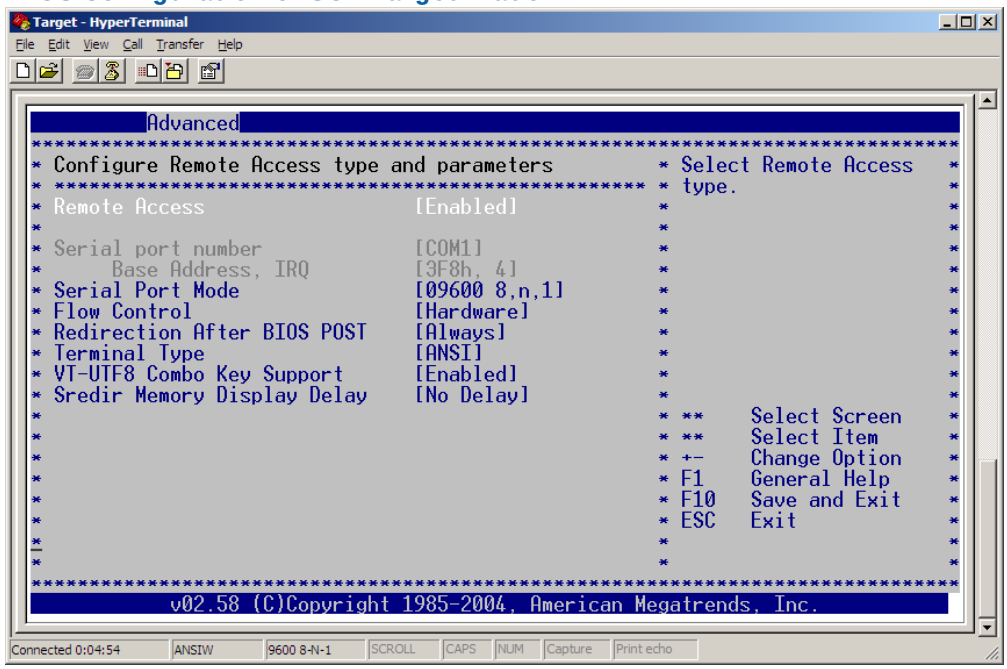
Note: The SOL target blade can operate at baud rates of 9600, 19200, and 38400 only. All examples in this document use a baud rate of 9600.

Configure the BIOS configuration of SOL target blade as follows:

1. When the blade starts booting, press **F4** from HyperTerminal (or an equivalent terminal program) to enter the BIOS setup menu.
2. Choose the **Advanced** menu.
3. Choose **Configure Remote Access** menu.
   Change the **Flow Contro**l parameter to "***Hardware***".
4. Change **Serial Port Mode** to the 9600 baud rate if it is not already set to that speed.
5. Press **Esc**.
6. Choose **Save and Exit**.

Note: If the default BIOS baud rate is changed to any baud rate other than 9600, then the *reference_cfg* script needs to be changed to match the same baud rate.

Figure 29. BIOS Configuration of SOL Target Blade



11.8.1.2 Operating System Configuration

Configure the operating system baud rate to match the BIOS baud rate.

1. For MontaVista:
   a. Edit the `/etc/lilo.conf` file.
   b. Type `vi /etc/lilo.conf`.
   c. Set the boot loader baud rate by adding/modifying a line as follows:
      `serial=0,9600n8r`
   d. Change the append line to read as follows:
      `append="ip=off console=ttyS0,9600n8r panic=5"`

Note: Hardware flow control is required. (hence the "**r**" option)

   e. Once completed, save the `lilo.conf` file using the command **wq!**
   f. On the serial console, type `lilo`

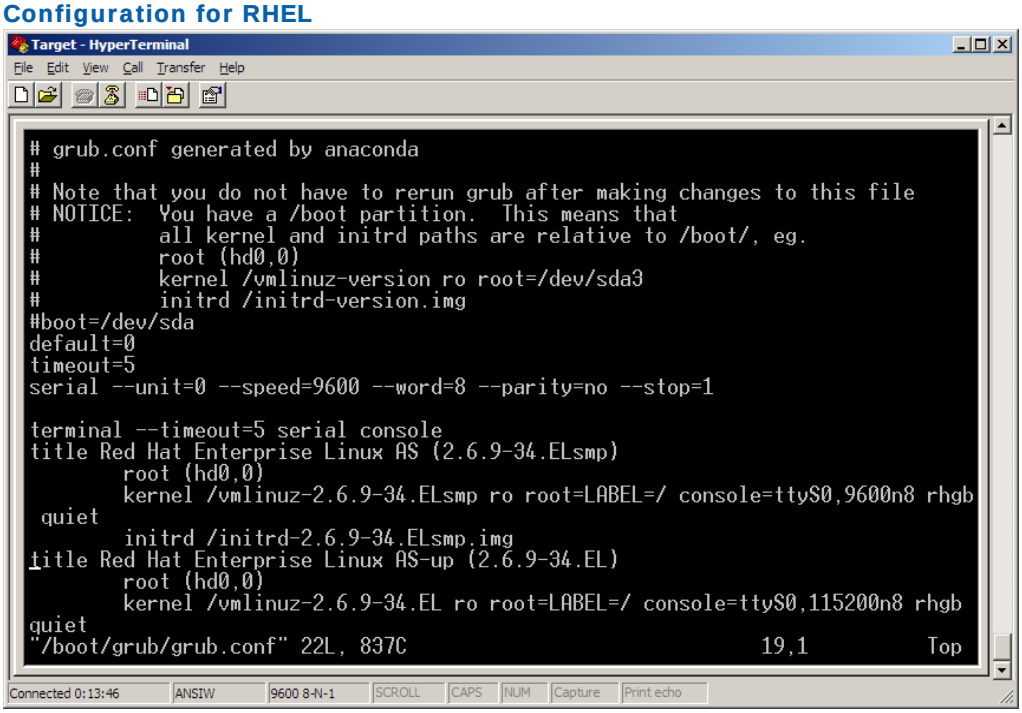
2. For RedHat* RHEL4 U3:
   a. Edit the `/boot/grub/grub.conf` file.
   b. Type `vi /boot/grub/grub.conf`
   c. Change the serial parameter to read
      `serial --unit=0 --speed=9600 --word=8 --parity=no --stop=1`

d. Change the kernel line to read
`kernel /vmlinuz-2.6.9-34.ELsmp ro root=LABEL=/ console=ttyS0,9600n8 rhgb quiet`

Here you are adding `console=ttyS0,9600n8 rhgb quiet` to the end of your kernel line if it does not already exist.

e. Type `:wq!` to save the changes.

Figure 30. Configuration for RHEL



3. Ensure that at least one `agetty` process is running on the serial port.
To do this, modify the file `/etc/inittab. vi /etc/inittab`
Change the system console by adding/modifying the "**co**" service.

   a. For MontaVista:
   `co:2345:respawn:/sbin/agetty ttyS0 CON9600 vt102`

   b. For RHEL:
   `co:2345:respawn:/sbin/agetty ttyS0 9600 vt100-nav`

4. Reboot the blade.
Change HyperTerminal to `9600, 8, n, 1, n` to make sure the BIOS, bootloader, and OS come up at 9600 baud.

5. Optionally, if needed, configure the host OS IP address now.
This IP address can be the same as the IP address that will be assigned to the IPMC controller on the blade or different.
The IP address of the host OS and IPMC should be on the same subnet. For the MPCBL0010 SBC blade, use **Eth1** for base interface port A.

   To configure IP on MontaVista:
   `# vi /etc/network/interfaces`

To configure IP on RedHat RHEL:

```
# vi /etc/sysconfig/network-scripts/ifcfg-ethN
```

11.8.1.3 sbcutils RPM Installation

1. Install the sbcutils RPM. For complete details on the sbcutils installation, refer to the sbcutilities RPM install procedure on the MPCBL0010 SBC product page
   a. Copy the RPM to the target blade. Ensure that the RPM copied is for the particular OS installed on the target blade.
   b. Check the version of sbcutils installed:
      `rpm -q sbcutils`
   c. If a previous version of the sbcutils RPM is installed, remove it by using this command:
      `rpm -e sbcutils`
   d. install a new version of sbcutils
      For MontaVista* 3.1
      `rpm -ivh sbcutils-1.3.0-3.i386-mv31.rpm`

      For MontaVista* 4.0
      `rpm -ivh sbcutils-1.3.0-3.i386-mv40.rpm`

      For Wind River* PNE 1.2
      `rpm -ivh sbcutils-1.3.0-3.i386-wr12.rpm`

      For RedHat* RHEL U3
      `rpm -ivh sbcutils-1.3.0-3.i386-rhel4.rpm`

11.8.1.4 Execute the reference_cfg Script

1. For RedHat* RHEL only: Before using the `reference_cfg` script, start the IPMI drivers.
   In MontaVista, the IPMI drivers start automatically.

   Start the IPMI drivers by issuing the following commands:
   `# /etc/init.d/ipmi start` (This will start IPMI drivers for this particular session only.)
   `# chkconfig ipmi on` (Tthis will start IPMI drivers by default on the next reboot.)

The following note applies to the commands in step 2 below.

Note: When the SOL client and SOL target are behind the same gateway, the "`<Gateway MAC Addr>`" and "`<Gateway IP Addr>`" parameters can be omitted.

The "`-l <SOL Target IPMB Addr>`" parameter needs to be entered as "`-l 0xNN`" where `NN` is the IPMB address of the target blade. The IPMB address will depend upon the location of the target blade in the chassis. Refer to Table 125 for the IPMB address for each physical slot in the MPCHC0001 chassis. Other chassis may have different IPMB addresses.

2. Choose one of the three interfaces below to execute the *reference_cfg* script. It does not matter which interface is chosen. The ***reference_cfg*** script can be executed through any of these interfaces.
   a. **Script executed on the local SOL target blade payload**
      Communication will be from the host processor to the local IPMC through the KCS interface

Execute this command to configure SOL on the target blade:
`reference_cfg -I kcs -g -i <SOL Target IP Addr>`

b. **Script executed on the Intel CMM**
Communication will be from the CMM to the target blade through IPMB.

Note: This requires an MPCMM0001 or MPCMM0002 chassis and firmware `6.1.0.2779` or later.

FTP these two files (`/usr/bin/reference_cfg and /usr/lib/sbcutils/reference_funcs`) to the CMM `/home/scripts` directory.

"The CMM default IP address is `10.90.90.91`.

If you are not able to FTP to the CMM:
at the CMM prompt type
`vi /etc/ftpusers`

Comment out root (`# root`)

Type `wq!`

Execute this command to change the *reference_cfg* file attributes:
`chmod 777 reference_cfg`

Execute this command to configure SOL on the target blade:
`reference_cfg -I ipmb -g -i <SOL Target IP Addr> -j <Gateway IP Addr> -n <Gateway MAC Addr> -l <SOL Target IPMB Addr>`

c. **Script executed on a remote computer**
Communication is from the remote computer to the CMM through a LAN interface (RMPC) that is then bridged to the target blade IPMC through IPMB.

Transfer these two files (`/usr/bin/reference_cfg` and `/usr/lib/sbcutils/reference_funcs`) to the remote computer using FTP.
Transfer this file, `/usr/share/doc/sbcutils/cmdPrivilege.ini`, to both the active and standby CMMs.

Place ***cmdPrivilege.ini*** in the `/etc/` directory. This file is needed to set up RMCP.

Reboot both CMMs

Once the CMMs have booted, from the remote computer execute this command:
`reference_cfg -I lan -g -i <SOL Target IP Addr> -j <Gateway IP Addr> -n <Gateway MAC Addr> -l <SOL Target IPMB Addr> -H <CMM IP Addr> -U root -P cmmrootpass -A md5`

3. If the configuration script is successful, you will see similar output to the following on the console. Once the configuration has been successfully written to the SOL target blade, it is ready activating the SOL session from the client blade.

```
cmmget -l blade14 -t raw -d "0x06 0x41 1 0x80"
reference_cfg: Data response "0x2A 0x03"
reference_cfg: Success
cmmget -l blade14 -t raw -d "0x0C 0x21 1 0x01 0x01"
reference_cfg: Success
cmmget -l blade14 -t raw -d "0x0C 0x21 1 0x02 0x03"
```

```
reference_cfg: Success
cmmget -l blade14 -t raw -d "0x0C 0x21 1 0x03 0x07 0x2A"
reference_cfg: Success
cmmget -l blade14 -t raw -d "0x0C 0x21 1 0x04 0x03 0x0A"
reference_cfg: Success
cmmget -l blade14 -t raw -d "0x0C 0x21 1 0x05 0x06"
reference_cfg: Success
cmmget -l blade14 -t raw -d "0x0C 0x21 1 0x06 0x06"
reference_cfg: Success
```

11.8.2 Client Blade Setup

The client blade is the SOL blade that activates SOL on the target and receives serial output from the target. The output is displayed on the client console.

Ensure the MPCBL0010 SBC has the following firmware/OS versions loaded:

- IPMC Firmware 4.56_R006 or later
- Bios 045.P04 or later
- sbcutilities 1.2.0.10 or later
- MontaVista 4.0 LSP,
  RedHat RHEL 4.0 U3

Note: **ipmitool** needs to be installed on a Linux computer located anywhere in the network. In this example, **ipmitool** is running on another blade in the same chassis.

11.8.2.1 Configure the Ethernet Port

For MontaVista* 4.0:

1. Configure the IP address of the Ethernet port:
   ```
   vi /etc/network/interfaces
   ```
   ```
   auto lo ethN
   iface lo inet loopback
   auto ethN
   iface ethN inet static
      address 192.168.0.42
      network 192.168.0.0
      netmask 255.255.255.0
      broadcast 192.168.0.255
      gateway 192.168.0.1
   ```
2. Execute this command to restart the network:
   ```
   /etc/init.d/networking restart
   ```

For RedHat* RHEL:

1. Configure IP address of the Ethernet port:
   ```
   vi /etc/sysconfig/network-scripts/ifcfg-ethN
   ```
   ```
   ifcfg-eth4
   BOOTPROTO=static
   IPADDR=10.90.90.113
   NETMASK=255.0.0.0
   ONBOOT=yes
   TYPE=Ethernet
   DHCP_HOSTNAME=rhel4u3
   ```
2. Execute this command to restart the network:
   ```
   service network restart
   ```

11.8.2.2 Installing ipmitool

1. Download 1.8.7 or newer version of ipmitool from http://ipmitool.sourceforge.net/
2. Install ipmitool 1.8.7 on the Client Blade. ipmitool provides the SOL client interface.
3. Type: `tar zxvf ipmitool-1.8.7.tar.gz`
4. Change directory to the ipmitool directory created after tar, cd ipmitool-1.8.7
5. Type: `./configure`
6. Type: `make install`
7. For RedHat* RHEL only: Before using **ipmitool**, start the IPMI drivers. In MontaVista, the IPMI drivers start automatically.
   a. Start the IPMI drivers:
      `# /etc/init.d/ipmi start` (This will start IPMI drivers for this particular session only.)
      `# chkconfig ipmi on` (This starts IPMI drivers by default onthe next reboot.)
8. If the computer that **ipmitool** was just installed on has a local IPMC, the **ipmitool** installation can be tested by typing:
   `ipmitool raw 6 1`

   If **ipmitool** is running correctly, the response should be in a format similar to:
   `20 81 01 03 02 3f 57 01 00 0c 08 01 05 01 00.`

11.8.2.3 Start an SOL Session

Before starting an SOL session, first make sure you can ping the target blade.

On the Client Blade, execute this command:
```
# ipmitool -I lanplus -L operator -H <SOL Target IP addr> -U solusername -
P  soluserpassword sol activate
```

If the SOL session is activated successfully, you get the following message:
`[SOL Session operational.  Use ~? for help]`

Press **enter** and the target output should be displayed on your console.

If the SOL session does not activate, run this command and check how **ipmitool** is configured:
```
# ipmitool -I lanplus -L operator -H <SOL Target IP Addr> -U solusername -
P  soluserpassword sol info
```

11.8.2.4 Checking SOL Configuration

There are two commands that can be issued to check the SOL configuration. on the Ethernet channels.

Note: **ipmitool** must be installed on the SOL target blade as well.

Use "`ipmitool lan print 1`" to display the configuration for the first Ethernet channel.
(This Ethernet port is connected to the Ethernet switch located in Slot #7 on the MPCH0001 chassis)

Use "`ipmitool lan print 2`" to display the configuration for the second Ethernet channel (This Ethernet port is connected to the Ethernet switch located in Slot #8 on the MPCH0001 chassis)

```
root@DRBlade14:/usr/bin# ipmitool lan print 1
Set in Progress         : Set Complete
Auth Type Support       : NONE MD2 MD5 PASSWORD
Auth Type Enable        : Callback :
                        : User     :
                        : Operator :
                        : Admin    :
                        : OEM      :
IP Address Source       : Unspecified
IP Address              : 10.90.90.14
Subnet Mask             : 255.255.255.0
MAC Address             : 00:0e:0c:98:55:6e
SNMP Community String   :
IP Header               : TTL=0x40 Flags=0x40 Precedence=0x00 TOS=0x10
BMC ARP Control         : ARP Responses Disabled, Gratuitous ARP Disabled
Gratituous ARP Intrvl   : 2.0 seconds
Default Gateway IP      : 0.0.0.0
Default Gateway MAC     : 00:00:00:00:00:00
Backup Gateway IP       : 0.0.0.0
Backup Gateway MAC      : 00:00:00:00:00:00
RMCP+ Cipher Suites     : None
Cipher Suite Priv Max   : XXXXXXXXXXXXXXX
                        :     X=Cipher Suite Unused
                        :     c=CALLBACK
                        :     u=USER
                        :     o=OPERATOR
                        :     a=ADMIN
```

11.8.2.5 Ending an SOL Session

In order to use the front panel serial console port on the target blade, end the SOL session.

1. Type: `~.`

Note: After pressing ~ just once, this symbol will not appear on the console screen. This is done at the login prompt.

2. After typing ~ the SOL session will deactivate on the SOL Target Blade. To make sure the Target Blade SOL session is deactivated, type the following command:

```
# ipmitool -I lanplus -L operator -H <SOL Target IP Addr> -U solusername -
P soluserpassword sol deactivate
```

SOL ise stopped completely and the serial console port is now redirected to the front panel of the SOL target blade.

11.9 Operating Systems for SOL Client (ipmitool)

The SOL client utility (ipmitool) can be compiled to work with any Linux OS.

12.0 Telecom Clock

12.1 Functional Description

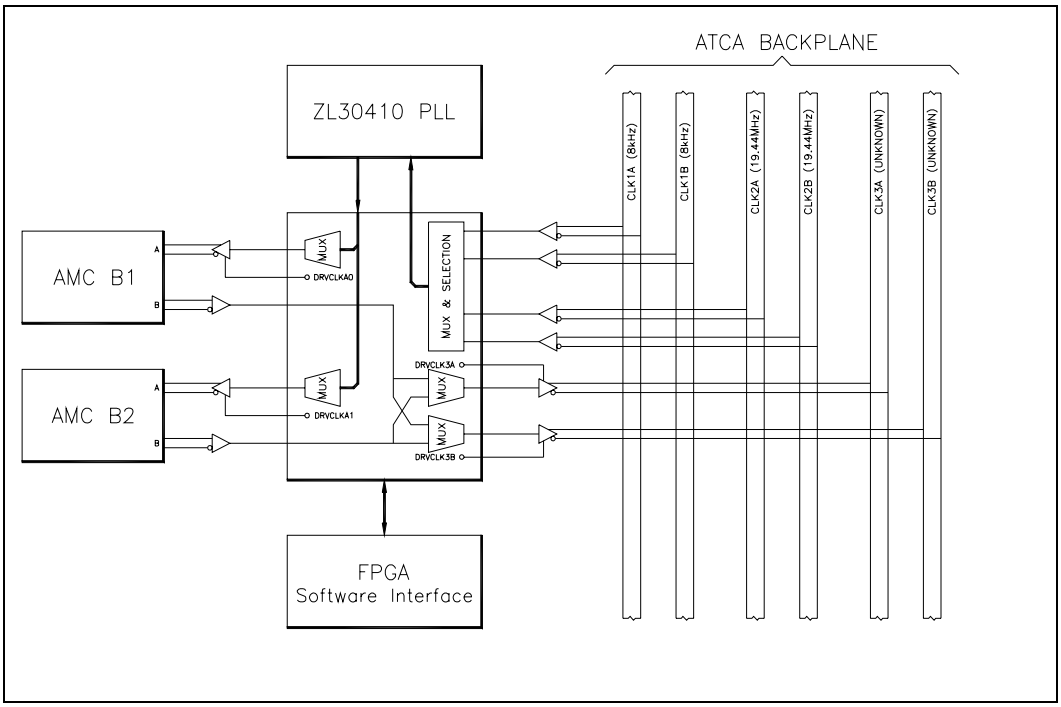
The MPCBL0010 SBC has a built-in telecom clock synchronization circuit. This circuit uses the Zarlink* ZL30410* Multi-Service Line Card PLL and a PLD that act as a clock multiplexer on inputs and outputs. The clock can be synchronized to the AdvancedTCA* backplane clocks, and the output clocks can be routed to the AdvancedMC* CLKA and CLKB signals.

Control and status registers are implemented in the FPGA. States are synchronized between the FPGA and the PLD through a 33 MHz full-duplex synchronous serial link. The FPGA is attached to the main processor as well as the IPMC to allow for flexibility and simple access to the control/status registers.

The main features of the telecom clock are:

- Redundant reference clock pair selection from CLK1A, 1B with 8 kHz and CLK2A, 2B with 19.44 MHz
- Automatic hitless switching between selected redundant reference clock pair (between CLK1A and CLK1B, or CLK2A and CLK2B)
- Provision of line transmission clocks with diverse frequencies to the AdvancedMC modules
- Setup and alarm interface through the I^2C bus and additional interrupt signal

Figure 31. Block Diagram of the Telecom Clock



12.2 Interface Description

12.2.1 AdvancedTCA Backplane Interface

The redundant reference clock CLK1A /CLK1B (8 kHz), and CLK2A/CLK2B (19.44 MHz), are connected from the AdvancedTCA* backplane. These signals use Multipoint-Low Voltage Differential Signaling (M-LVDS). Since only very short stub lengths are allowed with these signals, M-LVDS to Low Voltage Transistor-Transistor Logic (LV-TTL) level converters have to been placed near to the backplane connectors. Two pairs of the redundant clocks are connected to the telecom clock module inputs.

12.2.2 AdvancedMC Interface

The telecom clock module supports two AdvancedMC modules. Each module has one clock input (CLKA), and one clock output (CLKB). These clocks have LVDS signal levels that have to be realized in point-to-point connection. These clocks can be disabled separately for cases when they are not needed. The AdvancedMC clock output, which is used to pass a recovered line clock, enables the system to use a line interface as a synchronization source. The clock frequency of this interface is unchanged and the clocks are passed to CLK3A/CLK3B on the AdvancedTCA backplane. These inputs can be left open if an AdvancedMC module is not installed.

12.2.3 Reset/Interrupt Interface

The telecom clock module has to be reset once after power-up to define the default state in all devices on the module. The interrupt signals (open drain, active low) when any alarm occurs.

12.2.4 LPC Interface

The LPC interface is used to configure the telecom clock module. It is also used to check the status of the configuration information saved in the I^2C EEPROM.

12.3 Function Description

12.3.1 Redundant Reference Clock Selection

CLK1A/CLK1B (8 kHz) and CLK2A/CLK2B (19.44 MHz) are derived from the AdvancedTCA backplane. The signal level is converted from M-LVDS into LVTTL. One of these redundant pairs can be selected as a redundant source pair. Both signals of the pair are supervised to detect loss of clock. Frequency accuracy is not supervised. If the selected clock fails (more than about two clock cycles), a loss of signal (LOS) alarm is declared via an interrupt and the reference clock is switched to another one in a hitless-switch manner.

The selected clock is used as the phase lock loop (PLL) reference clock on which the generated clocks synchronize. The PLL unlock and/or holdover alarm can also be used as a cause for switchover.

12.3.2 PLL Clock Generation

The PLL supports many different frequencies for flexibility. The following frequencies can be selected individually per AdvancedMC module:

- 8 kHz
- 1.544 MHz

- 2.048 MHz
- 2.048 MHz
- 4.096 MHz
- 6.312 MHz
- 8.192 MHz,
- 8.592 MHz
- 11.184 MHz
- 19.44 MHz
- 34.368 MHz
- 44.735 MHz.

Note: Only one frequency per AdvancedMC module can be selected.

12.3.3 Recovered Clock Selection

Each AdvancedMC module has one clock output. This clock can be forwarded to CLK3A and/or CLK3B on the AdvancedTCA backplane without changing the frequency. The output level converters convert from LVTTL to M-LVDS. The M-LVDS buffers can be tri-stated by the telecom clock module using its I^2C interface.

12.3.4 Configuration

The clock outputs are disabled by default. The following basic and operational configurations are necessary:

12.3.4.1 Operational Configuration

For the operational configuration, the following parameters must be defined:

- Frequency of the redundant reference clock (CLK1=8 kHz or CLK2=19.44 MHz)
- Which AdvancedMC modules are installed and which frequency of the reference clock for the transmission is required
- Which AdvancedMC clock is used as a source of the system reference clock, and to which clock bus it has to be connected
- Operating mode of the PLL (normal, holdover, or free-run)
- Switchover by PLL unlock enabled
- Switchover by PLL holdover enabled

12.3.5 Alarm Handling

The following alarms are available:

- Primary redundant clock lost (PRI_LOS)
- Secondary redundant clock lost (SEC_LOS)
- PLL is in the holdover mode (HOLDOVER)
- PLL is in unlock (UNLOCK)

A change of status to any of the alarms will cause an interrupt. The interrupt is deactivated when the status register is read.

Additionally the currently selected redundant reference clock (REFSEL) is available. Since the hitless switchover is executed by hardware automatically, the software only has to read out the current status of the clock selection.

12.4 Telecom Clock API

This section describes how to configure the telecom clock using the telecom clock API. The telecom clock API is included with the MontaVista* Linux Support Package (LSP) for the MPCBL0010 SBC.

Note: The telecom clock API is open source. it has been implemented as the **tlclk** driver in the main-line 2.6.15 kernel at http://www.kernel.org/pub/linux/kernel/v2.6/linux-2.6.15.tar.bz2.

To access the telecom clock registers, it must first be enabled in the MontaVista Linux kernel ***config*** file. Set the option **CONFIG_TELCLOCK=m** to enable the telecom clock as a driver module in the kernel ***config*** file. Then use the command **modprobe tlclk** to load the driver.

Note: For MontaVista Linux, the kernel config file is created by default as a hidden file. To see it, you must do an "**ls –a**" in the root of the kernel source tree. The file name is "***.config***".

12.4.1 TRANSMIT CLOCK

See the table below to select the transmission clock frequency to the AdvancedMC B1 module or AdvancedMC B2 module.

Functions:

```
IOCTL_SELECT_AMCB2_TRANSMIT_CLOCK

IOCTL_SELECT_AMCB1_TRANSMIT_CLOCK
```

Table 126. Module Transmission Frequency Selection

Name	Used For	Value
CLK_8kHz	E1/T1/J1/J2	0xFF
CLK_1_544MHz	T1/J1	0x00
CLK_2_048MHz	E1	0x01
CLK_4_096MHz	E1	0x02
CLK_6_312MHz	J2	0x03
CLK_8_192MHz	E1	0x04
CLK_19_440MHz	E3/T3	0x06
CLK_8_592MHz	E3/T3	0x08
CLK_16_384MHz	E1/T1/J1/J2	0xFB
CLK_11_184MHz	OC3, 12/STM-1, 4	0x09
CLK_34_368MHz	E3/T3	0x0B
CLK_44_736MHz	E3/T3	0x0A

12.4.2 Enable / Disable Transmission Clock

To enable/disable the transmission clock for the AdvancedMC B1 module or AdvancedMC B2 module, use the following:

Functions:

IOCTL_ENABLE_CLKA0_OUTPUT

IOCTL_ENABLE_CLKB0_OUTPUT

IOCTL_ENABLE_CLKA1_OUTPUT

IOCTL_ENABLE_CLKB1_OUTPUT

Possible values:

0x01 = Enables transmission clock

0x00 = Disables transmission clock

12.4.3 Recovered Clock

To drive the recovered reference clock to the AdvancedTCA backplane from the AdvancedMC modules, use the following:

Functions:

IOCTL_ENABLE_CLK3A_OUTPUT

IOCTL_ENABLE_CLK3B_OUTPUT

Possible Values:

0x01 = Enables reference clock

0x00 = Disabled reference clock

12.4.4 Automatic Switchover

To enable automatic hitless switchover to the redundant reference clock in case of holdover or loss of reference clock, use the following:

Function:

IOCTL_HARDWARE_SWITCHING

Table 127. Automatic Switchover Values

Name	Description	Value
HW_ENABLE	Enables hardware switchover	0x80
HW_DISABLE	Disables hardware switchover	0x00

12.4.5 Automatic Switchover Mode

To define the hardware switchover mode criteria, use the following:

Function:

IOCTL_HARDWARE_SWITCHING_MODE

Table 128. Switchover Mode Values

Name	Description	Value
PLL_HOLDOVER	Use PLL holdover detection	0x40
LOST_CLOCK	Use loss of clock signal	0x00

12.4.6 Select Reference Clock

To select the received reference clock from AdvancedMC for AdvancedTCA backplane CLK3B and CLK3A, use the following:

Functions:

IOCTL_SELECT_RECEIVED_REF_CLK3A

IOCTL_SELECT_RECEIVED_REF_CLK3B

Table 129. Received Reference Clock Values

Name	Description	Value
AMC_B1	Source from AdvancedMC B1	0x00
AMC_B2	Source from AdvancedMC B2	0x10

12.4.7 Reference Frequency for PLL

To select the reference frequency that feeds the clocks to the PLL, use the following:

Function:

IOCTL_SELECT_REF_FREQUENCY

Table 130. Reference Frequency PLL Values

Name	Description	Value
REF_CLK1_8kHz	PLL input clocks = CLK1A and CLK1B (8 kHz, per AdvancedTCA specification)	0x00
REF_CLK2_19_44MHz	PLL input clocks = CLK2A and CLK2B (19.44 MHz, per AdvancedTCA specification)	0x02

12.4.8 Primary/Secondary Redundant Clock

To select the primary or secondary redundant clock, use the following:

Function:

IOCTL_SELECT_REDUNDANT_CLOCK

Table 131. Primary/Secondary Redundant Clock Values

Name	Value
PRIMARY_CLOCK	0x00
SECONDARY_CLOCK	0x01

12.4.9 Corner Frequency

To select the corner frequency of the PLL loop filter, use the following:

Function:

`IOCTL_FILTER_SELECT`

Table 132. Corner Frequency Values

Name	Description	Value
FILTER_6HZ	Change the corner frequency of the PLL loop filter to 6Hz and limits the phase slope to 41 ns per 1.326 ms.	0x04
FILTER_12HZ	Change the corner frequency to 12 Hz without phase slope limitation.	0x00

12.4.10 PLL Operating Mode

To select the operating mode of the PLL device, use the following:

Function:

`IOCTL_MODE_SELECT`

Table 133. PLL Operating Mode Values

Name	Value
NORMAL_MODE	0x00
HOLDOVER_MODE	0x10
FREERUN_MODE	0x20

12.4.11 Reference Clock Alignment

The PLL device locks in an arbitrary phase dependency. If needed, the phase of the output clock (transmission clock to the AdvancedMC) can be aligned to the reference clock.

Function:

`IOCTL_REFALIGN`

Possible Values :

None - just call the function for realignment.

12.4.12 Hardware Reset

To issue a hardware reset of the telecom clock PLL, use the following:

Function:

`IOCTL_RESET`

Table 134. Hardware Reset Values

Name	Description	Value
RESET_ON	Reset asserted	0x00
RESET_OFF	Reset deasserted	0x02

12.4.13 Read Alarm States

To read alarms state of the telecom clock, use the following:

Function:

IOCTL_READ_ALARMS

Table 135. Alarm State Values

Bit	Description	Define Bit Mask
0–3	None	None
4	Unlock detected	UNLOCK_MASK
5	Hold over detected. HOLDOVER_MASK	Hold over detected. HOLDOVER_MASK
6	Loss of secondary reference clock detected	SEC_LOST_MASK
7	Loss of primary reference clock detected.	PRI_LOST_MASK

12.4.14 Read New Events

To read all new events that occurred since the last read, use the following:

Function:

IOCTL_READ_EVENTS

Table 136. New Event Values

Bit	Description	Define Bit Mask
0	Loss of primary and secondary clocks	EVENT_LOST_CLOCKS
1	Primary clock is gone	EVENT_LOST_PRIMARY_CLOCK
2	Primary clock is back	EVENT_PRIMARY_CLOCK_BACK
3	Secondary clock is gone	EVENT_LOST_SECONDARY_CLOCK
4	Secondary clock is back	EVENT_SECONDARY_CLOCK_BACK
5	PLL in holdover	EVENT_PLL_HOLDOVER
6	Switchover to primary done	EVENT_SWITCHOVER_PRIMARY
7	Switchover to secondary done	EVENT_SWITCHOVER_SECONDARY
8	End of holdover condition	EVENT_END_HOLDOVER
9	PLL lost synchronization	EVENT_PLL_LOST_SYNC
10	PLL synchronized	EVENT_PLL_SYNC

12.4.15 Read the Current Reference Clock

To determine the current reference clock used by the telecom clock, use the following:

Function:

`IOCTL_READ_CURRENT_REF`

Table 137. Reference Clock Values

Current Reference Clock	Value
Primary Clock	0
Secondary Clock	q

12.4.16 sysfs Interface

When the Telecom Clock driver is loaded, it creates a ***sysfs*** directory under `/sys/devices/platform/telco_clock`.

This directory exports the following interfaces as shown in Table 138 where they are mapped to Telecom Clock API functions. (See Section 12.4, "Telecom Clock API" for information about using the Telecom Clock API.)

Table 138. Telecom Clock API Function Mapping for the sysfs Interface

sysfs Interface Name (File Name)	Telecom Clock API Function Name
alarms	IOCTL_READ_ALARMS
current_ref	IOCTL_READ_CURRENT_REF
received_ref_clk3a	IOCTL_SELECT_RECEIVED_REF_CLK3A
received_ref_clk3b	IOCTL_SELECT_RECEIVED_REF_CLK3B
enable_clk3a_output	IOCTL_ENABLE_CLK3A_OUTPUT
enable_clk3b_output	IOCTL_ENABLE_CLK3B_OUTPUT
enable_clka0_output	IOCTL_ENABLE_CLKA0_OUTPUT
enable_clka1_output	IOCTL_ENABLE_CLKA1_OUTPUT
enable_clkb0_output	IOCTL_ENABLE_CLKB0_OUTPUT
enable_clkb1_output	IOCTL_ENABLE_CLKB1_OUTPUT
filter_select	IOCTL_FILTER_SELECT
hardware_switching	IOCTL_HARDWARE_SWITCHING
hardware_switching_mode	IOCTL_HARDWARE_SWITCHING_MODE
telclock_version	-
mode_select	IOCTL_MODE_SELECT
refalign	IOCTL_REFALIGN
reset	IOCTL_RESET
select_amcb1_transmit_clock	IOCTL_SELECT_AMCB1_TRANSMIT_CLOCK
select_amcb2_transmit_clock	IOCTL_SELECT_AMCB2_TRANSMIT_CLOCK
select_redundant_clock	IOCTL_SELECT_REDUNDANT_CLOCK
select_ref_frequency	IOCTL_SELECT_REF_FREQUENCY

Note: All sysfs interfaces are integers in hex format, i.e., echo 99 > refalign has the same effect as echo 0x99

> refalign.

12.5 Telecom Clock Registers

This section provides descriptions of the Field Programmable Gate Array (FPGA) register settings as they apply to the telecom clock.

Note: Unused bits are reserved. To ensure compatibility with other product and upgrades to this product, do not modify unused bits.

Table 139. FPGA Register Legend

Symbol	Description
U	Unchanged (stay unchanged after reset)
X	Not Defined
NU	Not Used

See Chapter 9.0, “Addressing” for a complete list of FPGA register settings.

Table 140. FPGA Register Overview

80h	POST Code
81h	Extended POST Code (16-bit write only)
A00h	FPGA Version
A01h	Debug LED Control
A02h	FWUM Control (manufacturing use only)
A03h	Reserved
A04h	Development Features
A05-A07h	Reserved
A08h	Telecom Clock Register 0: Configuration
A09h	Telecom Clock Register 1: Configuration
A0Ah	Telecom Clock Register 2: Configuration & Status
A0Bh	Telecom Clock Register 3: Configuration
A0Ch	Telecom Clock Register 4: Reset and Test Modes
A0Dh	Telecom Clock Register 5: PLD Version
A0Eh	Telecom Clock Register 6: Alarms
A0Fh	Telecom Clock Register 7: Interrupt Number
A10-A1Fh	Reserved

Table 141. Telecom Clock Register 0 0A08h

Address	Action	D7	D6	D5	D4	D3	D2	D1	D0
0xA08	Read	HWMODE	HO_LOS	MS2	MS1	REFALIGN	FCS	E3DS3	E3DS30C3
	Write	HWMODE	HO_LOS	MS2	MS1	REFALIGN	FCS	E3DS3	E3DS30C3
	Reset	0	0	0	0	0	0	0	0

HWMODE: Enables automatic switching by hardware

HO_LOS: Switch criteria in HW mode:
When set, uses PLL holdover detection as the switch criteria
When cleared, uses loss of clock (internal to PLD) as the switch criteria

MS2 / MS1: PLL Mode selection:

MS[2..1] = 00: Normal operation

MS[2..1] = 01: Holdover mode

MS[2..1] = 10: Free-run mode

MS[2..1] = 11: Reserved

REFALIGN: Reference clock phase alignment: changing this bit from 0 to 1 starts the alignment

FCS: Filter characteristics of the PLL

0: 12Hz filter without phase slope limitation

1: 6Hz filter with phase slope limited to 41 ns per 1.326 ms

E3DS3 / E3DS3OC3: These bits select the transmission clock frequency, when TXREFx_SEL[2..0] = 111 in telecom clock register 3.

E3DS3OC3 = 0, E3DS3 = 1: 8.592 MHz

E3DS3OC3 = 0, E3DS3 = 0: 11.184 MHz

E3DS3OC3 = 1, E3DS3 = 1: 34.368 MHz

E3DS3OC3 = 1, E3DS3 = 0: 44.736 MHz

Table 142. Telecom Clock Register 1 0A09h

Address	Action	D7	D6	D5	D4	D3	D2	D1	D0
0xA09	Read	RSV1	RSV0	SELCLK3B	SELCLK3A	REFSEL	8K_16M	SEL_REFFRQ	SEL_RDNCLK
	Write	NU	NU	SELCLK3B	SELCLK3A	NU	8K_16M	SEL_REFFRQ	SEL_RDNCLK
	Reset	X	X	0	0	X	0	0	0

SELCLK3B: Select clock to send to backplane CLK3B:

0 = from first AdvancedMC module (AMC B1, CLKC)

1 = from second AdvancedMC module (AMC B2, CLKC)

SELCLK3A: Select clock to send to backplane CLK3A:

0 = from first AdvancedMC module (AMC B1, CLKC)

1 = from second AdvancedMC module (AMC B2, CLKC).

8K_16M: This bit is valid only when the transmission clock is selected by setting TXREFx_SEL[2..0]=101 in the TelClock3 register.
Setting this bit selects the transmission clock frequency as 16.384 MHz
Clearing this bit selects 8.0 kHz.

SEL_REFFRQ: Selects the reference frequency (8 k or 19.44 M):

0 = 8 kHz

1=19.44 MHz

SEL_REFFRQ: this bit controls the multiplexer that feeds clocks to the PLL:

0: PLL input clocks = CLK1A and CLK1B (8 kHz, per AdvancedTCA specification)

1: PLL input clocks = CLK2A and CLK2B (19.44 MHz, per AdvancedTCA specification).

SEL_RDNCLK: Setting this bit to the value of the formerly read REFSEL enables the switchover to the unused reference in the case of LOS for the actual reference.

REFSEL: Show the reference that is currently selected:

0: Primary reference

1: Secondary reference

RSV1 / RSV0: Reserved.

Table 143. Telecom Clock Register 2 0A0Ah

Address	Action	D7	D6	D5	D4	D3	D2	D1	D0
0xA0A	Read	PRI_LOS	SEC_LOS	HOLDOVER	UNLOCK	DRVCLKB1	DRVCLKA1	DRVCLKB0	DRVCLKA0
	Write	NU	NU	NU	NU	DRVCLKB1	DRVCLKA1	DRVCLKB0	DRVCLKA0
	Reset	X	X	X	X	X	0	X	0

PRI_LOS: Loss of primary reference clock detected: this bit is high when the primary clock at the input of the PLL (i.e., after PLD mux) is lost.

SEC_LOS: Loss of secondary reference clock detected: this bit is high when the primary clock at the input of the PLL (i.e. after PLD mux) is lost.

HOLDOVER: Holdover detected by the PLL

UNLOCK: Unlock detected by the PLL

DRVCLKA1: Drive transmission clock CLKA1 for AdvancedMC module B2: this bit is forced to 0 when advancedMC module B2 is absent or unpowered.

DRVCLKA0: Drive transmission clock CLKA0 for AdvancedMC module B1: this bit is forced to 0 when AdvancedMC module B1 is absent or unpowered.

DRVCLKB1: Drive transmission clock CLKB1 for AdvancedMC module B2. This bit is forced to 0 when AdvancedMC module B2 is absent or unpowered.

DRVCLKB0: Drive transmission clock CLKB0 for AdvancedMC module B1. This bit is forced to 0 when AdvancedMC module B1 is absent or unpowered.

Table 144. Telecom Clock Register 3 0A0Bh

Address	Action	D7	D6	D5	D4	D3	D2	D1	D0
0xA0B	Read	DRVCLK3B	DRVCLK3A	TXREF1_SEL[2..0]			TXREF0_SEL[2..0]		
	Write	DRVCLK3B	DRVCLK3A	TXREF1_SEL[2..0]			TXREF0_SEL[2..0]		
	Reset	0	0	000			000		

DRVCLK3B: Enables MLVDS buffer to drive CLK3B to the backplane

DRVCLK3A: Enables MLVDS buffer to drive CLK3A to the backplane

TXREF1_SEL[2..0]: Transmission reference clock for AdvancedMC module B2 selection (see Table 145 below).

TXREF0_SEL[2..0]: Transmission reference clock for AdvancedMC module B1 selection (see Table 145 below).

The transmission frequency is selected according to the following table:

Table 145. Transmission Frequency Selection

TXREFx_SEL[2..0]	Transmission Clock Frequency
000	1.544 MHz (T1, J1)
001	2.048 MHz (E1)
010	4.096 MHz (E1)
011	6.312 MHz (J2)
100	8.192 MHz (E1)
101	8 kHz / 16.384 MHz† (E1, T1, J1, J2)
110	19.44 MHz (OC3, 12/STM-1, 4)
111	34.368 / 44.736 MHz‡ (E3, T3) or 8.592 / 11.184 MHz

Notes:

† 8kHz or 16 MHz can be selected by bit 8K_16M in telecom clock register 1.

‡ One frequency can be selected by bits E3DS3 and E3DS3OC3 in telecom clock register 0.

Table 146. Telecom Clock Register 4 0A0Ch

Address	Action	D7	D6	D5	D4	D3	D2	D1	D0
0xA0C	Read	NU	NU	NU	NU	NU	IRQTST	RESET	TEST
	Write	NU	NU	NU	NU	NU	IRQTST	RESET	TEST
	Reset	X	X	X	X	X	0	1	0

IRQTST: Interrupt test. The state of this bit is OR'd with the real interrupt. This bit is for software testing. Ignore in normal operation. A "**1**" asserts the interrupt request.

TEST: Ignores IPMC and shelf manager authorization. Use this bit for testing only. In normal operation, leave this bit set to "**0**". Otherwise, the MPCBL0010 SBC will not be compliant with the AdvancedTCA specification.

RESET: Hardware reset of the PLL.

Table 147. Telecom Clock Register 5 0A0Dh

Address	Action	D7	D6	D5	D4	D3	D2	D1	D0
0xA0D	Read	PCB	Version						
	Write	NU	NU						
	Reset	PCB	Version						

PCB: Set to "**1**" to indicate that the compilation switch was properly set in the source code and that the PLD is compiled for PCB revision 1.

VERSION: PLD code version. A value of:

PCB&Version = FF: indicates a test PLD to make a clock generator.

PCB&Version = FE: indicates a test PLD used during manufacturing tests.

Table 148. Telecom Clock Register 6 0A0Eh

Address	Action	D7	D6	D5	D4	D3	D2	D1	D0
0xA0E	Read	UNLOCK10	UNLOCK01	HLDOVR10	HLDOVR01	SEC10	SEC01	PRI10	PRI01
	Write	NU	NU	NU	NU	NU	NU	NU	NU
	Reset	X	X	X	X	X	X	X	X

PRI01: Bit PRI_LOS in telecom clock register 2 switched from 0 to 1

PRI10: Bit PRI_LOS in telecom clock register 2 switched from 1 to 1

SEC01: Bit SEC_LOS in telecom clock register 2 switched from 0 to 1

SEC10: Bit SEC_LOS in telecom clock register 2 switched from 1 to 0

HLDOVR01: Bit HOLDOVER in telecom clock register 2 switched from 0 to 1

HLDOVR10: Bit HOLDOVER in telecom clock register 2 switched from 1 to 0

UNLOCK01: Bit UNLOCK in telecom clock register 2 switched from 0 to 1

UNLOCK10: Bit UNLOCK in telecom clock register 2 switched from 1 to 0

This register reports changes since the last time it was read. A legacy ISA interrupt is generated when any of these bits are set. The actual interrupt used is assigned by the BIOS at boot time and can be read from telecom clock register 7.

Reading this register clears all bits that were '**1**' prior to reading. Bits that turned to '**1**' during the reading will not be affected.

Table 149. Telecom Clock Register 7 0A0Fh

Address	Action	D7	D6	D5	D4	D3	D2	D1	D0
0xA0F	Read	NU	NU	NU	NU	Interrupt Number			
	Write	NU	NU	NU	NU	Interrupt Number			
	Reset	X	X	X	X	0101b			

The content of this register is the number of the legacy ISA interrupt used for events (see Table 148). It is initialized at boot time by the BIOS.

The interrupt is acknowledged by a read of telecom clock register 6. Always perform a read to this register before enabling the interrupt in the chipset to remove any pending interrupt.

A value of '**2'** hooks the interrupt to an SMI.

Table 150. FPGA/PLD Serial Link Bit Definition

Bit	Write	Read
0	0 (to avoid spurious reset)	TelClock1: REFSEL
1	0 (to avoid spurious reset)	TelClock1: RSV0
2	0 (to avoid spurious reset)	TelClock1: RSV1
3	TelClock4: Reset	TelClock2: UNLOCK
4	TelClock0:E3DS30C3	TelClock2: HOLDOVER
5	TelClock0: E3DS3	TelClock2: SEC_LOS
6	TelClock0: FCS	TelClock2: PRI_LOS
7	TelClock0: REFALIGN	TelClock5: Version(0)
8	TelClock0: MS1	TelClock5: Version(1)
9	TelClock0: MS2	TelClock5: Version(2)
10	TelClock0: HO_LOS	TelClock5: Version(3)
11	TelClock0: HWMODE	TelClock5: Version(4)
12	TelClock1: SEL_RDNCLK	TelClock5: Version(5)
13	TelClock1: SEL_REFFRQ	TelClock5: Version(6)
14	TelClock1: 8K_16M	TelClock5: Version(7)
15	TelClock1: SELCLK3A	
16	TelClock1: SELCLK3B	
17	TelClock2: DRVCLKA0	
18	TelClock2: DRVCLKB0	
19	TelClock2: DRVCLKA1	
20	TelClock2: DRVCLKB1	
21	TelClock3: TXREF0_SEL(0)	
22	TelClock3: TXREF0_SEL(1)	
23	TelClock3: TXREF0_SEL(2)	
24	TelClock3: TXREF1_SEL(0)	
25	TelClock3: TXREF1_SEL(1)	
26	TelClock3: TXREF1_SEL(2)	
27	TelClock3: DRVCLK3A	
28	TelClock3: DRVCLK3B	
29	TelClock4: TEST	
30	0 (not used)	
31	0 (not used)	

13.0 Maintenance

13.1 Supervision

Table 151 lists the main components that perform hardware monitoring of voltages and timers.

Table 151. Hardware Monitoring Components

Component	Function	Monitors
Intelligent Platform Management Controller (IPMC)	WDT #1	Commands from the BIOS. If the timer expires (times out), causes a hard reset, power down, or power cycle and IPMI event.
6300ESB (Intel® 82801CA I/O Controller Hub 3)	WDT #3	The first attempt to fetch an instruction after a power failure.
FWUM (R1C13)	WDT #2	Strobed by IPMC firmware. If it expires, it isolates The MPCBL0010 SBC from the backplane IPMB buses, and resets the IPMC. Also performs fail safe field upgrade of the IPMC.

13.2 Diagnostics

13.2.1 In-Target Probe (ITP)

The ITP connector supports the use of a tool that helps you observe and control the step-by-step execution of your program for debugging hardware and software. Debugging includes finding a hardware or software error and identifying the location and cause of the error so it can be corrected.

To maximize the development and delivery of mission-critical tools, we works with third party vendors to develop and deliver specific tools. The following vendors provide in-circuit emulation hardware and software:

- American Arium* currently develops in-circuit emulation and run control tools for Intel processors.

  http://www.arium.com/

- Agilent Technologies* currently develops logic analyzer and probing tools for Intel processors.

  http://we.home.agilent.com

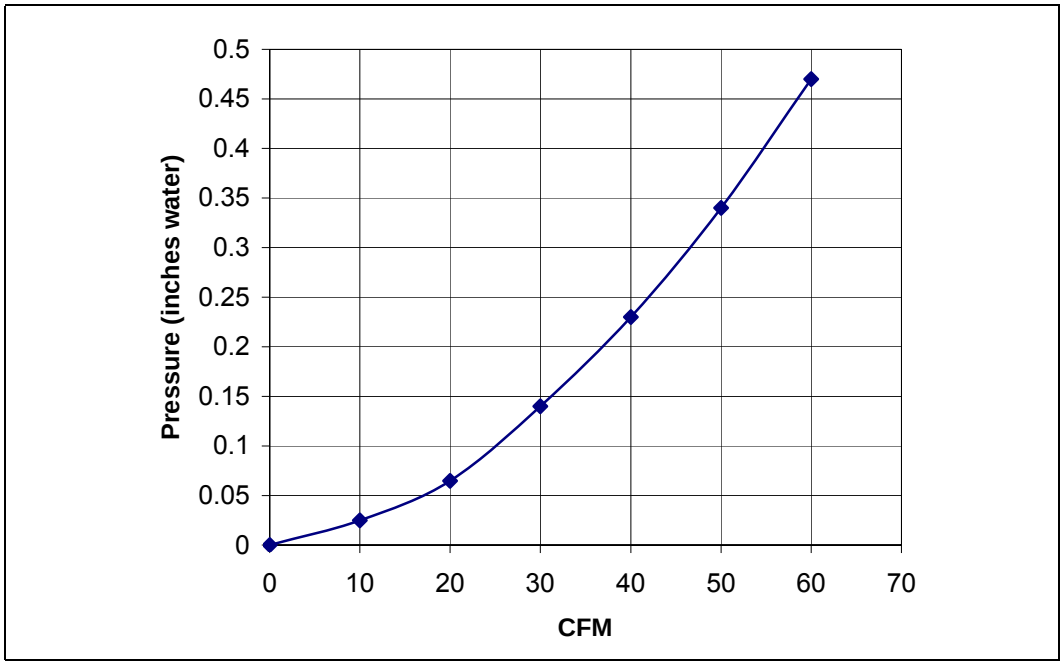
- Tektronix* currently develops logic analyzer and probing tools for Intel processors.

  http://www.tek.com/Measurement/logic_analyzers/index.html

14.0 Thermals

The pressure drop versus flow rate curve in Figure 32 represents flow impedance of the slot. This information is provided in accordance with Section 5 of the *PICMG 3.0 specification* to aid in using the MPCBL0010 SBC SBC in various AdvancedTCA* shelves.

Figure 32. Power vs. Flow Rate



15.0 Component Technology

The main components implemented on the Intel NetStructure® MPCBL0010 Single Board Computer are listed below:

- Low Voltage Intel® Xeon™ Processor
- Intel® E7520 Chipset
- Intel® E7520 Memory Controller Hub (MCH)
- Intel® 6300ESB I/O Controller Hub (ICH)
- Intel® 6700PXH 64-bit PCI Hub
- Intel® 82546GB Dual Gigabit Ethernet Controller
- Renesas* H8S/2168 Group
- Atmel* AT49LW080 Firmware Hub
- Vitesse* VSC3108 8x8 Crosspoint Switch

16.0 Warranty Information

16.1 Intel NetStructure® Compute Boards and Platform Products Limited Warranty

Intel warrants to the original owner that the product delivered in this package will be free from defects in material and workmanship for two (2) year(s) following the latter of: (i) the date of purchase only if you register by returning the registration card as indicated thereon with proof of purchase; or (ii) the date of manufacture; or (iii) the registration date if by electronic means provided such registration occurs within 30 days from purchase. This warranty does not cover the product if it is damaged in the process of being installed. Intel recommends that you have the company from whom you purchased this product install the product.

THE ABOVE WARRANTY IS IN LIEU OF ANY OTHER WARRANTY, WHETHER EXPRESS, IMPLIED OR STATUTORY, INCLUDING, BUT NOT LIMITED TO, ANY WARRANTY OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, ANY WARRANTY OF INFRINGEMENT OF ANY OTHER PARTY'S INTELLECTUAL PROPERTY RIGHTS, OR ANY WARRANTY ARISING OUT OF ANY PROPOSAL, SPECIFICATION OR SAMPLE.

This warranty does not cover replacement of products damaged by abuse, accident, misuse, neglect, alteration, repair, disaster, improper installation or improper testing. If the product is found to be otherwise defective, Intel, at its option, will replace or repair the product at no charge except as set forth below, provided that you deliver the product along with a return material authorization (RMA) number (see below) either to the company from whom you purchased it or to Intel. If you ship the product, you must assume the risk of damage or loss in transit. You must use the original container (or the equivalent) and pay the shipping charge. Intel may replace or repair the product with either a new or reconditioned product, and the returned product becomes Intel's property. Intel warrants the repaired or replaced product to be free from defects in material and workmanship for a period of the greater of: (i) ninety (90) days from the return shipping date; or (ii) the period of time remaining on the original two (2) year warranty.

This warranty gives you specific legal rights and you may have other rights which vary from state to state. All parts or components contained in this product are covered by Intel's limited warranty for this product. The product may contain fully tested, recycled parts, warranted as if new.

16.2 Returning a Defective Product (RMA)

Before returning any product, contact an Intel Customer Support Group to obtain either a Direct Return Authorization (DRA) or Return Material Authorization (RMA). Return Material Authorizations are only available for products purchased within 30 days.

16.3 For the Americas

Return contact information by geography:

Return Material Authorization (RMA) credit requests e-mail address:
requests.rma@intel.com

Direct Return Authorization (DRA) repair requests e-mail address:
uspss.repair@intel.com

DRA on-line form: http://support.intel.com/support/motherboards/draform.htm

Intel Business Link (IBL): http://www.intel.com/ibl

Telephone No.: 1-800-INTEL4U or 480-554-4904

Office Hours: Monday - Friday 0700-1700 MST Winter / PST Summer

16.3.1 For Europe, Middle East, and Africa (EMEA)

Return Material Authorization (RMA) e-mail address EMEA.Returns@Intel.com

Direct Return Authorization (DRA) for repair requests e-mail address: EMEA.Returns@Intel.com

Intel Business Link (IBL): http://www.intel.com/ibl

Telephone No.: 00 44 1793 403063

Fax No.: 00 44 1793 403109

Office Hours: Monday - Friday 0900-1700 UK time

16.3.2 For Asia and Pacific (APAC)

RMA/DRA requests e-mail address: apac.rma.front-end@intel.com

Telephone No.: 604-859-3111 or 604-859-3325

Fax No.: 604-859-3324

Office Hours: Monday - Friday 0800-1700 Malaysia time

Return Material Authorization (RMA) requests e-mail address: rma.center.jpss@intel.com

Telephone No.: 81-298-47-0993 or 81-298-47-5417

Fax No.: 81-298-47-4264

Direct Return Authorization (DRA) for repair requests, contact the JPSS Repair center.

E-mail address: sugiyamakx@intel.co.jp

Telephone No.: 81-298-47-8920

Fax No.: 81-298-47-5468

Office Hours: Monday - Friday 0830-1730 Japan time

If the Customer Support Group verifies that the product is defective, they will have the Direct Return Authorization/Return Material Authorization Department issue you a DRA/RMA number to place on the outer package of the product. Intel cannot accept any product without a DRA/RMA number on the package.

16.3.3 Limitation of Liability and Remedies

INTEL SHALL HAVE NO LIABILITY FOR ANY INDIRECT OR SPECULATIVE DAMAGES (INCLUDING, WITHOUT LIMITING THE FOREGOING, CONSEQUENTIAL, INCIDENTAL AND SPECIAL DAMAGES) ARISING FROM THE USE OF OR INABILITY TO USE THIS PRODUCT, WHETHER ARISING OUT OF CONTRACT, NEGLIGENCE, TORT, OR UNDER ANY WARRANTY, OR FOR INFRINGEMENT OF ANY OTHER PARTY'S INTELLECTUAL PROPERTY RIGHTS, IRRESPECTIVE OF WHETHER INTEL HAS ADVANCE NOTICE OF THE

POSSIBILITY OF ANY SUCH DAMAGES, INCLUDING, BUT NOT LIMITED TO LOSS OF USE, BUSINESS INTERRUPTIONS, AND LOSS OF PROFITS. NOTWITHSTANDING THE FOREGOING, INTEL'S TOTAL LIABILITY FOR ALL CLAIMS UNDER THIS AGREEMENT SHALL NOT EXCEED THE PRICE PAID FOR THE PRODUCT. THESE LIMITATIONS ON POTENTIAL LIABILITIES WERE AN ESSENTIAL ELEMENT IN SETTING THE PRODUCT PRICE. INTEL NEITHER ASSUMES NOR AUTHORIZES ANYONE TO ASSUME FOR IT ANY OTHER LIABILITIES.

Some states do not allow the exclusion or limitation of incidental or consequential damages, so the above limitations or exclusions may not apply to you.

17.0 Customer Support

17.1 Customer Support

This chapter offers technical and sales assistance information for this product. Information on returning an Intel NetStructure® product for service is in the following chapter.

17.2 Technical Support and Return for Service Assistance

For all product returns and support issues, please contact your Intel product distributor or Intel Sales Representative for specific information.

17.3 Sales Assistance

If you have a sales question, please contact your local Intel NetStructure Sales Representative or the Regional Sales Office for your area. Address, telephone and fax numbers, and additional information is available at Intel's web site located at:

http://www.intel.com/network/csp/sales/

Intel Corporation
Telephone (in U.S.) 1-800-755-4444
Telephone (Outside U.S.) 1-973-993-3030
FAX 1-973-967-8780

17.4 Product Code Summary

Table 152 lists the MPCBL0010 SBC product codes.

Table 152. Product Codes

Product Code	MM#	Description
MPCBL0010N01Q	873803	MPCBL0010 SBC RoHS Lead Free
MPCBL0010S01Q	875258	MPCBL0010 SBC RoHS Lead Free (custom SKU)

18.0 Certifications

The Intel NetStructure® MPCBL0010 Single Board Computer has the following approvals:

- UL/cUL 60950-1
- EN/IEC 60950-1
- EN55024
- VCCI
- CISPRZZ

19.0 Agency Information—Class B

19.1 North America (FCC Class B)

Note: In order to ensure compliance to Class B requirements, it is recommended to use shielded cable for installations.

FCC Verification Notice

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) this device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

For questions related to the EMC performance of this product, contact:

Intel Corporation
5200 N.E. Elam Young Parkway
Hillsboro, OR 97124
1-800-628-8686

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the use will be required to correct the interference at his own expense.

19.2 Canada – Industry Canada (ICES-003 Class B) (English and French-translated)

CANADA – INDUSTRY CANADA

Cet appareil numérique respecte les limites bruits radioélectriques applicables aux appareils numériques de Classe B prescrites dans la norme sur le matériel brouilleur: “Appareils Numériques”, NMB-003 édictée par le Ministre Canadian des Communications.

(English translation of the notice above) This digital apparatus does not exceed the Class B limits for radio noise emissions from digital apparatus set out in the interference-causing equipment standard entitled “Digital Apparatus,” ICES-003 of the Canadian Department of Communications.

19.3 Japan VCCI Class B

この装置は、情報処理装置等電波障害自主規制協議会（ＶＣＣＩ）の基準に基づくクラスＢ情報技術装置です。この装置は、家庭環境で使用することを目的としていますが、この装置がラジオやテレビジョン受信機に近接して使用されると、受信障害を引き起こすことがあります。
取扱説明書に従って正しい取り扱いをして下さい。

19.4 Korean Class B

기종별	사 용 자 안 내 문
B급 기기 (가정용 정보통신기기)	이 기기는 가정용으로 전자파적합등록을 한 기기로서 주거지역에서는 물론 모든 지역에서 사용할 수 있습니다.

19.5 Australia, New Zealand

20.0 Safety Warnings

Caution: Review the following precautions to avoid personal injury and prevent damage to this product or products to which it is connected. To avoid potential hazards, use the product only as specified.

Read all safety information provided in the component product user manuals and understand the precautions associated with safety symbols, written warnings, and cautions before accessing parts or locations within the unit. Save this document for future reference.

This product is designed for use in a restricted access location only.

IMPORTANT: See installation instructions before connecting to the supply.

To reduce the risk of electric shock from a telephone or Ethernet* system, connect the unit's main power before making these connections. Disconnect these connections before removing main power from the unit.

Warning: Avoid electric overload, heat, shock, or fire hazard: Only connect the system to a to a properly rated supply circuit as specified in the product user manual. Do not make connections to terminals outside the range specified for that terminal. See the product user manual for correct connections.

Warning: Avoid electric shock: Do not operate in wet, damp, or condensing conditions. To avoid electric shock or fire hazard, do not operate this product with enclosure covers or panels removed.

Warning: Avoid electric shock: For units with multiple power sources, disconnect all external power connections before servicing.

Caution: System environmental requirements: Components such as Processor Boards, Ethernet Switches, etc., are designed to operate with external airflow. Components can be destroyed if they are operated without external airflow. External airflow is normally provided by chassis fans when components are installed in compatible chassis. Never restrict the airflow through the unit's fan or vents. Filler panels or air management boards must be installed in unused chassis slots. Environmental specifications for specific products may differ. Refer to product user manuals for airflow requirements and other environmental specifications.

Warning: Device heatsinks may be hot during normal operation: To avoid burns, do not allow anything to touch heatsinks.

Warning: Avoid injury, fire hazard, or explosion: Do not operate this product in an explosive atmosphere.

Warning: Avoid injury: This product may contain one or more laser devices that are visually accessible depending on the plug-in modules installed. Products equipped with a laser device must comply with International Electrotechnical Commission (IEC) 60825.

20.1 Mesures de Sécurité

Veuillez suivre les mesures de sécurité suivantes pour éviter tout accident corporel et ne pas endommager ce produit ou tout autre produit lui étant connecté. Pour éviter tout danger, veillez à utiliser le produit conformément aux spécifications mentionnées.

Lisez toutes les informations de sécurité fournies dans les manuels de l'utilisateur des produits composants et veillez à bien comprendre les mesures associées aux symboles de sécurité, aux avertissements écrits et aux mises en garde avant d'accéder à certains éléments ou emplacements de l'unité. Conservez ce document comme outil de référence.

IMPORTANT : reportez-vous aux instructions d'installation avant de connecter le bloc d'alimentation.

Pour réduire le risque d'un choc électrique en provenance d'un téléphone ou d'un système Ethernet*, connectez l'alimentation principale de l'unité avant d'établir ces connexions. De même, déconnectez-les avant de couper l'alimentation principale de l'unité.

Avertissement : évitez toute forme de surcharge, chaleur, choc électrique ou incendie. Connectez uniquement le système à un circuit d'alimentation dûment répertorié conformément aux spécifications du manuel de l'utilisateur du produit. N'établissez pas de connexions à des terminaux en dehors des limites spécifiées pour ce terminal. Reportez-vous au manuel de l'utilisateur du produit pour les connections adéquates.

Avertissement : évitez les chocs électriques. N'utilisez pas ce produit dans des endroits humides, mouillés ou provoquant de la condensation. Pour éviter tout risque de choc électrique ou d'incendie, n'utilisez pas ce produit si les couvercles ou les panneaux du boîtier ne sont pas en place.

Avertissement : évitez les chocs électriques. Pour les unités comportant plusieurs sources d'alimentation, déconnectez toutes les sources d'alimentation externes avant de procéder aux réparations.

Attention : exigences environnementales du système : les composants tels que les cartes de processeurs, les commutateurs Ethernet, etc., sont conçus pour fonctionner avec un flux d'air externe. Les composants peuvent être détruits s'ils fonctionnent dans d'autres conditions. Le flux d'air externe est généralement produit par les ventilateurs des châssis lorsque les composants sont installés dans des châssis compatibles. Veillez à ne jamais obstruer le flux d'air alimentant le ventilateur ou les conduits de l'unité. Des boucliers ou des panneaux de gestion de l'air doivent être installés dans les connecteurs inutilisés du châssis. Les spécifications environnementales peuvent varier d'un produit à un autre. Veuillez-vous reporter au manuel de l'utilisateur pour déterminer les exigences en matière de flux d'air et d'autres spécifications environnementales.

Avertissement : les dissipateurs de chaleur de l'appareil peuvent être chauds lors d'un fonctionnement normal. Pour éviter tout risque de brûlure, veillez à ce que rien n'entre en contact avec les dissipateurs de chaleur.

Avertissement : évitez les blessures, les incendies ou les explosions. N'utilisez pas ce produit dans une atmosphère présentant des risques d'explosion.

Avertissement : évitez les blessures. Ce produit peut contenir un ou plusieurs périphériques laser visuellement accessibles en fonction des modules plug-in installés. Les produits équipés d'un périphérique laser doivent être conformes à la norme IEC (International Electrotechnical Commission) 60825.

20.2 Sicherheitshinweise

Lesen Sie bitte die folgenden Sicherheitshinweise, um Verletzungen und Beschädigungen dieses Produkts oder der angeschlossenen Produkte zu verhindern. Verwenden Sie das Produkt nur gemäß den Anweisungen, um mögliche Gefahren zu vermeiden.

Lesen Sie alle Sicherheitsinformationen in den Benutzerhandbüchern der zu dem Produkt gehörenden Komponenten und machen Sie sich mit den Hinweisen zu den Sicherheitssymbolen, schriftlichen Warnungen und Vorsichtsmaßnahmen vertraut, ehe Sie Teile oder Stellen des Geräts anfassen. Bewahren Sie dieses Dokument gut auf, um später darin nachlesen zu können.

WICHTIG: Lesen Sie vor dem Anschließen der Stromversorgung die Installationsanweisungen!

Um die Gefahr eines durch ein Telefon oder Ethernet*-System bedingten elektrischen Schlags zu verringern, schließen Sie das Stromkabel des Geräts an, ehe Sie diese Verbindungen einrichten. Trennen Sie diese Verbindungen, ehe Sie die Hauptstromversorgung des Geräts unterbrechen.

Warnung: Vermeiden Sie elektrische Überlastung, Hitze, elektrischen Schlag oder Feuergefahr: Schließen Sie das System nur an einen den Spezifikationen des Produkt-Benutzerhandbuchs entsprechenden Stromkreis an. Stellen Sie keine Verbindung zu Terminals her, die nicht den jeweiligen Spezifikationen entsprechen. Für die korrekten Verbindungen siehe das Benutzerhandbuch des Produkts.

Warnung: Vermeiden Sie einen elektrischen Schlag: Unterlassen Sie den Betrieb in nassen, feuchten oder kondensierenden Betriebsumgebungen. Um die Gefahr eines elektrischen Schlags oder eines Feuers zu vermeiden, betreiben Sie dieses Produkt nicht ohne Gehäuse oder Abdeckungen.

Warnung: Vermeiden Sie einen elektrischen Schlag: Trennen Sie bei Geräten mit mehreren Stromquellen vor der Wartung alle externen Stromverbindungen.

Vorsicht: Anforderungen an die Systemumgebung: Komponenten wie Prozessor-Boards, Ethernet-Schalter usw. sind auf den Betrieb mit externer Luftzufuhr ausgelegt. Diese Komponenten können bei Betrieb ohne externe Luftzufuhr beschädigt werden. Wenn die Komponenten in einem kompatiblen Gehäuse installiert sind, wird Luft von außen normalerweise durch Gehäuselüfter zugeführt. Blockieren Sie niemals die Luftzufuhr der Gerätelüfter oder -ventilatoren. In ungenutzten Gehäusesteckplätzen müssen Füllelemente oder Luftsteuerungseinheiten eingesetzt werden. Die Betriebsbedingungen können zwischen den verschiedenen Produkten variieren. Für die Anforderungen an die Belüftung und andere Betriebsbedingungen siehe die Benutzerhandbücher der jeweiligen Produkte.

Warnung: Die Kühlkörper des Geräts können sich während des normalen Betriebs erhitzen: Um Verbrennungen zu vermeiden, sollte jeder Kontakt mit den Kühlkörpern vermieden werden.

Warnung: Vermeiden Sie Verletzungen, Feuergefahr oder Explosionen: Unterlassen Sie den Betrieb dieses Produkts in einer explosionsgefährdeten Betriebsumgebung.

Warnung: Vermeiden Sie Verletzungen: Dieses Produkt kann ein oder mehrere Lasergeräte enthalten, die abhängig von den installierten Plug-In-Modulen optisch zugänglich sind. Mit einem Lasergerät ausgestattete Produkte müssen der International Electrotechnical Commission (IEC) 60825 entsprechen.

20.3 Norme di Sicurezza

Leggere le norme seguenti per prevenire lesioni personali ed evitare di danneggiare questo prodotto o altri a cui è collegato. Per evitare qualsiasi pericolo potenziale, usare il prodotto unicamente come indicato.

Leggere tutte le informazioni sulla sicurezza fornite nella guida per l'utente relativa al componente e comprendere le norme associate ai simboli di pericolo, agli avvisi scritti e alle precauzioni da adottare prima di accedere a componenti o aree dell'unità. Custodire il presente documento per usi futuri.

IMPORTANTE: prima di collegare l'unità alla fonte di alimentazione, leggere le istruzioni di installazione.

Per ridurre il rischio di scariche elettriche da parte della linea telefonica o dalla rete Ethernet*, collegare l'unità all'alimentazione principale prima di effettuare tale collegamento. Rimuovere i collegamenti prima di togliere l'alimentazione principale all'unità.

Avvertenza: evitare sovraccarichi elettrici, calore diretto, scosse e possibili cause di incendio. Collegare il sistema solo ad una rete elettrica la cui tensione nominale corrisponda al valore indicato nella guida per l'utente. Non collegarlo a fonti di alimentazione con valori di tensione esterne a quanto specificato per il sistema. Per ulteriori informazioni sul corretto collegamento, consultare la guida per l'utente del prodotto.

Avvertenza: evitare le scosse elettriche. Non usare l'apparecchio in ambienti umidi o in presenza di condensa. Per evitare scosse elettriche o possibili cause di incendio, non adoperare il prodotto senza le custodie o i pannelli appositi.

Avvertenza: evitare le scosse elettriche. Prima di intervenire su unità con più fonti di alimentazione, rimuovere tutti i collegamenti all'alimentazione esterna.

Attenzione: rispettare i requisiti ambientali del sistema. I componenti come le schede di processore, i commutatori Ethernet, ecc., sono progettati per funzionare in presenza di un flusso di aria proveniente dall'esterno, in assenza del quale rischiano di danneggiarsi irrimediabilmente. In genere, il flusso di aria esterno viene generato da appositi ventilatori installati contemporaneamente ai componenti nello chassis compatibile. Non ostacolare mai il flusso di aria convogliato dal ventilatore e dai condotti dell'unità. I pannelli di copertura o le schede per il controllo dell'aria devono essere installati negli alloggiamenti vuoti dello chassis. I requisiti ambientali possono variare a seconda del prodotto. Per ulteriori informazioni sui requisiti del flusso di aria e sugli altri requisiti ambientali, consultare la guida per l'utente del prodotto.

Avvertenza: i dissipatori di calore possono scaldarsi durante il funzionamento normale. Per evitare bruciature o danni, evitare il contatto del dissipatore di calore con qualsiasi altro elemento.

Avvertenza: evitare lesioni, possibili cause di incendio o di esplosione. Non usare il prodotto in un'atmosfera in cui sussiste il rischio di esplosione.

Avvertenza: evitare le lesioni. Questo prodotto può contenere uno o più dispositivi laser accessibili alla vista, a seconda dei moduli installati. I prodotti provvisti di un dispositivo laser devono essere conformi alla norma 60825 della Commissione elettrotecnica internazionale (IEC).

20.4 Instrucciones de Seguridad

Examine las instrucciones sobre condiciones de seguridad que siguen para evitar cualquier tipo de daños personales, así como para evitar perjudicar el producto o productos a los que esté conectado. Para evitar riesgos potenciales, utilice el producto únicamente en la forma especificada.

Lea toda la información relativa a seguridad que se incluye en los manuales de usuario de los distintos componentes y procure familiarizarse con los distintos símbolos de seguridad, advertencias escritas y normas de precaución antes de manipular las distintas piezas o secciones de la unidad. Guarde este documento para consultarlo en el futuro.

IMPORTANTE: Consulte las instrucciones de instalación antes de conectar la unidad a la alimentación.

Para reducir los riesgos de descargas eléctricas a través de un teléfono o un sistema de Ethernet*, conecte la alimentación principal de la unidad antes de realizar este tipo de conexiones. Desconecte estas conexiones antes de desconectar la alimentación principal de la unidad.

Advertencia: Evite sobrecargas eléctricas, calor y riesgos de descarga eléctrica o incendio: Conecte el sistema sólo a un circuito de alimentación que tenga el régimen apropiado, según lo especificado en el manual de usuario del producto. No realice conexiones con terminales cuya capacidad no se ajuste al régimen especificado para ellos. Consulte el manual de usuario del producto para que las conexiones que realice sean las correctas.

Advertencia: Evite descargas eléctricas: No haga funcionar el sistema en condiciones de humedad, mojado o si se produce condensación de la humedad. Para evitar descargas eléctricas o posibles incendios, no permita que el aparato funcione con sus tapas o paneles del chasis desmontados.

Advertencia: Evite descargas eléctricas: En el caso de unidades que cuenten con varias fuentes de alimentación, desconecte las conexiones con alimentación externa antes de proceder a realizar labores de mantenimiento.

Precaución: Requisitos de entorno para el sistema: Los componentes del tipo de placas de procesador, conmutadores de Ethernet, etc., están concebidos para funcionar en condiciones que permitan el paso de aire. Los componentes pueden averiarse si funcionan sin que circule el aire en su entorno. La circulación del aire suele estar facilitada por los ventiladores incorporados en el armazón cuando los componentes están instalados en armazones compatibles. Nunca interrumpa el paso del aire por los ventiladores or los respiraderos. Los paneles de relleno y las placas para el control de la circulación del aire deben instalarse en ranuras del chasis que no estén destinadas a ningún otro uso. Las características técnicas relativas al entorno pueden variar entre productos. Consulte los manuales de usuario del producto si necesita conocer sus necesidades en términos de circulación de aire u otras características técnicas.

Advertencia: En condiciones de funcionamiento normales, los disipadores de calor pueden recalentarse. Evite que ningún elemento entre en contacto con los disipadores para evitar quemaduras.

Advertencia: Riesgos de daños, incendio o explosión: No permita que el aparato funcione en una atmósfera que presente riesgos de explosión.

Advertencia: Daños personales: Este producto puede contener uno o varios dispositivos láser, que estarán a la vista dependiendo de los módulos enchufables que se hayan instalado. Los productos provistos de un dispositivo láser deben ajustarse a la norma 60825 de la International Electrotechnical Commission (IEC).

20.5 Chinese Safety Warning

系统信息

请阅读以下警告信息，以避免人身伤害并防止损坏本产品或与之相连的产品。为避免潜在的危险，请仅按规定使用产品。

在接近设备中的部件或元件之前，请阅读在组件产品用户手册中载明的所有安全信息并了解与安全标志、书面警告及注意事项有关的预防措施。请保存本文档以备将来参考。

和（或）直流电源安全警告： 和（或）直流电源线是设备的主要 和（或）直流电连接装置，任何时候均必须方便取用。辅助 和（或）直流电开关和（或）断路器开关仅用于控制电源（非主要断电装置）。

重要：在连接到电源前，请先参阅安装说明。

对于直流电系统，本设备要求建筑物安装短路（过电流）保护装置。请确保在所有载流导线中使用不大于 72VDC、15A，经过认证和鉴定的保险丝或断路器。对于永久连接设备，应在建筑物布线中安装便于断开的装置。对于永久连线，应使用系统用户手册中指定的标准铜线。

机壳配备了单独的接地接线柱。请先接好接地线后再通电或连接其它线路，在通电或接通周边电线时，切勿断开接地线。

为降低电话或 Ethernet* 系统电击的危险，请在连接设备主电源后，再连接其它线路；在从设备上卸下主电源前，请先断开这些线路。

机架装配或机壳的安全性： 本设备采用固定机架装配。机架装配的设计符合 NEBS GR-63-CORE 和 NEBS GR 487 的机械强度要求。在机架上安装或拆卸设备前，务必断开所有电源和外部连线。

卸下所有热交换设备可最大限度地减少系统重量。小心装配系统以确保机架载重均衡，载重分配不均衡可能导致危险情况发生。当机架上安装机壳时，请上紧所有装配螺栓。

警告：请检查电源线与电源插座是否兼容。 请使用与电源插座配置对应的电源线。有关详情，请访问下面的网址：http://kropla.com/electric2.htm.

警告：避免电力过载、过热、电击或火灾： 仅将系统连接到产品用户手册中指定的适当额定供电电路。请勿连接到超出接线端规定范围的接线端。有关正确连接，请参阅产品用户手册。

警告：避免电击： 请勿在潮湿或冷凝条件下运行。为避免电击或火灾，请勿在卸下机壳或面板的情况下使用本产品。

警告：避免电击： 对于具有多个电源的设备，请在维修前断开所有外部电源连接。

警告：更换电源只能由合格的维修人员进行。

注意：系统环境要求： 处理器插件板、以太网开关等组件要求在外部空气流通的环境下工作。在没有外部空气流通的情况下操作，可能会损坏组件。当组件安装在封闭机箱中时，外部气流通常是由机箱风扇提供的。切勿阻碍气流通过的设备风扇或通风口。在不使用的机箱插槽中，必须安装填充板或空气控制板。环境规范因特定产品而异。有关气流要求和其它环境规范，请参阅产品用户手册。

警告：设备散热片在正常运行期间可能发热。 为避免燃烧，请勿让任何物体接触散热片。

警告：避免人身伤害、火灾或爆炸： 切勿在可能引起爆炸的环境中使用本产品。

注意：锂电池不是可现场更换的部件。 如果更换或处理不当，可能会引起爆炸。切勿拆掉电池或对电池充电，切勿让电池靠近火源。更换电池时，必须使用制造商建议的相同类型或同等类型的电池。旧电池必须按照制造商的指示加以处理，并将电池退回给英特尔修理。

警告：避免损伤： 本产品可能包含一个或多个激光装置，是否可见取决于所安装的插件模块。装有激光装置的产品必须遵循国际电工委员会 (IEC) 60825 号规定。

Appendix A Reference Documents

The following documents should be available when using this specification. Documents that are not available on web sites can be obtained from your IBL (Intel Business Link) account, or by contacting your Intel Field Sales Engineer (FSE) or Field Application Engineer (FAE).

- AdvancedTCA* Specification (http://www.advancedtca.org)
- PICMG* Advanced Mezzanine Card AMC.0 Specification D0.97, September, 2004 (http://www.picmg.org)
- Renesas* H8S/2168 Group Product Specification (http://www.renesas.com/fmwk.jsp?cnt=h8s2168_root.jsp&fp=/products/mpumcu/h8s_family/h8s2100_series/h8s2168_group/)
- Zarlink* ZL30410 Multi-service Line Card PLL Product Information (http://products.zarlink.com/product_profiles/ZL30410.htm)
- Vitesse* VSC3108 8x8 Crosspoint Switch (http://www.vitesse.com/products/product.php?number=VSC3108)

The following Intel Corporation documents may be required for more detailed information:

- Intel® 6300ESB I/O Controller Hub Datasheet (http://www.intel.com/design/chipsets/embedded/docs/6300esb.htm)
- Intel® 6700PXH 64-bit PCI Hub Datasheet (http://www.intel.com/design/chipsets/embedded/docs/e7520.htm)
- Intel® 82546GB Gigabit Ethernet Controller Datasheet (http://www.intel.com/design/network/products/lan/controllers/82546gb.htm)
- Intel® 82551ER Fast Ethernet PCI Controller Datasheet (http://www.intel.com/design/network/datashts/82551ER_ds.htm)
- Intel® E7520 Chipset Datasheet: Intel E7520 Memory Controller Hub (MCH) (http://www.intel.com/design/chipsets/embedded/docs/e7520.htm)
- Intel® Boot Agent. (http://www.intel.com/support/network/adapter/pro100/bootagent/manual.htm)
- Intel NetStructure® MPCHC0001 14U Shelf Technical Product Specification (http://www.intel.com/design/network/products/cbp/atca/MPCHC0001.htm)
- Intel NetStructure® MPCMM0001 Chassis Management Module Hardware Technical Product Specification (http://www.intel.com/design/network/products/cbp/atca/mpcmm0001.htm)
- Intel NetStructure® MPCMM0001 Chassis Management Module Software Technical Product Specification (http://www.intel.com/design/network/products/cbp/atca/mpcmm0001.htm)
- Intel AdvancedTCA product line (http://developer.intel.com/technology/atca/)
- Intelligent Platform Management Interface v1.5 Specification (http://developer.intel.com/design/servers/ipmi/spec.htm)
- IPMI Platform Management FRU Information Storage Definition V1.0 Document Revision 1.1(http://developer.intel.com/design/servers/ipmi/spec.htm)
- Intelligent Platform Management Interface Implementer's Guide (http://developer.intel.com/design/servers/ipmi/spec.htm)
- ITP700 Debug Port Design Guide (http://www.intel.com/design/xeon/documentation.htm)

- Low Pin Count (LPC) Interface specification (http://www.intel.com/design/chipsets/industry/lpc.htm)
- Low Voltage Intel® Xeon™ Processor Datasheet (http://www.intel.com/design/xeon/documentation.htm)
- Low Voltage Intel® Xeon™ Processor Product Page (http://www.intel.com/products/server/processors/server/xeon/index.htm?iid=ipp_srvr_proc+xeon512kb&)

Appendix B List of Supported Commands (IPMI v1.5 and PICMG 3.0)

Table 153. IPMI 1.5 Supported Commands (Sheet 1 of 2)

IPM Device Global Commands			
Command	**NetFn[1]**	**CMD**	**IPMI 1.5 Spec Func**
Get Device ID[1]	App	01h	17.1
Cold Reset	App	02h	17.2
Get Self Test Results	App	04h	17.4
Broadcast "Get Device ID"	App	TBD	17.9
BMC Watchdog Timer Commands			
Command	**NetFn[1]**	**CMD**	**IPMI 1.5 Spec Func**
Reset Watchdog Timer	App	22h	21.5
Set Watchdog Timer	App	24h	21.6
Get Watchdog Timer	App	25h	21.7
BMC Device and Messaging Commands			
Command	**NetFn[1]**	**CMD**	**IPMI 1.5 Spec Func**
Set IPMC Global Enables	App	2Eh	18.1
Get IPMC Global Enables	App	2Fh	18.2
Clear Message Flags	App	30h	18.3
Get Message Flags	App	31h	18.4
Get Message Flags	App	33h	18.6
Send Message	App	34h	18.7
Read Event Message Buffer	App	35h	18.8
Event Commands			
Command	**NetFn[1]**	**CMD**	**IPMI 1.5 Spec Func**
Set Event Receiver	S/E	00h	23.1
Get Event Receiver	S/E	01h	23.2
Platform Event (Event Message)	S/E	02h	23.3
Sensor Device Commands			
Command	**NetFn[1]**	**CMD**	**IPMI 1.5 Spec Func**
Get Device SDR Info	S/E	20h	29.2
Get Device SDR	S/E	21h	29.3
Sensor Device Commands			
Command	**NetFn**	**CMD**	**IPMI 1.5 Spec Func**
Reserve Device SDR Repository	S/E	22h	29.4
Set Sensor Hysteresis	S/E	24h	29.6

Table 153. IPMI 1.5 Supported Commands (Sheet 2 of 2)

Get Sensor Hysteresis	S/E	25h	29.7
Set Sensor Threshold	S/E	26h	29.8
Get Sensor Threshold	S/E	27h	29.9
Set Sensor Event Enable	S/E	28h	29.10
Get Sensor Event Enable	S/E	29h	29.11
Get Sensor Reading	S/E	2Dh	29.14
FRU Device Commands			
Command	**NetFn**	**CMD**	**IPMI 1.5 Spec Func**
Get FRU Inventory Area Info	Storage	10h	28.1
Read FRU Data	Storage	11h	28.2
Write FRU Data	Storage	12h	28.3

Note: [1]For Get Device ID:
The SDR version and Maintenance Release number are available in the "Auxilliary Firmware Revision' field in the response to the IPMI Get Device ID command. Bytes 13:16 are populated as described below:
Byte 13: SDR release that holds the SDR version and any board-specifc change (Specific command and specific Hardare Abstraction Layer): value 0 to 255
Byte 14: Not used, set to 0
Byte 15: Maintenance Release: value 0 to 255
Byte 16: Not used, set to 0

Table 154. PICMG 3.0 IPMI Supported Commands

Command	NetFn	Command	Interface
Get PICMG Properties	2Ch	00h	SMS/SMM/IPMB
Get Address Info	2Ch	01h	SMS/SMM/IPMB
FRU Control	2Ch	04h	SMS/SMM/IPMB
Get FRU LED Properties	2Ch	05h	SMS/SMM/IPMB
Get LED Color Properties	2Ch	06h	SMS/SMM/IPMB
Set FRU LED State	2Ch	07h	SMS/SMM/IPMB
Get FRU LED State	2Ch	08h	SMS/SMM/IPMB
Set IPMB State	2Ch	09h	SMS/SMM/IPMB
Set FRU Activation Policy	2Ch	0Ah	IPMB
Get FRU Activation Policy	2Ch	0Bh	SMS/SMM/IPMB
Set FRU Activation	2Ch	0Ch	SMS/SMM/IPMB
Get Device Locator Record ID	2Ch	0Dh	SMS/SMM/IPMB
Set Port State	2Ch	0Eh	IPMB
Get Port State	2Ch	0Fh	SMS/SMM/IPMB
Compute Power Properties	2Ch	10h	SMS/SMM/IPMB
Set Power Level	2Ch	11h	IPMB
Get Power Level	2Ch	12h	SMS/SMM/IPMB

Notes:
1. If a command is received over an invalid interface, a completion code of insufficient privilege level (D4h) is returned.