OCPRF100 MP Server System

Supporting Up To Eight Intel$^{®}$ Pentium$^{®}$ III Xeon$^{™}$ Processors

Technical Product Specification

Intel Order #753674-001
Revision 1.0

Revision History

Date	Rev.	Modifications
September, 1999	1.0	Initial release.

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1. Introduction

This document provides an overview of the OCPRF100 MP server system and includes information on cabling, connectors, power supply, and regulatory requirements.

Document Structure and Outline

This document is organized into ten chapters:

Chapter 1: **Introduction**
Provides an overview of this document.

Chapter 2: **Server System Chassis and Assemblies**
Provides an overview of the chassis hardware.

Chapter 3: **System Overview**
Provides an overview of the system hardware.

Chapter 4: **Cables and Connectors**
Describes the cables and connectors used to interconnect the OPRF100 board set and the server system components.

Chapter 5: **Power Supply**
Describes the specifications for the 750-W power supply.

Chapter 6: **OCPRF100 MP Server Software**
Provides an overview of the system software.

Chapter 7: **Regulatory Specifications**
Describes system compliance to regulatory specifications.

Chapter 8: **Peripheral Bay Backplane Board**
Describes the features and functionality of the peripheral bay backplane board.

Chapter 9: **Peripheral Bay Board (Chassis Side)**
Describes the design of the peripheral bay board (chassis side).

Chapter 10: **Front Panel**
Describes the design and external interface of the OCPRF100 MP server system front panel.

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2. Server System Chassis and Assemblies

This chapter describes the chassis and assembly pieces that reside within the chassis. This chapter is divided into the following areas:

- Front panel assembly
- Peripheral bay
- Top cover assembly
- Fan bay
- Front panel board
- Processor mezzanine board
- Processor retention mechanism
- Profusion® carrier tray
- Midplane assembly
- I/O carrier assembly
- Power supply
- OCPRF100 MP server system chassis
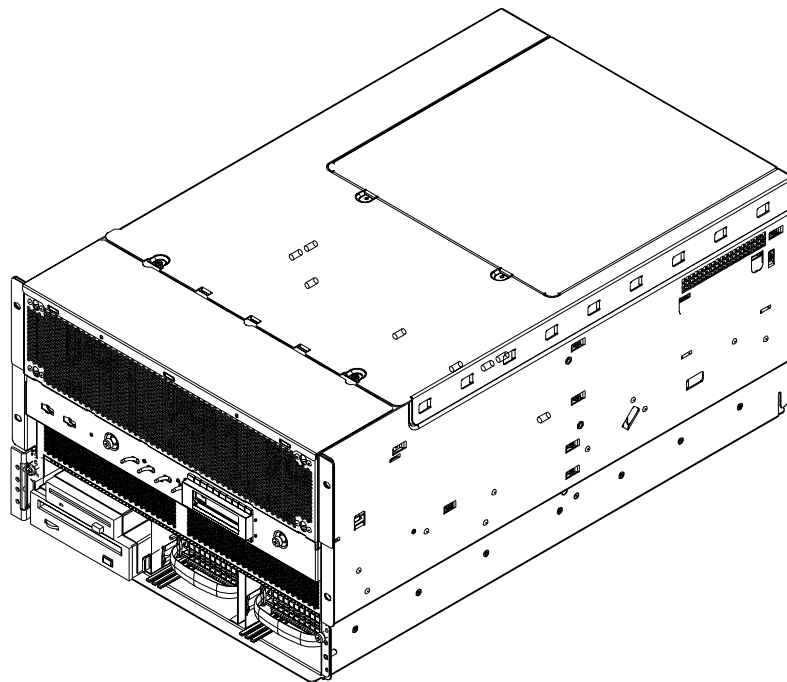
Figure 2-1: OCPRF100 MP Server System Chassis

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2.1   Front Panel Assembly

The front panel assembly consists of an upper and lower bezel. The bezels serve as cosmetic pieces only, and can be integrator specific. Finger grips are provided to make it easy to remove the bezels. Removing the bezels exposes the front side of the fan bay, the front panel controller (FPC) switches (power, reset, and nonmaskable interrupt (NMI)), as well as the indicator lights (power indicator, predictive power supply failure, predictive fan failure, and hard drive failure). From this location, the hot-swap hard drives and/or the peripheral bay may be removed from the system.
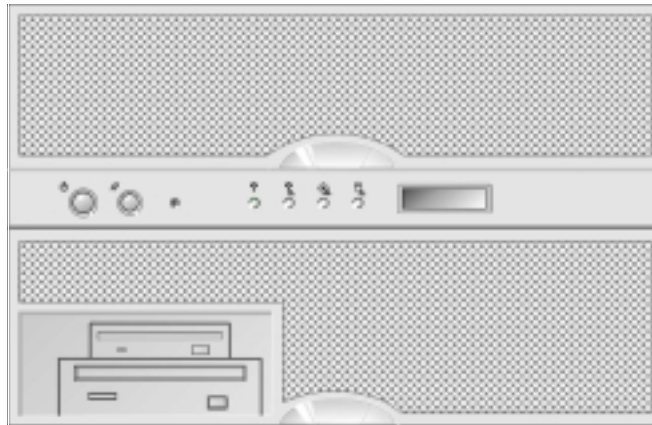
Figure 2-2: Front Panel

2.2   Peripheral Bay

The peripheral bay is defined to be a customer specific, removable device capable of supporting a floppy drive, dual hot-swap hard drives, and a low-voltage differential SCSI (LVDS) or single ended SCSI device. The integrator has the option of defining the size and capacity of the hard drives, as well as deciding whether the LVDS will support CD-ROM, tape, or other device. A single ended SCSI channel is provided for support of a SCSI device, should the integrator so desire.

The peripheral bay is designed to be easily added and removed from the front of the server by removing the front cover and four mounting screws. The peripheral bay connects to the OPRF100 I/O carrier and the power supply via a blind mate board connector and cabling. The blind mate board is located in front of the midplane board, on the left side of the server (when viewing the server from the front). The blind mate connector connects to the peripheral bay's LVDS board upon insertion, thus connecting all peripheral devices to the I/O carrier.

The peripheral bay will contain a 1.4 MB floppy drive, space for a half-height 5 ¼ inch device (typically a CD-ROM), and has two bays designed to accommodate either a 1-inch or a 1.6-inch SCA hard drive.

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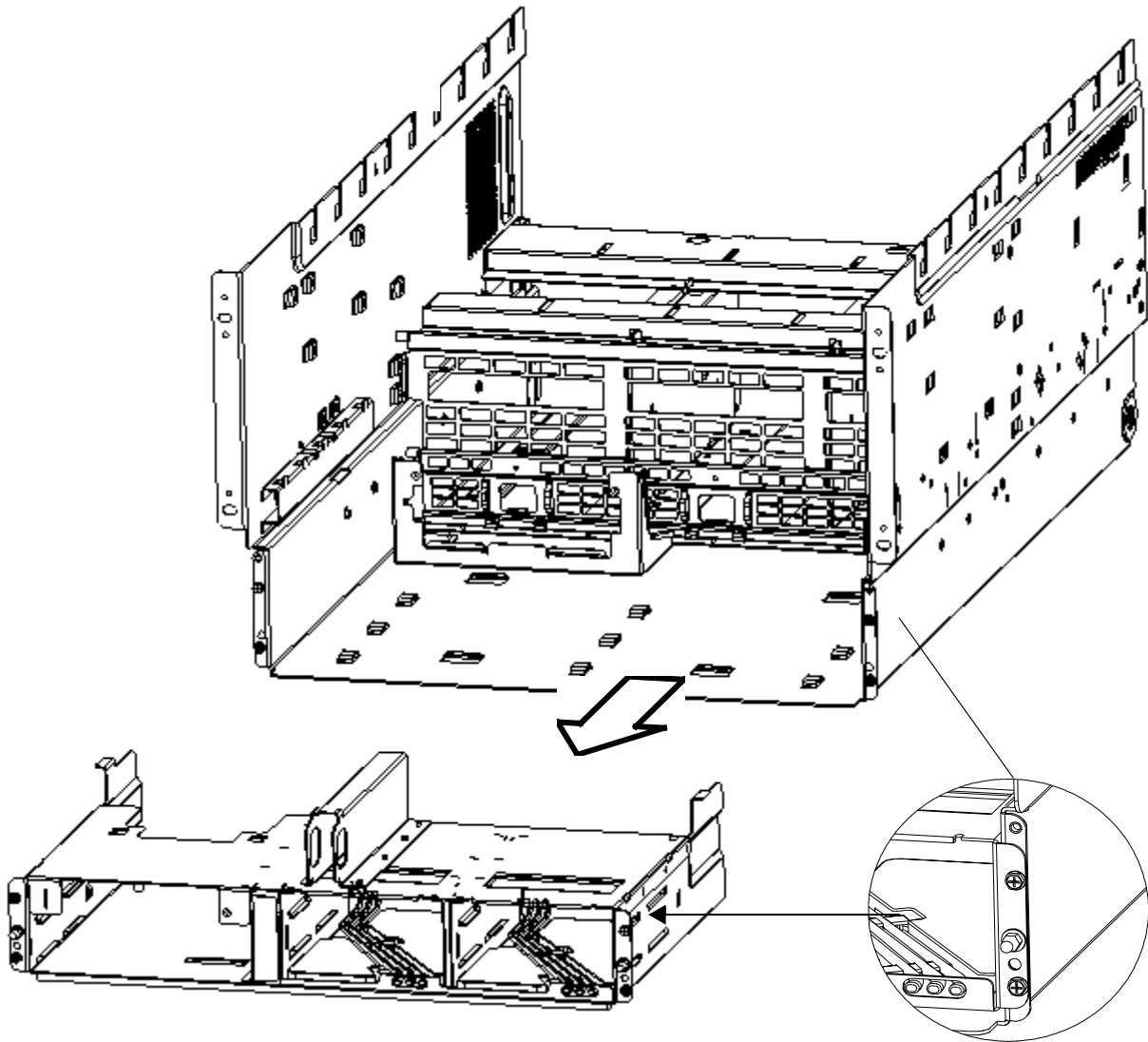
Figure 2-3: Peripheral Bay

2.3   Top Cover Assembly

The top cover assembly is released by removing the two retaining screws located on the top toward the front (E in Figure 2-4: Hot-plug PCI Access Door), between the fan bay assembly and the top cover assembly marked with the AC caution icon. The cover slides toward the rear of the server and then lifts straight up off of the server chassis, exposing the upper portion of the server for maintenance, upgrades, or adding components.

Tape and sheet metal work were done to the sides of the top cover assembly to provide a better gripping surface for easier removal and replacement of the top cover assembly. Care should be taken to avoid damage to the electromagnetic compatibility (EMC) gasket material on the inside of the top cover.

2.3.1   Hot-plug PCI Access Door

The hot-plug PCI access door is released by removing the two retaining screws (A in Figure 2-4: Hot-plug PCI Access Door) located on the top, middle area of the server. The cover slides toward the rear of the server and lifts straight up off of the server chassis, exposing the hot-plug PCI cards.

The hot-plug PCI access door is designed to maintain a flush surface with the top cover assembly, such that a vacuum-based hoist may be used during the assembly process.
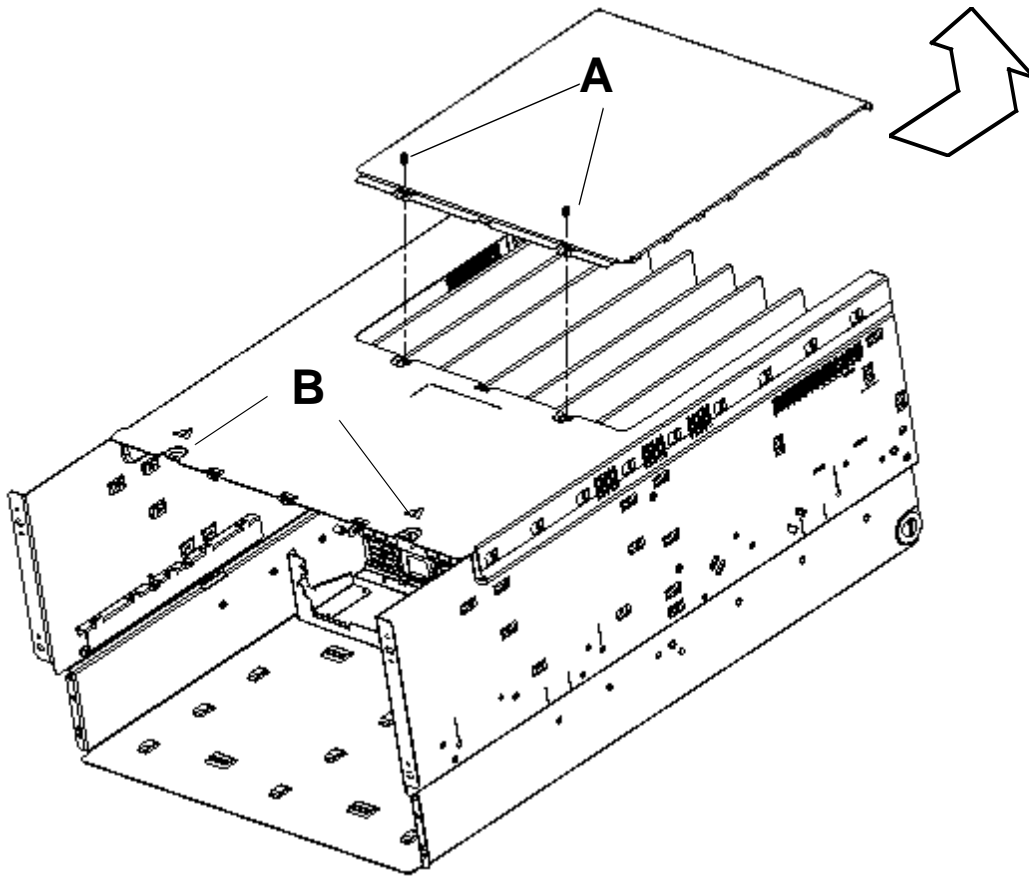
Figure 2-4: Hot-plug PCI Access Door

2.4   Fan Bay

The fan bay is a mechanical structure designed to contain six separate 120-mm cooling fans. These fans operate at a nominal voltage of 8.4 Vdc (2% tolerance) under normal conditions. Each fan produces a tachometer-based output to indicate the revolutions per minute (RPM) reading of the motor. Should a fan's tachometer output drop below a predefined normal range of operation, the FPC notifies the server management software that a fan has entered into the predictive fan failure condition. At this point, the fans will operate at an elevated voltage of approximately 12 Vdc.

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The fan bay will operate at high speed on the following conditions:

- Internal temperature has reached an elevated, but noncritical set-point.
- Ambient temperate exceeds 30°C.
- A fan has entered into the predictive failure mode.
- A fan has failed.

If the FPC detects a fan entering the predictive fan failure mode, the speed of all of the fans will be increased to maintain thermal requirements. The individual fans within the fan bay are all hot-swappable, meaning that they can be removed and inserted while the server is running. Server management will identify that a fan has either failed or has entered into the predictive failure mode. In both cases, the fan should be replaced immediately. Removal of a fan is accomplished by opening the fan bay cover and pulling (A) to lift the malfunctioning fan (B) out through the top of the server as shown in Figure 2-5: Fan Bay. The malfunctioning fan should then be replaced with a new fan. The system will detect that the fan has been replaced, and as long as no other thermal violations are currently occurring, the fan will resume operation at the reduced speed.
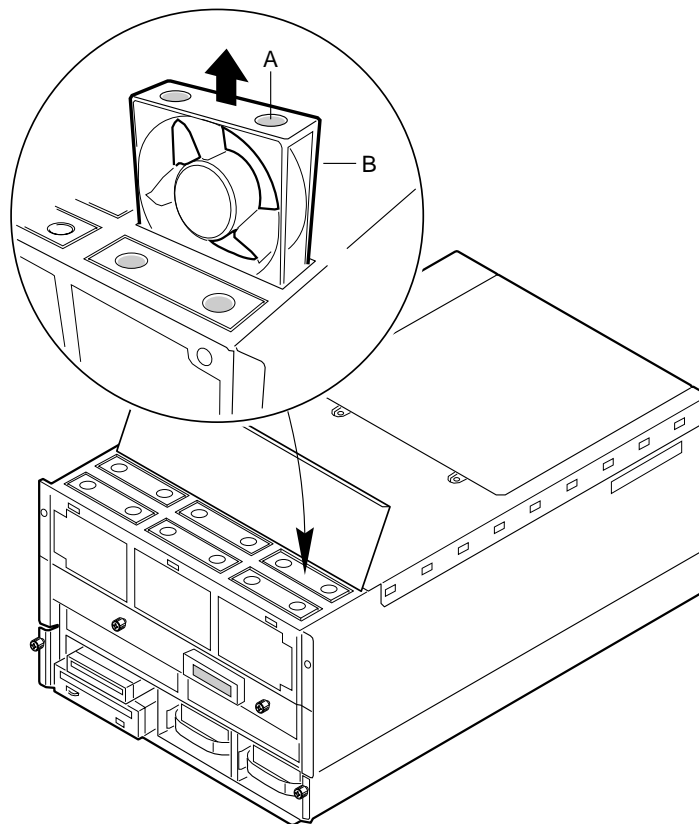
OM07304

Figure 2-5: Fan Bay

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Fans are installed with the connector on the left side facing down. The cavities in the fan bay are keyed to prevent a fan from being installed backwards.

The fan bay is installed after the Profusion carrier assembly is installed and completely seated into the midplane. The fan bay is lowered into the chassis until it is seated on the flanges of the Profusion tray. Two screw holes, one on each side, should now be aligned on the sides of the chassis. Insert screws into these holes to secure the fan bay into the chassis.

The fan bay cover is hinged at the rear and captivated by the system top cover assembly. Tabs in the rear of the fan bay cover engage with slots on the rear of the fan bay to secure the cover in normal operation. The fan bay cover is secured by one noncaptive screw located on the center of the cover's front flange. Remove the screw, slide the cover forward and lift. The cover remains open while servicing the fans.

To remove the fan bay from the chassis, it is first necessary to remove all individual fans from the fan bay. The fans plug directly into the front panel board and must be removed before the fan bay can be lifted out.

The fan bay cover provides critical electromagnetic interference (EMI) containment. To avoid electrical interference with adjacent equipment, close and secure the fan bay cover during normal system operation.

In systems with only one processor mezzanine board, an air baffle needs to be installed on the vacant side of the CPU retention cage to ensure proper cooling for the installed processors.

2.5   Front Panel Board

The FPC board provides power and monitors the tachometer readings from each individual fan within the fan bay. The FPC also serves as a platform for the server controller switches, and supports circuitry required for server management.

The FPC board is located on the same plane as, and connects to the Profusion carrier board via a connector. Both the FPC and Profusion carrier board are mounted to the topside of the Profusion carrier tray. On the left front edge of the FPC board are three push button switches—power, reset, and NMI. Each switch plunger has a small black cap on its end, which is necessary for the proper operation of the buttons on the front bezel.

To install an FPC board, tilt the board forward as shown in Figure 2-6: Front Panel Board Installation, and insert the switches into the openings on the front flange of the Profusion carrier tray. Lower the back of the board onto the standoffs on the tray. Align the board-to-board connectors and slide the board back to engage the connectors. Secure with nine screws. Reverse this operation to remove the board.
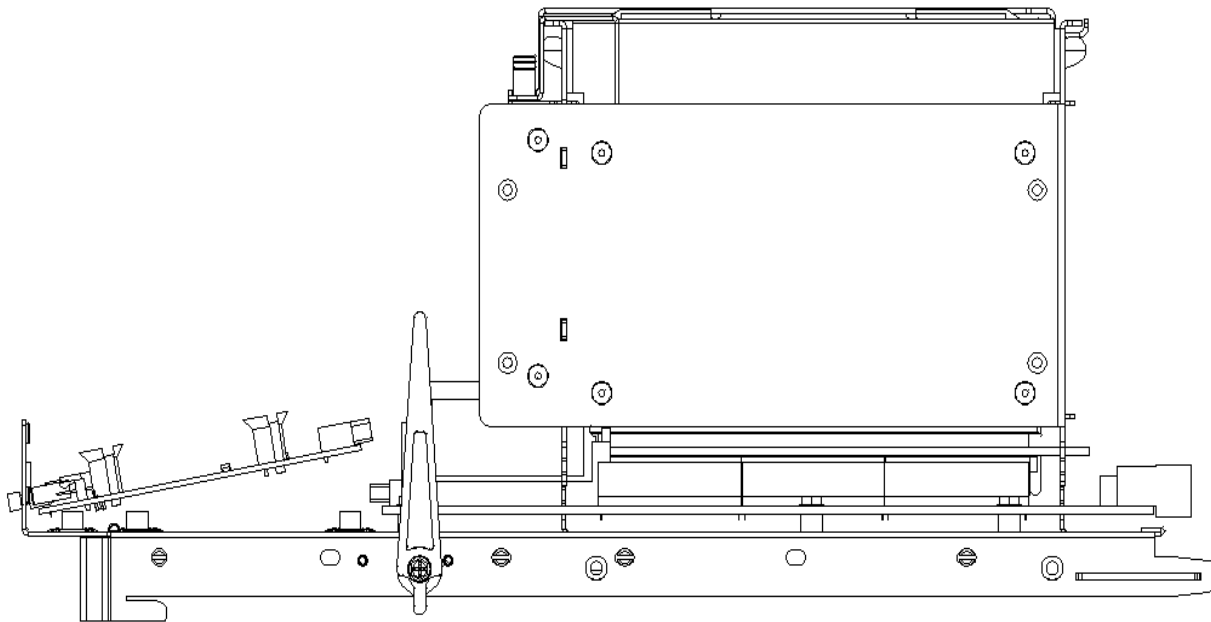
Figure 2-6: Front Panel Board Installation

2.6   Processor Mezzanine Board

The base configuration of an OCPRF100 MP server system consists of a single processor mezzanine board. The processor mezzanine board is designed to support one to four Pentium® III Xeon™ processors, providing power, ground and other connections to the processor(s) and to the Profusion carrier. The processor mezzanine board incorporates integrated voltage regulator modules (VRMs) to supply the internal voltage requirements to the processor cartridge.

2.7   Processor Retention Mechanism

The processors and termination cards are secured in their respective slots by means of the processor retention mechanism. The processor retention mechanism holds up to eight processors or termination cards. In the event the server is populated with only a single processor mezzanine card, the processor retention mechanism will be populated with a total of four contiguous processors and/or terminators.

A	B	C
Captive Screw	**Hold-down Strap**	**Air Baffle**
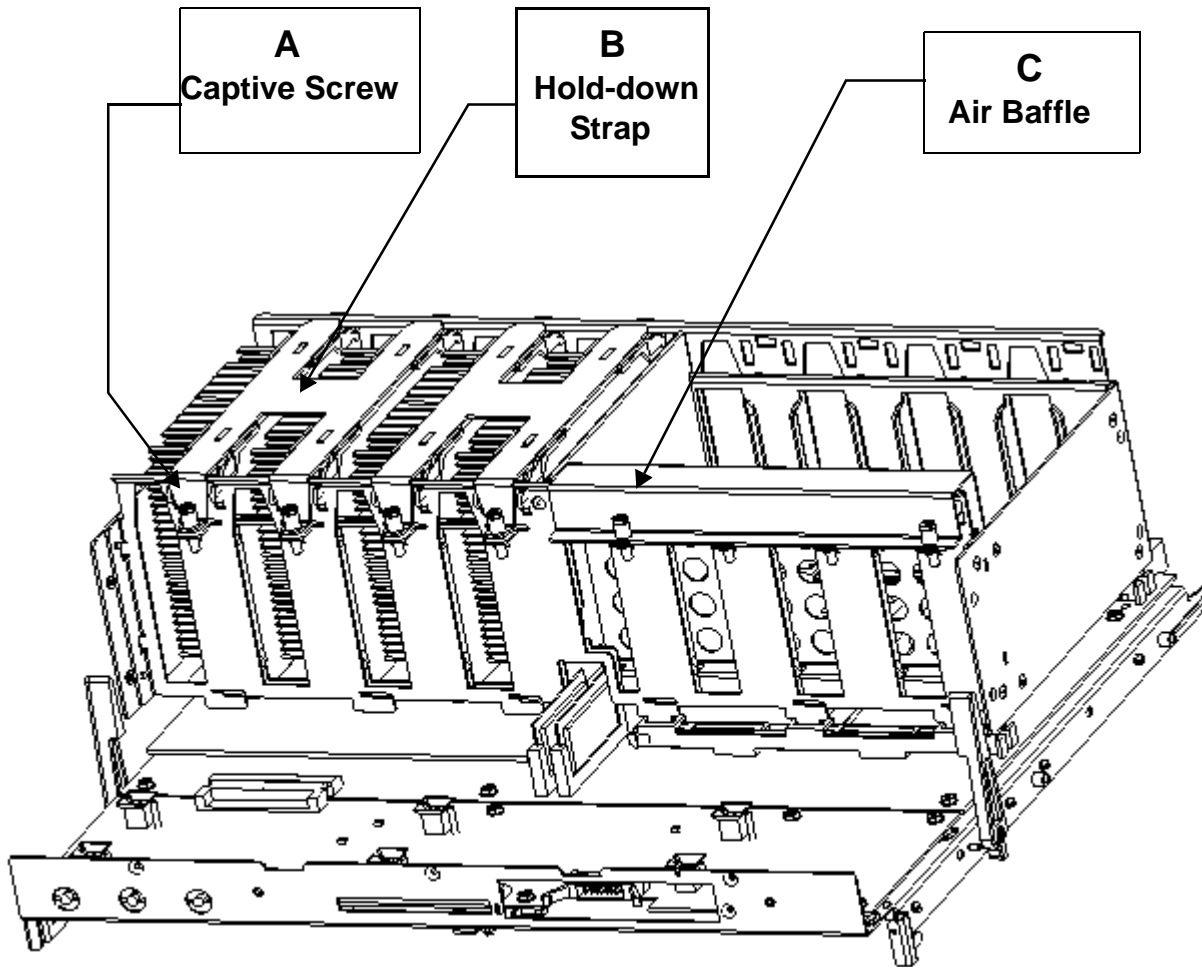
Figure 2-7: Processor Retention Mechanism

A processor/termination card pair is secured with a hold-down strap (B) that hooks into the back of the retention mechanism and is fastened at the front with two captive screws (A). (The retention strap is for a pair of processors or terminators). See Figure 2-7: Processor Retention Mechanism.

The processor retention mechanism is secured to the mezzanine boards with the same four lock bars that secure the mezzanine boards to the Profusion carrier board. In the event the server is populated with only a single processor mezzanine card, an air baffle (C) must be installed on the vacant side of the processor retention mechanism.

To remove or add a processor, first release the captive screws (A), then swing the retention strap (B) upward. Remove the terminator card, and install the processor. Replace the retention strap (B), and tighten the captive screw (A).

Due to space restrictions in the system, the Profusion carrier tray assembly must be removed from the chassis to install and service the mezzanine boards. The fan bay assembly must be removed prior to removing the Profusion carrier tray.

2.8   Profusion® Carrier Tray

The processor mezzanine boards plug into the Profusion carrier tray. The Profusion carrier tray serves as a platform to provide power and signals to the processor mezzanine board, route signals through the 1008-pin grand connector, and carry components of the Profusion chip set. Components of the Profusion chip set that reside on the Profusion carrier are the memory access controller (MAC) and the data interface buffer (DIB).

The Profusion chip set allows a five-port system data bus, with concurrent switching taking place. This is a requirement for an efficient eight-way server. The Profusion chip set will support two processor buses (each bus containing between one and four processors), two memory buses, and a single I/O bus. All of the buses operate at 100 MHz for maximum throughput. The data is routed through the Profusion tray, into the midplane connector for distribution to the appropriate source (memory carriers or the I/O carrier).
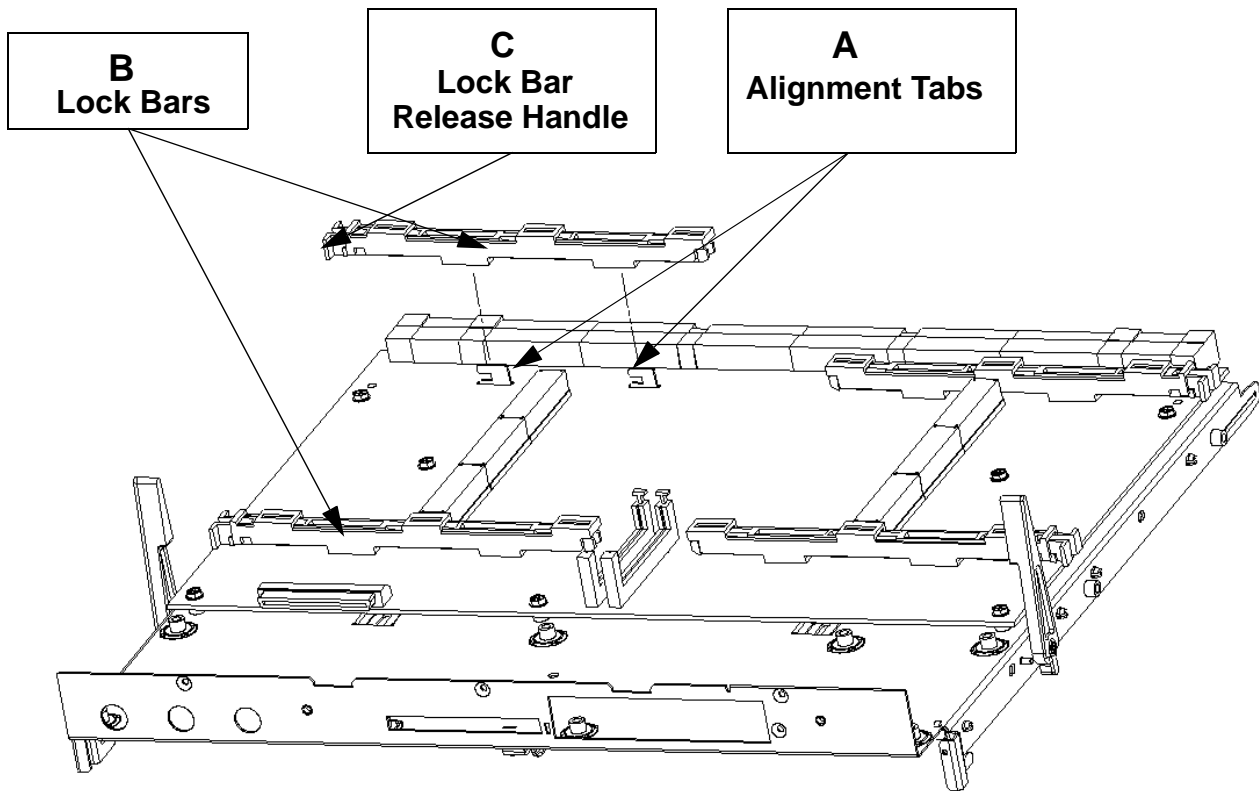
Figure 2-8: Profusion® Carrier Tray

Assembly of the Profusion carrier board, and mezzanine boards to the Profusion carrier tray, is performed outside the chassis. To start the assembly, install the Profusion carrier to the Profusion tray by aligning the eight tabs on the tray with the slots on the board (See Figure 2-8 (A)). Next, install the FPC board by passing the FPC switches through the switch openings in the tray and

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then moving back into place for connection to the Profusion carrier board. Place the four lock bars over the protruding tabs and onto the Profusion carrier board (B). The release handles of the lock bars (C) should be pointed to the outside of the board and they should be in the unlocked position. Place the first mezzanine board on the left side of the Profusion carrier board, oriented so the mezzanine board does not extend over the 1008-pin grand connector on the Profusion carrier board. Press down in the center of the mezzanine board until it is seated down onto the lock bars. If the configuration calls for a second mezzanine board, install it on the right side of the Profusion carrier board by following the same steps as described for the first board.
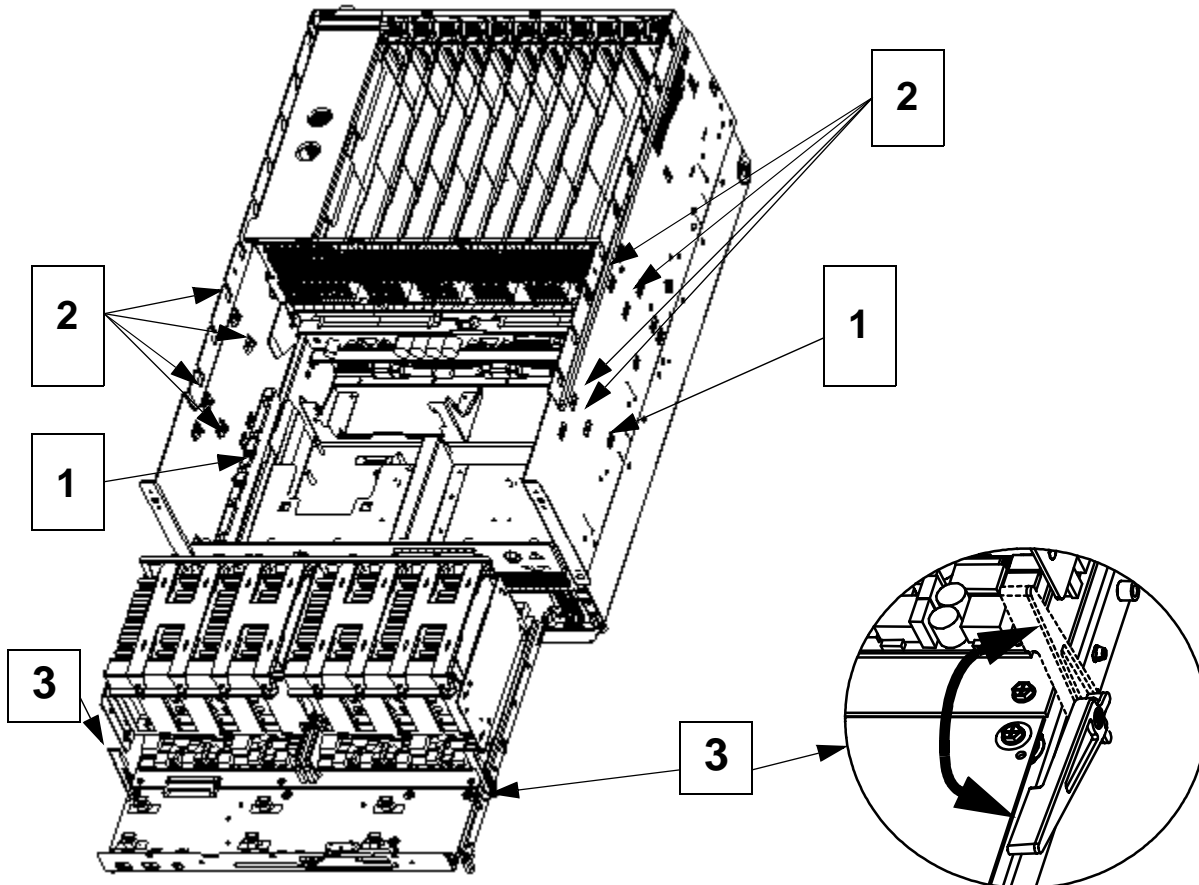
Figure 2-9: Profusion® Carrier Tray

Lower the processor retention mechanism onto the mezzanine board(s), aligning the hooks on its bottom with the slots in the mezzanine board(s). The processor retention mechanism should be oriented such that the center notch for the coherency filters is facing forward. Engage the four lock bars by pushing in on their ends until they click. The Profusion carrier tray assembly is now ready for installation in the chassis.

To install the Profusion carrier tray assembly into the chassis, set the tray on the tray supports on the inside walls of the chassis and slide it toward the midplane. The tray and chassis have self-aligning features to help guide the tray as it approaches the grand connector on the midplane. When the connectors are within approximateily 1" from connecting, check under the Profusion carrier tray for proper engagement of the center supports. The insertion/extraction levers (3) on the side of the tray should be tilted forward as the connectors approach each other. As the con-

nectors begin to engage, rotate the levers back until the connectors are fully engaged. Levers should be in an upright or near upright position. Secure the tray and the processor retention mechanism to the sides of the chassis with screws (1) and (2) as indicated in Figure 2-9.

2.9   Midplane Assembly

The midplane assembly serves as an interconnect between the power supplies, memory boards, Profusion carrier, and the I/O carrier. With the exception of limited server management and field replaceable unit (FRU) components, the midplane assembly serves merely as an interconnection device, routing the signals between the boards, while maintaining the signal integrity required for the 100-MHz buses.
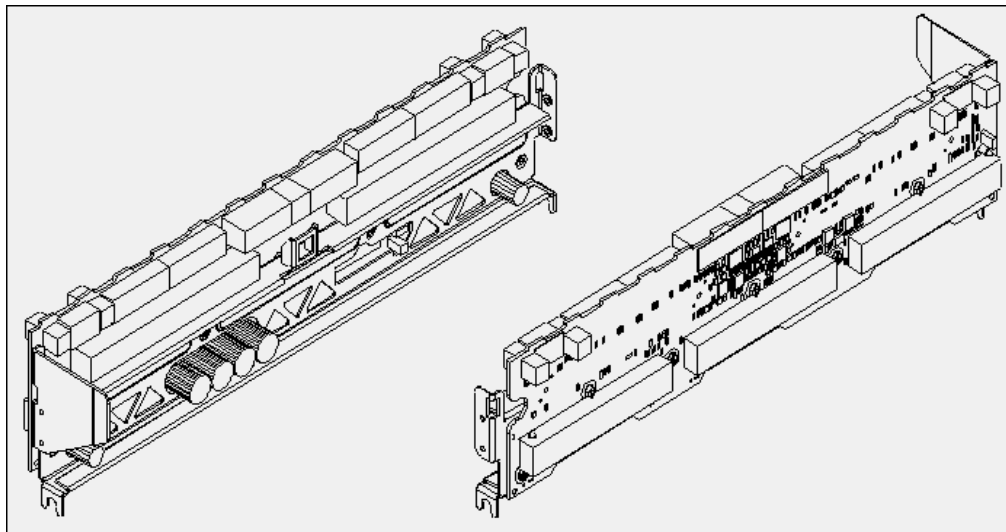
Figure 2-10: Midplane Assembly

The midplane assembly is installed into the OCPRF100 MP server system chassis by rotating the assembly about two alignment structures. The assembly is secured by a total of four screws, two screws are located on each side of the system. All four screws must be removed to extract the midplane assembly. The tab on the midplane assembly is used to manage the cables between the I/O baseboard and the peripheral blind-mate board.

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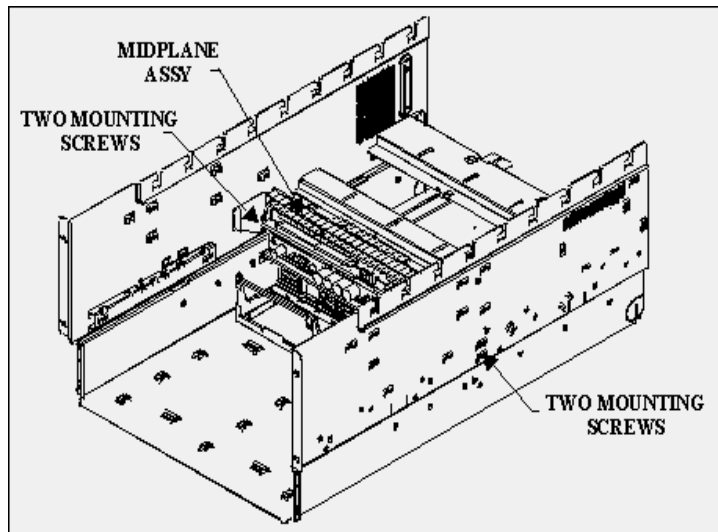
Figure 2-11: Midplane Assembly Installed in System

2.10 I/O Carrier

The I/O carrier is the interface that connects the I/O port of the Profusion chip set to the following:

- Ten hot-swappable PCI slots (four of which support 66-MHz transactions).
- Legacy connector (video, keyboard, serial, parallel, USB, and Intelligent Chassis Management Bus (ICMB) ports).
- Dual LVDS.
- Internal IDE buses, floppy disk, disk drives, and SCSI connectors for peripheral support.

The PCI hot-plug (PHP) I/O carrier, legacy connector, LVDS connectors, ICMB board, and enhanced PCI hot-plug board are assembled onto the I/O carrier tray. The PCI hot-plug base shield is assembled and mounted over the PHP I/O board, and secured by six screws. The PHP slot dividers snap onto the PHP base shield.

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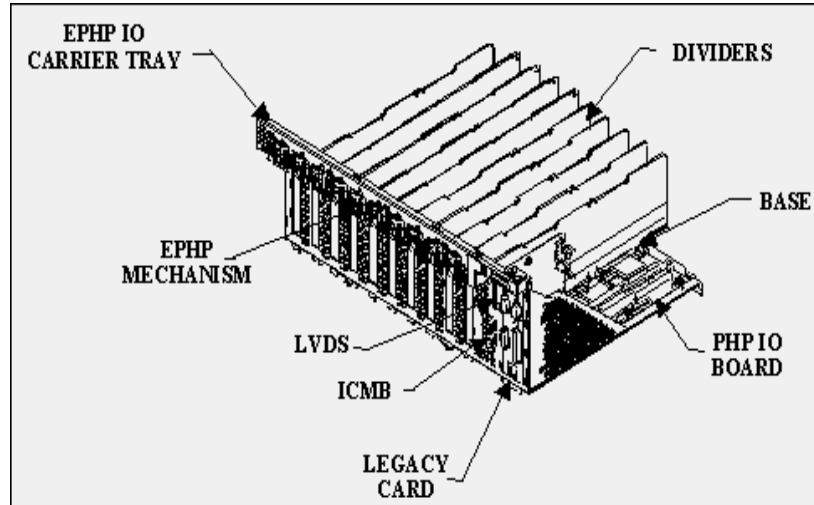
Figure 2-12: I/O Carrier Tray

The I/O carrier tray features tabs on the base of the tray that engage into slots on the horizontal members in the chassis. Lower the tray from the top of the system and slide the tray toward the center of the chassis using the two insert/extract handles located on the back of the tray. Secure the I/O carrier tray to the chassis with the four screws located on the sides and back of the chassis.
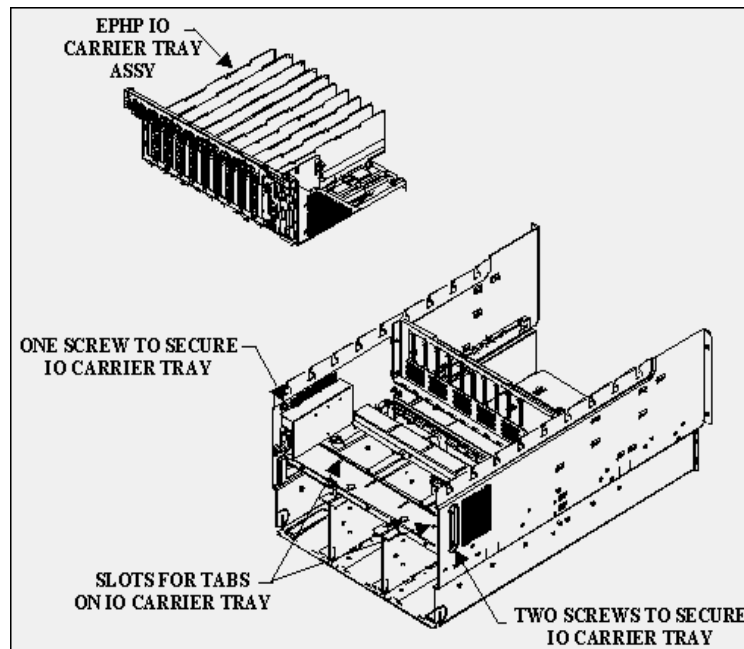
Figure 2-13: Installing the I/O Carrier Tray

The PHP mechanism is a rotating part that actuates a switch located on the PHP board. There are four light emitting diodes (LEDs) per slot--two can be viewed from the rear of the system and two from inside the system. Once the LED shows which slot is powered down, the PHP mechanism can be depressed on the PHP actuator and the mechanism can be rotated out of place to remove the PCI card. Once the new PCI card is installed, rotate the PHP mechanism back into place to activate the switch and secure the PCI card.
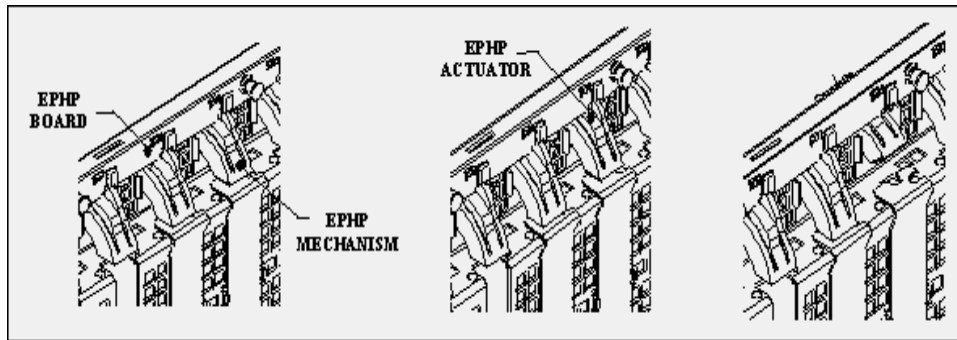
Figure 2-14: PHP Mechanism

2.11 Power Supply

The OCPRF100 MP server system power supply operates at 208 - 220 Vac, or 100 - 115 Vac is rated at 750 watts, and is designed to be hot-swappable, with a 2+1 redundancy factor. Each power supply has indicators showing correct operation, failure, and predictive failure. A power supply displaying the predictive failure LED still will operate corectly, but needs to be sent out for repair as quickly as possible. The predictive failure feature is designed to warn the operator of an impending power supply failure.

2.12 OCPRF100 MP Server System Chassis

The system chassis is the rack-mount chassis used in the system. The system chassis is designed to house all of the components listed above within a 7Ux 32" (+/-) deep space, and mount in a 19-inch rack. The chassis itself is 28" deep with the extra 4" to account for cable management. The chassis was engineered to provide easy access to perform maintenance, upgrades, add memory, and add or remove PCI cards.

The functional server weighs between 120 and 140 pounds, depending on internal configurations. The chassis is designed to provide adequate thermal cooling of all devices within an ambient temperature of 10° to 40°C, while maintaining noise levels below 57 dB. If the ambient temperature exceeds 30°C, the fans in the fan bay will switch to high speed, cooling the system to operational values. Server management will log that a thermal excursion has occurred. Several internal heat sensors will monitor the temperature at key points inside the server. Should any of these sensors indicate that the temperature has exceeded a critical thermal set-point, server management will log the event, and the server will be shut down gracefully, according to user setup.

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3. System Overview

This chapter describes the features of the OCPRF100 MP server system chassis.

System Features

Table 3-1 provides a list and brief description of the features of the OCPRF100 MP server system, which utilizes the OPRF100 board set.

Table 3-1: OCPRF100 MP Server System Feature List

Feature	Description
Upgradeability	The system can be upgraded to future processors within the Pentium® III Xeon™ processor family.
PCI hot plug	The chassis with the OPRF100 board set supports 10 64-bit PCI hot-plug slots (four at 66 MHz, six at 33 MHz).
Compact, high-density system	The system size is a 7U (12.25-inch) rack-mount server.
Redundant power	The system supports three 750-W power supplies in a redundant (2 + 1) configuration.
Redundant cooling	Six system fans in a redundant (5+1) configuration cool the upper system (CPU and I/O). Three internal power supply fans cool the lower system (memory, peripheral bay, and power supplies) in a redundant configuration when the power supply configuration is redundant (2+1).
Modular peripheral bay	The peripheral bay supports one floppy disk drive, one 5.25-inch half-height device, and two 3.5-inch by 1.0- or 1.6-inch hot-swappable LVDS SCSI hard drives.
Front panel liquid crystal display (LCD)	A two line LCD provides the system status.
Intelligent Management Platform Initiative (IPMI) compliant	Intelligent Platform Management Bus (IPMB) for intrachassis communication is provided. Emergency management port (EMP) is used for remote management.

3.1 Introduction

The scalable architecture of the OCPRF100 MP server system supports symmetrical multiprocessing (SMP) and a variety of operating systems (OS). The server provides 10 PCI card slots.

The Profusion carrier contains connectors for installing up to eight Pentium III Xeon processors packaged in single-edge contact cartridges (SECC). Each of the two memory carriers supports

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up to 16 GB of error correction code (ECC) PC-100 compatible registered DIMMs. The I/O carrier contains four 66-MHz and six 33-MHz 64-bit hot-swap PCI slots, I/O ports, and various controllers.

Figure 3-1: OCPRF100 MP Server System Chassis with Peripheral Bay shows an isometric view of the chassis with the peripheral bay installed.
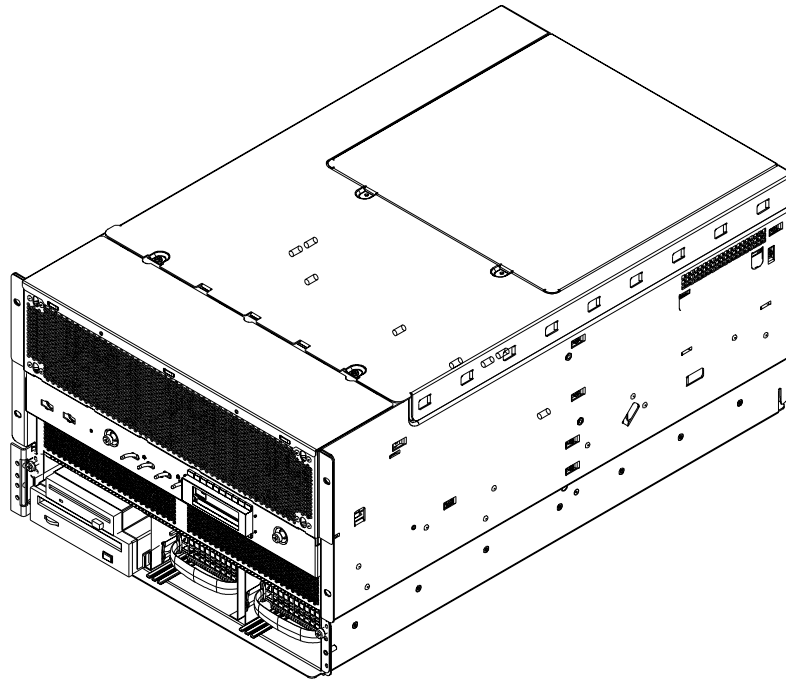
Figure 3-1: OCPRF100 MP Server System Chassis with Peripheral Bay

Figure 3-2: OPRF100 Board Set/System Board Locations within Server Chassis displays the layout of the OPRF100 board set with respect to location within the chassis. The Profusion carrier and I/O carrier are mounted horizontally, with the Profusion carrier toward the front of the chassis and the I/O carrier immediately behind at the rear of the chassis. The midplane distributes power and signal connections to all boards. The midplane resides between the Profusion carrier and the I/O carrier, and interconnects these carriers with the memory carriers and system power supplies. The front panel resides in front of the Profusion carrier in the same plane and provides the user interface, system management, and cooling system power and control.
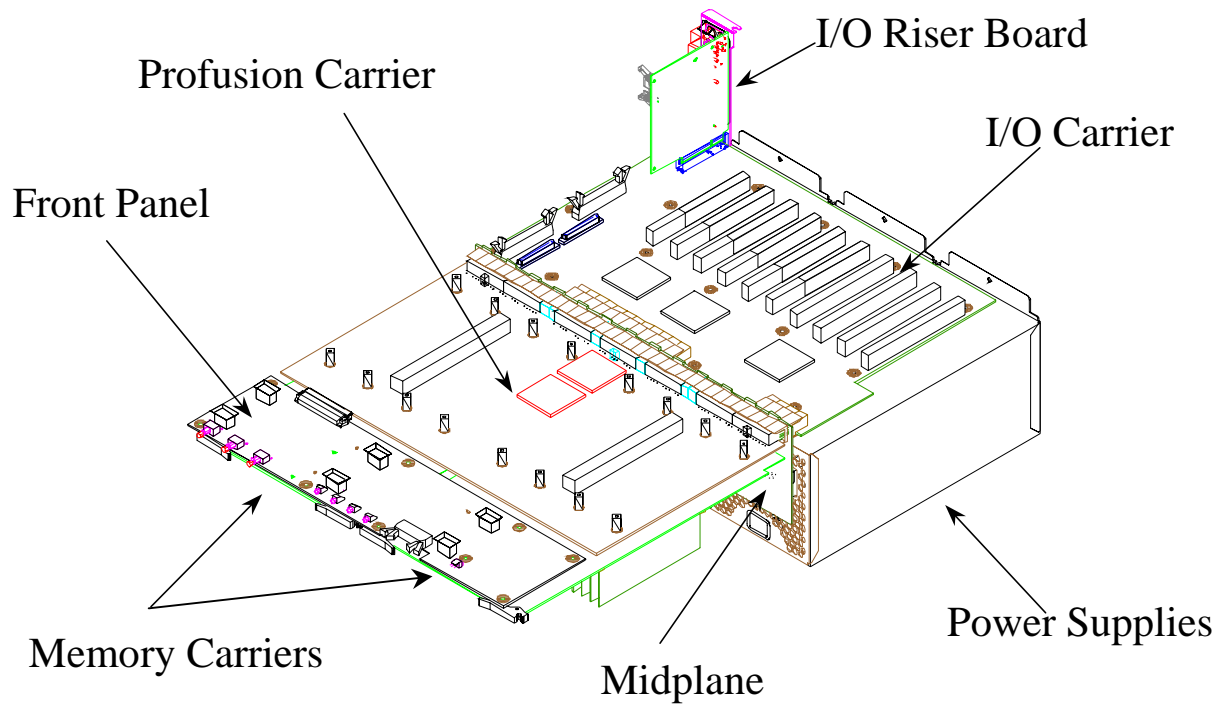
Figure 3-2: OPRF100 Board Set/System Board Locations within Server Chassis

The peripheral bay mounted at the lower front of the chassis supports a 3.5-inch floppy drive, a half-height 5.25-inch device (e.g., CD-ROM) and two 3.5-inch by 1.0- or 1.6-inch hot-swap hard drives. SCSI drives in the hot-swap hard drive bays can be hot-swapped without shutting down the server.

The chassis supports up to three hot-swap, redundant power supplies in a 2+1 configuration. These supplies provide redundant and hot-swappable cooling to the memory carriers and peripherals when the power supplies are in a redundant configuration. A cover plate for the unoccupied power supply location is supplied for systems without redundancy, and should be used to provide adequate cooling and EMI shielding.

The system design provides a hot-swap, redundant (5+1) cooling system for the Profusion and I/O carriers. Basic controls and indicators are located on the front panel.

The front bezel can be customized for integrators to meet their industrial design requirements. The front bezel contains openings to provide adequate cooling for the chassis components and access to the peripherals.

Figure 3-3: OCPRF100 MP Server System Chassis Block Diagram shows a block diagram of the server system.
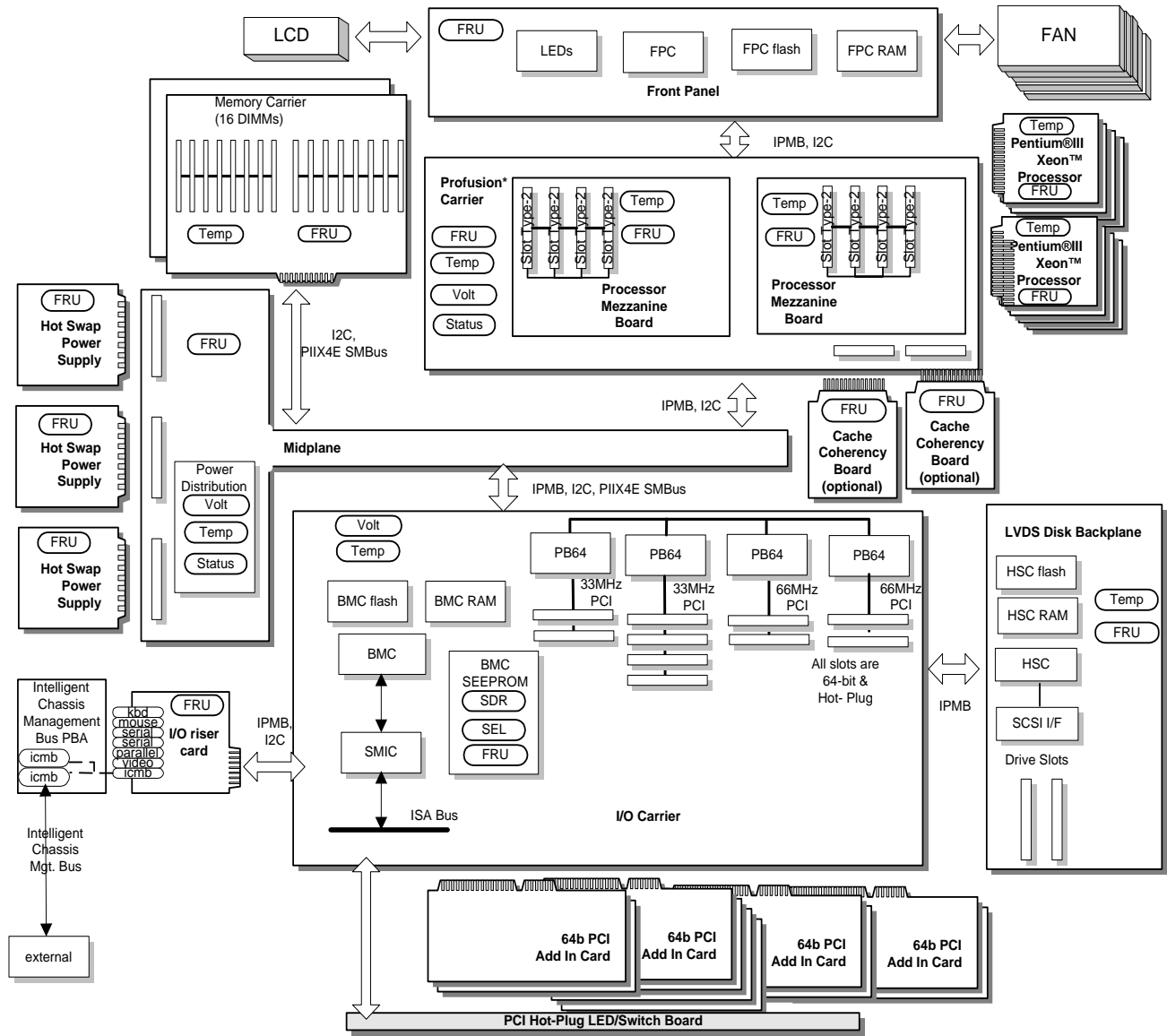
Figure 3-3: OCPRF100 MP Server System Chassis Block Diagram

3.2   External Chassis Features

3.2.1   Front View of Chassis

The front bezel of the server has two main user-accessible areas:

Front panel liquid crystal display (LCD), switches and indicators.

Replaceable media bays—floppy drive and 5.25-inch half-height bay.

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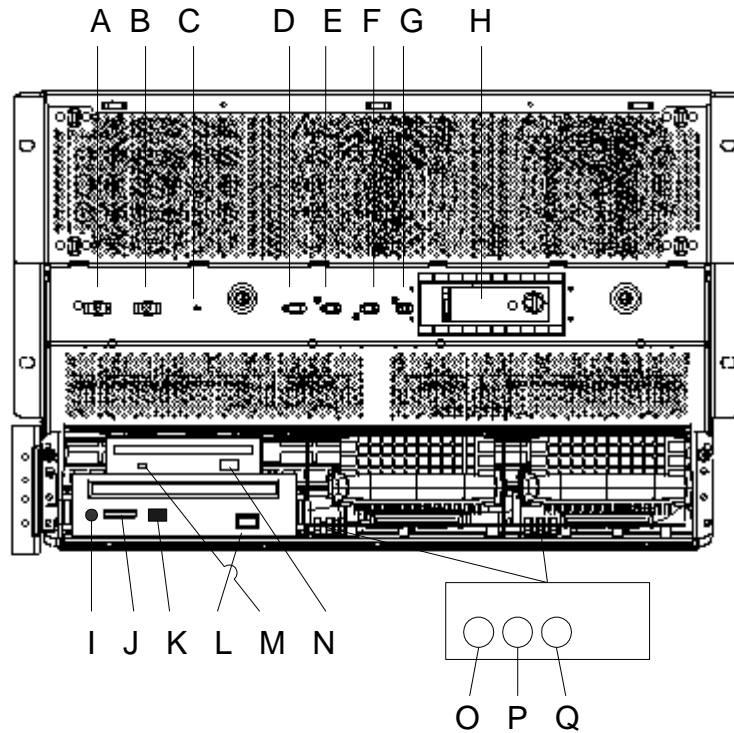
Figure 3-4: Front View of Chassis with No Bezel

Table 3-2: System Features – Front

Item	Feature	Description
Front Panel Controls and Indicators		
A	Power switch	When pressed, turns the DC power inside the server on or off.
B	Reset switch	When pressed, resets the server and causes the power-on self-test (POST) to run.
C	NMI switch	When pressed, causes a nonmaskable interrupt (NMI). This switch is recessed behind the front panel to prevent inadvertent activation. (The switch must be pressed with a narrow tool.)
D	Power (LED) (green)	When continuously lit, indicates the presence of DC power in the server. The light emitting diode (LED) goes out when the power is turned off or when the power source is disrupted. When flashing, indicates the system is in advanced configuration and power interface (ACPI) sleep mode.
E	Power fault LED (yellow)	When continuously lit, indicates a power supply failure. When flashing, indicates a 240 VA overload shutdown and power control failure.

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Table 3-2: System Features – Front

F	Fan fault LED (yellow)	When lit, indicates either a fan failure, or that a predictive fan failure has been detected in the server.
G	Drive fault LED (yellow)	When continuously lit, indicates an asserted fault status on one or more hard disk drives in the hot-swap bay. When flashing, indicates drive rebuild in progress.
H	Front panel LCD	Displays information about processor type and failure codes.
(Items I through L on are control buttons for the CD-ROM, and the location may vary from manufacturer to manu-facturer.)		
3.5-inch Floppy Diskette Drive Descriptions		
M	Activity LED	When lit, indicates the drive is in use.
N	Ejector button	When pressed, ejects the diskette.
Status LEDs for SCSI Drives in Hot-swap Bays		
O	Drive power LED (green)	When continuously lit, indicates the presence of the drive and that drive is powered on.
P	Drive activity LED (green)	When flashing, indicates drive activity.
Q	Drive fault LED (yellow)	When continuously lit, indicates an asserted fault status on one or more hard disk drives in the hot-swap bay. When flashing, indicates that drive rebuild is in progress.

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3.2.2   Rear View of Chassis
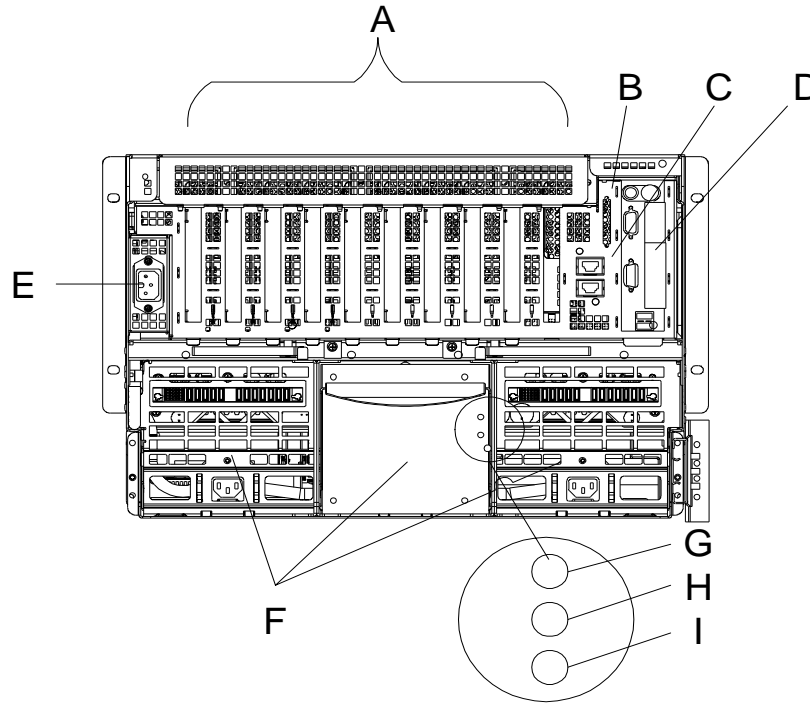
Figure 3-5: Rear View of Chassis

Table 3-3: System Features – Rear

Item	Description
A	PCI add-in board slots.
B	External LVDS connector.
C	ICMB connectors in/out.
D	I/O riser board.
E	AC input power connector.
F	Three power supplies.

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Table 3-3: System Features – Rear

G	PWR LED (green) – power condition – refer to Chapter Power Supply for details.
H	FAIL LED (yellow) – failure condition – refer to Chapter Power Supply for details.
I	PR_FL LED (yellow) – power supply fan predictive failure – refer to Chapter Power Supply for details.

3.2.3   Riser Board External I/O Connectors
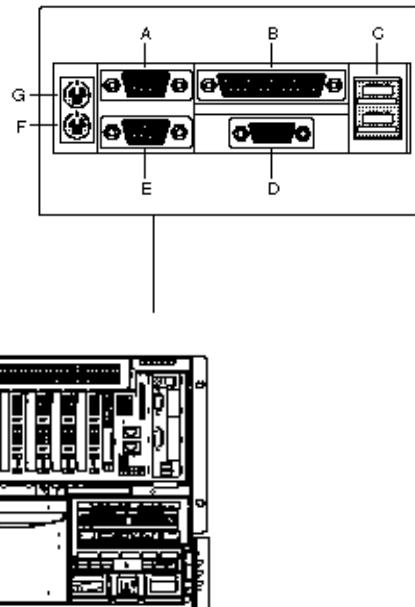
Figure 3-6: Riser Board External I/O Connectors

Table 3-4: Riser Board External I/O Connectors

Item	Description
A.	Serial port 1 (COM1), 9-pin RS-232 connector.
B.	Parallel port, 25-pin bidirectional connector.

Table 3-4: Riser Board External I/O Connectors

C.	USB ports 0 (upper) and 1 (lower).
D.	Super VGA compatible, 15-pin video connector.
E.	Serial port 2 (COM2), 9-pin RS-232 connector.
F.	PS/2-compatible keyboard port.
G.	PS/2-compatible mouse port.
H.	ICMB port, SEMCONN* 6-pin connector.
I.	ICMB port, SEMCONN 6-pin connector.

3.2.4   Peripheral Bay

An optional peripheral bay provides the following:

- One 3.5-inch floppy drive bay
- One 5.25-inch user-accessible drive bay for removable media
- Two 3.5-inch by 1.0- or 1.6-inch hot-swap bays for SCSI SCA hard disk drives
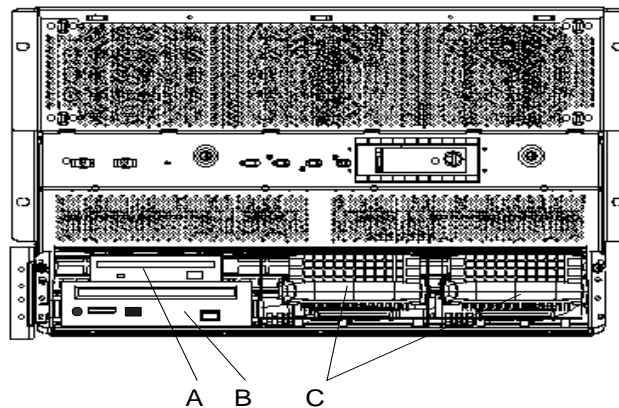
Figure 3-7: Chassis Drive Bays

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Table 3-5: I/O External Connectors

Item	Bay	Description
A	3.5-inch bay	3.5-inch floppy drive.
B	5.25-inch half-height bay	5.25-inch half-height peripheral drive.
C	3.5-inch by 1.0- or 1.6-inch bays	Two hot-swap capable hard drives.

3.2.5   3.5-inch User-accessible Drive Bay

The system ships from the factory without the peripheral bay installed.

3.2.6   5.25-inch User-accessible Drive Bay

The system ships from the factory without the peripheral bay installed.

Note: Installation of hard disk drives in the 5.25-inch user-accessible bay is not recommended due to cooling and EMI constraints.

3.2.7   3.5-inch SCSI Hot-swap Drive Bays

Two 3.5-inch hot-swap capable bays support either 1.0- or 1.6-inch high SCA SCSI hard disk drives. These bays are accessible following removal of the lower bezel section. The wide LVDS SCSI hot-swap backplane provides industry standard 80-pin SCA-2 connectors for two drives. Two wide/fast-20 SCSI III SCA type hard disk drives can be installed in these bays. The wide LVDS SCSI hot-swap backplane is designed to accept drives that consume up to 28 watts of power and run at a maximum ambient temperature of 50°C (112°F).

Extruded aluminum drive carriers with integral heat sinks that accommodate 3.5-inch wide by either 1.0- or 1.6-inch high drives are required as part of the hot-swap implementation. The carrier is attached to the drive with four fasteners, and is retained in the chassis by a locking handle.

The LEDs below each drive display individual drive status. There are three LEDs for each drive: a power on (green) LED; an activity (green) LED; and a fault (yellow) LED. A fault LED on the front panel board also indicates a fault on these drives.

Note: Because all hard drives have different cooling, power and vibration characteristics, Intel will not validate hard drive types in the system chassis. Refer to the *OCPRF100 MP Server System Validation Summary* document for a list of these drives.

3.3 Internal Chassis Features

3.3.1 Power System

Three 750-W supplies in a standard configuration provide the modular power system for the system. The power system may be configured with three power supplies (2+1) for power redundancy, or with two supplies in a nonredundant configuration. The power supplies are mounted in a row at the rear bottom of the chassis. A single AC power cord provides power to the daisy-chained supplies.

When the server is configured with three power supplies, the user can hot swap a failed supply without affecting system functionality.

The midplane provides power distribution of the internal power system with minimal active circuitry. The power distribution circuitry reports quantity and location of the installed power supplies through I^2C^* server management.

Two 750-W, 208-Vac supplies are capable of handling power requirements for the OPRF100 board set and peripherals. For the OPRF100 board set, this includes eight Pentium III Xeon processors, 32 GB of memory and two 1.6-inch hard drives.

The Profusion carrier provides headers for two processor mezzanine boards, each providing four slots for Pentium III Xeon processors. Each mezzanine board has six integrated VRM 8.3 compatible voltage converters. The converter input is +12 Vdc from the power supply. Each Pentium III Xeon processor core has its own converter. One converter provides power for a pair of Pentium III Xeon processor L2 caches.

The total power requirement for the OPRF100 board set exceeds the 240 VA energy hazard limit that defines an operator accessible area. As a result, only qualified technical individuals should access the processor, memory, and non-hot-plug I/O carrier areas while the system is energized.

Refer to Chapter Power Supply Power Supply of this document for detailed power specifications.

Table 3-6: System Power Budget – Current (A) and Power (W)

OCPRF100 MP Server System Power Budget	Units	+3.3 V	+5 V	+12 V	-12 V	+5 VSB	Power

Board	Spec	Units	+3.3 V	+5 V	+12 V	-12 V	+5 VSB	Power
I/O Carrier	Min. Load	Adc	0.20	0.70	0.00	0.20	0.65	**9.81**
	Max. Load	Adc	7.99	45.20	5.00	1.20	0.75	**330.52**
	Max. Step Load	Adc	2.00	12.17	4.50	0.25	0.10	

Table 3-6: System Power Budget – Current (A) and Power (W)

Profusion®	Min. Load	Adc	4.60	0.75	0.25	0.000	0.00	**21.93**
Carrier w/	Max. Load	Adc	12.00	1.50	46.00	0.000	0.00	**599.10**
Mezzanines	Max. Step Load	Adc	2.00	0.75	18.00			
Front Panel	Min. Load	Adc	0.00	0.05	2.00	0.001	0.10	**24.76**
	Max. Load	Adc	0.00	0.23	5.40	0.010	0.25	67.32
Plugs into	Max. Step Load	Adc		0.18	0.10	0.001	0.15	
Profusion Carrier								
Memory Carrier 1	Min. Load	Adc	1.20	0.00	0.00	0.000	0.00	**3.96**
	Max. Load	Adc	23.00	0.00	0.00	0.000	0.00	75.90
	Max. Step Load	Adc	8.00					
Memory Carrier 2	Min. Load	Adc	0.00	0.00	0.00	0.000	0.00	**0.00**
(Note: 2)	Max. Load	Adc	23.00	0.00	0.00	0.000	0.00	**75.90**
	Max. Step Load	Adc	8.00					
Peripherals	Min. Load	Adc	0.00	0.70	0.25	0.000	0.00	**6.50**
(SCSI Backplane)	Max. Load	Adc	0.00	4.50	5.99	0.000	0.00	94.38
	Max. Step Load	Adc		0.90	5.40			
Midplane	Min. Load	Adc						
	Max. Load	Adc	0.01	0.01	0.01			**0.20**
Total min. load		Adc	**6.00**	**2.20**	**2.50**	**0.20**	**0.75**	66.96
	Total max. step load	Adc	**20.00**	**14.00**	**28.00**	**0.25**	**0.25**	
Max. step di/dt		A/uS	**0.50**	**1.00**	**0.60**	**0.10**	**0.10**	
Total max. load		Adc	**66.00**	**51.44**	**62.40**	**1.21**	**1.00**	
Total load power:	1243.32	W	217.8	257.2	748.80	14.52	5	1243.32

Table 3-6: System Power Budget – Current (A) and Power (W)

		Total power (includes 2% distribution loss)		1268.19

Notes:
1. There is no 240 VA protection circuit in the OCPRF100 MP server system.
2. Minimum load for second memory carrier is zero; assumes no carrier is installed.

3.3.2   Cooling System

3.3.2.1   Description

There are two independent cooling subsystems:

The upper system, encompassing the front panel, Profusion carrier, and I/O carrier.

The lower systems, encompassing the memory carriers, peripheral bay, and power supplies.

Air flows in through the bezel and exhausts out the rear of the chassis.

Cooling system redundancy to the upper system is provided by the 5+1 redundant fans at the front top of the system. All systems come with redundant cooling for the upper area in standard factory configuration with six upper system fans. Each fan provides tachometer signal output to the front panel to indicate a fan failure. There may be time limit restrictions on the service time for fan and PCI hot-plug card replacement.

Cooling system redundancy of the lower system is provided by the 2+1 system power supplies. Each power supply fan provides tachometer signal output. A power supply fan failure is indicated at the front panel as a predictive power supply failure. There may be time restrictions on the service time for power supply hot swap replacement.

3.3.2.2   Redundancy and Ambient Temperature Control

3.3.2.2.1   System Fans

The front panel provides either of two fan input voltages to the system fans. Under normal ambient room conditions (less than 30°C), the front panel supplies 8.4 Vdc to the system fans. When a system fan fails or when the room ambient temperature exceeds 30°C, the fan input voltage is increased to 12 Vdc. Following a room temperature excursion above 30°C, the fan voltage does not change back to 8.4 Vdc until the room temperature drops below 28°C and all system fans are operational.

3.3.2.2.2   Power Supply Fans

The power supply fans are controlled independently by each supply. The ambient temperature sensed at the inlet to each supply is used as the input to a control circuit, which continuously var-

ies the fan input voltage. At 28°C ambient temperature, the fan input voltage is 8.0 ± 0.5 Vdc, and at 35°C, the fan input voltage is 13.5 Vdc.

3.3.2.3   Cooling Summary

The system fans are sized to provide cooling for up to eight Pentium III Xeon processors. The power supply fans are sized to cool both fully populated SDRAM board sets, two hot-swap hard drives, and for maintaining power supply function under a full load condition. The cooling system is designed using a worst case analysis with no margin under a single fan failure (system or power supply fan) condition. The environmental conditions are summarized in Section Specifications. Figure 3-8: OCPRF100 MP Server System Cooling summarizes the cooling provided to the system components when system and power supply fans are operating with 12 Vdc input. The lower fan speed settings were chosen to meet acoustic and thermal requirements.
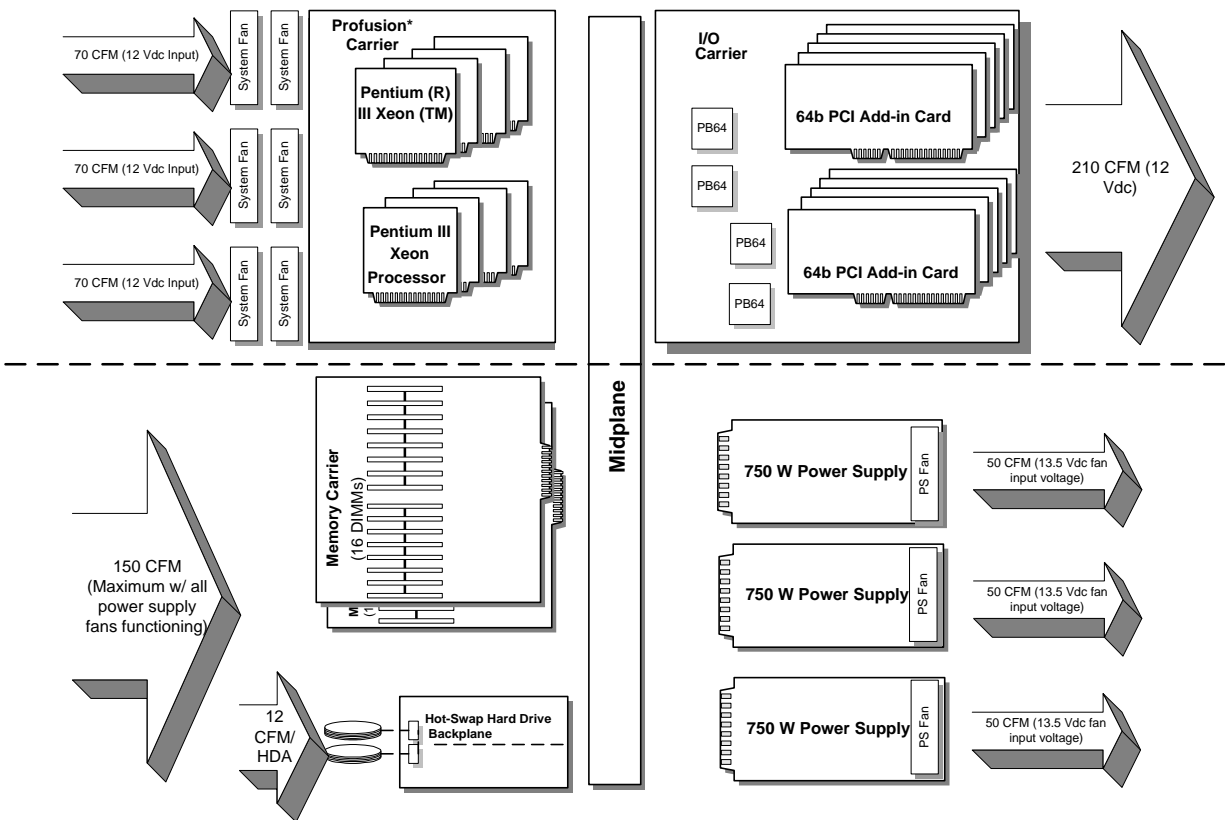
Figure 3-8: OCPRF100 MP Server System Cooling

3.3.3 PCI Hot-plug

3.3.3.1 Description

PCI hot plug (PHP) is the concept of removing or inserting a standard PCI adapter card from a system without stopping the software or powering down the system as a whole.

"Hot Replace" means the user can replace a PCI card with an identical card. The replacement card will use the same PCI resources assigned to the previous card. OS support is required for this function.

"Hot Add" means the user can add a PCI card to a previously unoccupied slot. The system BIOS needs to reserve PCI resource space for the added adapter card upon boot.

"Hot Upgrade" means to replace an existing adapter card with a new version of the card and/or driver. A hot upgrade is not actually a unique operation. It is implemented as a hot removal followed by a hot addition.

3.3.3.2 Hardware Components

Intel has licensed the hardware technology and methods for the implementation of PHP, which conform to the *PCI Hot-plug Specification*. The basic components are:

- Power cycling and reset generation hardware that complies with the *PCI Local Bus Specification*, Rev. 2.1.
- Bus isolation switches to physically disconnect the PHP capable card from the PCI bus (these switches are located on the I/O carrier between each PHP PCI card).
- Indicators (LEDs), located on the PHP LED/switch board, provide service personnel with positive slot identification (these LEDs are visible when viewed from above the I/O carrier, and can be seen from the rear of the system through holes in the chassis).
- Electromechanical hardware to prevent accidental insertion/removal from a live slot (a PHP switch is provided for each slot; when disengaged this switch immediately removes power from that slot. Normal slot power down should be through the control utility
- Protection hardware to isolate the live components of the system from the card being inserted/removed (a mechanical barrier prevents access to the I/O carrier and Profusion carrier components, and is present between PCI cards; each PHP PCI connector is limited to 240 VA).
- A controller element which controls the above hardware and provides an interface for system software.

3.3.3.3 Software Components

The main software components for a PHP system are:

Hot-plug User Interface

- Provides user with access to the hot-plug control panel

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- Receives user input and sends requests to the service layer

- Displays the status of the PCI slot

- Provides user with access to PHP functions that may be available through multiple interfaces

Hot-plug Service

- Provides communication between the user interface and the hot-plug controller driver and is responsible for configuring, loading, and unloading the adapter driver component

- Puts the system into a quiescent state through the hot-plug adapter card by making standard system calls

- Provides communication to the hot-plug controller

- Reports status to the hot-plug user interface

Hot-plug Driver

- Communicates a hot-plug request from the system's service layer

- Provides a software bridge to the PCI hot-plug hardware

- Drives the hot-plug controller

BIOS

- Supplies initialization of the hot-plug hardware components

- Provides DIMM ID monitoring and presence detection

- Provides Advanced Configuration and Power Interface (ACPI) table generation

Adapter Drivers

- For Windows NT* 4.0, changes need to be made to standard miniport drivers.

- For SCO* UnixWare* Version 7.01, the driver must be DDI-8 compliant.

- For Novell* NetWare* Version 5.0, the driver must comply with the NWPA 2.32 or ODI 3.31 specifications.

3.3.3.4   PCI Hot Plug Mechanical Implementation

. The mechanical retention solution includes the following items:

- LED PC board

- Cable between LED board and the I/O carrier baseboard

- Rocker mechanism

- Plastic card guide/retention mechanism to secure the rear of each installed PCI card

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- A 240 VA protective shield on the I/O baseboard and the plastic dividers between PCI slots

The LED PC board contains both the green and amber LEDs, as well as the switch that controls the PCI slot power. These items will no longer reside on the I/O carrier baseboard. This LED board is mounted in the I/O tray directly above where the PCI cards were previously screwed into the tray ledge. The LEDs can be seen from both inside and outside of the chassis. Each switch hangs down off of the LED board so that it can be activated by the rocker mechanism as it is folded into the chassis. See Figure 3-9: Rocker Mechanism.
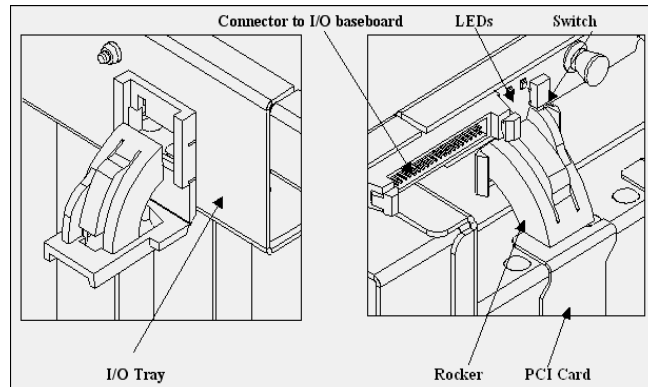
Figure 3-9: Rocker Mechanism

The rocker mechanism activates the slot power switch as it enters the I/O tray. The rocker can be released only from within the chassis. This is to prevent unintentional power down of PCI slots when the system is powered up and the chassis has not yet been pulled out of the rack. The rocker also acts as a retention mechanism for the PCI card. An additional retention mechanism at the back edge of the PCI card is currently being developed.

The opposite end of the PCI card is held in place by a plastic, snap-in, locking card guide. The guide, installed on the center support bracket, has a built in retention mechanism that secures the top-rear edge of the PCI card. (See Figure 3-10.)

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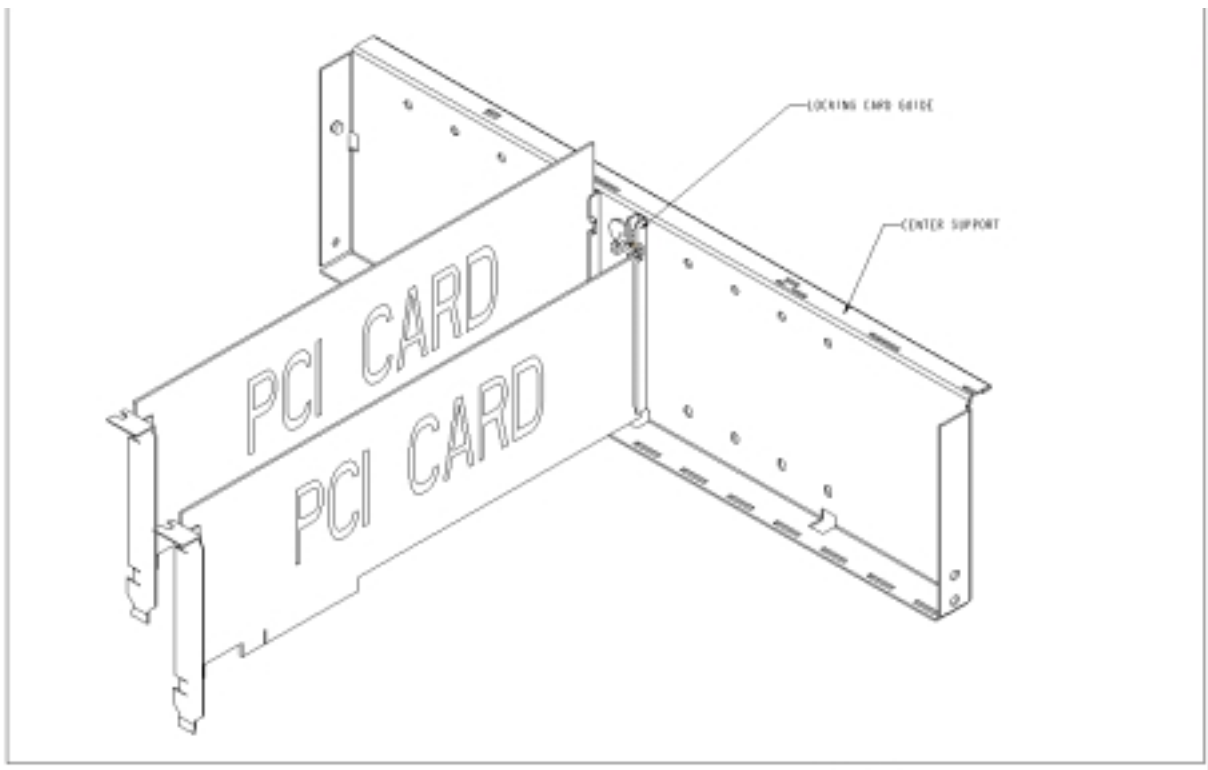
Figure 3-10: PCI Card Retention Mechanism

Revised non-hot plug, hot plug, and top covers are required to accommodate the additional hard-ware used in this enhanced solution.

3.4 Server Management

The server system management architecture features several management controllers, which autonomously monitor server status and provide the interface to server management control functions. The controllers communicate via an I^{2}C-based serial bus referred to as the Intelligent Platform Management Bus (IPMB).

The functions of each controller are summarized in the following sections. The firmware of all the controllers is field upgradeable, using the Server Management Firmware Update Utility. Refer to the *OCPRF100 MP Server Management External Architecture Specification* for more details.

3.4.1 Front Panel Controller

The FPC on the OCPRF100 MP server system chassis front panel board manages the front panel operations. Since this controller is responsible for system power control, it is powered from

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the +5 V standby output of the power supply. The FPC takes part in implementing the following system functions:

- Power and reset switch interfaces

- Fan failure detection

- Chassis FRU inventory

- System hard reset generation

- System power fault indication

- ICMB bridge device

- Emergency management port (EMP)

- LCD interface

3.4.2   Baseboard Management Controller

The baseboard management controller (BMC) on the OPRF100 board set I/O carrier provides server management monitoring capabilities. Associated with the BMC is a flash memory that holds the operation code and the BMC configuration defaults. The various server management functions provided by the BMC are listed below.

- Baseboard voltage monitoring

- Processor voltage monitoring

- Processor voltage ID (VID) monitoring

- Processor presence detection

- Processor internal error (IERR) and thermal trip monitoring

- Fault resilient booting (FRB)

- Processor disable control

- Watchdog timer

- Periodic system management interrupt (SMI) timer

- I^2C master controller

- Private management bus interface

- System management software (SMS) and SMM IPMB message receiver

- Event message receiver

- System event log management and access

- Sensor data record (SDR) repository management and access

- Processor NMI monitoring

- Processor SMI monitoring

- Time-stamp clock

- POST code log

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- Secure mode, video blank, and floppy write protect
- Front panel NMI monitoring
- Software front panel NMI generation

3.4.3   Hot-swap Controller

The hot-swap controller (HSC) on the LVDS SCSI hot-swap backplane is connected to other system boards via the IPMB. The HSC provides server management information through both the IPMB and the SCSI Accessed Fault-Tolerant Enclosures (SAF-TE). SAF-TE is an industry standard for communicating drive and slot status.

The HSC:

- implements the SAF-TE command set accessed through SCSI;
- provides an IPMB path for drive presence, drive fault status, backplane temperature, and fan failure;
- controls the fault lights and drive power on the OCPRF100 MP server system chassis hot-swap backplane;
- monitors the power distribution backplane for power supply status; and
- controls drive power on and off, facilitating hot-swapping of drives.

3.5   Expansion Support

Table 3-7: OCPRF100 MP Server System Expansion Support summarizes the expansion support provided by the server system.

Table 3-7: OCPRF100 MP Server System Expansion Support

Quantity	Type
10	64-bit PCI hot-plug expansion bus slots
2	Single connector attachment (SCA-2) SCSI hard disk drive bays
1	5.25-inch half-height drive bays
1	External LVDS connector
32	72-bit SDRAM PC-100 registered DIMM module sockets (16 per memory module)

3.6   Specifications

3.6.1   Environmental Specifications

The system will be tested to the environmental specifications as indicated in Table 3-8.

Table 3-8: Environmental Specifications Summary

Environmental Feature	Specification
Operating temperature	10° to 35°C (50° to 95°F). See Altitude exception.
Nonoperating temperature	-40°C to 70°C (-40°F to 158°F).
Altitude	0 to 3048 m (0 to 10000 ft.). Note: Maximum ambient temperature is linearly derated between 1520 m (5000 ft.) and 3050 m (10000 ft.) by 1°C per 305 m (1000 ft.).
Operating humidity	85%, noncondensing at 40°C (104°F).
	<33°C (91.4°F) wet bulb at 40°C (104°F) without peripherals.
Nonoperating humidity	95%, noncondensing at +55°C (131°F).
Safety	UL 1950, CSA 950, IEC 950, TUV EN60 950, NEMKO.
Emissions	Certified to FCC Class B; tested to CISPR 22B, EN 55022, and registered with VCCI.
Immunity	Verified to comply with EN 50082-2.
Electrostatic discharge (ESD)	Tested to ESD levels up to 20 kilovolts (kV) air discharge without physical damage as per the Intel® environmental test specification.
Acoustic	Sound pressure: < 57 dbA at ambient temperatures. < 28°C measured at bystander positions in operating mode. Sound power: < 6.5 BA at ambient temperatures. < 28°C in operating mode.

3.6.2   Physical Specifications

Table 3-8 describes the physical specifications of the system.

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Table 3-8: Dimensions and Weight

Specification	Value
Height	31.12 cm (12.25 inches, 7u)
Width	44.45 cm (17.5 inches)
Depth	71.12 cm (28.0 inches)
Weight	51.4 kg (113 lbs.) minimum configuration 63 kg (140 lbs.) maximum configuration
Required front clearance	10 inches (inlet airflow <35 °C / 95 °F)
Required rear clearance	8 inches (no airflow restriction)

Notes: 1.   The system weight listed above is only an approximation and can vary depending on number of peripherals and add-in cards in the system.

2.   The system dimensions exclude the power supply handles for depth.

4.   Cables and Connectors

This chapter describes cables and connectors that interconnect various components of the OCPRF100 MP server system.

The block diagram in Figure 4-1: OCPRF100 Server System Interconnect Diagram shows cables that connect the boards used in the OCPRF100 MP server system.
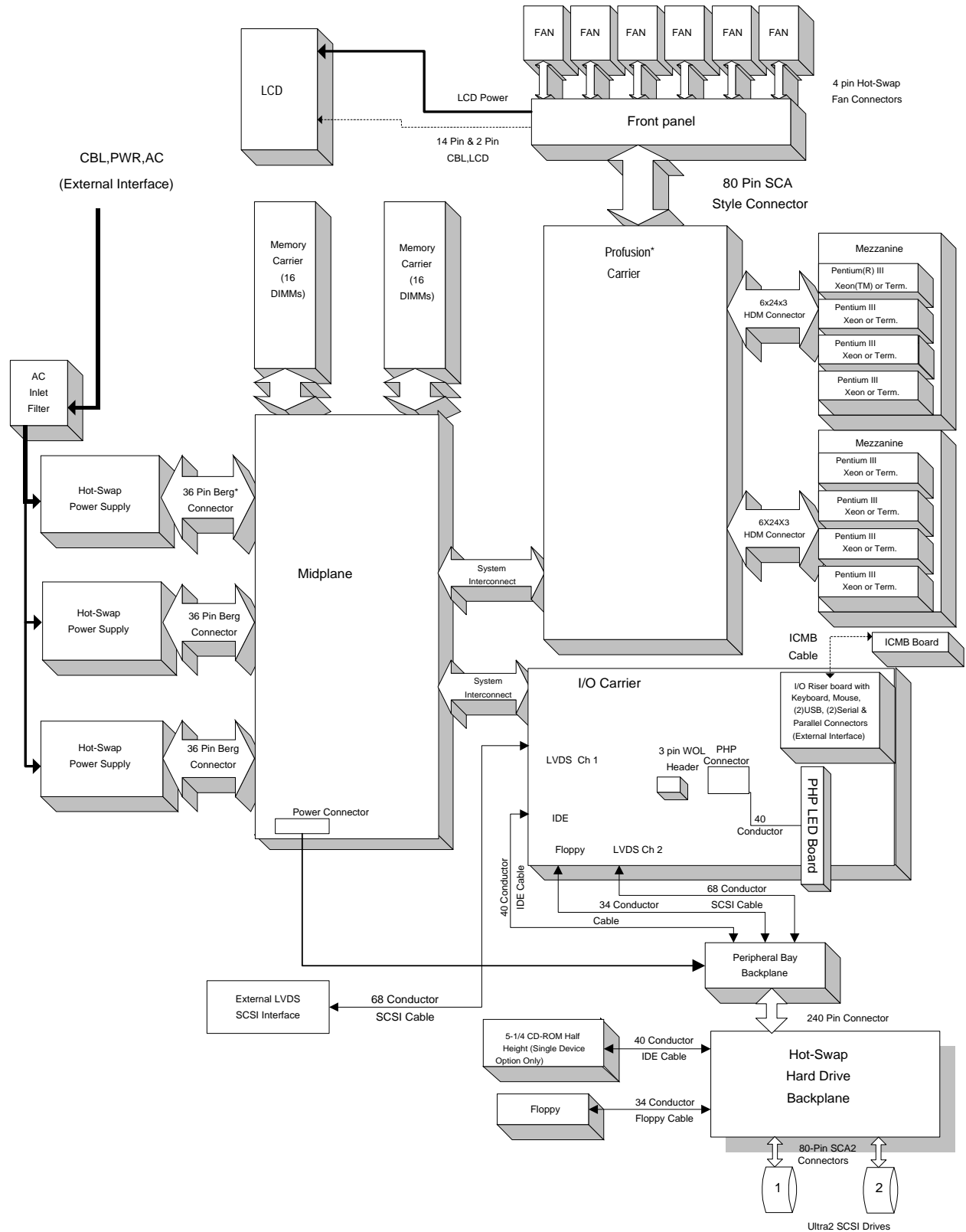
Figure 4-1: OCPRF100 Server System Interconnect Diagram

4.1   Cables

Table 4-1 through Table 4-3 list flat ribbon cables and wire bundles that are used in the assembly of the OCPRF100 MP server system.

Table 4-1: Flat Ribbon Cables

Quantity	Number of Pins	Type	Path
1	68	Wide SCSI cable w/VHDCI interconnect module (solid core)	Routes from the PHP I/O carrier to a panel cut in the back of the system, where a VHDCI interconnect module can link an external VHDCI cable with the internal SCSI devices.
1	68	Wide SCSI cable (solid core)	From the PHP I/O carrier to the peripheral bay backplane.
1	40	IDE cable (long)	From the I/O carrier to the peripheral bay backplane.
1	40	IDE cable (short)	From the LVDS backplane to the IDE CD-ROM.
1	34	Floppy drive cable (long)	From the I/O carrier to the peripheral bay backplane.
1	34	Floppy drive cable (short)	From the LVDS backplane to the floppy drive.
1	40	Flat ribbon cable (LED board)	From the I/O board to the PHP LED board

Table 4-2: Wire Bundles

Quantity	Number of Pins	Type	Path
1	4	Power cable	From the LVDS backplane to the CD ROM and floppy drive.
1	20	Power cable	From the midplane to the peripheral bay backplane.

Table 4-3: Optional Cable

Quantity	Number of Pins	Type	Path
1	50	Narrow SCSI cable	From the LVDS backplane to the 5-1/4" device bay, if an IDE device is not present.

4.2 Connectors

The following section describes the signals and pinouts for various connectors on the OPRF100 board set.

4.2.1 User-accessible I/O Connectors

4.2.1.1 Keyboard and Mouse Ports

These identical PS/2-compatible ports share a common housing. The top port is for the mouse and the bottom port is for the keyboard.

Table 4-4: Keyboard and Mouse Ports

Mouse		Keyboard	
Pin	**Signal**	**Pin**	**Signal**
1	MSEDAT (mouse data)	1	KEYDAT (keyboard data)
2	No connection	2	No connection
3	GND (ground)	3	GND (ground)
4	FUSED_VCC (+5 V)	4	FUSED_VCC (+5 V)
5	MSECLK (mouse clock)	5	KEYCLK (keyboard clock)
6	No connection	6	No connection

Figure 4-2: Keyboard or Mouse Connector

4.2.2 Serial Ports

The I/O carrier provides two stacked RS-232C serial ports (the top one is COM1 and the bottom one is COM2). They are D-subminiature 9-pin connectors. Each serial port can be enabled separately with the configuration control provided on the I/O carrier.

The COM2 serial port can be used either as an emergency management port or as a normal serial port. As an emergency management port, COM2 is used as a communication path by the server management RS-232 connection to the FPC on the front panel board. This provides a level of emergency management through an external modem. The RS-232 connection can be monitored by the FPC when the system is in a powered down (standby) state. For additional information, see the *Emergency Management Port v1.0 Interface External Product Specification*.

Table 4-5: Serial Port Connectors

Pin	Signal
1	DCD
2	RXD
3	TXD
4	DTR
5	GND
6	DSR
7	RTS
8	CTS
9	RIA
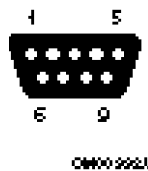
Figure 4-3: Serial Port Connector

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4.2.3   Parallel Port

The IEEE 1284-compatible parallel port—used primarily for a printer—sends data in parallel format. The parallel port is accessed through a D-subminiature 25-pin connector.

Table 4-6: Parallel Port Connector

Pin	Signal	Pin	Signal
1	STROBE_L	14	AUFDXT_L (auto feed)
2	Data bit 0	15	ERROR_L
3	Data bit 1	16	INIT_L (initialize printer)
4	Data bit 2	17	SLCTIN_L (select input)
5	Data bit 3	18	GND (ground)
6	Data bit 4	19	GND
7	Data bit 5	20	GND
8	Data bit 6	21	GND
9	Data bit 7	22	GND
10	ACK_L (acknowledge)	23	GND
11	BUSY	24	GND
12	PE (paper end)	25	GND
13	SLCT (select)		
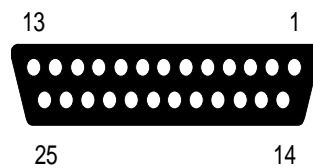
OM00933A

Figure 4-4: Parallel Port Connector

4.2.4   VGA Video Port

The video port interface is a standard VGA compatible 15-pin connector. Onboard video is supplied by a Cirrus Logic* GD5446 PCI video controller with 2 MB of onboard video DRAM.

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Table 4-7: Video Connector

Pin	Signal
1	Red (analog color signal R)
2	Green (analog color signal G)
3	Blue (analog color signal B)
4	No connection
5	GND (video ground, shield)
6–8	GND (video ground, shield)
9	No connection
10	GND (video ground)
11–12	No connection
13	HSYNC (horizontal sync)
14	VSYNC (vertical sync)
15	No connection
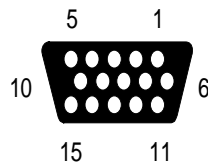
OM00936A

Figure 4-5: Video Connector

4.2.5 Universal Serial Bus Interface

The built-in USB ports permit the direct connection of two USB peripherals without an external hub. If more devices are required, an external hub can be connected to either of the built-in ports.

Table 4-8: Dual USB Connector

Pin	Signal	Description
A1	VCC	Overcurrent monitor line port 0.

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Table 4-8: Dual USB Connector

A2	DATAL0	Differential data line paired with DATAH0.
A3	DATAH0	Differential data line paired with DATAL0.
A4	GND	Ground potential.
B1	VCC	Overcurrent monitor line port 1.
B2	DATAL1	Differential data line paired with DATAH1.
B3	DATAH1	Differential data line paired with DATAL1.
B4	GND	Ground potential.
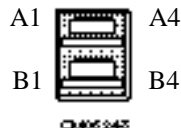
Figure 4-6: Dual USB Connector

4.2.6   ICMB Connectors

The ICMB connector provides external access to the ICMB. This makes it possible to externally access chassis management functions, alert logs, post-mortem data, etc. It also provides a mechanism for chassis power control. The server provides two SEMCONN* 6-pin connectors to allow daisy chained cabling. Additional information about ICMB can be found in the *External Intelligent Management Bus Bridge External Program Specification*.

Table 4-9: ICMB Connector

Pin	Signal
1	No connection
2	No connection
3	B (negative)
4	A (positive)
5	No connection
6	No connection

Figure 4-7: ICMB Connector

4.2.7   Fan Connector

Table 4-10: Fan Connectors (J1A1,J9A1,J10A1)

Pin	Signal
1	Ground
2	VCCFAN
3	Ground
4	FAN_Tach

4.2.8   Peripheral Bay Power Connector

Table 4-11: Peripheral Bay Power Connector

Pin	Signal	Color
1	+12V	Yellow
2	GND	Black
3	+12V	Yellow
4	+5V	Red
5	GND	Black
6	+5V	Red
7	GND	Black
8	SCL	Green
9	GND	Black
10	PWR_Good	White
11	+12V	Yellow

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Table 4-11: Peripheral Bay Power Connector

12	GND	Black
13	+12V	Yellow
14	+5V	Red
15	GND	Black
16	+5V	Red
17	GND	Black
18	SDA	Light Blue
19	GND	Black
20	RST_I2C_L	Violet

4.2.9   Peripheral Bay Backplane Header

Table 4-12: Peripheral Bay Backplane Header (240 position)

Column	A	B	C	D	E
1	RESET(1)	GND	DD8 (4)	GND	GND
2	DD7 (3)	GND	DD9 (6)	GND	FD_DENSEL
3	DD6 (5)	GND	DD10 (8)	GND	GND
4	DD5 (7)	GND	DD11 (10)	GND	N/C
5	DD4 (9)	GND	DD12 (12)	GND	GND
6	DD3 (11)	GND	DD13 (14)	GND	FD_DRATE0
7	DD2 (13)	GND	DD14 (16)	GND	GND
8	DD1 (15)	GND	DD15 (18)	GND	FD_INDEX_L
9	DD0 (17)	GND	GND	DIOW (23)	GND
10	DMARQ (21)	GND	GND	GND	FD_MTR0_L
11	GND	GND	GND	DIOR (25)	GND
12	GND	GND	RESERVED (32)	GND	FD_DR1_L
13	IORDY (27)	GND	PDIAG (34)	GND	GND
14	DMACK (29)	GND	DA2 (36)	GND	FD_DR0_L
15	INTRQ (31)	GND	CS0 (37)	GND	GND

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Table 4-12: Peripheral Bay Backplane Header (240 position)

16	DA1 (33)	GND	DA0 (35)	GND	FD_MTR1_L
17	DASP (39)	GND	CS1 (38)	GND	FD_MSEN1
18	GND	GND	GND	GND	FD_DIR_L
19	GND	GND	FD_STEP_L	GND	GND
20	FD_WDATA_L	GND	GND	GND	FD_WGATE_L
21	GND	GND	FD_TRK0_L	GND	FD_MSEN0
22	FD_WPROT_L	GND	GND	GND	FD_RDATA_L
23	GND	GND	FD_HDSEL_L	GND	GND
24	FD_DSKCHG_L	GND	S35 (-DB 12)	S2 (+DB 13)	S37 (-DB 14)
25	+12V	+12V	S1 (+DB 12)	S36 (-DB 13)	S3 (+DB 14)
26	+12V	+12V	S38 (-DB 15)	S5 (+DB P1)	GND
27	+12V	+12V	S4 (+DB 15)	S39 (-DB P1)	GND
28	+12V	+12V	S41 (-DB 0)	S8 (+DB 1)	S43 (-DB 2)
29	+12V	+12V	S7 (+DB 0)	S42 (-DB 1)	S9 (+DB 2)
30	+12V	+12V	S44 (-DB 3)	S11 (+DB 4)	S46 (-DB 5)
31	+12V	+12V	S10 (+DB 3)	S45 (-DB 4)	S12 (+DB5)
32	+12V	+12V	S47 (-DB 6)	S14 (+DB 7)	S49 (-DB P)
33	+12V	+12V	S13 (+DB 6)	S48 (-DB 7)	S15 (+DB P)
34	+12V	+12V	GND	S17 (TERM-PWR)	S52 (TERMPWR)
35	+12V	+12V	S16 (DIFFSENS)	S51 (TERM-PWR)	S18 (TERMPWR)
36	+12V	+12V	S53 (RESERVED)	S20 (+ATN)	GND
37	+5V	+5V	S19 (RESERVED)	S54 (-ATN)	GND
38	+5V	+5V	S56 (-BSY)	S23 (+ACK)	S58 (-RST)
39	+5V	+5V	S22 (+BSY)	S57 (-ACK)	S24 (+RST)
40	+5V	+5V	S59 (-MSG)	S26 (+SEL)	S61 (-C/D)
41	+5V	+5V	S25 (+MSG)	S60 (-SEL)	S27 (+C/D)
42	+5V	+5V	S62 (-REQ)	S29 (+I/O)	GND
43	+5V	+5V	S28 (+REQ)	S63 (-I/O)	GND
44	+5V	+5V	S65 (-DB8)	S32 (+DB 9)	S67 (-DB 10)
45	+5V	+5V	S31 (+DB 8)	S66 (-DB 9)	S33 (+DB 10)

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Table 4-12: Peripheral Bay Backplane Header (240 position)

46	+5V	+5V	S68 (-DB 11)	GND	GND
47	+5V	+5V	S34 (+DB 11)	SDA	RST_I2C_L
48	+5V	+5V	+5V	PWR_GOOD	SCL

4.2.10   LED Board Connector

Table 4-13: LED Board Connectors

Signal Name	Pin #	Pin #	Signal Name
S1_A_SWITCH	1	2	S2_A_SWITCH
S1_A_GREEN	3	4	S2_A_GREEN
S1_A_AMBER	5	6	S2_A_AMBER
S1_B_SWITCH	7	8	S2_B_SWITCH
S1_B_GREEN	9	10	S2_B_GREEN
S1_B_AMBER	11	12	S2_B_AMBER
S3_B_SWITCH	13	14	S4_B_SWITCH
S3_B_GREEN	15	16	S4_B_GREEN
S3_B_AMBER	17	18	S4_B_AMBER
S1_C_SWITCH	19	20	S2_C_SWITCH
S1_C_GREEN	21	22	S2_C_GREEN
S1_C_AMBER	23	24	S2_C_AMBER
S1_D_SWITCH	25	26	S2_D_SWITCH
S1_D_GREEN	27	28	S2_D_GREEN
S1_D_AMBER	29	30	S2_D_AMBER
+3.3V	31	32	GND
+3.3V	33	34	GND
+3.3V	35	36	GND
+3.3V	37	38	GND
+3.3V	39	40	GND

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4.2.11   SCSI Connector

Table 4-14: SCSI Connector

	WIDE SCSI CONNECTOR		
Pin	Signal	Signal	Pin
1	S1 (+DB 12)	S35 (-DB 12)	35
2	S2 (-DB 13)	S36 (-DB 13)	36
3	S3 (+DB 14)	S37 (-DB 14)	37
4	S4 (+DB 15)	S38 (-DB 15)	38
5	S5 (+DB P1)	S39 (-DB P1)	39
6	S6 (+DB 0)	S40 (-DB 0)	40
7	S7 (+DB 1)	S41 (-DB 1)	41
8	S8 (+DB 2)	S42 (-DB 2)	42
9	S9 (DB 3)	S43 (-DB 3)	43
10	S10 (+DB 4)	S44 (-DB 4)	44
11	S11 (+DB5)	S45 (-DB 5)	45
12	S12 (+DB 6)	S46 (-DB 6)	46
13	S13 (+DB 7)	S47 (-DB 7)	47
14	S14 (+DB P)	S48 (-DB P)	48
15	S15	S49	49
16	S16 (DIFFSENS)	S50	50
17	S17 (TERMPWR)	S51 (TERMPWR)	51
18	S18 (TERMPWR)	S52 (TERMPWR)	52
19	S19 (RESERVED)	S53 (RESERVED)	53
20	S20	S54	54
21	S21 (+ATN)	S55 (-ATN)	55
22	S22	S56	56
23	S23 (+BSY)	S57 (-BSY)	57
24	S24 (+ACK)	S58 (-ACK)	58
25	S25 (+RST)	S59 (-RST)	59
26	S26 (+MSG)	S60 (-MSG)	60
27	S27 (+SEL)	S61 (-SEL)	61

Table 4-14: SCSI Connector

28	S28 (+C/D)	S62 (-C/D)	62
29	S29 (+REQ)	S63 (-REQ)	63
30	S30 (+I/O)	S64 (-I/O)	64
31	S31 (+DB 8)	S65 (-DB8)	65
32	S32 (+DB 9)	S66 (-DB 9)	66
33	S33 (DB 10)	S67 (-DB 10)	67
34	S34 (DB 11)	S68 (-DB 11)	68

4.2.12   IDE Connectors

Table 4-15: IDE Connectors

	IDE 40 PIN Connector		
Pin			**Pin**
1	RESET	GND	2
3	DD7	DD8	4
5	DD6	DD9	6
7	DD5	DD10	8
9	DD4	DD11	10
11	DD3	DD12	12
13	DD2	DD13	14
15	DD1	DD14	16
17	DD0	DD15	18
19	GND	KEYPIN (NC)	20
21	DMARQ	GND	22
23	DIOW	GND	24
25	DIOR	GND	26
27	IORDY	CSEL	28
29	DMACK	GND	30
31	INTRQ	RESERVED	32

Table 4-15: IDE Connectors

33	DA1	PDIAG	34
35	DA0	DA2	36
37	CS0	CS1	38
39	DASP	GND	40

4.2.13   Floppy Connectors

Table 4-16: Floppy Connectors

	FLOPPY CONNECTOR		
Pin			Pin
1	GND	FD_DENSEL	2
3	GND	N/C	4
5	KEY	FD_DRATE0	6
7	GND	FD_INDEX_L	8
9	GND	FD_MTR0_L	10
11	GND	FD_DR1_L	12
13	GND	FD_DR0_L	14
15	GND	FD_MTR1_L	16
17	FD_MSEN1	FD_DIR_L	18
19	GND	FD_STEP_L	20
21	GND	FD_WDATA_L	22
23	GND	FD_WGATE_L	24
25	GND	FD_TRK0_L	26
27	FD_MSEN0	FD_WPROT_L	28
29	GND	FD_RDATA_L	30
31	GND	FD_HDSEL_L	32
33	GND	FD_DSKCHG_L	34

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5. Power Supply

This document defines the requirements for a universal input switching power supply, which provides 750 watts DC with power factor corrected AC input and with current and remote sense regulation. The power supply is used with its DC outputs paralleled with other identical supplies to form a redundant power system with system operating replacement capability (hot-swap). All power supply connectors, including AC and DC connectors, accommodate "blind mating." The supply has four externally enabled outputs, one +5 V standby output at 1.0 A, and one +15 Vdc standby output at 200 mA. Both +5 Vdc and +15 Vdc standby outputs are present whenever AC power is applied. The four externally enabled outputs have the following ratings:

- +3.3 Vdc at 36 A
- +5 Vdc at 36 A
- +12 Vdc at 36 A with 42 A peak
- -12 Vdc at 1 A

5.1 Mechanical Requirements

5.1.1 Mechanical Outline

The mechanical outline and dimensions are shown in Figure 5-1: Outline Drawing of Power Supply Enclosure. The unit of measurement is inches. The following mechanical sketches should be used for preliminary reference only. Refer to the *Power Supply, 750/650W, PFC, 5 Outputs* document for a detailed drawing.

Figure 5-1: Outline Drawing of Power Supply Enclosure

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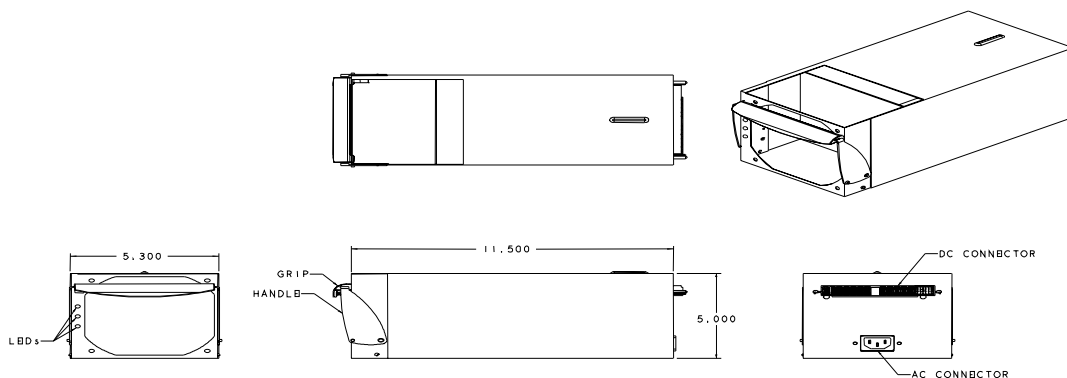
The power supply dimensions are 5.0" H by 5.3" W by 11.5" D.

5.1.2   Fan Requirements

The power supply incorporates a 120 mm fan for self-cooling. The air comes in from the connector side, passes through the power supply, and exhausts on the fan side of the power supply.

5.2   Interface Requirements

5.2.1   AC Inlet Connector

The power supply has a standard IEC inlet connector.

5.2.2   DC Output Connector(s)

DC power and control signals are interfaced to the system distribution and control subsystem via connectors which dock with mating connectors when the power supply is inserted into the system backplane.

The DC connector is equivalent to the Berg* hybrid 36-pin connector with Intel® P/N 703983-001 and Berg P/N 51219-XX002. The pin assignment for the DC connector is shown in Table 5-1: Connector and Pin Assignments.

Table 5-1: Connector and Pin Assignments

Signal Pins						
	1	2	3	4	5	6
D	+ 12 V LS	P_Good	AC_OK	+15 V Standby	Remote SEN RTN	- 12 V
C	A0	SCL	FAULT	PRED FAIL	+12 V SENSE	KEY
B	A1	SDA	+3.3 V SENSE	+5 V SENSE	+5 V Stdby	+5 V Stdby
A	+ 3.3 V LS	Power Present	Spare	+5 V LS	PS_ON	PS_KILL

Power Blades											
P1	P2	P3	P4	P5	P6	P7	P8	P9	P10	P11	P12
+12 V	+12 V	GND	GND	GND	GND	GND	GND	+5 V	+5 V	3.3 V	3.3 V

Note: PS_On and PS_Kill are 1.2 mm shorter in mating length compared to other pins in the connector.

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Notes: 1.   Power blades (P1 – P12) are rated at 25 A each.
2.   Signal pins (A1 – D6) are rated at 1 A each.

Figure 5-2: DC Connector Drawing

5.3   Marking and Identification

The power supply marking must support the following requirements: safety agency requirements, government requirements (if required, e.g., point of manufacturing), power supply vendor requirements, and Intel manufacturing and field support requirements.

5.3.1   LED Labeling

The power LED (green), the power supply failure LED (yellow), and the predictive failure LED (yellow) are marked or labeled as follows.

- The power LED is labeled **PWR**.

- The predictive failure LED is labeled **PRFL**.

- The power supply failure LED is labeled **FAIL**.

The LEDs should be viewable on the outside rear of the chassis when the power supply is installed in the system chassis. LEDs are located to meet all electrostatic discharge (ESD) requirements.

5.4   Internal System Marking

The power supply is marked to support the safety agency requirements, government requirements (if required, e.g., point of manufacturing), power supply vendor requirements, and Intel manufacturing and field support requirements. This marking is applied on an external surface of the power supply and is not be visible from the exterior of the server system.

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```
MANUFACTURER
LOGO                          SAFETY AGENCY
                              MARKINGS

MANUFACTURER  NAME
MANUFACTURER MODEL NO.  AND REVISION

AUTORANGING INPUT: 50/60HZ
INPUT 100-120V ~ 12A, OUTPUT 650W

+3.3V   ===   31.0A MAX    -12V     ===    1.0.A MAX
+5V     ===   31.0A MAX    +5VSB    ===    1.0A  MAX
+12V    ===   31.0A MAX    +15VSB   ===    0.2A MAX

INPUT 200-240V ~ 7A, OUTPUT 750W

+3.3V         33.0A MAX
+5V           33.0A MAX    -12V            1.0.A MAX
+12V          33.0A MAX    +5VSB           1.0A  MAX
                           +15VSB          0.2A MAX

P/N:    ┌──────────────────────────────┐
        │   CODE 3 OF 9 BAR CODE        │
        └──────────────────────────────┘
        HUMAN READABLE PART NUMBER

S/N     ┌──────────────────────────────┐
        │   CODE 3 OF 9 BAR CODE        │
        └──────────────────────────────┘
        HUMAN READABLE SERIAL NUMBER

DATE CODE :XXXX               COUNTRY OFORIGIN
```

Figure 5-3: Internal Label

The power supply is marked with the international label to indicate that no user serviceable parts are contained in the power supply. This label is shown in Figure 5-4: Service Label. This label is printed on bright yellow vinyl label stock with black symbols.

```
      15.0
     (.600)

              30.0
            (1.187)
```
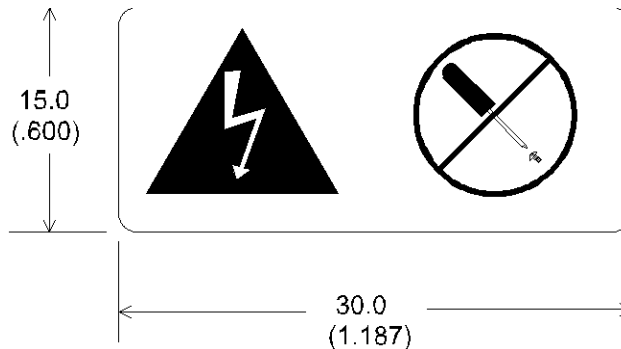
Figure 5-4: Service Label

Note: The temperature of the power supply chassis cannot exceed 70°C under all circumstances; otherwise, a UL international HOT SURFACE label must be added. This HOT SURFACE label, if required, will be placed in such a way that when the power supply is extracted from the system, the label will be visible before the operator has a chance to touch the hot surface of the power supply.

5.5   Electrical Requirements

5.5.1   Efficiency

The power supply has a minimum efficiency of 65% to its DC output pins at maximum load currents and at rated nominal input voltages and frequencies. The power supply has a minimum efficiency of 70% to its DC output pins at maximum load currents when the input voltage is higher than 180 Vac.

5.5.2   AC Input Voltage Specification

5.5.3   AC Input Voltage Ranges

The nominal input voltage ranges specified in AC volts root-mean-square (rms)# are 100-120 and 200-240 Vac. The power supply incorporates a universal power input with active power factor correction, which reduces line harmonics in accordance with EN61000-3-2 and JEIDA MITI standards. The ratings are marked on the supply labels as referenced in Table 5-2: Input Voltage Requirements and Section Internal System Marking.

Table 5-2: Input Voltage Requirements

Parameter	Min	Nom	Max	Units
Vin (115)	90	100-120	132	Vrms
Vin (230)	180	200-240	264	Vrms
Vin Frequency	47	50/60	63	Hz
Input Current 220 Vac range		†		Amps

† Proper values to be determined by the power supply manufacturer. Correct values are to be printed on the internal system label shown in Figure 5-3: Internal Label.

5.5.3.1   AC Line Dropout

AC line dropout condition is a transient condition defined when the line voltage input to the power supply drops to 0 volts. AC line dropout will not damage the power supply under any load conditions. While operating at full load, an AC line dropout condition with a period equivalent to a complete cycle of AC input power frequency (i.e., 20 milliseconds at 50 Hz) or less, will not cause any out-of-regulation conditions, such as overshoot or undershoot, nor will it cause any nuisance trips of any of the power supply protection circuits.

5.5.3.2   AC Line Fuse

Both the LINE and NEUTRAL AC inputs are fused. AC line fusing is compliant with all safety agency requirements. AC inrush current will not cause the AC line fuses to blow under any condi-

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tions. Protection circuits in the power supply will not cause the AC fuse to blow unless a component in the power supply has failed. This includes DC output load short conditions. The DC load short circuit protection circuits will shut down or limit power supply without causing the AC line fuse to blow.

5.5.3.3   Power Factor Correction

The power supply incorporates a power factor correction circuit.

The power supply is tested as described in *EN 61000-3-2: Electromagnetic Compatibility (EMC) Part 3: Limits- Section 2: Limits for Harmonic Current Emissions*, and must meet the harmonic current emissions limits specified for ITE equipment.

The power supply is tested as described in *JEIDA MITI Guideline for Suppression of High Harmonics in Appliances and General-Use Equipment* and must meet the harmonic current emissions limits specified for ITE equipment.

5.5.4   DC Output Specification

The power supply DC output specification is met by a single supply, by two supplies, or by three supplies operating with their outputs directly paralleled. When operated in parallel, the supplies share the total load currents equally within the limits specified, and meet all performance requirements of individual supplies. Failure of a supply in a paralleled group, or removal of an operational or failed supply from a paralleled group will not cause DC output transients in excess of the limits specified. Adding an operational or failed supply to a paralleled group will not cause DC output transients in excess of the limits specified.

Table 5-3: DC Output Voltage Limits

Parameter	Min		Max	Units	Tolerance
+3.3 V	+3.25		+3.35	V	± 50 mV
+5 V	+4.90		+5.10	V	± 2%
+12 V	+11.76		+12.24	V	± 2%
-12 V	-10.80		-13.20	V	± 10%
+5 V Standby	+4.85		+5.20	V	+ 4% & -3%
+ 15 V Standby	+ 13.5		+ 16.5	V	± 10%

5.5.4.1   DC Outputs Rating

The steady state and peak DC output load currents are in the ranges shown in Table 5-4: Load Range.

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Table 5-4: Load Range

Voltage	Single Power Supply Load Condition		
	Minimum Continuous	Maximum Continuous	Peak
+3.3 V	1.1 A	36 A	
+5 V	0.7 A	36 A	
+12 V	0.7 A	36 A	42 A
-12 V	0 A	1.0 A	
+5 V Standby	0.05 A	1.00 A	
+15 V Standby	0 A	200 mA	

5.5.4.2   Remote Sense

The power supply provides remote sense on the +3.3 Vdc, +5 Vdc, and +12 Vdc outputs and their common DC return to provide regulation at those remote points.

5.5.4.3   Ripple and Noise

Ripple and noise are defined as periodic or random signals over the frequency band of 10 Hz to 30 MHz. The power supply DC output ripple and noise will not exceed the values shown in Table 5-5: Ripple and Noise.

Table 5-5: Ripple and Noise

VOLTAGE	Ripple/Noise pk-pk	Ripple/Noise pk-pk
+3.3 V	1.5%	50 mV
+5 V	1%	50 mV
+12 V	1%	120 mV
-12 V	1%	120 mV
+5 V Standby	2%	100 mV
+15 V Standby	5%	750 mV

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5.5.4.4 Over-voltage Protection

The power supply over-voltage protection is sensed locally. The power supply will shut down in a latch off mode after an over-voltage condition. The latch is cleared by toggling the power supply on signal, or by an AC power interruption of greater than 1 second but less than 10 seconds to reset from the latch off condition. This limit applies over all specified AC input voltages and output loading conditions. Table 5-6: Over-voltage Protection contains the over-voltage limits. The values are measured at the output of the power supply connector.

Table 5-6: Over-voltage Protection

Output Voltage	Protection Point [V]
+3.3 V	3.8 – 4.3
+5 V	6.0 – 6.5
+12 V	13 – 14

5.5.4.5 Over-current Protection

The power supply has current limits to prevent the +3.3 Vdc, +5 Vdc, and +12 Vdc outputs from exceeding the values shown in Table 5-7: Over-current Protection. The current limiting is of the voltage fold-back type. The over-current limit level is maintained for a period of 1.6 seconds minimum and 2.0 seconds maximum. After this time, the power supply latches off. The latch will be cleared as described in Section Over-voltage Protection. The power supply will not be damaged from repeated power cycling in this condition.

Table 5-7: Over-current Protection

Voltage	Over Current Limit
+3.3 V	39.6 A minimum; 46.8 A maximum
+5 V	39.6 A minimum; 46.8 A maximum
+12 V	46 A minimum; 51 A maximum

5.5.4.6 Short Circuit Protection

The power supply will not be damaged by application of a short circuit to any DC output. Short circuits will not turn into the over-current protection process described in Section Over-current

Protection. A hard short circuit should turn off the power supply immediately. A hard short circuit is defined as when the load level is less than 10 milliohms.

5.5.4.7   Current Share Requirements

Equal power sharing of paralleled power supplies is required. The failure of a power supply does not affect the current sharing or output voltages of other power supplies still in operation in a redundant configuration.

The +3.3 V, +5 V, and +12 V output currents of paralleled supplies maintain a load deviation of $\pm$ 10% at rated current.

Signals to control current share may consist of one wire connecting all paralleled supplies for each output voltage required to share current. One separate ground wire may be supplied for these signals, if required.

5.6   Control Signals

5.6.1   Power Supply On (Input)

The power supply on circuit will be safety extra-low voltage (SELV). Upon receiving this signal, the power supply is turned on and power outputs and other signals are provided at the corresponding DC connector output pins. The characteristics of this signal are shown in Table 5-8: Power Supply on Specification. The power supply on is an input signal to the power supply from the system.

Table 5-8: Power Supply on Specification

DC Power Enable Signal	Voltage Level †	Current
HIGH, PWR SUPPLY ENABLED	4 V min	0.5 mA max source current
LOW, PWR SUPPLY DISABLED	1 V max or open circuit	

† Measured relative to the power supply DC common output ground pins.

5.6.2   AC OK Signal (Output)

Each power supply provides an "AC OK" signal. A pin must be allocated for this signal on the DC connector. This signal indicates that input line AC voltage has reached the minimum level to power up the corresponding power supply. This signal is to be utilized by the system to synchronize the power on timing of multiple power supplies within the system. The characteristics of the AC OK signal are shown in Table 5-9: AC Good Signal.

Table 5-9: AC Good Signal

AC OK Signal	Voltage Level †	Current
LOW: AC is not yet up to the level.	0.4 V max	4 mA min sink current
HIGH: AC is up to the level.	4 V min	0.5 mA max source current

† Measured relative to the power supply DC common output ground pins

5.6.3   Power Good (Output)

Each power supply provides a power good signal. A pin must be allocated for this signal. This signal indicates that all outputs have reached acceptable operating voltage. The power good signal levels and sourcing/sinking requirements are shown in Table 5-10: Power Good Signal. The power good signal is an output signal from the power supply to the system.

Table 5-10: Power Good Signal

Power Good Signal	Voltage Level †	Current
LOW STATE DE-ASSERTED (Power Not Good)	0.4 V max	4 mA min sink current
HIGH STATE ASSERTED (Power Good)	4 V min	0.5 mA max source current

† Measured relative to the power supply DC common output ground pins.

The power good signal is held low until all outputs have reached at least 90% of their respective operating voltages. The turn on delay for the power good signal is between 100 and 1500 milliseconds.

The power good signal is low for a minimum of 1 millisecond before any of the output voltages fall below the regulation limits. Tests are conducted with a maximum load and minimum line voltage.

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```
                                              ┌──────────┐  TTL HIGH
POWER                                         │          │
GOOD                                          │          │  TTL LOW
SIGNAL    ───────────────────────────────────┘          └───────────
       Vn ─ ─ ─ ─ ─ ─ ─ ─ ─ ─ ─ ─ ─ ─ ─ ┌─────────────────┐
       Vm                               ╱                   ╲
+5VDC                                  ╱   │            │    ╲
OUTPUT                                ╱    │            │     ╲
VOLTAGE  ────────────────────────────      │            │      ─────
                                      │← t1→│            │← t2→│
                                    (100-1500msec)       (1msec min.)
```

Vn Nominal Output Voltage +5 VDC
Vm Minimum Output Voltage +4.75 VDC
t1 Delay Turn-on (100-1500msec)
t2 Delay Turn-off(1msec min)
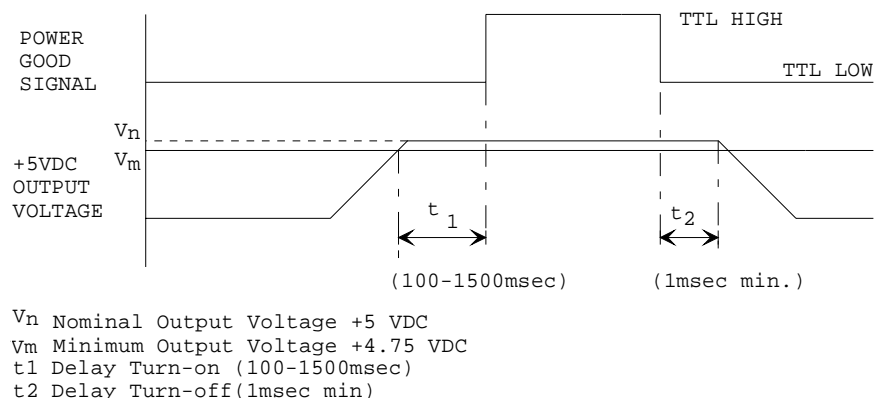
Figure 5-5: Power Good Signal Characteristics

5.6.4   Power Supply Present Indicator (Output)

This signal is used to sense the number of power supplies in the system (operational or not). A pin on the output connector must be allocated to pull the power supply present signal on the power supply backplane to DC output ground. Without this pull-down, the power supply present signal will be pulled up through a pull-up resistor to +5 V standby on the backplane. The power supply present is an output signal from the power supply to the system.

5.6.5   Predictive Failure Signal (Output)

This signal is available on the power supply connector. A "high" state in this signal indicates that the power supply is likely to fail in the near future due to a poorly performing fan. The predictive fan failure signal going "high" will not cause the power supply to shut down, but it must cause the "PRED FAIL" LED to turn on. The predictive failure is an output signal from the power supply to the system.

Table 5-11: Predictive Failure Signals

Predictive Failure Signal	Voltage Level †	Current
LOW STATE (power supply OK)	0.4 V max	4 mA min sink current
HIGH STATE (poorly performing fan)	4 V min	0.5 mA max source current

† Measured relative to the power supply DC common output ground pins

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5.6.6   Power Supply Failure Signal (Output)

This signal is available on the power supply connector. Upon receiving this signal, the system informs the operator that the appropriate power supply has failed, and therefore, a replacement

of that power supply is necessary. A "low" state indicates the power supply failure. The power supply failure signal is an output signal from the power supply to the system.

Table 5-12: Power Supply Failure

Power Supply Failure Signal	Voltage Level †
LOW STATE (power supply failure)	0.4 V max
HIGH STATE (power supply OK)	4 V min

† Measured relative to the power supply DC common output ground pins.

5.6.7   Power Supply Kill (Input)

The power supply kill signal is available on the power supply connector. The mating pin of this signal on the backplane should be tied to ground potential on the backplane. Internal to the power supply, the power supply kill pin should be connected to the +5 V standby through a pull-up resistor.

Upon receiving a low state signal at the power supply kill pin, the power supply will be allowed to turn on. A logic low on this pin by itself should not turn on the power outputs. With the power supply kill signal in a low state, a logic high signal on the power supply on signal will be able to turn on the power supply.

When this pin is pulled up high (power supply is extracting from the backplane), the power supply should be shut down immediately without any delay, regardless of the condition of the PS_On signal.

The truth table for the logic of power supply kill and power supply on is shown in Table 5-13: Logic Table for Power Supply Kill and Power Supply On.

Table 5-13: Logic Table for Power Supply Kill and Power Supply On

Power Supply Kill	Power Supply On	Power Supply Conditions
Low	High	DC outputs are On
X	Low	DC outputs are Off
High	X	DC outputs are Off

The characteristics of the power supply kill signal are shown in Table 5-14: Power Supply Kill Specification. The power supply kill is an input signal to the power supply from the system.

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Table 5-14: Power Supply Kill Specification

Power Supply Kill Signal	Voltage Level †
HIGH, PWR SUPPLY IS DISABLED	4.5 V minimum
LOW, PWR SUPPLY IS ENABLED	0.25 V maximum

† Measured relative to the power supply DC common output ground pins.

5.6.8 Power Supply Field Replacement Unit Signals

Four pins are allocated for the FRU information on the power supply connector. One pin is the Serial Clock (SCL). The second pin is used for Serial Data (SDA). Both pins are bidirectional and are used to form a serial bus. The third pin is address line A0 of the EEPROM, and the last pin is address line A1 of the EEPROM.

Inside the power supply, the highest address bit of the EEPROM A2 should be tied to +5 V standby on the cathode side of the OR'ing diode.

The Vcc pin of the EEPROM should also be tied to the +5 V standby on the cathode side of the OR'ing diode so that even during failure, the FRU information within the power supply can be accessed.

The write control (or write protect) pin should be tied to ground inside the power supply so that information can be written to the EEPROM.

5.6.9 LED Indicators

There is a green power LED (PWR) to indicate that AC is applied to the power supply and standby voltages are available when blinking. This same LED goes solid to indicate that all the power outputs are ready. There is a yellow power supply fail LED (FAIL) to indicate that the power supply has failed and a replacement of the unit is necessary. There is a yellow predictive failure LED (PRFL) to indicate that the power supply is about to fail in the near future due to a poor performing fan. This LED should be blinking to indicate the predictive failure condition and should be latched into the blinking state once the condition has occurred. Refer to Table 5-15: Power Supply LEDs and Output Signal State Logic for conditions of the LEDs. The LEDs are marked as shown in Table 5-15: Power Supply LEDs and Output Signal State Logic.

The LEDs are visible on the power supply surface that is opposite the docking end. The LED location meets ESD requirements. LEDs are securely mounted in such a way that incidental pressure on the LED will not cause it to become displaced.

Table 5-15: Power Supply LEDs and Output Signal State Logic shows the LED indicator and the control signals.

Table 5-15: Power Supply LEDs and Output Signal State Logic

Conditions	Power Supply LEDs			Power Supply Output Signal States			Input to PS
	PWR (green)	PRFL (yellow)	FAIL (yellow)	P_Good H = pwr good	Pred. Failure H = pred. failure	PS Failure H = PS OK	PS On H = PS enable
No AC Power	OFF	OFF	OFF	L	L	L	L
AC In/Standby On	Blinking	OFF	OFF	L	L	H	L
DC Outputs OK	ON	OFF	OFF	H	L	H	H
Power Supply Failure	OFF	OFF	ON	L	L	L	H
Current Limit	ON	OFF	Blinking/ No Latch	L	L	H	H
Predictive Failure	ON	Blinking/ Latched	OFF	H	H	H	H

5.7 Fan Speed Control

The fan circuitry implements variable speed fan control and fan failure detection.

5.8 Environmental Requirements

5.8.1 Physical Environment

The power supply is located inside an Intel® system assembly. A system may contain two or three power supplies.

5.8.2 Thermal Protection

The power supply incorporates thermal protection that causes a shutdown if air flow through the power supply is insufficient. Thermal protection activates a shutdown if the temperature of any power supply component is more than 85% (°C) of rated temperature. This shutdown takes place prior to over-temperature induced damage to the power supply.

5.9 Regulatory Agency Requirements

The power supply must have UL recognition, CSA certification to level 3, Bauart and any NOR-DIC CENELEC certified (such as SEMKO, NEMKO or SETI) markings demonstrating compliance. The power supply must also meet FCC Class B, VDE 0871 Level B, and CISPR Class B requirements.

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6.   System Software

This chapter describes three software components of the OCPRF100 MP server system product:

- System BIOS
- BIOS Setup Utility
- iFLASH

Detailed information about these components can be found in the *OPRF100 MP Board Set Technical Product Specification*

Drawing from previous Intel® products, the system BIOS provides standard PC-compatible features plus routines that support the extended hardware features of the OCPRF100 MP server system's OPRF100 board set and chassis. These extended features include:

- Eight symmetric processors
- 32 GB of shared memory using PC-100 registered DIMMs
- Four peer PCI buses
- 10 hot-plug PCI slots (with four 66-MHz/64-bit slots and six 33-MHz/64-bit slots)

The BIOS configures the Profusion PCIset including the memory controller and PCI host bridges. It also supports the server management capabilities of the Intelligent Platform Management Bus (IPMB).

Adherence to industry standards enables a wide range of "shrink wrapped" operating systems and adapter choices. Intel has participated in industry initiatives to develop standards that address highly scalable machines.

A system vendor can customize the OCPRF100 MP server system product through the user binary facility. This facility provides for splash screens and other custom code that can differentiate a product offering. In addition to the space reserved for user binaries, over 1 MB of the system flash ROM is reserved for use by system vendors.

The system BIOS includes features that enhance the reliability, availability, and serviceability (RAS) of the product. The BIOS Power-on Self-test (POST) contains routines that check the integrity of processors, memory DIMMs, memory ports, and coherency filters. If these routines detect a failure, BIOS deconfigures the failing device and attempts to boot using the healthy hardware that remains. Like previous Intel® platforms, BIOS provides a consistent way to handle, display, and record system errors that occur during POST or during run-time. Errors are recorded in a system event log (SEL) which is available in-band from a system processor and out-of-band over the IPMB.

Because the BIOS automatically configures system resources, many users will never need to execute a configuration utility. Nevertheless, the system provides a flash-resident setup utility that allows users to set preferences about system operation. This utility, called BIOS Setup, is

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entered by pressing F2 during POST. BIOS Setup is further described in Section BIOS Setup Utility.[1]

The iFLASH utility updates the system flash ROM. It provides security features that reduce the risk of tampering.

A recovery boot block allows recovery from catastrophic problems. The recovery boot block is electrically protected from erasure by a jumper on the OPRF100 I/O carrier.

6.1   System Hardware

The OCPRF100 MP server system supports eight Pentium III Xeon processors. The Profusion PCIset connects these processors in a symmetric, cache-coherent configuration. The system supports a wide range of memory configurations from a minimum of 128 MB to a maximum of 32 GB.[2] Four peer PCI buses provide high-speed access to resources in 10 hot-plug, 64-bit PCI slots.

For additional information about the chip set, see the *Gemini External Design Specification* and the *PB64 External Design Specification*. For additional board set information, see the *OPRF100 MP Board Set Technical Product Specification.*

6.1.1   Processors

The BIOS supports eight-way symmetric multiprocessing (SMP) using the Pentium III Xeon processor and the Profusion PCIset. It automatically detects and initializes each processor. The BIOS permits mixed steppings of the processor. The flash ROM contains space for four updates.[3]

BIOS supports the following processor features:

- Power-on Built-in Self-test (BIST)

- Processor bus error checking and correcting (ECC)

- Processor BIOS updates

- System management mode (SMM)

- Memory type range registers (MTRRs)

- Model specific registers (MSRs)

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1. BIOS Setup should not be confused with the System Setup Utility (SSU), a DOS-based program that provides the means to specially configure adapter cards and various embedded devices. See the *System Setup Utility External Product Specification* for more information.
2. Support for 32 GB depends upon the commercial availability of the required DIMMs.
3. Although BIOS supports mixed steppings, uncharacterized errata may exist. Intel recommends using identical steppings because other configurations receive limited, if any, testing. The system BIOS does not support combinations that have known incompatibilities. Refer to the processor literature for further information about mixing processor steppings.

If the boot strap processor (BSP) fails during POST, BIOS will attempt to boot the system using another processor. This feature is called fault resilient booting (FRB). For additional information on FRB, see the *OPRF100 MP Board Set Technical Product Specification.*

6.1.2   Profusion® Chip Set

The Profusion PCIset connects the processors, memory, and four peer PCI buses. It consists of the memory access controller (MAC), data interface buffer (DIB), and PCI host bridge (PB64).

The OCPRF100 MP server system BIOS supports the following features of the chip set:

- Memory port interleaving
- Coherency filters
- Coherency rules SRAM
- Routing of memory cycles for PCI, VGA, APICs, and ROM space
- Routing of I/O cycles
- System management RAM (SMRAM)
- Bus ECC
- Memory ECC

Memory gaps from 512KB to 640KB and from 15 MB to 16 MB are not supported. The memory in these regions is treated as normal system memory; memory-mapped I/O resources cannot be placed there.

BIOS automatically initializes system memory, the coherency filters, and the rules SRAM. It examines the PC-100 serial presence detect (SPD) EEPROMs on the PC-100 DIMMs and adjusts the memory timings accordingly. Three levels of memory tests accommodate different preferences about test time versus thoroughness. For higher availability, BIOS can deconfigure a failing memory DIMM, memory port, and coherency filter.

6.1.3   I/O Subsystem

The OPRF100 I/O carrier provides a PC-AT compatible I/O subsystem with PCI slots instead of ISA/EISA slots. It provides 10 PCI slots, an embedded PCI VGA, and an embedded dual-channel LVDS controller. It also supports the standard compatibility devices: two serial ports, one parallel port, two USB ports, an IDE port, a floppy controller, and a PS/2 keyboard and mouse.

The PIIX4E provides the bridge to ISA-compatible resources on the I/O carrier. It also provides an IDE controller and a USB controller. BIOS uses its SMBus to access the SPD EEPROMs on the PC-100 DIMMs. BIOS uses the 256 bytes of CMOS configuration RAM for nonvolatile storage of BIOS Setup options and other BIOS parameters.

The SMC* Ultra I/O chip (FDC37C937APM) provides a floppy controller, parallel port, two serial ports, a keyboard port, and a mouse port. The BIOS supports four modes of the parallel port: output-only, bidirectional, enhanced parallel port (EPP), and extended capabilities port (ECP). The

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Ultra I/O chip also provides a keyboard controller containing Phoenix* microcode. BIOS down-loads commands to the keyboard controller to provide various security features.

The I/O carrier contains 10 hot-plug PCI slots plus a PCI SVGA controller (Cirrus Logic* CL-GD5446) and a dual-channel low-voltage differential SCSI controller (Symbios* SYM53C896). The flash ROM contains the option ROM (OPROM) for both of these components.

BIOS uses the programmable interrupt device (PID) to route PCI interrupts to the AT-compatible PICs. The PID also contains an I/O APIC that can handle interrupts when enabled by the operating system (OS). BIOS provides the standard Plug and Play interfaces for PCI interrupt routing.

The system flash ROM contains 2 MB of field programmable memory. The upper 1 MB contains BIOS and other regions reserved for Intel. The lower 1 MB is available for use by system vendors. BIOS implements a security mechanism that reduces the risk of unauthorized modification of the system flash ROM.

6.1.4   Intelligent Platform Management Bus

BIOS communicates with the IPMB to update the SEL through the baseboard management controller (BMC), display messages on the LCD, and implement FRB. By passing messages over the IPMB to the BMC, server management cards can access the log, even if the system processors are not running.

The server management interface controller (SMIC) provides the gateway to the IPMB. The BMC accesses many of the system components.

The BIOS provides interface functions that allow real-mode software to send messages over the IPMB.

6.2   Industry Standards

The OCPRF100 MP server system BIOS supports industry standards wherever possible. These standards expand the range of operating systems, software, adapters, and peripheral devices supported by the system.

System vendors that develop software to differentiate their server products also benefit because standards provide a consistent programming interface, regardless of the underlying hardware.

The system BIOS is governed by the following industry standards.

6.2.1   ACPI

The system BIOS supports the *Advanced Configuration and Power Interface (ACPI) Specification*, Revision 1.0. ACPI is the key element in operating system directed power management. It supports an orderly transition from existing (legacy) hardware to ACPI-compliant hardware. With ACPI, the operating system can take direct control over the power management and Plug and Play functions of the system. ACPI makes the MPS table and the Plug and Play BIOS run-time interfaces obsolete.

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The system supports the S1, S4 OS, and S5 sleep states. It also supports Wake-on-LAN* from the S1 and S4 states.

After the operating system sends the command to switch to ACPI mode, the power button acts as a sleep button and a power button. If the button is pressed for less than four seconds, the system enters a sleep state determined by the operating system. If it is pressed for more than four seconds, the system powers down to the S5 state.

S1 Sleep State. The system enters the S1 sleep state when the power button is pressed momentarily or when the operating system directs it to enter S1. The S1 sleep state retains the system context; all processors' caches, memory, and chip set devices retain their state information. Only the power button and power management events (Wake-on-LAN) can wake the system from S1.

S4 Sleep State. The system enters the S4 state when the power button is pressed (if configured for hibernation) or when the hibernate option is chosen in the shutdown menu. If the operating system supports save-to-disk, it stores the system context to hard disk before powering down. When the system powers on, the operating system restores all processes from the disk. When the system awakens, BIOS performs a normal boot; BIOS does not participate in saving and restoring the system context.

S5 Sleep State. The system powers down without saving context.

6.2.2   Boot Devices and Peripherals

The system BIOS supports a wide range of peripherals and boot devices. The system can boot an operating system from a floppy, an IDE device, a SCSI device, a network card, or an I_2O device. Bootable CD-ROMs are supported in emulation and nonemulation modes.

The system BIOS supports the following specifications:

- *BIOS Boot Specification*, Version 1.01.

- *El Torito CD-ROM Boot Specification*, Version 1.0.

- *Intelligent I/O (I_2O) Architecture Specification*, Revision 1.0.

- *Universal Serial Bus (USB) Specification*, Revision 1.0.

Legacy USB devices are not supported by BIOS, but nothing in BIOS precludes support by an operating system. A USB-aware operating system can enable the USB functionality.

Ordinarily, the system BIOS boots from the first device detected in its scan order. If adapters conform to the *BIOS Boot Specification*, the boot device can be selected without changing the placement of the adapter cards.

I_2O defines a standard architecture for intelligent I/O. This is an approach to I/O in which low-level interrupts are handled by specially designed I/O processors which communicate by passing messages. Although the OCPRF100 MP server system does not include any built-in I_2O devices,

the system BIOS provides the run-time functions necessary to boot from an I$_2$O mass-storage adapter card. I$_2$O devices are added to the interrupt 13h chain and booted using these calls.

6.2.3   Management

Management of clients and servers is a major issue for end users. The system BIOS supports server management applications through the following specifications:

- *Desktop Management Interface (DMI) Specification*, Version 2.00

- *System Management BIOS (SMBIOS) Reference Specification*, Version 2.1

- *Wired for Management Baseline Specification*, Version 1.1a

The BIOS provides the data and interfaces required by the DMI specification. In addition, the BIOS provides a memory image of DMI data to allow operating systems to read DMI structures from protected-mode.

6.2.4   Configuration

Plug and Play compatibility allows most devices to be added to the system with no manual configuration at all. The BIOS supports the following industry standards for full Plug and Play compatibility:

- *Multiprocessor Specification (MPS)*, Versions 1.1 and 1.4

- *Extended System Configuration Data Specification*, Version 1.02a

- *Plug and Play BIOS Specification*, Version 1.0a

- *Plug and Play ISA Specification*, Version 1.0a

- *PCI Specification*, Revision 2.1

- *PCI BIOS Specification*, Revision 2.1

- *PCI to PCI Bridge Specification*, Revision 1.0

- *PCI Power Management Specification*, Revision 1.0

- *PCI Hot-plug Specification*, Revision 1.0

- *POST Memory Manager (PMM) Specification*, Version 1.01

Although the system contains no ISA slots, the *Plug and Play ISA Specification* is supported because of the embedded peripherals.

The system BIOS can support either version of the *Multiprocessor Specification.* If version 1.1 is selected, BIOS simply includes entries for the processors, buses, APICs, and interrupts. If version 1.4 is selected, BIOS also creates entries describing the bus, memory, and I/O topology of the system. BIOS Setup allows the user to specify which version of tables should be generated.

The BIOS allows users to use the SSU to specify PIC-mode interrupt assignments. This configuration step is completely optional unless required by higher level software.

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6.3   BIOS Setup Utility

The OCPRF100 MP server system BIOS automatically configures system resources. BIOS Setup allows the user to set preferences about system operation. It stores these preferences in CMOS configuration RAM. Because BIOS Setup resides in flash ROM, the user can invoke it without booting an operating system.

During POST, BIOS prompts the user to enter BIOS Setup with the following message:

```
Press <F2> to enter Setup
```

After the user presses F2, a few seconds may pass while BIOS completes its test and initialization tasks.

BIOS Setup supports security passwords which reduce the risk of unauthorized modifications. If enabled, BIOS Setup requests an administrator password before allowing modifications.

Screen Format. The BIOS Setup screen is divided into four functional areas.

Table 6-1. BIOS Setup Screen Format

Functional Areas	Description
Menu Selection Bar	Located at the top of the screen, the Menu Selection Bar allows the user to select the top level menus. These are the Main Menu, Advanced Menu, Security Menu, Server Menu, and Boot Menu.
Menu Area	Located at the center of the screen, the Menu Area displays options and information. Some items have submenus.
Item Specific Help	Located at the right side of the screen, this area supplies help messages for the menu items.
Keyboard Command Bar	Located at the bottom of the screen, the Keyboard Command Bar displays keyboard commands for modifying settings and for navigating through the menus and submenus.

Keyboard Commands. BIOS Setup supports the following keystroke commands.

Table 6-2. BIOS Setup Keyboard Commands

Key	Command	Description
F1	**Help**	Pressing F1 on any menu invokes the general help window.

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Table 6-2. BIOS Setup Keyboard Commands

ESC	**Exit**	The Escape key allows the user to back out of any field. When the Escape key is pressed while editing a field, the edit of that field is terminated. When the Escape key is pressed in a submenu, the parent menu is re-entered. When it is pressed in a top-level menu, the Exit Menu appears.
¦	**Select Item**	The up arrow selects the previous value in an option list.
Ø	**Select Item**	The down arrow selects the next value in an option list.
´	**Select Menu**	The left and right arrow keys move between top level menus.
-	**Change Value**	The minus key changes the value of an item to the previous value in the list.
+	**Change Value**	The plus key changes the value of an item to the next value in the list. Pressing the space bar performs the same function.
Enter	**Execute Command**	The Enter key activates submenus, selects options, and changes an item's value.
F9	**Setup Defaults**	The F9 key restores the default values for configuration options. A pop-up menu confirms the choice before modifying the values.
F10	**Save and Exit**	The F10 key saves the settings and reboots the system. A pop-up menu confirms the choice before saving the values.

6.3.1   Main Menu

Table 6-3: Main Menu through Table 6-6: Keyboard Features Submenu describe the Main Menu and its submenus.

Table 6-3: Main Menu

Feature	Option	Description
System Time	HH:MM:SS	Sets the system time.
System Date	MM/DD/YYYY	Sets the system date.
Legacy Diskette A:	Disabled 360KB, 5 ¼" 1.2 MB, 5 ¼" 720KB, 3 ½" 1.44/1.25 MB, 3 ½"† 2.88 MB, 3 ½"	Selects the floppy diskette type for drive A.

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Table 6-3: Main Menu

Legacy Diskette B:	Disabled† 360KB, 5 ¼" 1.2 MB, 5 ¼" 720KB, 3 ½" 1.44/1.25 MB, 3 ½" 2.88 MB, 3 ½"	Selects the floppy diskette type for drive B.
Primary Master		Selects IDE submenu.
Primary Slave		Selects IDE submenu.
Processor Information		Selects Processor Information submenu.
Keyboard Features		Selects Keyboard Features submenu.
Language	English (US)† French German Italian Spanish	Selects language used by BIOS.

NOTES: Default values are marked with the "†" symbol.

Table 6-4. IDE Submenu

Feature	Option	Description
Autotype Fixed Disk		Pressing the Enter key instructs BIOS Setup to detect the type of fixed disk. If successful, the remaining value fields on this menu are automatically filled in.
Type	None CD-ROM IDE Removable ATAPI Removable User Auto†	If "Auto" is selected, BIOS determines the parameters during POST. If "User" is selected, BIOS Setup prompts the user to fill in the drive parameters. Drive types 1 through 39 are predetermined drive types.
Cylinders		Displays the number of cylinders.
Heads		Displays the number of read/write heads.
Sectors		Displays the number of sectors per track.
Maximum Capacity		Displays the capacity of the drive.
Multisector Transfers	Disabled 2 Sectors 4 Sectors 8 Sectors 16 Sectors	Displays status of multisector transfers. Autotyped by BIOS.

Table 6-4. IDE Submenu

LBA Mode Control	Disabled Enabled	Displays status of Logical Block Access. Autotyped by BIOS.
32 Bit I/O	Disabled† Enabled	Enables 32-bit IDE data transfers.
Transfer Mode	Standard Fast PIO 1 Fast PIO 2 Fast PIO 3 Fast PIO 4	Selects the method for transferring data to/from the drive. Auto-typed by BIOS.
Ultra-DMA Mode	Disabled Mode 0 Mode 1 Mode 2	Selects the Ultra-DMA mode used for transferring data to/from the drive. Autotyped by BIOS.

NOTES: Default values are marked with the "†" symbol.

Table 6-5: Processor Information Submenu

Feature	Option	Description
Left Processor 1 Stepping ID		Displays the stepping of the processor.
Left Processor 1 L2 Cache Size		Displays the size of the L2 cache.
Left Processor 2 Stepping ID		Displays the stepping of the processor.
Left Processor 2 L2 Cache Size		Displays the size of the L2 cache.
Left Processor 3 Stepping ID		Displays the stepping of the processor.
Left Processor 3 L2 Cache Size		Displays the size of the L2 cache.
Left Processor 4 Stepping ID		Displays the stepping of the processor.
Left Processor 4 L2 Cache Size		Displays the size of the L2 cache.
Right Processor 1 Stepping ID		Displays the stepping of the processor.
Right Processor 1 L2 Cache Size		Displays the size of the L2 cache.
Right Processor 2 Stepping ID		Displays the stepping of the processor.
Right Processor 2 L2 Cache Size		Displays the size of the L2 cache.
Right Processor 3 Stepping ID		Displays the stepping of the processor.
Right Processor 3 L2 Cache Size		Displays the size of the L2 cache.
Right Processor 4 Stepping ID		Displays the stepping of the processor.
Right Processor 4 L2 Cache Size		Displays the size of the L2 cache.

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Table 6-6: Keyboard Features Submenu

Feature	Option	Description
Numlock	Auto† On Off	Selects the power-on state of the Num Lock key.
Key click	Disabled† Enabled	Enables key click.
Keyboard auto-repeat rate	30/sec† 26.7/sec 21.8/sec 18.5/sec 13.3/sec 10/sec 6/sec 2/sec	Selects key repeat rate.
Keyboard auto-repeat delay	¼ sec ½ sec† ¾ sec 1 sec	Selects delay before key repeat.

NOTES: Default values are marked with the "†" symbol.

6.3.2   Advanced Menu

Table 6-7 through Table 6-11 describe the Advanced Menu and submenus.

Warning: Setting items on this menu to incorrect values may cause the system to malfunction.

Table 6-7: Advanced Menu

Feature	Option	Description
Reset Configuration Data	No† Yes	If "Yes" is selected, BIOS clears System Configuration Data during the next boot. The field is automatically reset to "No" in next boot.
System Wakeup Feature	Disabled† Enabled	Enables Wake-on-LAN for operating systems that do not support ACPI. If the operating system enables ACPI, this mode has no effect.
Use Multiprocessor Specification	1.1 1.4†	Selects the version of MP spec to use. Some operating systems require version 1.1 for compatibility reasons.
Large Disk Access Mode	CHS LBA†	Select the drive access method for IDE drives. Most operating systems use LBA or "Logical Block Addressing." Some operating systems, however, may use the CHS or "Cylinder-Head-Sector" method.Consult your operating system documentation for more information.

Table 6-7: Advanced Menu

Pause Before Boot	Disabled Enabled†	If enabled, BIOS pauses for five seconds before booting the operating system.
PCI Configuration		Selects PCI Configuration submenu.
I/O Device Configuration		Selects I/O Device Configuration submenu.
Advanced Chip Set Control		Selects Advanced Chip Set Control submenu.

NOTES: Default values are marked with the "†" symbol.

Table 6-8: PCI Configuration Submenu

Feature	Option	Description
Processor bus	100 MHz	Displays the clock speed of the processor bus.
PCI Slots 1-2	33 MHz	Displays the clock speed of PCI Segment A.
PCI Slots 3-6	33 MHz	Displays the clock speed of PCI Segment B.
PCI Slots 7-8	33 MHz 66 MHz	Displays the clock speed of PCI Segment C.
PCI Slots 9-10	33 MHz 66 MHz	Displays the clock speed of PCI Segment D.
PCI Device, Embedded SCSI		Selects PCI Mode Submenu for the embedded LVDS controller.
PCI Slot 1		Selects PCI Mode Submenu for this PCI slot.
PCI Slot 2		Selects PCI Mode Submenu for this PCI slot
PCI Slot 3		Selects PCI Mode Submenu for this PCI slot
PCI Slot 4		Selects PCI Mode Submenu for this PCI slot
PCI Slot 5		Selects PCI Mode Submenu for this PCI slot
PCI Slot 6		Selects PCI Mode Submenu for this PCI slot
PCI Slot 7		Selects PCI Mode Submenu for this PCI slot
PCI Slot 8		Selects PCI Mode Submenu for this PCI slot
PCI Slot 9		Selects PCI Mode Submenu for this PCI slot
PCI Slot 10		Selects PCI Mode Submenu for this PCI slot

Table 6-9: PCI Mode Submenu

Feature	Option	Description
Option ROM Scan	Disabled Enabled†	Enables option ROM scan.
Enable Master	Disabled Enabled†	Enables device(s) as a PCI bus master.
Latency Timer	Default 0020h 0040h 0060h 0080h† 00A0h 00C0h 00E0h	Specifies the minimum guaranteed number of PCI bus clocks that a device can master on a PCI bus during one transaction.

NOTES: Default values are marked with the "†" symbol.

Table 6-10: I/O Device Configuration Submenu

Feature	Option	Description
Serial Port A	Disabled Enabled† Auto	If set to "Auto," BIOS configures the port.
Base I/O Address	3F8h† 2F8h 3E8h 2E8h	Selects the base I/O address for COM port A.
Interrupt	IRQ 3 IRQ 4†	Selects the IRQ for COM port A.
Serial Port B	Disabled Enabled† Auto	If set to "Auto," BIOS configures the port.
Base I/O Address	3F8h 2F8h† 3E8h 2E8h	Selects the base I/O address for COM port B.
Interrupt	IRQ 3† IRQ 4	Selects the IRQ for COM port B.
Parallel Port	Disabled Enabled† Auto	If set to "Auto," BIOS configures the port.

Table 6-10: I/O Device Configuration Submenu

Mode	Output only Bidirectional† EPP ECP	Selects the mode of the LPT port.
Base I/O Address	378h† 278h 178h 3BCh	Selects the base I/O address for LPT port. 178h is only available when the LPT port is in EPP mode. Otherwise, 3BCh is available.
Interrupt	IRQ 5 IRQ 7†	Selects the IRQ for LPT port.
DMA channel	DMA 1 DMA 3†	Selects the DMA channel for LPT port when configured for ECP mode.
Floppy disk controller	Disabled Enabled† Auto	Enables embedded floppy disk controller.

NOTES: Default values are marked with the "†" symbol.

Table 6-11: Advanced Chip Set Control Submenu

Feature	Option	Description
Extended RAM Step	1 MB† 1KB Every location	Selects the thoroughness of the extended memory. If "1 MB" is selected, BIOS tests each 1 MB boundary. If "1KB" is selected, BIOS tests each 1KB boundary. If "Every location" is selected, BIOS tests every byte. BIOS defaults to the fastest test.
L2 Cache	Disabled Enabled†	Enables the second level cache. The second level cache should be disabled only for diagnostic purposes.
Multiboot Support	Disabled† Enabled	Enables Boot Device Selection.
Override PHP Switches	Disabled† Enabled	If enabled, all PCI slots power-up. If disabled, only PCI slots with plug-in cards power-up.

NOTES: Default values are marked with the "†" symbol.

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6.3.3   Security Menu

Table 6-12: Security Menu describes the Security Menu.

Table 6-12: Security Menu

Feature	Option	Description
User Password is	Set Clear†	Status only. Administrator password must be enabled before user password can be enabled. User password is enabled by entering a user password and disabled by entering a null user password.
Administrator Password is	Set Clear†	Status only. Enabled by entering an administrator password and disabled by entering a null administrator password.
Set User Password	Press Enter	When the Enter key is pressed, the user is prompted for a password; press ESC key to abort.
Set Administrator Password	Press Enter	When the Enter key is pressed, the user is prompted for a password; press ESC key to abort.
Password on boot	Disabled† Enabled	Requires password entry on boot. System remains in Secure Mode until password is entered. Password On Boot takes precedence over Secure Mode Boot.
Diskette access	User Administrator†	Controls access to diskette drives based on password.
Secure Mode Timer	Disabled† 1 min 2 min 5 min 10 min 20 min 1 hr 2 hr	Sets the period of key/PS2 mouse inactivity specified before Secure Mode activates. A password is required for Secure Mode to function.
Secure Mode Hot Key (Ctrl-Alt-?)	Disabled† [A, B, ..., Z]	Assigns a hot key that invokes Secure Mode.
Secure Mode Boot	Disabled† Enabled	System will boot in Secure Mode. The user must enter a password to unlock the system.
Video Blanking	Disabled† Enabled	Blank video when Secure Mode is activated. A password is required to unlock the system.
Floppy Write Protect	Disabled† Enabled	When Secure Mode is activated, the floppy drive is write protected. A password is required to re-enable floppy writes.
Front Panel Lockout	Disabled† Enabled	When Secure Mode is activated, the Reset and Power switches are locked. A password is required to unlock the system.

NOTES: Default values are marked with the "†" symbol.

6.3.4 Server Menu

Table 6-13: Server Menu through Table 6-16: Console Redirection Submenu describe the Server Menu and submenus.

Table 6-13: Server Menu

Feature	Option	Description
System Management		Selects System Management submenu.
Console Redirection		Selects Console Redirection submenu.
Processor Retest	No† Yes	Select "Yes" to clear historical processor status and retest all processors on the next boot.
EMP Password Switch	Disabled† Enabled	Enables the EMP password.
EMP Password		Selects the EMP password.
EMP ESC Sequence		This field is updated from the front panel controller firmware.
EMP Hangup Line String		This field is updated from the front panel controller firmware.
Modem Initialization String		This field is updated from the front panel controller firmware.
High Modem Initialization String		This field is updated from the front panel controller firmware.
EMP Access Mode	Pre-Boot Only Always Active Disabled†	Selected when the EMP is enabled. If "Always Active," the EMP is always enabled. If "Pre-Boot Only," the EMP is enabled during power down or POST only. If "Disabled," the EMP is disabled.
EMP Restricted Mode Access	Disabled† Enabled	Enables Restricted Mode. In Restricted Mode, Power Down, Front Panel NMI, and Reset Control via EMP are disabled.
EMP Direct Connect/ Modem Mode	Direct Connect† Modem Mode	Allows the user to connect to a local machine without using a modem.

NOTES: Default values are marked with the "†" symbol.

Table 6-14: System Management Submenu

Feature	Option	Description
Firmware SMIs	Disabled Enabled†	Enables SMI generation by agents on the Intelligent Platform Management Bus. Because BIOS requires SMIs for various tasks, setting this field to disabled does not disable all sources of SMIs.
System Event Logging	Disabled Enabled†	Enables logging of critical events.

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Table 6-14: System Management Submenu

Clear Event Log	Disabled† Enabled	Clears the system event log. This option is reset to disabled on each boot.
Memory Scrubbing	Disabled Enabled†	Enables memory scrubbing by the Profusion® chip set.
AERR Enable	Disabled Enabled†	Enables AERR to be asserted on the processor host buses.
Assert NMI on BERR	Disabled Enabled†	Enables BERR to be reported as a critical event via NMI. . Requires SERR to be enabled as well.
Assert NMI on PERR	Disabled† Enabled	Enables PERR to be reported as a critical event via NMI. Requires SERR to be enabled as well.
Assert NMI on SERR	Disabled Enabled†	Enables SERR to be reported as a critical event via NMI.
Enable Host Bus Error	Disabled Enabled†	Enables ECC checking on the processor buses.
FPC Error Check	Disabled† Enabled	Enables front panel controller (FPC) checking. If enabled, BIOS verifies that it can communicate with the FPC.
HSC Error Check	Disabled† Enabled	Enables hot-swap controller (HSC) checking. If enabled, BIOS verifies that it can communicate with the HSC.
Server Management Info		Selects Server Management Information submenu.

NOTES: Default values are marked with the "†" symbol.

Table 6-15: Server Management Information Submenu

Feature	Description
Board Part Number	Displays Board Part Number.
Board Serial Number	Displays Board Serial Number.
System Part Number	Displays System Part Number.
System Serial Number	Displays System Serial Number.
Chassis Part Number	Displays Chassis Part Number.
Chassis Serial Number	Displays Chassis Serial Number.
BMC Revision	Displays Baseboard Management Controller Revision.
FPC Revision	Displays Front Panel Controller Revision.
HSC Revision	Displays Hot-swap Controller Revision.

Table 6-16: Console Redirection Submenu

Feature	Option	?Description
COM Port Address	Disabled† 3F8 2F8 3E8	When enabled, use the I/O port specified.
IRQ #	3† 4	When enabled, use the IRQ specified.
COM Port Baud Rate	9600† 19.2KB 38.4KB 115.2KB	When enabled, use the baud rate specified. The maximum baud rate supported by the Emergency Management Port is 19.2K.
Flow Control	No Flow Control CTS/RTS XON/XOFF CTS/RTS + CD†	When enabled, use the flow control type specified.

NOTES: Default values are marked with the "†" symbol.

6.3.5   Boot Menu

Table 6-17 describes the Boot Menu options, which allow the user to select the boot device. This table also shows an example list of devices ordered in priority of the boot invocation. Items can be reprioritized by using the UP and DOWN arrow keys to select the device. Once the device is selected, use the + (plus) key to move the device higher in the boot priority list. Use the - (minus) key to move the device lower in the boot priority list.

Table 6-17: Boot Menu

Feature	Option	Description
Floppy Check	Disabled† Enabled	If Enabled, system will verify floppy type on boot. "Disabled" will result in a faster boot.
Boot Device Priority		Selects the Boot Device Priority submenu.
Hard Drive		Selects the Hard Drive submenu.
Removable Devices		Selects the Removable Devices submenu.
Removable Format		Selects the Removable Format submenu.
Maximum Number of I_2O Drives	1† 4	Selects the maximum number of I_2O (Intelligent I/O) drives that will be assigned a DOS drive.

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Table 6-17: Boot Menu

Message Timeout Mul-tiplier	1† 2 4 8 10 50 100 1000	All I_2O message timeout values are multiplied by this number.
Pause During POST	Disabled† Enabled	Use this to start the IRTOS (I_2O Real Time Operating System) man-ually. When POST has stopped, it issues three beeps. Pressing any key continues POST.

NOTES: Default values are marked with the "†" symbol.

6.3.6   Exit Menu

Table 6-18 describes the Exit Menu.

Table 6-18: Exit Menu

Option	Description
Exit Saving Changes	Exit Setup and save changes.
Exit Discarding Changes	Exit Setup without saving changes.
Load Setup Defaults	Load default values for all Setup items.
Load Custom Defaults	Load settings from Custom Defaults.
Save Custom Defaults	Save changes as Custom Defaults. If CMOS fails, BIOS uses Custom Defaults if available. If not, it uses the factory defaults.
Discard Changes	Load previous values of all Setup items.
Save Changes	Save all changes.

6.4   Flash Utility

The Flash Memory Update utility (iFLASH) updates the flash ROM with new system software. The loaded code and data include the following:

- System BIOS

- Embedded video BIOS and SCSI BIOS

- BIOS Setup Utility

- Integrator-supplied user binary area

- Language file

iFLASH communicates with the existing BIOS to provide security mechanisms which reduce the risk of tampering. It also communicates with BIOS to verify that the new BIOS image is compatible with the existing image. This helps to prevent an incorrect BIOS from being placed into flash memory.

iFLASH operates in three modes: Interactive Mode, Command Line Mode, and Recovery Mode. Interactive Mode and Command Line Mode are used in normal situations. In these modes, the user boots DOS and then executes the iFLASH utility. The keyboard and video monitor are available for issuing commands, locating files, and displaying progress. If iFLASH is interrupted by a power failure or by user intervention, the flash ROM may contain an incomplete BIOS. Recovery Mode provides a method to install the BIOS when the flash ROM has been corrupted.

For best results, iFLASH should run under DOS with no extended memory managers loaded. The flash utility does not support DPMI environments such as Windows*, Windows 95, or Windows NT*. Because the utility is written for DOS, it does not run under any other operating system.

For more information on iFLASH, see the *OPRF100 MP Board Set Technical Product Specification*.

7. Regulatory Specifications

The OCPRF100 MP server system, utilizing the OPRF100 board set, meets the specifications and regulations for safety and EMC as defined in this chapter.

7.1 Safety Compliance

USA/Canada:	UL 1950, 3rd Edition/CSA 22.2, No. 950-M93, 3rd Edition
Europe:	Low Voltage Directive, 73/23/EEC TUV/GS to EN60950 2nd Edition with Amendments, A1 = A2 + A3 + A4
International:	CB Certificate and Report to IEC 950, 2nd Edition w/ A1 + A2 + A3 + A4 including EMKO-TSE (74-SEC) 207/94

7.2 Electromagnetic Compatibility

USA	FCC 47 CFR Parts 2 and 15, Verified Class A Limit
Canada	IC ICES-003 Class A Limit
Europe	EMC Directive, 89/336/EEC EN55022, Class A Limit, Radiated & Conducted Emissions EN50082-1 Generic Immunity Standard EN61000-4-2 ESD Immunity (level 2 contact discharge, level 3 air discharge) EN61000-4-3 Radiated Immunity (level 2) EN61000-4-4 Electrical Fast Transient (level 2) EN61000-3-2 Harmonic Currents
Australia/New Zealand	AS/NZS 3548, Class A Limit
Japan	VCCI Class A ITE (CISPR 22, Class A Limit). IEC 1000-3-2; Harmonic Currents
International	CISPR 22, Class A Limit

7.3 CE Mark

The CE marking on this product indicates that the product is in compliance with the European Community's EMC Directive 89/336/EEC, and Low Voltage Directive, 73/23/EEC.

7.4   Electromagnetic Compatibility Notice (USA)

This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference, in which case the user will be required to correct the interference at his own expense.

7.5   Electromagnetic Compatibility Notices (International)

> この装置は、情報処理装置等電波障害自主規制協議会（ＶＣＣＩ）の基準に基づくクラスＡ情報技術装置です。この装置を家庭環境で使用すると電波妨害を引き起こすことがあります。この場合には使用者が適切な対策を講ずるよう要求されることがあります。

English translation of the notice above:
This is a Class A product based on the standard of the Voluntary Control Council for Interference by Information Technology Equipment (VCCI). If this equipment is used in a domestic environment, radio disturbance may arise. When such trouble occurs, the user may be required to take corrective actions.

> Cet appareil numérique respecte les limites bruits radioélectriques applicables aux appareils numériques de Classe A prescrites dans la norme sur le matériel brouilleur: "Appareils Numériques", NMB-003 édictée par le Ministre Canadian des Communications.

English translation of the notice above:
This digital apparatus does not exceed the Class A limits for radio noise emissions from digital apparatus set out in the interference-causing equipment standard entitled "Digital Apparatus," ICES-003 of the Canadian Department of Communications.

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8.   Peripheral Bay Backplane Board

This chapter describes the features and functionality of the peripheral bay backplane board, which is also referred to as the backplane. The backplane is designed in compliance with the *SCSI Command Set For Enclosure Services Document Specification*, and *SCSI Accessed Fault-Tolerant Enclosures Interface Specification.*

Features

The backplane supports the following features:

- Single channel maximum of two 1-inch or 1.6-inch low-voltage differential signal (LVDS) SCSI (16-bit) drives and one 8-bit SCSI device.

- Single connector attachment (SCA-2) connectors to simplify insertion and removal of hard disk drives.

- Insertion and removal of hard drives during power on (hot swap).

- LED indicators for each drive.

- Field effect transistor (FET) power control for each hard drive.

- FET short protection.

- Microcontroller to monitor enclosure services.

- I^2C bus for management information.

- Flash memory for upgrading firmware.

- Temperature sensing.

- Programmable logic device (PLD) reprogrammability.

- SCSI accessed fault-tolerant enclosures (SAF-TE).

- Tolerant of baseboard management controller (BMC) failure.

- Supports SCSI-3 (LVDS SCSI) and SCSI-2.

- LVD/SE multimode support.

- IDE/FD connections on board.

8.1   Peripheral Bay Backplane Overview

The backplane will be an LVDS SCSI design. The single backplane has one channel with SAF-TE and microcontroller with a capacity of two drives maximum, either 1.0 or 1.6 inches tall and 3.5 inches wide.

The backplane incorporates indicator LEDs. These LEDs will indicate drive power (green), drive activity (green), and drive fault (yellow). A light pipe will transmit the LED indicators from the backplane to the front bezel.

8.1.1   Architectural Overview

The backplane is an integral part of the OCPRF100 MP Server System. It is designed to provide a cost effective ease of power-on (hot-swap) drive replacement, provide easy RAID integration over a wide range of RAID controller products, and be vendor independent.

The single feature that simplifies RAID integration is the addition of an onboard SCSI target whose command set allows vendor independent controller management and monitoring for associated drive functions such as drive insertion and removal, light indicators, and drive power control. Its use simplifies cable management and eliminates errors caused by the possibility of incorrect correlation of several cables.

The backplane performs the tasks associated with hot-swappable SCSI drives, and enclosure (chassis) monitoring and management, as specified in the *SAF-TE Specification*. The tasks supported by the backplane include, but are not limited to, the following:

² Monitoring the SCSI bus for enclosure services messages, and acting on them appropriately. Examples of such messages include: activate a drive fault indicator, power down a drive which has failed, and report backplane temperature.

² SAF-TE intelligent agent, which acts as a proxy for "dumb" I^2C devices (that have no bus mastering capability) during intrachassis communications.

8.1.2   Placement Diagram
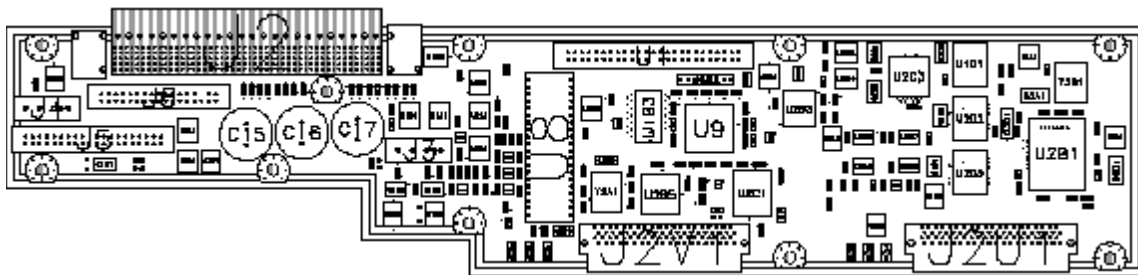
Figure 8-1: Placement Diagram Primary Side

8.1.3   Deviations from SAF-TE Specification

The SAF-TE specification requires the use of a PAIR signal. The intended use of this signal is to allow inter-backplane processor communication. Since this design is not intended to be connected to other backplanes, this signal is deemed unnecessary and is not implemented here.

8.2   Functional Description

This section defines the architecture of the backplane, including descriptions of functional blocks and how they operate. Figure 8-2: Functional Block Diagram shows the functional blocks on the SCSI channel of the backplane. An overview of each block follows.

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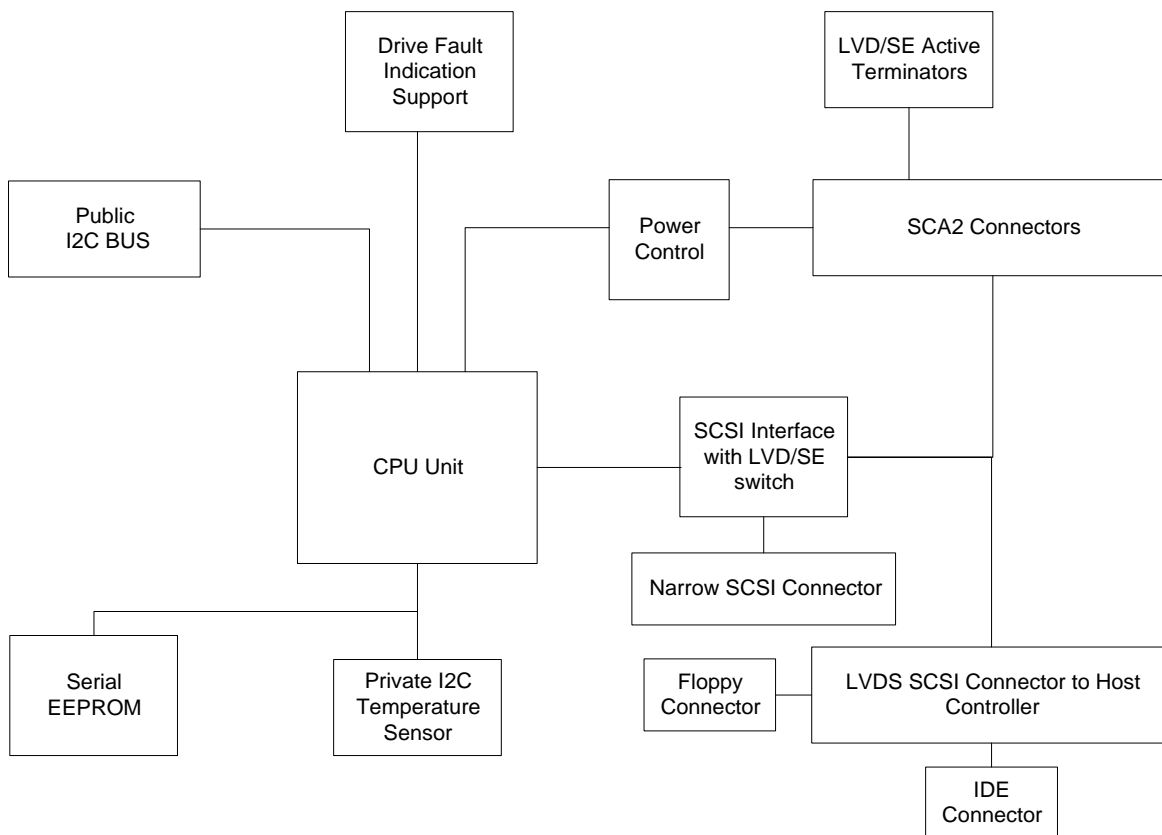
Figure 8-2: Functional Block Diagram

8.2.1   Hot-swap Connectors

The backplane provides two hot-swap SCA-2 right angle connectors, which provide power and SCSI signals using a single connector. Each SCSI drive attaches to the backplane using one of these connectors.

8.2.2   SCSI Interface

There is one LVDS SCSI channel on the backplane. The SCSI interface on the backplane provides the required additional circuitry between the SCSI bus and the microcontroller (containing the intelligence for the backplane), which allows the microcontroller to respond as a SCSI target. This is implemented using a Symbios Logic* 53C80S SCSI interface chip (or equivalent).

8.2.3   LVD/SE Active Termination

The LVD/SE active terminators provide SCSI-3 compliant termination for the backplane end of the SCSI bus. It is assumed that the other end of the SCSI segment is properly terminated as required by the SCSI-3 specification.

8.2.4   Power Control

Power control on the backplane supports the following features.

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² Spin-down of a drive when failure is detected and reported (using enclosure services messages) via the SCSI bus. An application or RAID controller detects a drive-related problem that indicates a data risk. In response, it takes the drive out of service and sends a spin down SCSI command to the drive. This decreases the likelihood that the drive is damaged during removal from the hot-swap drive bay. When a new drive is inserted, the power control waits a small amount of time for the drive to be fully seated, and then appiles power to the drive to prepare for operation.

² If system power is on, the backplane immediately powers off a drive slot when it detects a drive has been removed. This prevents possible damage to the drive when it is partially removed and reinserted while full power is available. It also prevents disruption of the entire SCSI array due to possible sags in supply voltage and resultant current spikes.

8.2.5   FET Short Protection

The FET short protection circuit is useful to protect both 12 volt and 5 volt power control FETs located on the backplane.

8.2.6   Microcontroller

The microcontroller provides all the intelligence for the LVDS SCSI backplane. It is an 80C652 microcontroller, with a built-in I^{2}C interface. The 80C652 microcontroller uses Flash for program code storage, and static RAM for program variables and buffers.

8.2.7   LED Arrangement

The three LEDs per drive are arranged as follows (viewed from the drive bay):
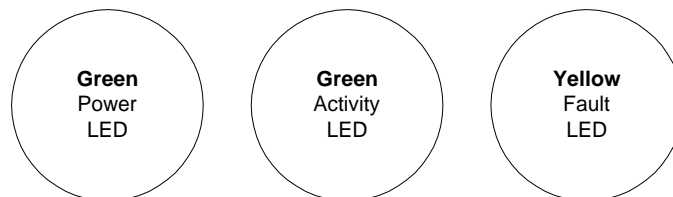

Figure 8-3: LED Arrangement

8.2.7.1   Power LEDs

Power LEDs are green and they indicate the drive is receiving power. Power LED control is driven by the FET switched +5 volts applied to the drive.

8.2.7.2   Drive Activity LEDs

The activity LEDs are green and are driven by the drive, pin 77, and interfaces directly to the LED.

8.2.7.3   Fault LEDs

The hot-swap controller is responsible for turning the drive fault LEDs on or off according to the states specified via commands received through SAF-TE and the IPMB. The drive fault LEDs are yellow and serve to indicate failure status for each drive. The LEDs are physically located on the LVDS SCSI backplane, and are driven from the backplane.

During initialization, the microcontroller flashes the LEDs for 2 seconds to signal POST completion successfully.

8.2.8   IPMB (I^{2}C bus)

The Intelligent Platform Management Bus(IPMB) is a system-wide I^{2}C server management bus. It provides a way for various system components to communicate independent of the other system interfaces (e.g., the PCI bus or the processor/memory bus). The I^{2}C bus controller is integrated into the microcontroller.

8.2.9   Temperature Sensor

A Dallas* DS1621 temperature sensor device is connected to each microcontroller on a "private" I^{2}C bus. This device is used to monitor the drive bay temperature. The temperature may be read via SAF-TE and IPMB commands. In addition, settable temperature thresholds are provided via IPMB commands. The hot-swap controller (HSC) can be configured to issue an event message on the IPMB when the temperature threshold is crossed.

Microcontroller programming implements the private I^{2}C connection by explicitly setting and clearing appropriate clock and data signals, to emulate an I^{2}C-like interface to the sensor.

8.2.10   Serial EEPROM

The AT24C02N* provides 256 bytes of nonvolatile storage. This is used to hold the serial number, part number, and other field replaceable unit (FRU) inventory information and miscellaneous application code used by firmware about the backplane.

8.3   Board Functions

This section describes functioning parts as required by the *SCSI Accessed Fault-Tolerant Enclosures Interface Specification* and *SCSI Command Set For Enclosure Services Document Specification*. In addition to these requirements, the board is capable of downloading code via IPMB to update the Flash executable code. The backplane functions begin at power up.

8.3.1   Reset

8.3.1.1   Cold Reset

At power up, all logic on the backplane is held in reset until the power supplies are stable. Two sources of power-good signaling are used. The first is the PWR_GOOD signal from the power

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supply. The second is the output from an onboard Dallas DS1233* reset controller, in which RST is kept active for approximately 350 ms after the power supply has reached the selected tolerance. These two signals are ORed to keep the board in reset. When both signals indicate that power is good, two things happen: 1) the reset signals are negated to the controllers, SCSI target, and other logic; and 2) power is applied sequentially to each SCA drive connector where a drive is present. Onboard logic sequentially enables each drive's FET drive power circuitry every 200 μsec.

8.3.2   Microcontroller

The microcontroller is a Philips* P80C652FBB operating at 12 MHz. The microprocessor boots itself up via code residing in the Flash boot block. The following is a list of the microcontroller features:

- Operating frequency from 1.2 MHz to 16 MHz.

- 80C51 based architecture.

- Four 8-bit I/O ports.

- Two 16-bit timer/counters.

- Full-duplex UART facilities.

- I^2C serial interface.

- Two power control modes: idle mode, power-down mode.

- Operating temperature range: 0°C to +70°C.

8.3.2.1   Overview

The 80C652 is a derivative of the 80C51 8-bit CMOS microcontroller. The 80C652 contains all of the features of the 80C51 (that is, the counter/timers T0 and T1, the serial I/O (UART), and four 8-bit I/O ports).

The 80C652 is pin-for-pin compatible and code compatible with the 80C51, except for additional Vss pins at the QFP package.

8.3.2.2   Differences from the 80C51*

The organization of the data memory is similar to the 80C51, except that the 80C652 has an additional 128 bytes of RAM overlapped with the special function register (SFR) space. This additional RAM is addressed using indirect addressing only and is available as stack space.

8.3.2.3   Special Function Registers

The 80C652 special function register space is the same as that on the 80C51, except that it contains four additional SFRs. The added registers are: S1CON, S1STA, S1DAT, and S1ADR. In addition to these, the UART special function registers SCON and SBUF have been renamed S0CON and S0BUF for clarity.

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Since the standard 80C51 onchip functions are the same on the 80C652, the SFR locations, bit locations, and operation are unchanged. The only exception is in the interrupt enable and interrupt priority SFRs. These have been changed to include the interrupt from the I^{2}C serial port.

8.3.2.4   I^{2}C Serial Communication-SI01

The I^{2}C pins are alternate functions to port pins P1.6 and P1.7. Because of this, P1.6 and P1.7 on these parts do not have a pull-up structure as found on the 80C51. Therefore P1.6 and P1.7 have open drain outputs on the 80C652.

8.3.2.5   I^{2}C Electrical Input/Output Specifications

The I^{2}C bus allows communication between devices made in different technologies, which might also use different supply voltages.

For devices with fixed input levels, operating on a supply voltage of +5 V ±10%, the following levels have been defined:

V_{ILmax} = 1.5 V (maximum input low voltage).
V_{IHmin} = 3 V (minimum input high voltage).

Devices operating on a fixed supply voltage different from +5 V (e.g., I^{2}L), must also have these input levels of 1.5 V and 3 V for V_{IL} and V_{IH} respectively.

For devices operating over a wide range of supply voltages (e.g., CMOS), the following levels have been defined:

V_{ILmax} = 0.3 V_{DD} (maximum input low voltage).
V_{IHmin} = 0.7 V_{DD} (minimum input high voltage).

For both groups of devices, the maximum output low value has been defined as follows:

V_{OLmax} = 0.4 V (maximum output voltage low) at 3 mA sink current.

The maximum low-level input current at V_{OLmax} of both the SDA pin and the SCL pin of an I^{2}C device is -10µA, including the leakage current of a possible output stage.

The maximum high-level input current at 0.9V_{DD} of both the SDA pin and SCL pin of an I^{2}C device is 10µA, including the leakage current of a possible output stage.

The maximum capacitance of both the SDA pin and the SCL pin of an I^{2}C device is 10 pf.

8.3.2.6   Noise Margin

Noise margin minimum on the low level is 0.1 V_{DD}.

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Noise margin minimum on the high level is 0.2 V_{DD}.

8.3.3   SCSI Controller

The SCSI controller selected for this backplane is an 8-bit SYM53C80S controller. Device selection is memory mapped at address FB00-FC00.

It is reset on power up and when reset is asserted to the backplane.

SYM53C80S access slows down the bus; it is recommended to pulse SAF-TE infrequently.

SAF_TE command processing is 2–10 ms. The following is a feature summary of the SCSI controller:

- Supports the ANSI X3.131-1994 standard.

- Parity generation with optional checking.

- No external clock required.

- Onchip 48 mA single-ended drivers and receivers.

- Functions in both the target and initiator roles.

- Direct control of all SCSI signals.

- Asynchronous data transfers of up to 5.0 MB/second.

- Variety of packaging options.

- SCSI protocol efficiency is directly proportional to the speed of the microprocessor.

- CMOS parts provide additional grounding and controlled fall times that reduce noise generated by SCSI bus switching.

- SCAM level 1 and 2 compatibility.

8.4   LVDS SCSI Termination

8.4.1   LVDS Termination

The following is a list of the features of the LVDS SCSI termination.

Auto selection multimode single ended or low-voltage differential termination

2.7 V to 5.25 V operation

Differential failsafe bias

Thermal packaging for low junction temperature and better MTBF

Master/slave inputs

Supports active negation

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Standby (Disable Mode) 5µA

3 pF channel capacitance

8.4.2   Single Ended Termination

The following is a list of the features of the single-ended SCSI termination.

- Fully compliant with SCSI, SCSI-2, and SCSI-3 standards.

- Backward compatible to the DS2107* and DS2107A*.

- Provides active termination for nine signal lines.

- Laser-trimmed 110 ohm termination resistors have 2% tolerance.

- Low dropout voltage regulator.

- Power-down mode isolates termination resistors from the bus.

- Fully supports actively negated SCSI signals.

- Onboard thermal shutdown circuitry.

8.5   Programmable Logic

PLDs are used in order to enhance board simplicity, board layout, and design maintainability. The backplane uses one Lattice* programmable logic device. The device is used for: address decode, drive power control, and miscellaneous registers. The following is a summary of the programmable logic features:

- High-performance, E^2CMOS technology.

- In-system programmability (ISP) via a simple 5-wire interface.

- 7.5 ns propagation delays with up a 125-MHz maximum operating frequency.

- Complete programmable device can combine glue logic and structured designs.

- Unused product term shutdown saves power.

- Programmable output slew rate control to minimize switching noise.

8.6   Memory Map

This section describes the microcontroller memory map and individual regions of memory. 80C652 architecture allows up to 64KB of byte-addressable memory. No I/O space is provided, since 80C652 architecture makes no distinction between memory and I/O addresses (all I/O accesses are memory-mapped). However, four I/O ports available to the microcontroller are also defined in this chapter.

8.6.1   Memory Map

Figure 8-4 shows the memory map viewed from the perspective of the microcontroller.

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A description of each memory block is provided, showing the purpose and function as determined by microcontroller programming. These functions may also be controlled by system software using SCSI commands defined in the SAF-TE specification.

```
FFFFH ┌─────────────────────────┬────┐
      │        RESERVED         │ ↑  │
FF00H ├─────────────────────────┤    │
      │        RESERVED         │    │
FE00H ├─────────────────────────┤    │
      │        RESERVED         │    │
FD00H ├─────────────────────────┤    │
      │        SCSI DACK        │    │
FC00H ├─────────────────────────┤ 2K │
      │         53C80S          │    │
FB00H ├─────────────────────────┤    │
      │      DRIVE PRESENT      │    │
FA00H ├─────────────────────────┤    │
      │      DRIVE POWER        │    │
F900H ├─────────────────────────┤    │
      │      DRIVE FAULT        │ ↓  │
F800H ├─────────────────────────┼────┤
      │                         │    │
      │          RAM            │30K │
      │                         │    │
8000H ├─────────────────────────┼────┤
      │                         │    │
      │         FLASH           │28K │
      │                         │    │
1000H ├─────────────────────────┼────┤
      │  WRITE PROTECTED FLASH  │ 4K │
0000H └─────────────────────────┴────┘
```
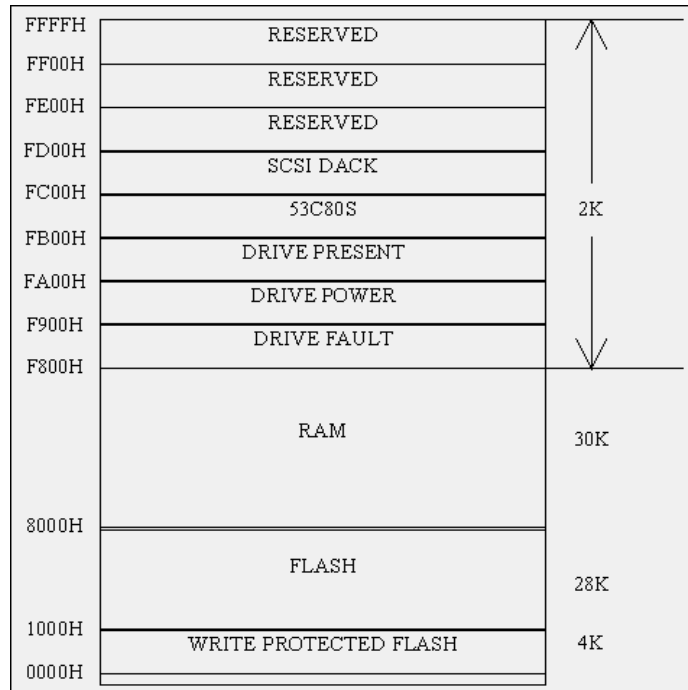
Figure 8-4: Microcontroller Memory Map

8.6.1.1   Flash Memory Region (0x0000 – 0x7FFF)

The Atmel* 27C257 or equivalent Flash EPROM is accessible as either a data or program memory read. Writes to Flash are also allowed in order to support field-upgradeable code. The lower 4KB (0x0000 – 0x0fff) are not writeable unless the boot block write protect bit in the fan mux register is cleared.

8.6.1.2   Static RAM Region (0x8000 – 0xF7FF)

The static RAM is accessible as either data or program accesses. It is possible to load executable code into the static RAM and execute directly from RAM.

8.6.1.3   Memory Mapped Registers (0xF800 – 0xFFFF)

The upper 2KB of the controller address space are mapped to eight regions of 256 bytes for memory-mapped registers and miscellaneous functions. For each of the regions listed, the actual function occupies less than the full 256 bytes of its address decode. Unless specifically stated,

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each region is a single address. Thus, aliases will occur on byte boundaries throughout the remainder of the region decoded for that function. Note that the eighth region from 0xFF00 – 0xFFFF is not used.

In register bit descriptions listed below, five fields are shown: the data bit number(s), the name of the field, how the bit(s) respond to a reset, whether the bits are readable and/or writeable, and a description of the field. RO indicates read-only, WO indicates write-only, and RW indicates readable and writeable. Any fields that are marked as reserved should be ignored when read, and should be set to zero when written.

8.6.1.3.1   Drive Fault Status Region (0xF800 – 0xF8FF)

The drive fault LEDs are controlled by this register. Writing a one to a bit turns the corresponding LED on. Reading the register returns the current state of the LEDs. A warm or cold reset clears all register bits to zero. The upper two bits are undefined.

Table 8-1: Drive Fault Status Byte Format

Bit(s)	Name	Reset Action	R/W	Description
7:2	Reserved	N/A		Reserved bits.
1:0	FLT[1:0]	Clear	RW	Drive fault LED enable. 0=LED off, 1=LED on. Bit 0 corresponds to drive ID 0.

8.6.1.3.2   Drive Power Enable Region (0xF900 – 0xF9FF)

Power is applied to a drive when its corresponding power-enable bit is set to one in this register. Following a cold reset, each drive that is present will have its power-enable bit turned on. A warm reset has no effect on this register.

Table 8-2: Drive Power Enable Byte Format

Bit(s)	Name	Reset Action	R/W	Description
7:2	Reserved	N/A		Reserved bits.
1:0	DRVPWR[1:0]	(see text)	RW	Drive power enable. 0=power off, 1=power on. Bit 0 corresponds to drive ID 0.

8.6.1.3.3   Drive Present Status Region (0xFA00 – 0xFAFF)

The absence or presence of each drive is detected by the state of pin 44 on that drive's SCA con-nector. A drive that is present will have its corresponding bit set to one in this register. Bits 7:6 in this register indicate the revision of the PLD code that is installed.

Table 8-3: Drive Present Status Byte Format

Bit(s)	Name	Reset Action	R/W	Description
1:0	DRVPRES[1:0]	N/A	RO	Drive present sense. 0=drive absent, 1=drive present. Bit 0 corresponds to drive ID 0.

SCSI Target Access Region (0xFB00 – 0xFBFF)
The Symbios 53C80 SCSI target appears to the controller as a set of eight registers at sequential addresses. For details, refer to the *Symbios SYM53C80E/S Data Manual.*

8.6.1.3.4   SCSI DACK Access Region (0xFC00 – 0xFCFF)

When the SCSI target is in DMA mode, data bytes may be read from or written to the 53C80S by reading or writing the DACK access region. This asserts the DACK_L input of the 53C80S instead of the CS_L input.

8.6.2   I/O Ports

80C652 architecture provides four memory-mapped I/O ports:

- Port #0 (P0).
- Port #1 (P1).
- Port #2 (P2).
- Port #3 (P3).

8.6.2.1   P0

Since the firmware for the microcontroller is located in a Flash memory device (for ease of debugging and for possible field upgradeability), and all memory and memory-mapped I/O is located outside the microcontroller, P0 is used as a time-multiplexed low-order address and data bus. It is not used for general I/O purposes.

8.6.2.2   P1

P1 has two dedicated-function signals, and six implementation-specific control signals, as shown in Table 8-4: P1 Functions.

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Table 8-4: P1 Functions

Bit	Name	I/O	Fixed†	Function
7	SDA	I/O	Y	I^{2}C serial data signal for the IPMB.
6	SCL	I/O	Y	I^{2}C serial clock signal for the IPMB.
5	Reserved	-	N	Reserved for future use.
4	SCSI _reset_L	O	N	Reset SCSI controller. If 0, places the 53C80S SCSI chip into reset. If 1, the SCSI interface chip comes out of reset and operates normally.
3	SCSI_DRQ	I	N	SCSI DMA Request. Connected to the DRQ signal of the 53C80S SCSI chip. Allows the microcontroller to use the DMA transfer capabilities of the SCSI interface chip, which results in higher performance.
2	Reserved	-	N	Reserved for future use.
1	SDA_Local	I/O	N	Serial data for private I^{2}C connection to temperature sensor.
0	SCL_Local	O	N	Serial clock for private I^{2}C connection to temperature sensor.

Notes:† "Fixed" indicates whether the function/pin is defined by the microcontroller pinout (fixed) or is implementation-specific (not fixed).

8.6.2.3   P2

P2 is the high-order address and data bus for external device access. It is not used for general I/O purposes.

8.6.2.4   P3

P3 provides four dedicated-function signals, and four implementation-specific control signals, as shown in Table 8-5: P3 Functions.

Table 8-5: P3 Functions

Bit	Name	I/O	Fixed†	Function
7	RD_L	O	Y	Read strobe. Indication from the microcontroller that the current bus cycle is a read operation.

Table 8-5: P3 Functions

6	WR_L	O	Y	Write strobe. Indication from the microcontroller that the current bus cycle is a write operation.
5	Reserved	-	N	Reserved for future use.
4	Reserved	-	N	Reserved for future use.
3	INT1_L	I	Y	Interrupt 1. Connected to the SCSI bus reset signal RST_L.
2	INT0_L	I	Y	Interrupt 0. Connected to the 53C80S* SCSI chip interrupt.
1	Reserved	-	N	Reserved for future use.
0	Reserved	-	N	Reserved for future use.

Notes: † "Fixed" indicates whether the function/pin is defined by the microcontroller pinout (fixed) or is implementation-specific (not fixed).

8.7   Signal Descriptions

This section defines the function of signal pins on the backplane connector interfaces.

8.7.1   Power Good Signal

This is an input signal from the OCPRF100 midplane. When asserted high, this signal signifies that the power supplies have their PWR_GOOD asserted meaning that power has been applied and not faulted. The PWR_GOOD signal and signal from an onboard Dallas DS1233* reset controller are ORed to keep the board in reset. When both signals indicate that power is good, two things happen: 1) the reset signals are negated to the controllers, SCSI target, and other logic; and 2) power is sequentially applied to each SCA drive connector where a drive is present.

8.7.2   CONN_EN_L

This signal enables the programming capability. When this signal is low, the two microcontrollers are held in reset, and the JTAG mode pin is gated through to the TMS input on the PLDs. When this signal is high, the microcontroller reset is controlled via normal means and the TMS input to the PLDs is held high, which keeps the JTAG interface in an idle state.

8.7.3   CONN_SDI

This is the serial data input stream into the TDI input of the first device on the JTAG chain.

8.7.4   CONN_SDO

This is the serial data output stream from the TDO output of the last device on the JTAG chain.

8.7.5   CONN_MODE

This becomes the TMS input on the JTAG ports of all the PLDs. TMS is a mode select pin which controls the function of the JTAG port. If the enable signal is high (i.e., disabled), the mode signal is degated from the TMS pin, and TMS is held high, which keeps the JTAG port in an idle state.

8.7.6   CONN_SCLK

This is connected to the TCK clock input on the JTAG port of all the PLDs.

8.8   Electrical, Mechanical Specifications

This section specifies the operational parameters and physical characteristics for the backplane.

8.8.1   Connectors

This section defines all the major connectors on the backplane. All the connectors on the backplane are keyed.

8.8.1.1   Connector Specifications

Table 8-6: Connector Specifications shows the quantity, manufacturer, and Intel part number for connectors on the backplane. Refer to manufacturers' documentation for more information on connector mechanical specifications.

Table 8-6: Connector Specifications

Item	Quantity	Manufacturers and Part Number	Description
1	2	AMP* (787535-1)	80 pin right angle SCA-2 connector.
2	1	BERG* (73957-1002)	240 pin recp right angle 5X48.
3	1	FOXCONN* (HL03177-P4)	34 pin (2x17) BMC connector KY5.
4	2	Molex* (15-24-4342)	4 pin power connector.
5	1	Molex (87256-4043)	40 pin IDE cable.
6	1	FOXCONN (HL07256-D6)	50 pin SE SCSI connector.

8.8.1.2   SCSI SCA-2 Drive Connector

An SCA-2 connector is used on the primary side of the board. The pinout is the same as SCA-1. Connector pin assignment is for the current draft *Small Form Factor-8046 Rev. 1.1* document.
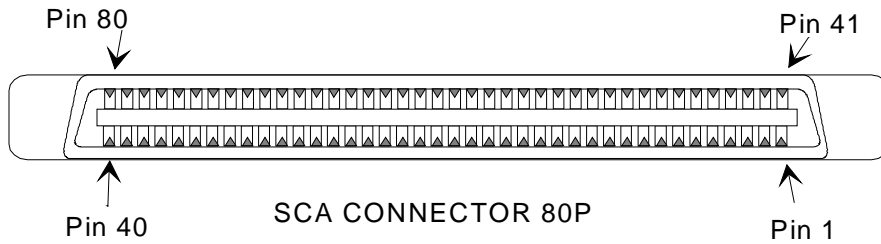
Figure 8-5: SCA-2 Connector 80P

Table 8-7: SCA-2 Connector

80-pin connector contact and signal name			Cable conductor numbers are not applicable	80-pin connector contact and signal name		
1	12V Charge	(L)		(L)	12V Ground	41
2	12V	(S)		(L)	12V Ground	42
3	12V	(S)		(L)	12V Ground	43
4	12V	(S)		(S)	Mated 1	44
5	Reserved/ESI-1	(S)		(L)	-EFW	45
6	Reserved/ESI-2	(S)		(L)	DIFFSNS	46
7	-DB(11)	(S)		(S)	+DB(11)	47
8	-DB(10)	(S)		(S)	+DB(10)	48
9	-DB(9)	(S)		(S)	+DB(9)	49
10	-DB(8)	(S)		(S)	+DB(8)	50
11	-I/O	(S)		(S)	+I/O	51
12	-REQ	(S)		(S)	+REQ	52
13	-C/D	(S)		(S)	+C/D	53
14	-SEL	(S)		(S)	+SEL	54
15	-MSG	(S)		(S)	+MSG	55
16	-RST	(S)		(S)	+RST	56
17	-ACK	(S)		(S)	+ACK	57
18	-BSY	(S)		(S)	+BSY	58
19	-ATN	(S)		(S)	+ATN	59

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Table 8-7: SCA-2 Connector

20	-DB(P)	(S)		(S)	+DB(P)	60
21	-DB(7)	(S)		(S)	+DB(7)	61
22	-DB(6)	(S)		(S)	+DB(6)	62
23	-DB(5)	(S)		(S)	+DB(5)	63
24	-DB(4)	(S)		(S)	+DB(4)	64
25	-DB(3)	(S)		(S)	+DB(3)	65
26	-DB(2)	(S)		(S)	+DB(2)	66
27	-DB(1)	(S)		(S)	+DB(1)	67
28	-DB(0)	(S)		(S)	+DB(0)	68
29	-DB(P1)	(S)		(S)	+DB(P1)	69
30	-DB(15)	(S)		(S)	+DB(15)	70
31	-DB(14)	(S)		(S)	+DB(14)	71
32	-DB(13)	(S)		(S)	+DB(13)	72
33	-DB(12)	(S)		(S)	+DB(12)	73
34	5V	(S)		(S)	Mated 2	74
35	5V	(S)		(L)	5V Ground	75
36	5V Charge	(L)		(L)	5V Ground	76
37	Spindle Sync	(L)		(L)	Active LED Out	77
38	MTRON	(L)		(L)	DLYD_START	78
39	SCSI ID (0)	(L)		(L)	SCSI ID (1)	79
40	SCSI ID (2)	(L)		(L)	SCSI ID (3)	80

8.8.1.3 Floppy Disk Port Connection

Table 8-6: Floppy Disk Connector

Pin	Name	Pin	Name
1	GND	2	FD_DENSEL
3	GND	4	n/c
5	Key	6	FD_DRATE0
7	GND	8	FD_INDEX_L

Table 8-6: Floppy Disk Connector

9	GND	10	FD_MTR0_L
11	GND	12	FD_DR1_L
13	GND	14	FD_DR0_L
15	GND	16	FD_MTR1_L
17	FD_MSEN1	18	FD_DIR_L
19	GND	20	FD_STEP_L
21	GND	22	FD_WDATA_L
23	GND	24	FD_WGATE_L
25	GND	26	FD_TRK0_L
27	FD_MSEN0	28	FD_WPROT_L
29	GND	30	FD_RDATA_L
31	GND	32	FD_HDSEL_L
33	GND	34	FD_DSKCHG_L

8.8.1.4 BERG* 240-pin Right Angle 5 X 48 Connector

Table 8-8: BERG 240-Pin Right Angle 5 X 48 Connector Pinout*

	ROW				
Col-umn	A	B	C	D	E
1	RESET(1)	GND	DD8 (4)	GND	FD_DSKCHG_L
2	DD7 (3)	GND	DD9 (6)	GND	FD_HDSEL_L
3	DD6 (5)	GND	DD10 (8)	GND	FD_RDATA_L
4	DD5 (7)	GND	DD11 (10)	GND	FD_WPROT_L
5	DD4 (9)	GND	DD12 (12)	GND	FD_MSEN0
6	DD3 (11)	GND	DD13 (14)	GND	FD_TRK0_L
7	DD2 (13)	GND	DD14 (16)	GND	FD_WGATE_L
8	DD1 (15)	GND	DD15 (18)	GND	FD_WDATA_L

Table 8-8: BERG* 240-Pin Right Angle 5 X 48 Connector Pinout

9	DD0 (17)	GND	GND	GND	FD_STEP_L
10	GND	GND	DIOW (23)	GND	FD_DIR_L
11	DMARQ (21)	GND	CSEL (28)	GND	FD_MSEN1
12	GND	GND	DIOR (25)	GND	FD_MTR1_L
13	IORDY (27)	GND	GND	GND	FD_DR0_L
14	DMACK (29)	GND	RESERVED (32)	GND	FD_DR1_L
15	GND	GND	PDIAG (34)	GND	FD_MTR0_L
16	INTRQ (31)	GND	DA2 (36)	GND	FD_INDEX_L
17	DA1 (33)	GND	CS0 (37)	GND	FD_DRATE0
18	DASP (39)	GND	DA0 (35)	GND	KEY
19	GND	GND	CS1 (38)	GND	N/C
20	GND	GND	GND	GND	FD_DENSEL
21	GND	GND	GND	GND	Reserved
22	GND	GND	S68 (-DB 11)	GND	Reserved
23	GND	GND	S34 (+DB 11)	GND	Reserved
24	GND	GND	S65 (-DB8)	S32 (+DB 9)	S67 (-DB 10)
25	+12v	+12v	S31 (+DB 8)	S66 (-DB 9)	S33 (+DB 10)
26	+12v	+12v	S62 (-C/D)	S29 (+REQ)	S64 (-I/O)
27	+12v	+12v	S28 (+C/D)	S63 (-REQ)	S30 (+I/O)
28	+12v	+12v	S59 (-RST)	S26 (+MSG)	S61 (-SEL)
29	+12v	+12v	S25 (+RST)	S60 (-MSG)	S27 (+SEL)
30	+12v	+12v	S56	S23 (+BSY)	S58 (-ACK)
31	+12v	+12v	S22	S57 (-BSY)	S24 (+ACK)
32	+12v	+12v	S53 (RESERVED)	S20	S55 (-ATN)
33	+12v	+12v	S19 (RESERVED)	S54	S21 (+ATN)
34	+12v	+12v	S50	S17 (TERMPWR)	S52 (TERMPWR)
35	+12v	+12v	S16 (DIFFSENS)	S51 (TERMPWR)	S18 (TERMPWR)
36	+12v	+12v	S47 (-DB 7)	S14 (+DB P)	S49
37	+5v	+5v	S13 (+DB 7)	S48 (-DB P)	S15
38	+5v	+5v	S44 (-DB 4)	S11 (+DB5)	S46 (-DB 6)
39	+5v	+5v	S10 (+DB 4)	S45 (-DB 5)	S12 (+DB 6)
40	+5v	+5v	S41 (-DB 1)	S8 (+DB 2)	S43 (-DB 3)

Table 8-8: BERG* 240-Pin Right Angle 5 X 48 Connector Pinout

41	+5v	+5v	S7 (+DB 1)	S42 (-DB 2)	S9 (+DB 3)
42	+5v	+5v	S38 (-DB 15)	S5 (+DB P1)	S40 (-DB 0)
43	+5v	+5v	S4 (+DB 15)	S39 (-DB P1)	S6 (+DB 0)
44	+5v	+5v	S35 (-DB 12)	S2 (+DB 13)	S37 (-DB 14)
45	+5v	+5v	S1 (+DB 12)	S36 (-DB 13)	S3 (+DB 14)
46	+5v	+5v	GND	GND	GND
47	+5v	+5v	GND	SDA	Reserved
48	+5v	+5v	GND	PWR_GOOD	SCL

8.8.1.5   IDE Connector

Table 8-9: IDE Connector

Pin	Signal	Pin	Signal
1	RSTDRV	2	GROUND
3	DD7	4	DD8
5	DD6	6	DD9
7	DD5	8	DD10
9	DD4	10	DD1
11	DD3	12	DD12
13	DD2	14	DD13
15	DD1	16	DD14
17	DD0	18	DD15
19	GROUND	20	KEY PIN
21	DRQ	22	GROUND
23	DIOW	24	GROUND
25	DIOR	26	GROUND
27	IORDY	28	CSEL
29	DACK	30	GROUND
31	IRQ	32	No Connection
33	DA1	34	No Connection

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Table 8-9: IDE Connector

35	DA0	36	DA2
37	CS1P_L	38	DS3P_L
39	DHACT_L	40	GROUND

8.8.1.6 Power Supply Connectors

Table 8-10: Power Supply Connectors

Pin #	Signal:
1	VCC12
2	GND
3	GND
4	VCC5

9. Peripheral Bay Board (Chassis Side)

This chapter describes the design of the peripheral bay board (chassis side). This board, used in the OCPRF100 MP server system, is attached to the OCPRF100 MP server system chassis and provides power and signal distribution to the peripheral bay backplane and other system peripheral devices.

Features

The OCPRF100 MP server system peripheral bay board has the following features:

- Provides an interface which allows plugging of the peripheral bay into the system.
- Distributes power and signal connections from the midplane and I/O board to the floppy, IDE CD-ROM, and the peripheral bay backplane.
- Provides a common interface for an integrator's custom peripheral bay solutions.

9.1   Introduction

The peripheral bay board (chassis side) provides power and signal interconnection from the midplane and I/O boards to the peripheral devices and the peripheral bay backplane. This board allows the single point connection of all power and signals required by the peripheral bay backplane. The peripheral bay board (chassis side) contains no active components. Also, it does not provide or contain any field replaceable unit (FRU) information.

9.2   Mechanical Description

The blind mate is the junction of the peripheral bay board (chassis side) with the peripheral bay backplane. The peripheral bay backplane meets the peripheral bay board (chassis side) at a 90-degree angle.

The blind mate consists of one 240-pin connector in between two long guide pins.

9.2.1   Board Layout

Figure 9-1: Peripheral Bay Board (Chassis Side) Layout illustrates the layout of the peripheral bay board (chassis side) with the connectors.

Figure 9-2 shows the printed circuit board dimensions, mounting holes, and connector placements.
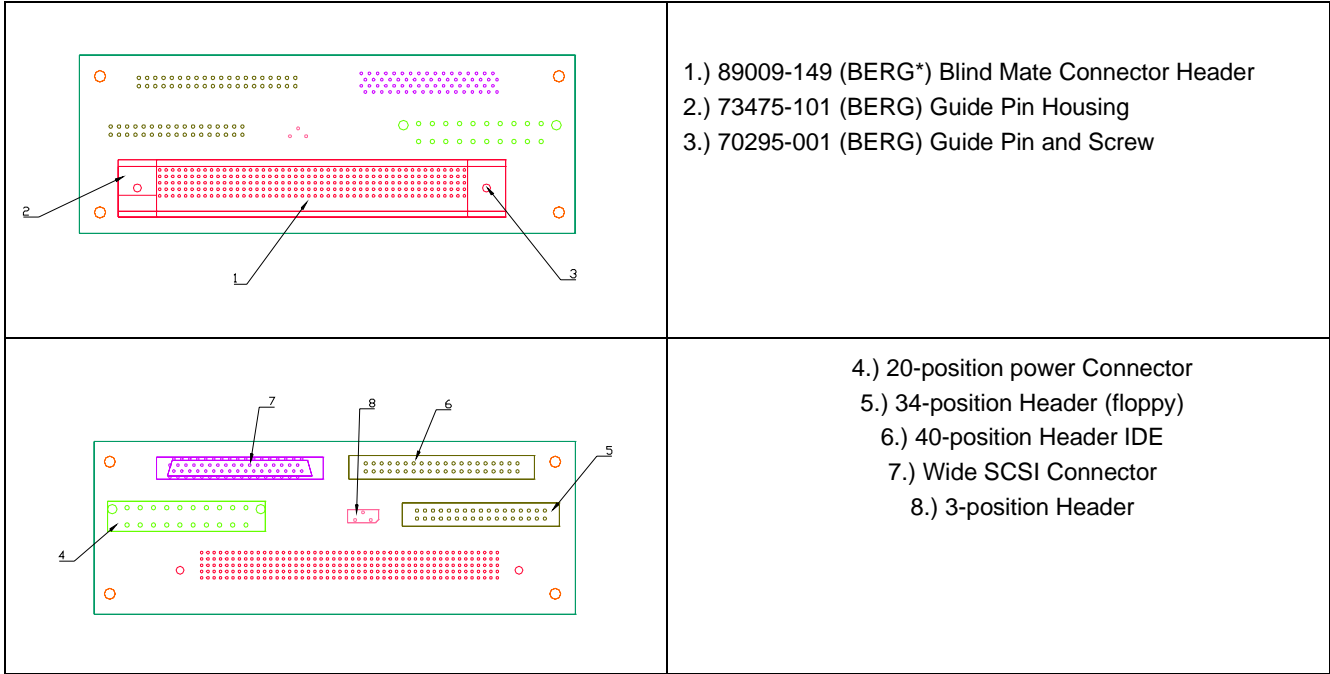
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	1.) 89009-149 (BERG*) Blind Mate Connector Header 2.) 73475-101 (BERG) Guide Pin Housing 3.) 70295-001 (BERG) Guide Pin and Screw
	4.) 20-position power Connector 5.) 34-position Header (floppy) 6.) 40-position Header IDE 7.) Wide SCSI Connector 8.) 3-position Header

Figure 9-1: Peripheral Bay Board (Chassis Side) Layout

g
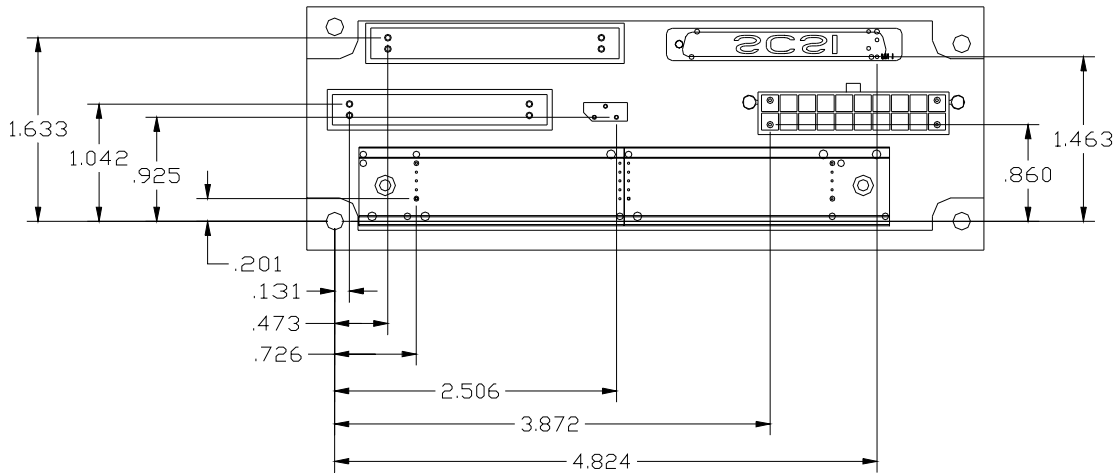
Figure 9-2: Peripheral Bay Board (Chassis Side) Connector Layoui

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10. Front Panel

This chapter describes the design and external interface of the OCPRF100 MP server system front panel. The front panel provides a user interface to the OCPRF100 MP server system via push buttons, indicator LEDs, an LCD panel, and a speaker. It also provides an interface to external systems via the ICMB. All of the front panel functions are controlled by a Philips* 80C652 microcontroller. LEDs used to indicate individual fan failure and a dual speed fan converter that controls the system fans are located on the front panel. System fan tachometer inputs are monitored by the front panel.

Features

- Philips 80C652* microcontroller

- Power, reset, and NMI push buttons

- Fan speed control, monitoring, and individual fan fail indication

- Power-off and reset security

- Power, power fail, hard drive fail, and fan fail indicator LEDs

- LCD panel, which provides boot status and other information

- Concurrent ICMB and COM2 EMP interface

- Speaker

- Operation from standby power

- Full authority power management

10.1 Introduction

This section provides an overview of the OCPRF100 MP server system front panel. It also discusses the primary components and their relationships, and provides diagrams of the physical board layout.

10.1.1 Board Overview

The OCPRF100 MP server system front panel provides a simple user interface to the OCPRF100 MP server system. Push buttons on the front panel allow for power-up and reset as well as NMI assertion. LEDs indicate when the system is powered on and when there has been a power supply failure, hard drive failure, fan or other system cooling failure. The LCD panel provides information about the system, including boot status, available number of processors, and other server management information.

The front panel also allows other systems to communicate with the server, even while power is down, via an ICMB. The ICMB is an extension of the internal IPMB. Although the control circuitry for ICMB is present on the front panel, the ICMB user interface connectors are located at the rear of the chassis.

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All of the front panel's functions are controlled by a Philips 80C652 microcontroller and are available at all times when AC power is available. The connection from the front panel to the rest of the OCPRF100 MP server system is via the 80-pin connector to the OCPRF100 Profusion carrier. All six system fans plug into the OCPRF100 MP server system front panel. Circuitry located on the front panel controls the fan speed, monitors individual fan tachometer signals, and indicates (via LEDs) the failure of an individual fan in the system.
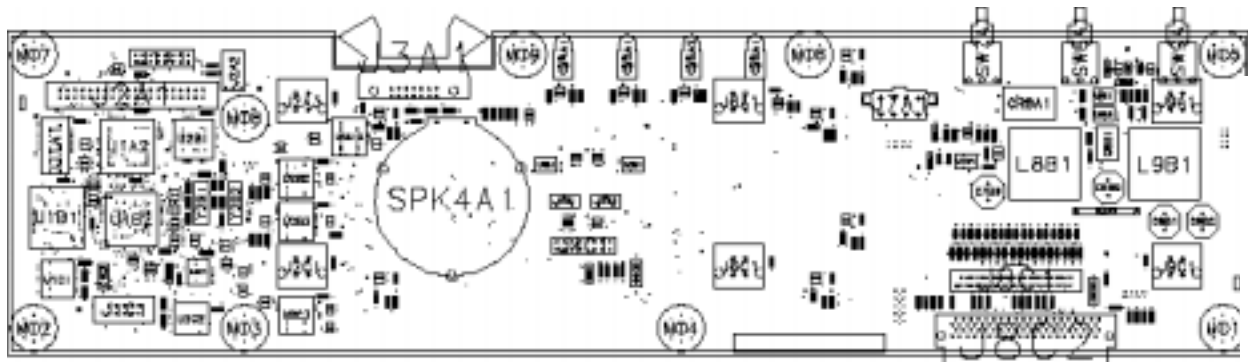

Figure 10-1: OCPRF100 MP Server System Front Panel Layout

10.2 Functional Description

This section provides a functional description of the front panel including the microcontroller, push buttons, indicator LEDs, LCD panel, ICMB, and RS-232 extension.

10.2.1   Microcontroller

All of the "intelligent" functions on the front panel are implemented with a Philips 80C652 microcontroller (also referred to in this document as the FPC). The FPC has 32KB of RAM, 7.5KB of which is accessible; and, 64KB of flash, 56KB of which is accessible. The flash contains all of the firmware the front panel needs, while the RAM is used to store the stack and local variables.

The microcontroller is always active as long as AC power is present. This power is also known as 5 V standby power, standby power, or always-alive power. The microcontroller records the current power state (on or off) in its nonvolatile memory (NVM); in the event of an AC power failure, the FPC can return the system's power status to the state it was in prior to the power failure.

The microcontroller constantly monitors the switches, the state of the power supplies (via its private I^2C bus, I2C_FPC_Sxx), and the ICMB, which is described below in further detail. While the system is powered on, the front panel also monitors the IPMB and responds to IPMB messages.

10.2.2   Memory Maps

This section contains a device maps subsection and an I/O memory maps subsection.

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10.2.2.1   Device Maps

Table 10-1: Device Maps

Function	Address Range	Access	Width
Output Latch #1	FFF0 - FFFF	Write (Read RAM Shadow)	Byte
Output Latch #0	FFE0 - FFEF	Write (Read RAM Shadow)	Byte
RAM, Output Latch Shadow	FF00 - FFFF	Execute, Read, Write (Shadows Output Latches)	Byte
Input Latch #1	FFD0 - FFDF	Read	Byte
Input Latch #0	FFC0 - FFCF	Read	Byte
PLD	FE00 - FFFF	Read, Write	Byte
RAM # 0	E000 - FDFF	Execute, Read, Write	Byte
FLASH, OPS	1000 - DFFF	Execute, Read, Write	Byte
FLASH, BOOT	0000 - 0FFF	Execute, Read	Byte

10.2.2.2   I/O Memory Maps

Table 10-2: I/O Signals and Devices provides a cross reference between the I/O signals and the individual devices. These can be referenced against the device map section to resolve the absolute address.

Table 10-2: I/O Signals and Devices

Topic	Signal	Device	Address	Access	Offset	Bit
Not Applicable	Not Applicable (Muxed Address/Data BUS)	Micro Port 0	-	-	-	0 to 7
LCD	LCD_RW	Micro Port 1	-	RW	-	0
LCD	LCD_EN	Micro Port 1	-	RW	-	1
LCD	LCD_RS	Micro Port 1	-	RW	-	2
Miscellaneous	RESET_OUTPUTS_L	Micro Port 1	-	RW	-	3

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Table 10-2: I/O Signals and Devices

ICMB/COM2	COM2_TO_SIO_EN	Micro Port 1	-	RW	-	4
ICMB/COM2	COM2_TO_FP_EN_L	Micro Port 1	-	RW	-	5
I^{2}C Interfaces	I2C_BACKUP_SCL	Micro Port 1	-	RW	-	6
I^{2}C Interfaces	I2C_BACKUP_SDA	Micro Port 1	-	RW	-	7
Not Applicable	Not Applicable (Upper Address Bus)	Micro Port 2	-	-	-	0 to 7
ICMB/COM2	MICRO_RXD	Micro Port 3	-	-	-	0
ICMB/COM2	MICRO_TXD	Micro Port 3	-	-	-	1
System Power	PWR_INTR_L	Micro Port 3	-	R	-	2
ICMB/COM2	MICRO_RXD_INTR_L	Micro Port 3	-	R	-	3
I^{2}C Interfaces	I2C_FPC_SCL	Micro Port 3	-	RW	-	4
I^{2}C Interfaces	I2C_FPC_SDA	Micro Port 3	-	RW	-	5
Processor	MICRO_WR_L	Micro Port 3	-	W	-	6
Processor	MICRO_RD_L	Micro Port 3	-	W	-	7
Reserved	Reserved	Input Latch #0	FFC0	R	-	0
Miscellaneous	SECURE_MODE_BMC	Input Latch #0	FFC0	R	-	1
ICMB/COM2	RI_TTL_FP	Input Latch #0	FFC0	R	-	2
Reserved	Reserved	Input Latch #0	FFC0	R	-	3
Reserved	Reserved	Input Latch #0	FFC0	R	-	4
System Power	PS_PWR_ON (input)	Input Latch #0	FFC0	R	-	5
ICMB/COM2	DCD_TTL_FP	Input Latch #0	FFC0	R	-	6
Reserved	Reserved	Input Latch #0	FFC0	R	-	7
Reserved	Reserved	Input Latch #1	FFD0	R	-	0
Fan Control	FAN_TACH1	Input Latch #1	FFD0	R	-	1
Fan Control	FAN_TACH2	Input Latch #1	FFD0	R	-	2
Fan Control	FAN_TACH3	Input Latch #1	FFD0	R	-	3
Fan Control	FAN_TACH4	Input Latch #1	FFD0	R	-	4
Fan Control	FAN_TACH5	Input Latch #1	FFD0	R	-	5
Fan Control	FAN_TACH6	Input Latch #1	FFD0	R	-	6
Reserved	Reserved	Input Latch #1	FFD0	R	-	7

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Table 10-2: I/O Signals and Devices

LCD	DB4	Output Latch # 0	FFE0	RW	-	0
LCD	DB5	Output Latch # 0	FFE0	RW	-	1
LCD	DB6	Output Latch # 0	FFE0	RW	-	2
LCD	DB7	Output Latch # 0	FFE0	RW	-	3
LED	POWER_FAIL_LED_CMD	Output Latch # 0	FFE0	RW	-	4
LED	DRIVE_FAIL_LED_CMD	Output Latch # 0	FFE0	RW	-	5
System Power	POWER_GOOD_LED_CMD	Output Latch # 0	FFE0	RW	-	6
Reset	HARD_RESET	Output Latch # 0	FFE0	RW	-	7
Fan Control	FAN_LED_CMD_1	Output Latch #1	FFF0	RW	-	0
Fan Control	FAN_LED_CMD_2	Output Latch #1	FFF0	RW	-	1
Fan Control	FAN_LED_CMD_3	Output Latch #1	FFF0	RW	-	2
Fan Control	FAN_LED_CMD_4	Output Latch #1	FFF0	RW	-	3
Fan Control	FAN_LED_CMD_5	Output Latch #1	FFF0	RW	-	4
Fan Control	FAN_LED_CMD_6	Output Latch #1	FFF0	RW	-	5
Reserved	Reserved	Output Latch #1	FFF0	RW	-	6
Reserved	Reserved	Output Latch #1	FFF0	RW	-	7
COM2	UART_ADDR	PLD	FFB0	R	27	0
Memory	FW_BOOT_PGM_EN	PLD	FFA0	R	26	0
Reset	RST_SWT_LATCH	PLD	FF90	R	25	0
System Power	PWR_CNTRL_RTC_L	PLD	FF80	R	24	0
Memory	FRC_UPDATE_L (was SPARE_JUMPER)	PLD	FF70	R	23	0
Power	POWER_CNTRL_SFC_L	PLD	FF60	R	22	0
Power	POWER_GOOD	PLD	FF50	R	21	0
COM2	UART_RESET	PLD	FF30	R	19	0
Memory	BOOT_PGM_EN_LATCH	PLD	FF20	RW	18	0
Reset	SYS_RESET_STATE_LATCH	PLD	FF10	RW	17	0
Power	PS_PWR_ON (output)	PLD	FF00	RW	16	0
FP_TO_PIIX4_ PWRBTN	ACPI	PLD	FEF0	RW	15	0
COM2/ICMB	ICMB_ACTIVITY_LATCH	PLD	FEE0	RW	14	0

Table 10-2: I/O Signals and Devices

COM2/ICMB	COM2_ACTIVITY_LATCH	PLD	FED0	RW	13	0
Memory	I2C_CEL_CONNECT_FPC	PLD	FEC0	RW	12	0
Memory	I2C_CEL_CONNECT_BMC	PLD	FEB0	RW	11	0
System Power	PWR_GOOD_LATCH	PLD	FEA0	RW	10	0
COM2/ICMB	ICMB_EN_LATCH	PLD	FE90	RW	9	0
COM2/ICMB	FORCE_RXD_ICMB_LATCH	PLD	FE80	RW	8	0
COM2/ICMB	FORCE_RXD_COM2_LATCH	PLD	FE70	RW	7	0
Reserved	Reserved	PLD	FE60	RW	6	0
SPEAKER	SPEAKER_LATCH	PLD	FE50	RW	5	0
System Power	PWR_RTC_TRANS_LATCH	PLD	FE40	RW	4	0
System Power	PWR_SFC_LATCH	PLD	FE30	RW	3	0
System Power	PWR_SWT_LATCH	PLD	FE20	RW	2	0
System Power	PWR_INTR_LATCH_L	PLD	FE10	RW	1	0
Memory Map	UART_INT	PLD	FE00	RW	0	0

NOTE: The programmable logic device (PLD) addresses are calculated using offset term and the following equation:
ADDRESS = PLD_BASE + OFFSET * 80H

10.2.3   Memory

10.2.3.1   Program Memory, Flash

The front panel contains an ATMEL 29C512* for storing program memory and initialized variables. This device is nominally 64KB by 8 but is expandable to 128KB by 8. In order to use the 128KB by 8 devices, the memory model would need to be changed to provide enough address space, or a paging scheme would need to be incorporated.

FRU information is not stored in this device, but, rather, is stored in the serial EEPROM.

10.2.3.2   RAM

There is 32KB by 8 of RAM on the FPC. Note that only approximately 7.5KB of the RAM is accessible according to the memory map.

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10.2.3.3   UART

A universal asynchronous receiver/transmitter (UART) is memory mapped to the microcontroller's bus to allow concurrent operation of the ICMB and EMP ports. The UART is used for the EMP interface.

10.2.3.4   Serial EEPROM/Temperature Sensor

The serial EEPROM is accessible on the FPC's private I^{2}C bus. A DS1621* temperature sensor is also on the private I^{2}C bus, which is used to sense the ambient temperature outside of the system.

Table 10-3: FRU Device Address

Device	Function	I^{2}C Address
24C02*	Front panel FRU information	A0h, A1h
DS1621*	Temperature sensor to detect ambient temperature	90h, 91h

The 24C02*, when accessed via the I^{2}C bus, provides the following FRU information. The FRU information is read by the Intel® LANDesk® Server Manager or similar management software and is available via the LANDesk Server Manager console.

The 24C02 SEEPROM has 256 bytes of programmable space, which is broken into four areas. Table 10-4: SEEPROM Programming Areas is a list of the areas, a brief description of their purpose, and the space allocated to each area.

Table 10-4: SEEPROM Programming Areas

Area	Size	Description
Common header	8 Bytes	Programming offsets to the other areas below.
Internal use	80 Bytes	This area is reserved for general purpose use by Intel® server management firmware/controllers.
Chassis information	32 Bytes	Contains chassis information.
Board information	56 Bytes	Contains the board FRU information listed in .
Product information	80 Bytes	Available for integrator use.†

†   A utility provided by Intel, called the *FRU & SDR Load Utility,* allows the integrator to program any of the FRU SEEPROM in the chassis.

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Table 10-5: FRU Information lists the board specific FRU information that is programmed into the board information area.

Table 10-5: FRU Information

Board Information			
Information	**Description**	**Example**	**Notes**
Manufacturing date/ time	Time and date of board man- ufacture (value programmed [in hex] is the number of minutes after 0:00 hrs 1/1/ 96).	000f593h (Date/time translation shown below.) f593h = 62867 min. = 43 Days & 947 min. = Feb 12, 1997, 3:47p.m.	2
Manufacturer	Board manufacturer.	Intel	1
Board product name	Board name/description.	OCPRF100 server system front panel	1
Board serial number	Intel board serial number.	N42385906	2
Board part number	Intel board part number.	703106-002	2

Notes: 1. Actual value programmed into the board.

2. Example value. Actual value varies with each board and/or fab revision.

Table 10-6: I/O Signals and Devices SEEPROM Byte Map identifies the exact purpose for which bytes are allocated within the 24C02 SEEPROM. This information is useful for those who will be accessing the hardware directly (i.e., BIOS and server management software developers).

Table 10-6: I/O Signals and Devices SEEPROM Byte Map

Address	Length	Description	Default Value
0x00	1	Common header format version	0x01
0x01	1	Internal use area offset (8-byte multiples)	0x01
0x02	1	Chassis information area offset (8-byte multiples)	0x0B
0x03	1	Board information area offset (8-byte multiples)	0x0F
0x04	1	Product information area offset (8-byte multiples)	0x16
0x05	2	Zero padding	

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Table 10-6: I/O Signals and Devices SEEPROM Byte Map

0x07	1	Common header checksum	0xCE
0x08	80	Internal use area	
0x58	1	Chassis information area format version	0x01
0x59	1	Chassis information area length (8-byte multiples)	0x04
0x5A	1	Chassis type	0x11
0x5B	1	Chassis part number type/length byte	0xCA
0x5C	10	Chassis part number	
0x66	1	Chassis serial number type/length byte	0xC9
0x67	9	Chassis serial number	
0x70	1	No more fields flag	0xC1
0x71	6	Zero padding	
0x77	1	Chassis information area checksum	0X2C
0x78	1	Board information area format version	0x01
0x79	1	Board Information area length (8-byte multiples)	0x0A
0x7A	1	Unicode country base	0x00
0x7B	3	Manufacturer date/time	
0x7E	1	Board manufacturer type/length byte	0xC5
0x7F	5	Board manufacturer (ASCII)	Intel
0x84	1	Product name type/length byte	0xDC
0x85	17	Product name	OCPRF100 front panel
0x96	1	Board serial number type/length byte	0xC9
0x97	9	Board serial number	
0xA0	1	Board part number type/length byte	0xCA
0xA1	10	Board part number	
0xAB	1	No more fields flag	0xC1
0xAC	3	Zero padding	
0xAF	1	Board information area checksum	0x7A
0xB0	80	Product information area	

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10.2.3.5   System Event Log (SEL)

The system event log (SEL) serial EEPROM (which resides on the OCPROF100 I/O carrier on the BMC's private I^{2}C bus) can be accessed by the front panel's private bus under certain conditions. This feature has been added to allow access when main power is down.

When the I2C_CEL_CONNECT_FPC signal is asserted, the serial EEPROM is connected electrically to the FPC's private I^{2}C bus and is powered off of the 5 V standby supply.

When the I2C_CEL_CONNECT_BMC signal is asserted, the serial EEPROM is connected electrically to the I/O's private I^{2}C bus and is powered off of the +3.3 V supply.

When both the I2C_CEL_CONNECT_FPC and the I2C_CEL_CONNECT_BMC signals are asserted, the 5 V standby, +5 V, and the +3.3 V supplies are connected together. Firmware provisions prevent this scenario from happening.

An additional consideration is the BMC on power-up. A firmware mechanism is required to tell the BMC when this device is available.

It is required that the BMC's I^{2}C bus be static between 0 and 20 ms after the rising edge of the I2C_CEL_CONNECT_BMC signal.

Upon power-up, the I2C_CEL_CONNECT_BMC signal is asserted and the I2C_CEL_CONNECT_FPC is deasserted.

10.2.4   Front Panel Indicator LEDs

The POWER_FAIL LED is under the control of the FPC. When the FPC asserts (high) the POWER_FAIL_LED_CMD signal, the LED becomes illuminated. This LED is off when deasserted and during an FPC reset. This LED is powered off of 5 V standby so it can be illuminated even when +5 V is invalid.

The DRIVE_FAIL_LED is an indication of hard drive failure. It is illuminated when the DRIVE_FAIL_LED_CMD signal is asserted (high). It is off when this signal is deasserted (low) and during an FPC reset.

The POWER_GOOD_LED is an indication of good DC power in the system. It is illuminated when the POWER_GOOD_LED_CMD signal is asserted (high). It is off when this signal is deasserted (low) and during an FPC reset.

The FAN_FAIL_LED is under the control of the BMC. The FPC queries the BMC for system fan fail status. It illuminates when the FAN_FAILED_L signal is asserted (low) from the BMC. It is an indication of system cooling failure. Additionally, there is an LED associated with each fan. These LEDs are located adjacent to each individual fan to provide an indication of which of the six system fans has failed. These LEDs are driven by the FPC.

10.2.5   Front Panel LCD

The front panel LCD is a Stanley GMD1620A*. The LCD and the LCD's LED backlighting unit are powered off of the main +5 V. Therefore, this capability is only available when the +5 V power is available.

In order to avoid loss of 5 V standby power and LCD latch-up, the firmware must comply with the following. When main power is OFF, all signals driving the LCD should be disabled or driven low. These include the D0 through D3, RW, EN, and RS signals. Also, when main power is removed the LCD signals should be brought to this safe state within 200 μs.

10.2.6   System Power

10.2.6.1   Power Supply Monitoring

Each of the three supplies has three signals that can be monitored. These are the PS_PRES, PS_FAULT and the PRED_FAIL signals. These are available via the private I^{2}C bus.

10.2.6.2   Power Interrupt Routing

There are three hardware signals that can initiate power cycling. They are the real time clock (RTC) (PWR_CNTRL_RTC_L), the Intel$^®$ SMM card (PWR_CNTRL_SFC_L), and main power going out (PWR_GOOD). These are accessed via the PWR_RTC_TRANS_LATCH, the PWR_SFC_LATCH, and the PWR_GOOD_LATCH signals per the memory map. Upon assertion, each of these signals is individually latched in the programmable logic device (PLD). The asserted state remains latched even if the signal becomes deasserted. The asserted state remains latched until the latch is read by the microcontroller. When read by the microcontroller, the latch becomes cleared.

The PWR_CNTRL_RTC_L transition latch (PWR_RTC_TRANS_LATCH) becomes set (asserted) on either transition of the PWR_CNTRL_RTC_L signal. When set, the latch remains set until read by the FPC. Note that by reading the PWR_RTC_TRANS_LATCH latch, it is not possible to obtain the absolute state of the PWR_CNTRL_RTC_L signal. Therefore, the PWR_CNTRL_RTC_L signal can also be read by the FPC.

The PWR_CNTRL_SFC_L latch (PWR_SFC_LATCH) becomes set (asserted) on a high to low transition of the PWR_CNTRL_SFC_L signal. When set, the latch remains set until read by the FPC. When the latch is read, it becomes cleared and remains cleared until the next high to low transition of the PWR_CNTRL_SFC_L signal. The state of the PWR_CNTRL_SFC_L signal can also be read directly.

The PWR_GOOD_LATCH becomes set (asserted) when the PWR_GOOD signal has a high to low transition. This occurs when main power goes bad. Once read, the latch is cleared and will not be set until the next high to low transition. The state of the POWER_GOOD signal can also be read directly. Each of these three latches is fed into a fourth latch (PWR_INTR_LATCH_L), which drives the PWR_INTR_L signal. The PWR_INTR_L signal drives the FPC's INT0 input. This latch is asserted (low) if **any** of the power cycle signals become asserted (high). This latch signal is deasserted (high) whenever it is read, as long as all three inputs are also deasserted.

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All four latches may be read by the microcontroller. Reading by the microcontroller causes the latch to be deasserted (assuming that the asserting signal is also deasserted).

With this interrupting scheme, it is suggested that the FPC use the power interrupt in level mode, not edge mode. This is because a reassertion of an interrupting source at the wrong time could prevent the interrupt pin from being toggled.

10.2.6.3   Front Panel Power Switch

The paramount design concern is the capture of an asserted switch with a microcontroller/firmware design that experiences starved threads, specifically the thread that polls the power switch. (In normal real time control, a starved thread is an indication of abnormal operation that would cause a fatal error and abortion of microcontroller operation.) This is addressed by latching the asserted state in hardware via the PWR_SWT_LATCH. This latch is set whenever the switch is asserted. Whenever the switch is read, the latch is cleared. Therefore, when the starved thread regains the FPC, it can read the latch. If the switch was asserted after the last polling, the latch reads a one.

10.2.6.4   Hardware Control of Power Supply ON Command

The following describes the hardware control over the PS_PWR_ON (output) signal. The FPC has only marginal control over this signal. The system-power-on command (PS_PWR_ON) is asserted by the FPC via the PS_PWR_ON (output) signal, **as long as** there is not a 240 volt-amp incident.

10.2.6.5   Default Power State

The default power state is OFF. This is the state that the front panel commands for the main power via the PS_PWR_ON (output) signal. During normal operation the firmware must assert the PS_PWR_ON (output) signal to turn on the supplies. This is controlled from the PLD. During a firmware-driven PLD download, the PLD's outputs become tristated. When tristated, the power supplies are commanded on via an external pull-up resistor.

10.2.6.6   Dual Speed Fan Power

The system cooling fans typically operate at low voltage to minimize acoustic noise. Under normal conditions, the fans run at this slower, quieter speed. When a fan failure is sensed, the fan speed is set to high. Also, if the ambient temperature sensor reads 31 degrees or higher, the fan speed will be set to high (there are 2 degrees of hysteresis built into this algorithm, so the ambient temperature must drop to 29 degrees before the fan speed is reduced to low again). The high/low decision is made by the FPC, via the FULL_FAN_SEL_L signal.

The fan voltage is derived via a buck converter from 12 V, and is current limited at 9 A. Maximum current during high speed operation is 5.04 A.

10.2.7   Reset

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10.2.7.1   Resetting the System

The FPC has the capability to reset the entire system (processors, chip sets, etc.) by asserting the HARD_RESET signal. It must be asserted for a minimum of 500 ms. There is no maximum.

10.2.7.2   Reset Inputs

The state of the reset switch can be determined by reading the RST_SWT_LATCH signal within the PLD. If the reset switch has been asserted since the previous reading of this latch, then the latch will be asserted (high). Reading of this latch clears the latch. Therefore, there are no minimum polling requirements to detect an asserted switch. The latch is asynchronously set whenever the switch is pressed and remains set as long as the switch is pressed, whether or not the latch is read by the FPC.

10.2.7.3   Reset Switch During +5 V Power Cycle

While +5 V power is inactive, the RST_SWT_LATCH remains asserted. This is because the reset switch circuitry incorporates a pull-up to main +5 V, and when main power is off, the main +5 V power is at 0 V, making the switch appear asserted. This pull-up is tied to main +5 V to save power on +5 V standby.

The RST_SWT_LATCH might remain asserted up to and including the first read after the PWR_GOOD indicates that main +5 V power is valid. The first valid RST_SWT_LATCH read occurs on the SECOND READ after PWR_GOOD becomes asserted (high).

10.2.7.4   Resetting the FPC

The FPC is reset whenever the VCC_STDBY is invalid and 500 ms (typically) after VCC_STDBY becomes valid. The front panel has development support for a push button reset input. Removing the default RP1A1 and connecting a switch between J1A1 pins 3 and 4 activates this by controlling the PUSH_BTN_RST_L signal.

10.2.7.5   Determining the System Reset State

Signal PROC_RESET _LATCH provides firmware with an indication of the processor reset state. A latch is used because a processor reset assertion may last as short a period of time as 40 ns, and as long as many seconds. Therefore, an assertion of the PROC_RESET_L signal causes the PROC_RESET _LATCH to become set. When the signal is read by the FPC, the latch is cleared (assuming the PROC_RESET_L signal is no longer asserted).

To determine whether an assertion of the PROC_RESET_L signal has occured since the last reset **and** the current state, read the PROC_RESET_LATCH twice. If PROC_RESET_LATCH returns sequential ones, then the processors are currently in reset. If PROC_RESET_LATCH returns one, then zero, the processors have gone through reset since the last time the latch was read, but are not currently in reset. If PROC_RESET_L returns two zeroes, the processors have not gone through reset since the last time the latch was read.

Whenever the front panel goes through a hardware reset this latch is cleared.

10.2.7.6   Development and Test Reset

In development and board testing the PLD and microcontroller can be put into a reset state by asserting the PB_RST_L signal.

10.2.8   Speaker

The front panel contains a speaker that is controlled by either the FPC or the I/O board. The speaker is energized if either source commands the speaker on. The speaker impedance is approximately 8 ohms.

The FPC commands the speaker on by setting the PLD's SPEAKER_LATCH. This latch also can be read. The state of the I/O board's speaker command cannot be read by the FPC.

During reset the SPEAKER_LATCH is set to deasserted (off, low).

10.2.9   Fan Control

There are six fans which plug into the front panel board. Each fan is powered from the VCCFAN supply (see *Section Dual Speed Fan Power, Dual Speed Fan Power*). Each fan also has a tachometer out signal, which is fed into Input Latch #1, to be monitored by the FPC. If a fan is determined to have failed, the FAN_FAILED_L signal turns on the yellow fan failed LED on the front panel. Also, an LED near the fan that has failed is illuminated by the FPC (via Output Latch #1).

10.2.10 ICMB and COM2 Redirection

The ICMB/COM2 redirection circuitry provides a number of capabilities. These capabilities are dealt with individually in the following subsections.

10.2.10.1 Receive Auto Switching

Both the COM2 RXD (received) and the ICMB RXD signals are routed to the front panel and are continuously available, regardless of the state of any other control signals. In certain conditions it is desirable to monitor both signals and to switch to whichever signal goes active first into the FPC's RXD input. This section covers such an auto-switch capability, implemented in the PLD.

The FP PLD supports auto-switching of the first-active incoming RXD signal into the incoming RXD signals. The auto-switch is enabled by deasserting both the FORCE_RXD_ICMB_LATCH and the FORCE_RXD_COM2_LATCH. When these are both deasserted by firmware, the PLD goes into auto-switch mode.

Upon RXD activity, the microcontroller can determine which RXD signal is routed to the micro-controller by reading the states of both FORCE bits within the PLD. Only the FORCE bit corre-sponding to the switched RXD (ICMB or COM2) signal becomes asserted. In no case will both FORCE bits become asserted.

10.2.10.2 Receive Forced Switching

In certain cases it is desirable to force a specific RXD (COM2 or ICMB) into the FPC's RXD input. This section covers this forced switch capability.

To force the ICMB's RXD signal into the FPC's RXD input, assert the FORCE_RXD_ICMB_LATCH and deassert the FORCE_RXD_COM2_LATCH.

To force the COM2's RXD signal into the FPC's RXD input, assert the FORCE_RXD_COM2_LATCH and deassert the FORCE_RXD_ICMB_LATCH.

The following (or equivalent) sequence occurs in firmware. **The deassertion must occur whether or not it had previously been asserted.**

Disable interrupts.

Assert desired FORCE bit.

Deassert undesired FORCE bit.

Enable interrupts.

There is no guarantee that incoming RXD streams will be coherently switched in the hardware. It is probably a good idea to discard any immediate UART receptions after a switch.

10.2.10.3 Receive Interrupt

The microcontroller interrupt number one is programmed in the PLD to be logically the same as the microcontroller's RXD input.

10.2.10.4 Receive Activity Detection

A completely independent circuit monitors activity on the ICMB and COM2 receive inputs. This allows bus activity monitoring regardless of the state of the auto-detect switch. Note that the receive (RXD) inputs from both COM2 and ICMB are always available to the front panel, regardless of the states of the COM2_TO_FP_EN_L and the COM2_TO_SIO_EN signals.

The ICMB_ACTIVITY_LATCH becomes set when the SIN_TTL_ICMB signal becomes asserted (low). This assertion corresponds to receive activity. The latch remains asserted (set) until read by the FPC at which time the latch is cleared. The latch remains cleared until the next activity on this line is detected.

The COM2_ACTIVITY_LATCH becomes set when the SIN_TTL_COM2 signal becomes asserted (low). This assertion corresponds to receive activity. The latch remains asserted (set) until read by the FPC at which time the latch is cleared. The latch remains cleared until the next activity on this line is detected.

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10.2.10.5 ICMB Transmit Control

The FPC's TXD (transmitted) pin drives both the COM2's SOUT_TTL_COM2 signal and the ICMB's SOUT_TTL_ICMB signal. There is no interlock for preventing the FPC from simultaneously transmitting on both ICMB and COM2; in fact, this capability could be desirable.

The FPC drives the ICMB bus with the FPC's TXD output whenever the ICMB_EN_LATCH is asserted (high).

10.2.10.6 COM2 Transmit Control

The COM2 transmit signals are connected to either the FPC or the SMC Super I/O* (SIO) chip depending on the states of the COM2 signals. Note that this discussion is limited solely to the TXD signals since this is the only signal that the FPC can control.

The routing of COM2 to the SMC I/O chip or FPC and the routing of the ICMB to the FPC is controlled by two signals, COM2_TO_FP_EN_L and COM2_TO_SIO_EN. Note that if these two signals are not carefully controlled by firmware, the VCC_BACKUP can be shorted to ground. The VCC_BACKUP is shorted to ground via the SIO's power pins. In this case, the power supplies will cycle the entire system and component damage may occur. **When switching between enabling of these routings, it is important never to enable both these signals at the same time.**

Table 10-7: Allowed Combination of States shows the allowed combination of states.

Table 10-7: Allowed Combination of States

Main Power	COM2_TO_FP_EN_L	COM2_TO_SIO_EN	Result
OFF	Deasserted (1)	Deasserted (0)	COM2 disconnected ICMB available†
ON	Deasserted (1)	Deasserted (0)	COM2 disconnected ICMB available†
OFF	Asserted (0)	Deasserted (0)	COM2 routed to front panel ICMB available†
ON	Asserted (0)	Deasserted (0)	COM2 routed to front panel ICMB available†
ON	Deasserted (1)	Asserted (1)	COM2 connected with SMC* ICMB available†
All Other States			Possible main power cycle Possible component damage

† ICMB available means that if the ICMB_SOUT_EN signal is asserted then the FPC will transmit to the ICMB bus. The data that is transmitted comes from the microcontroller's TXD output pin. Note that this capability is independent of the states of the COM2_TO_SIO_EN and COM2_TO_FPC_EN signals; it depends only on the state of the ICMB_SOUT_EN signal.

To switch between the SMC and FPC connection of COM2, both signals should be deasserted before either signal is asserted.

When main power is off, the COM2_TO_SIO_EN signal should never be asserted.

10.2.10.7 Transmit and SMC/Front Panel Connection Control

The FPC's interrupt 2 input is logically the same signal as the signal connected to the FPC's RXD pin. The description in this section, therefore, applies to both signals.

The FPC's TXD pin drives both the COM2's SOUT_TTL_COM2 signal and the ICMB's SOUT_TTL_ICMB signal.

10.2.10.8 COM2 Data Carrier Detect (DCD) Input Signal

COM2's data carrier detect (DCD) input is availabe as signal name DCD_TTL_FP. This input is available to the firmware at all times, regardless of the states of any ICMB and COM2 control signals. This signal is a direct pass through from the COM2 port. The memory map location is described in *Section Memory Maps Memory Maps*.

10.2.11 Front Panel Push Buttons

The OCPRF100 front panel has three momentary-contact push button switches: power, reset, and NMI. The power and reset switches are easily accessible by the user, whereas the NMI button is accessible only via a "pinhole" protective cover. The power switch controls main system power. If the system is powered off, pressing this button will always turn system power on. However, if the system is on, the microcontroller qualifies this button press with the current security state of the system, and decides whether the system is actually to be powered off.

The power switch is available to the FPC and is described in Section Front Panel Power Switch.

The reset switch is available to the FPC and is described in Section Resetting the FPC.

10.2.11.1 Switch Debounce

Table 10-8: Debounce Characteristics and Requirements describes the debounce characteristics and requirements for all push button switches.

Table 10-8: Debounce Characteristics and Requirements

Event	Mininum (milliseconds)	Typical	Maximum (milliseconds)
Switch Press Ramp (High-Low)	0	20	200
Switch Release Ramp (Low-High)	0	12	150
Required switch cycle duration detection by firmware	50†	20	Infinity

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Table 10-8: Debounce Characteristics and Requirements

Potential Switch Cycle characteristics (Press to Release) [no firmware requirements derived from this row]	0	200	Infinity

† Note that although the keypad press-release cycle may be as short as zero, worst case, the firmware is only required to detect a cycle as short as 50 ms.

10.2.11.2 NMI Switch

The NMI push button is hidden behind the main front panel bezel, except for a small "pinhole" access hole. This is done to prevent inadvertent activation of the NMI switch. The NMI switch is routed directly to the BMC. There is no interface to the FPC.

10.2.12 I^{2}C Interfaces

The FPC interfaces to two I^{2}C buses; the FPC's I^{2}C bus and the global I^{2}C bus. These are described in the following subsections.

10.2.12.1 The FPC Private I^{2}C Bus

The FPC's private I^{2}C bus is used for the FPC to communicate with dumb I^{2}C devices that do not support multimaster mode. These are shown in Figure 10-2: Devices Not Supporting Multimaster Mode.

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**OCPRF100
FPC Private I2C Bus Diagram**
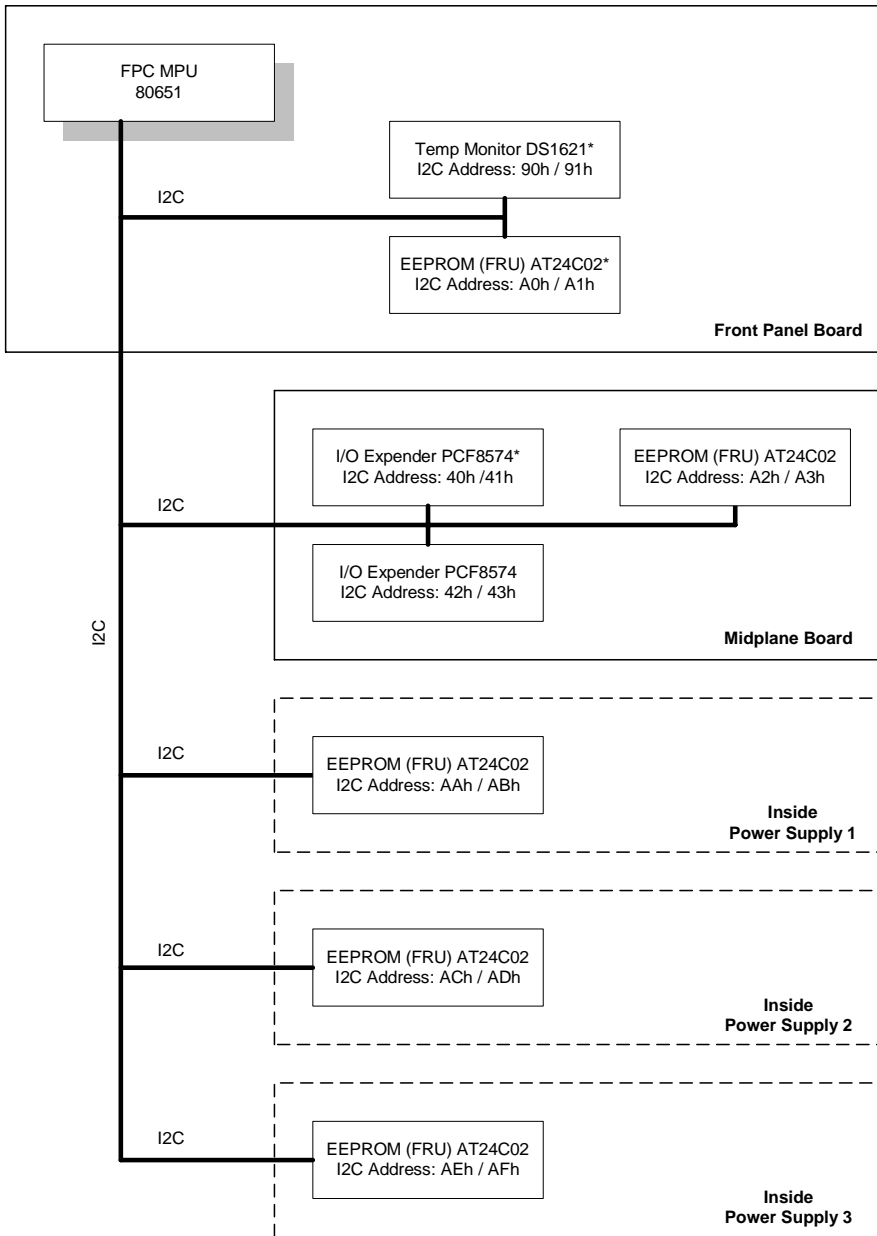
Figure 10-2: Devices Not Supporting Multimaster Mode

10.2.12.2 Global I²C Bus

The global I²C bus is connected automatically to the IPMB whenever power is valid. This bus is used to allow communication between smart I²C devices that operate in multimaster mode. Spe-

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cifically, this bus connects the FPC and BMC. Also, there may be an SMM based device on the bus and a cluster card connector based device.

On the FPC, this bus consists of the I2C_BACKUP_SCL and the I2C_BACKUP_SDA signals.

10.2.12.3 I^{2}C Development Support Jumpers

Development support jumpers on the I^{2}C buses are provided to isolate I^{2}C devices. These jumpers must first be enabled by removing Resistor Pack RP3A4 and RP3A5 and adding all J3 jumpers. Once enabled, specific I^{2}C devices/sections can be isolated by removing the jumpers.

In production, the jumper blocks are not stuffed.

10.2.13 Miscellaneous

10.2.13.1 Signal RESET_OUTPUTS_L

The RESET_OUTPUTS_L signal is used to enable the output latch. Immediately after the microcontroller comes out of a hard reset, this signal goes to the deasserted (high) state. In this state, the output latch is output disabled, but retains any states written to it. The microcontroller initializes the latch with proper values before the RESET_OUTPUTS_L signal is asserted (low).

Appendix A: Glossary

This appendix contains important terms used in the preceding chapters.

Term	Definition
ACPI	Advanced Configuration and Power Interface
AP	Application processor
APIC	Advanced Programmable Interrupt Controller
ASR	Asynchronous system reset
BDA	BIOS data area
BIOS	Basic Input-Output System
BIST	Built-In Self-test
BMC	Baseboard management controller
BSP	Bootstrap processor
Byte	An 8-bit quantity
dB	Decibels
DIB	Data Interface Buffer
DIMM	Dual inline memory module
DMI	Desktop management interface
DOS	Disk operating system
DWORD	Double Word. A 32-bit quantity.
ECC	Error checking and correcting
ECP	Extended capabilities port
EEPROM	Electrically erasable programmable read-only memory
EMI	Electromagnetic interference
EMP	Emergency management port
EPP	Enhanced parallel port
ESCD	Extended system configuration data
ESD	Electrostatic discharge
Flash ROM	EEPROM
FPC	Front panel controller
FRB	Fault resilient booting

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FRU	Field replaceable unit
GB	Gigabyte. 1024 MB
GPNV	General purpose nonvolatile [storage]
GPO	General purpose output
HSC	Hot-swap controller
I/O	Input/Output
I/O APIC	APIC that delivers interrupts from devices to the processors
I^{2}C*	Inter Integrated Circuit bus
ICMB	Intelligent Chassis Management Bus
IDE	Integrated drive electronics
iFLASH	A utility to update Flash EEPROM
IPI	Interprocessor interrupt
IPMB	Intelligent Platform Management Bus
IPMI	Intelligent Platform Management Initiative
IRQ	Interrupt request line
KB	Kilobyte. 1024 bytes
L2	Second-level cache
LCD	Liquid crystal display
LVDS	Low-voltage differential SCSI
MAC	Memory Access Controller
MB	Megabyte. 1024 KB
MIF	Management information format
MPS	Multiprocessor specification
MSR	Model specific register
MTRR	Memory type range register
NMI	Nonmaskable interrupt
OEM	Original equipment manufacturer
OPROM	Option ROM
OS	Operating system
PB64	PCI host bridge with hot-plug controller
PC-100	Collection of specifications for 100-MHz memory modules
PCI	Peripheral component interconnect

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PHP	PCI hot-plug
PIC	Programmable interrupt controller
PID	Programmable interrupt device
PIIX4e	PCI ISA IDE (and USB) accelerator chip from 82440LX chip set
PIRQ	PCI interrupt request line
PMM	POST memory manager
PnP	Plug and Play
POST	Power-On Self Test
Profusion®	Eight processor chip set used in OCPRF100 MP Server System
RAS	Reliability, availability, and serviceability
RPM	Revolutions per minute
SAF-TE	SCSI Accessed Fault-Tolerance Enclosures
SCL	Serial clock
SCSI	Small computer systems interface
SECC	Single edge contact cartridge
SEL	System event log
SELV	Safety extra-low voltage
SMBIOS	System management BIOS
SMBus	Subset of I^2C bus/protocol
SMI	System management interrupt
SMIC	Server management interface controller
SMM	System management mode
SMP	Symmetric multiprocessing
SMRAM	System management RAM
SMS	System management software
SPD	Serial presence detect
SSU	System Setup Utility
UC	Uncacheable
USB	Universal Serial Bus
Vac	Volts of alternating current
Vdc	Volts of direct current
VGA	Video graphics array

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VID	Voltage ID
VRM	Voltage regulator module
WB	Write-back cacheable
Word	A 16-bit quantity
WP	Write protected

Appendix B: References

The following documents further describe the OCPRF100 MP Server System:

- *Saber System External Architecture Specification*, Intel Corporation, OR-1300.

- *OCPRF100 MP Server System BIOS External Architecture Specification*, Revision 2.0, Intel Corporation, OR-1522.

- *System Setup Utility External Product Specification*, Intel Corporation, OR-1510.

- *OCPRF100 MP Server Management External Architecture Specification*, Intel Corporation, OR-1409.

- *OPRF100 Board Set External Product Specification*, Revision 2.0, OR-1542.

Refer to the following documents for additional information:

ACPI
- *Advanced Configuration And Power Interface Specification*, Revision 1.0, 22 December 1996, http://www.teleport.com/~acpi.

- *Errata to the Advanced Configuration and Power Interface Specification*, Revision 1.0, http://www.teleport.com/~acpi.

- *ACPI Implementor's Guide*, v. 0.50, http://www.teleport.com/~acpi.

Boot
- *BIOS Boot Specification*, Version 1.01, http://www.ptltd.com/techs/specs.html.

- *El Torito CD-ROM Boot Specification*, v. 1.0, http://www.ptltd.com/techs/specs.html.

DMI
- *Desktop Management Interface Specification*, Version 2.00, 27 March 1996, Desktop Management Task Force, Inc., http://www.dmtf.org/tech/specs.html.

- *DMI 2.0, ERRATA #1*, 6 August 1997, Desktop Management Task Force, Inc., http://www.dmtf.org/tech/specs.html.

ESCD
- *Extended System Configuration Data Specification*, v. 1.02a, 31 May 1994, http://www.microsoft.com/hwdev/respec/PNPSPECS.HTM.

Flash
- *28F016SA FlashFile™ Memory Datasheet*, December 1997, Intel Corporation, Number 290489-005, ftp://download.intel.com/design/flcomp/datashts/29048905.PDF.

- *28F016SA/DD28F032SA Specification Update*, July 1996, Intel Corporation, Number 297408-006, ftp://download.intel.com/design/flcomp/SPECUPDT/29740806.pdf.

Hot-plug PCI
- *PCI Hot-plug Specification*, Revision 1.0, PCI Special Interest Group.

- *PCI Hot-plug (PHP) Usage Model Whitepaper*, version 0.55.

I₂O

- *Intelligent I/O (I₂O) Architecture Specification*, Revision 1.0, I₂O Special Interest Group.

MPS
- *MultiProcessor Specification*, Versions 1.1 and 1.4, Intel Corporation.

PC-100
- *PC SDRAM Registered DIMM Specification*, Revision 1.0, February 1998, Intel Corporation,
  http://developer.intel.com/design/pcisets/memory/index.htm

- *PC SDRAM Reistered DIMM Design Support Document*, Rev 1.0, February 1998, Intel Corporation

- *PC SDRAM Specification*, Revision 1.63, October 1998, Intel Corporation,
  http://developer.intel.com/design/pcisets/memory/index.htm

- *PC SDRAM Serial Presence Detect (SPD) Specification*, Revision 1.2A, December 1997, Intel Corporation,
  http://developer.intel.com/design/pcisets/memory/index.htm

PCI
- *PCI Local Bus Specification*, Revision 2.1S, PCI Special Interest Group.
- *PCI BIOS Specification*, Revision 2.1, PCI Special Interest Group.
- *PCI to PCI Bridge Specification*, Revision 1.0, PCI Special Interest Group.
- *PCI Power Management Specification*, Revision 1.0, PCI Special Interest Group.

Pentium® II Xeon™ Processor
- *Pentium® Pro Family Developer's Manual: Specifications*, 1996, Intel Corporation, Number 242690.

- *Pentium® Pro Family Developer's Manual: Programmer's Reference Manual*, 1996, Intel Corporation, Number 242691.

- *Pentium® Pro Family Developer's Manual: Operating System Writer's Guide*, 1996, Intel Corporation, Number 242692.

- *Pentium® Pro Processor BIOS Writer's Guide*, Version 2.0, January 1996, Intel Corporation, ftp://ftp.intel.com/pub/IAL/p6/pppbios.pdf.

- *RS - Extension to Pentium® Pro Processor BIOS Writer's Guide*, Revision 2.0, Intel Corporation, Number OR-1031.

Phoenix BIOS*
- *Phoenix BIOS* 6.0 Users Manual*, Phoenix Technologies Ltd.

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PID

- *Programmable Interrupt Device External Product Specification*, Revision 1.1, Intel Corporation, Number OR4-680777.

PIIX4

- *82371AB PCI-TO-ISA/IDE Xcelerator (PIIX4) Datasheet*, April 1997, Intel Corporation, Number 290562-001, ftp://download.intel.com/design/pcisets/datashts/29056201.pdf.

- *Intel 82371AB (PIIX4) Specification Update*, December 1997, Intel Corporation, Number 297738-002, ftp://download.intel.com/design/pcisets/SPECUPDT/29773802.PDF.

Plug and Play

- *Plug and Play BIOS Specification*, v. 1.0a, 5 May 1994, http://www.microsoft.com/hwdev/respec/PNPSPECS.HTM.

- *Clarification to Plug and Play BIOS Specification*, v. 1.0a, 6 October 1994, http://www.microsoft.com/hwdev/respec/PNPSPECS.HTM.

- *Plug and Play ISA Specification*, v. 1.0a, 5 May 1994, http://www.microsoft.com/hwdev/respec/PNPSPECS.HTM.

- *Clarification to Plug and Play ISA Specification*, v. 1.0a, 10 December 1994, http://www.microsoft.com/hwdev/respec/PNPSPECS.HTM.

PMM

- *POST Memory Manager Specification*, Version 1.01, http://www.ptltd.com/techs/specs.html.

Profusion®

- *Gemini External Design Specification*, June, 1998, Corollary, Inc., Number 99-00322-000-12.

- *PB64 External Design Specification*, 25 June 1998, Corollary, Inc., Number 99-00570-000-02.

SCSI

- *SYM53C896 Data Manual*, version 0.6, Symbios Logic Inc.*

Server Management

- *Emergency Management Port v1.0 Interface External Product Specification*, Revision 0.83, 18 December 1997, Intel Corporation.

- *Intelligent Platform Management Interface Specification*, Version 0.9, Revision 0.17, 28 March 1998, Intel Corporation.

- *Platform Sensor and Event Interface External Product Specification*, Version 1.0, Revision 0.89, 19 December 1997, Intel Corporation.

SMBIOS

- *System Management BIOS Reference Specification*, Version 2.1, 16 June 1997, http://www.ptltd.com/techs/specs.html.

Ultra I/O

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- *FDC37C93xAPM Advance Information*, 15 July 1996, Standard Microsystems Corporation.*

USB
- *Universal Serial Bus Specification*, Revision 1.0, 15 January 1996, http://www.usb.org/developers.

VGA
- *CL-GD5446 Advance Product Bulletin*, Cirrus Logic.*

- *Alpine VGA Family - CL-GD543x/4x Technical Reference Manual*, February 1995, Cirrus Logic.

Wired for Management

- *Wired for Management Baseline Specification*, Version 1.1a, 28 August 1997, Intel Corporation, ftp://download.intel.com/ial/wfm/baseline.pdf.

Windows*
- *Hardware Design Guide for Microsoft Windows NT Server*, Version 1.0.

Miscellaneous
- *Power Supply, 750/650W, PFC, 5 Outputs*, Intel document 676912.

- EN 61000-3-2: Electromagnetic Compatibility (EMC) Part 3: Limits - Section 2: Limits for Harmonic Current Emissions.

- JEIDA MITI Guideline for Suppression of High Harmonics in Appliances and General-Use Equipment.

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