



# Intel<sup>®</sup> I/O Controller Hub 7 (ICH7)/ Intel<sup>®</sup> High Definition Audio/ AC'97

Programmer's Reference Manual (PRM)

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*For the Intel<sup>®</sup> 82801GB ICH7 and 82801GR ICH7R I/O Controller  
Hubs*

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## Revision History

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| Revision | Description       | Date       |
|----------|-------------------|------------|
| -001     | • Initial release | April 2005 |

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# 1 Intel® High Definition Audio Controller Registers (D27:F0)

The Intel® HD Audio controller resides in PCI Device 27, Function 0 on bus 0. This function contains a set of DMA engines that are used to move samples of digitally encoded data between system memory and external codecs.

**Note:** All registers in this function (including memory-mapped registers) must be addressable in byte, word, and DWord quantities. The software must always make register accesses on natural boundaries (i.e. DWord accesses must be on DWord boundaries; word accesses on word boundaries, etc.) In addition, the memory-mapped register space must not be accessed with the LOCK semantic exclusive-access mechanism. If software attempts exclusive-access mechanisms to the Intel® HD Audio memory-mapped space, the results are undefined.

**Note:** Users interested in providing feedback on the Intel® HD Audio specification or planning to implement the Intel® High Definition Audio specification into a future product will need to execute the *Intel® High Definition Audio Specification Developer's Agreement*. For more information, contact [nextgenaudio@intel.com](mailto:nextgenaudio@intel.com).

## 1.1 Intel® High Definition Audio PCI Configuration Space (Intel® High Definition Audio— D27:F0)

**Note:** Address locations that are not shown should be treated as Reserved.

**Table 1-1. Intel® High Definition Audio PCI Register Address Map (Intel® High Definition Audio D27:F0)**

| Offset  | Mnemonic | Register Name                                            | Default                   | Access   |
|---------|----------|----------------------------------------------------------|---------------------------|----------|
| 00h–01h | VID      | Vendor Identification                                    | 8086h                     | RO       |
| 02h–03h | DID      | Device Identification                                    | See register description. | RO       |
| 04h–05h | PCICMD   | PCI Command                                              | 0000h                     | R/W, RO  |
| 06h–07h | PCISTS   | PCI Status                                               | 0010h                     | R/WC, RO |
| 08h     | RID      | Revision Identification                                  | See register description. | RO       |
| 09h     | PI       | Programming Interface                                    | 00h                       | RO       |
| 0Ah     | SCC      | Sub Class Code                                           | 03h                       | RO       |
| 0Bh     | BCC      | Base Class Code                                          | 04h                       | RO       |
| 0Ch     | CLS      | Cache Line Size                                          | 00h                       | R/W      |
| 0Dh     | LT       | Latency Timer                                            | 00h                       | RO       |
| 0Eh     | HEADTYP  | Header Type                                              | 00h                       | RO       |
| 10h–13h | HDBARL   | Intel® High Definition Audio Lower Base Address (Memory) | 00000004h                 | R/W, RO  |

Table 1-1. Intel® High Definition Audio PCI Register Address Map (Intel® High Definition Audio D27:F0)

|           |         |                                                          |                          |               |
|-----------|---------|----------------------------------------------------------|--------------------------|---------------|
| 14h–17h   | HDBARU  | Intel® High Definition Audio Upper Base Address (Memory) | 00000000h                | R/W           |
| 2Ch–2Dh   | SVID    | Subsystem Vendor Identification                          | 0000h                    | R/WO          |
| 2Eh–2Fh   | SID     | Subsystem Identification                                 | 0000h                    | R/WO          |
| 34h       | CAPPTR  | Capability List Pointer                                  | 50h                      | RO            |
| 3Ch       | INTLN   | Interrupt Line                                           | 00h                      | R/W           |
| 3Dh       | INTPN   | Interrupt Pin                                            | See Register Description | RO            |
| 40h       | HDCTL   | Intel High Definition Audio Control                      | 00h                      | R/W, RO       |
| 44h       | TCSEL   | Traffic Class Select                                     | 00h                      | R/W           |
| 4Dh       | DCKSTS  | Docking Status                                           | 80h                      | R/WO, RO      |
| 50h–51h   | PID     | PCI Power Management Capability ID                       | 6001h                    | RO            |
| 52h–53h   | PC      | Power Management Capabilities                            | C842                     | RO            |
| 54h–57h   | PCS     | Power Management Control and Status                      | 00000000h                | R/W, RO, R/WC |
| 60h–61h   | MID     | MSI Capability ID                                        | 7005h                    | RO            |
| 62h–63h   | MMC     | MSI Message Control                                      | 0080h                    | R/W, RO       |
| 64h–67h   | MMLA    | MSI Message Lower Address                                | 00000000h                | R/W, RO       |
| 68h–6Bh   | MMUA    | SMI Message Upper Address                                | 00000000h                | R/W           |
| 6Ch–6Dh   | MMD     | MSI Message Data                                         | 0000h                    | R/W           |
| 70h–71h   | PXID    | PCI Express* Capability Identifiers                      | 0010h                    | RO            |
| 72h–73h   | PXC     | PCI Express Capabilities                                 | 0091h                    | RO            |
| 74h–77h   | DEVCAP  | Device Capabilities                                      | 00000000h                | RO, R/WO      |
| 78h–79h   | DEVC    | Device Control                                           | 0800h                    | R/W, RO       |
| 7Ah–7Bh   | DEVS    | Device Status                                            | 0010h                    | RO            |
| 100h–103h | VCCAP   | Virtual Channel Enhanced Capability Header               | 13010002h                | RO            |
| 104h–107h | PVCCAP1 | Port VC Capability Register 1                            | 00000001h                | RO            |
| 108h–10Bh | PVCCAP2 | Port VC Capability Register 2                            | 00000000h                | RO            |
| 10Ch–10D  | PVCCTL  | Port VC Control                                          | 0000h                    | RO            |
| 10Eh–10Fh | PVCSTS  | Port VC Status                                           | 0000h                    | RO            |
| 110h–103h | VC0CAP  | VC0 Resource Capability                                  | 00000000h                | RO            |
| 114h–117h | VC0CTL  | VC0 Resource Control                                     | 800000FFh                | R/W, RO       |
| 11Ah–11Bh | VC0STS  | VC0 Resource Status                                      | 0000h                    | RO            |
| 11Ch–11Fh | VCiCAP  | VCi Resource Capability                                  | 00000000h                | RO            |
| 120h–123h | VCiCTL  | VCi Resource Control                                     | 00000000h                | R/W, RO       |
| 126h–127h | VCiSTS  | VCi Resource Status                                      | 0000h                    | RO            |
| 130h–133h | RCCAP   | Root Complex Link Declaration Enhanced Capability Header | 00010005h                | RO            |
| 134h–137h | ESD     | Element Self Description                                 | 0F000100h                | RO            |
| 140h–143h | L1DESC  | Link 1 Description                                       | 00000001h                | RO            |
| 148h–14Bh | L1ADDL  | Link 1 Lower Address                                     | See Register Description | RO            |
| 14Ch–14Fh | L1ADDU  | Link 1 Upper Address                                     | 00000000h                | RO            |



### 1.1.1 VID—Vendor Identification Register (Intel® High Definition Audio Controller—D27:F0)

Offset: 00h-01h Attribute: RO  
Default Value: 8086h Size: 16 bits

| Bit  | Description                                                                        |
|------|------------------------------------------------------------------------------------|
| 15:0 | <b>Vendor ID</b> — RO. This is a 16-bit value assigned to Intel. Intel VID = 8086h |

### 1.1.2 DID—Device Identification Register (Intel® High Definition Audio Controller—D27:F0)

Offset Address: 02h-03h Attribute: RO  
Default Value: See bit description Size: 16 bits

| Bit  | Description                                                                                                                                                                                                                                    |
|------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:0 | <b>Device ID</b> — RO. This is a 16-bit value assigned to the Intel® ICH7 Intel® High Definition Audio controller. Refer to the <i>Intel® I/O Controller Hub 7 (ICH7) Family Specification Update</i> for the value of the Device ID Register. |

### 1.1.3 PCICMD—PCI Command Register (Intel® High Definition Audio Controller—D27:F0)

Offset Address: 04h–05h  
Default Value: 0000h

Attribute: R/W, RO  
Size: 16 bits

| Bit   | Description                                                                                                                                                                                                                                                              |
|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:11 | Reserved                                                                                                                                                                                                                                                                 |
| 10    | <p><b>Interrupt Disable (ID)</b> — R/W.<br/>0= The INTx# signals may be asserted.<br/>1= The Intel® High Definition Audio controller's INTx# signal will be de-asserted</p> <p><b>NOTE:</b> This bit does not affect the generation of MSIs.</p>                         |
| 9     | Fast Back to Back Enable (FBE) — RO. Not implemented. Hardwired to 0.                                                                                                                                                                                                    |
| 8     | SERR# Enable (SERR_EN) — R/W. SERR# is not generated by the ICH7 Intel High Definition Audio Controller.                                                                                                                                                                 |
| 7     | Wait Cycle Control (WCC) — RO. Not implemented. Hardwired to 0.                                                                                                                                                                                                          |
| 6     | Parity Error Response (PER) — RO. Not implemented. Hardwired to 0.                                                                                                                                                                                                       |
| 5     | VGA Palette Snoop (VPS). Not implemented. Hardwired to 0.                                                                                                                                                                                                                |
| 4     | Memory Write and Invalidate Enable (MWIE) — RO. Not implemented. Hardwired to 0.                                                                                                                                                                                         |
| 3     | Special Cycle Enable (SCE). Not implemented. Hardwired to 0.                                                                                                                                                                                                             |
| 2     | <p><b>Bus Master Enable (BME)</b> — R/W. Controls standard PCI Express* bus mastering capabilities for Memory and I/O, reads and writes. Note that this bit also controls MSI generation since MSIs are essentially Memory writes.</p> <p>0 = Disable<br/>1 = Enable</p> |
| 1     | <p><b>Memory Space Enable (MSE)</b> — R/W. Enables memory space addresses to the Intel High Definition Audio controller.</p> <p>0 = Disable<br/>1 = Enable</p>                                                                                                           |
| 0     | I/O Space Enable (IOSE)—RO. Hardwired to 0 since the Intel High Definition Audio controller does not implement I/O space.                                                                                                                                                |





### 1.1.6 PI—Programming Interface Register (Intel® High Definition Audio Controller—D27:F0)

Offset: 09h Attribute: RO  
Default Value: 00h Size: 8 bits

| Bit | Description                 |
|-----|-----------------------------|
| 7:0 | Programming Interface — RO. |

### 1.1.7 SCC—Sub Class Code Register (Intel® High Definition Audio Controller—D27:F0)

Address Offset: 0Ah Attribute: RO  
Default Value: 03h Size: 8 bits

| Bit | Description                                      |
|-----|--------------------------------------------------|
| 7:0 | Sub Class Code (SCC) — RO.<br>03h = Audio Device |

### 1.1.8 BCC—Base Class Code Register (Intel® High Definition Audio Controller—D27:F0)

Address Offset: 0Bh Attribute: RO  
Default Value: 04h Size: 8 bits

| Bit | Description                                            |
|-----|--------------------------------------------------------|
| 7:0 | Base Class Code (BCC) — RO.<br>04h = Multimedia device |

### 1.1.9 CLS—Cache Line Size Register (Intel® High Definition Audio Controller—D27:F0)

Address Offset: 0Ch Attribute: R/W  
Default Value: 00h Size: 8 bits

| Bit | Description                                                                                   |
|-----|-----------------------------------------------------------------------------------------------|
| 7:0 | Cache Line Size — R/W. Implemented as R/W register, but has no functional impact to the ICH7. |



### 1.1.14 SVID—Subsystem Vendor Identification Register (Intel® High Definition Audio Controller—D27:F0)

Address Offset: 2Ch–2Dh                      Attribute: R/WO  
Default Value: 0000h                      Size: 16 bits

The SVID register, in combination with the Subsystem ID register (D27:F0:2Eh), enable the operating environment to distinguish one audio subsystem from the other(s).

This register is implemented as write-once register. Once a value is written to it, the value can be read back. Any subsequent writes will have no effect.

This register is not affected by the D3<sub>HOT</sub> to D0 transition.

| Bit  | Description                 |
|------|-----------------------------|
| 15:0 | Subsystem Vendor ID — R/WO. |

### 1.1.15 SID—Subsystem Identification Register (Intel® High Definition Audio Controller—D27:F0)

Address Offset: 2Eh–2Fh                      Attribute: R/WO  
Default Value: 0000h                      Size: 16 bits

The SID register, in combination with the Subsystem Vendor ID register (D27:F0:2Ch) make it possible for the operating environment to distinguish one audio subsystem from the other(s).

This register is implemented as write-once register. Once a value is written to it, the value can be read back. Any subsequent writes will have no effect.

This register is not affected by the D3<sub>HOT</sub> to D0 transition.

| Bit  | Description                 |
|------|-----------------------------|
| 15:0 | <b>Subsystem ID</b> — R/WO. |



### 1.1.19 HDCTL—Intel® High Definition Audio Control Register (Intel® High Definition Audio Controller—D27:F0)

Address Offset: 40h Attribute: R/W, RO  
 Default Value: 00h Size: 8 bits

| Bit | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
|-----|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:4 | Reserved.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
| 3   | <p><b>BITCLK Detect Clear (CLKDETCLR)</b> — R/W.</p> <p>0 = Clock detect circuit is operational and maybe enabled.<br/>           1 = Writing a 1 to this bit clears bit 1 (CLKDET#) in this register. CLKDET# bit remains clear when this bit is set to 1.</p> <p><b>NOTE:</b> This bit is not affected by the D3<sub>HOT</sub> to D0 transition.</p>                                                                                                                                                                                                                                                                                 |
| 2   | <p><b>BITCLK Detect Enable (CLKDETEN)</b> — R/W.</p> <p>0 = Latches the current state of bit 1 (CLKDET#) in this register<br/>           1 = Enables the clock detection circuit</p> <p><b>NOTE:</b> This bit is not affected by the D3<sub>HOT</sub> to D0 transition.</p>                                                                                                                                                                                                                                                                                                                                                            |
| 1   | <p>BITCLK Detected Inverted (CLKDET#) — RO. This bit is modified by hardware.<br/>           It is set to 0 when the Intel® ICH7 detects that the BITCLK is toggling, indicating the presence of an AC'97 codec on the link</p> <p><b>NOTES:</b></p> <ol style="list-style-type: none"> <li>Bit 2 (CLKDETEN) and bit 3 (CLKDETCLR) in this register control the operation of this bit and must be manipulated correctly in order to get a valid CLKDET# indicator.</li> <li>This bit is not affected by the D3<sub>HOT</sub> to D0 transition.</li> </ol>                                                                              |
| 0   | <p><b>Intel® High Definition Audio/AC '97 Signal Mode</b> — R/W. This bit selects the shared Intel High Definition Audio/AC '97 signals.</p> <p>0 = AC '97 mode is selected (Default)<br/>           1 = Intel High Definition Audio mode is selected</p> <p><b>NOTES:</b></p> <ol style="list-style-type: none"> <li>This bit has no effect on the visibility of the Intel High Definition Audio and AC '97 function configuration space.</li> <li>This bit is in the resume well and only clear on a power-on reset. Software must not makes assumptions about the reset state of this bit and must set it appropriately.</li> </ol> |







### 1.1.23 PC—Power Management Capabilities Register (Intel® High Definition Audio Controller—D27:F0)

Address Offset: 52h–53h Attribute: RO  
 Default Value: C842h Size: 16 bits

| Bit   | Description                                                                                                                    |
|-------|--------------------------------------------------------------------------------------------------------------------------------|
| 15:11 | PME Support — RO. Hardwired to 11001b. Indicates PME# can be generated from D3 and D0 states.                                  |
| 10    | D2 Support — RO. Hardwired to 0. Indicates that D2 state is not supported.                                                     |
| 9     | D1 Support —RO. Hardwired to 0. Indicates that D1 state is not supported.                                                      |
| 8:6   | Aux Current — RO. Hardwired to 001b. Reports 55 mA maximum suspend well current required when in the D3 <sub>COLD</sub> state. |
| 5     | Device Specific Initialization (DSI) — RO. Hardwired to 0. Indicates that no device specific initialization is required.       |
| 4     | Reserved                                                                                                                       |
| 3     | PME Clock (PMEC) — RO. Does not apply. Hardwired to 0.                                                                         |
| 2:0   | Version — RO. Hardwired to 010b. Indicates support for version 1.1 of the PCI Power Management Specification.                  |

### 1.1.24 PCS—Power Management Control and Status Register (Intel® High Definition Audio Controller—D27:F0)

Address Offset: 54h–57h Attribute: RO, R/W, R/WC  
 Default Value: 00000000h Size: 32 bits

| Bit   | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:24 | Data — RO. Does not apply. Hardwired to 0.                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
| 23    | Bus Power/Clock Control Enable — RO. Does not apply. Hardwired to 0.                                                                                                                                                                                                                                                                                                                                                                                                                                      |
| 22    | B2/B3 Support — RO. Does not apply. Hardwired to 0.                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
| 21:16 | Reserved.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
| 15    | <b>PME Status (PMES)</b> — R/WC.<br>0 = Software clears the bit by writing a 1 to it.<br>1 = This bit is set when the Intel® High Definition Audio controller would normally assert the PME# signal independent of the state of the PME_EN bit (bit 8 in this register)<br>This bit is in the resume well and only cleared on a power-on reset. Software must not make assumptions about the reset state of this bit and must set it appropriately.                                                       |
| 14:9  | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| 8     | <b>PME Enable (PMEE)</b> — R/W.<br>0 = Disable<br>1 = when set and if corresponding PMES also set, the Intel High Definition Audio controller sets the AC97_STS bit in the GPE0_STS register (PMBASE +28h). The AC97_STS bit is shared by AC '97 and Intel High Definition Audio functions since they are mutually exclusive.<br>This bit is in the resume well and only cleared on a power-on reset. Software must not make assumptions about the reset state of this bit and must set it appropriately. |
| 7:2   | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |

| Bit | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
|-----|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1:0 | <p><b>Power State (PS)</b> — R/W. This field is used both to determine the current power state of the Intel High Definition Audio controller and to set a new power state.</p> <p>00 = D0 state<br/>11 = D3<sub>HOT</sub> state<br/>Others = reserved</p> <p><b>NOTES:</b></p> <ol style="list-style-type: none"> <li>1. If software attempts to write a value of 01b or 10b in to this field, the write operation must complete normally; however, the data is discarded and no state change occurs.</li> <li>2. When in the D3<sub>HOT</sub> states, the Intel High Definition Audio controller's configuration space is available, but the I/O and memory space are not. Additionally, interrupts are blocked.</li> <li>3. When software changes this value from D3<sub>HOT</sub> state to the D0 state, an internal warm (soft) reset is generated, and software must re-initialize the function.</li> </ol> |

### 1.1.25 MID—MSI Capability ID Register (Intel® High Definition Audio Controller—D27:F0)

Address Offset: 60h–61h                      Attribute: RO  
Default Value: 7005h                      Size: 16 bits

| Bit  | Description                                                                                     |
|------|-------------------------------------------------------------------------------------------------|
| 15:8 | Next Capability (Next) — RO. Hardwired to 70h. Points to the PCI Express* capability structure. |
| 7:0  | Cap ID (CAP) — RO. Hardwired to 05h. Indicates that this pointer is a MSI capability            |

### 1.1.26 MMC—MSI Message Control Register (Intel® High Definition Audio Controller—D27:F0)

Address Offset: 62h–63h                      Attribute: RO, R/W  
Default Value: 0080h                      Size: 16 bits

| Bit  | Description                                                                                                                                                   |
|------|---------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:8 | Reserved                                                                                                                                                      |
| 7    | 64b Address Capability (64ADD) — RO. Hardwired to 1 indicating the ability to generate a 64-bit message address                                               |
| 6:4  | Multiple Message Enable (MME) — RO. Normally this is a R/W register. However, since only 1 message is supported, these bits are hardwired to 000 = 1 message. |
| 3:1  | Multiple Message Capable (MMC) — RO. Hardwired to 0 indicating request for 1 message.                                                                         |
| 0    | <p><b>MSI Enable (ME)</b> — R/W.</p> <p>0 = an MSI may not be generated<br/>1 = an MSI will be generated instead of an INTx signal.</p>                       |



### 1.1.31 PXC—PCI Express\* Capabilities Register (Intel® High Definition Audio Controller—D27:F0)

Address Offset: 72h–73h                      Attribute: RO  
 Default Value: 0091h                      Size: 16 bits

| Bit   | Description                                                                                                        |
|-------|--------------------------------------------------------------------------------------------------------------------|
| 15:14 | Reserved                                                                                                           |
| 13:9  | Interrupt Message Number (IMN) — RO. Hardwired to 0.                                                               |
| 8     | Slot Implemented (SI) — RO. Hardwired to 0.                                                                        |
| 7:4   | Device/Port Type (DPT) — RO. Hardwired to 1001b. Indicates that this is a Root Complex Integrated endpoint device. |
| 3:0   | Capability Version (CV) — RO. Hardwired to 0001b. Indicates version #1 PCI Express capability.                     |

### 1.1.32 DEVCAP—Device Capabilities Register (Intel® High Definition Audio Controller—D27:F0)

Address Offset: 74h–77h                      Attribute: R/WO, RO  
 Default Value: 00000000h                      Size: 32 bits

| Bit   | Description                                                                                           |
|-------|-------------------------------------------------------------------------------------------------------|
| 31:28 | Reserved                                                                                              |
| 27:26 | Captured Slot Power Limit Scale (SPLS) — RO. Hardwired to 0.                                          |
| 25:18 | Captured Slot Power Limit Value (SPLV) — RO. Hardwired to 0.                                          |
| 17:15 | Reserved                                                                                              |
| 14    | Power Indicator Present — RO. Hardwired to 0.                                                         |
| 13    | Attention Indicator Present — RO. Hardwired to 0.                                                     |
| 12    | Attention Button Present — RO. Hardwired to 0.                                                        |
| 11:9  | Endpoint L1 Acceptable Latency — R/WO.                                                                |
| 8:6   | Endpoint L0s Acceptable Latency — R/WO.                                                               |
| 5     | Extended Tag Field Support — RO. Hardwired to 0. Indicates 5-bit tag field support                    |
| 4:3   | Phantom Functions Supported — RO. Hardwired to 0. Indicates that phantom functions are not supported. |
| 2:0   | Max Payload Size Supported — RO. Hardwired to 0. Indicates 128-B maximum payload size capability.     |

### 1.1.33 DEVC—Device Control Register (Intel® High Definition Audio Controller—D27:F0)

Address Offset: 78h–79h Attribute: R/W, RO  
 Default Value: 0800h Size: 16 bits

| Bit   | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| 14:12 | Max Read Request Size — RO. Hardwired to 0 enabling 128B maximum read request size.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
| 11    | <p><b>No Snoop Enable (NSNPEN)</b> — R/W.</p> <p>0 = The Intel® High Definition Audio controller will not set the No Snoop bit. In this case, isochronous transfers will not use VC1 (VCi) even if it is enabled since VC1 is never snooped. Isochronous transfers will use VC0.</p> <p>1 = The Intel High Definition Audio controller is permitted to set the No Snoop bit in the Requester Attributes of a bus master transaction. In this case, VC0 or VC1 may be used for isochronous transfers.</p> <p><b>NOTE:</b> This bit is not reset on D3<sub>HOT</sub> to D0 transition; however, it is reset by PLTRST#.</p> |
| 10    | Auxiliary Power Enable — RO. Hardwired to 0, indicating that Intel High Definition Audio device does not draw AUX power.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| 9     | Phantom Function Enable — RO. Hardwired to 0 disabling phantom functions.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
| 8     | Extended Tag Field Enable — RO. Hardwired to 0 enabling 5-bit tag.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
| 7:5   | Max Payload Size — RO. Hardwired to 0 indicating 128B.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
| 4     | Enable Relaxed Ordering — RO. Hardwired to 0 disabling relaxed ordering.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| 3     | Unsupported Request Reporting Enable — RO. Not implemented. Hardwired to 0.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
| 2     | Fatal Error Reporting Enable — RO. Not implemented. Hardwired to 0.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
| 1     | Non-Fatal Error Reporting Enable — RO. Not implemented. Hardwired to 0.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
| 0     | Correctable Error Reporting Enable — RO. Not implemented. Hardwired to 0.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |

### 1.1.34 DEVS—Device Status Register (Intel® High Definition Audio Controller—D27:F0)

Address Offset: 7Ah–7Bh Attribute: RO  
 Default Value: 0010h Size: 16 bits

| Bit  | Description                                                                                                                                                                                                                                            |
|------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:6 | Reserved                                                                                                                                                                                                                                               |
| 5    | <p>Transactions Pending — RO.</p> <p>0 = Indicates that completions for all non-posted requests have been received.</p> <p>1 = Indicates that Intel® High Definition Audio controller has issued non-posted requests that have not been completed.</p> |
| 4    | AUX Power Detected — RO. Hardwired to 1 indicating the device is connected to resume power.                                                                                                                                                            |
| 3    | Unsupported Request Detected — RO. Not implemented. Hardwired to 0.                                                                                                                                                                                    |
| 2    | Fatal Error Detected — RO. Not implemented. Hardwired to 0.                                                                                                                                                                                            |
| 1    | Non-Fatal Error Detected — RO. Not implemented. Hardwired to 0.                                                                                                                                                                                        |
| 0    | Correctable Error Detected — RO. Not implemented. Hardwired to 0.                                                                                                                                                                                      |

### 1.1.35 VCCAP—Virtual Channel Enhanced Capability Header (Intel® High Definition Audio Controller—D27:F0)

Address Offset: 100h–103h                      Attribute: RO  
 Default Value: 13010002h                      Size: 32 bits

| Bit   | Description                                                                                                                                                |
|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:20 | Next Capability Offset — RO. Hardwired to 130h. Points to the next capability header that is the Root Complex Link Declaration Enhanced Capability Header. |
| 19:16 | Capability Version — RO. Hardwired to 1h.                                                                                                                  |
| 15:0  | PCI Express* Extended Capability — RO. Hardwired to 0002h.                                                                                                 |

### 1.1.36 PVCCAP1—Port VC Capability Register 1 (Intel® High Definition Audio Controller—D27:F0)

Address Offset: 104h–107h                      Attribute: RO  
 Default Value: 00000001h                      Size: 32 bits

| Bit   | Description                                                                                                                                               |
|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:12 | Reserved.                                                                                                                                                 |
| 11:10 | Port Arbitration Table Entry Size — RO. Hardwired to 0 since this is an endpoint device.                                                                  |
| 9:8   | Reference Clock — RO. Hardwired to 0 since this is an endpoint device.                                                                                    |
| 7     | Reserved.                                                                                                                                                 |
| 6:4   | Low Priority Extended VC Count — RO. Hardwired to 0. Indicates that only VC0 belongs to the low priority VC group.                                        |
| 3     | Reserved.                                                                                                                                                 |
| 2:0   | Extended VC Count — RO. Hardwired to 001b. Indicates that 1 extended VC (in addition to VC0) is supported by the Intel® High Definition Audio controller. |

### 1.1.37 PVCCAP2 — Port VC Capability Register 2 (Intel® High Definition Audio Controller—D27:F0)

Address Offset: 108h–10Bh                      Attribute: RO  
 Default Value: 00000000h                      Size: 32 bits

| Bit   | Description                                                                                                                                                                                                     |
|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:24 | VC Arbitration Table Offset — RO. Hardwired to 0 indicating that a VC arbitration table is not present.                                                                                                         |
| 23:8  | Reserved.                                                                                                                                                                                                       |
| 7:0   | VC Arbitration Capability — RO. Hardwired to 0. These bits are not applicable since the Intel® High Definition Audio controller reports a 0 in the Low Priority Extended VC Count bits in the PVCCAP1 register. |

### 1.1.38 PVCCTL — Port VC Control Register (Intel® High Definition Audio Controller—D27:F0)

Address Offset: 10Ch–10Dh                      Attribute: RO  
 Default Value: 0000h                              Size: 16 bits

| Bit  | Description                                                                                                                                                                                                                                       |
|------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:4 | Reserved.                                                                                                                                                                                                                                         |
| 3:1  | VC Arbitration Select — RO. Hardwired to 0. Normally these bits are R/W. However, these bits are not applicable since the Intel® High Definition Audio controller reports a 0 in the Low Priority Extended VC Count bits in the PVCCAP1 register. |
| 0    | Load VC Arbitration Table — RO. Hardwired to 0 since an arbitration table is not present.                                                                                                                                                         |

### 1.1.39 PVCSTS—Port VC Status Register (Intel® High Definition Audio Controller—D27:F0)

Address Offset: 10Eh-10Fh                      Attribute: RO  
 Default Value: 0000h                              Size: 16 bits

| Bit  | Description                                                                                 |
|------|---------------------------------------------------------------------------------------------|
| 15:1 | Reserved.                                                                                   |
| 0    | VC Arbitration Table Status — RO. Hardwired to 0 since an arbitration table is not present. |

### 1.1.40 VC0CAP—VC0 Resource Capability Register (Intel® High Definition Audio Controller—D27:F0)

Address Offset: 110h–113h      Attribute: RO  
 Default Value: 00000000h      Size: 32 bits

| Bit   | Description                                                                                            |
|-------|--------------------------------------------------------------------------------------------------------|
| 31:24 | Port Arbitration Table Offset — RO. Hardwired to 0 since this field is not valid for endpoint devices. |
| 23    | Reserved.                                                                                              |
| 22:16 | Maximum Time Slots — RO. Hardwired to 0 since this field is not valid for endpoint devices.            |
| 15    | Reject Snoop Transactions — RO. Hardwired to 0 since this field is not valid for endpoint devices.     |
| 14    | Advanced Packet Switching — RO. Hardwired to 0 since this field is not valid for endpoint devices.     |
| 13:8  | Reserved.                                                                                              |
| 7:0   | Port Arbitration Capability — RO. Hardwired to 0 since this field is not valid for endpoint devices.   |

### 1.1.41 VC0CTL—VC0 Resource Control Register (Intel® High Definition Audio Controller—D27:F0)

Address Offset: 114h–117h      Attribute: R/W, RO  
 Default Value: 800000FFh      Size: 32 bits

| Bit   | Description                                                                                                                  |
|-------|------------------------------------------------------------------------------------------------------------------------------|
| 31    | VC0 Enable — RO. Hardwired to 1 for VC0.                                                                                     |
| 30:27 | Reserved.                                                                                                                    |
| 26:24 | VC0 ID — RO. Hardwired to 0 since the first VC is always assigned as VC0.                                                    |
| 23:20 | Reserved.                                                                                                                    |
| 19:17 | Port Arbitration Select — RO. Hardwired to 0 since this field is not valid for endpoint devices.                             |
| 16    | Load Port Arbitration Table — RO. Hardwired to 0 since this field is not valid for endpoint devices.                         |
| 15:8  | Reserved.                                                                                                                    |
| 7:0   | <b>TC/VC0 Map</b> — R/W, RO. Bit 0 is hardwired to 1 since TC0 is always mapped VC0. Bits [7:1] are implemented as R/W bits. |

### 1.1.42 VC0STS—VC0 Resource Status Register (Intel® High Definition Audio Controller—D27:F0)

Address Offset: 11Ah–11Bh      Attribute: RO  
 Default Value: 0000h      Size: 16 bits

| Bit  | Description                                                                                                                       |
|------|-----------------------------------------------------------------------------------------------------------------------------------|
| 15:2 | Reserved.                                                                                                                         |
| 1    | VC0 Negotiation Pending — RO. Hardwired to 0 since this bit does not apply to the integrated Intel® High Definition Audio device. |
| 0    | Port Arbitration Table Status — RO. Hardwired to 0 since this field is not valid for endpoint devices.                            |



### 1.1.43 VCI<sub>CAP</sub>—VCI Resource Capability Register (Intel® High Definition Audio Controller—D27:F0)

Address Offset: 11Ch–11Fh                      Attribute: RO  
 Default Value: 00000000h                      Size: 32 bits

| Bit   | Description                                                                                            |
|-------|--------------------------------------------------------------------------------------------------------|
| 31:24 | Port Arbitration Table Offset — RO. Hardwired to 0 since this field is not valid for endpoint devices. |
| 23    | Reserved.                                                                                              |
| 22:16 | Maximum Time Slots — RO. Hardwired to 0 since this field is not valid for endpoint devices.            |
| 15    | Reject Snoop Transactions — RO. Hardwired to 0 since this field is not valid for endpoint devices.     |
| 14    | Advanced Packet Switching — RO. Hardwired to 0 since this field is not valid for endpoint devices.     |
| 13:8  | Reserved                                                                                               |
| 7:0   | Port Arbitration Capability — RO. Hardwired to 0 since this field is not valid for endpoint devices.   |

### 1.1.44 VCI<sub>CTL</sub>—VCI Resource Control Register (Intel® High Definition Audio Controller—D27:F0)

Address Offset: 120h–123h                      Attribute: R/W, RO  
 Default Value: 00000000h                      Size: 32 bits

| Bit   | Description                                                                                                                                                                                                                                                                                        |
|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31    | <b>VCI Enable</b> — R/W.<br>0 = VCI is disabled<br>1 = VCI is enabled<br><br><b>NOTE:</b> This bit is not reset on D3 <sub>HOT</sub> to D0 transition; however, it is reset by PLTRST#.                                                                                                            |
| 30:27 | Reserved.                                                                                                                                                                                                                                                                                          |
| 26:24 | <b>VCI ID</b> — R/W. This field assigns a VC ID to the VCI resource. This field is not used by the ICH7 hardware, but it is R/W to avoid confusing software.                                                                                                                                       |
| 23:20 | Reserved.                                                                                                                                                                                                                                                                                          |
| 19:17 | Port Arbitration Select — RO. Hardwired to 0 since this field is not valid for endpoint devices.                                                                                                                                                                                                   |
| 16    | Load Port Arbitration Table — RO. Hardwired to 0 since this field is not valid for endpoint devices.                                                                                                                                                                                               |
| 15:8  | Reserved.                                                                                                                                                                                                                                                                                          |
| 7:0   | <b>TC/VCI Map</b> — R/W, RO. This field indicates the TCs that are mapped to the VCI resource. Bit 0 is hardwired to 0 indicating that it cannot be mapped to VCI. Bits [7:1] are implemented as R/W bits. This field is not used by the ICH7 hardware, but it is R/W to avoid confusing software. |

### 1.1.45 VCiSTS—VCi Resource Status Register (Intel® High Definition Audio Controller—D27:F0)

Address Offset: 126h–127h                      Attribute: RO  
 Default Value: 0000h                          Size: 16 bits

| Bit  | Description                                                                                            |
|------|--------------------------------------------------------------------------------------------------------|
| 15:2 | Reserved.                                                                                              |
| 1    | VCi Negotiation Pending — RO. Does not apply. Hardwired to 0.                                          |
| 0    | Port Arbitration Table Status — RO. Hardwired to 0 since this field is not valid for endpoint devices. |

### 1.1.46 RCCAP—Root Complex Link Declaration Enhanced Capability Header Register (Intel® High Definition Audio Controller—D27:F0)

Address Offset: 130h–133h                      Attribute: RO  
 Default Value: 00010005h                      Size: 32 bits

| Bit   | Description                                                                         |
|-------|-------------------------------------------------------------------------------------|
| 31:20 | Next Capability Offset — RO. Hardwired to 0 indicating this is the last capability. |
| 19:16 | Capability Version — RO. Hardwired to 1h.                                           |
| 15:0  | PCI Express* Extended Capability ID — RO. Hardwired to 0005h.                       |

### 1.1.47 ESD—Element Self Description Register (Intel® High Definition Audio Controller—D27:F0)

Address Offset: 134h–137h                      Attribute: RO  
 Default Value: 0F000100h                      Size: 32 bits

| Bit   | Description                                                                                                                                                 |
|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:24 | Port Number — RO. Hardwired to 0Fh indicating that the Intel® High Definition Audio controller is assigned as Port #15d.                                    |
| 23:16 | Component ID — RO. This field returns the value of the ESD.CID field of the chip configuration section. ESD.CID is programmed by BIOS.                      |
| 15:8  | Number of Link Entries — RO. The Intel High Definition Audio only connects to one device, the ICH7 egress port. Therefore this field reports a value of 1h. |
| 7:4   | Reserved.                                                                                                                                                   |
| 3:0   | Element Type (ELTYP) — RO. The Intel High Definition Audio controller is an integrated Root Complex Device. Therefore, the field reports a value of 0h.     |

### 1.1.48 L1DESC—Link 1 Description Register (Intel® High Definition Audio Controller—D27:F0)

Address Offset: 140h–143h                      Attribute: RO  
 Default Value: 00000001h                      Size: 32 bits

| Bit   | Description                                                                                                                                   |
|-------|-----------------------------------------------------------------------------------------------------------------------------------------------|
| 31:24 | Target Port Number — RO. The Intel® High Definition Audio controller targets the Intel® ICH7's Port #0.                                       |
| 23:16 | Target Component ID — RO. This field returns the value of the ESD.CID field of the chip configuration section. ESD.CID is programmed by BIOS. |
| 15:2  | Reserved.                                                                                                                                     |
| 1     | Link Type — RO. Hardwired to 0 indicating Type 0.                                                                                             |
| 0     | Link Valid — RO. Hardwired to 1.                                                                                                              |

### 1.1.49 L1ADDL—Link 1 Lower Address Register (Intel® High Definition Audio Controller—D27:F0)

Address Offset: 148h–14Bh                      Attribute: RO  
 Default Value: See Register Description                      Size: 32 bits

| Bit   | Description                                                                                               |
|-------|-----------------------------------------------------------------------------------------------------------|
| 31:14 | Link 1 Lower Address — RO. Hardwired to match the RCBA register value in the PCI-LPC bridge (D31:F0:F0h). |
| 13:0  | Reserved.                                                                                                 |

### 1.1.50 L1ADDU—Link 1 Upper Address Register (Intel® High Definition Audio Controller—D27:F0)

Address Offset: 14Ch–14Fh                      Attribute: RO  
 Default Value: 00000000h                      Size: 32 bits

| Bit  | Description                                        |
|------|----------------------------------------------------|
| 31:0 | Link 1 Upper Address — RO. Hardwired to 00000000h. |

## 1.2 Intel® High Definition Audio Memory Mapped Configuration Registers (Intel® High Definition Audio— D27:F0)

The base memory location for these memory mapped configuration registers is specified in the HDBAR register (D27:F0:offset 10h and D27:F0:offset 14h). The individual registers are then accessible at HDBAR + Offset as indicated in Table 1-2.

These memory mapped registers must be accessed in byte, word, or DWord quantities.

**Table 1-2. Intel® High Definition Audio PCI Register Address Map (Intel® High Definition Audio D27:F0) (Sheet 1 of 4)**

| HDBAR + Offset | Mnemonic   | Register Name                    | Default   | Access  |
|----------------|------------|----------------------------------|-----------|---------|
| 00h–01h        | GCAP       | Global Capabilities              | 4401h     | RO      |
| 02h            | VMIN       | Minor Version                    | 00h       | RO      |
| 03h            | VMAJ       | Major Version                    | 01h       | RO      |
| 04h–05h        | OUTPAY     | Output Payload Capability        | 003Ch     | RO      |
| 06h–07h        | INPAY      | Input Payload Capability         | 001Dh     | RO      |
| 08h–0Bh        | GCTL       | Global Control                   | 00000000h | R/W     |
| 0Ch–0Dh        | WAKEEN     | Wake Enable                      | 0000h     | R/W     |
| 0Eh–0Fh        | STATESTS   | State Change Status              | 0000h     | R/WC    |
| 10h–11h        | GSTS       | Global Status                    | 0000h     | R/WC    |
| 12h–13h        | Rsv        | Reserved                         | 0000h     | RO      |
| 18h–19h        | OUTSTRMPAY | Output Stream Payload Capability | 0030h     | RO      |
| 1Ah–1Bh        | INSTRMPAY  | Input Stream Payload Capability  | 0018h     | RO      |
| 1Ch–1Fh        | Rsv        | Reserved                         | 00000000h | RO      |
| 20h–23h        | INTCTL     | Interrupt Control                | 00000000h | R/W     |
| 24h–27h        | INTSTS     | Interrupt Status                 | 00000000h | RO      |
| 30h–33h        | WALCLK     | Wall Clock Counter               | 00000000h | RO      |
| 34h–37h        | SSYNC      | Stream Synchronization           | 00000000h | R/W     |
| 40h–43h        | CORBLOWER  | CORB Lower Base Address          | 00000000h | R/W, RO |
| 44h–47h        | CORBUBASE  | CORB Upper Base Address          | 00000000h | R/W     |
| 48h–49h        | CORBWP     | CORB Write Pointer               | 0000h     | R/W     |
| 4Ah–4Bh        | CORBWP     | CORB Read Pointer                | 0000h     | R/W     |
| 4Ch            | CORBCTL    | CORB Control                     | 00h       | R/W     |
| 4Dh            | CORBST     | CORB Status                      | 00h       | R/WC    |
| 4Eh            | CORBSIZE   | CORB Size                        | 42h       | RO      |
| 50h–53h        | RIRBLBASE  | RIRB Lower Base Address          | 00000000h | R/W, RO |
| 54h–57h        | RIRBUBASE  | RIRB Upper Base Address          | 00000000h | R/W     |
| 58h–59h        | RIRBWP     | RIRB Write Pointer               | 0000h     | R/W, RO |
| 5Ah–5Bh        | RINTCNT    | Response Interrupt Count         | 0000h     | R/W     |

**Table 1-2. Intel® High Definition Audio PCI Register Address Map (Intel® High Definition Audio D27:F0) (Sheet 2 of 4)**

| HDBAR + Offset | Mnemonic  | Register Name                                           | Default   | Access    |
|----------------|-----------|---------------------------------------------------------|-----------|-----------|
| 5Ch            | RIRBCTL   | RIRB Control                                            | 00h       | R/W       |
| 5Dh            | RIRBSTS   | RIRB Status                                             | 00h       | R/WC      |
| 5Eh            | RIRBSIZE  | RIRB Size                                               | 42h       | RO        |
| 60h–63h        | IC        | Immediate Command                                       | 00000000h | R/W       |
| 64h–67h        | IR        | Immediate Response                                      | 00000000h | RO        |
| 68h–69h        | IRS       | Immediate Command Status                                | 0000h     | R/W, R/WC |
| 70h–73h        | DPLBASE   | DMA Position Lower Base Address                         | 00000000h | R/W, RO   |
| 74h–77h        | DPUBASE   | DMA Position Upper Base Address                         | 00000000h | R/W       |
| 80–82h         | ISD0CTL   | Input Stream Descriptor 0 (ISD0) Control                | 040000h   | R/W, RO   |
| 83h            | ISD0STS   | ISD0 Status                                             | 00h       | R/WC, RO  |
| 84h–87h        | ISD0LPIB  | ISD0 Link Position in Buffer                            | 00000000h | RO        |
| 88h–8Bh        | ISD0CBL   | ISD0 Cyclic Buffer Length                               | 00000000h | R/W       |
| 8Ch–8Dh        | ISD0LVI   | ISD0 Last Valid Index                                   | 0000h     | R/W       |
| 8Eh–8Fh        | ISD0FIFOW | ISD0 FIFO Watermark                                     | 0004h     | R/W       |
| 90h–91h        | ISD0FIFOS | ISD0 FIFO Size                                          | 0077h     | RO        |
| 92h–93h        | ISD0FMT   | ISD0 Format                                             | 0000h     | R/W       |
| 98h–9Bh        | ISD0BDPL  | ISD0 Buffer Descriptor List Pointer-Lower Base Address  | 00000000h | R/W, RO   |
| 9Ch–9Fh        | ISD0BDPU  | ISD0 Buffer Description List Pointer-Upper Base Address | 00000000h | R/W       |
| A0h–A2h        | ISD1CTL   | Input Stream Descriptor 1 (ISD01) Control               | 040000h   | R/W, RO   |
| A3h            | ISD1STS   | ISD1 Status                                             | 00h       | R/WC, RO  |
| A4h–A7h        | ISD1LPIB  | ISD1 Link Position in Buffer                            | 00000000h | RO        |
| A8h–ABh        | ISD1CBL   | ISD1 Cyclic Buffer Length                               | 00000000h | R/W       |
| ACh–ADh        | ISD1LVI   | ISD1 Last Valid Index                                   | 0000h     | R/W       |
| AEh–AFh        | ISD1FIFOW | ISD1 FIFO Watermark                                     | 0004h     | R/W       |
| B0h–B1h        | ISD1FIFOS | ISD1 FIFO Size                                          | 0077h     | RO        |
| B2–B3h         | ISD1FMT   | ISD1 Format                                             | 0000h     | R/W       |
| B8–BBh         | ISD1BDPL  | ISD1 Buffer Descriptor List Pointer-Lower Base Address  | 00000000h | R/W, RO   |
| BCh–BFh        | ISD1BDPU  | ISD1 Buffer Description List Pointer-Upper Base Address | 00000000h | R/W       |
| C0h–C2h        | ISD2CTL   | Input Stream Descriptor 2 (ISD2) Control                | 040000h   | R/W, RO   |
| C3h            | ISD2STS   | ISD2 Status                                             | 00h       | R/WC, RO  |
| Ch4–C7h        | ISD2LPIB  | ISD2 Link Position in Buffer                            | 00000000h | RO        |
| C8h–CBh        | ISD2CBL   | ISD2 Cyclic Buffer Length                               | 00000000h | R/W       |
| CCh–CDh        | ISD2LVI   | ISD2 Last Valid Index                                   | 0000h     | R/W       |
| CEh–CFh        | ISD1FIFOW | ISD1 FIFO Watermark                                     | 0004h     | R/W       |

**Table 1-2. Intel® High Definition Audio PCI Register Address Map  
(Intel® High Definition Audio D27:F0) (Sheet 3 of 4)**

| HDBAR + Offset | Mnemonic  | Register Name                                           | Default   | Access   |
|----------------|-----------|---------------------------------------------------------|-----------|----------|
| D0h–D1h        | ISD2FIFOS | ISD2 FIFO Size                                          | 0077h     | RO       |
| D2h–D3h        | ISD2FMT   | ISD2 Format                                             | 0000h     | R/W      |
| D8h–DBh        | ISD2BDPL  | ISD2 Buffer Descriptor List Pointer-Lower Base Address  | 00000000h | R/W, RO  |
| DCh–DFh        | ISD2BDPU  | ISD2 Buffer Description List Pointer-Upper Base Address | 00000000h | R/W      |
| E0h–E2h        | ISD3CTL   | Input Stream Descriptor 3 (ISD3) Control                | 040000h   | R/W, RO  |
| E3h            | ISD3STS   | ISD3 Status                                             | 00h       | R/WC, RO |
| E4h–E7h        | ISD3LPIB  | ISD3 Link Position in Buffer                            | 00000000h | RO       |
| E8h–EBh        | ISD3CBL   | ISD3 Cyclic Buffer Length                               | 00000000h | R/W      |
| ECh–EDh        | ISD3LVI   | ISD3 Last Valid Index                                   | 0000h     | R/W      |
| EEh–EFh        | ISD3FIFOW | ISD3 FIFO Watermark                                     | 0004h     | R/W      |
| F0h–F1h        | ISD3FIFOS | ISD3 FIFO Size                                          | 0077h     | RO       |
| F2h–F3h        | ISD3FMT   | ISD3 Format                                             | 0000h     | R/W      |
| F8h–FBh        | ISD3BDPL  | ISD3 Buffer Descriptor List Pointer-Lower Base Address  | 00000000h | R/W, RO  |
| FCh–FFh        | ISD3BDPU  | ISD3 Buffer Description List Pointer-Upper Base Address | 00000000h | R/W      |
| 100h–102h      | OSD0CTL   | Output Stream Descriptor 0 (OSD0) Control               | 040000h   | R/W, RO  |
| 103h           | OSD0STS   | OSD0 Status                                             | 00h       | R/WC, RO |
| 104h–107h      | OSD0LPIB  | OSD0 Link Position in Buffer                            | 00000000h | RO       |
| 108h–10Bh      | OSD0CBL   | OSD0 Cyclic Buffer Length                               | 00000000h | R/W      |
| 10Ch–10Dh      | OSD0LVI   | OSD0 Last Valid Index                                   | 0000h     | R/W      |
| 10Eh–10Fh      | OSD0FIFOW | OSD0 FIFO Watermark                                     | 0004h     | R/W      |
| 110h–111h      | OSD0FIFOS | OSD0 FIFO Size                                          | 00BFh     | R/W      |
| 112–113h       | OSD0FMT   | OSD0 Format                                             | 0000h     | R/W      |
| 118h–11Bh      | OSD0BDPL  | OSD0 Buffer Descriptor List Pointer-Lower Base Address  | 00000000h | R/W, RO  |
| 11Ch–11Fh      | OSD0BDPU  | OSD0 Buffer Description List Pointer-Upper Base Address | 00000000h | R/W      |
| 120h–122h      | OSD1CTL   | Output Stream Descriptor 1 (OSD1) Control               | 040000h   | R/W, RO  |
| 123h           | OSD1STS   | OSD1 Status                                             | 00h       | R/WC, RO |
| 124h–127h      | OSD1LPIB  | OSD1 Link Position in Buffer                            | 00000000h | RO       |
| 128h–12Bh      | OSD1CBL   | OSD1 Cyclic Buffer Length                               | 00000000h | R/W      |
| 12Ch–12Dh      | OSD1LVI   | OSD1 Last Valid Index                                   | 0000h     | R/W      |
| 12Eh–12Fh      | OSD1FIFOW | OSD1 FIFO Watermark                                     | 0004h     | R/W      |
| 130h–131h      | OSD1FIFOS | OSD1 FIFO Size                                          | 00BFh     | R/W      |
| 132h–133h      | OSD1FMT   | OSD1 Format                                             | 0000h     | R/W      |



**Table 1-2. Intel® High Definition Audio PCI Register Address Map (Intel® High Definition Audio D27:F0) (Sheet 4 of 4)**

| HDBAR + Offset | Mnemonic  | Register Name                                           | Default   | Access   |
|----------------|-----------|---------------------------------------------------------|-----------|----------|
| 138h–13Bh      | OSD1BDPL  | OSD1 Buffer Descriptor List Pointer-Lower Base Address  | 00000000h | R/W, RO  |
| 13Ch–13Fh      | OSD1BDPU  | OSD1 Buffer Description List Pointer-Upper Base Address | 00000000h | R/W      |
| 140h–142h      | OSD2CTL   | Output Stream Descriptor 2 (OSD2) Control               | 040000h   | R/W, RO  |
| 143h           | OSD2STS   | OSD2 Status                                             | 00h       | R/WC, RO |
| 144h–147h      | OSD2LPIB  | OSD2 Link Position in Buffer                            | 00000000h | RO       |
| 148h–14Bh      | OSD2CBL   | OSD2 Cyclic Buffer Length                               | 00000000h | R/W      |
| 14Ch–14Dh      | OSD2LVI   | OSD2 Last Valid Index                                   | 0000h     | R/W      |
| 14Eh–14Fh      | OSD2FIFOW | OSD2 FIFO Watermark                                     | 0004h     | R/W      |
| 150h–151h      | OSD2FIFOS | OSD2 FIFO Size                                          | 00BFh     | R/W      |
| 152h–153h      | OSD2FMT   | OSD2 Format                                             | 0000h     | R/W      |
| 158h–15Bh      | OSD2BDPL  | OSD2 Buffer Descriptor List Pointer-Lower Base Address  | 00000000h | R/W, RO  |
| 15Ch–15Fh      | OSD2BDPU  | OSD2 Buffer Description List Pointer-Upper Base Address | 00000000h | R/W      |
| 160h–162h      | OSD3CTL   | Output Stream Descriptor 3 (OSD3) Control               | 040000h   | R/W, RO  |
| 163h           | OSD3STS   | OSD3 Status                                             | 00h       | R/WC, RO |
| 164h–167h      | OSD3LPIB  | OSD3 Link Position in Buffer                            | 00000000h | RO       |
| 168h–16Bh      | OSD3CBL   | OSD3 Cyclic Buffer Length                               | 00000000h | R/W      |
| 16Ch–16Dh      | OSD3LVI   | OSD3 Last Valid Index                                   | 0000h     | R/W      |
| 16Eh–16Fh      | OSD3FIFOW | OSD3 FIFO Watermark                                     | 0004h     | R/W      |
| 170h–171h      | OSD3FIFOS | OSD3 FIFO Size                                          | 00BFh     | R/W      |
| 172h–173h      | OSD3FMT   | OSD3 Format                                             | 0000h     | R/W      |
| 178h–17Bh      | OSD3BDPL  | OSD3 Buffer Descriptor List Pointer-Lower Base Address  | 00000000h | R/W, RO  |
| 17Ch–17Fh      | OSD3BDPU  | OSD3 Buffer Description List Pointer-Upper Base Address | 00000000h | R/W      |

### 1.2.1 GCAP—Global Capabilities Register (Intel® High Definition Audio Controller—D27:F0)

Memory Address: HDBAR + 00h                      Attribute:                      RO  
 Default Value:    4401h                              Size:                              16 bits

| Bit   | Description                                                                                                                                                                                                        |
|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:12 | Number of Output Stream Supported — RO. Hardwired to 0100b indicating that the ICH7 Intel® High Definition Audio controller supports 4 output streams.                                                             |
| 11:8  | Number of Input Stream Supported — RO. Hardwired to 0100b indicating that the ICH7 Intel High Definition Audio controller supports 4 input streams.                                                                |
| 7:3   | Number of Bidirectional Stream Supported — RO. Hardwired to 0 indicating that the ICH7 Intel High Definition Audio controller supports 0 bidirectional stream.                                                     |
| 2     | Reserved.                                                                                                                                                                                                          |
| 1     | Number of Serial Data Out Signals — RO. Hardwired to 0 indicating that the ICH7 Intel High Definition Audio controller supports 1 serial data output signal.                                                       |
| 0     | 64-bit Address Supported — RO. Hardwired to 1b indicating that the ICH7 Intel High Definition Audio controller supports 64-bit addressing for BDL addresses, data buffer addressees, and command buffer addresses. |

### 1.2.2 VMIN—Minor Version Register (Intel® High Definition Audio Controller—D27:F0)

Memory Address: HDBAR + 02h                      Attribute:                      RO  
 Default Value:    00h                                              Size:                                              8 bits

| Bit | Description                                                                                                                                              |
|-----|----------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:0 | Minor Version — RO. Hardwired to 0 indicating that the Intel® ICH7 supports minor revision number 00h of the Intel® High Definition Audio specification. |

### 1.2.3 VMAJ—Major Version Register (Intel® High Definition Audio Controller—D27:F0)

Memory Address: HDBAR + 03h                      Attribute:                      RO  
 Default Value:    01h                                              Size:                                              8 bits

| Bit | Description                                                                                                                                              |
|-----|----------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:0 | Major Version — RO. Hardwired to 01h indicating that the Intel® ICH7 supports major revision number 1 of the Intel® High Definition Audio specification. |





## 1.2.6 GCTL—Global Control Register (Intel® High Definition Audio Controller—D27:F0)

Memory Address: HDBAR + 08h  
Default Value: 00000000h

Attribute: R/W  
Size: 32 bits

| Bit  | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
|------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:9 | Reserved.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
| 8    | <p><b>Accept Unsolicited Response Enable</b> — R/W.</p> <p>0 = Unsolicited responses from the codecs are not accepted.<br/>1 = Unsolicited response from the codecs are accepted by the controller and placed into the Response Input Ring Buffer.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| 7:2  | Reserved.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
| 1    | <p><b>Flush Control</b> — R/W.</p> <p>0 = Flush <b>Not</b> in progress.<br/>1 = Writing a 1 to this bit initiates a flush. When the flush completion is received by the controller, hardware sets the Flush Status bit and clears this Flush Control bit. Before a flush cycle is initiated, the DMA Position Buffer must be programmed with a valid memory address by software, but the DMA Position Buffer bit 0 needs not be set to enable the position reporting mechanism. Also, all streams must be stopped (the associated RUN bit must be 0).</p> <p>When the flush is initiated, the controller will flush the pipelines to memory to ensure that the hardware is ready to transition to a D3 state. Setting this bit is not a critical step in the power state transition if the content of the FIFOs is not critical.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
| 0    | <p><b>Controller Reset #</b> — R/W.</p> <p>0 = Writing a 0 to this bit causes the Intel® High Definition Audio controller to be reset. All state machines, FIFOs, and non-resume well memory mapped configuration registers (not PCI configuration registers) in the controller will be reset. The Intel High Definition Audio link RESET# signal will be asserted, and all other link signals will be driven to their default values. After the hardware has completed sequencing into the reset state, it will report a 0 in this bit. Software must read a 0 from this bit to verify the controller is in reset.</p> <p>1 = Writing a 1 to this bit causes the controller to exit its reset state and deassert the Intel High Definition Audio link RESET# signal. Software is responsible for setting/clearing this bit such that the minimum Intel High Definition Audio link RESET# signal assertion pulse width specification is met. When the controller hardware is ready to begin operation, it will report a 1 in this bit. Software must read a 1 from this bit before accessing any controller registers. This bit defaults to a 0 after Hardware reset, therefore, software needs to write a 1 to this bit to begin operation.</p> <p><b>NOTES:</b></p> <ol style="list-style-type: none"> <li>1. The CORB/RIRB RUN bits and all stream RUN bits must be verified cleared to 0 before writing a 0 to this bit in order to assure a clean re-start.</li> <li>2. When setting or clearing this bit, software must ensure that minimum link timing requirements (minimum RESET# assertion time, etc.) are met.</li> <li>3. When this bit is 0 indicating that the controller is in reset, writes to all Intel High Definition Audio memory mapped registers are ignored as if the device is not present. The only exception is this register itself. The Global Control register is write-able as a DWord, Word, or Byte even when CRST# (this bit) is 0 if the byte enable for the byte containing the CRST# bit (Byte Enable 0) is active. If Byte Enable 0 is not active, writes to the Global Control register will be ignored when CRST# is 0. When CRST# is 0, reads to Intel High Definition Audio memory mapped registers will return their default value except for registers that are not reset with PLTRST# or on a D3<sub>HOT</sub> to D0 transition.</li> </ol> |



## 1.2.9 GSTS—Global Status Register (Intel® High Definition Audio Controller—D27:F0)

Memory Address: HDBAR + 10h  
Default Value: 0000h

Attribute: R/WC  
Size: 16 bits

| Bit  | Description                                                                                                                                                                                                                                                                                                                                                           |
|------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:4 | Reserved.                                                                                                                                                                                                                                                                                                                                                             |
| 3    | Reserved                                                                                                                                                                                                                                                                                                                                                              |
| 2    | Reserved                                                                                                                                                                                                                                                                                                                                                              |
| 1    | <p><b>Flush Status</b> — R/WC.</p> <p>0 = Flush <b>not</b> completed<br/>1 = This bit is set to 1 by hardware to indicate that the flush cycle initiated when the Flush Control bit (HDBAR + 08h, bit 1) was set has completed.</p> <p><b>NOTE:</b> Software must write a 1 to clear this bit before the next time the Flush Control bit is set to clear the bit.</p> |
| 0    | Reserved.                                                                                                                                                                                                                                                                                                                                                             |

## 1.2.10 OUTSTRMPAY—Output Stream Payload Capability (Intel® High Definition Audio Controller—D27:F0)

Memory Address: HDBAR + 18h  
Default Value: 0030h

Attribute: RO  
Size: 16 bits

| Bit   | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:14 | <p><b>Output FIFO Padding Type (OPADTYPE)</b>— RO: This field indicates how the controller pads the samples in the controller's buffer (FIFO). Controllers may not pad at all or may pad to byte or memory container sizes.</p> <p>0h = Controller pads all samples to bytes<br/>1h = Reserved<br/>2h = Controller pads to memory container size<br/>3h = Controller does not pad and uses samples directly</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
| 13:0  | <p><b>Output Stream Payload Capability (OUTSTRMPAY)</b>— RO: This field indicates maximum number of words per frame for any single output stream. This measurement is in 16 bit word quantities per 48 kHz frame. The maximum supported is 48 Words (96B); therefore, a value of 30h is reported in this register. The value does not specify the number of words actually transmitted in the frame, but is the size of the data in the controller buffer (FIFO) after the samples are padded as specified by OPADTYPE. Thus, to compute the supported streams, each sample is padded according to OPADTYPE and then multiplied by the number of channels and samples per frame. If this computed value is larger than OUTSTRMPAY, then that stream is not supported. The value specified is not affected by striping.</p> <p>Software must ensure that a format that would cause more Words per frame than indicated is not programmed into the Output Stream Descriptor Register.</p> <p>The value may be larger than the OUTPAY register value in some cases.</p> |



## 1.2.12 INTCTL—Interrupt Control Register (Intel® High Definition Audio Controller—D27:F0)

Memory Address: HDBAR + 20h  
Default Value: 00000000h

Attribute: R/W  
Size: 32 bits

| Bit  | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
|------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31   | <p><b>Global Interrupt Enable (GIE)</b> — R/W. Global bit to enable device interrupt generation.</p> <p>0 = Disable.<br/>1 = Enable. The Intel® High Definition Audio function is enabled to generate an interrupt. This control is in addition to any bits in the bus specific address space, such as the Interrupt Enable bit in the PCI configuration space.</p> <p><b>NOTE:</b> This bit is not affected by the D3<sub>HOT</sub> to D0 transition.</p>                                                                                                                                                                                                                                                                                                                                                                          |
| 30   | <p><b>Controller Interrupt Enable (CIE)</b> — R/W. Enables the general interrupt for controller functions.</p> <p>0 = Disable.<br/>1 = Enable. The controller generates an interrupt when the corresponding status bit gets set due to a Response Interrupt, a Response Buffer Overrun, and State Change events.</p> <p><b>NOTE:</b> This bit is not affected by the D3<sub>HOT</sub> to D0 transition.</p>                                                                                                                                                                                                                                                                                                                                                                                                                         |
| 29:8 | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
| 7:0  | <p><b>Stream Interrupt Enable (SIE)</b> — R/W.</p> <p>0 = Disable.<br/>1 = Enable. When set to 1, the individual streams are enabled to generate an interrupt when the corresponding status bits get set.</p> <p>A stream interrupt will be caused as a result of a buffer with IOC = 1 in the BDL entry being completed, or as a result of a FIFO error (underrun or overrun) occurring. Control over the generation of each of these sources is in the associated Stream Descriptor.</p> <p>The streams are numbered and the SIE bits assigned sequentially, based on their order in the register set.</p> <p>Bit 0: input stream 1<br/>Bit 1: input stream 2<br/>Bit 2: input stream 3<br/>Bit 3: input stream 4<br/>Bit 4: output stream 1<br/>Bit 5: output stream 2<br/>Bit 6: output stream 3<br/>Bit 7: output stream 4</p> |



### 1.2.15 SSYNC—Stream Synchronization Register (Intel® High Definition Audio Controller—D27:F0)

Memory Address: HDBAR + 34h  
Default Value: 00000000h

Attribute: R/W  
Size: 32 bits

| Bit  | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
|------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:8 | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
| 7:0  | <p><b>Stream Synchronization (SSYNC) — R/W.</b></p> <p>0 = Data is <b>Not</b> blocked from being sent on or received from the link<br/>1 = The set bits block data from being sent on or received from the link. Each bit controls the associated stream descriptor (i.e., bit 0 corresponds to the first stream descriptor, etc.)</p> <p>To synchronously start a set of DMA engines, these bits are first set to 1. The RUN bits for the associated stream descriptors are then set to 1 to start the DMA engines. When all streams are ready (FIFORDY =1), the associated SSYNC bits can all be set to 0 at the same time, and transmission or reception of bits to or from the link will begin together at the start of the next full link frame.</p> <p>To synchronously stop the streams, first these bits are set, and then the individual RUN bits in the stream descriptor are cleared by software.</p> <p>If synchronization is not desired, these bits may be left as 0, and the stream will simply begin running normally when the stream's RUN bit is set.</p> <p>The streams are numbered and the SIE bits assigned sequentially, based on their order in the register set.</p> <p>Bit 0: input stream 1<br/>Bit 1: input stream 2<br/>Bit 2: input stream 3<br/>Bit 3: input stream 4<br/>Bit 4: output stream 1<br/>Bit 5: output stream 2<br/>Bit 6: output stream 3<br/>Bit 7: output stream 4</p> |

### 1.2.16 CORBLBASE—CORB Lower Base Address Register (Intel® High Definition Audio Controller—D27:F0)

Memory Address: HDBAR + 40h  
Default Value: 00000000h

Attribute: R/W, RO  
Size: 32 bits

| Bit  | Description                                                                                                                                                                                                                                                              |
|------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:7 | <b>CORB Lower Base Address — R/W.</b> Lower address of the Command Output Ring Buffer, allowing the CORB base address to be assigned on any 128-B boundary. This register field must not be written when the DMA engine is running or the DMA transfer may be corrupted. |
| 6:0  | <b>CORB Lower Base Unimplemented Bits — RO.</b> Hardwired to 0. This requires the CORB to be allocated with 128B granularity to allow for cache line fetch optimizations.                                                                                                |





## 1.2.20 CORBCTL—CORB Control Register (Intel® High Definition Audio Controller—D27:F0)

Memory Address: HDBAR + 4Ch                      Attribute:                      R/W  
 Default Value:    00h                                      Size:                                8 bits

| Bit | Description                                                                                                                                                                                                                                                                                                                   |
|-----|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:2 | Reserved.                                                                                                                                                                                                                                                                                                                     |
| 1   | <b>Enable CORB DMA Engine</b> — R/W. After software writes a 0 to this bit, the hardware may not stop immediately. The hardware will physically update the bit to 0 when the DMA engine is truly stopped. Software must read a 0 from this bit to verify that the DMA engine is truly stopped.<br>0 = DMA stop<br>1 = DMA run |
| 0   | <b>CORB Memory Error Interrupt Enable</b> — R/W.<br>0 = Disable.<br>1 = Enable. The controller will generate an interrupt if the CMEI status bit (HDBAR + 4Dh: bit 0) is set.                                                                                                                                                 |

## 1.2.21 CORBST—CORB Status Register (Intel® High Definition Audio Controller—D27:F0)

Memory Address: HDBAR + 4Dh                      Attribute:                      R/WC  
 Default Value:    00h                                      Size:                                8 bits

| Bit | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
|-----|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:1 | Reserved.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
| 0   | <b>CORB Memory Error Indication (CMEI)</b> — R/WC.<br>0 = Error <b>Not</b> detected.<br>1 = The controller has detected an error in the path way between the controller and memory. This may be an ECC bit error or any other type of detectable data error which renders the command data fetched invalid.<br><br><b>NOTE:</b> Software can clear this bit by writing a 1 to it. However, this type of error leaves the audio subsystem in an un-viable state and typically requires a controller reset by writing a 0 to the Controller Reset # bit (HDBAR + 08h: bit 0). |

## 1.2.22 CORBSIZE—CORB Size Register Intel® High Definition Audio Controller—D27:F0)

Memory Address: HDBAR + 4Eh                      Attribute:                      RO  
 Default Value:    42h                                      Size:                                8 bits

| Bit | Description                                                                                                                   |
|-----|-------------------------------------------------------------------------------------------------------------------------------|
| 7:4 | CORB Size Capability — RO. Hardwired to 0100b indicating that the ICH7 only supports a CORB size of 256 CORB entries (1024B). |
| 3:2 | Reserved.                                                                                                                     |
| 1:0 | CORB Size — RO. Hardwired to 10b which sets the CORB size to 256 entries (1024B).                                             |



## 1.2.26 RINTCNT—Response Interrupt Count Register (Intel® High Definition Audio Controller—D27:F0)

Memory Address: HDBAR + 5Ah  
Default Value: 0000h

Attribute: R/W  
Size: 16 bits

| Bit  | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
|------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:8 | Reserved.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
| 31:0 | <p><b>N Response Interrupt Count</b> — R/W.<br/>0000 0001b = 1 response sent to RIRB<br/>.....<br/>1111 1111b = 255 responses sent to RIRB<br/>0000 0000b = 256 responses sent to RIRB<br/>The DMA engine should be stopped when changing this field or else an interrupt may be lost.<br/>Note that each response occupies 2 DWords in the RIRB.<br/>This is compared to the total number of responses that have been returned, as opposed to the number of frames in which there were responses. If more than one codec responds in one frame, then the count is increased by the number of responses received in the frame.</p> |

## 1.2.27 RIRBCTL—RIRB Control Register (Intel® High Definition Audio Controller—D27:F0)

Memory Address: HDBAR + 5Ch  
Default Value: 00h

Attribute: R/W  
Size: 8 bits

| Bit | Description                                                                                                                                                                                                                                                                                                                            |
|-----|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:3 | Reserved.                                                                                                                                                                                                                                                                                                                              |
| 2   | <p><b>Response Overrun Interrupt Control</b> — R/W.<br/>0 = Hardware will <b>Not</b> generated an interrupt as described below.<br/>1 = The hardware will generate an interrupt when the Response Overrun Interrupt Status bit (HDBAR + 5Dh: bit 2) is set.</p>                                                                        |
| 1   | <p><b>Enable RIRB DMA Engine</b> — R/W. After software writes a 0 to this bit, the hardware may not stop immediately. The hardware will physically update the bit to 0 when the DMA engine is truly stopped. Software must read a 0 from this bit to verify that the DMA engine is truly stopped.<br/>0 = DMA stop<br/>1 = DMA run</p> |
| 0   | <p><b>Response Interrupt Control</b> — R/W.<br/>0 = Disable Interrupt<br/>1 = Generate an interrupt after N number of responses are sent to the RIRB buffer OR when an empty Response slot is encountered on all SDI[x] inputs (whichever occurs first). The N counter is reset when the interrupt is generated.</p>                   |



### 1.2.31 IR—Immediate Response Register (Intel® High Definition Audio Controller—D27:F0)

Memory Address: HDBAR + 64h                      Attribute:                      RO  
 Default Value:    00000000h                      Size:                            32 bits

| Bit  | Description                                                                                                                                                                                                                                                                                                                                                                          |
|------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | <p>Immediate Response Read (IRR) — RO. This register contains the response received from a codec resulting from a command sent via the Immediate Command mechanism.</p> <p>If multiple codecs responded in the same time, there is no assurance as to which response will be latched. Therefore, broadcast-type commands must not be issued via the Immediate Command mechanism.</p> |

### 1.2.32 IRS—Immediate Command Status Register (Intel® High Definition Audio Controller—D27:F0)

Memory Address: HDBAR + 68h                      Attribute:                      R/W, R/WC  
 Default Value:    0000h                                              Size:                            16 bits

| Bit  | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
|------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:2 | Reserved.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
| 1    | <p><b>Immediate Result Valid (IRV)</b> — R/WC.</p> <p>0 = Software must clear this bit by writing a 1 to it before issuing a new command so that the software may determine when a new response has arrived.</p> <p>1 = Set to 1 by hardware when a new response is latched into the Immediate Response register (HDBAR + 64). This is a status flag indicating that software may read the response from the Immediate Response register.</p>                                                                                                                                                                                                                                                   |
| 0    | <p><b>Immediate Command Busy (ICB)</b> — R/W. When this bit is read as 0, it indicates that a new command may be issued using the Immediate Command mechanism. When this bit transitions from 0-to-1 (via software writing a 1), the controller issues the command currently stored in the Immediate Command register to the codec over the link. When the corresponding response is latched into the Immediate Response register, the controller hardware sets the IRV flag and clears the ICB bit back to 0.</p> <p><b>NOTE:</b> An Immediate Command must not be issued while the CORB/RIRB mechanism is operating, otherwise the responses conflict. This must be enforced by software.</p> |



| Bit   | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 23:20 | <p><b>Stream Number</b> — R/W. This value reflects the Tag associated with the data being transferred on the link.</p> <p>When data controlled by this descriptor is sent out over the link, it will have its stream number encoded on the SYNC signal.</p> <p>When an input stream is detected on any of the SDI signals that match this value, the data samples are loaded into FIFO associated with this descriptor.</p> <p>Note that while a single SDI input may contain data from more than one stream number, two different SDI inputs may not be configured with the same stream number.</p> <p>0000 = Reserved<br/>0001 = Stream 1<br/>.....<br/>1110 = Stream 14<br/>1111 = Stream 15</p>             |
| 19    | <p><b>Bidirectional Direction Control</b> — RO. This bit is only meaningful for bidirectional streams; therefore, this bit is hardwired to 0.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
| 18    | <p><b>Traffic Priority</b> — RO. Hardwired to 1 indicating that all streams will use VC1 if it is enabled through the PCI Express* registers.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
| 17:16 | <p><b>Stripe Control</b> — RO. This bit is only meaningful for input streams; therefore, this bit is hardwired to 0.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
| 15:5  | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
| 4     | <p><b>Descriptor Error Interrupt Enable</b> — R/W.<br/>0 = Disable<br/>1 = An interrupt is generated when the Descriptor Error Status bit is set.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
| 3     | <p><b>FIFO Error Interrupt Enable</b> — R/W.<br/>0 = Disable.<br/>1 = Enable. This bit controls whether the occurrence of a FIFO error (overflow for input or underflow for output) will cause an interrupt or not. If this bit is not set, bit 3 in the Status register will be set, but the interrupt will not occur. Either way, the samples will be dropped.</p>                                                                                                                                                                                                                                                                                                                                            |
| 2     | <p><b>Interrupt on Completion Enable</b> — R/W.<br/>0 = Disable.<br/>1 = Enable. This bit controls whether or not an interrupt occurs when a buffer completes with the IOC bit set in its descriptor. If this bit is not set, bit 2 in the Status register will be set, but the interrupt will not occur.</p>                                                                                                                                                                                                                                                                                                                                                                                                   |
| 1     | <p><b>Stream Run (RUN)</b> — R/W.<br/>0 = Disable. The DMA engine associated with this input stream will be disabled. The hardware will report a 0 in this bit when the DMA engine is actually stopped. Software must read a 0 from this bit before modifying related control registers or restarting the DMA engine.<br/>1 = Enable. The DMA engine associated with this input stream will be enabled to transfer data from the FIFO to the main memory. The SSYNC bit must also be cleared in order for the DMA engine to run. For output streams, the cadence generator is reset whenever the RUN bit is set.</p>                                                                                            |
| 0     | <p><b>Stream Reset (SRST)</b> — R/W.<br/>0 = Writing a 0 causes the corresponding stream to exit reset. When the stream hardware is ready to begin operation, it will report a 0 in this bit. Software must read a 0 from this bit before accessing any of the stream registers.<br/>1 = Writing a 1 causes the corresponding stream to be reset. The Stream Descriptor registers (except the SRST bit itself) and FIFO's for the corresponding stream are reset. After the stream hardware has completed sequencing into the reset state, it will report a 1 in this bit. Software must read a 1 from this bit to verify that the stream is in reset. The RUN bit must be cleared before SRST is asserted.</p> |



### 1.2.36 SDSTS—Stream Descriptor Status Register (Intel® High Definition Audio Controller—D27:F0)

Memory Address: Input Stream[0]: HDBAR + 83h                      Attribute: R/WC, RO  
 Input Stream[1]: HDBAR + A3h  
 Input Stream[2]: HDBAR + C3h  
 Input Stream[3]: HDBAR + E3h  
 Output Stream[0]: HDBAR + 103h  
 Output Stream[1]: HDBAR + 123h  
 Output Stream[2]: HDBAR + 143h  
 Output Stream[3]: HDBAR + 163h

Default Value: 00h                                                              Size: 8 bits

| Bit | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
|-----|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:6 | Reserved.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
| 5   | <p>FIFO Ready (FIFORDY) — RO.</p> <p>For output streams, the controller hardware will set this bit to 1 while the output DMA FIFO contains enough data to maintain the stream on the link. This bit defaults to 0 on reset because the FIFO is cleared on a reset.</p> <p>For input streams, the controller hardware will set this bit to 1 when a valid descriptor is loaded and the engine is ready for the RUN bit to be set.</p>                                                                                                                                                                                                                   |
| 4   | <p><b>Descriptor Error</b> — R/WC.</p> <p>0 = No error detected.<br/>           1 = A serious error occurred during the fetch of a descriptor. This could be a result of a Master Abort, a parity or ECC error on the bus, or any other error which renders the current Buffer Descriptor or Buffer Descriptor list useless. This error is treated as a fatal stream error, as the stream cannot continue running. The RUN bit will be cleared and the stream will stop.</p> <p><b>NOTE:</b> Software may attempt to restart the stream engine after addressing the cause of the error and writing a 1 to this bit to clear it.</p>                    |
| 3   | <p><b>FIFO Error</b> — R/WC. The bit is cleared by writing a 1 to it.</p> <p>0 = No error detected.<br/>           1 = FIFO error occurred. This bit is set even if an interrupt is not enabled.</p> <p>For an input stream, this indicates a FIFO overrun occurring while the RUN bit is set. When this happens, the FIFO pointers do not increment and the incoming data is not written into the FIFO, thereby being lost.</p> <p>For an output stream, this indicates a FIFO underrun when there are still buffers to send. The hardware should not transmit anything on the link for the associated stream if there is not valid data to send.</p> |
| 2   | <p><b>Buffer Completion Interrupt Status</b> — R/WC.</p> <p>0 = Last sample of a buffer has <b>Not</b> been processed as described below.<br/>           1 = Set to 1 by the hardware after the last sample of a buffer has been processed, AND if the Interrupt on Completion bit is set in the command byte of the buffer descriptor. It remains active until software clears it by writing a 1 to it.</p>                                                                                                                                                                                                                                           |
| 1:0 | Reserved.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |



### 1.2.39 SDLVI—Stream Descriptor Last Valid Index Register (Intel® High Definition Audio Controller—D27:F0)

Memory Address: Input Stream[0]: HDBAR + 8Ch                      Attribute: R/W  
 Input Stream[1]: HDBAR + ACh  
 Input Stream[2]: HDBAR + CCh  
 Input Stream[3]: HDBAR + ECh  
 Output Stream[0]: HDBAR + 10Ch  
 Output Stream[1]: HDBAR + 12Ch  
 Output Stream[2]: HDBAR + 14Ch  
 Output Stream[3]: HDBAR + 16Ch

Default Value: 0000h                                              Size: 16 bits

| Bit  | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
|------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:8 | Reserved.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
| 7:0  | <p><b>Last Valid Index</b> — R/W. The value written to this register indicates the index for the last valid Buffer Descriptor in BD. After the controller has processed this descriptor, it will wrap back to the first descriptor in the list and continue processing.</p> <p>This field must be at least 1 (i.e., there must be at least 2 valid entries in the buffer descriptor list before DMA operations can begin).</p> <p>This value should only be modified when the RUN bit is 0.</p> |

### 1.2.40 SDFIFOW—Stream Descriptor FIFO Watermark Register (Intel® High Definition Audio Controller—D27:F0)

Memory Address: Input Stream[0]: HDBAR + 8Eh                      Attribute: R/W  
 Input Stream[1]: HDBAR + AEh  
 Input Stream[2]: HDBAR + CEh  
 Input Stream[3]: HDBAR + EEh  
 Output Stream[0]: HDBAR + 10Eh  
 Output Stream[1]: HDBAR + 12Eh  
 Output Stream[2]: HDBAR + 14Eh  
 Output Stream[3]: HDBAR + 16Eh

Default Value: 0004h                                              Size: 16 bits

| Bit  | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
|------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:3 | Reserved.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
| 2:0  | <p><b>FIFO Watermark (FIFOW)</b> — R/W. Indicates the minimum number of bytes accumulated/free in the FIFO before the controller will start a fetch/eviction of data.</p> <p>010 = 8B<br/>                 011 = 16B<br/>                 100 = 32B (Default)<br/>                 Others = Unsupported</p> <p><b>NOTES:</b></p> <ol style="list-style-type: none"> <li>When the bit field is programmed to an unsupported size, the hardware sets itself to the default value.</li> <li>Software must read the bit field to test if the value is supported after setting the bit field.</li> </ol> |



### 1.2.41 SDFIFOS—Stream Descriptor FIFO Size Register (Intel® High Definition Audio Controller—D27:F0)

Memory Address: Input Stream[0]: HDBAR + 90h      Attribute: Input: RO  
 Input Stream[1]: HDBAR + B0h                      Output: R/W  
 Input Stream[2]: HDBAR + D0h  
 Input Stream[3]: HDBAR + F0h  
 Output Stream[0]: HDBAR + 110h  
 Output Stream[1]: HDBAR + 130h  
 Output Stream[2]: HDBAR + 150h  
 Output Stream[3]: HDBAR + 170h

Default Value: Input Stream: 0077h                      Size: 16 bits  
 Output Stream: 00BFh

| Bit        | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |       |                |           |                                         |           |                                         |           |                                         |            |                                         |            |                                 |            |                           |       |               |            |                             |            |                          |
|------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------|----------------|-----------|-----------------------------------------|-----------|-----------------------------------------|-----------|-----------------------------------------|------------|-----------------------------------------|------------|---------------------------------|------------|---------------------------|-------|---------------|------------|-----------------------------|------------|--------------------------|
| 15:8       | Reserved.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |       |                |           |                                         |           |                                         |           |                                         |            |                                         |            |                                 |            |                           |       |               |            |                             |            |                          |
| 7:0        | <p><b>FIFO Size</b> — RO (Input stream), R/W (Output stream). Indicates the maximum number of bytes that could be fetched by the controller at one time. This is the maximum number of bytes that may have been DMA'd into memory but not yet transmitted on the link, and is also the maximum possible value that the PICB count will increase by at one time.</p> <p>The value in this field is different for input and output streams. It is also dependent on the Bits per Samples setting for the corresponding stream. Following are the values read/written from/to this register for input and output streams, and for non-padded and padded bit formats:</p> <p><i>Output Stream R/W value:</i></p> <table border="1"> <thead> <tr> <th>Value</th> <th>Output Streams</th> </tr> </thead> <tbody> <tr> <td>0Fh = 16B</td> <td>8, 16, 20, 24, or 32 bit Output Streams</td> </tr> <tr> <td>1Fh = 32B</td> <td>8, 16, 20, 24, or 32 bit Output Streams</td> </tr> <tr> <td>3Fh = 64B</td> <td>8, 16, 20, 24, or 32 bit Output Streams</td> </tr> <tr> <td>7Fh = 128B</td> <td>8, 16, 20, 24, or 32 bit Output Streams</td> </tr> <tr> <td>BFh = 192B</td> <td>8, 16, or 32 bit Output Streams</td> </tr> <tr> <td>FFh = 256B</td> <td>20, 24 bit Output Streams</td> </tr> </tbody> </table> <p><b>NOTES:</b></p> <ol style="list-style-type: none"> <li>All other values not listed are not supported.</li> <li>When the output stream is programmed to an unsupported size, the hardware sets itself to the default value (BFh).</li> <li>Software must read the bit field to test if the value is supported after setting the bit field.</li> </ol> <p><i>Input Stream RO value:</i></p> <table border="1"> <thead> <tr> <th>Value</th> <th>Input Streams</th> </tr> </thead> <tbody> <tr> <td>77h = 120B</td> <td>8, 16, 32 bit Input Streams</td> </tr> <tr> <td>9Fh = 160B</td> <td>20, 24 bit Input Streams</td> </tr> </tbody> </table> <p><b>NOTE:</b> The default value is different for input and output streams, and reflects the default state of the BITS fields (in Stream Descriptor Format registers) for the corresponding stream.</p> | Value | Output Streams | 0Fh = 16B | 8, 16, 20, 24, or 32 bit Output Streams | 1Fh = 32B | 8, 16, 20, 24, or 32 bit Output Streams | 3Fh = 64B | 8, 16, 20, 24, or 32 bit Output Streams | 7Fh = 128B | 8, 16, 20, 24, or 32 bit Output Streams | BFh = 192B | 8, 16, or 32 bit Output Streams | FFh = 256B | 20, 24 bit Output Streams | Value | Input Streams | 77h = 120B | 8, 16, 32 bit Input Streams | 9Fh = 160B | 20, 24 bit Input Streams |
| Value      | Output Streams                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |       |                |           |                                         |           |                                         |           |                                         |            |                                         |            |                                 |            |                           |       |               |            |                             |            |                          |
| 0Fh = 16B  | 8, 16, 20, 24, or 32 bit Output Streams                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |       |                |           |                                         |           |                                         |           |                                         |            |                                         |            |                                 |            |                           |       |               |            |                             |            |                          |
| 1Fh = 32B  | 8, 16, 20, 24, or 32 bit Output Streams                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |       |                |           |                                         |           |                                         |           |                                         |            |                                         |            |                                 |            |                           |       |               |            |                             |            |                          |
| 3Fh = 64B  | 8, 16, 20, 24, or 32 bit Output Streams                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |       |                |           |                                         |           |                                         |           |                                         |            |                                         |            |                                 |            |                           |       |               |            |                             |            |                          |
| 7Fh = 128B | 8, 16, 20, 24, or 32 bit Output Streams                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |       |                |           |                                         |           |                                         |           |                                         |            |                                         |            |                                 |            |                           |       |               |            |                             |            |                          |
| BFh = 192B | 8, 16, or 32 bit Output Streams                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |       |                |           |                                         |           |                                         |           |                                         |            |                                         |            |                                 |            |                           |       |               |            |                             |            |                          |
| FFh = 256B | 20, 24 bit Output Streams                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |       |                |           |                                         |           |                                         |           |                                         |            |                                         |            |                                 |            |                           |       |               |            |                             |            |                          |
| Value      | Input Streams                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |       |                |           |                                         |           |                                         |           |                                         |            |                                         |            |                                 |            |                           |       |               |            |                             |            |                          |
| 77h = 120B | 8, 16, 32 bit Input Streams                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |       |                |           |                                         |           |                                         |           |                                         |            |                                         |            |                                 |            |                           |       |               |            |                             |            |                          |
| 9Fh = 160B | 20, 24 bit Input Streams                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |       |                |           |                                         |           |                                         |           |                                         |            |                                         |            |                                 |            |                           |       |               |            |                             |            |                          |



## 1.2.42 SDFMT—Stream Descriptor Format Register (Intel® High Definition Audio Controller—D27:F0)

Memory Address: Input Stream[0]: HDBAR + 92h      Attribute: R/W  
 Input Stream[1]: HDBAR + B2h  
 Input Stream[2]: HDBAR + D2h  
 Input Stream[3]: HDBAR + F2h  
 Output Stream[0]: HDBAR + 112h  
 Output Stream[1]: HDBAR + 132h  
 Output Stream[2]: HDBAR + 152h  
 Output Stream[3]: HDBAR + 172h

Default Value: 0000h      Size: 16 bits

| Bit   | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15    | Reserved.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
| 14    | <b>Sample Base Rate</b> — R/W<br>0 = 48 kHz<br>1 = 44.1 kHz                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
| 13:11 | <b>Sample Base Rate Multiple</b> — R/W<br>000 = 48 kHz, 44.1 kHz or less<br>001 = x2 (96 kHz, 88.2 kHz, 32 kHz)<br>010 = x3 (144 kHz)<br>011 = x4 (192 kHz, 176.4 kHz)<br>Others = Reserved.                                                                                                                                                                                                                                                                                                                                                   |
| 10:8  | <b>Sample Base Rate Divisor</b> — R/W.<br>000 = Divide by 1(48 kHz, 44.1 kHz)<br>001 = Divide by 2 (24 kHz, 22.05 kHz)<br>010 = Divide by 3 (16 kHz, 32 kHz)<br>011 = Divide by 4 (11.025 kHz)<br>100 = Divide by 5 (9.6 kHz)<br>101 = Divide by 6 (8 kHz)<br>110 = Divide by 7<br>111 = Divide by 8 (6 kHz)                                                                                                                                                                                                                                   |
| 7     | Reserved.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
| 6:4   | <b>Bits per Sample (BITS)</b> — R/W.<br>000 = 8 bits. The data will be packed in memory in 8-bit containers on 16-bit boundaries<br>001 = 16 bits. The data will be packed in memory in 16-bit containers on 16-bit boundaries<br>010 = 20 bits. The data will be packed in memory in 32-bit containers on 32-bit boundaries<br>011 = 24 bits. The data will be packed in memory in 32-bit containers on 32-bit boundaries<br>100 = 32 bits. The data will be packed in memory in 32-bit containers on 32-bit boundaries<br>Others = Reserved. |
| 3:0   | <b>Number of Channels (CHAN)</b> — R/W. Indicates number of channels in each frame of the stream.<br>0000 =1<br>0001 =2<br>.....<br>1111 =16                                                                                                                                                                                                                                                                                                                                                                                                   |

### 1.2.43 SBDPDL—Stream Descriptor Buffer Descriptor List Pointer Lower Base Address Register (Intel® High Definition Audio Controller—D27:F0)

Memory Address: Input Stream[0]: HDBAR + 98h      Attribute: R/W,RO  
 Input Stream[1]: HDBAR + B8h  
 Input Stream[2]: HDBAR + D8h  
 Input Stream[3]: HDBAR + F8h  
 Output Stream[0]: HDBAR + 118h  
 Output Stream[1]: HDBAR + 138h  
 Output Stream[2]: HDBAR + 158h  
 Output Stream[3]: HDBAR + 178h

Default Value: 00000000h      Size: 32 bits

| Bit  | Description                                                                                                                                                                                              |
|------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:7 | <b>Buffer Descriptor List Pointer Lower Base Address</b> — R/W. Lower address of the Buffer Descriptor List. This value should only be modified when the RUN bit is 0, or DMA transfer may be corrupted. |
| 6:0  | Hardwired to 0 forcing alignment on 128-B boundaries.                                                                                                                                                    |

### 1.2.44 SBDPU—Stream Descriptor Buffer Descriptor List Pointer Upper Base Address Register (Intel® High Definition Audio Controller—D27:F0)

Memory Address: Input Stream[0]: HDBAR + 9Ch      Attribute: R/W  
 Input Stream[1]: HDBAR + BCh  
 Input Stream[2]: HDBAR + DCh  
 Input Stream[3]: HDBAR + FCh  
 Output Stream[0]: HDBAR + 11Ch  
 Output Stream[1]: HDBAR + 13Ch  
 Output Stream[2]: HDBAR + 15Ch  
 Output Stream[3]: HDBAR + 17Ch

Default Value: 00000000h      Size: 32 bits

| Bit  | Description                                                                                                                                                                                                     |
|------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | <b>Buffer Descriptor List Pointer Upper Base Address</b> — R/W. Upper 32-bit address of the Buffer Descriptor List. This value should only be modified when the RUN bit is 0, or DMA transfer may be corrupted. |

§

## 2 AC '97 Audio Controller Registers (D30:F2)

### 2.1 AC '97 Audio PCI Configuration Space (Audio—D30:F2)

**Note:** Registers that are not shown should be treated as Reserved.

**Table 2-1. AC '97 Audio PCI Register Address Map (Audio—D30:F2)**

| Offset  | Mnemonic | Register Name                           | Default                   | Access    |
|---------|----------|-----------------------------------------|---------------------------|-----------|
| 00h–01h | VID      | Vendor Identification                   | 8086h                     | RO        |
| 02h–03h | DID      | Device Identification                   | See register description. | RO        |
| 04h–05h | PCICMD   | PCI Command                             | 0000h                     | R/W, RO   |
| 06h–07h | PCISTS   | PCI Status                              | 0280h                     | R/WC, RO  |
| 08h     | RID      | Revision Identification                 | See register description  | RO        |
| 09h     | PI       | Programming Interface                   | 00                        | RO        |
| 0Ah     | SCC      | Sub Class Code                          | 01h                       | RO        |
| 0Bh     | BCC      | Base Class Code                         | 04h                       | RO        |
| 0Eh     | HEADTYP  | Header Type                             | 00h                       | RO        |
| 10h–13h | NAMBBAR  | Native Audio Mixer Base Address         | 00000001h                 | R/W, RO   |
| 14h–17h | NAMMBAR  | Native Audio Bus Mastering Base Address | 00000001h                 | R/W, RO   |
| 18h–1Bh | MMBAR    | Mixer Base Address (Mem)                | 00000000h                 | R/W, RO   |
| 1Ch–1Fh | MBBAR    | Bus Master Base Address (Mem)           | 00000000h                 | R/W, RO   |
| 2Ch–2Dh | SVID     | Subsystem Vendor Identification         | 0000h                     | R/WO      |
| 2Eh–2Fh | SID      | Subsystem Identification                | 0000h                     | R/WO      |
| 34h     | CAP_PTR  | Capabilities Pointer                    | 50h                       | RO        |
| 3Ch     | INT_LN   | Interrupt Line                          | 00h                       | R/W       |
| 3Dh     | INT_PN   | Interrupt Pin                           | See register description  | RO        |
| 40h     | PCID     | Programmable Codec ID                   | 09h                       | R/W       |
| 41h     | CFG      | Configuration                           | 00h                       | R/W       |
| 50h–51h | PID      | PCI Power Management Capability ID      | 0001h                     | RO        |
| 52h–53h | PC       | PC -Power Management Capabilities       | C9C2h                     | RO        |
| 54h–55h | PCS      | Power Management Control and Status     | 0000h                     | R/W, R/WC |

**Note:** Internal reset as a result of D3<sub>HOT</sub> to D0 transition will reset all the core well registers except the following BIOS programmed registers as BIOS may not be invoked following the D3-to-D0 transition. All resume well registers will not be reset by the D3<sub>HOT</sub> to D0 transition.

Core well registers **not** reset by the D3<sub>HOT</sub> to D0 transition:

- offset 2Ch–2Dh – Subsystem Vendor ID (SVID)
- offset 2Eh–2Fh – Subsystem ID (SID)
- offset 40h – Programmable Codec ID (PCID)
- offset 41h – Configuration (CFG)

Resume well registers **will not** be reset by the D3<sub>HOT</sub> to D0 transition:

- offset 54h–55h – Power Management Control and Status (PCS)
- Bus Mastering Register: Global Status Register, bits 17:16
- Bus Mastering Register: SDATA\_IN MAP register, bits 7:3

### 2.1.1 VID—Vendor Identification Register (Audio—D30:F2)

|                |         |             |         |
|----------------|---------|-------------|---------|
| Offset:        | 00h–01h | Attribute:  | RO      |
| Default Value: | 8086h   | Size:       | 16 Bits |
| Lockable:      | No      | Power Well: | Core    |

| Bit  | Description                                          |
|------|------------------------------------------------------|
| 15:0 | Vendor ID. This is a 16-bit value assigned to Intel. |

### 2.1.2 DID—Device Identification Register (Audio—D30:F2)

|                |                     |             |         |
|----------------|---------------------|-------------|---------|
| Offset:        | 02h–03h             | Attribute:  | RO      |
| Default Value: | See bit description | Size:       | 16 Bits |
| Lockable:      | No                  | Power Well: | Core    |

| Bit  | Description                                                                                                                                                                                                                                    |
|------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:0 | Device ID — RO. This is a 16-bit value assigned to the Intel <sup>®</sup> ICH7 AC '97 Audio controller. Refer to the <i>Intel<sup>®</sup> I/O Controller Hub 7 (ICH7) Family Specification Update</i> for the value of the Device ID Register. |



### 2.1.3 PCICMD—PCI Command Register (Audio—D30:F2)

|                 |         |             |         |
|-----------------|---------|-------------|---------|
| Address Offset: | 04h–05h | Attribute:  | R/W, RO |
| Default Value:  | 0000h   | Size:       | 16 bits |
| Lockable:       | No      | Power Well: | Core    |

PCICMD is a 16-bit control register. Refer to the PCI 2.3 specification for complete details on each bit.

| Bit   | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:11 | Reserved. Read 0.                                                                                                                                                                                                                                                                                                                                                                                                                                              |
| 10    | <b>Interrupt Disable (ID)</b> — R/W.<br>0 = The INTx# signals may be asserted and MSIs may be generated.<br>1 = The AC '97 controller's INTx# signal will be de-asserted and it may not generate MSIs.                                                                                                                                                                                                                                                         |
| 9     | Fast Back to Back Enable (FBE) — RO. Not implemented. Hardwired to 0.                                                                                                                                                                                                                                                                                                                                                                                          |
| 8     | SERR# Enable (SERR_EN) — RO. Not implemented. Hardwired to 0.                                                                                                                                                                                                                                                                                                                                                                                                  |
| 7     | Wait Cycle Control (WCC) — RO. Not implemented. Hardwired to 0.                                                                                                                                                                                                                                                                                                                                                                                                |
| 6     | Parity Error Response (PER) — RO. Not implemented. Hardwired to 0.                                                                                                                                                                                                                                                                                                                                                                                             |
| 5     | VGA Palette Snoop (VPS). Not implemented. Hardwired to 0.                                                                                                                                                                                                                                                                                                                                                                                                      |
| 4     | Memory Write and Invalidate Enable (MWIE) — RO. Not implemented. Hardwired to 0.                                                                                                                                                                                                                                                                                                                                                                               |
| 3     | Special Cycle Enable (SCE). Not implemented. Hardwired to 0.                                                                                                                                                                                                                                                                                                                                                                                                   |
| 2     | <b>Bus Master Enable (BME)</b> — R/W. Controls standard PCI bus mastering capabilities.<br>0 = Disable<br>1 = Enable                                                                                                                                                                                                                                                                                                                                           |
| 1     | <b>Memory Space Enable (MSE)</b> — R/W. Enables memory space addresses to the AC '97 Audio controller.<br>0 = Disable<br>1 = Enable                                                                                                                                                                                                                                                                                                                            |
| 0     | <b>I/O Space Enable (IOSE)</b> — R/W. This bit controls access to the AC '97 Audio controller I/O space registers.<br>0 = Disable (Default).<br>1 = Enable access to I/O space. The Native PCI Mode Base Address register should be programmed prior to setting this bit.<br><br><b>NOTE:</b> This bit becomes writable when the IOSE bit in offset 41h is set. If at any point software decides to clear the IOSE bit, software must first clear the IOS bit. |

## 2.1.4 PCISTS—PCI Status Register (Audio—D30:F2)

|               |         |             |          |
|---------------|---------|-------------|----------|
| Offset:       | 06h–07h | Attribute:  | RO, R/WC |
| Default Value | 0280h   | Size:       | 16 bits  |
| Lockable:     | No      | Power Well: | Core     |

PCISTA is a 16-bit status register. Refer to the PCI 2.3 specification for complete details on each bit.

| Bit  | Description                                                                                                                                                                                                       |
|------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15   | Detected Parity Error (DPE). Not implemented. Hardwired to 0.                                                                                                                                                     |
| 14   | Signaled System Error (SSE) — RO. Not implemented. Hardwired to 0.                                                                                                                                                |
| 13   | <b>Master Abort Status (MAS)</b> — R/WC. Software clears this bit by writing a 1 to it.<br>0 = No master abort generated.<br>1 = Bus Master AC '97 2.3 interface function, as a master, generates a master abort. |
| 12   | Reserved — RO. Will always read as 0.                                                                                                                                                                             |
| 11   | Signaled Target Abort (STA) — RO. Not implemented. Hardwired to 0.                                                                                                                                                |
| 10:9 | DEVSEL# Timing Status (DEV_STS) — RO. This 2-bit field reflects the ICH7's DEVSEL# timing when performing a positive decode.<br>01b = Medium timing.                                                              |
| 8    | Data Parity Error Detected (DPED) — RO. Not implemented. Hardwired to 0.                                                                                                                                          |
| 7    | Fast Back to Back Capable (FB2BC) — RO. Hardwired to 1. This bit indicates that the ICH7 as a target is capable of fast back-to-back transactions.                                                                |
| 6    | UDF Supported — RO. Not implemented. Hardwired to 0.                                                                                                                                                              |
| 5    | 66 MHz Capable (66MHZ_CAP) — RO. Hardwired to 0.                                                                                                                                                                  |
| 4    | Capabilities List (CAP_LIST) — RO. Indicates that the controller contains a capabilities pointer list. The first item is pointed to by looking at configuration offset 34h.                                       |
| 3    | <b>Interrupt Status (IS)</b> — RO.<br>0 = This bit is 0 after the interrupt is cleared.<br>1 = This bit is 1 when the INTx# is asserted.                                                                          |
| 2:0  | Reserved.                                                                                                                                                                                                         |

### 2.1.5 RID—Revision Identification Register (Audio—D30:F2)

Offset: 08h Attribute: RO  
 Default Value: See bit description Size: 8 Bits  
 Lockable: No Power Well: Core

| Bit | Description                                                                                                                                     |
|-----|-------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:0 | Revision ID — RO. Refer to the <i>Intel® I/O Controller Hub 7 (ICH7) Family Specification Update</i> for the value of the Revision ID Register. |

### 2.1.6 PI—Programming Interface Register (Audio—D30:F2)

Offset: 09h Attribute: RO  
 Default Value: 00h Size: 8 bits  
 Lockable: No Power Well: Core

| Bit | Description                 |
|-----|-----------------------------|
| 7:0 | Programming Interface — RO. |

### 2.1.7 SCC—Sub Class Code Register (Audio—D30:F2)

Address Offset: 0Ah Attribute: RO  
 Default Value: 01h Size: 8 bits  
 Lockable: No Power Well: Core

| Bit | Description                                      |
|-----|--------------------------------------------------|
| 7:0 | Sub Class Code (SCC) — RO.<br>01h = Audio Device |

### 2.1.8 BCC—Base Class Code Register (Audio—D30:F2)

Address Offset: 0Bh Attribute: RO  
 Default Value: 04h Size: 8 bits  
 Lockable: No Power Well: Core

| Bit | Description                                            |
|-----|--------------------------------------------------------|
| 7:0 | Base Class Code (BCC) — RO.<br>04h = Multimedia device |

## 2.1.9 HEADTYP—Header Type Register (Audio—D30:F2)

|                 |     |             |        |
|-----------------|-----|-------------|--------|
| Address Offset: | 0Eh | Attribute:  | RO     |
| Default Value:  | 00h | Size:       | 8 bits |
| Lockable:       | No  | Power Well: | Core   |

| Bit | Description                         |
|-----|-------------------------------------|
| 7:0 | Header Type — RO. Hardwired to 00h. |

## 2.1.10 NAMBAR—Native Audio Mixer Base Address Register (Audio—D30:F2)

|                 |          |             |         |
|-----------------|----------|-------------|---------|
| Address Offset: | 10–13h   | Attribute:  | R/W, RO |
| Default Value:  | 0000001h | Size:       | 32 bits |
| Lockable:       | No       | Power Well: | Core    |

The Native PCI Mode Audio function uses PCI Base Address register #1 to request a contiguous block of I/O space that is to be used for the Native Audio Mixer software interface. The mixer requires 256 bytes of I/O space. Native Audio Mixer and Modem codec I/O registers are located from 00h to 7Fh and reside in the codec. Access to these registers will be decoded by the AC '97 controller and forwarded over the AC-link to the codec. The codec will then respond with the register value.

In the case of the split codec implementation, accesses to the different codecs are differentiated by the controller by using address offsets 00h–7Fh for the primary codec and address offsets 80h–FEh for the secondary codec.

**Note:** The tertiary codec cannot be addressed via this address space. The tertiary space is only available from the new MMBAR register. This register powers up as read only and only becomes write-able when the IOSE bit in offset 41h is set.

For description of these I/O registers, refer to the *Audio Codec '97 Component Specification, Version 2.3*.

| Bit   | Description                                                                                                                                                                                                                                                                                                                                                                                                                                |
|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16 | Hardwired to 0's.                                                                                                                                                                                                                                                                                                                                                                                                                          |
| 15:8  | <b>Base Address</b> — R/W. These bits are used in the I/O space decode of the Native Audio Mixer interface registers. The number of upper bits that a device actually implements depends on how much of the address space the device will respond to. For the AC '97 mixer, the upper 16 bits are hardwired to 0, while bits 15:8 are programmable. This configuration yields a maximum I/O block size of 256 bytes for this base address. |
| 7:1   | Reserved. Read as 0s.                                                                                                                                                                                                                                                                                                                                                                                                                      |
| 0     | <b>Resource Type Indicator (RTE)</b> — RO. This bit defaults to 0 and changes to 1 if the IOSE bit is set (D30:F2:Offset 41h, bit 0). When 1, this bit indicates a request for I/O space.                                                                                                                                                                                                                                                  |

### 2.1.11 NABMBAR—Native Audio Bus Mastering Base Address Register (Audio—D30:F2)

|                 |           |             |         |
|-----------------|-----------|-------------|---------|
| Address Offset: | 14h–17h   | Attribute:  | R/W, RO |
| Default Value:  | 00000001h | Size:       | 32 bits |
| Lockable:       | No        | Power Well: | Core    |

The Native PCI Mode Audio function uses PCI Base Address register #1 to request a contiguous block of I/O space that is to be used for the Native Mode Audio software interface.

**Note:** The DMA registers for S/PDIF\* and Microphone In 2 cannot be addressed via this address space. These DMA functions are only available from the new MBBAR register. This register powers up as read only and only becomes write-able when the IOSE bit in offset 41h is set.

| Bit   | Description                                                                                                                                                                                                                                                                                                                                                                                                                                           |
|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16 | Hardwired to 0's                                                                                                                                                                                                                                                                                                                                                                                                                                      |
| 15:6  | <b>Base Address</b> — R/W. These bits are used in the I/O space decode of the Native Audio Bus Mastering interface registers. The number of upper bits that a device actually implements depends on how much of the address space the device will respond to. For AC '97 bus mastering, the upper 16 bits are hardwired to 0, while bits 15:6 are programmable. This configuration yields a maximum I/O block size of 64 bytes for this base address. |
| 5:1   | Reserved. Read as 0's.                                                                                                                                                                                                                                                                                                                                                                                                                                |
| 0     | <b>Resource Type Indicator (RTE)</b> — RO. This bit defaults to 0 and changes to 1 if the IOSE bit is set (D30:F2:Offset 41h, bit 0). When 1, this bit indicates a request for I/O space.                                                                                                                                                                                                                                                             |

### 2.1.12 MMBAR—Mixer Base Address Register (Audio—D30:F2)

|                 |           |             |         |
|-----------------|-----------|-------------|---------|
| Address Offset: | 18h–1Bh   | Attribute:  | R/W, RO |
| Default Value:  | 00000000h | Size:       | 32 bits |
| Lockable:       | No        | Power Well: | Core    |

This BAR creates 512 bytes of memory space to signify the base address of the register space. The lower 256 bytes of this space map to the same registers as the 256-byte I/O space pointed to by NAMBAR. The lower 384 bytes are divided as follows:

- 128 bytes for the primary codec (offsets 00–7Fh)
- 128 bytes for the secondary codec (offsets 80–FFh)
- 128 bytes for the tertiary codec (offsets 100h–17Fh).
- 128 bytes of reserved space (offsets 180h–1FFh), returning all 0's.

| Bit  | Description                                                                                                                                                                   |
|------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:9 | <b>Base Address</b> — R/W. This field provides the lower 32-bits of the 512-byte memory offset to use for decoding the primary, secondary, and tertiary codec's mixer spaces. |
| 8:3  | Reserved. Read as 0's.                                                                                                                                                        |
| 2:1  | Type — RO. Hardwired to 00b to indicate the base address exists in 32-bit address space                                                                                       |
| 0    | Resource Type Indicator (RTE) — RO. Hardwired to 0 to indicate a request for memory space.                                                                                    |

### 2.1.13 MBBAR—Bus Master Base Address Register (Audio—D30:F2)

|                 |           |             |         |
|-----------------|-----------|-------------|---------|
| Address Offset: | 1Ch–1Fh   | Attribute:  | R/W, RO |
| Default Value:  | 00000000h | Size:       | 32 bits |
| Lockable:       | No        | Power Well: | Core    |

This BAR creates 256-bytes of memory space to signify the base address of the bus master memory space. The lower 64-bytes of the space pointed to by this register point to the same registers as the MBBAR.

| Bit  | Description                                                                                                                          |
|------|--------------------------------------------------------------------------------------------------------------------------------------|
| 31:8 | <b>Base Address</b> — R/W. This field provides the I/O offset to use for decoding the PCM In, PCM Out, and Microphone 1 DMA engines. |
| 7:3  | Reserved. Read as 0's.                                                                                                               |
| 2:1  | Type — RO. Hardwired to 00b to indicate the base address exists in 32-bit address space                                              |
| 0    | Resource Type Indicator (RTE) — RO. Hardwired to 0 to indicate a request for memory space.                                           |

### 2.1.14 SVID—Subsystem Vendor Identification Register (Audio—D30:F2)

|                 |         |             |         |
|-----------------|---------|-------------|---------|
| Address Offset: | 2Ch–2Dh | Attribute:  | R/WO    |
| Default Value:  | 0000h   | Size:       | 16 bits |
| Lockable:       | No      | Power Well: | Core    |

The SVID register, in combination with the Subsystem ID register (D30:F2:2Eh), enable the operating environment to distinguish one audio subsystem from the other(s).

This register is implemented as write-once register. Once a value is written to it, the value can be read back. Any subsequent writes will have no effect.

This register is not affected by the D3<sub>HOT</sub> to D0 transition.

| Bit  | Description                        |
|------|------------------------------------|
| 15:0 | <b>Subsystem Vendor ID</b> — R/WO. |

### 2.1.15 SID—Subsystem Identification Register (Audio—D30:F2)

|                 |         |             |         |
|-----------------|---------|-------------|---------|
| Address Offset: | 2Eh–2Fh | Attribute:  | R/WO    |
| Default Value:  | 0000h   | Size:       | 16 bits |
| Lockable:       | No      | Power Well: | Core    |

The SID register, in combination with the Subsystem Vendor ID register (D30:F2:2Ch) make it possible for the operating environment to distinguish one audio subsystem from the other(s).

This register is implemented as write-once register. Once a value is written to it, the value can be read back. Any subsequent writes will have no effect.

This register is not affected by the D3<sub>HOT</sub> to D0 transition.

| Bit  | Description                 |
|------|-----------------------------|
| 15:0 | <b>Subsystem ID</b> — R/WO. |

### 2.1.16 CAP\_PTR—Capabilities Pointer Register (Audio—D30:F2)

|                 |     |             |        |
|-----------------|-----|-------------|--------|
| Address Offset: | 34h | Attribute:  | RO     |
| Default Value:  | 50h | Size:       | 8 bits |
| Lockable:       | No  | Power Well: | Core   |

This register indicates the offset for the capability pointer.

| Bit | Description                                                                                                             |
|-----|-------------------------------------------------------------------------------------------------------------------------|
| 7:0 | <b>Capabilities Pointer (CAP_PTR)</b> — RO. This field indicates that the first capability pointer offset is offset 50h |

### 2.1.17 INT\_LN—Interrupt Line Register (Audio—D30:F2)

|                 |     |             |        |
|-----------------|-----|-------------|--------|
| Address Offset: | 3Ch | Attribute:  | R/W    |
| Default Value:  | 00h | Size:       | 8 bits |
| Lockable:       | No  | Power Well: | Core   |

This register indicates which PCI interrupt line is used for the AC '97 module interrupt.

| Bit | Description                                                                                                                                                                      |
|-----|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:0 | <b>Interrupt Line (INT_LN)</b> — R/W. This data is not used by the Intel® ICH7. It is used to communicate to software the interrupt line that is connected to the interrupt pin. |

### 2.1.18 INT\_PN—Interrupt Pin Register (Audio—D30:F2)

|                 |                 |             |        |
|-----------------|-----------------|-------------|--------|
| Address Offset: | 3Dh             | Attribute:  | RO     |
| Default Value:  | See Description | Size:       | 8 bits |
| Lockable:       | No              | Power Well: | Core   |

This register indicates which PCI interrupt pin is used for the AC '97 module interrupt. The AC '97 interrupt is internally OR'd to the interrupt controller with the PIRQB# signal.

| Bit | Description                                                                                          |
|-----|------------------------------------------------------------------------------------------------------|
| 7:0 | AC '97 Interrupt Routing — RO. This reflects the value of D30IP.AAIP in chipset configuration space. |

### 2.1.19 PCID—Programmable Codec Identification Register (Audio—D30:F2)

|                 |     |             |        |
|-----------------|-----|-------------|--------|
| Address Offset: | 40h | Attribute:  | R/W    |
| Default Value:  | 09h | Size:       | 8 bits |
| Lockable:       | No  | Power Well: | Core   |

This register is used to specify the ID for the secondary and tertiary codecs for I/O accesses. This register is not affected by the D3<sub>HOT</sub> to D0 transition. The value in this register must be modified before any AC '97 codec accesses.

| Bit | Description                                                                                                                                                                                                                                                                                                                                   |
|-----|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:4 | Reserved.                                                                                                                                                                                                                                                                                                                                     |
| 3:2 | <b>Tertiary Codec ID (TID)</b> — R/W. These bits define the encoded ID that is used to address the tertiary codec I/O space. Bit 1 is the first bit sent and Bit 0 is the second bit sent on ACZ_SDOOUT during slot 0.                                                                                                                        |
| 1:0 | <b>Secondary Codec ID (SCID)</b> — R/W. These two bits define the encoded ID that is used to address the secondary codec I/O space. The two bits are the ID that will be placed on slot 0, bits 0 and 1, upon an I/O access to the secondary codec. Bit 1 is the first bit sent and bit 0 is the second bit sent on ACZ_SDOOUT during slot 0. |

### 2.1.20 CFG—Configuration Register (Audio—D30:F2)

|                 |     |             |        |
|-----------------|-----|-------------|--------|
| Address Offset: | 41h | Attribute:  | R/W    |
| Default Value:  | 00h | Size:       | 8 bits |
| Lockable:       | No  | Power Well: | Core   |

This register is used to specify the ID for the secondary and tertiary codecs for I/O accesses. This register is not affected by the D3<sub>HOT</sub> to D0 transition.

| Bit | Description                                                                                                                                                                                                                                                                                                                                                                               |
|-----|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:1 | Reserved—RO.                                                                                                                                                                                                                                                                                                                                                                              |
| 0   | <b>I/O Space Enable (IOSE)</b> — R/W.<br>0 = Disable. The IOS bit at offset 04h and the I/O space BARs at offset 10h and 14h become read only registers. Additionally, bit 0 of the I/O BARs at offsets 10h and 14h are hardwired to 0 when this bit is 0. This is the default state for the I/O BARs. BIOS must explicitly set this bit to allow a legacy driver to work.<br>1 = Enable. |







## 2.2 AC '97 Audio I/O Space (D30:F2)

The AC '97 I/O space includes Native Audio Bus Master registers and Native Mixer registers. For the ICH7, the offsets are important as they will determine bits 1:0 of the TAG field (codec ID).

Audio Mixer I/O space can be accessed as a 16-bit field only since the data packet length on AC-link is a word. Any S/W access to the codec will be done as a 16-bit access starting from the first active byte. In case no byte enables are active, the access will be done at the first word of the QWord that contains the address of this request.

**Table 2-2. Intel® ICH7 Audio Mixer Register Configuration**

| Primary Offset<br>(Codec ID =00) | Secondary Offset<br>(Codec ID =01) | Tertiary Offset<br>(Codec ID =10) | NAMBAR Exposed Registers<br>(D30:F2) |
|----------------------------------|------------------------------------|-----------------------------------|--------------------------------------|
| 00h                              | 80h                                | 100h                              | Reset                                |
| 02h                              | 82h                                | 102h                              | Master Volume                        |
| 04h                              | 84h                                | 104h                              | Aux Out Volume                       |
| 06h                              | 86h                                | 106h                              | Mono Volume                          |
| 08h                              | 88h                                | 108h                              | Master Tone (R & L)                  |
| 0Ah                              | 8Ah                                | 10Ah                              | PC_BEEP Volume                       |
| 0Ch                              | 8Ch                                | 10Ch                              | Phone Volume                         |
| 0Eh                              | 8Eh                                | 10Eh                              | Mic Volume                           |
| 10h                              | 90h                                | 110h                              | Line In Volume                       |
| 12h                              | 92h                                | 112h                              | CD Volume                            |
| 14h                              | 94h                                | 114h                              | Video Volume                         |
| 16h                              | 96h                                | 116h                              | Aux In Volume                        |
| 18h                              | 98h                                | 118h                              | PCM Out Volume                       |
| 1Ah                              | 9Ah                                | 11Ah                              | Record Select                        |
| 1Ch                              | 9Ch                                | 11Ch                              | Record Gain                          |
| 1Eh                              | 9Eh                                | 11Eh                              | Record Gain Mic                      |
| 20h                              | A0h                                | 120h                              | General Purpose                      |
| 22h                              | A2h                                | 122h                              | 3D Control                           |
| 24h                              | A4h                                | 124h                              | AC '97 RESERVED                      |
| 26h                              | A6h                                | 126h                              | Powerdown Ctrl/Stat                  |
| 28h                              | A8h                                | 128h                              | Extended Audio                       |
| 2Ah                              | AAh                                | 12Ah                              | Extended Audio Ctrl/Stat             |
| 2Ch                              | ACh                                | 12Ch                              | PCM Front DAC Rate                   |
| 2Eh                              | A Eh                               | 12Eh                              | PCM Surround DAC Rate                |
| 30h                              | B0h                                | 130h                              | PCM LFE DAC Rate                     |
| 32h                              | B2h                                | 132h                              | PCM LR ADC Rate                      |
| 34h                              | B4h                                | 134h                              | MIC ADC Rate                         |
| 36h                              | B6h                                | 136h                              | 6Ch Vol: C, LFE                      |
| 38h                              | B8h                                | 138h                              | 6Ch Vol: L, R Surround               |
| 3Ah                              | BAh                                | 13Ah                              | S/PDIF Control                       |
| 3Ch–56h                          | BC–D6h                             | 13C–156h                          | Intel RESERVED                       |
| 58h                              | D8h                                | 158h                              | AC '97 Reserved                      |

Table 2-2. Intel® ICH7 Audio Mixer Register Configuration

| Primary Offset<br>(Codec ID =00) | Secondary Offset<br>(Codec ID =01) | Tertiary Offset<br>(Codec ID =10) | NAMBAR Exposed Registers<br>(D30:F2) |
|----------------------------------|------------------------------------|-----------------------------------|--------------------------------------|
| 5Ah                              | DAh                                | 15Ah                              | Vendor Reserved                      |
| 7Ch                              | FCh                                | 17Ch                              | Vendor ID1                           |
| 7Eh                              | FEh                                | 17Eh                              | Vendor ID2                           |

**NOTE:**

1. Software should not try to access reserved registers
2. Primary Codec ID cannot be changed. Secondary codec ID can be changed via bits 1:0 of configuration register 40h. Tertiary codec ID can be changed via bits 3:2 of configuration register 40h.
3. The tertiary offset is only available through the memory space defined by the MMBAR register.

The Bus Master registers are located from offset + 00h to offset + 51h and reside in the AC '97 controller. Accesses to these registers do **not** cause the cycle to be forwarded over the AC-link to the codec. S/W could access these registers as bytes, word, DWord or qword quantities, but reads must not cross DWord boundaries.

In the case of the split codec implementation, accesses to the different codecs are differentiated by the controller by using address offsets 00h–7Fh for the primary codec, address offsets 80h–FFh for the secondary codec and address offsets 100h–17Fh for the tertiary codec.

The Global Control (GLOB\_CNT) (D30:F2:2Ch) and Global Status (GLOB\_STA) (D30:F2:30h) registers are aliased to the same global registers in the audio and modem I/O space. Therefore a read/write to these registers in either audio or modem I/O space affects the same physical register.

Bus Mastering registers exist in I/O space and reside in the AC '97 controller. The six channels, PCM in, PCM in 2, PCM out, Mic in, Mic 2, and S/PDIF out, each have their own set of Bus Mastering registers. The following register descriptions apply to all six channels. The register definition section titles use a generic “x\_” in front of the register to indicate that the register applies to all six channels. The naming prefix convention used in [Table 2-3](#) and in the register description I/O address is as follows:

PI = PCM in channel  
 PO = PCM out channel  
 MC = Mic in channel  
 MC2 = Mic 2 channel  
 PI2 = PCM in 2 channel  
 SP = S/PDIF out channel.

**Table 2-3. Native Audio Bus Master Control Registers (Sheet 1 of 2)**

| Offset | Mnemonic  | Name                                         | Default                  | Access             |
|--------|-----------|----------------------------------------------|--------------------------|--------------------|
| 00h    | PI_BDBAR  | PCM In Buffer Descriptor list Base Address   | 00000000h                | R/W                |
| 04h    | PI_CIV    | PCM In Current Index Value                   | 00h                      | RO                 |
| 05h    | PI_LVI    | PCM In Last Valid Index                      | 00h                      | R/W                |
| 06h    | PI_SR     | PCM In Status                                | 0001h                    | R/WC, RO           |
| 08h    | PI_PICB   | PCM In Position in Current Buffer            | 0000h                    | RO                 |
| 0Ah    | PI_PIV    | PCM In Prefetched Index Value                | 00h                      | RO                 |
| 0Bh    | PI_CR     | PCM In Control                               | 00h                      | R/W, R/W (special) |
| 10h    | PO_BDBAR  | PCM Out Buffer Descriptor list Base Address  | 00000000h                | R/W                |
| 14h    | PO_CIV    | PCM Out Current Index Value                  | 00h                      | RO                 |
| 15h    | PO_LVI    | PCM Out Last Valid Index                     | 00h                      | R/W                |
| 16h    | PO_SR     | PCM Out Status                               | 0001h                    | R/WC, RO           |
| 18h    | PO_PICB   | PCM In Position In Current Buffer            | 0000h                    | RO                 |
| 1Ah    | PO_PIV    | PCM Out Prefetched Index Value               | 00h                      | RO                 |
| 1Bh    | PO_CR     | PCM Out Control                              | 00h                      | R/W, R/W (special) |
| 20h    | MC_BDBAR  | Mic. In Buffer Descriptor List Base Address  | 00000000h                | R/W                |
| 24h    | MC_CIV    | Mic. In Current Index Value                  | 00h                      | RO                 |
| 25h    | MC_LVI    | Mic. In Last Valid Index                     | 00h                      | R/W                |
| 26h    | MC_SR     | Mic. In Status                               | 0001h                    | R/WC, RO           |
| 28h    | MC_PICB   | Mic. In Position In Current Buffer           | 0000h                    | RO                 |
| 2Ah    | MC_PIV    | Mic. In Prefetched Index Value               | 00h                      | RO                 |
| 2Bh    | MC_CR     | Mic. In Control                              | 00h                      | R/W, R/W (special) |
| 2Ch    | GLOB_CNT  | Global Control                               | 00000000h                | R/W, R/W (special) |
| 30h    | GLOB_STA  | Global Status                                | See register description | R/W, R/WC, RO      |
| 34h    | CAS       | Codec Access Semaphore                       | 00h                      | R/W (special)      |
| 40h    | MC2_BDBAR | Mic. 2 Buffer Descriptor List Base Address   | 00000000h                | R/W                |
| 44h    | MC2_CIV   | Mic. 2 Current Index Value                   | 00h                      | RO                 |
| 45h    | MC2_LVI   | Mic. 2 Last Valid Index                      | 00h                      | R/W                |
| 46h    | MC2_SR    | Mic. 2 Status                                | 0001h                    | RO, R/WC           |
| 48h    | MC2_PICB  | Mic 2 Position In Current Buffer             | 0000h                    | RO                 |
| 4Ah    | MC2_PIV   | Mic. 2 Prefetched Index Value                | 00h                      | RO                 |
| 4Bh    | MC2_CR    | Mic. 2 Control                               | 00h                      | R/W, R/W (special) |
| 50h    | PI2_BDBAR | PCM In 2 Buffer Descriptor List Base Address | 00000000h                | R/W                |
| 54h    | PI2_CIV   | PCM In 2 Current Index Value                 | 00h                      | RO                 |
| 55h    | PI2_LVI   | PCM In 2 Last Valid Index                    | 00h                      | R/W                |
| 56h    | PI2_SR    | PCM In 2 Status                              | 0001h                    | R/WC, RO           |

Table 2-3. Native Audio Bus Master Control Registers (Sheet 2 of 2)

| Offset | Mnemonic | Name                                       | Default   | Access             |
|--------|----------|--------------------------------------------|-----------|--------------------|
| 58h    | PI2_PICB | PCM In 2 Position in Current Buffer        | 0000h     | RO                 |
| 5Ah    | PI2_PIV  | PCM In 2 Prefetched Index Value            | 00h       | RO                 |
| 5Bh    | PI2_CR   | PCM In 2 Control                           | 00h       | R/W, R/W (special) |
| 60h    | SPBAR    | S/PDIF Buffer Descriptor List Base Address | 00000000h | R/W                |
| 64h    | SPCIV    | S/PDIF Current Index Value                 | 00h       | RO                 |
| 65h    | SPLVI    | S/PDIF Last Valid Index                    | 00h       | R/W                |
| 66h    | SPSR     | S/PDIF Status                              | 0001h     | R/WC, RO           |
| 68h    | SPPICB   | S/PDIF Position In Current Buffer          | 0000h     | RO                 |
| 6Ah    | SPPIV    | S/PDIF Prefetched Index Value              | 00h       | RO                 |
| 6Bh    | SPCR     | S/PDIF Control                             | 00h       | R/W, R/W (special) |
| 80h    | SDM      | SData_IN Map                               | 00h       | R/W, RO            |

**Note:** Internal reset as a result of D3<sub>HOT</sub> to D0 transition will reset all the core well registers except the registers shared with the AC '97 Modem (GCR, GSR, CASR). All resume well registers will not be reset by the D3<sub>HOT</sub> to D0 transition.

Core well registers and bits **not** reset by the D3<sub>HOT</sub> to D0 transition:

- offset 2Ch–2Fh – bits 6:0 Global Control (GLOB\_CNT)
- offset 30h–33h – bits [29,15,11:10,0] Global Status (GLOB\_STA)
- offset 34h – Codec Access Semaphore Register (CAS)

Resume well registers and bits **will not** be reset by the D3<sub>HOT</sub> to D0 transition:

- offset 30h–33h – bits [17:16] Global Status (GLOB\_STA)

## 2.2.1 x\_BDBAR—Buffer Descriptor Base Address Register (Audio—D30:F2)

|                |                                                                                                                                                               |             |         |
|----------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------|---------|
| I/O Address:   | NABMBAR + 00h (PIBDBAR),<br>NABMBAR + 10h (POBDBAR),<br>NABMBAR + 20h (MCBDBAR),<br>MBBAR + 40h (MC2BDBAR),<br>MBBAR + 50h (PI2BDBAR),<br>MBBAR + 60h (SPBAR) | Attribute:  | R/W     |
| Default Value: | 00000000h                                                                                                                                                     | Size:       | 32 bits |
| Lockable:      | No                                                                                                                                                            | Power Well: | Core    |

Software can read the register at offset 00h by performing a single 32-bit read from address offset 00h. Reads across DWord boundaries are not supported.

| Bit  | Description                                                                                                                                                                                                                          |
|------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:3 | <b>Buffer Descriptor Base Address[31:3]</b> — R/W. These bits represent address bits 31:3. The data should be aligned on 8-byte boundaries. Each buffer descriptor is 8 bytes long and the list can contain a maximum of 32 entries. |
| 2:0  | Hardwired to 0.                                                                                                                                                                                                                      |

### 2.2.2 x\_CIV—Current Index Value Register (Audio—D30:F2)

|                |                                                                                                                                                  |             |        |
|----------------|--------------------------------------------------------------------------------------------------------------------------------------------------|-------------|--------|
| I/O Address:   | NABMBAR + 04h (PICIV),<br>NABMBAR + 14h (POCIV),<br>NABMBAR + 24h (MCCIV)<br>MBBAR + 44h (MC2CIV)<br>MBBAR + 54h (PI2CIV)<br>MBBAR + 64h (SPCIV) | Attribute:  | RO     |
| Default Value: | 00h                                                                                                                                              | Size:       | 8 bits |
| Lockable:      | No                                                                                                                                               | Power Well: | Core   |

Software can read the registers at offsets 04h, 05h and 06h simultaneously by performing a single, 32-bit read from address offset 04h. Software can also read this register individually by doing a single, 8-bit read to offset 04h.

| Bit | Description                                                                                                                                                                                                                                               |
|-----|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:5 | Hardwired to 0                                                                                                                                                                                                                                            |
| 4:0 | <b>Current Index Value [4:0]</b> — RO. These bits represent which buffer descriptor within the list of 32 descriptors is currently being processed. As each descriptor is processed, this value is incremented. The value rolls over after it reaches 31. |

**NOTE:** Reads across DWord boundaries are not supported.

### 2.2.3 x\_LVI—Last Valid Index Register (Audio—D30:F2)

|                |                                                                                                                                                  |             |        |
|----------------|--------------------------------------------------------------------------------------------------------------------------------------------------|-------------|--------|
| I/O Address:   | NABMBAR + 05h (PILVI),<br>NABMBAR + 15h (POLVI),<br>NABMBAR + 25h (MCLVI)<br>MBBAR + 45h (MC2LVI)<br>MBBAR + 55h (PI2LVI)<br>MBBAR + 65h (SPLVI) | Attribute:  | R/W    |
| Default Value: | 00h                                                                                                                                              | Size:       | 8 bits |
| Lockable:      | No                                                                                                                                               | Power Well: | Core   |

Software can read the registers at offsets 04h, 05h and 06h simultaneously by performing a single, 32-bit read from address offset 04h. Software can also read this register individually by doing a single, 8-bit read to offset 05h.

| Bit | Description                                                                                                                                                                                         |
|-----|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:5 | Hardwired to 0.                                                                                                                                                                                     |
| 4:0 | <b>Last Valid Index [4:0]</b> — R/W. This value represents the last valid descriptor in the list. This value is updated by the software each time it prepares a new buffer and adds it to the list. |

**NOTE:** Reads across DWord boundaries are not supported.

## 2.2.4 x\_SR—Status Register (Audio—D30:F2)

|                |                                                                                                                                            |             |          |
|----------------|--------------------------------------------------------------------------------------------------------------------------------------------|-------------|----------|
| I/O Address:   | NABMBAR + 06h (PISR),<br>NABMBAR + 16h (POSR),<br>NABMBAR + 26h (MCSR)<br>MBBAR + 46h (MC2SR)<br>MBBAR + 56h (PI2SR)<br>MBBAR + 66h (SPSR) | Attribute:  | R/WC, RO |
| Default Value: | 0001h                                                                                                                                      | Size:       | 16 bits  |
| Lockable:      | No                                                                                                                                         | Power Well: | Core     |

Software can read the registers at offsets 04h, 05h and 06h simultaneously by performing a single, 32-bit read from address offset 04h. Software can also read this register individually by doing a single, 16-bit read to offset 06h. Reads across DWord boundaries are not supported.

| Bit  | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
|------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:5 | Reserved.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
| 4    | <p><b>FIFO Error (FIFOE)</b> — R/WC. Software clears this bit by writing a 1 to it.</p> <p>0 = No FIFO error.<br/>1 = FIFO error occurs.</p> <p><b>PISR Register:</b> FIFO error indicates a FIFO overrun. The FIFO pointers don't increment, the incoming data is not written into the FIFO, thus is lost.</p> <p><b>POSR Register:</b> FIFO error indicates a FIFO underrun. The sample transmitted in this case should be the last valid sample.</p> <p>The ICH7 will set the FIFO bit if the under-run or overrun occurs when there are more valid buffers to process.</p>                                                                                                                                                                                                                                                                                                                |
| 3    | <p><b>Buffer Completion Interrupt Status (BCIS)</b> — R/WC.</p> <p>0 = Software clears this bit by writing a 1 to it.<br/>1 = Set by the hardware after the last sample of a buffer has been processed, AND if the Interrupt on Completion (IOC) bit is set in the command byte of the buffer descriptor. It remains active until cleared by software.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
| 2    | <p><b>Last Valid Buffer Completion Interrupt (LVBCI)</b> — R/WC.</p> <p>0 = Software clears this bit by writing a 1 to it.<br/>1 = Last valid buffer has been processed. It remains active until cleared by software. This bit indicates the occurrence of the event signified by the last valid buffer being processed. Thus this is an event status bit that can be cleared by software once this event has been recognized. This event will cause an interrupt if the enable bit (D30:F2:NABMBAR + 0Bh, bit 2) in the Control Register is set. The interrupt is cleared when the software clears this bit.</p> <p>In the case of <i>Transmits</i> (PCM out, Modem out) this bit is set, after the last valid buffer has been fetched (not after transmitting it). While in the case of <i>Receives</i>, this bit is set after the data for the last buffer has been written to memory.</p> |
| 1    | <p><b>Current Equals Last Valid (CELV)</b> — RO.</p> <p>0 = Cleared by hardware when controller exists state (i.e., until a new value is written to the LVI register.)<br/>1 = Current Index is equal to the value in the Last Valid Index Register (D30:F2:NABMBAR + 05h), and the buffer pointed to by the CIV has been processed (i.e., after the last valid buffer has been processed). This bit is very similar to bit 2, except this bit reflects the state rather than the event. This bit reflects the state of the controller, and remains set until the controller exits this state.</p>                                                                                                                                                                                                                                                                                            |
| 0    | <p><b>DMA Controller Halted (DCH)</b> — RO.</p> <p>0 = Running.<br/>1 = Halted. This could happen because of the Start/Stop bit being cleared and the DMA engines are idle, or it could happen once the controller has processed the last valid buffer.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |



## 2.2.5 x\_PICB—Position In Current Buffer Register (Audio—D30:F2)

|                |                                                                                                                                                           |             |         |
|----------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------|-------------|---------|
| I/O Address:   | NABMBAR + 08h (PIPICB),<br>NABMBAR + 18h (POPICB),<br>NABMBAR + 28h (MCPICB),<br>MBBAR + 48h (MC2PICB),<br>MBBAR + 58h (PI2PICB),<br>MBBAR + 68h (SPPICB) | Attribute:  | RO      |
| Default Value: | 0000h                                                                                                                                                     | Size:       | 16 bits |
| Lockable:      | No                                                                                                                                                        | Power Well: | Core    |

Software can read the registers at the offsets 08h, 0Ah, and 0Bh by performing a 32-bit read from the address offset 08h. Software can also read this register individually by doing a single, 16-bit read to offset 08h. Reads across DWord boundaries are not supported.

| Bit  | Description                                                                                                                                                                                                                                                                                                                                                                                  |
|------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:0 | <b>Position In Current Buffer [15:0]</b> — RO. These bits represent the number of samples left to be processed in the current buffer. This means the number of samples not yet read from memory (in the case of reads from memory) or not yet written to memory (in the case of writes to memory), irrespective of the number of samples that have been transmitted/received across AC-link. |

## 2.2.6 x\_PIV—Prefetched Index Value Register (Audio—D30:F2)

|                |                                                                                                                                                     |             |        |
|----------------|-----------------------------------------------------------------------------------------------------------------------------------------------------|-------------|--------|
| I/O Address:   | NABMBAR + 0Ah (PIPIV),<br>NABMBAR + 1Ah (POPIV),<br>NABMBAR + 2Ah (MCPIV),<br>MBBAR + 4Ah (MC2PIV),<br>MBBAR + 5Ah (PI2PIV),<br>MBBAR + 6Ah (SPPIV) | Attribute:  | RO     |
| Default Value: | 00h                                                                                                                                                 | Size:       | 8 bits |
| Lockable:      | No                                                                                                                                                  | Power Well: | Core   |

Software can read the registers at the offsets 08h, 0Ah, and 0Bh by performing a 32-bit read from the address offset 08h. Software can also read this register individually by doing a single, 8-bit read to offset 0Ah. Reads across DWord boundaries are not supported.

| Bit | Description                                                                                                                                                                                             |
|-----|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:5 | Hardwired to 0.                                                                                                                                                                                         |
| 4:0 | <b>Prefetched Index Value [4:0]</b> — RO. These bits represent which buffer descriptor in the list has been prefetched. The bits in this register are also modulo 32 and roll over after they reach 31. |

## 2.2.7 x\_CR—Control Register (Audio—D30:F2)

|                |                                                                                                                                            |             |                    |
|----------------|--------------------------------------------------------------------------------------------------------------------------------------------|-------------|--------------------|
| I/O Address:   | NABMBAR + 0Bh (PICR),<br>NABMBAR + 1Bh (POCR),<br>NABMBAR + 2Bh (MCCR)<br>MBBAR + 4Bh (MC2CR)<br>MBBAR + 5Bh (PI2CR)<br>MBBAR + 6Bh (SPCR) | Attribute:  | R/W, R/W (special) |
| Default Value: | 00h                                                                                                                                        | Size:       | 8 bits             |
| Lockable:      | No                                                                                                                                         | Power Well: | Core               |

Software can read the registers at the offsets 08h, 0Ah, and 0Bh by performing a 32-bit read from the address offset 08h. Software can also read this register individually by doing a single, 8-bit read to offset 0Bh. Reads across DWord boundaries are not supported.

| Bit | Description                                                                                                                                                                                                                                                                                                                                                                                                                                              |
|-----|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:5 | Reserved.                                                                                                                                                                                                                                                                                                                                                                                                                                                |
| 4   | <b>Interrupt on Completion Enable (IOCE)</b> — R/W. This bit controls whether or not an interrupt occurs when a buffer completes with the IOC bit set in its descriptor.<br>0 = Disable. Interrupt will not occur.<br>1 = Enable.                                                                                                                                                                                                                        |
| 3   | <b>FIFO Error Interrupt Enable (FEIE)</b> — R/W. This bit controls whether the occurrence of a FIFO error will cause an interrupt or not.<br>0 = Disable. Bit 4 in the Status register will be set, but the interrupt will not occur.<br>1 = Enable. Interrupt will occur.                                                                                                                                                                               |
| 2   | <b>Last Valid Buffer Interrupt Enable (LVBIE)</b> — R/W. This bit controls whether the completion of the last valid buffer will cause an interrupt or not.<br>0 = Disable. Bit 2 in the Status register will still be set, but the interrupt will not occur.<br>1 = Enable.                                                                                                                                                                              |
| 1   | <b>Reset Registers (RR)</b> — R/W (special).<br>0 = Removes reset condition.<br>1 = Contents of all Bus master related registers to be reset, except the interrupt enable bits (bit 4,3,2 of this register). Software needs to set this bit but need not clear it since the bit is self clearing. This bit must be set only when the Run/Pause bit (D30:F2:2Bh, bit 0) is cleared. Setting it when the Run bit is set will cause undefined consequences. |
| 0   | <b>Run/Pause Bus Master (RPBM)</b> — R/W.<br>0 = Pause bus master operation. This results in all state information being retained (i.e., master mode operation can be stopped and then resumed).<br>1 = Run. Bus master operation starts.                                                                                                                                                                                                                |

## 2.2.8 GLOB\_CNT—Global Control Register (Audio—D30:F2)

|                |               |             |                    |
|----------------|---------------|-------------|--------------------|
| I/O Address:   | NABMBAR + 2Ch | Attribute:  | R/W, R/W (special) |
| Default Value: | 00000000h     | Size:       | 32 bits            |
| Lockable:      | No            | Power Well: | Core               |

| Bit   | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:30 | <p><b>S/PDIF Slot Map (SSM)</b> — R/W. If the run/pause bus master bit (bit 0 of offset 2Bh) is set, then the value in these bits indicate which slots S/PDIF data is transmitted on. Software must ensure that the programming here does not conflict with the PCM channels being used. If there is a conflict, unpredictable behavior will result — the hardware will not check for a conflict.</p> <p>00 = Reserved<br/>           01 = Slots 7 and 8<br/>           10 = Slots 6 and 9<br/>           11 = Slots 10 and 11</p>                                              |
| 29:24 | Reserved.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
| 23:22 | <p><b>PCM Out Mode (POM)</b> — R/W. Enables the PCM out channel to use 16- or 20-bit audio on PCM out. This does not affect the microphone of S/PDIF DMA. When greater than 16-bit audio is used, the data structures are aligned as 32-bits per sample, with the highest order bits representing the data, and the lower order bits as don't care.</p> <p>00 = 16 bit audio (default)<br/>           01 = 20 bit audio<br/>           10 = Reserved. If set, indeterminate behavior will result.<br/>           11 = Reserved. If set, indeterminate behavior will result.</p> |
| 21:20 | <p><b>PCM 4/6 Enable</b> — R/W. This field configures PCM Output for 2-, 4- or 6-channel mode.</p> <p>00 = 2-channel mode (default)<br/>           01 = 4-channel mode<br/>           10 = 6-channel mode<br/>           11 = Reserved</p>                                                                                                                                                                                                                                                                                                                                      |
| 19:7  | Reserved.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
| 6     | <p><b>ACZ_SDIN2 Interrupt Enable</b> — R/W.</p> <p>0 = Disable.<br/>           1 = Enable an interrupt to occur when the codec on the ACZ_SDIN2 causes a resume event on the AC-link.</p> <p><b>NOTE:</b> This bit is not affected by AC '97 Audio Function D3<sub>HOT</sub> to D0 reset.</p>                                                                                                                                                                                                                                                                                   |
| 5     | <p><b>ACZ_SDIN1 Interrupt Enable</b> — R/W.</p> <p>0 = Disable.<br/>           1 = Enable an interrupt to occur when the codec on the ACZ_SDIN1 causes a resume event on the AC-link.</p> <p><b>NOTE:</b> This bit is not affected by AC '97 Audio Function D3<sub>HOT</sub> to D0 reset.</p>                                                                                                                                                                                                                                                                                   |
| 4     | <p><b>ACZ_SDIN0 Interrupt Enable</b> — R/W.</p> <p>0 = Disable.<br/>           1 = Enable an interrupt to occur when the codec on ACZ_SDIN0 causes a resume event on the AC-link.</p> <p><b>NOTE:</b> This bit is not affected by AC '97 Audio Function D3<sub>HOT</sub> to D0 reset.</p>                                                                                                                                                                                                                                                                                       |
| 3     | <p><b>AC-LINK Shut Off (LSO)</b> — R/W.</p> <p>0 = Normal operation.<br/>           1 = Controller disables all outputs which will be pulled low by internal pull down resistors.</p> <p><b>NOTE:</b> This bit is not affected by AC '97 Audio Function D3<sub>HOT</sub> to D0 reset.</p>                                                                                                                                                                                                                                                                                       |

| Bit | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
|-----|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 2   | <p><b>AC '97 Warm Reset</b> — R/W (special).</p> <p>0 = Normal operation.<br/>           1 = Writing a 1 to this bit causes a warm reset to occur on the AC-link. The warm reset will awaken a suspended codec without clearing its internal registers. If software attempts to perform a warm reset while bit_clk is running, the write will be ignored and the bit will not change. This bit is self-clearing (it remains set until the reset completes and bit_clk is seen on the AC-link, after which it clears itself).</p> <p><b>NOTE:</b> This bit is not affected by AC '97 Audio Function D3<sub>HOT</sub> to D0 reset.</p>                                                            |
| 1   | <p><b>AC '97 Cold Reset#</b> — R/W.</p> <p>0 = Writing a 0 to this bit causes a cold reset to occur throughout the AC '97 circuitry. All data in the controller and the codec will be lost. Software needs to clear this bit no sooner than the minimum number of ms have elapsed.<br/>           1 = This bit defaults to 0 and hence after reset, the driver needs to set this bit to a 1. The value of this bit is retained after suspends; hence, if this bit is set to a 1 prior to suspending, a cold reset is not generated automatically upon resuming.</p> <p><b>NOTE:</b> This bit is in the core well and is not affected by AC '97 Audio Function D3<sub>HOT</sub> to D0 reset.</p> |
| 0   | <p><b>GPI Interrupt Enable (GIE)</b> — R/W. This bit controls whether the change in status of any GPI causes an interrupt.</p> <p>0 = Bit 0 of the Global Status register is set, but no interrupt is generated.<br/>           1 = The change on value of a GPI causes an interrupt and sets bit 0 of the Global Status register.</p> <p><b>NOTE:</b> This bit is not affected by AC '97 Audio Function D3<sub>HOT</sub> to D0 reset.</p>                                                                                                                                                                                                                                                      |

**NOTE:** Reads across DWord boundaries are not supported.

## 2.2.9 GLOB\_STA—Global Status Register (Audio—D30:F2)

|                |                                |             |               |
|----------------|--------------------------------|-------------|---------------|
| I/O Address:   | NABMBAR + 30h                  | Attribute:  | RO, R/W, R/WC |
| Default Value: | 00x0xxx0111000000000xxxx00xxxb | Size:       | 32 bits       |
| Lockable:      | No                             | Power Well: | Core          |

| Bit   | Description                                                                                                                                                                                                                                                                                                                                                                         |
|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:30 | Reserved.                                                                                                                                                                                                                                                                                                                                                                           |
| 29    | <p><b>ACZ_SDIN2 Resume Interrupt (S2RI)</b> — R/WC. This bit indicates a resume event occurred on ACZ_SDIN2. Software clears this bit by writing a 1 to it.</p> <p>0 = Resume event did Not occur.<br/>1 = Resume event occurred.</p> <p><b>NOTE:</b> This bit is not affected by D3<sub>HOT</sub> to D0 Reset.</p>                                                                 |
| 28    | <p><b>ACZ_SDIN2 Codec Ready (S2CR)</b> — RO. Reflects the state of the codec ready bit on ACZ_SDIN2. Bus masters ignore the condition of the codec ready bits, so software must check this bit before starting the bus masters. Once the codec is “ready”, it must never go “not ready” spontaneously.</p> <p>0 = Not Ready.<br/>1 = Ready.</p>                                     |
| 27    | <p><b>Bit Clock Stopped (BCS)</b> — RO. This bit indicates that the bit clock is not running.</p> <p>0 = Transition is found on BIT_CLK.<br/>1 = ICH7 detected that there has been no transition on BIT_CLK for four consecutive PCI clocks.</p>                                                                                                                                    |
| 26    | <p><b>S/PDIF Interrupt (SPINT)</b> — RO.</p> <p>0 = When the specific status bit is cleared, this bit will be cleared.<br/>1 = S/PDIF out channel interrupt status bits have been set.</p>                                                                                                                                                                                          |
| 25    | <p><b>PCM In 2 Interrupt (P2INT)</b> — RO.</p> <p>0 = When the specific status bit is cleared, this bit will be cleared.<br/>1 = One of the PCM In 2 channel status bits have been set.</p>                                                                                                                                                                                         |
| 24    | <p><b>Microphone 2 In Interrupt (M2INT)</b> — RO.</p> <p>0 = When the specific status bit is cleared, this bit will be cleared.<br/>1 = One of the Mic in channel interrupts status bits has been set.</p>                                                                                                                                                                          |
| 23:22 | <p><b>Sample Capabilities</b> — RO. This field indicates the capability to support greater than 16-bit audio.</p> <p>00 = Reserved<br/>01 = 16 and 20-bit Audio supported (ICH7 value)<br/>10 = Reserved<br/>11 = Reserved</p>                                                                                                                                                      |
| 21:20 | <p><b>Multichannel Capabilities</b> — RO. This field indicates the capability to support more 4 and 6 channels on PCM Out.</p>                                                                                                                                                                                                                                                      |
| 19:18 | Reserved.                                                                                                                                                                                                                                                                                                                                                                           |
| 17    | <p><b>MD3</b> — R/W. Power down semaphore for Modem. This bit exists in the suspend well and maintains context across power states (except G3). The bit has no hardware function. It is used by software in conjunction with the AD3 bit to coordinate the entry of the two codecs into D3 state.</p> <p><b>NOTE:</b> This bit is not affected by D3<sub>HOT</sub> to D0 Reset.</p> |
| 16    | <p><b>AD3</b> — R/W. Power down semaphore for Audio. This bit exists in the suspend well and maintains context across power states (except G3). The bit has no hardware function. It is used by software in conjunction with the MD3 bit to coordinate the entry of the two codecs into D3 state.</p> <p><b>NOTE:</b> This bit is not affected by D3<sub>HOT</sub> to D0 Reset.</p> |
| 15    | <p><b>Read Completion Status (RCS)</b> — R/WC. This bit indicates the status of codec read completions.</p> <p>0 = A codec read completes normally.<br/>1 = A codec read results in a time-out. The bit remains set until being cleared by software writing a 1 to the bit location.</p> <p><b>NOTE:</b> This bit is not affected by D3<sub>HOT</sub> to D0 Reset.</p>              |

| Bit | Description                                                                                                                                                                                                                                                                                                                                                                                                       |
|-----|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 14  | <b>Bit 3 of Slot 12</b> — RO. Display bit 3 of the most recent slot 12.                                                                                                                                                                                                                                                                                                                                           |
| 13  | <b>Bit 2 of Slot 12</b> — RO. Display bit 2 of the most recent slot 12.                                                                                                                                                                                                                                                                                                                                           |
| 12  | <b>Bit 1 of slot 12</b> — RO. Display bit 1 of the most recent slot 12.                                                                                                                                                                                                                                                                                                                                           |
| 11  | <p><b>ACZ_SDIN1 Resume Interrupt (S1R1)</b> — R/WC. This bit indicates that a resume event occurred on ACZ_SDIN1. Software clears this bit by writing a 1 to it.</p> <p>0 = Resume event did Not occur<br/>1 = Resume event occurred.</p> <p><b>NOTE:</b> This bit is not affected by D3<sub>HOT</sub> to D0 Reset.</p>                                                                                           |
| 10  | <p><b>ACZ_SDIN0 Resume Interrupt (S0R1)</b> — R/WC. This bit indicates that a resume event occurred on ACZ_SDIN0. Software clears this bit by writing a 1 to it.</p> <p>0 = Resume event did Not occur<br/>1 = Resume event occurred.</p> <p><b>NOTE:</b> This bit is not affected by D3<sub>HOT</sub> to D0 Reset.</p>                                                                                           |
| 9   | <p><b>ACZ_SDIN1 Codec Ready (S1CR)</b> — RO. Reflects the state of the codec ready bit in ACZ_SDIN1. Bus masters ignore the condition of the codec ready bits, so software must check this bit before starting the bus masters. Once the codec is “ready”, it must never go “not ready” spontaneously.</p> <p>0 = Not Ready.<br/>1 = Ready.</p>                                                                   |
| 8   | <p><b>ACZ_SDIN0 Codec Ready (S0CR)</b> — RO. Reflects the state of the codec ready bit in ACZ_SDIN0. Bus masters ignore the condition of the codec ready bits, so software must check this bit before starting the bus masters. Once the codec is “ready”, it must never go “not ready” spontaneously.</p> <p>0 = Not Ready.<br/>1 = Ready.</p>                                                                   |
| 7   | <p><b>Microphone In Interrupt (MINT)</b> — RO.</p> <p>0 = When the specific status bit is cleared, this bit will be cleared.<br/>1 = One of the Mic in channel interrupts status bits has been set.</p>                                                                                                                                                                                                           |
| 6   | <p><b>PCM Out Interrupt (POINT)</b> — RO.</p> <p>0 = When the specific status bit is cleared, this bit will be cleared.<br/>1 = One of the PCM out channel interrupts status bits has been set.</p>                                                                                                                                                                                                               |
| 5   | <p><b>PCM In Interrupt (PIINT)</b> — RO.</p> <p>0 = When the specific status bit is cleared, this bit will be cleared.<br/>1 = One of the PCM in channel interrupts status bits has been set.</p>                                                                                                                                                                                                                 |
| 4:3 | Reserved                                                                                                                                                                                                                                                                                                                                                                                                          |
| 2   | <p><b>Modem Out Interrupt (MOINT)</b> — RO.</p> <p>0 = When the specific status bit is cleared, this bit will be cleared.<br/>1 = One of the modem out channel interrupts status bits has been set.</p>                                                                                                                                                                                                           |
| 1   | <p><b>Modem In Interrupt (MIINT)</b> — RO.</p> <p>0 = When the specific status bit is cleared, this bit will be cleared.<br/>1 = One of the modem in channel interrupts status bits has been set.</p>                                                                                                                                                                                                             |
| 0   | <p><b>GPI Status Change Interrupt (GSCI)</b> — R/WC.</p> <p>0 = Software clears this bit by writing a 1 to it.<br/>1 = This bit reflects the state of bit 0 in slot 12, and is set when bit 0 of slot 12 is set. This indicates that one of the GPI's changed state, and that the new values are available in slot 12.</p> <p>This bit is not affected by AC '97 Audio Function D3<sub>HOT</sub> to D0 Reset.</p> |

**NOTE:** Reads across DWord boundaries are not supported.

### 2.2.10 CAS—Codec Access Semaphore Register (Audio—D30:F2)

I/O Address: NABMBAR + 34h                      Attribute: R/W (special)  
 Default Value: 00h                                  Size: 8 bits  
 Lockable: No                                              Power Well: Core

| Bit | Description                                                                                                                                                                                                                                                                                                                                                               |
|-----|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:1 | Reserved.                                                                                                                                                                                                                                                                                                                                                                 |
| 0   | <b>Codec Access Semaphore (CAS)</b> — R/W (special). This bit is read by software to check whether a codec access is currently in progress.<br>0 = No access in progress.<br>1 = The act of reading this register sets this bit to 1. The driver that read this bit can then perform an I/O access. Once the access is completed, hardware automatically clears this bit. |

**NOTE:** Reads across DWord boundaries are not supported.

### 2.2.11 SDM—SDATA\_IN Map Register (Audio—D30:F2)

I/O Address: NABMBAR + 80h                      Attribute: R/W, RO  
 Default Value: 00h                                  Size: 8 bits  
 Lockable: No                                              Power Well: Core

| Bit | Description                                                                                                                                                                                                                                                                                                                                                                                                                              |
|-----|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:6 | <b>PCM In 2, Microphone In 2 Data In Line (DI2L)</b> — R/W. When the SE bit is set, these bits indicates which ACZ_SDIN line should be used by the hardware for decoding the input slots for PCM In 2 and Microphone In 2. When the SE bit is cleared, the value of these bits are irrelevant, and PCM In 2 and Mic In 2 DMA engines are not available.<br>00 = ACZ_SDIN0<br>01 = ACZ_SDIN1<br>10 = ACZ_SDIN2<br>11 = Reserved           |
| 5:4 | <b>PCM In 1, Microphone In 1 Data In Line (DI1L)</b> — R/W. When the SE bit is set, these bits indicates which ACZ_SDIN line should be used by the hardware for decoding the input slots for PCM In 1 and Microphone In 1. When the SE bit is cleared, the value of these bits are irrelevant, and the PCM In 1 and Mic In 1 engines use the OR'd ACZ_SDIN lines.<br>00 = ACZ_SDIN0<br>01 = ACZ_SDIN1<br>10 = ACZ_SDIN2<br>11 = Reserved |
| 3   | <b>Steer Enable (SE)</b> — R/W. When set, the ACZ_SDIN lines are treated separately and not OR'd together before being sent to the DMA engines. When cleared, the ACZ_SDIN lines are OR'd together, and the "Microphone In 2" and "PCM In 2" DMA engines are not available.                                                                                                                                                              |
| 2   | Reserved — RO.                                                                                                                                                                                                                                                                                                                                                                                                                           |
| 1:0 | <b>Last Codec Read Data Input (LDI)</b> — RO. When a codec register is read, this indicates which ACZ_SDIN the read data returned on. Software can use this to determine how the codecs are mapped. The values are:<br>00 = ACZ_SDIN0<br>01 = ACZ_SDIN1<br>10 = ACZ_SDIN2<br>11 = Reserved                                                                                                                                               |

**NOTE:** Reads across DWord boundaries are not supported.

§





## 3 AC '97 Modem Controller Registers (D30:F3)

### 3.1 AC '97 Modem PCI Configuration Space (D30:F3)

**Note:** Registers that are not shown should be treated as Reserved.

**Table 3-1. AC '97 Modem PCI Register Address Map (Modem—D30:F3)**

| Offset  | Mnemonic | Register                            | Default                  | Access    |
|---------|----------|-------------------------------------|--------------------------|-----------|
| 00h–01h | VID      | Vendor Identification               | 8086                     | RO        |
| 02h–03h | DID      | Device Identification               | See register description | RO        |
| 04h–05h | PCICMD   | PCI Command                         | 0000h                    | R/W, RO   |
| 06h–07h | PCISTS   | PCI Status                          | 0290h                    | R/WC, RO  |
| 08h     | RID      | Revision Identification             | See register description | RO        |
| 09h     | PI       | Programming Interface               | 00h                      | RO        |
| 0Ah     | SCC      | Sub Class Code                      | 03h                      | RO        |
| 0Bh     | BCC      | Base Class Code                     | 07h                      | RO        |
| 0Eh     | HEADTYP  | Header Type                         | 00h                      | RO        |
| 10h–13h | MMBAR    | Modem Mixer Base Address            | 00000001h                | R/W, RO   |
| 14h–17h | MBAR     | Modem Base Address                  | 00000001h                | R/W, RO   |
| 2Ch–2Dh | SVID     | Subsystem Vendor Identification     | 0000h                    | R/WO      |
| 2Eh–2Fh | SID      | Subsystem Identification            | 0000h                    | R/WO      |
| 34h     | CAP_PTR  | Capabilities Pointer                | 50h                      | RO        |
| 3Ch     | INT_LN   | Interrupt Line                      | 00h                      | R/W       |
| 3Dh     | INT_PN   | Interrupt Pin                       | See register description | RO        |
| 50h–51h | PID      | PCI Power Management Capability ID  | 0001h                    | RO        |
| 52h–53h | PC       | Power Management Capabilities       | C9C2h                    | RO        |
| 54h–55h | PCS      | Power Management Control and Status | 0000h                    | R/W, R/WC |

**Note:** Internal reset as a result of D3<sub>HOT</sub> to D0 transition will reset all the core well registers except the following BIOS programmed registers as BIOS may not be invoked following the D3-to-D0 transition. All resume well registers will not be reset by the D3<sub>HOT</sub> to D0 transition.

Core well registers **not** reset by the D3<sub>HOT</sub> to D0 transition:

- offset 2Ch–2Dh – Subsystem Vendor ID (SVID)
- offset 2Eh–2Fh – Subsystem ID (SID)

Resume well registers **will not** be reset by the D3<sub>HOT</sub> to D0 transition:

- offset 54h–55h – Power Management Control and Status (PCS)

### 3.1.1 VID—Vendor Identification Register (Modem—D30:F3)

|                 |         |             |         |
|-----------------|---------|-------------|---------|
| Address Offset: | 00h–01h | Attribute:  | RO      |
| Default Value:  | 8086    | Size:       | 16 Bits |
| Lockable:       | No      | Power Well: | Core    |

| Bit  | Description                                               |
|------|-----------------------------------------------------------|
| 15:0 | Vendor ID — RO. This is a 16-bit value assigned to Intel. |

### 3.1.2 DID—Device Identification Register (Modem—D30:F3)

|                 |                     |             |         |
|-----------------|---------------------|-------------|---------|
| Address Offset: | 02h–03h             | Attribute:  | RO      |
| Default Value:  | See bit description | Size:       | 16 Bits |
| Lockable:       | No                  | Power Well: | Core    |

| Bit  | Description                                                                                                                                                                                                             |
|------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:0 | Device ID — RO. This is a 16-bit value assigned to the Intel® ICH7 AC '97 Modem controller. Refer to the <i>Intel® I/O Controller Hub 7 (ICH7) Family Specification Update</i> for the value of the Device ID Register. |

### 3.1.3 PCICMD—PCI Command Register (Modem—D30:F3)

|                 |         |             |         |
|-----------------|---------|-------------|---------|
| Address Offset: | 04h–05h | Attribute:  | R/W, RO |
| Default Value:  | 0000h   | Size:       | 16 bits |
| Lockable:       | No      | Power Well: | Core    |

PCICMD is a 16-bit control register. Refer to the *PCI Local Bus Specification* for complete details on each bit.

| Bit   | Description                                                                                                                                                                                                                                                   |
|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:11 | Reserved. Read 0.                                                                                                                                                                                                                                             |
| 10    | <b>Interrupt Disable (ID)</b> — R/W.<br>0 = The INTx# signals may be asserted and MSIs may be generated.<br>1 = The AC '97 controller's INTx# signal will be de-asserted and it may not generate MSIs.                                                        |
| 9     | Fast Back to Back Enable (FBE) — RO. Not implemented. Hardwired to 0.                                                                                                                                                                                         |
| 8     | SERR# Enable (SERR_EN) — RO. Not implemented. Hardwired to 0.                                                                                                                                                                                                 |
| 7     | Wait Cycle Control (WCC) — RO. Not implemented. Hardwired to 0.                                                                                                                                                                                               |
| 6     | Parity Error Response (PER) — RO. Not implemented. Hardwired to 0.                                                                                                                                                                                            |
| 5     | VGA Palette Snoop (VPS) — RO. Not implemented. Hardwired to 0.                                                                                                                                                                                                |
| 4     | Memory Write and Invalidate Enable (MWIE) — RO. Not implemented. Hardwired to 0.                                                                                                                                                                              |
| 3     | Special Cycle Enable (SCE) — RO. Not implemented. Hardwired to 0.                                                                                                                                                                                             |
| 2     | <b>Bus Master Enable (BME)</b> — R/W. This bit controls standard PCI bus mastering capabilities.<br>0 = Disable<br>1 = Enable                                                                                                                                 |
| 1     | Memory Space Enable (MSE) — RO. Hardwired to 0, AC '97 does not respond to memory accesses.                                                                                                                                                                   |
| 0     | <b>I/O Space Enable (IOSE)</b> — R/W. This bit controls access to the I/O space registers.<br>0 = Disable access. (default = 0).<br>1 = Enable access to I/O space. The Native PCI Mode Base Address register should be programmed prior to setting this bit. |

### 3.1.4 PCISTS—PCI Status Register (Modem—D30:F3)

|                 |         |             |          |
|-----------------|---------|-------------|----------|
| Address Offset: | 06h–07h | Attribute:  | R/WC, RO |
| Default Value:  | 0290h   | Size:       | 16 bits  |
| Lockable:       | No      | Power Well: | Core     |

PCISTS is a 16-bit status register. Refer to the *PCI Local Bus Specification* for complete details on each bit.

**Note:** For the writable bits, software must write a 1 to clear bits that are set. Writing a 0 to the bit has no effect.

| Bit  | Description                                                                                                                                                                                     |
|------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15   | Detected Parity Error (DPE) — RO. Not implemented. Hardwired to 0.                                                                                                                              |
| 14   | Signaled System Error (SSE) —RO. Not implemented. Hardwired to 0.                                                                                                                               |
| 13   | <b>Master Abort Status (MAS)</b> — R/WC.<br>0 = Master abort Not generated by bus master AC '97 function.<br>1 = Bus Master AC '97 interface function, as a master, generates a master abort.   |
| 12   | Reserved. Read as 0.                                                                                                                                                                            |
| 11   | Signaled Target Abort (STA) — RO. Not implemented. Hardwired to 0.                                                                                                                              |
| 10:9 | DEVSEL# Timing Status (DEV_STS) — RO. This 2-bit field reflects the ICH7's DEVSEL# timing parameter. These read only bits indicate the ICH7's DEVSEL# timing when performing a positive decode. |
| 8    | Data Parity Error Detected (DPED) — RO. Not implemented. Hardwired to 0.                                                                                                                        |
| 7    | Fast Back to Back Capable (FB2BC) — RO. Hardwired to 1. This bit indicates that the ICH7 as a target is capable of fast back-to-back transactions.                                              |
| 6    | User Definable Features (UDF) — RO. Not implemented. Hardwired to 0.                                                                                                                            |
| 5    | 66 MHz Capable (66MHZ_CAP) — RO. Hardwired to 0.                                                                                                                                                |
| 4    | Capabilities List (CAP_LIST) — RO. Indicates that the controller contains a capabilities pointer list. The first item is pointed to by looking at configuration offset 34h.                     |
| 3    | <b>Interrupt Status (INTS)</b> — RO.<br>0 = This bit is 0 after the interrupt is cleared.<br>1 = This bit is 1 when the INTx# is asserted.                                                      |
| 2:0  | Reserved                                                                                                                                                                                        |





### 3.1.11 MBAR—Modem Base Address Register (Modem—D30:F3)

Address Offset: 14h–17h                      Attribute: R/W, RO  
 Default Value: 00000001h                  Size: 32 bits

The Modem function uses PCI Base Address register #1 to request a contiguous block of I/O space that is to be used for the Modem software interface. The Modem Bus Mastering register space requires 128 bytes of I/O space. All Modem registers reside in the controller, therefore cycles are **not** forwarded over the AC-link to the codec.

| Bit   | Description                                                                                                                                                                                                                                                                                                                                                                                                                   |
|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16 | Hardwired to 0's.                                                                                                                                                                                                                                                                                                                                                                                                             |
| 15:7  | <b>Base Address</b> — R/W. These bits are used in the I/O space decode of the Modem interface registers. The number of upper bits that a device actually implements depends on how much of the address space the device will respond to. For the AC '97 Modem, the upper 16 bits are hardwired to 0, while bits 15:7 are programmable. This configuration yields a maximum I/O block size of 128 bytes for this base address. |
| 6:1   | Reserved. Read as 0                                                                                                                                                                                                                                                                                                                                                                                                           |
| 0     | Resource Type Indicator (RTE) — RO. Hardwired to 1 indicating a request for I/O space.                                                                                                                                                                                                                                                                                                                                        |

### 3.1.12 SVID—Subsystem Vendor Identification Register (Modem—D30:F3)

Address Offset: 2Ch–2Dh                      Attribute: R/WO  
 Default Value: 0000h                        Size: 16 bits  
 Lockable: No                                  Power Well: Core

The SVID register, in combination with the Subsystem ID register, enable the operating environment to distinguish one audio subsystem from the other(s). This register is implemented as write-once register. Once a value is written to it, the value can be read back. Any subsequent writes will have no effect.

This register is not affected by the D3<sub>HOT</sub> to D0 transition.

| Bit  | Description                        |
|------|------------------------------------|
| 15:0 | <b>Subsystem Vendor ID</b> — R/WO. |

### 3.1.13 SID—Subsystem Identification Register (Modem—D30:F3)

|                 |         |             |         |
|-----------------|---------|-------------|---------|
| Address Offset: | 2Eh–2Fh | Attribute:  | R/WO    |
| Default Value:  | 0000h   | Size:       | 16 bits |
| Lockable:       | No      | Power Well: | Core    |

The SID register, in combination with the Subsystem Vendor ID register make it possible for the operating environment to distinguish one audio subsystem from another. This register is implemented as write-once register. Once a value is written to it, the value can be read back. Any subsequent writes will have no effect.

This register is not affected by the D3<sub>HOT</sub> to D0 transition.

| Bit  | Description          |
|------|----------------------|
| 15:0 | Subsystem ID — R/WO. |

### 3.1.14 CAP\_PTR—Capabilities Pointer Register (Modem—D30:F3)

|                 |     |             |        |
|-----------------|-----|-------------|--------|
| Address Offset: | 34h | Attribute:  | RO     |
| Default Value:  | 50h | Size:       | 8 bits |
| Lockable:       | No  | Power Well: | Core   |

This register indicates the offset for the capability pointer.

| Bit | Description                                                                                                       |
|-----|-------------------------------------------------------------------------------------------------------------------|
| 7:0 | Capabilities Pointer (CAP_PTR) — RO. This field indicates that the first capability pointer offset is offset 50h. |

### 3.1.15 INT\_LN—Interrupt Line Register (Modem—D30:F3)

|                 |     |             |        |
|-----------------|-----|-------------|--------|
| Address Offset: | 3Ch | Attribute:  | R/W    |
| Default Value:  | 00h | Size:       | 8 bits |
| Lockable:       | No  | Power Well: | Core   |

This register indicates which PCI interrupt line is used for the AC '97 module interrupt.

| Bit | Description                                                                                                                                                                           |
|-----|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:0 | Interrupt Line (INT_LN) — R/W. This data is not used by the Intel <sup>®</sup> ICH7. It is used to communicate to software the interrupt line that is connected to the interrupt pin. |

### 3.1.16 INT\_PIN—Interrupt Pin Register (Modem—D30:F3)

|                 |                 |             |        |
|-----------------|-----------------|-------------|--------|
| Address Offset: | 3Dh             | Attribute:  | RO     |
| Default Value:  | See description | Size:       | 8 bits |
| Lockable:       | No              | Power Well: | Core   |

This register indicates which PCI interrupt pin is used for the AC '97 modem interrupt. The AC '97 interrupt is internally OR'd to the interrupt controller with the PIRQB# signal.

| Bit | Description                                                                                        |
|-----|----------------------------------------------------------------------------------------------------|
| 7:3 | Reserved                                                                                           |
| 2:0 | Interrupt Pin (INT_PN) — RO. This reflects the value of D30IP.AMIP in chipset configuration space. |

### 3.1.17 PID—PCI Power Management Capability Identification Register (Modem—D30:F3)

|                 |       |             |         |
|-----------------|-------|-------------|---------|
| Address Offset: | 50h   | Attribute:  | RO      |
| Default Value:  | 0001h | Size:       | 16 bits |
| Lockable:       | No    | Power Well: | Core    |

| Bit  | Description                                                                                                  |
|------|--------------------------------------------------------------------------------------------------------------|
| 15:8 | Next Capability (NEXT) — RO. This field indicates that this is the last item in the list.                    |
| 7:0  | Capability ID (CAP) — RO. This field indicates that this pointer is a message signaled interrupt capability. |

### 3.1.18 PC—Power Management Capabilities Register (Modem—D30:F3)

|                 |       |             |         |
|-----------------|-------|-------------|---------|
| Address Offset: | 52h   | Attribute:  | RO      |
| Default Value:  | C9C2h | Size:       | 16 bits |
| Lockable:       | No    | Power Well: | Core    |

| Bit   | Description                                                                                                                   |
|-------|-------------------------------------------------------------------------------------------------------------------------------|
| 15:11 | PME Support — RO. This field indicates PME# can be generated from all D states.                                               |
| 10:9  | Reserved.                                                                                                                     |
| 8:6   | Auxiliary Current — RO. This field reports 375 mA maximum Suspend well current required when in the D3 <sub>COLD</sub> state. |
| 5     | Device Specific Initialization (DSI) — RO. This bit indicates that no device-specific initialization is required.             |
| 4     | Reserved — RO.                                                                                                                |
| 3     | PME Clock (PMEC) — RO. This bit indicates that PCI clock is not required to generate PME#.                                    |
| 2:0   | Version (VS) — RO. This field indicates support for Revision 1.1 of the PCI Power Management Specification.                   |



### 3.1.19 PCS—Power Management Control and Status Register (Modem—D30:F3)

|                 |       |             |           |
|-----------------|-------|-------------|-----------|
| Address Offset: | 54h   | Attribute:  | R/W, R/WC |
| Default Value:  | 0000h | Size:       | 16 bits   |
| Lockable:       | No    | Power Well: | Resume    |

This register is not affected by the D3<sub>HOT</sub> to D0 transition.

| Bit  | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
|------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15   | <p><b>PME Status (PMES)</b> — R/WC.</p> <p>0 = Software clears this bit by writing a 1 to it.<br/>           1 = This bit is set when the AC '97 controller would normally assert the PME# signal independent of the state of the PME_En bit. This bit resides in the resume well.</p>                                                                                                                                                                                                                                                                                                                                                                                              |
| 14:9 | Reserved — RO.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
| 8    | <p><b>PME Enable (PMEE)</b> — R/W.</p> <p>0 = Disable.<br/>           1 = Enable. When set, and if corresponding PMES is also set, the AC '97 controller sets the AC97_STS bit in the GPE0_STS register.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
| 7:2  | Reserved — RO.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
| 1:0  | <p><b>Power State (PS)</b> — R/W. This field is used both to determine the current power state of the AC '97 controller and to set a new power state. The values are:</p> <p>00 = D0 state<br/>           01 = not supported<br/>           10 = not supported<br/>           11 = D3<sub>HOT</sub> state</p> <p>When in the D3<sub>HOT</sub> state, the AC '97 controller's configuration space is available, but the I/O and memory spaces are not. Additionally, interrupts are blocked.</p> <p>If software attempts to write a value of 10b or 01b in to this field, the write operation must complete normally; however, the data is discarded and no state change occurs.</p> |

## 3.2 AC '97 Modem I/O Space (D30:F3)

In the case of the split codec implementation accesses to the modem mixer registers in different codecs are differentiated by the controller by using address offsets 00h–7Fh for the primary codec and address offsets 80h–FEh for the secondary codec. Table 3-2 shows the register addresses for the modem mixer registers.

**Table 3-2. Intel® ICH7 Modem Mixer Register Configuration**

| Register   |            | MMBAR Exposed Registers (D30:F3)  |
|------------|------------|-----------------------------------|
| Primary    | Secondary  | Name                              |
| 00h:38h    | 80h:B8h    | Intel RESERVED                    |
| 3Ch        | BCh        | Extended Modem ID                 |
| 3Eh        | BEh        | Extended Modem Stat/Ctrl          |
| 40h        | C0h        | Line 1 DAC/ADC Rate               |
| <i>42h</i> | <i>C2h</i> | <i>Line 2 DAC/ADC Rate</i>        |
| <i>44h</i> | <i>C4h</i> | <i>Handset DAC/ADC Rate</i>       |
| 46h        | C6h        | Line 1 DAC/ADC Level Mute         |
| <i>48h</i> | <i>C8h</i> | <i>Line 2 DAC/ADC Level Mute</i>  |
| <i>4Ah</i> | <i>CAh</i> | <i>Handset DAC/ADC Level Mute</i> |
| 4Ch        | CCh        | GPIO Pin Config                   |
| 4Eh        | CEh        | GPIO Polarity/Type                |
| 50h        | D0h        | GPIO Pin Sticky                   |
| 52h        | D2h        | GPIO Pin Wake Up                  |
| 54h        | D4h        | GPIO Pin Status                   |
| 56h        | D6h        | Misc. Modem AFE Stat/Ctrl         |
| 58h        | D8h        | AC '97 Reserved                   |
| 5Ah        | DAh        | Vendor Reserved                   |
| 7Ch        | FCh        | Vendor ID1                        |
| 7Eh        | FEh        | Vendor ID2                        |

**NOTES:**

1. Registers in italics are for functions not supported by the ICH7.
2. Software should not try to access reserved registers.
3. The ICH7 supports a modem codec connected to ACZ\_SDIN[2:0], as long as the Codec ID is 00 or 01. However, the ICH7 does not support more than one modem codec. For a complete list of topologies, see your ICH7 enabled Platform Design Guide.

The Global Control (GLOB\_CNT) and Global Status (GLOB\_STA) registers are aliased to the same global registers in the audio and modem I/O space. Therefore a read/write to these registers in either audio or modem I/O space affects the same physical register. Software could access these registers as bytes, word, DWord quantities, but reads must not cross DWord boundaries.

These registers exist in I/O space and reside in the AC '97 controller. The two channels, Modem in and Modem out, each have their own set of Bus Mastering registers. The following register descriptions apply to both channels. The naming prefix convention used is as follows:

MI = Modem in channel  
MO = Modem out channel

**Table 3-3. Modem Registers**

| Offset  | Mnemonic | Name                                          | Default   | Access                |
|---------|----------|-----------------------------------------------|-----------|-----------------------|
| 00h–03h | MI_BDBAR | Modem In Buffer Descriptor List Base Address  | 00000000h | R/W                   |
| 04h     | MI_CIV   | Modem In Current Index Value                  | 00h       | RO                    |
| 05h     | MI_LVI   | Modem In Last Valid Index                     | 00h       | R/W                   |
| 06h–07h | MI_SR    | Modem In Status                               | 0001h     | R/WC, RO              |
| 08h–09h | MI_PICB  | Modem In Position In Current Buffer           | 0000h     | RO                    |
| 0Ah     | MI_PIV   | Modem In Prefetch Index Value                 | 00h       | RO                    |
| 0Bh     | MI_CR    | Modem In Control                              | 00h       | R/W,<br>R/W (special) |
| 10h–13h | MO_BDBAR | Modem Out Buffer Descriptor List Base Address | 00000000h | R/W                   |
| 14h     | MO_CIV   | Modem Out Current Index Value                 | 00h       | RO                    |
| 15h     | MO_LVI   | Modem Out Last Valid                          | 00h       | R/W                   |
| 16h–17h | MO_SR    | Modem Out Status                              | 0001h     | R/WC, RO              |
| 18h–19h | MI_PICB  | Modem In Position In Current Buffer           | 0000h     | RO                    |
| 1Ah     | MO_PIV   | Modem Out Prefetched Index                    | 00h       | RO                    |
| 1Bh     | MO_CR    | Modem Out Control                             | 00h       | R/W,<br>R/W (special) |
| 3Ch–3Fh | GLOB_CNT | Global Control                                | 00000000h | R/W,<br>R/W (special) |
| 40h–43h | GLOB_STA | Global Status                                 | 00300000h | RO, R/W,<br>R/WC      |
| 44h     | CAS      | Codec Access Semaphore                        | 00h       | R/W (special)         |

**NOTE:**

- MI = Modem in channel; MO = Modem out channel

**Note:** Internal reset as a result of D3<sub>HOT</sub> to D0 transition will reset all the core well registers except the registers shared with the AC '97 audio controller (GCR, GSR, CASR). All resume well registers will not be reset by the D3<sub>HOT</sub> to D0 transition.

Core well registers and bits **not** reset by the D3<sub>HOT</sub> to D0 transition:

- offset 3Ch–3Fh – bits [6:0] Global Control (GLOB\_CNT)
- offset 40h–43h – bits [29,15,11:10] Global Status (GLOB\_STA)
- offset 44h – Codec Access Semaphore Register (CAS)

Resume well registers and bits **will not** be reset by the D3<sub>HOT</sub> to D0 transition:

- offset 40h–43h – bits [17:16] Global Status (GLOB\_STA)

### 3.2.1 **x\_BDBAR—Buffer Descriptor List Base Address Register (Modem—D30:F3)**

|                |                                               |             |        |
|----------------|-----------------------------------------------|-------------|--------|
| I/O Address:   | MBAR + 00h (MIBDBAR),<br>MBAR + 10h (MOBDBAR) | Attribute:  | R/W    |
| Default Value: | 00000000h                                     | Size:       | 32bits |
| Lockable:      | No                                            | Power Well: | Core   |

Software can read the register at offset 00h by performing a single, 32-bit read from address offset 00h. Reads across DWord boundaries are not supported.

| Bit  | Description                                                                                                                                          |
|------|------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:3 | <b>Buffer Descriptor List Base Address [31:3]</b> — R/W. These bits represent address bits 31:3. The entries should be aligned on 8-byte boundaries. |
| 2:0  | Hardwired to 0.                                                                                                                                      |

### 3.2.2 **x\_CIV—Current Index Value Register (Modem—D30:F3)**

|                |                                            |             |       |
|----------------|--------------------------------------------|-------------|-------|
| I/O Address:   | MBAR + 04h (MICIV),<br>MBAR + 14h (MOCIV), | Attribute:  | RO    |
| Default Value: | 00h                                        | Size:       | 8bits |
| Lockable:      | No                                         | Power Well: | Core  |

Software can read the registers at offsets 04h, 05h and 06h simultaneously by performing a single, 32-bit read from address offset 04h. Software can also read this register individually by doing a single, 8-bit read to offset 04h. Reads across DWord boundaries are not supported.

| Bit | Description                                                                                                                                                                                                     |
|-----|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:5 | Hardwired to 0.                                                                                                                                                                                                 |
| 4:0 | <b>Current Index Value [4:0]</b> — RO. These bits represent which buffer descriptor within the list of 16 descriptors is being processed currently. As each descriptor is processed, this value is incremented. |

### 3.2.3 **x\_LVI—Last Valid Index Register (Modem—D30:F3)**

|                |                                           |             |      |
|----------------|-------------------------------------------|-------------|------|
| I/O Address:   | MBAR + 05h (MILVI),<br>MBAR + 15h (MOLVI) | Attribute:  | R/W  |
| Default Value: | 00h                                       | Power Well: | Core |

Software can read the registers at offsets 04h, 05h and 06h simultaneously by performing a single, 32-bit read from address offset 04h. Software can also read this register individually by doing a single, 8-bit read to offset 05h. Reads across DWord boundaries are not supported.

| Bit | Description                                                                                                                                                                            |
|-----|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:5 | Hardwired to 0                                                                                                                                                                         |
| 4:0 | <b>Last Valid Index [4:0]</b> — R/W. These bits indicate the last valid descriptor in the list. This value is updated by the software as it prepares new buffers and adds to the list. |

### 3.2.4 x\_SR—Status Register (Modem—D30:F3)

|                |                                         |             |          |
|----------------|-----------------------------------------|-------------|----------|
| I/O Address:   | MBAR + 06h (MISR),<br>MBAR + 16h (MOSR) | Attribute:  | R/WC, RO |
| Default Value: | 0001h                                   | Size:       | 16 bits  |
| Lockable:      | No                                      | Power Well: | Core     |

Software can read the registers at offsets 04h, 05h and 06h simultaneously by performing a single, 32-bit read from address offset 04h. Software can also read this register individually by doing a single, 16-bit read to offset 06h. Reads across DWord boundaries are not supported.

| Bit  | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
|------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:5 | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
| 4    | <p><b>FIFO Error (FIFOE) — R/WC.</b><br/>                     0 = Software clears this bit by writing a 1 to it.<br/>                     1 = FIFO error occurs.</p> <p><b>Modem in:</b> FIFO error indicates a FIFO overrun. The FIFO pointers don't increment, the incoming data is not written into the FIFO, thereby being lost.</p> <p><b>Modem out:</b> FIFO error indicates a FIFO underrun. The sample transmitted in this case should be the last valid sample.</p> <p>The ICH7 will set the FIFO bit if the under-run or overrun occurs when there are more valid buffers to process.</p>                                                                                                                                                                                                                                                                                                            |
| 3    | <p><b>Buffer Completion Interrupt Status (BCIS) — R/WC.</b><br/>                     0 = Software clears this bit by writing a 1 to it.<br/>                     1 = Set by the hardware after the last sample of a buffer has been processed, AND if the Interrupt on Completion (IOC) bit is set in the command byte of the buffer descriptor. Remains active until software clears bit.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
| 2    | <p><b>Last Valid Buffer Completion Interrupt (LVBCI) — R/WC.</b><br/>                     0 = Software clears this bit by writing a 1 to it.<br/>                     1 = Set by hardware when last valid buffer has been processed. It remains active until cleared by software. This bit indicates the occurrence of the event signified by the last valid buffer being processed. Thus, this is an event status bit that can be cleared by software once this event has been recognized. This event will cause an interrupt if the enable bit in the Control Register is set. The interrupt is cleared when the software clears this bit.</p> <p>In the case of transmits (PCM out, Modem out) this bit is set, after the last valid buffer has been fetched (not after transmitting it). While in the case of Receives, this bit is set after the data for the last buffer has been written to memory.</p> |
| 1    | <p><b>Current Equals Last Valid (CELV) — RO.</b><br/>                     0 = Hardware clears when controller exists state (i.e., until a new value is written to the LVI register).<br/>                     1 = Current Index is equal to the value in the Last Valid Index Register, AND the buffer pointed to by the CIV has been processed (i.e., after the last valid buffer has been processed). This bit is very similar to bit 2, except this bit reflects the state rather than the event. This bit reflects the state of the controller, and remains set until the controller exits this state.</p>                                                                                                                                                                                                                                                                                                 |
| 0    | <p><b>DMA Controller Halted (DCH) — RO.</b><br/>                     0 = Running.<br/>                     1 = Halted. This could happen because of the Start/Stop bit being cleared and the DMA engines are idle, or it could happen once the controller has processed the last valid buffer.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |

### 3.2.5 x\_PICB—Position in Current Buffer Register (Modem—D30:F3)

|                |                                              |             |         |
|----------------|----------------------------------------------|-------------|---------|
| I/O Address:   | MBAR + 08h (MIPICB),<br>MBAR + 18h (MOPICB), | Attribute:  | RO      |
| Default Value: | 0000h                                        | Size:       | 16 bits |
| Lockable:      | No                                           | Power Well: | Core    |

Software can read the registers at the offsets 08h, 0Ah, and 0Bh by performing a 32-bit read from the address offset 08h. Software can also read this register individually by doing a single, 16-bit read to offset 08h. Reads across DWord boundaries are not supported.

| Bit  | Description                                                                                                                          |
|------|--------------------------------------------------------------------------------------------------------------------------------------|
| 15:0 | <b>Position In Current Buffer[15:0]</b> — RO. These bits represent the number of samples left to be processed in the current buffer. |

### 3.2.6 x\_PIV—Prefetch Index Value Register (Modem—D30:F3)

|                |                                           |             |        |
|----------------|-------------------------------------------|-------------|--------|
| I/O Address:   | MBAR + 0Ah (MIPIV),<br>MBAR + 1Ah (MOPIV) | Attribute:  | RO     |
| Default Value: | 00h                                       | Size:       | 8 bits |
| Lockable:      | No                                        | Power Well: | Core   |

Software can read the registers at the offsets 08h, 0Ah, and 0Bh by performing a 32-bit read from the address offset 08h. Software can also read this register individually by doing a single, 8-bit read to offset 0Ah. Reads across DWord boundaries are not supported.

| Bit | Description                                                                                                             |
|-----|-------------------------------------------------------------------------------------------------------------------------|
| 7:5 | Hardwired to 0                                                                                                          |
| 4:0 | <b>Prefetched Index Value [4:0]</b> — RO. These bits represent which buffer descriptor in the list has been prefetched. |

### 3.2.7 x\_CR—Control Register (Modem—D30:F3)

|                |                                         |             |                    |
|----------------|-----------------------------------------|-------------|--------------------|
| I/O Address:   | MBAR + 0Bh (MICR),<br>MBAR + 1Bh (MOCR) | Attribute:  | R/W, R/W (special) |
| Default Value: | 00h                                     | Size:       | 8 bits             |
| Lockable:      | No                                      | Power Well: | Core               |

Software can read the registers at the offsets 08h, 0Ah, and 0Bh by performing a 32-bit read from the address offset 08h. Software can also read this register individually by doing a single, 8-bit read to offset 0Bh. Reads across DWord boundaries are not supported.

| Bit | Description                                                                                                                                                                                                                                                                                                                                                                                                     |
|-----|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:5 | Reserved                                                                                                                                                                                                                                                                                                                                                                                                        |
| 4   | <b>Interrupt on Completion Enable (IOCE)</b> — R/W. This bit controls whether or not an interrupt occurs when a buffer completes with the IOC bit set in its descriptor.<br>0 = Disable<br>1 = Enable                                                                                                                                                                                                           |
| 3   | <b>FIFO Error Interrupt Enable (FEIE)</b> — R/W. This bit controls whether the occurrence of a FIFO error will cause an interrupt or not.<br>0 = Disable. Bit 4 in the Status Register will be set, but the interrupt will not occur.<br>1 = Enable. Interrupt will occur.                                                                                                                                      |
| 2   | <b>Last Valid Buffer Interrupt Enable (LVBIE)</b> — R/W. This bit controls whether the completion of the last valid buffer will cause an interrupt or not.<br>0 = Disable. Bit 2 in the Status register will still be set, but the interrupt will not occur.<br>1 = Enable                                                                                                                                      |
| 1   | <b>Reset Registers (RR)</b> — R/W (special).<br>0 = Removes reset condition.<br>1 = Contents of all registers to be reset, except the interrupt enable bits (bit 4,3,2 of this register). Software needs to set this bit. It must be set only when the Run/Pause bit is cleared. Setting it when the Run bit is set will cause undefined consequences. This bit is self-clearing (software needs not clear it). |
| 0   | <b>Run/Pause Bus Master (RPBM)</b> — R/W.<br>0 = Pause bus master operation. This results in all state information being retained (i.e., master mode operation can be stopped and then resumed).<br>1 = Run. Bus master operation starts.                                                                                                                                                                       |

### 3.2.8 GLOB\_CNT—Global Control Register (Modem—D30:F3)

|                |            |             |                    |
|----------------|------------|-------------|--------------------|
| I/O Address:   | MBAR + 3Ch | Attribute:  | R/W, R/W (special) |
| Default Value: | 00000000h  | Size:       | 32 bits            |
| Lockable:      | No         | Power Well: | Core               |

| Bit  | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
|------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:6 | Reserved.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
| 6    | <b>ACZ_SDIN2 Interrupt Enable (S2RE)</b> — R/W.<br>0 = Disable.<br>1 = Enable an interrupt to occur when the codec on the ACZ_SDIN2 causes a resume event on the AC-link.                                                                                                                                                                                                                                                                                                                                                                                                                      |
| 5    | <b>ACZ_SDIN1 Resume Interrupt Enable (S1RE)</b> — R/W.<br>0 = Disable.<br>1 = Enable an interrupt to occur when the codec on the ACZ_SDIN1 causes a resume event on the AC-link.                                                                                                                                                                                                                                                                                                                                                                                                               |
| 4    | <b>ACZ_SDIN0 Resume Interrupt Enable (S0RE)</b> — R/W.<br>0 = Disable.<br>1 = Enable an interrupt to occur when the codec on ACZ_SDIN0 causes a resume event on the AC-link.                                                                                                                                                                                                                                                                                                                                                                                                                   |
| 3    | <b>AC-LINK Shut Off (LSO)</b> — R/W.<br>0 = Normal operation.<br>1 = Controller disables all outputs which will be pulled low by internal pull down resistors.                                                                                                                                                                                                                                                                                                                                                                                                                                 |
| 2    | <b>AC '97 Warm Reset</b> — R/W (special).<br>0 = Normal operation.<br>1 = Writing a 1 to this bit causes a warm reset to occur on the AC-link. The warm reset will awaken a suspended codec without clearing its internal registers. If software attempts to perform a warm reset while bit_clk is running, the write will be ignored and the bit will not change. This bit is self-clearing (it remains set until the reset completes and bit_clk is seen on the AC-link, after which it clears itself).                                                                                      |
| 1    | <b>AC '97 Cold Reset#</b> — R/W.<br>0 = Writing a 0 to this bit causes a cold reset to occur throughout the AC '97 circuitry. All data in the controller and the codec will be lost. Software needs to clear this bit no sooner than the minimum number of ms have elapsed.<br>1 = This bit defaults to 0 and hence after reset, the driver needs to set this bit to a 1. The value of this bit is retained after suspends; hence, if this bit is set to a 1 prior to suspending, a cold reset is not generated automatically upon resuming.<br><br><b>NOTE:</b> This bit is in the Core well. |
| 0    | <b>GPI Interrupt Enable (GIE)</b> — R/W. This bit controls whether the change in status of any GPI causes an interrupt.<br>0 = Bit 0 of the Global Status Register is set, but no interrupt is generated.<br>1 = The change in value of a GPI causes an interrupt and sets bit 0 of the Global Status Register.<br><br><b>NOTE:</b> This bit is cleared by the AC '97 Modem function D3 <sub>HOT</sub> to D0 reset.                                                                                                                                                                            |

**Note:** Reads across DWord boundaries are not supported.



### 3.2.9 GLOB\_STA—Global Status Register (Modem—D30:F3)

|                |            |             |               |
|----------------|------------|-------------|---------------|
| I/O Address:   | MBAR + 40h | Attribute:  | RO, R/W, R/WC |
| Default Value: | 00300000h  | Size:       | 32 bits       |
| Lockable:      | No         | Power Well: | Core          |

| Bit   | Description                                                                                                                                                                                                                                                                                                                                                               |
|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:30 | Reserved.                                                                                                                                                                                                                                                                                                                                                                 |
| 29    | <b>ACZ_SDIN2 Resume Interrupt (S2RI)</b> — R/WC. This bit indicates a resume event occurred on ACZ_SDIN2.<br>0 = Software clears this bit by writing a 1 to it.<br>1 = Resume event occurred.<br><b>NOTE:</b> This bit is not affected by D3 <sub>HOT</sub> to D0 Reset.                                                                                                  |
| 28    | <b>ACZ_SDIN2 Codec Ready (S2CR)</b> — RO. This bit reflects the state of the codec ready bit on ACZ_SDIN2. Bus masters ignore the condition of the codec ready bits, so software must check this bit before starting the bus masters. Once the codec is “ready”, it must never go “not ready” spontaneously.<br>0 = Not Ready.<br>1 = Ready.                              |
| 27    | <b>Bit Clock Stopped (BCS)</b> — RO. This bit indicates that the bit clock is not running.<br>0 = Transition is found on BIT_CLK.<br>1 = Intel® ICH7 detects that there has been no transition on BIT_CLK for four consecutive PCI clocks.                                                                                                                                |
| 26    | <b>S/PDIF* Interrupt (SPINT)</b> — RO.<br>0 = When the specific status bit is cleared, this bit will be cleared.<br>1 = S/PDIF out channel interrupt status bits have been set.                                                                                                                                                                                           |
| 25    | <b>PCM In 2 Interrupt (P2INT)</b> — RO.<br>0 = When the specific status bit is cleared, this bit will be cleared.<br>1 = One of the PCM In 2 channel status bits have been set.                                                                                                                                                                                           |
| 24    | <b>Microphone 2 In Interrupt (M2INT)</b> — RO.<br>0 = When the specific status bit is cleared, this bit will be cleared.<br>1 = One of the Mic in channel interrupts status bits has been set.                                                                                                                                                                            |
| 23:22 | <b>Sample Capabilities</b> — RO. This field indicates the capability to support greater than 16-bit audio.<br>00 = Reserved<br>01 = 16 and 20-bit Audio supported (ICH7 value)<br>10 = Reserved<br>11 = Reserved                                                                                                                                                          |
| 21:20 | <b>Multichannel Capabilities</b> — RO. This field indicates the capability to support 4 and 6 channels on PCM Out.                                                                                                                                                                                                                                                        |
| 19:18 | Reserved.                                                                                                                                                                                                                                                                                                                                                                 |
| 17    | <b>MD3</b> — R/W. Power down semaphore for Modem. This bit exists in the suspend well and maintains context across power states (except G3). The bit has no hardware function. It is used by software in conjunction with the AD3 bit to coordinate the entry of the two codecs into D3 state.<br><b>NOTE:</b> This bit is not affected by D3 <sub>HOT</sub> to D0 Reset. |
| 16    | <b>AD3</b> — R/W. Power down semaphore for Audio. This bit exists in the suspend well and maintains context across power states (except G3). The bit has no hardware function. It is used by software in conjunction with the MD3 bit to coordinate the entry of the two codecs into D3 state.<br><b>NOTE:</b> This bit is not affected by D3 <sub>HOT</sub> to D0 Reset. |
| 15    | <b>Read Completion Status (RCS)</b> — R/WC. This bit indicates the status of codec read completions. Software clears this bit by writing a 1 to it.<br>0 = A codec read completes normally.<br>1 = A codec read results in a time-out.<br><b>NOTE:</b> This bit is not affected by D3 <sub>HOT</sub> to D0 Reset.                                                         |
| 14    | <b>Bit 3 of Slot 12</b> — RO. Display bit 3 of the most recent slot 12.                                                                                                                                                                                                                                                                                                   |

| Bit | Description                                                                                                                                                                                                                                                                                                                                                                                                                           |
|-----|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 13  | <b>Bit 2 of Slot 12</b> — RO. Display bit 2 of the most recent slot 12.                                                                                                                                                                                                                                                                                                                                                               |
| 12  | <b>Bit 1 of Slot 12</b> — RO. Display bit 1 of the most recent slot 12.                                                                                                                                                                                                                                                                                                                                                               |
| 11  | <p><b>ACZ_SDIN1 Resume Interrupt (S1RI)</b> — R/WC. This bit indicates that a resume event occurred on ACZ_SDIN1. Software clears this bit by writing a 1 to it.</p> <p>0 = Resume event did Not occur.<br/>1 = Resume event occurred.</p> <p><b>NOTE:</b> This bit is not affected by D3<sub>HOT</sub> to D0 Reset.</p>                                                                                                              |
| 10  | <p><b>ACZ_SDIN0 Resume Interrupt (S0RI)</b> — R/WC. This bit indicates that a resume event occurred on ACZ_SDIN0. Software clears this bit by writing a 1 to it.</p> <p>0 = Resume event did Not occur.<br/>1 = Resume event occurred.</p> <p><b>NOTE:</b> This bit is not affected by D3<sub>HOT</sub> to D0 Reset.</p>                                                                                                              |
| 9   | <p><b>ACZ_SDIN1 Codec Ready (S1CR)</b> — RO. This bit reflects the state of the codec ready bit in ACZ_SDIN1. Bus masters ignore the condition of the codec ready bits, so software must check this bit before starting the bus masters. Once the codec is “ready”, it must never go “not ready” spontaneously.</p> <p>0 = Not Ready.<br/>1 = Ready.</p>                                                                              |
| 8   | <p><b>ACZ_SDIN0 Codec Ready (S0CR)</b> — RO. This bit reflects the state of the codec ready bit in ACZ_SDIN 0. Bus masters ignore the condition of the codec ready bits, so software must check this bit before starting the bus masters. Once the codec is “ready”, it must never go “not ready” spontaneously.</p> <p>0 = Not Ready.<br/>1 = Ready.</p>                                                                             |
| 7   | <p><b>Microphone In Interrupt (MINT)</b> — RO.</p> <p>0 = When the specific status bit is cleared, this bit will be cleared.<br/>1 = One of the Mic in channel interrupts status bits has been set.</p>                                                                                                                                                                                                                               |
| 6   | <p><b>PCM Out Interrupt (POINT)</b> — RO.</p> <p>0 = When the specific status bit is cleared, this bit will be cleared.<br/>1 = One of the PCM out channel interrupts status bits has been set.</p>                                                                                                                                                                                                                                   |
| 5   | <p><b>PCM In Interrupt (PIINT)</b> — RO.</p> <p>0 = When the specific status bit is cleared, this bit will be cleared.<br/>1 = One of the PCM in channel interrupts status bits has been set.</p>                                                                                                                                                                                                                                     |
| 4:3 | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                              |
| 2   | <p><b>Modem Out Interrupt (MOINT)</b> — RO.</p> <p>0 = When the specific status bit is cleared, this bit will be cleared.<br/>1 = One of the modem out channel interrupts status bits has been set.</p>                                                                                                                                                                                                                               |
| 1   | <p><b>Modem In Interrupt (MIINT)</b> — RO.</p> <p>0 = When the specific status bit is cleared, this bit will be cleared.<br/>1 = One of the modem in channel interrupts status bits has been set.</p>                                                                                                                                                                                                                                 |
| 0   | <p><b>GPI Status Change Interrupt (GSCI)</b> — R/WC.</p> <p>0 = Software clears this bit by writing a 1 to it.<br/>1 = This bit reflects the state of bit 0 in slot 12, and is set when bit 0 of slot 12 is set. This indicates that one of the GPI's changed state, and that the new values are available in slot 12.</p> <p><b>NOTE:</b> This bit has not affected by AC '97 Audio Modem function D3<sub>HOT</sub> to D0 Reset.</p> |

**Note:** On reads from a codec, the controller will give the codec a maximum of four frames to respond, after which if no response is received, it will return a dummy read completion to the processor (with all F's on the data) and also set the Read Completion Status bit in the Global Status Register.

**Note:** Reads across DWord boundaries are not supported.

### 3.2.10 CAS—Codec Access Semaphore Register (Modem—D30:F3)

|                |               |             |               |
|----------------|---------------|-------------|---------------|
| I/O Address:   | NABMBAR + 44h | Attribute:  | R/W (special) |
| Default Value: | 00h           | Size:       | 8 bits        |
| Lockable:      | No            | Power Well: | Core          |

| Bit | Description                                                                                                                                                                                                                                                                                                                                                                                      |
|-----|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:1 | Reserved                                                                                                                                                                                                                                                                                                                                                                                         |
| 0   | <p><b>Codec Access Semaphore (CAS)</b> — R/W (special). This bit is read by software to check whether a codec access is currently in progress.</p> <p>0 = No access in progress.<br/>           1 = The act of reading this register sets this bit to 1. The driver that read this bit can then perform an I/O access. Once the access is completed, hardware automatically clears this bit.</p> |

**Note:** Reads across DWord boundaries are not supported.

§



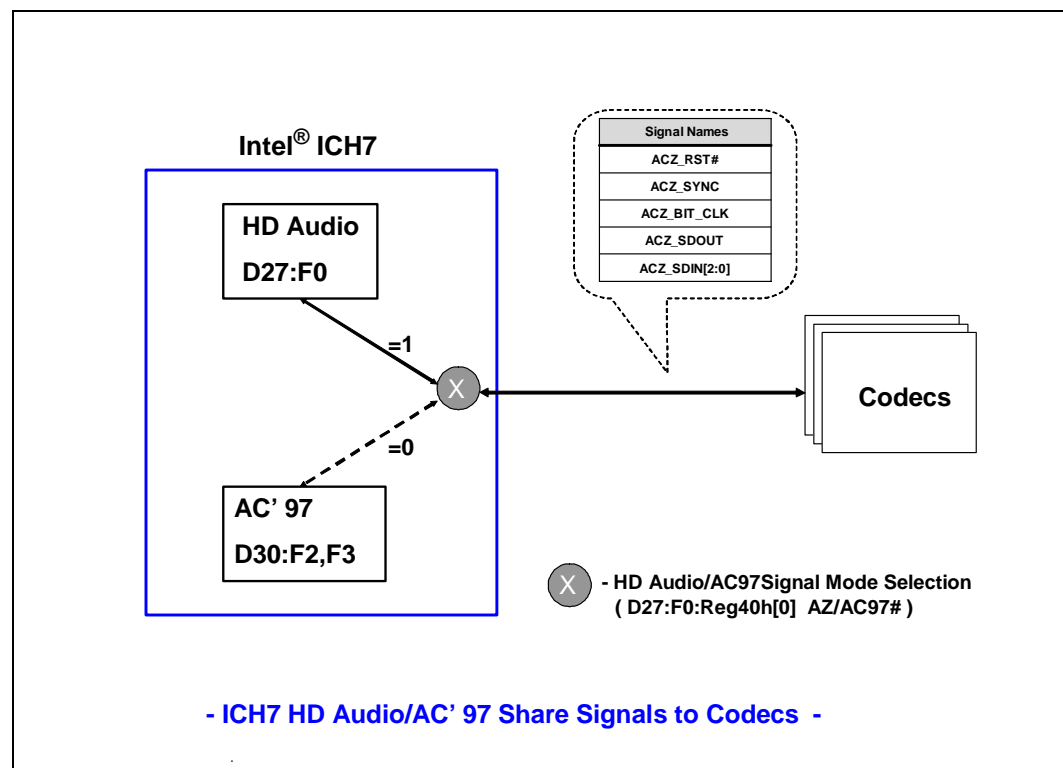
# 4 Intel® High Definition Audio BIOS Considerations

The Intel® HD Audio controller (Bus #0, Device #27, Function #0) is an ICH7 internal PCI Express Endpoint device. Software may access the Intel® HD Audio controller registers (including the memory mapped registers) by byte, word, DWord quantities and on natural boundaries; DWord accesses must be on dWord boundaries, word accesses on word boundaries, etc. This chapter describes BIOS requirements for Intel® HD Audio controller support.

## 4.1 Intel® High Definition Audio/AC' 97 Signal Mode Selection

The Intel® HD Audio controller and the AC'97 controllers (audio and modem) share the same physical signal pins to communicate with codecs as Figure 4-1 shows. The **Intel® HD Audio/AC97# Signal Mode (AZ/AC97#)** bit at D27:F0:Reg40h[0] determines which one of the two controllers is connected to the codec.

Figure 4-1. Intel® ICH7 High Definition Audio/AC' 97 Share Signals to Codecs



### 4.1.1 Intel® High Definition Audio/AC' 97 Codec Detection

Before PCI device enumeration during POST, BIOS must determine the type of codec present on the platform, then program the AZ/AC97# bit to select either Intel® HD Audio or AC' 97 signal mode, and program the corresponding bit in the Function Disable register (RCBA+ 3418h[6:4]) to disable the other controller.

If the BIOS has inherent knowledge of which type of Codec(s) will be connected to the ICH7's signals, it can set the AZ/AC97# bit accordingly.

ICH7 also provides a mechanism for software to detect the type of the codec present on the platform. Below is the Intel® HD Audio register used in the codec detection.

#### D27:F0:Reg40h – AZCTL—Intel® HD Audio Control

| Bit | Type  | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
|-----|-------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:4 | RsvdP | 0s    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| 3   | R/W   | 0     | <b>BITCLK Detect Clear (CLKDETCLR):</b> Writing a 1 to this bit clears the CLKDET# bit. The CLKDET# bit remains clear while this bit is set to 1. When a 0 is written to this bit, the clock detect circuit is operational and may be enabled.                                                                                                                                                                                                                                                                                                                                                                                                                            |
| 2   | R/W   | 0     | <b>BITCLK Detect Enable (CLKDETEN):</b> Writing a 1 to this bit enables the clock detection circuit. Writing a 0 latches the current state of the CLKDET# bit.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
| 1   | RO    | 0     | <b>BITCLK Detected Inverted (CLKDET#):</b> This bit is modified by hardware. It is set to 0 when the ICH7 detects that the BITCLK signal is toggling, indicating the presence of an AC'97 codec on the link. Note that the CLKDETEN and CLKDETCLR bits control the operation of this bit and must be manipulated correctly to get a valid CLKDET# indicator.                                                                                                                                                                                                                                                                                                              |
| 0   | R/W   | 0     | <b>Intel® HD Audio/AC97# Signal Mode (AZ/AC97#):</b> This bit selects the mode of the shared Intel® HD Audio/AC97 signals.<br>0 = AC97 mode is selected.<br>1 = Intel® HD Audio mode is selected.<br>The bit defaults to 0 (AC97 mode) to protect against contention on BCLK when an AC97 codec is connected.<br>Note that this bit has no effect on the visibility of the AC97 and Intel® HD Audio function configuration space. That is controlled through individual function enable bits.<br>This bit is in the resume well and only cleared on a power-on reset. Software must not make assumptions about the reset state of this bit and must set it appropriately. |

In the Intel® HD Audio environment the ICH7 drives BITCLK signal. The AZ/AC97# bit defaults to 0 (AC97 mode) after reset, so the BITCLK signal will be configured as an input. The ICH7 samples the BITCLK signal. If it is toggling the CLKDET# bit will be set to 0. The BIOS can read this bit and set the AZ/AC97# bit accordingly.

BIOS should perform this detection prior to PCI enumeration. The following is the BIOS software flow for codec detection:

1. Ensure that ICH7 RCBA base address register (D31:F0:Reg F0h) is initialized and enabled.
2. Ensure that both AC'97 and Intel® HD Audio functions are present (RCBA+ 3418h[6:4]=000b), which is the power on default.
3. Set IOSE bit (D30:F2:Reg41h[0]=1), program the AC'97 function's PCI BARs with temporary address values and enable IO BAR space via PCI command register.

4. De-assert AC\_RESET# bit to take the link out of RESET# (NABMBAR at D30:F2:Reg14h + offset 2Ch[1]=1).
5. Wait ~20ms for AC'97 codec driven BIT\_CLK startup.
6. Write a 0 to the Intel® HD Audio/AC97# bit (D27:F0:Reg40h[0]=0) to ensure that AC'97 mode is selected.
7. Make sure that CLKDET# bit is cleared by writing a 1 and then a 0 to the CLKDETCLR bit.
8. Write a 1 to the CLKDETEN bit to enable the clock detection circuit.
9. Write a 0 to the CLKDETEN bit.
10. Read the CLKDET# bit.
11. If CLKDET# is clear(==0), then the codec(s) are AC'97. Disable and hide the Intel® HD Audio function. Skip the steps below and exit.
12. If CLKDET# is set (==1), then the codec(s) are Intel® HD Audio.
13. Reassert AC\_RESET# bit to put the link back into reset state (NABMBAR at D30:F2:Reg14h + offset 2Ch[1]=0).
14. Clear the AC'97 BARs and disable memory/IO space through its PCI register 04h.
15. Hide the AC'97 functions (RCBA+ 3418h[6:5] = 11b)
16. Set the AZ/AC'97# bit to 1 to enable Intel® HD Audio signal mode (D27:F0:Reg40h[0]=1b)
17. Program the Intel® HD Audio AZBAR at PCI config space 10h-17h to a temporary address and enable it by setting PCI command register 04h[1]=1.
18. De-assert the Controller Reset# bit in Intel® HD Audio to cause the link to start up (AZBAR+08h [0] = 1)
19. Clear STATESTS bits (AZBAR+0Eh [2:0]) by writing 1s to them.
20. Turn off the link by writing a 0 to the Controller Reset# bit in Intel® HD Audio (AZBAR+08h [0] = 0). Poll Controller Reset# bit until it reads back as 0.
21. Turn on the link again by writing a 1 to Controller Reset# bit (AZBAR+08h [0] = 1). This causes a codec link re-enumeration. Wait for about 1 millisecond (ms). Poll Controller Reset# bit until it reads back as 1.
22. Read the STATESTS bits (AZBAR+0Eh [2:0]) which will indicate which SDIN lines have codecs on them. If there is one or more bits set to 1, Intel® HD Audio codec(s) are present, go to step 24. Otherwise there is no codec present.
23. If there is no codec present, BIOS can disable the Intel® HD Audio controller by
  - Turning off the link by writing a 0 to the Controller Reset bit (AZBAR+08h [0] = 0).
  - Clearing Intel® HD Audio AZBAR register (offset 10h), then write 0 to PCI command register at offset 04h.
  - Disabling Intel® HD Audio controller via Function Disable register (set RCBA+ 3418h[4]=1).

Skip the following steps and exit.
24. For each Intel® HD Audio codec present as indicated by AZBAR+0Eh[2:0], perform codec initialization as described in the next section.

## 4.1.2 Intel® High Definition Audio Codec Initialization

This section involves the programming interface on Intel® HD Audio codec link. Readers are encouraged to read the relevant chapters of Intel® HD Audio Specification for information regarding architecture overview, register interface, programming model and codec features and requirements.

Intel® HD Audio allows flexible configurations of the inputs and outputs among its internal functional units and between codec and external jacks. Each pair of pins in the codec is assigned to an internal node in the codec, so the information related to the jack position, color coding, etc. is mapped to the node that is internally assigned to the pins and wired to a jack. This information will allow the audio driver to configure the audio codecs correctly.

After BIOS has determined the presence of Intel® HD Audio codec(s), it must follow the programming sequence given in this section to update the codec with correct jack information specific to the platform for Intel® HD Audio driver to retrieve and use later. If the codecs are not initialized with this platform-specific information, the Intel® HD Audio driver will use the default data in the codecs which may or may not match the pin/jack connections or jack locations of the platform.

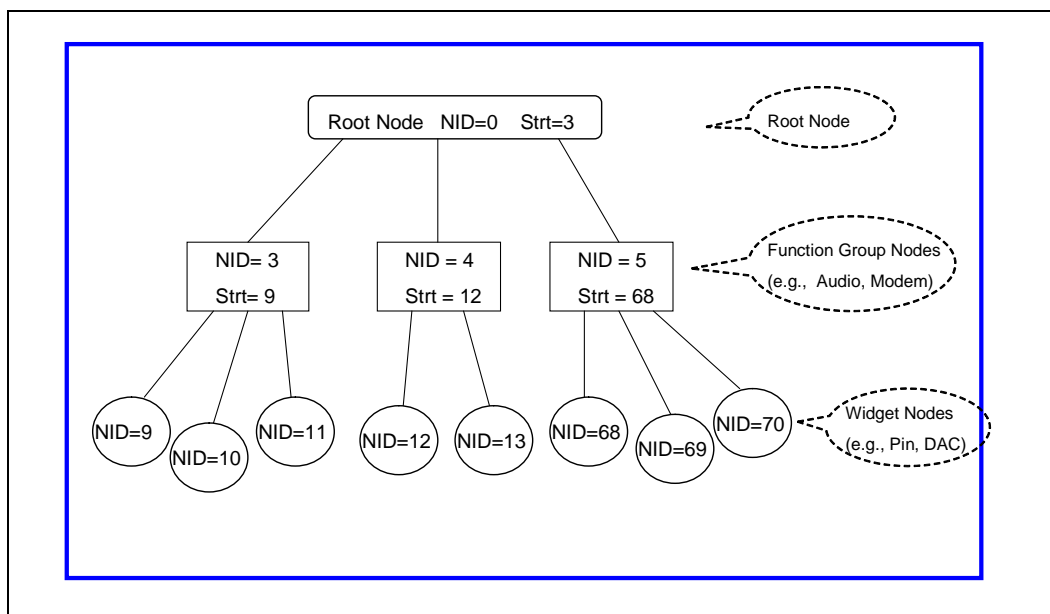
### 4.1.2.1 Intel® High Definition Audio Codec Architecture Introduction

The Intel® HD Audio Specification defines a modular codec architecture that is fully discoverable and configurable by software. It provides for the construction and description of various codec functions from a defined set of parameterized modules (building blocks, or Widgets). Each such module and each collection of modules becomes a uniquely addressable Node, from which software can read capability parameters and to which it can send control commands. The root node is the top level node and always has a Node ID (NID) of 0. Each node contains information of the next level of nodes below it, in a tree structure as shown in [Figure 4-2](#).

For each Intel® HD Audio codec present, a unique Codec Address (CA<sub>d</sub>) is assigned to the codec by hardware after reset during the codec link initialization and will be used for software to address each codec. For instance, the codec connected to SDI0 (as indicated by AZBAR+0Eh[0]=1) has its CA<sub>d</sub>=0, the codec connected to SDI1 (as indicated by AZBAR+0Eh[1]=1) has its CA<sub>d</sub>=1, and so on, each node in a codec has its pre-defined, unique Node ID (NID). The CA<sub>d</sub>+NID combination is used by a Verb to uniquely address a codec node.



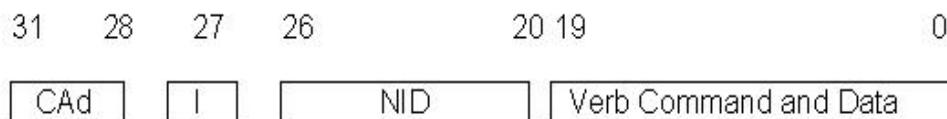
Figure 4-2. Intel® High Definition Audio Codec Node Structure and Addressing



A codec **verb** is a 32-bit DWord command sent to a codec by software that contains the following information:

- Codec address and Node ID of the target node in the codec
- Command to be performed by the target node
- Data payload (if any)

Below is the format of a Verb dword.



There are two ways for software to send verbs to and receive response data from codecs over the Intel® HD Audio codec link: Using CORB/RIRB (Command Output Ring Buffer / Response Input Ring Buffer), or using Immediate Command/Immediate Response register pair. See the Intel® HD Audio Specification for details of register description and programming interface.

#### 4.1.2.2 Codec Verb Table

For each codec present on the Intel® HD Audio codec link, a corresponding pre-defined “Codec Verb Table” must be available to BIOS. The Codec Verb Tables are based on codec specific information (coded datasheet) and platform design specific information (schematics) and are built by BIOS writers and platform designers. The table contains a list of 32-bit “Verb”s (command and data payload) to be sent to the corresponding codec over the Intel® HD Audio codec link.

Below is a sample Intel® HD Audio Codec Verb Table, defined in Intel x86 Assembly Language, for a platform with 1 codec at codec address 01h.

```

;Sample Intel® HD Audio Codec Verb Table
;Codec Address (CAAd) = 01h
;Codec Vendor: XYZ Company
;VenID DevID:
  dd 12345678h
;SubsystemID: Program 0x87654321h
  dd 10172021h
  dd 10172143h
  dd 10172265h
  dd 10172387h

;-----
;FrontPanel_Supported? ; 1=Supported , 0=Not supported
  db 01h
; # of Rear Panel Pin Complexes
  dw 0009h
; # of Front Panel Pin Complexes
  dw 0002h-----

```

VerbTable0:

```

;Pin Complex 1 (NID 12h)
  dd 11271C11h
  dd 11271D81h
  dd 11271E30h
  dd 11271F00h
;Pin Complex 2 (NID 11h)
  dd 11171C11h
  dd 11171D01h
  dd 11171E40h
  dd 11171F00h
;Pin Complex 3 (NID 13h)
  dd 11371C11h
  dd 11371DA1h
  dd 11371E60h
  dd 11371F00h
;Pin Complex 4 (NID 32h)
  dd 13271C11h
  dd 13271D01h
  dd 13271E00h
  dd 13271F00h

```

*;Pin Complex 5 (NID 15h)*

*dd 11571C11h*  
*dd 11571D01h*  
*dd 11571E00h*  
*dd 11571F00h*

*;Pin Complex 6 (NID 31h)*

*dd 13171C11h*  
*dd 13171D01h*  
*dd 13171E00h*  
*dd 13171F00h*

*;Pin Complex 9 (NID 19h)*

*dd 11971C11h*  
*dd 11971DC4h*  
*dd 11971E00h*  
*dd 11971F00h*

*;Pin Complex 10 (NID 18h)*

*dd 11871C11h*  
*dd 11871D04h*  
*dd 11871E00h*  
*dd 11871F00h*

*;Pin Complex 11 (NID 17h)*

*dd 11771C90h*  
*dd 11771D3Fh*  
*dd 11771E00h*  
*dd 11771F00h*

*VerbTable0FP:*

*;Pin Complex 7 (NID 14h) Front Panel Jack*

*dd 11471C02h*  
*dd 11471D21h*  
*dd 11471E10h*  
*dd 11471F00h*

*;Pin Complex 8 (NID 16h) Front Panel Jack*

*dd 11671C02h*  
*dd 11671DA1h*  
*dd 11671E10h*  
*dd 11671F00h*

### 4.1.2.3 Codec Initialization Programming Sequence

After BIOS has determined the presence of Intel® HD Audio codec(s), it must follow the programming sequence given in this section to update the codec with correct jack information specific to the platform for Intel® HD Audio driver to retrieve and use later.

There are two ways for software to send verbs to and receive response data from codecs over the Intel® HD Audio codec link: Using CORB/RIRB (Command Output Ring Buffer / Response Input Ring Buffer), or using Immediate Command/Immediate Response register pair. The sequence below uses the latter which does not require the availability of a memory buffer.

BIOS should ensure that the Intel® HD Audio AZBAR at PCI config space 10h-17h contains a valid address value and is enabled by setting PCI command register 04h[1]=1. BIOS should also ensure that the Controller Reset# bit of Global Control register in memory-mapped space (AZBAR+08h[0]) is set to 1 and read back as 1.

For each Intel® HD Audio codec present as indicated by AZBAR+0Eh[2:0], BIOS should perform the codec initialization as described below:

1. Read the VendorID/DeviceID pair from the attached codec
  - Poll the ICB bit of IRS register at AZBAR+68h[0] to make sure it returns 0.
  - Write verb c00F0000h (dword) to the IC register at AZBAR+60h, where: 'c' (bits 31:28) represents the codec address (CA<sub>D</sub>).
  - Write the bits of IRS register at AZBAR+68h[1:0] to 11b to send the verb to codec.
  - Poll IRS register bits at AZBAR+68h[1:0] until it returns 10b indicating the verb has been sent to the codec and response data from codec is now valid.
  - Read the IR register at AZBAR+64h, the dword data is the VID/DID value returned by the codec.
2. Check against internal list to determine if there is a stored verb table which matches the CA<sub>D</sub>/VID/DID information.

Note that steps 1 and 2 are BIOS implementation-specific steps and can be done in different ways. If a BIOS has prior knowledge of fixed platform/codec combination (e.g., for a BIOS having 3 stored verb tables for 3 known codecs at known codec addresses on a known platform), a simple pre-defined codec-to-table matching can be used and steps 1 and 2 can be eliminated. For a BIOS to support multiple codec/platform combinations, an internal match-list might be needed to match a platform/codec combination to a codec verb table.

3. If there is a match, send the entire list of verbs in the matching verb table one by one to the codec.
  - Poll the ICB bit of IRS register at AZBAR+68h[0] to make sure it returns 0.
  - Write the next verb (dword) in the table to the IC register at AZBAR+60h,
  - Write the bits of IRS register at AZBAR+68h[1:0] to 11b to send the verb to codec.
  - Poll the ICB bit of IRS register at AZBAR+68h[0] until it returns 0 indicating the verb has been sent to the codec.
  - Repeat the steps until all the verbs in the table have been sent.

**Note:** Some verbs in the table may need to be qualified by certain platform-specific conditions. For example, for the sample table above, the verbs for Pin Complex 7 and 8 (NID=14,16 respectively) should be sent only if the Front Panel Jacks are present and connected on the platform, which may be indicated by a software flag that is controlled by certain GPIO pin state.

#### 4.1.2.4 Codec Initialization Sample Code

This section shows an example of code implementation of the Intel® HD Audio codec initialization sequence.

```

;-----
;
; Procedure:InitializeIntel®HDAudioCodecs
;
; Description:Initialize Intel®HDAudioCodecs by sending
; codec verbs to codecs.
;
; Input:
; ES - 0000h with 4GB limit.
; STACK- Available.
; Intel® HD Audio controller's AZBAR is initialized and enabled.
; Codec verb tables are available and defined in the
; same code segment.
;
; Output:
; CF : 1 = Codec initialization failure
; CF : 0 = Codec initialization success
;
; Registers modified:All except segment registers.
;
; Notes:
; MKF_HDAudio_BASE_ADDRESS = the value of AZBAR register
; MKF_MAX_NUM_AZAL_CODECS = 3 (max of 3 codecs supported)
; HDAudio_MMIO_STATESTS = 0Eh
; HDAudio_MMIO_IC = 60h
; HDAudio_MMIO_IR = 64h
; HDAudio_MMIO_ICS_ICB = 68h
; VerbHeaderSize = 11d
;-----

InitializeHDAudioCodecs PROC NEAR PUBLIC
; ebx will always hold the Intel® HD Audio base address
mov ebx, MKF_HDAudio_BASE_ADDRESS
; ecx is the current codec address (only 15 codecs are supported in the
; Intel® HD Audio spec so only the lower 4 bits are relevant)
mov ecx, MKF_MAX_NUM_AZAL_CODECS

```

```

; dx is the map of SDI pins, and the bits will be cleared as the
; associated codecs are serviced
mov dx, word ptr es:[ebx+HDAudio_MMIO_STATESTS]

InitCurrentCodec:
    dec cx
    btr dx, cx                ; Test for 'cx'th codec
    jnc NextSDI

;-----
;1. Ensure Intel® HD Audio device is enabled and BARs are programmed
;
; a. Program Intel® HD Audio BARs with temporary values
; b. Enable memory space and bus mastering
; c. Deassert CRST#
;-----
; a. Set the AZ/AC'97# bit to 1 to enable Intel® HD Audio signal mode
(D27:F0:Reg40h[0]=1b)
    mov ah, HDAudio_AZCTL_OFFSET
    mov al, HDAudio_AZCTL_OFFSET_AZ_AC97
    _SET_PCI_FAR HDAudio
; b. Program the Intel® HD Audio AZBAR at PCI config space 10h-17h
to a temporary address
    mov ah, PCI_BAR0
    mov ebx, MKF_HDAudio_BASE_ADDRESS
    _WRITE_PCI_DWORD_FAR HDAudio
; c. Enable memory space and bus mastering for Intel® HD Audio
    mov al, CMD_MEM_SPACE+CMD_BUS_MASTER
    _SET_PCI_FAR HDAudio
; d. Deassert the CRST bit in Intel® HD Audio to cause the link to start
up(AZBAR+08h[0]=1)
    or byte ptr es:[ebx+HDAudio_MMIO_GCTL],
HDAudio_MMIO_GCTL_CRST

;-----
;2. Read the Vendor ID/Device ID pair from the attached codec
;
; a. Poll the ICB bit in the ICS register at AZBAR+68h[0] until it returns 0
; b. Write verb c00F0000h (dword) to the IC register at AZBAR+60h;
where 'c'

```

```

; (bits 31:28) represents the codec address (CAAd).
; c. Set bits 1:0 of the IRS register at AZBAR+68h[1:0]
; d. Poll ICS register bits at AZBAR+68h[1:0] until they return 10b
indicating
; the verb has been sent to the codec and response data from codec is
now valid.
; e. Read IR register at AZBAR+64h, the dword data is the VendorID/
Device
; ID value returned by the codec
;-----
; a. Poll the ICB bit in the ICS register at AZBAR+68h[0] until it returns 0

    push  cx
    xor   cx, cx                ; 64K cycles
PollICBBit:
        test   word ptr es:[ebx+HDAudio_MMIO_ICS],
HDAudio_MMIO_ICS_ICB
        jz    ICBBitClear      ; Poll ICB bit until it returns 0
        loop  PollICBBit
; Add error handling code here
; When timeout occurs, reset link per audio driver team request
        and   byte ptr es:[ebx+HDAudio_MMIO_GCTL], NOT
HDAudio_MMIO_GCTL_CRST
        or    byte ptr es:[ebx+HDAudio_MMIO_GCTL],
HDAudio_MMIO_GCTL_CRST
ICBBitClear:
    pop   cx

; b. Write verb c00F0000h (dword) to the IC register at AZBAR+60h;
where 'c'
; (bits 31:28) represents the codec address (CAAd).
    mov   eax, ecx
    shl  eax, 28
    or   eax, 000F0000h
    mov  dword ptr es:[ebx+HDAudio_MMIO_IC], eax ; Write the verb
; c. Set bits 1:0 of the IRS register at AZBAR+60h[1:0]
    or   word ptr es:[ebx+HDAudio_MMIO_ICS], BIT1+BIT0 ; Send the
command

; d. Poll ICS register bits at AZBAR+68h[1:0] until they return 10b
indicating

```

```

; the verb has been sent to the codec and response data from codec
is now valid.

```

```

PollDataValid:

```

```

    mov    al, byte ptr es:[ebx+HDAudio_MMIO_ICS]
    cmp    al, 10b
    jne    PollDataValid

```

```

; e. Read IR register at AZBAR+64h, the dword data is the VendorID/
Device

```

```

; ID value returned by the codec
    mov    eax, dword ptr es:[ebx+HDAudio_MMIO_IR] ; eax=vendorID/
deviceID

```

```

;-----
;3. Check against the list of supported vendor ID/Device ID combinations
; to determine if the received VID/DID is supported.
;-----

```

```

    push   ecx

    call  CheckforValidCodec
    or    cx, cx
jz    VerbTableDone          ; jump if VID/DID not supported

```

```

;-----
;4. If there is a match, send the entire list of verbs in the matching verb
; table one by one to the codec
; a. Poll the ICB bit of the ICS register at AZBAR+68h[0] until it returns 0.
; b. Write the next verb (dword) in the table to the IC register at
AZBAR+60h.
; c. Write the bits of the ICS register at AZBAR+68h[1:0] to 11b to send the
; verb to the codec.
; d. Repeat steps 4a-4c until all verbs in the table have been sent for the
; current codec.
;-----

```

```

; a. Poll the ICB bit of the ICS register at AZBAR+68h[0] until it returns 0.

```

```

    push   cx
    xor    cx, cx

```

```

PollICBBit2:

```



```

                                test     word ptr es:[ebx+HDAudio_MMIO_ICS],
HDAudio_MMIO_ICS_ICB
                                jz      ICBBit2          ; Poll ICB bit until it returns 0 (need to
change "HDAudio" in this command to HDAudio?
                                loop    PollICBBit2
;   Add error handling code here
ICBBit2:
                                pop     cx

;   b. Write the current verb (dword) in the table to the IC register at
AZBAR+60h.
                                mov     eax, dword ptr cs:[si]
                                mov     dword ptr es:[ebx+HDAudio_MMIO_IC], eax ; Write verb

;   c. Write the bits of the ICS register at AZBAR+68h[1:0] to 11b to send
the
;   verb to the codec.
                                or      word ptr es:[ebx+HDAudio_MMIO_ICS], BIT1+BIT0
;   d. Repeat steps 3a-3d until all verbs in the table have been sent for the
;   current codec.

                                loop    PollICBBit2          ; Continue until all verbs written

VerbTableDone:
                                pop     ecx

NextSDI:
                                or      dx, dx
                                jnz     InitCurrentCodec

HDAudioCodecComplete:
                                ret

InitializeHDAudioCodecs ENDP

;-----
;
;
; Procedure: CheckforValidCodec

```

```

;
; Description: Detects whether the vendor and device ID of the current
; codec
;           is supported based on whether the value is found at the start
;           of any of the codec verb tables.
;
; Input: EAX - Vendor and device ID of the current codec
;        ECX - Current codec address
;        DS - BDA_DSEG.
;        ES - 0000h with 4GB limit.
;        FS - POST_DSEG.
;        GS - RUN_CSEG.
;        STACK - Available.
;
; Output: CX - Size of codec verb table (in dwords) if a valid
;          codec is present. Else cx = 0.
;         SI - Address of the codec verb table (valid if CF=0)
;
; Modified: SI
;-----

CheckValidCodec PROC NEAR PUBLIC
    push    bx
    push    edx
    push    si

    xor    bx, bx
CheckNextCodecTable:
    mov    si, word ptr cs:[bx+offset CodecVerbTableList]
    cmp    dword ptr cs:[si], eax
    je     FoundValidCodec

; end of table?
    add    bx, 2                ; Next verb table entry
    cmp    bx, (offset CodecVerbTableListEnd - offset
CodecVerbTableList)
    jb    CheckNextCodecTable

CodecNotValid:
    xor    cx, cx

```

```
jmp CodecCheckDone
```

*FoundValidCodec:*

```
mov  edx, dword ptr cs:[si+VerbHeaderSize]    ; Get first verb
shr  edx, 28
cmp  edx, ecx                                ; Is the codec address correct?
jne  CodecNotValid
add  si, 6
call GetVerbTableSize                        ; Codec has valid DID/VID and addr
```

*CodecCheckDone:*

```
pop  si
pop  edx
pop  bx
ret
```

*CheckforValidCodec*    *ENDP*

```
;-----
;
; Procedure: GetVerbTableSize
;
; Description: Checks the front panel sensing GPIO to determine if front
;               panel jacks are present. The routine returns the size of
;               the verb table (size may depend on whether front panel is
;               supported or if the codec supports front panel).
;
; Input: SI      - Address of the front panel supported status byte
;               DS - BDA_DSEG.
;               ES - 0000h with 4GB limit.
;               FS - POST_DSEG.
;               GS - RUN_CSEG.
;               STACK- Available.
;
; Output: CX     - Size of codec verb table in dwords
;               SI  - Address of the codec verb table
;
; Modified: EBX, CX, SI
```

```

;-----
GetVerbTableSize    PROC NEAR PUBLIC
    push    ebx

    mov     cl, byte ptr cs:[si]      ; al = Front panel support bit
    inc     si

    or      cl, cl

    mov     cx, word ptr cs:[si]      ; cx = length of rear panel table
    jz     FPSupportDone             ; If front panel not supported
                                        ; by the codec, no need to add
                                        ; FP table size

;     TODO: OEMs must add code here to query the GPIO dedicated to
front
;     panel sensing.
    jz     FPSupportDone
;     If control comes here, front panel jack is supported by the codec and
;     is present in the system, so add the size of the FP table.
    add     cx, word ptr cs:[si+2]    ; cx = rear panel table size +
                                        ; front panel table size

FPSupportDone:

    add     si, 4                    ; si = start of codec verb table
    shl     cx, 2                    ; cx = # of Pin complexes * 4
                                        ; = # of dwords in table

    pop     ebx
    ret

GetVerbTableSize    ENDP

CodecVerbTableList:
    dw offset VerbTable0
    dw offset VerbTable1
CodecVerbTableListEnd:

```

### 4.1.3 Intel® High Definition Audio Codec Initialization on S3 Resume

According to Microsoft, the SSID response from the Intel® HD Audio codec must be consistent at any point the OS may read the value. Similarly other codec configuration information must follow the same rule. Additionally, the assumption of relying on the function driver to ensure such consistency across different sleep states is not always practical due to the fact that the function driver can be disabled/unloaded by user (for whatever reason) prior to system power state transitions.

This requires that any programming of the Intel® Hd Audio codecs that the BIOS performs during POST must also be performed any time the codec power plane loses power. In particular, this means that the codec verb table, if programmed into the codec during POST, must be restored by BIOS on S3 resume if the codec context is not constantly maintained by standby power.

Note that this requirement does not apply to platforms that use the codec's hardware default configurations without changing them, or platforms that maintain the codec context in S3 by standby power.

#### S3 Resume BIOS Requirement

The BIOS programming on resume is complicated by the need to preserve the wake status information in the codec, so that the bus driver can determine if a codec (usually a modem) has 'awoken' the system. The following programming sequence is therefore recommended during S3 resume:

1. Read the original STATESTS from AZBAR+0Eh[2:0], save it to OldState.
2. Set AZBAR+08h[0] = 1 to take the controller out of reset, wait for about 1ms.
3. Program Verb Tables to codecs as BIOS did during the POST.
4. Write AZBAR+0Eh[2:0]=NOT(OldState) to restore previous STATESTS.
5. Set AZBAR+08h[0] = 0 to put the controller back in reset.

## 4.2 Intel® High Definition Audio Controller Configuration

Once the Intel® HD Audio codec is determined to be present and Intel® HD Audio controller is kept enabled via Function Disable register (RCBA+ 3418h[4]=1), BIOS should:

- Initialize the configuration space of Intel® HD Audio controller as a regular PCI device (assign memory and interrupt resources and enable the device using standard PCI command register 04h).
- Initialize SSID/SVID registers at D27:F0:Reg2C-2Fh to OEM-specific IDs. This is similar to the SSID/SVIDs given to other ICH7 devices such as IDE, SATA, SMBus, USBs, etc.

## 4.3 Intel® High Definition Audio PME Event

Although it is a PCI Express Root Complex Integrated endpoint, the Intel® HD Audio controller in the ICH7 is not capable of supporting the native PME software model. Its PME is supported in the same manner as a PCI PME.

The AC97\_STS/AC97\_EN bit-pair in ICH7 GPE0 register (PMBase+28h[5], PMBase+2Ch[5]) is shared between AC97 and Intel® HD Audio PME event, depending on which one of the two devices is selected and enabled by BIOS. To support this PME feature in ACPI OS environment, BIOS needs to provide the proper `_PRW` object and `\_GPE._L05()` control method in the ACPI name space. Below is an example of the ACPI name space for Intel® HD Audio/AC97 PME support:

```

Scope (\_SB)
{
    Device (PCI0)      // PCI Bus0
    {
        Name (_BBN, 0) // Bus Number of PCI0

        Method(_PRT, 0)
        {
            //
            _PRT package for PCI0
        }

        .....

        Device (AC97)          // AC97 controller
        {
            Name(_ADR, 0x001E0002)// Device30:Func2
            Name ( _PRW, Package () {0x05,0x03} ) // PME Wake
            capability reporting
            .....
        } // End AC97

        Device (AZAL)          // Intel® HD Audio
        controller
        {
            Name(_ADR, 0x001B0000)// Device27:Func0
            Name ( _PRW, Package () {0x05,0x03} ) // PME Wake
            capability reporting
            .....
    }
}

```

```
    } // End AZAL

} // End Device PCI0
} // End \_SB scope

Scope (\_GPE) //
GPE event handlers
{

    Method (_L05, 0) // Intel® HD Audio/
AC97 PME event handler
    {
        // If Intel® HD Audio is the enabled controller
        // Notify (\_SB.PCI0.AZAL, 0x02)// notify wake event
        // Else
        // Notify (\_SB.PCI0.AC97, 0x02)// notify wake event

    } // End of _L05
} // End of \_GPE scope
```

§

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