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Designing a Hi-Speed USB host PCI adapter using the ISP1562, ISP1563

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Document information

Info	Content
Keywords	isp1562; isp1563; usb; universal serial bus; host; pci adapter
Abstract	This document contains a description of the ISP1562/3 application schematics and the PCB design recommendations.

Revision history

Rev	Date	Description
04	20071101	Fourth revision. Corrected typo in Section 4: it is 2.5 inches ± 0.1 inch, not ± 1 inch. Last line of Section 3.4.
03	20061212	Third revision. Updated Fig 6.
02	20060707	Second revision. Updated Section 5.
01	20051004	First release.

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1. Introduction

The ISP1562 and the ISP1563 are Hi-Speed Universal Serial Bus (USB) host controllers (HCs) that can be directly connected to a standard 32-bit, 33 MHz PCI bus. For the rest of this document, they will be known as 'ISP1562/3'. The ISP1562/3 complies with *PCI Local Bus Specification Rev. 2.2* and *PCI Bus Power Management Interface Specification Rev. 1.1*. No additional logic is required to implement a complete Hi-Speed USB host controller solution on Peripheral Component Interconnect (PCI).

Adapter cards based on the ISP1562/3 implement three functions: function 0 and function 1 for OHCI1 and OHCI2, and function 2 for EHCI. According to *PCI Local Bus Specification*, each physical PCI device may incorporate one to eight separate functions (logical devices). Each function contains its own memory-mapped individually addressable configuration space of 256 bytes, containing configuration registers.

The configuration registers of the ISP1562/3 are used by the system's BIOS and the operating system to detect the presence of the respective functions, that is, Vendor ID (VID) and Product ID (PID), to determine the necessary resource requirements, that is, memory and I/O space, interrupt lines, and so on, and for specific capabilities.

A set of on-chip 'operational' registers is also defined for each of the three host controllers implemented in the ISP1562/3. The respective host controller device driver interacts with these registers to implement the USB functionality and the legacy support. A detailed description of configuration registers and operational registers can be found in the ISP1562 and ISP1563 data sheets.

The ISP1562/3 implements two internal 'power wells', V_{DD} and V_{DDX}, to benefit from the PCI V_{AUX} = 3.3 V dedicated power source, which is present on the PCI connector (pin A14) even when PCI V_{CC} = 3.3 V is off. This enables the ISP1562/3 PME# signal to be asserted and activates the wake-up logic of the motherboard, even if the rest of the system is powered down; for example, in $S3_{cold}$ system standby mode. This is applicable mainly to onboard (desktop) or mobile designs, but not applicable to PCI add-on cards because the PCI +5 V, used for V_{BUS}, is also off during $S3_{cold}$.

The ISP1562/3 may use PCI V_{AUX} to power its four internal transceivers connected to the ISP1562/3 V_{DDA_AUX} (analog), and also the clock circuitry, port router, root hub and Power Management Event (PME#) logic connected to the ISP1562/3 $V_{CC(I/O)\_AUX}$ (digital).

For details on implementation of the PCB design, see Section 4.

The power management capabilities enabled by using PCI V_{AUX} allow system designers to meet the governmental energy regulations that are becoming increasingly essential worldwide: Energy Star/USA: 30 W standby, White Swan/Europe: 5 W standby, Blue Angel/Europe: 5 W standby.

This document provides a description of the application schematics and the PCB design recommendations.

2. ISP1562/3 initialization

The following sequence is required during the ISP1562/3 initialization, for correct functionality:

1. Register HcRhDescriptorA = 902h. This means that bit PSM = 1b.
2. Register HcControl = 680h. This means that bits HCFS[1:0] = 10b (operational mode).

3. Register HcRhStatus = 18000h. This implies that bit LPSC = 1b (port powered).

Microsoft Windows 2000, Windows XP and Linux drivers normally use this sequence. The order of the steps may, however, be reversed in Windows CE default drivers so changes are required for normal functionality.

3. Description of the application schematics

The schematics (see Section 5) contain a complete implementation of the ISP1562/3 and allow testing of all its features in different types of design: PCI add-on card, onboard design in standard desktop or mobile solution.

In the case of a standard PCI add-on card design, some simplifications to the schematics can be done, as described here. Some features will not be normally used in a standard PCI add-on card. For example: The legacy support, wake-up from $S3_{cold}$ (no external +5 V input for V_{BUS}) and the alternative 48 MHz clock input. All these alternatives, however, are included in the schematics and are described in this document.

3.1 Distribution of power sources and power management support

As shown in the schematics (see Section 5), a simple solution by using one jumper (JP1) may be adopted to choose between PCI V_{CC} = 3.3 V or PCI V_{AUX} = 3.3 V as the main power source for the ISP1562/3. Power source PCI V_{AUX} = 3.3 V is introduced in *PCI Local Bus Specification Revision 2.2*. It allows powering an add-on card and generation of the PME# signal, even if the system is in a deep power management state and PCI V_{CC} is off. An alternative solution to using a jumper may be a simple circuit containing a pair of MOSFET transistors that allows to detect the presence of PCI V_{AUX} = 3.3 V and automatic selection of the input voltage.

Selection of PCI V_{CC} = +3.3 V must be the default position of jumper JP1 in the case of a standard add-on card design. The other possible position of JP1 selects PCI V_{AUX} = 3.3 V for complete Power Management tests, including $S3_{cold}$ in the case of on-motherboard or notebook. Note that pins 3, 77, 98 and 100 of the ISP1562, and pins 6, 12 and 95 of the ISP1563 are connected to the PCB $V_{CC(I/O)\_AUX}$ power plane and pins 86 and 93 of the ISP1562, and pins 104, 111, 120 and 128 of the ISP1563 are connected to the PCB V_{DDA_AUX} power plane. Each of these planes is separated from PCI V_{AUX} by its own set of inductors and decoupling capacitors.

Although most of the motherboards provide the PCI V_{AUX} power source in all system power management modes, including $S3_{cold}$, the PCI +5 V power supply is simultaneously interrupted with PCI V_{CC} = +3.3 V.

In certain standby modes ($S3_{cold}$), the devices connected to USB ports will not be powered once the +5 V power is removed because the V_{BUS} voltage present on USB connectors is normally derived from the PCI +5 V power supply. Therefore, PCI V_{AUX} is not useful in the case of a standard PCI add-on card implementation for a system wake-up from $S3_{cold}$. It is, however, a very useful feature for onboard and mobile application designs because it allows additional considerable power savings and also wakes up the system by using a USB device. The system wake-up from $S3_{cold}$, generated from a USB device, for example, USB mouse or USB keyboard, connected to the ISP1562/3 host controller must be supported in system's BIOS, hardware (a continuous +5 V must be supplied to V_{BUS}) and operating system drivers.

To be able to test the remote wake-up, especially, from those power management states in which the +5 V power source on PCI is not present, for example, $S3_{cold}$, a special connector (J1) is added for an external +5 V source. Any external independent power

supply that provides +5 V ± 5 % @ 2 A stabilized can be used. For example, a standard hub power supply.

Note the distribution of pull-up resistors in the recommended schematics. For example, to achieve correct functionality, it is recommended that you connect the pull-up resistors placed on the PWEn_N and OCn_N input signals of the power switch, for example, MIC2026, to DV_{AUX} NET, maintaining a good condition of these signals even when +3.3 V and +5 V are off. The 'fault flag' pins (OCn_N) of MIC2026 are open-drain and require the presence of pull-up resistors. A 100 nF capacitor is used on each OCn_N signal to prevent false fault conditions.

CLKRUN# is implemented in the ISP1562 on pin 42 and in the ISP1563 on pin 52. This signal is targeted mainly for mobile system designs. CLKRUN is an I/O pin. It is used by the system to safely turn-off the PCI CLK for power saving, with acknowledgment from the ISP1562/3 according to a predefined protocol. In the case of the PCI adapter card design, CLKRUN# must always be LOW because it is not present in the PCI connector. CLKRUN# may directly be connected to GND. For details on CLKRUN# function, refer to *PCI Mobile Design Guide Version 1.1*.

3.2 Input clock: applies only to the ISP1563

You can use either of the following as clock input:

- A 12 MHz crystal; the default recommended solution for best ElectroMagnetic Interference (EMI) results.
- A 48 MHz oscillator; this may be a useful alternative, typically, in the case of on-motherboard design.

Both solutions for the input clock are shown in the schematics.

To use a 48 MHz clock as input, connect the clock signal to the ISP1563 pin 86 (XTAL1), pin 87 (XTAL2) can be left open, and pin 121 (SEL48M) must be pulled up as shown in the schematics.

In an add-on card configuration, normally, the 12 MHz crystal is used. In such a case, oscillators OSC2 and R45 are not necessary. Also, pin 121 (SEL48M) must directly be connected to GND. Another possibility is using a 12 MHz clock as an input. In this case, the 12 MHz-clock signal is directly connected to the ISP1563 pin 86 (XTAL1). This is similar to the case in which the 48 MHz clock is used; however, the ISP1563 pin 121 must still be connected to GND.

3.3 Selecting the number of ports: applies only to the ISP1563

The selection of the number of ports, 2 or 4, is done using the SEL2PORTS signal (ISP1563 pin 5). It must be pulled to LOW, that is, connected to GND, for normal use of all four ports. If SEL2PORTS is HIGH, only two ports, that is, port 1 and port 2, are enabled; one port from each OHCI will be used in this case for performance improvement. Details regarding the power consumption and possible power savings in a two-port configuration can be found in the ISP1563 data sheet.

3.4 Subsystem vendor ID and subsystem device ID

The ISP1562/3 allows loading of the Subsystem Vendor ID (VID) and the Subsystem Device ID (DID) for both EHCI and OHCI from an external EEPROM. Loading of these values in the configuration registers of the ISP1562/3 will occur only if a value of 15h is found in byte 7 of the EEPROM. The necessary signals, I^2C-bus clock and I^2C-bus data,

are defined on pins 96 (SCL) and 97 (SDA) of the ISP1562, and pins 122 (SCL) and 123 (SDA) of the ISP1563, respectively. When not in use, these signals must be connected to ground using a pull-down resistor, typically 10 kΩ.

3.5 Legacy support: applies only to the ISP1563

Legacy signals, IRQ1, IRQ12, A20OUT, KBIRQ1, MUIRQ12 and SMI#, are not normally used on a PCI add-on card design. In this case, the MUIRQ12 and KBIRQ1 input signals must be connected to GND. The other signals that are mentioned in this category (that are outputs) can be left open.

Details on legacy signals and a block diagram showing correct connection of these signals in the case of onboard design can be found in *ISP1563 Eval Board User Manual (UM10066).*

3.6 Overcurrent protection

The ISP1562/3 implements the digital overcurrent protection scheme.

The recommended solution to implement an external overcurrent protection is a standard power switch with integrated overcurrent detection, such as:

- LM3526 and MIC2526 (2 ports), or
- LM3544 (4 ports).

The overcurrent protection logic of the ISP1562/3 uses the following two pins for each USB port:

- PWEn_N: It is used to enable or disable the respective external port power switch. For example, MIC2526 and LM3526.
- OCn_N: It is an input on which a fault condition on the respective USB port is signaled to the ISP1562/3 by the external port power-switching device.

The fault condition that is usually signaled by an external power-switching device can be an overcurrent or a thermal shutdown. The port power-switching integrated devices commonly implement a delay of 1 ms to 3 ms to prevent false OC_N reporting because of inrush currents, when plugging a USB device.

Once a fault condition is received, it will be detected by the operating system and the respective device driver will disable the port power switch by programming the Port Power (PP) bit in the PORTSC register. This device driver is the OHCI driver in the case of an Original USB device to create the fault condition, or the EHCI driver in the case of a Hi-Speed USB device to create the overcurrent condition. This is according to the USB port allocation at the moment when the OC# signal was asserted.

A possible alternative is to use a resettable fuse on each port. This has the advantage of simplicity. It, however, does not inform the operating system of the fault condition and, therefore, no message is generated to inform the user. The resettable fuse will continue to protect the port by switching ‘on or off’ as long as the overcurrent condition persists.

A possible enhancement of this scheme is connecting V_{BUS} to the OCn_N input of the ISP1562/3 to detect the OCn_N condition, the first time V_{BUS} is cut-off a LOW level will appear on the OCn_N pin.

Using only an external PMOS transistor for overcurrent protection is not possible because the ISP1562/3 does not implement the analog overcurrent protection (not measuring the current through the transistor).

4. PCB design recommendations

Some important recommendations for a successful PCB design, applicable to both adapter card and motherboard design solutions, are as follows:

- Typically, a solution using four layers PCB (signal 1, GND, V_{CC}, signal 2) is sufficient for proper routing, allowing you to obtain good functionality and meeting all compliance tests requirements. Start your design by placing the ISP1562/3 chip, the major components, and routing of the high-speed DP and DM traces and clock traces. Also, a complete 'clean' solution for routing the power and GND (split planes) must be defined before you start routing the rest of the signals.
- The trace length for all PCI signals, except the PCI clock signal, to the PCI connector must be limited to a maximum of 1.5 inches.
- The length of the PCI clock signal from the PCI bus connector to the ISP1562/3 must be 2.5 inches ± 0.1 inch in length and must be routed to only one load. It must usually be 'snaked'. Ensure that all corners of this trace are rounded. Do not use 90° sharp corners.
- Route the high-speed USB differential pairs over continuous GND or power planes. Avoid crossing anti-etch areas and any breaks in the internal planes (plane splits). The minimum recommended distance to a plane split is 25 mils. You must also avoid placing a series of via holes near the DP and DM lines because these will create 'break areas' in the GND plane below. This is because of the clearance imposed by the manufacturing process around any via holes to an internal plane.
- Try to keep the length of the DP and DM traces equal. The maximum trace length mismatch between high-speed USB signal pairs must not be greater than 70 mils.
- Maintain parallelism between USB differential signals, with the trace spacing needed to achieve 90 Ω differential impedance. To achieve the required impedance of the pair traces, it is recommended that you use 8 mils traces and keep the distance between the DP and DM traces at 8 mils. These values may vary, depending on the actual PCB parameters.
- Avoid corners when routing the differential pairs DP and DM. Any 90° direction change of traces must be accomplished with two 45° turns or by using an arc of an imaginary circle tangent to the DP and DM lines.
- Avoid routing the USB differential pairs near I/O connectors, signal headers, crystals, oscillators, magnetic devices and power connectors.
- Maintain the maximum possible distance between high-speed USB differential pairs, high-speed or low-speed clock, and non-periodic signals. The minimum recommended distances are as follows:
  - 20 mils between the DP and DM traces and low-speed non-periodic signal traces
  - 50 mils between the DP and DM traces, and clock or high-speed periodic signal traces
  - 20 mils between two pairs of the DP and DM traces
- Avoid creating stubs to connect the 15 kΩ pull-down resistors or to test points. If a stub is unavoidable in the design, no stub must be greater than 80 mils.
- Route all the DP and DM lines on one layer. Do not change layers (avoid using vias) even to avoid crossing a plane split. It is better to place a non-split plane under high-speed USB signals, ground layer or power layer. It is recommended that you place a ground layer beneath the DP and DM lines.

- The maximum allowed length of the DP and DM lines for onboard solutions (or [trace + cable length] for a front-panel solution) is 18 inches.
- A decoupling capacitor must be placed on V_{BUS} as close as possible to each USB connector. A value of about 150 µF/10 V is recommended on each port.
- The common-mode choke used, if really necessary, on the DP and DM lines must be placed as close as possible to the USB connector and must have $Z_{com} < 8\ \Omega$ @ 100 MHz and $Z_{diff} < 300\ \Omega$ @ 100 MHz.
- The common-mode choke, as well as the ElectroStatic Discharge (ESD) protection components will be used only if necessary (in case the design does not pass EMI or the ESD tests) because these may affect the signaling quality. Nevertheless, it is recommended that you include the necessary footprints for common-mode chokes and ESD protection components on the PCB as safeguards. The footprints must be placed as close as possible to the USB connector. Special attention must be given when placing additional components on the DP and DM lines and routing recommendations must be followed.
- Both V_{DDA_AUX} (analog) and $V_{CC(I/O)\_AUX}$ (digital) are derived from the PCI V_{AUX} voltage, found on pin A14 of the PCI connector. $V_{CC(I/O)\_AUX}$ can directly be connected to PCI V_{AUX}. V_{DDA_AUX} is separated from PCI V_{AUX} by an inductor and each of $V_{CC(I/O)\_AUX}$ and V_{DDA_AUX} uses its own decoupling capacitors.
- The design must ensure that the V_{DDA_AUX} and $V_{CC(I/O)\_AUX}$ power planes are isolated from the main PCI 3.3 V power plane. This is achieved by creating two separate power planes that do not come in contact with the PCI 3.3 V power plane.
- The decoupling capacitors must be placed as close as possible to the ISP1562/3. A good choice is the four corners of the IC because these areas will not normally be occupied by traces or other components, according to the ISP1562/3 pinout.
- For good EMI testing results, it is recommended that you provide a good path from the USB connector shell to the chassis ground. The USB connector shell must be connected to an isolated ground plane.

For more information, refer to the Intel document *The USB 2.0 Platform Design Guideline, Rev. 1.0*.

5. Schematics

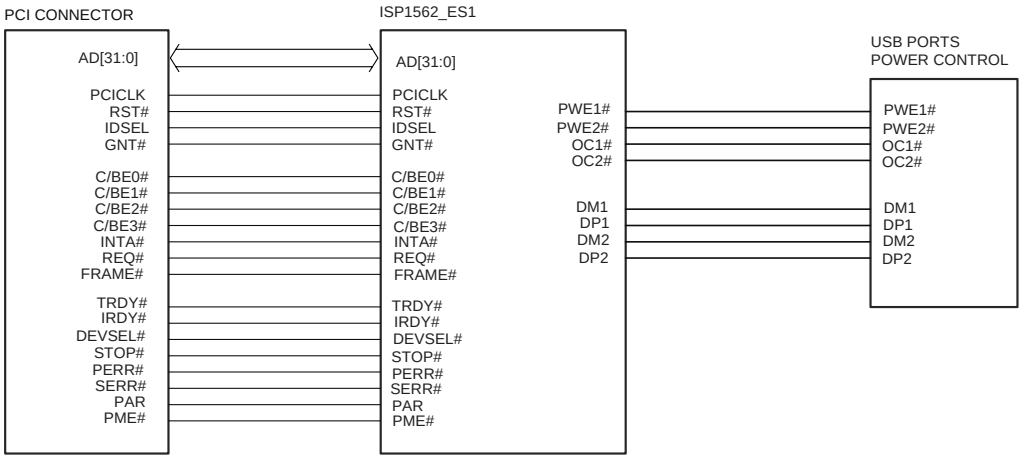

Fig 1. ISP1562 eval board schematic – top level interfaces

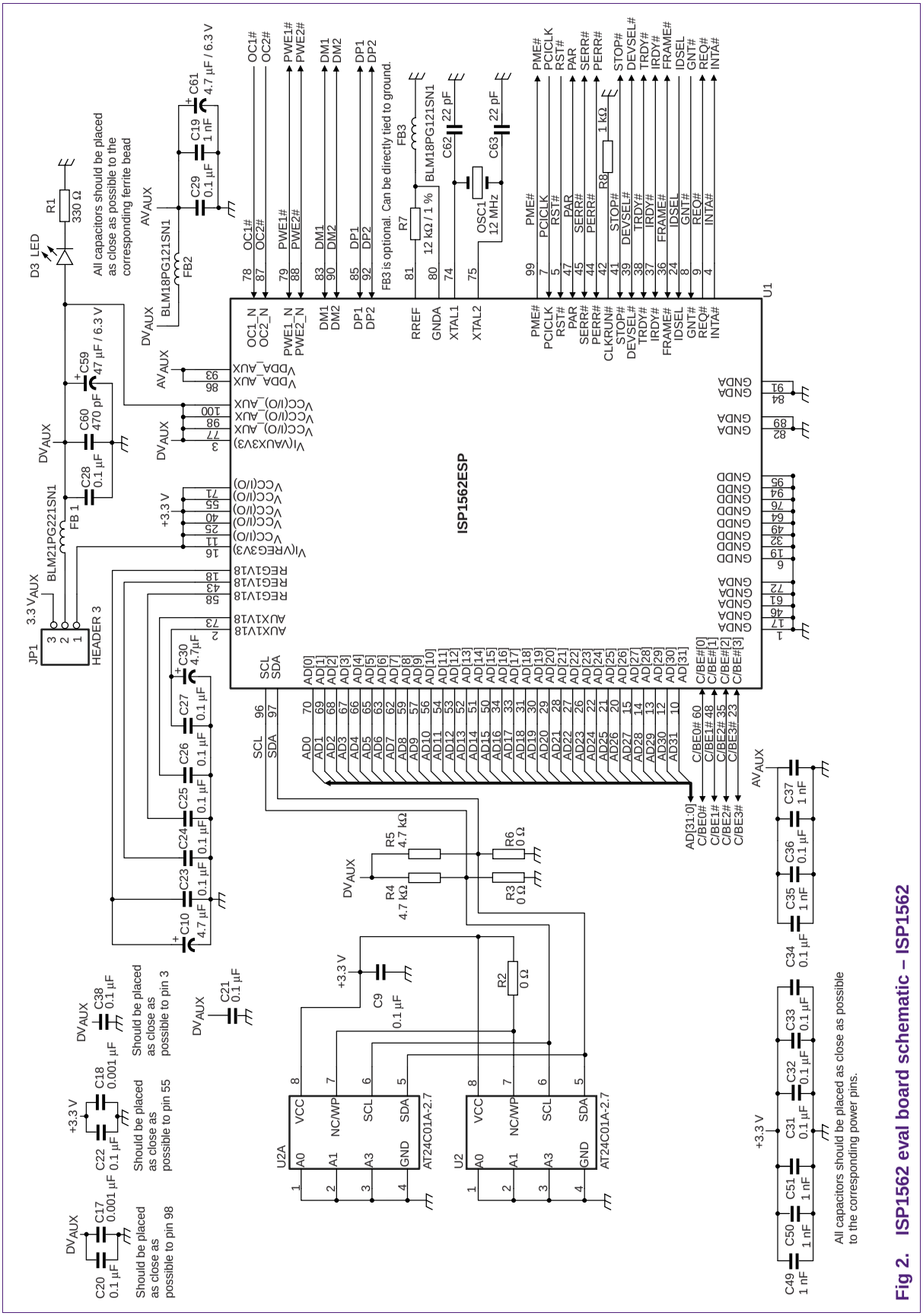

Fig 2. ISP1562 eval board schematic – ISP1562

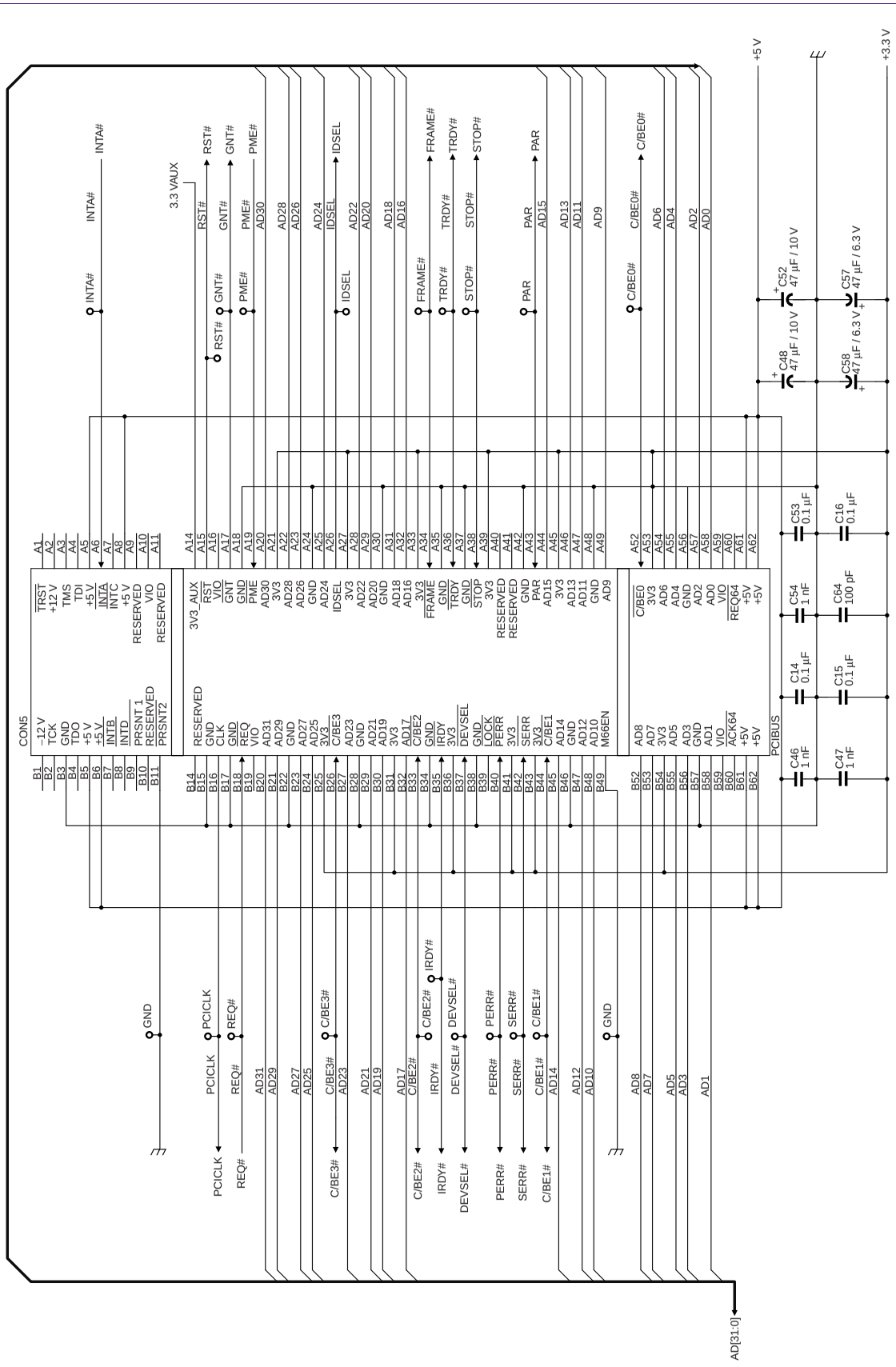

Fig 3. ISP1562 eval board schematic – PCI edge connector

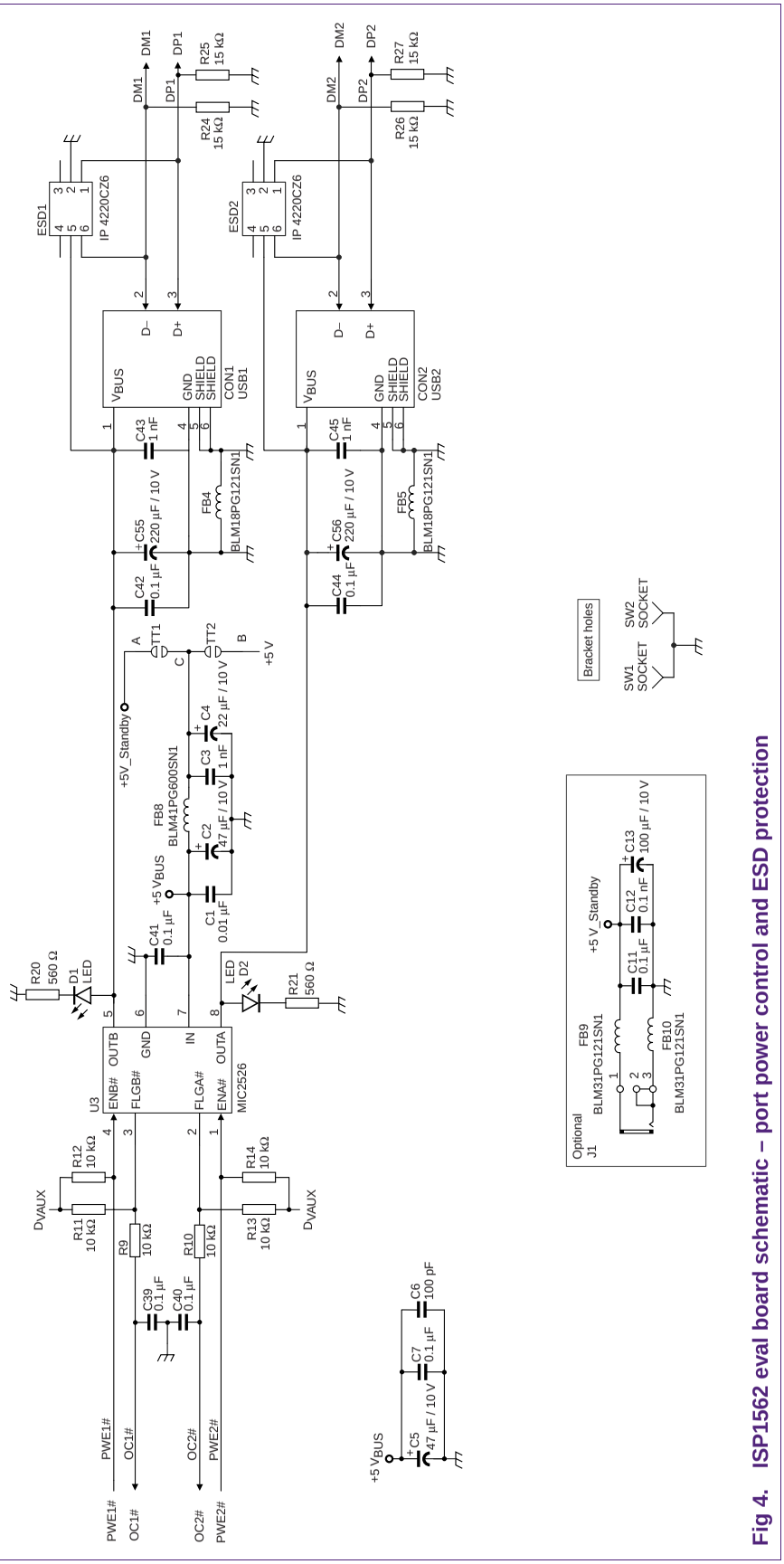

Fig 4. ISP1562 eval board schematic – port power control and ESD protection

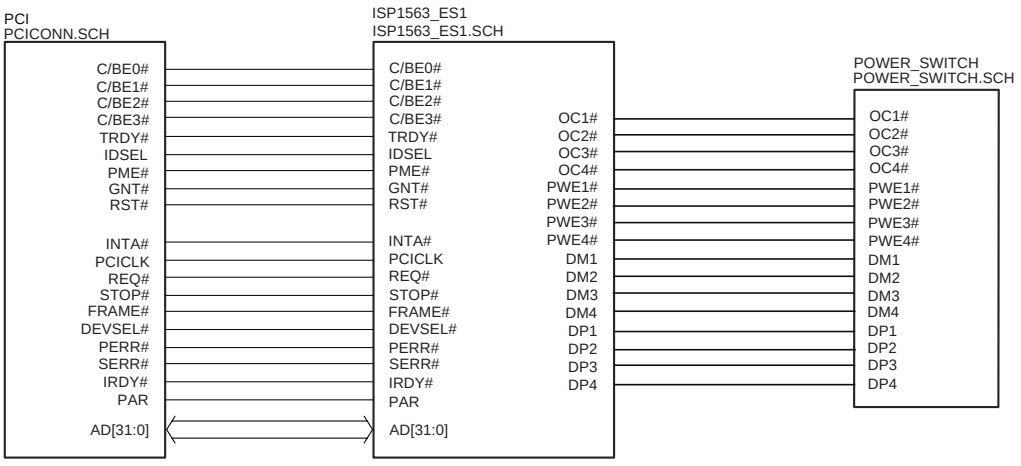

Fig 5. ISP1563 eval board schematic – top-level interfaces

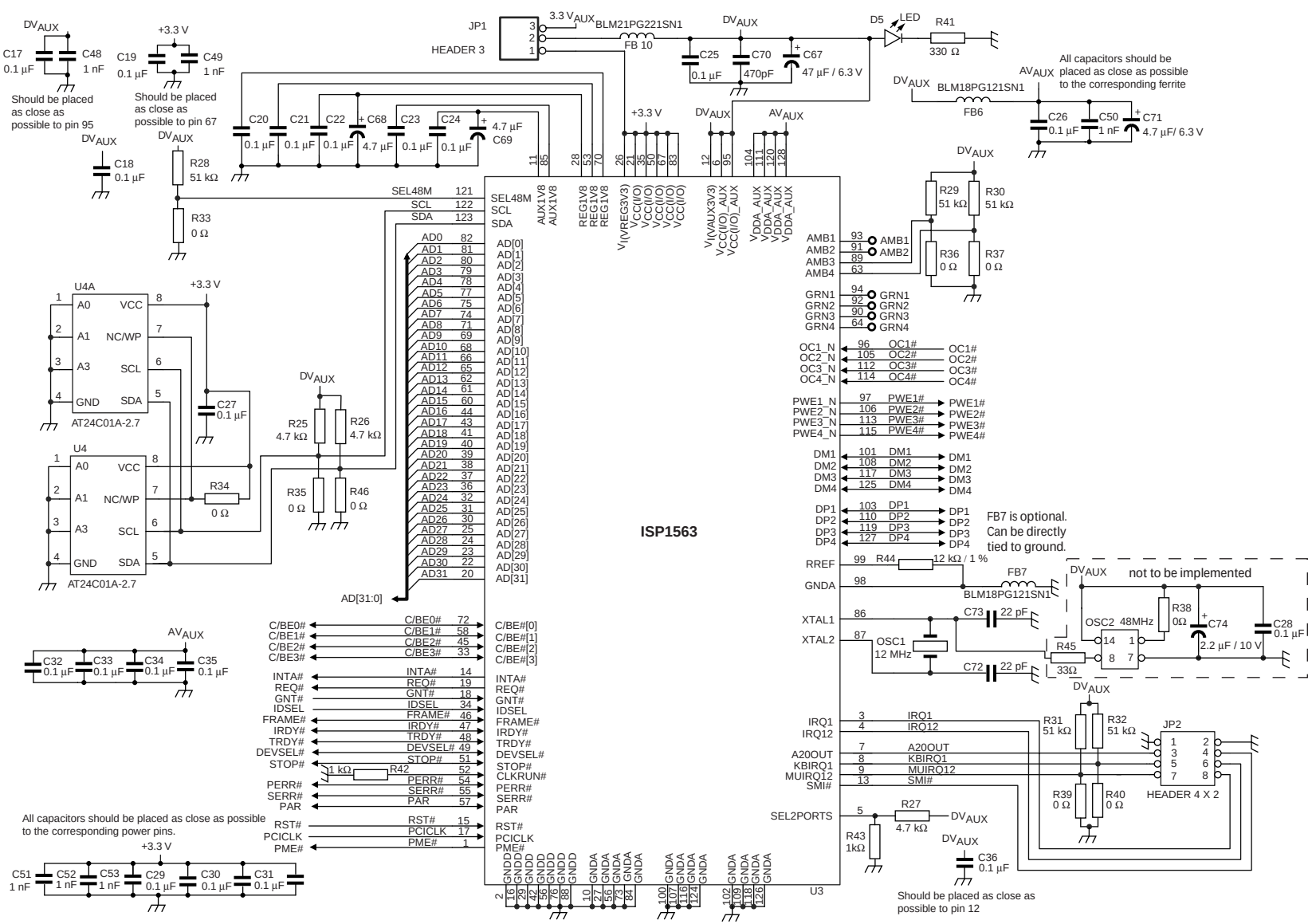

Fig 6. ISP1563 eval board schematic – ISP1563

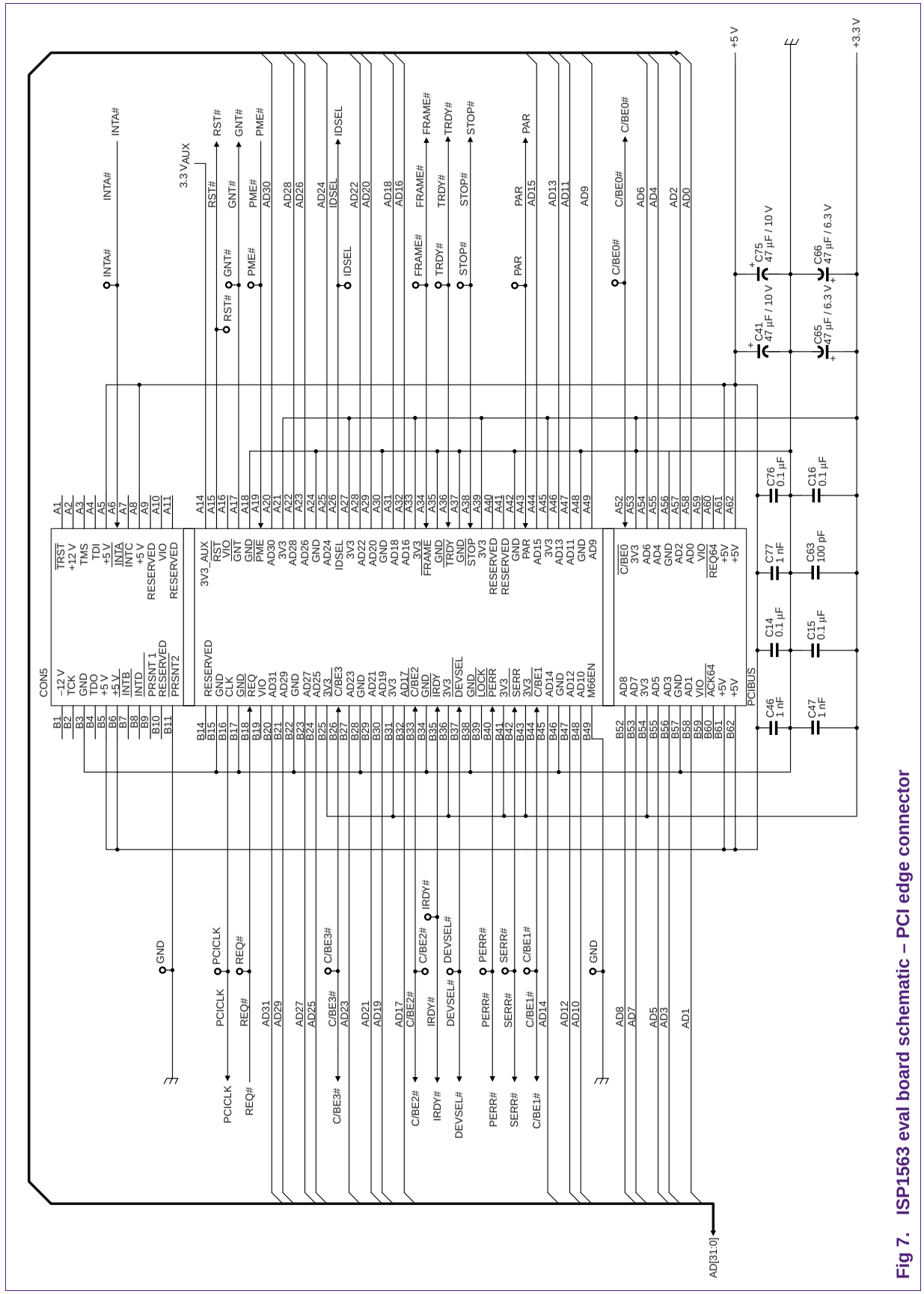

Fig 7. ISP1563 eval board schematic – PCI edge connector

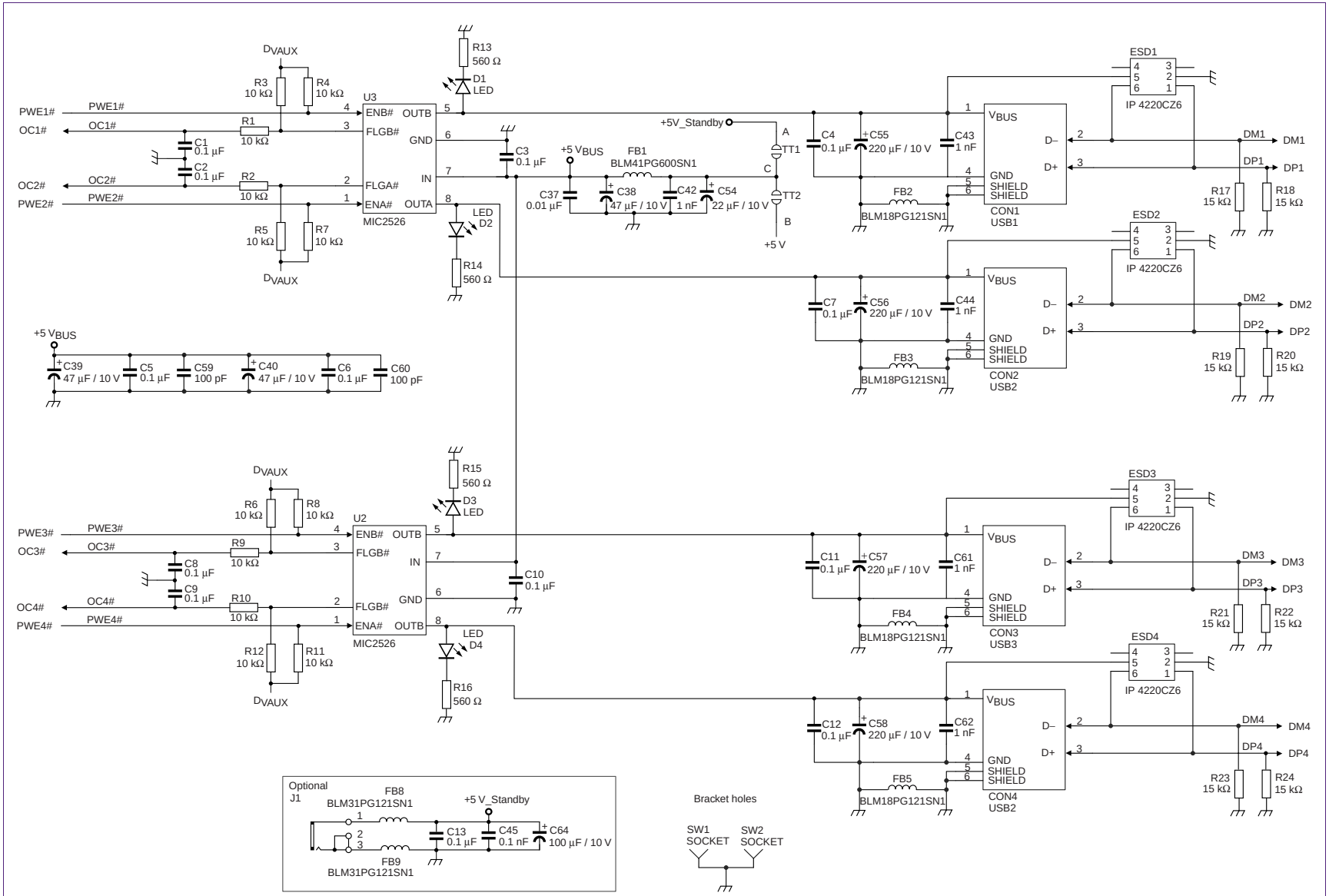

Fig 8. ISP1563 eval board schematic – port power control and ESD protection

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