OKI Semiconductor

MSM80C154S/83C154S

CMOS 8-bit Microcontroller

GENERAL DESCRIPTION

The MSM80C154S/MSM83C154S, designed for the high speed version of the existing MSM80C154/MSM83C154, is a higher performance 8-bit microcontroller providing low-power consumption.
The MSM80C154S/MSM83C154S covers the functions and operating range of the existing MSM80C154/83C154/80C51F/80C31F.
The MSM80C154S is identical to the MSM83C154S except it does not contain the internal program memory (ROM).

FEATURES

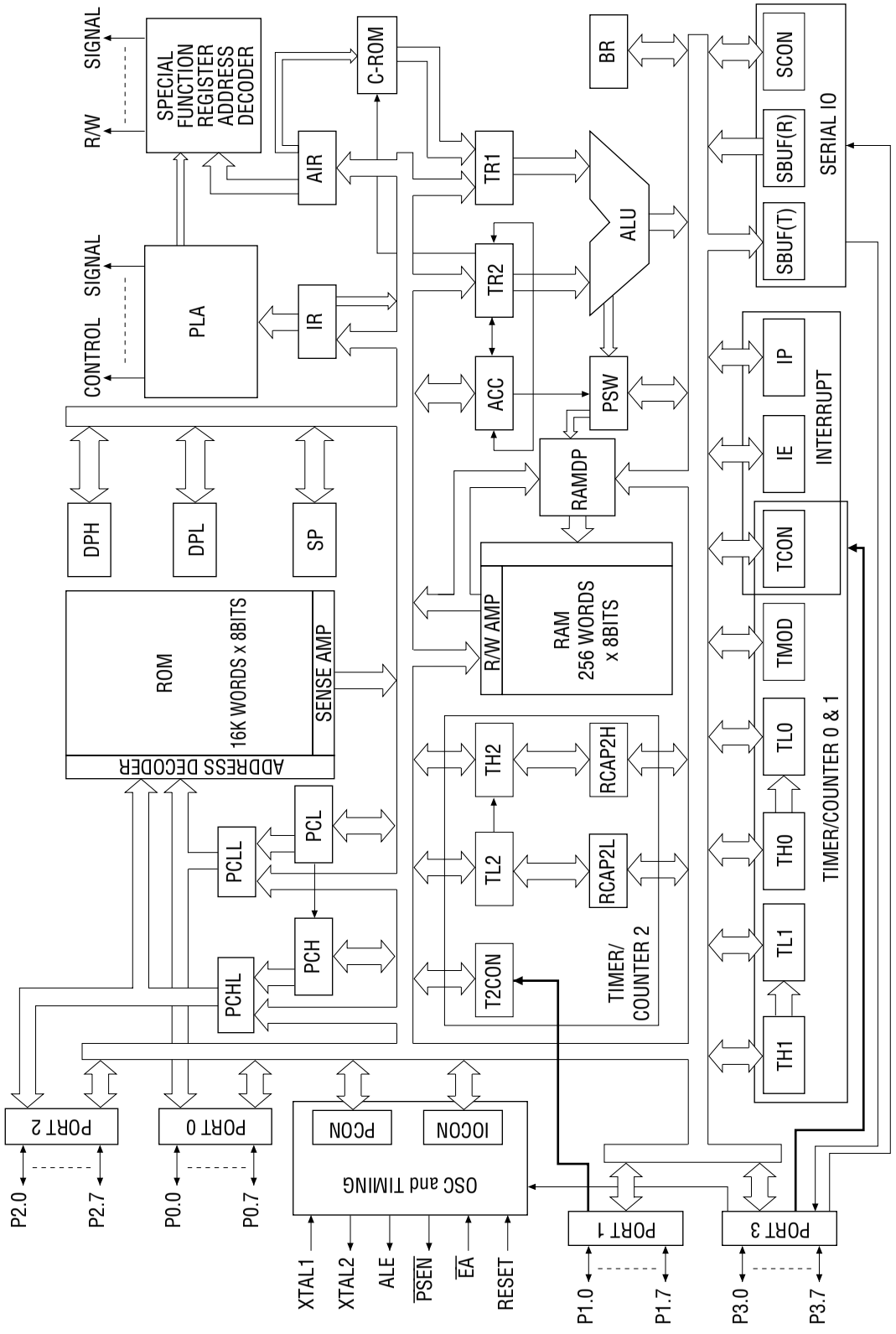
- Operating range
  - Operating frequency : 0 to 3 MHz (V_{CC}=2.2 to 6.0 V)
    0 to 12 MHz (V_{CC}=3.0 to 6.0 V)
    0 to 24 MHz (V_{CC}=4.5 to 6.0 V)
  - Operating voltage : 2.2 to 6.0 V
  - Operating temperature : –40 to +85°C (Operation at +125°C conforms to the other specification.)
- Fully static circuit
- Upward compatible with the MSM80C51F/80C31F
- On-chip program memory : 16K words x 8 bits ROM (MSM83C154S only)
- On-chip data memory : 256 words x 8 bits RAM
- External program memory address space : 64K bytes ROM (Max)
- External data memory address space : 64K bytes RAM
- I/O ports : 4 ports x 8 bits
  (Port 1, 2, 3, impedance programmable) : 32
- 16-bit timer/counters : 3
- Multifunctional serial port : I/O Expansion mode
  : UART mode (featuring error detection)
- 6-source 2-priority level
  Interrupt and multi-level
  Interrupt available by programming IP and IE registers
- Memory-mapped special function registers
- Bit addressable data memory and SFRs
- Minimum instruction cycle : 500 ns @ 24 MHz operation
- Standby functions : Power-down mode (oscillator stop)
  Activated by software or hardware; providing ports with floating or active status
  The software power-down stet mode is terminated by interrupt signal enabling execution from the interrupted address.

• Package options

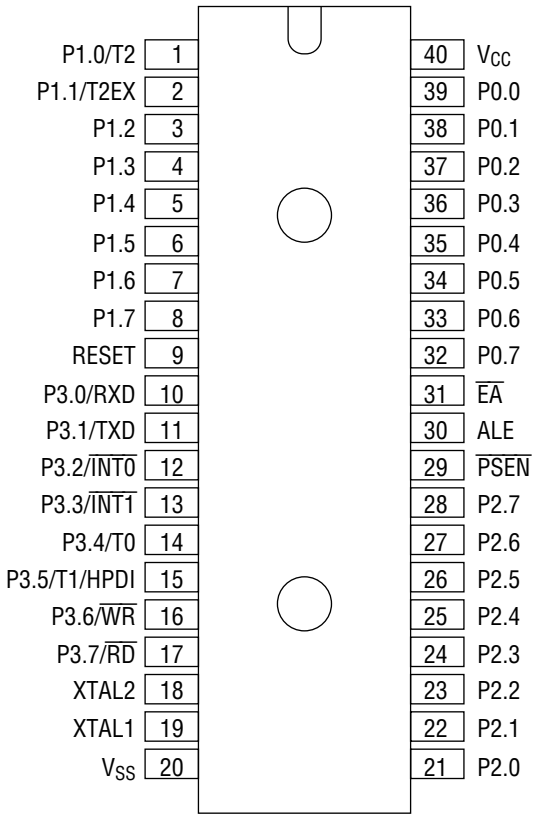
40-pin plastic DIP (DIP40-P-600-2.54)	:	(Product name: MSM80C154SRS/ MSM83C154S-xxxRS)
44-pin plastic QFP (QFP44-P-910-0.80-2K)	:	(Product name: MSM80C154SGS-2K/ MSM83C154S-xxxGS-2K)
44-pin QFJ (QFJ44-P-S650-1.27)	:	(Product name: MSM80C154SJS/ MSM83C154S-xxxJS)
44-pin TQFP (TQFP44-P-1010-0.80-K)	:	(Product name: MSM80C154STS-K/ MSM83C154S-xxxTS-K)

xxx: indicates the code number

BLOCK DIAGRAM (MSM83C154S)

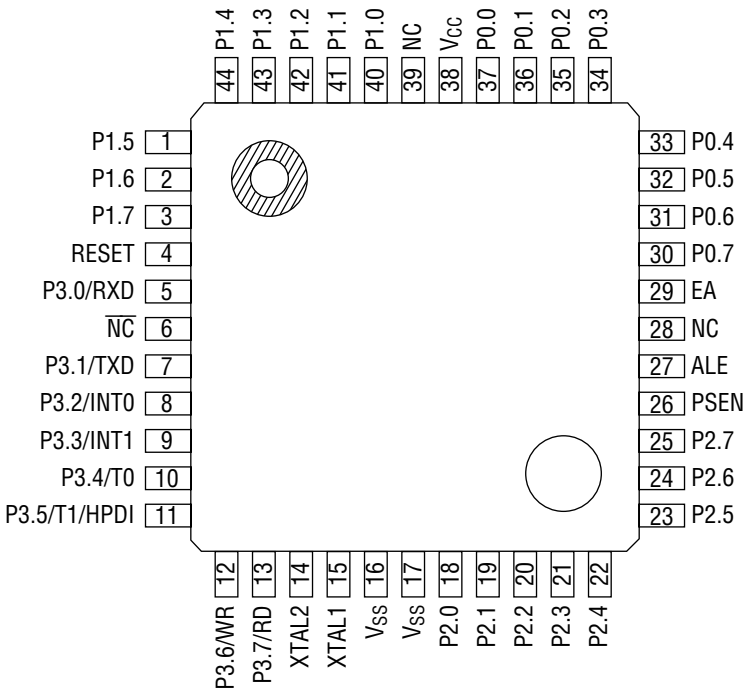


PIN CONFIGURATION (TOP VIEW)



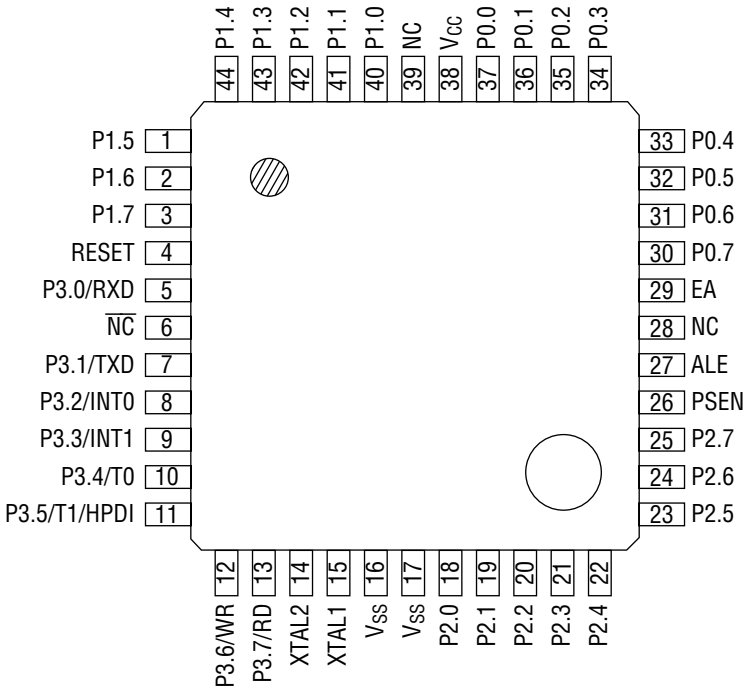
40-Pin Plastic DIP

PIN CONFIGURATION (Continued)



NC : No-connection pin

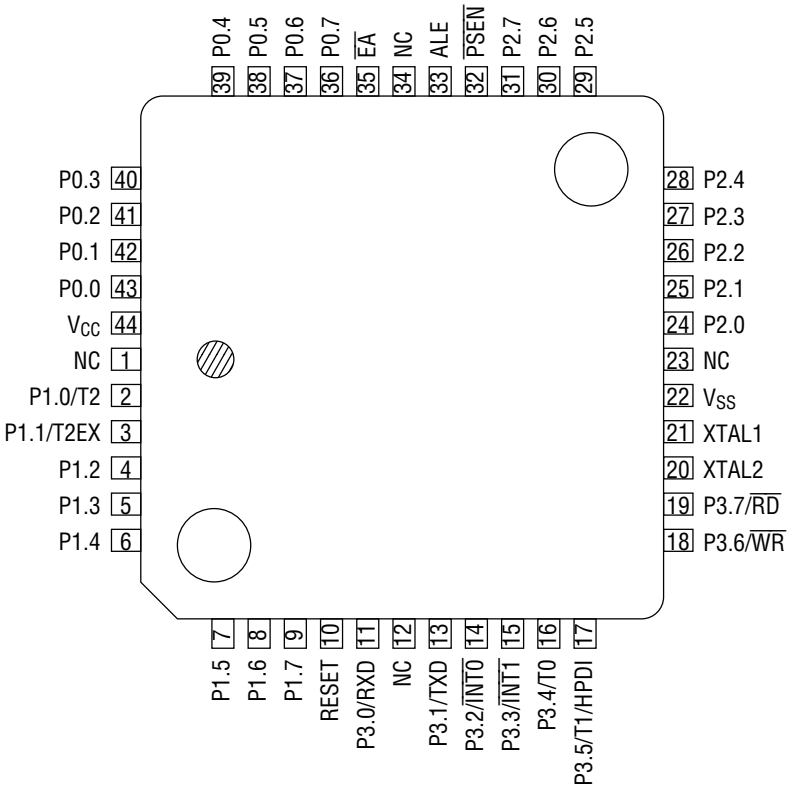
44-Pin Plastic QFP



NC : No-connection pin

44-Pin Plastic TQFP

PIN CONFIGURATION (Continued)



NC : No-connection pin

44-Pin Plastic QFJ

PIN DESCRIPTIONS

Symbol	Descriptipn
P0.0 to P0.7	Bidirectional I/O ports. They are also the data/address bus (input/output of data and output of lower 8-bit address when external memory is accessed). They are open-drain outputs when used as I/O ports, but 3-state outputs when used as data/address bus.
P1.0 to P1.7	P1.0 to P1.7 are quasi-bidirectional I/O ports. They are pulled up internally when used as input ports. Two of them have the following secondary functions: •P1.0 (T2) : used as external clock input pins for the timer/counter 2. •P1.1 (T2EX) : used as trigger input for the timer/counter 2 to be reloaded or captured; causing the timer/counter 2 interrupt.
P2.0 to P2.7	P2.0 to P2.7 are quasi-bidirectional I/O ports. They also output the higher 8-bit address when an external memory is accessed. They are pulled up internally when used as input ports.
P3.0 to P3.7	P3.0 to P3.7 are quasi-bidirectional I/O ports. They are pulled up internally when used as input ports. They also have the following secondary functions: •P3.0 (RXD) Serial data input/output in the I/O expansion mode and serial data input in the UART mode when the serial port is used. •3.1 (TXD) Synchronous clock output in the I/O expansion mode and serial data output in the UART mode when the serial port is used. •3.2 ($\overline{INT0}$) Used as input pin for the external interrupt 0, and as count-up control pin for the timer/counter 0. •3.3 ($\overline{INT1}$) Used as input pin for the external interrupt 1, and as count-up control pin for the timer/counter 1. •3.4 (T0) Used as external clock input pin for the timer/counter 0. •3.5 (T1) Used as external clock input pin for the timer/counter 1 and power-down-mode control input pin. •3.6 ($\overline{WR}$) Output of the write-strobe signal when data is written into external data memory. •3.7 ($\overline{RD}$) Output of the read-strobe signal when data is read from external data memory.
ALE	Address latch enable output for latching the lower 8-bit address during external memory access. Two ALE pulses are activated per machine cycle except during external data memory access at which time one ALE pulse is skipped.
$\overline{PSEN}$	Program store enable output which enables the external memory output to the bus during external program memory access. Two $\overline{PSEN}$ pulses are activated per machine cycle except during external data memory access at which two $\overline{PSEN}$ pulses are skipped.
$\overline{EA}$	When $\overline{EA}$ is held at "H" level, the MSM 83C154S executes instructions from internal program memory at address 0000H to 3FFFH, and executes instructions from external program memory above address 3FFFH. When $\overline{EA}$ is held at "L" level, the MSM80C154S/MSM83C154S executes instructions from external program memory for all addresses.

PIN Descriptions (Continued)

Symbol	Descriptipn
RESET	If this pin remains "H" for at least one machine cycle, the MSM80C154S/MSM83C154S is reset. Since this pin is pulled down internally, a power-on reset is achieved by simply connecting a capacitor between V_{CC} and this pin.
XTAL1	Oscillator inverter input pin. External clock is input through XTAL1 pin.
XTAL2	Oscillator inverter output pin.
V_{CC}	Power supply pin during both normal operation and standby operations.
V_{SS}	GND pin.

REGISTERS

Diagram of Special Function Registers

REGISTER NAME	BIT ADDRESS								DIRECT ADDRESS
	b7	b6	b5	b4	b3	b2	b1	b0	
IOCON	FF	FE	FD	FC	FB	FA	F9	F8	0F8H (248)
B	F7	F6	F5	F4	F3	F2	F1	F0	0F0H (240)
ACC	E7	E6	E5	E4	E3	E2	E1	E0	0E0H (224)
PSW	D7	D6	D5	D4	D3	D2	D1	D0	0D0H (208)
TH2									0CDH (205)
TL2									0CCH (204)
RCAP2H									0CBH (203)
RCAP2L									0CAH (202)
T2CON	CF	CE	CD	CC	CB	CA	C9	C8	0C8H (200)
IP	BF	BE	BD	BC	BB	BA	B9	B8	0B8H (184)
P3	B7	B6	B5	B4	B3	B2	B1	B0	0B0H (176)
IE	AF	AE	AD	AC	AB	AA	A9	A8	0A8H (168)
P2	A7	A6	A5	A4	A3	A2	A1	A0	0A0H (160)
SBUF									99H (153)
SCON	9F	9E	9D	9C	9B	9A	99	98	98H (152)
P1	97	96	95	94	93	92	91	90	90H (144)
TH1									8DH (141)
TH0									8CH (140)
TL1									8BH (139)
TL0									8AH (138)
TMOD									89H (137)
TCON	8F	8E	8D	8C	8B	8A	89	88	88H (136)
PCON									87H (135)
DPH									83H (131)
DPL									82H (130)
SP									81H (129)
P0	87	86	85	84	83	82	81	80	80H (128)

Special Function Registers

Timer mode register (TMOD)

NAME	ADDRESS	MSB 7	6	5	4	3	2	1	LSB 0
TMOD	89H	GATE	C/$\overline{T}$	M1	M0	GATE	C/$\overline{T}$	M1	M0

BIT LOCATION	FLAG	FUNCTION		
TMOD.0	M0	M1	M0	Timer/counter 0 mode setting
		0	0	8-bit timer/counter with 5-bit prescalar.
		0	1	16-bit timer/counter.
		1	0	8-bit timer/counter with 8-bit auto reloading.
TMOD.1	M1	1	1	Timer/counter 0 separated into TL0 (8-bit) timer/counter and TH0 (8-bit) timer/counter. TF0 is set by TL0 carry, and TF1 is set by TH0 carry.
TMOD.2	C/$\overline{T}$	Timer/counter 0 count clock designation control bit. XTAL1•2 divided by 12 clocks is the input applied to timer/counter 0 when C/$\overline{T}$ = "0". The external clock applied to the T0 pin is the input applied to timer/counter 0 when C/$\overline{T}$ = "1".		
TMOD.3	GATE	When this bit is "0", the TR0 bit of TCON (timer control register) is used to control the start and stop of timer/counter 0 counting. If this bit is "1", timer/counter 0 starts counting when both the TR0 bit of TCON and $\overline{INT0}$ pin input signal are "1", and stops counting when either is changed to "0".		
TMOD.4	M0	M1	M0	Timer/counter 1 mode setting
		0	0	8-bit timer/counter with 5-bit prescalar.
		0	1	16-bit timer/counter
		1	0	8-bit timer/counter with 8-bit auto reloading.
TMOD.5	M1	1	1	Timer/counter 1 operation stopped.
TMOD.6	C/$\overline{T}$	Timer/counter 1 count clock designation control bit. XTAL1•2 divided by 12 clocks is the input applied to timer/counter 1 when C/$\overline{T}$ = "0". The external clock applied to the T1 pin is the input applied to timer/counter 1 when C/$\overline{T}$ = "1".		
TMOD.7	GATE	When this bit is "0", the TR1 bit of TCON is used to control the start and stop of timer/counter 1 counting. If this bit is "1", timer/counter 1 starts counting when both the TR1 bit of TCON and $\overline{INT1}$ pin input signal are "1", and stops counting when either is changed to "0".		

Power control register (PCON)

NAME	ADDRESS	MSB 7	6	5	4	3	2	1	LSB 0
PCON	87H	SMOD	HPD	RPD	—	GF1	GF0	PD	IDL

BIT LOCATION	FLAG	FUNCTION
PCON.0	IDL	IDLE mode is set when this bit is set to "1". CPU operations are stopped when IDLE mode is set, but XTAL1•2, timer/counters 0, 1 and 2, the interrupt circuits, and the serial port remain active. IDLE mode is cancelled when the CPU is reset or when an interrupt is generated.
PCON.1	PD	PD mode is set when this bit is set to "1". CPU operations and XTAL1•2 are stopped when PD mode is set. PD mode is cancelled when the CPU is reset or when an interrupt is generated.
PCON.2	GF0	General purpose bit.
PCON.3	GF1	General purpose bit.
PCON.4	—	Reserved bit. The output data is "1", if the bit is read.
PCON.5	RPD	This bit is used to specify cancellation of CPU power down mode (IDLE or PD) by an interrupt signal. Power-down mode cannot be cancelled by an interrupt signal if the interrupt is not enabled by IE (interrupt enable register) when this bit is "0". If the interrupt flag is set to "1" by an interrupt request signal when this bit is "1" (even if interrupt is disabled), the program is executed from the next address of the power-down-mode setting instruction. The flag is reset to "0" by software.
PCON.6	HPD	The hard power-down setting mode in enabled when this bit is set to "1". If the level of the power failure detect signal applied to the HPDI pin (pin 3.5) is changed from "1" to "0" when this bit is "1", XTAL1•2 oscillation is stopped and the system is put into hard power down mode. HPD mode is cancelled when the CPU is reset.
PCON.7	SMOD	When the timer/counter 1 carry signal is used as a clock in mode 1, 2 or 3 of the serial port, this bit has the following functions. The serial port operation clock is reduced by 1/2 when the bit is "0" for delayed processing. When the bit is "1", the serial port operation clock is normal for faster processing.

Timer control register (TCON)

NAME	ADDRESS	MSB 7	6	5	4	3	2	1	LSB 0
TCON	88H	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0
BIT LOCATION	**FLAG**	**FUNCTION**							
TCON.0	IT0	External interrupt 0 signal is used in level-detect mode when this bit is "0" and in trigger detect mode when "1".							
TCON.1	IE0	Interrupt request flag for external interrupt 0. The bit is reset automatically when an interrupt is serviced. The bit can be set and reset by software when IT0 = "1".							
TCON.2	IT1	External interrupt 1 signal is used in level detect mode when this bit is "0", and in trigger detect mode when "1".							
TCON.3	IE1	Interrupt request flag for external interrupt 1. The bit is reset automatically when an interrupt is serviced. The bit can be set and reset by software when IT1 = "1".							
TCON.4	TR0	Counting start and stop control bit for timer/counter 0. Timer/counter 0 starts counting when this bit is "1", and stops counitng when "0".							
TCON.5	TF0	Interrupt request flag for timer interrupt 0. The bit is reset automatically when an interrupt is serviced. The bit is set to "1" when a carry signal is generated from timer/counter 0.							
TCON.6	TR1	Counting start and stop control bit for timer/counter 1. The timer/counter 1 starts counting when this bit is "1", and stops counting when "0".							
TCON.7	TF1	Interrupt request flag for timer interrupt 1. The bit is reset automatically when interrupt is serviced. The bit is set to "1" when carry signal is generated from timer/counter 1.							

Serial port control register (SCON)

NAME	ADDRESS	MSB 7	6	5	4	3	2	1	LSB 0
SCON	98H	SM0	SM1	SM2	REN	TB8	RB8	TI	RI

BIT LOCATION	FLAG	FUNCTION
SCON.0	RI	"End of serial port reception" interrupt request flag. This flag must be reset by software during interrupt service routine. This flag is set after the eighth bit of data has been received when in mode 0, or by the STOP bit when in any other mode. In mode 2 or 3, however, RI is not set if the RB8 data is "0" with SM2 = "1". RI is set in mode 1 if STOP bit is received when SM2 = "1".
SCON.1	TI	"End of serial port tramsmission" interrupt request flag. This flag must be reset by software during interrupt service routine. This flag is set after the eighth bit of data has been sent when in mode 0, or after the last bit of data has been sent when in any other mode.
SCON.2	RB8	The ninth bit of data received in mode 2 or 3 is passed to RB8. The STOP bit is applied to RB8 if SM2 = "0" when in mode 1. RB8 can not be used in mode 0.
SCON.3	TB8	The TB8 data is sent as the ninth data bit when in mode 2 or 3. Any desired data can be set in TB8 by software.
SCON.4	REN	Reception enable control bit. No reception when REN = "0". Reception enabled when REN = "1".
SCON.5	SM2	If the ninth bit of received data is "0" with SM2 = "1" in mode 2 or 3, the "end of reception" signal is not set in the RI flag. The "end of reception" signal set in the RI flag if the STOP bit is not "1" when SM2 = "1" in mode 1.
SCON.6	SM1	SM0 = 0, SM1 = 0, MODE = 0: 8-bit shift register I/O
		SM0 = 0, SM1 = 1, MODE = 1: 8-bit UART variable baud rate
SCON.7	SM0	SM0 = 1, SM1 = 0, MODE = 2: 9-bit UART 1/32 XTAL1, 1/64 XTAL1 baud rate
		SM0 = 1, SM1 = 1, MODE = 3: 9-bit UART variable baud rate

Interrupt enable register (IE)

NAME	ADDRESS	MSB 7	6	5	4	3	2	1	LSB 0
IE	0A8H	EA	—	ET2	ES	ET1	EX1	ET0	EX0

BIT LOCATION	FLAG	FUNCTION
IE.0	EX0	Interrupt control bit for external interrupt 0. Interrupt disabled when bit is "0". Interrupt enabled when bit is "1".
IE.1	ET0	Interrupt control bit for timer interrupt 0. Interrupt disabled when bit is "0". Interrupt enabled when bit is "1".
IE.2	EX1	Interrupt control bit for external interrupt 1. Interrupt disabled when bit is "0". Interrupt enabled when bit is "1".
IE.3	ET1	Interrupt control bit for timer interrupt 1. Interrupt disabled when bit is "0". Interrupt enabled when bit is "1".
IE.4	ES	Interrupt control bit for serial port. Interrupt disabled when bit is "0". Interrupt enabled when bit is "1".
IE.5	ET2	Interrupt control bit for timer interrupt 2. Interrupt disabled when bit is "0". Interrupt enabled when bit is "1".
IE.6	—	Reserved bit. The output data is "1" if the bit is read.
IE.7	EA	Overall interrupt control bit. All interrupts are disabled when bit is "0". All interrupts are controlled by IE.0 thru IE.5 when bit is "1".

Interrupt priority register (IP)

NAME	ADDRESS	MSB 7	6	5	4	3	2	1	LSB 0
IP	0B8H	PCT	—	PT2	PS	PT1	PX1	PT0	PX0

BIT LOCATION	FLAG	FUNCTION
IP.0	PX0	Interrupt priority bit for external interrupt 0. Priority is assigned when bit is "1".
IP.1	PT0	Interrupt priority bit for timer interrupt 0. Priority is assigned when bit is "1".
IP.2	PX1	Interrupt priority bit for external interrupt 1. Priority is assigned when bit is "1".
IP.3	PT1	Interrupt priority bit for timer interrupt 1. Priority is assigned when bit is "1".
IP.4	PS	Interrupt priority bit for serial port. Priority is assigned when bit is "1".
IP.5	PT2	Interrupt priority bit for timer interrupt 2. Priority is assigned when bit is "1".
IP.6	—	Reserved bit. The output data is "1" if the bit is read.
IP.7	PCT	Priority interrupt circuit control bit. The priority register contents are valid and priority assigned interrupts can be processed when this bit is "0". When the bit is "1", the priority interrupt circuit is stopped, and interrupts can only be controlled by the interrupt enable register (IE).

Program status word register (PSW)

NAME	ADDRESS	MSB 7	6	5	4	3	2	1	LSB 0
PSW	0D0H	CY	AC	F0	RS1	RS0	OV	F1	P

BIT LOCATION	FLAG	FUNCTION
PSW.0	P	Accumulator (ACC) parity indicator. This bit is "1" when the "1" bit number in the accumulator is an odd number, and "0" when an even number.
PSW.1	F1	User flag which may be set to "0" or "1" as desired by the user.
PSW.2	OV	Overflow flag which is set if the carry C6 from bit 6 of the ALU or CY is "1" as a result of an arithmetic operation. The flag is also set to "1" if the resultant product of executing multiplication instruction (MUL AB) is greater than 0FFH, but is reset to "0" if the product is less than or equal to 0FFH.
PSW.3	RS0	RAM register bank switch
PSW.4	RS1	

RS1	RS0	BANK	RAM ADDRESS
0	0	0	00H - 07H
0	1	1	08H - 0FH
1	0	2	10H - 17H
1	1	3	18H - 1FH

PSW.5	F0	User flag which may be set to "0" or "1" as desired by the user.
PSW.6	AC	Auxiliary carry flag. This flag is set to "1" if a carry C_3 is generated from bit 3 of the ALU as a result of executing an arithmetic operation instruction. In all other cases, the flag is reset to "0".
PSW.7	CY	Main carry flag. This flag is set to "1" if a carry C_7 is generated from bit 7 of the ALU as result of executing an arithmetic operation instruction. If a carry C_7 is not generated, the flag is reset to "0".

I/O control register (IOCON)

NAME	ADDRESS	MSB 7	6	5	4	3	2	1	LSB 0
IOCON	0F8H	—	T32	SERR	IZC	P3HZ	P2HZ	P1HZ	ALF

BIT LOCATION	FLAG	FUNCTION
IOCON.0	ALF	If CPU power down mode (PD, HPD) is activated with this bit set to "1", the outputs from ports 0, 1, 2, and 3 are switched to floating status. When this bit is "0", ports 0, 1, 2, and 3 are in output mode.
IOCON.1	P1HZ	Port 1 becomes a high impedance input port when this bit is "1".
IOCON.2	P2HZ	Port 2 becomes a high impedance input port when this bit is "1".
IOCON.3	P3HZ	Port 3 becomes a high impedance input port when this bit is "1".
IOCON.4	IZC	The 10 kΩ pull-up resistor for ports 1, 2, and 3 is switched off when this bit is "1", leaving only the 100 kΩ pull-up resistor.
IOCON.5	SERR	Serial port reception error flag. This flag is set to "1" if an overrun or framing error is generated when data is received at a serial port. The flag is reset by software.
IOCON.6	T32	Timer/counters 0 and 1 are connected serially to from a 32-bit timer/counter when this bit is set to "1". TF1 of TCON is set if a carry is generated in the 32-bit timer/counter.
IOCON.7	—	Leave this bit at "0".

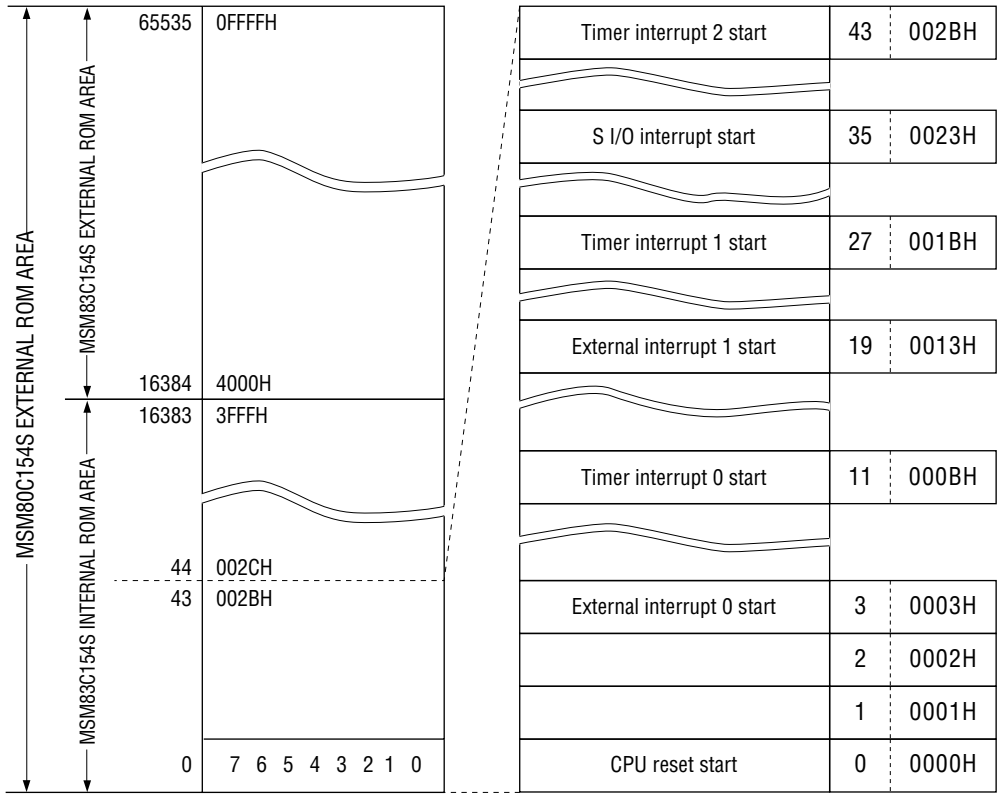
Timer 2 control register (T2CON)

NAME	ADDRESS	MSB 7	6	5	4	3	2	1	LSB 0
T2CON	0C8H	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/$\overline{T2}$	CP/$\overline{RL2}$

BIT LOCATION	FLAG	FUNCTION
T2CON.0	CP/$\overline{RL2}$	Capture mode is set when TCLK + RCLK = "0" and CP/$\overline{RL2}$ = "1". 16-bit auto reload mode is set when TCLK + RCLK = "0" and CP/$\overline{RL2}$ = "0". CP/$\overline{RL2}$ is ignored when TCLK + RCLK = "1".
T2CON.1	C/$\overline{T2}$	Timer/counter 2 count clock designation control bit. The internal clocks (XTAL1•2 ÷ 12, XTAL1•2 ÷ 2) are used when this bit is "0", and the external clock applied to the T2 pin is passed to timer/counter 2 when the bit is "1".
T2CON.2	TR2	Timer/counter 2 counting start and stop control bit. Timer/counter 2 commences counting when this bit is "1" and stops counting when "0".
T2CON.3	EXEN2	T2EX timer/counter 2 external control signal control bit. Input of the T2EX signal is disabled when this bit is "0", and enabled when "1".
T2CON.4	TCLK	Serial port transmit circuit drive clock control bit. Timer/counter 2 is switched to baud rate generator mode when this bit is "1", and the timer/counter 2 carry signal becomes the serial port transmit clock. Note, however, that the serial ports can only use the timer/counter 2 carry signal in serial port modes 1 and 3.
T2CON.5	RCLK	Serial port receive circuit drive clock control bit. Timer/counter 2 is switched to baud rate generator mode when this bit is "1", and the timer/counter 2 carry signal becomes the serial port transmit clock. Note, however, that the serial ports can only use the timer/counter 2 carry signal in serial port modes 1 and 3.
T2CON.6	EXF2	Timer/counter 2 external flag. This bit is set to "1" when the T2EX timer/counter 2 external control signal level is changed from "1" to "0" while EXEN2 = "1". This flag serves as the timer interrupt 2 request signal. If an interrupt is generated, EXF2 must be reset to "0" by software.
T2CON.7	TF2	Timer/counter 2 carry flag. This bit is set to "1" by a carry signal when timer/counter 2 is in 16-bit auto reload mode or in capture mode. This flag serves as the timer interrupt 2 request signal. If an interrupt is generated, TF2 must be reset to "0" by software.

MEMORY MAPS

Program Area



Internal Data Memory and Special Function Register Layout Diagram

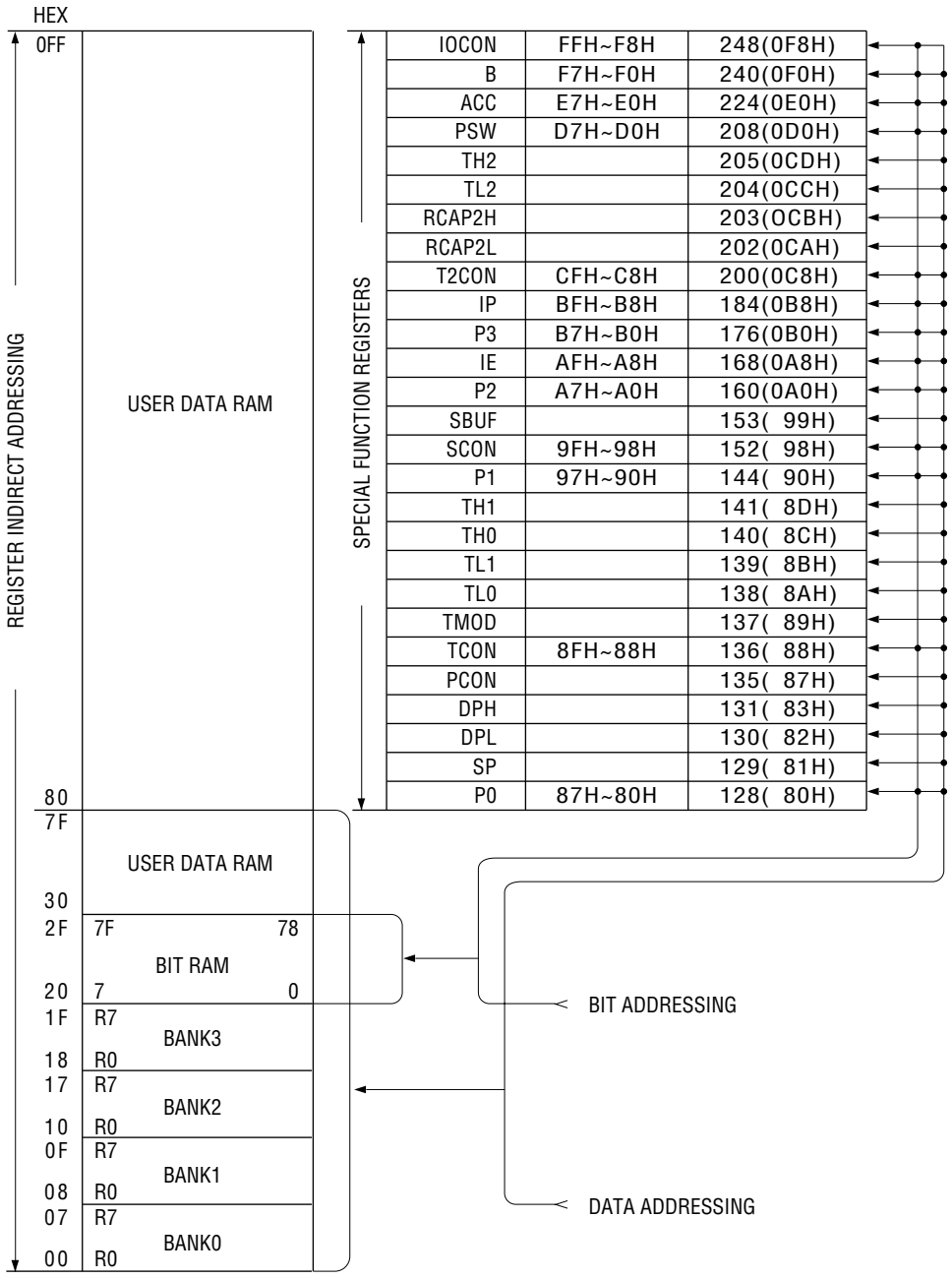
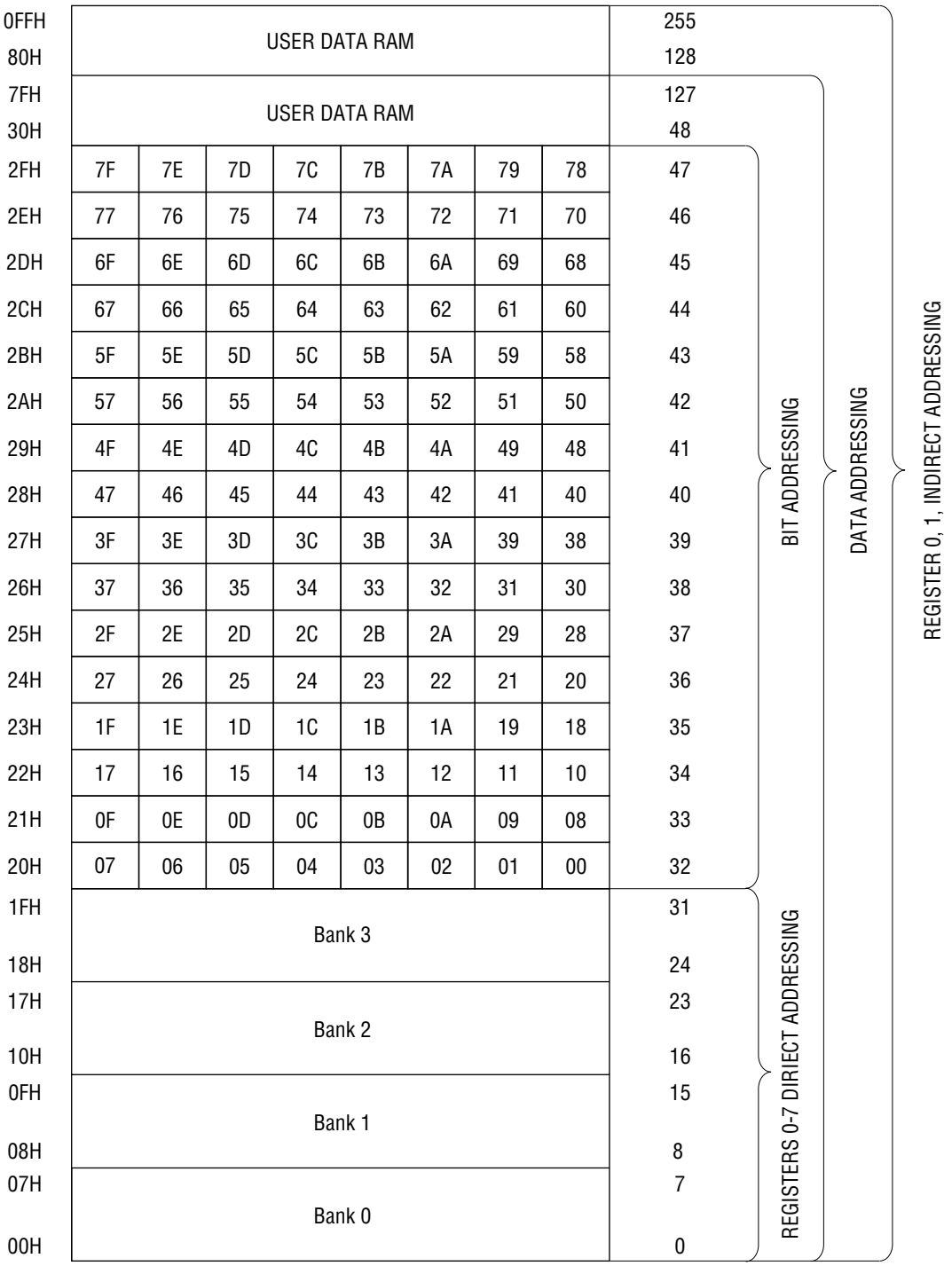


Diagram of Internal Data Memory (RAM)



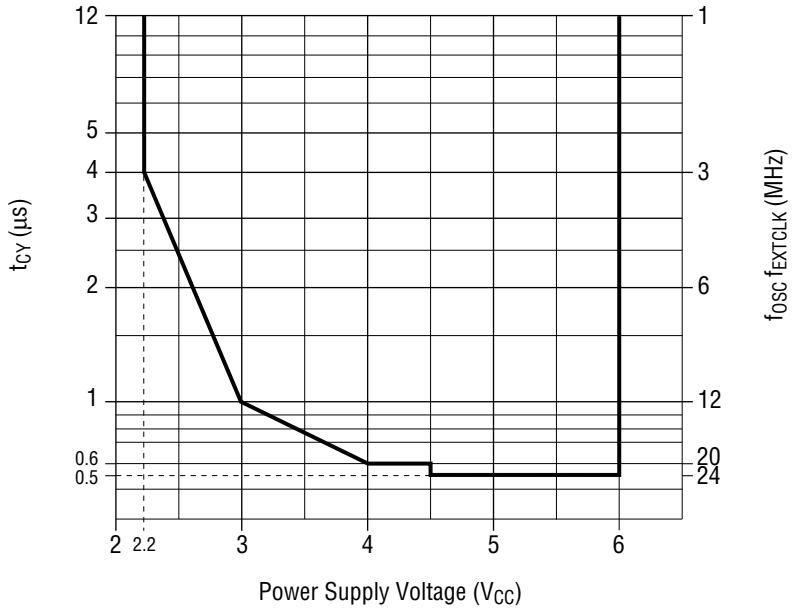
ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Rating	Unit
Supply voltage	V_{CC}	Ta=25°C	–0.5 to 7	V
Input voltage	V_I	Ta=25°C	–0.5 to V_{CC}+0.5	V
Storage temperature	T_{STG}	—	–55 to +150	°C

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Condition	Range	Unit
Power supply voltage	V_{CC}	See below	2.0 to 6.0	V
Memory retension voltage	V_{CC}	f_{OSC}=0 Hz (Oscillation stop)	2.0 to 6.0	V
Oxcillation frequency	f_{OSC}	See below	1 to 24	MHz
External clock operating frequency	f_{EXTCLK}	See below	0 to 24	MHz
Ambient temperature	Ta	—	–40 to +85	°C

*1 Depends on the specifications for the oscillator or ceramic resonater.



ELECTRICAL CHARACTERISTICS

DC Characteristics 1

(V_{CC}=4.0 to 6.0 V, V_{SS}=0 V, Ta=-40 to +85°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Measuring circuit
Input Low Voltage	V_{IL}	—	–0.5	—	0.2 V_{CC}–0.1	V	1
Input High Voltage	V_{IH}	Except XTAL1, $\overline{EA}$, and RESET	0.2 V_{CC}+0.9	—	V_{CC}+0.5	V	
Input High Voltage	V_{IH1}	XTAL1, RESET and $\overline{EA}$	0.7 V_{CC}	—	V_{CC}+0.5	V	
Output Low Voltage (PORT 1, 2, 3)	V_{OL}	I_{OL}=1.6 mA	—	—	0.45	V	
Output Low Voltage (PORT 0, ALE, $\overline{PSEN}$)	V_{OL1}	I_{OL}=3.2 mA	—	—	0.45	V	
Output High Voltage (PORT 1, 2, 3)	V_{OH}	I_{OH}=–60 µA V_{CC}=5 V±10%	2.4	—	—	V	
		I_{OH}=–30 µA	0.75 V_{CC}	—	—	V	
		I_{OH}=–10 µA	0.9 V_{CC}	—	—	V	
Output High Voltage (PORT 0, ALE, $\overline{PSEN}$)	V_{OH1}	I_{OH}=–400 µA V_{CC}=5 V±10%	2.4	—	—	V	
		I_{OH}=–150 µA	0.75 V_{CC}	—	—	V	
		I_{OH}=–40 µA	0.9 V_{CC}	—	—	V	
Logical 0 Input Current/ Logical 1 Output Current/ (PORT 1, 2, 3)	I_{IL} / I_{OH}	V_I=0.45 V / V_O=0.45 V	–5	–20	–80	µA	2
Logical 1 to 0 Transition Output Current (PORT 1, 2, 3)	I_{TL}	V_I=2.0 V	—	–190	–500	µA	
Input Leakage Current (PORT 0 floating, $\overline{EA}$)	I_{LI}	V_{SS} < V_I < V_{CC}	—	—	±10	µA	3
RESET Pull-down Resistance	R_{RST}	—	20	40	125	kΩ	2
Pin Capacitance	C_{IO}	Ta=25°C, f=1 MHz (except XTAL1)	—	—	10	pF	—
Power Down Current	I_{PD}	—	—	1	50	µA	4

Maximum power supply current normal operation I_{CC} (mA)

V_{CC}	4 V	5 V	6 V
Freq			
1 MHz	2.2	3.1	4.1
3 MHz	3.9	5.2	7.0
12 MHz	12.0	16.0	20.0
16 MHz	16.0	20.0	25.0
20 MHz	19.0	25.0	30.0

V_{CC}	4.5 V	5 V	6 V
Freq			
24 MHz	25.0	29.0	35.0

Maximum power supply current idle mode I_{CC} (mA)

V_{CC}	4 V	5 V	6 V
Freq			
1 MHz	0.8	1.2	1.6
3 MHz	1.2	1.7	2.3
12 MHz	3.1	4.4	5.9
16 MHz	3.8	5.5	7.3
20 MHz	4.5	6.4	8.6

V_{CC}	4.5 V	5 V	6 V
Freq			
24 MHz	6.4	7.4	9.8

DC Characteristics 2

(V_{CC}=2.2 to 4.0 V, V_{SS}=0 V, Ta=-40 to +85°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Measuring circuit
Input Low Voltage	V_{IL}	—	–0.5	—	0.25 V_{CC}–0.1	V	1
Input High Voltage	V_{IH}	Except XTAL1, $\overline{EA}$, and RESET	0.25 V_{CC}+0.9	—	V_{CC}+0.5	V	
Input High Voltage	V_{IH1}	XTAL1, RESET, and $\overline{EA}$	0.6 V_{CC}+0.6	—	V_{CC}+0.5	V	
Output Low Voltage (PORT 1, 2, 3)	V_{OL}	I_{OL}=10 µA	—	—	0.1	V	
Output Low Voltage (PORT 0, ALE, $\overline{PSEN}$)	V_{OL1}	I_{OL}=20 µA	—	—	0.1	V	
Output High Voltage Output High Voltage	V_{OH}	I_{OH}=–5 µA	0.75 V_{CC}	—	—	V	
(PORT 1, 2, 3) (PORT 0, ALE, $\overline{PSEN}$)	V_{OH1}	I_{OH}=–20 µA	0.75 V_{CC}	—	—	V	
Logical 0 Input Current/ Logical 1 Output Current/ (PORT 1, 2, 3)	I_{IL} / I_{OH}	V_I=0.1 V / V_O=0.1 V	–5	–10	–40	µA	2
Logical 1 to 0 Transition Output Current (PORT 1, 2, 3)	I_{TL}	V_I=1.9 V	—	–80	–300	µA	
Input Leakage Current (PORT 0 floating, $\overline{EA}$)	I_{LI}	V_{SS} < V_I < V_{CC}	—	—	±10	µA	3
RESET Pull-down Resistance	R_{RST}	—	20	40	125	kΩ	2
Pin Capacitance	C_{IO}	Ta=25°C, f=1 MHz (except XTAL1)	—	—	10	pF	—
Power Down Current	I_{PD}	—	—	1	10	µA	4

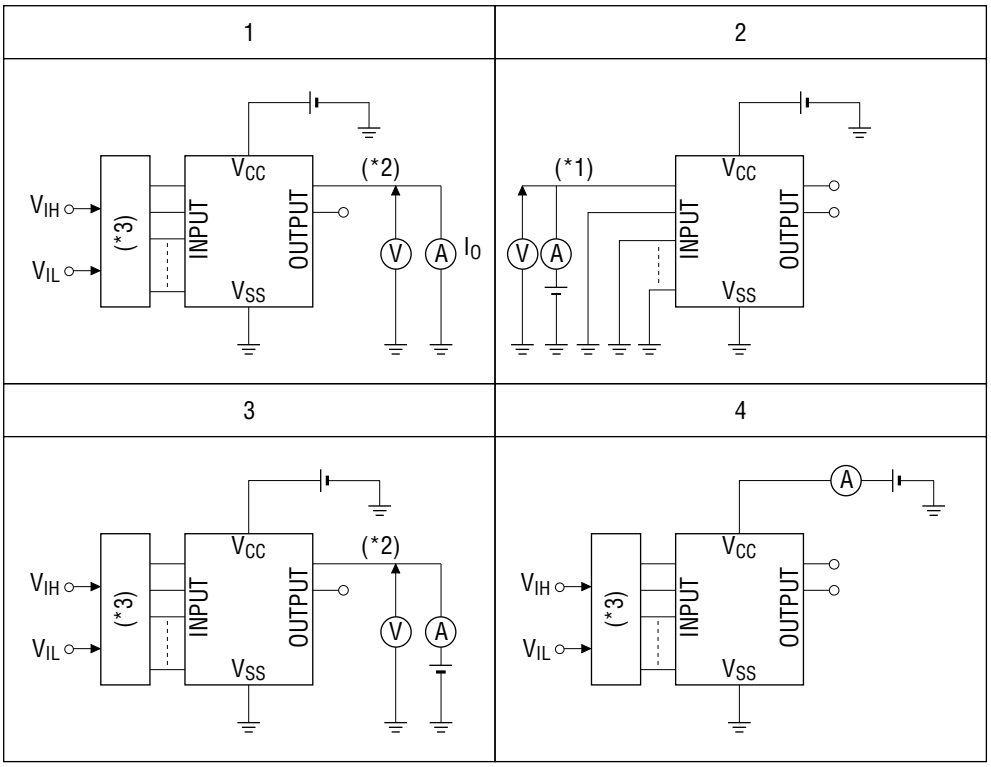
Maximum power supply current normal operation I_{CC} (mA)

V_{CC}	2.2 V	3.0 V	4.0 V
Freq			
1 MHz	0.9	1.4	2.2
3 MHz	1.8	2.4	4.3
12 MHz	—	8.0	12.0
16 MHz	—	—	16.0

Maximum power supply current idle mode I_{CC} (mA)

V_{CC}	2.2 V	3.0 V	4.0 V
Freq			
1 MHz	0.3	0.5	0.8
3 MHz	0.5	0.8	1.2
12 MHz	—	2.0	3.1
16 MHz	—	—	3.8

Measuring circuits



*1: Repeated for specified input pins.
*2: Repeated for specified output pins.
*3: Input logic for specified status.

AC Characteristics

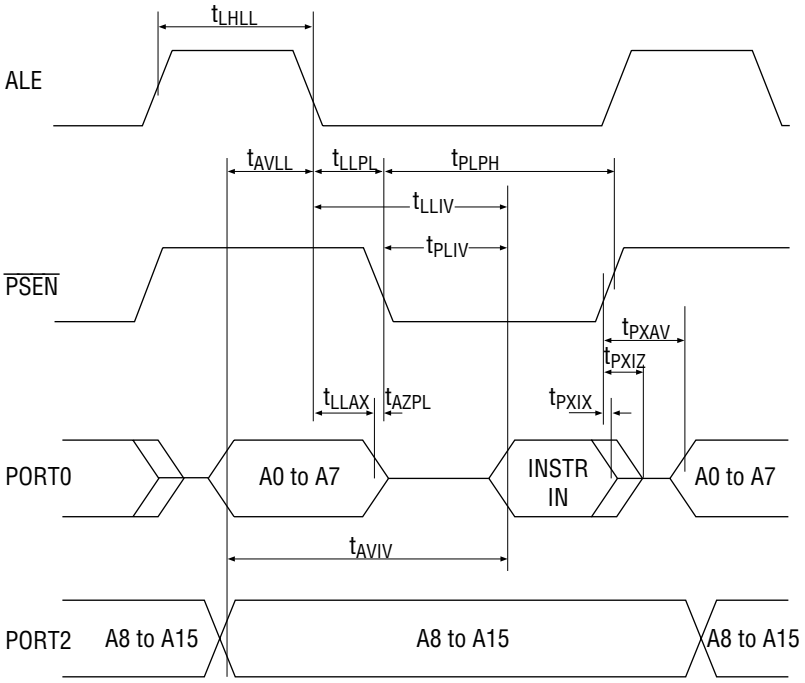
(1) External program memory access AC characteristics

(V_{CC}=2.2 to 6.0V, V_{SS}=0V, Ta=–40°C to +85°C
PORT 0, ALE, and $\overline{PSEN}$ connected with 100pF load, other connected with 80pF load)

Parameter	Symble	Variable clock from*1 1 to 24 MHz		Unit
		Min.	Max.	
XTAL1, XTAL 2 Oscillation Cycle	t_{CLCL}	41.7	1000	ns
ALE Signal Width	t_{LHLL}	$2t_{CLCL}$-40	—	ns
Address Setup Time (to ALE Falling Edge)	t_{AVLL}	$1t_{CLCL}$-15	—	ns
Address Hold Time (from ALE Falling Edge)	t_{LLAX}	$1t_{CLCL}$-35	—	ns
Instruction Data Read Time (from ALE Falling Edge)	t_{LLPL}	—	$4t_{CLCL}$-100	ns
From ALE Falling Edge to $\overline{PSEN}$ Falling Edge	t_{LLPL}	$1t_{CLCL}$-30	—	ns
$\overline{PSEN}$ Signal Width	t_{PLPH}	$3t_{CLCL}$-35	—	ns
Instruction Data Read Time (from $\overline{PSEN}$ Falling Edge)	t_{PLIV}	—	$3t_{CLCL}$-45	ns
Instruction Data Hold Time (from $\overline{PSEN}$ Rising Edge)	t_{PXIX}	0	—	ns
Bus Floating Time after Instruction Data Read (from $\overline{PSEN}$ Rising Edge)	t_{PXIZ}	—	$1t_{CLCL}$-20	ns
Instruction Data Read Time (from Address Output)	t_{AVIV}	—	$5t_{CLCL}$-105	ns
Bus Floating Time($\overline{PSEN}$ Rising Edge from Address float)	t_{AZPL}	0	—	ns
Address Output Time from $\overline{PSEN}$ Rising Edge	t_{PXAV}	$1t_{CLCL}$-20	—	ns

*1 The variable check is from 0 to 24 MHz when the external check is used.

(2) External program memory read cycle



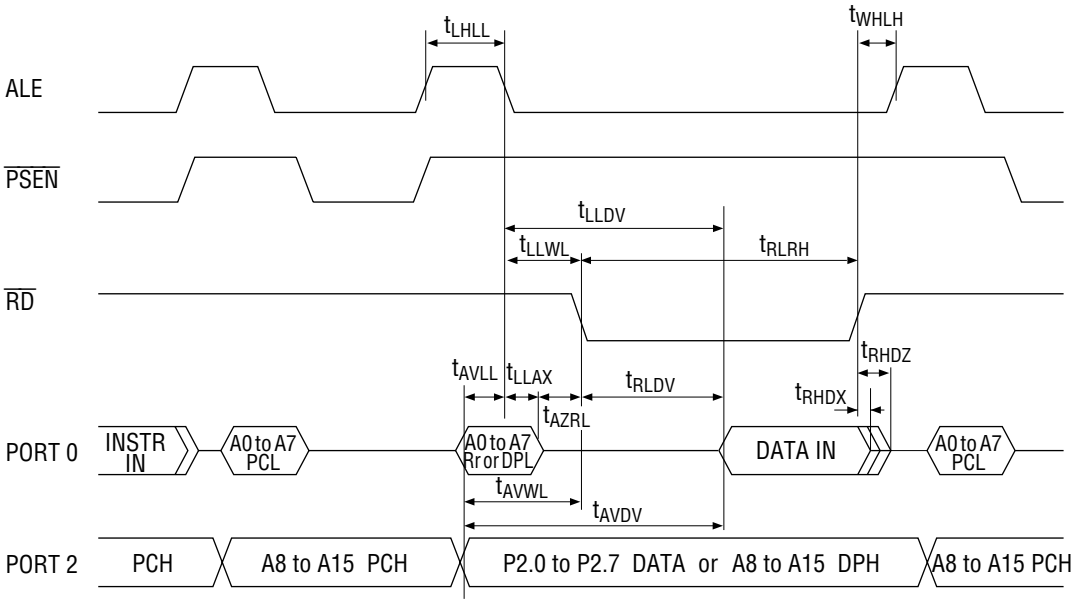
(3) External data memory access AC characteristics

(V_{CC}=2.2 to 6.0V, V_{SS}=0V, Ta=–40°C to +85°C
PORT 0, ALE, and $\overline{PSEN}$ connected with 100pF load, other connected with 80pF load)

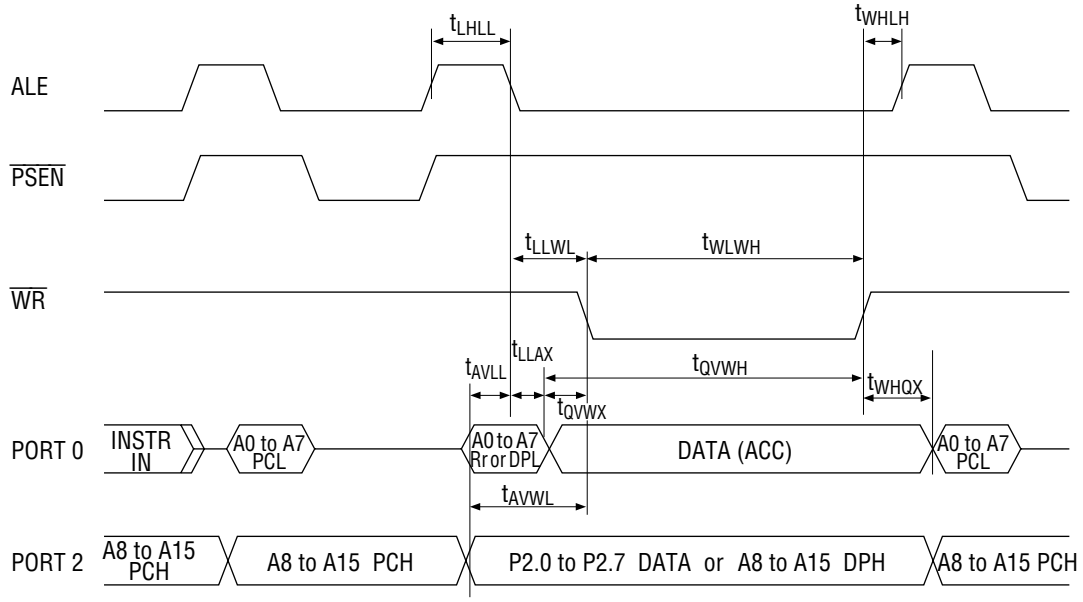
Parameter	Symbol	Variable clock from*1 1 to 24 MHz		Unit
		Min.	Max.	
XTAL1, XTAL2 Oscillator Cycle	t_{CLCL}	41.7	1000	ns
ALE Signal Width	t_{LHLL}	$2t_{CLCL}$-40	—	ns
Address Setup Time (to ALE Falling Edge)	t_{AVLL}	$1t_{CLCL}$-15	—	ns
Address Hold Time (from ALE Falling Edge)	t_{LLAX}	$1t_{CLCL}$-35	—	ns
$\overline{RD}$ Signal Width	t_{RLRL}	$6t_{CLCL}$-100	—	ns
$\overline{WR}$ Signal Width	t_{WLWH}	$6t_{CLCL}$-100	—	ns
RAM Data Read Time (from $\overline{RD}$ Signal Falling Edge)	t_{RLDV}	—	$5t_{CLCL}$-105	ns
RAM Data Read Hold Time (from $\overline{RD}$ Signal Rising Edge)	t_{RHDX}	0	—	ns
Data Bus Floating Time (from $\overline{RD}$ Signal Rising Edge)	t_{RHDZ}	—	$2t_{CLCL}$-70	ns
RAM Data Read Time (from ALE Signal Falling Edge)	t_{LLDV}	—	$8t_{CLCL}$-100	ns
RAM Data Read Time (from Address Output)	t_{AVDV}	—	$9t_{CLCL}$-105	ns
$\overline{RD}$/$\overline{WR}$ Output Time from ALE Falling Edge	t_{LLWL}	$3t_{CLCL}$-40 *2 $3t_{CLCL}$-100	$3t_{CLCL}$+40	ns
$\overline{RD}$/$\overline{WR}$ Output Time from Address Output	t_{AVWL}	$4t_{CLCL}$-70	—	ns
$\overline{WR}$ Output Time from Data Output	t_{QVWX}	$1t_{CLCL}$-40	—	ns
Time from Data to $\overline{WR}$ Rising Edge	t_{QVWH}	$7t_{CLCL}$-105	—	ns
Data Hold Time (from $\overline{WR}$ Rising Edge)	t_{WHQX}	$2t_{CLCL}$-50	—	ns
Time from to Address Float $\overline{RD}$ Output	t_{RLAZ}	0	—	ns
Time from $\overline{RD}$/$\overline{WR}$ Rising Edge to ALE Rising Edge	t_{WHLH}	$1t_{CLCL}$-30	$1t_{CLCL}$+40 *2 $1t_{CLCL}$+100	ns

*1 The variable check is from 0 to 24 MHz when the external check is used.
*2 For 2.2≤V_{CC}<4 V

(4) External data memory read cycle



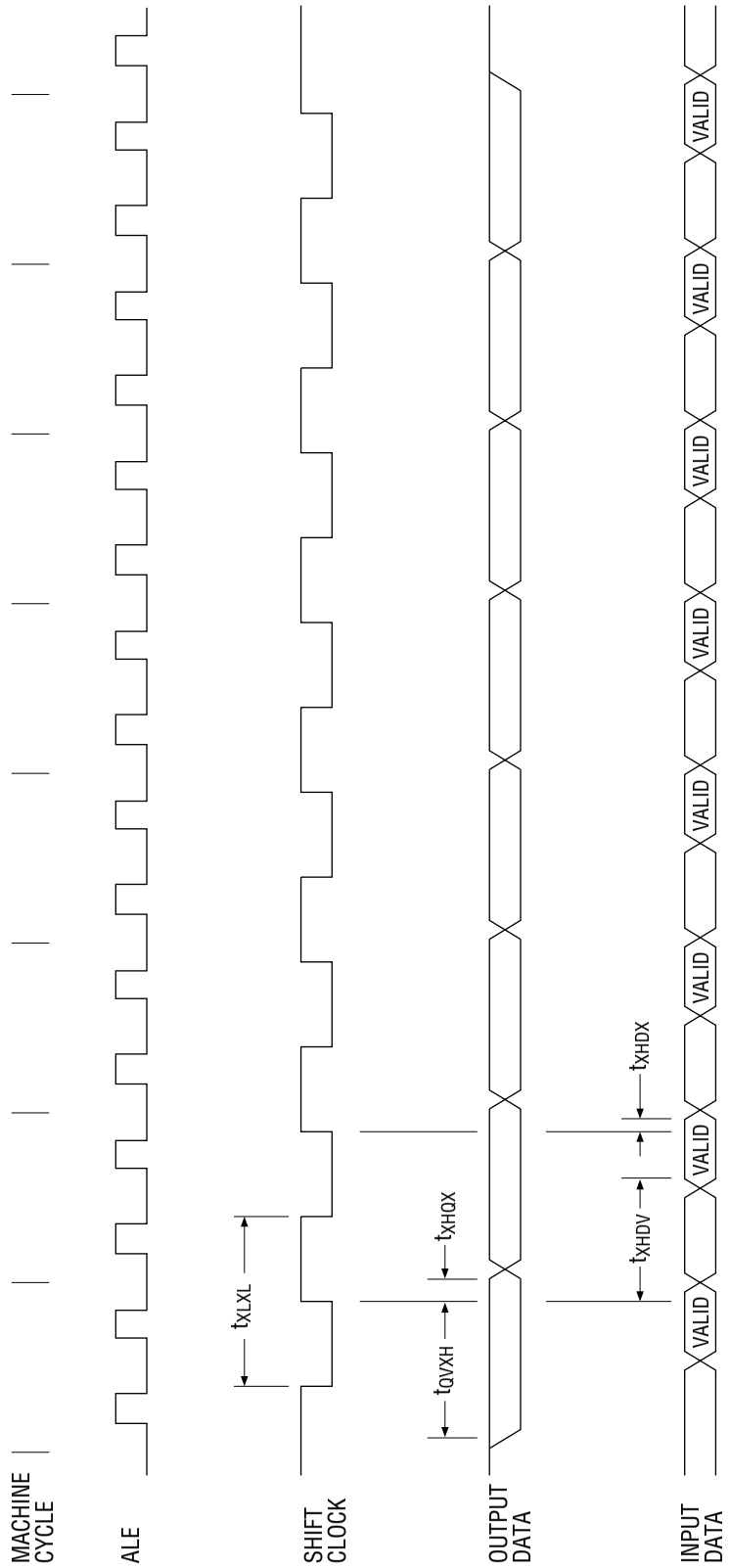
(5) External data memory write cycle



(6) Serial port (I/O Extension Mode) AC characteristics

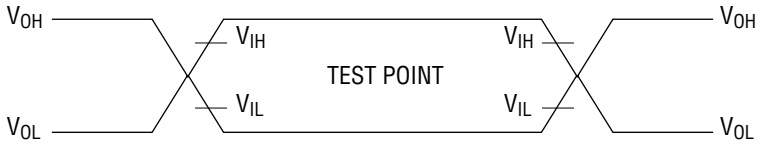
(V_{CC}=2.2 to 6.0V, V_{SS}=0V, Ta=–40°C to +85°C)

Parameter	Symbol	Min.	Max.	Unit
Serial Port Clock Cycle Time	t_{XLXL}	$12t_{CLCL}$	—	ns
Output Data Setup to Clock Rising Edge	t_{QVXH}	$10t_{CLCL}$-133	—	ns
Output Data Hold After Clock Rising Edge	t_{XHQX}	$2t_{CLCL}$-75	—	ns
Input Data Hold After Clock Rising Edge	t_{XHDX}	0	—	ns
Clock Rising Edge to Input Data Valid	t_{XHDV}	—	$10t_{CLCL}$-133	ns



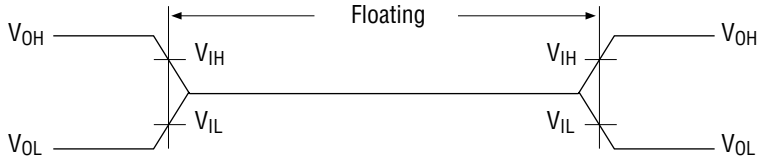
(7) AC Characteristics Measuring Conditions

1. Input/output signal



* The input signals in AC test mode are either V_{OH} (logic "1") or V_{OL} (logic "0") input signals where logic "1" corresponds to a CPU output signal waveform measuring point in excess of V_{IH}, and logic "0" to a point below V_{IL}.

2. Floating

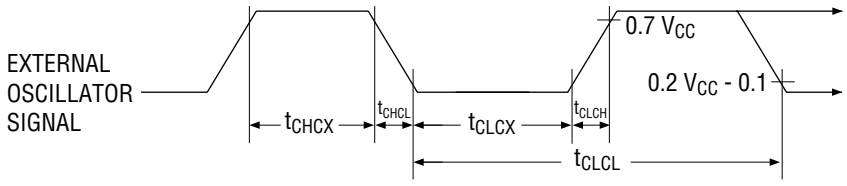


* The port 0 floating interval is measured from the time the port 0 pin voltage drops below V_{IH} after sinking to GND at 2.4 mA when switching to floating status from a "1" output, and from the time the port 0 pin voltage exceeds V_{IL} after connecting to a 400 µA source when switching to floating status from a "0" output.

(8) XTAL1 external clock input waveform conditions

Parameter	Symbol	Min.	Max.	Unit
External Clock Freq.	$1/t_{CLCL}$	0	24	MHz
Clock Pulse width 1	t_{CHCx}	15	—	ns
Clock Pulse width 2	t_{CLCX}	15	—	ns
Rise Time	t_{CLCH}	—	5	ns
Fall Time	t_{CHCL}	—	5	ns

External Clock Drive Waveform



Timing Diagram

Basic timing