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MICROCOMPUTER MN101C

MN101C77C/F77G
LSI User's Manual

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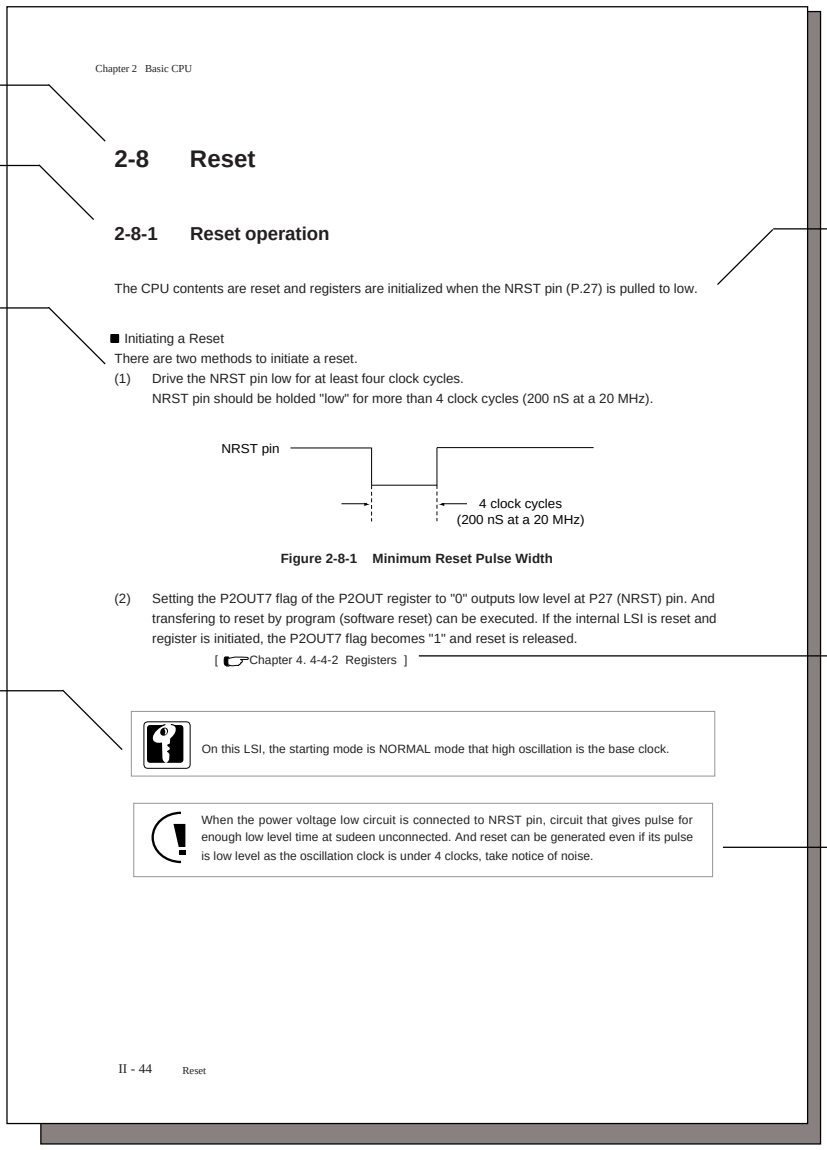
About This Manual

■Organization

In this LSI manual, this LSI functions are presented in the following order : overview, basic CPU functions, interrupt functions, port functions, timer functions, serial functions, and other peripheral hardware functions.
Each section contains overview of function, block diagram, control register, operation, and setting example.

■Manual Configuration

Each section of this manual consists of a title, summary, main text, key information, precautions and warnings, and references.
The layout and definition of each section are shown below.



Subtitle

Sub-subtitle
The smallest block in this manual.

Main text

Key information
Important information from the text.

Summary
Introduction to the section.

References
References for the main text.

Precautions and warnings
Precautions are listed in case.
Be sure to read these of lost functionality or damage.

■Finding Desired Information

This manual provides three methods for finding desired information quickly and easily.

(1) Consult the index at the front of the manual to locate the beginning of each section.
(2) Consult the table of contents at the front of the manual to locate desired titles.
(3) Chapter names are located at the top outer corner of each page, and section titles are located at the bottom outer corner of each page.

■Related Manuals

Note that the following related documents are available.

"MN101C Series LSI user's Manual"
<Describes the device hardware>
"MN101C Series Instruction Manual"
<Describes the instruction set.>
"MN101C Series C Compiler User's Manual: Usage Guide"
<Describes the installation, the commands, and options of the C Compiler.>
"MN101C Series C Compiler User's Manual: Language Description"
<Describes the syntax of the C Compiler.>
"MN101C Series C Compiler User's Manual: Library Reference"
<Describes the standard library of the C Compiler.>
"MN101C Series Cross-assembler User's Manual"
<Describes the assembler syntax and notation.>
"MN101C Series C Source Code Debugger User's Manual"
<Describes the use of C source code debugger.>
"MN101C Series PanaX Series Installation Manual"
<Describes the installation of C compiler, cross-assembler and C source code debugger and the procedure for bringing up the in-circuit emulator.>

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Chapter 1 Overview

1-1 Overview

1-1-1 Overview

The MN101C series of 8-bit single-chip microcontroller incorporates multiple types of peripheral functions. This chip series is well suited for camera, VCR, MD, TV, CD, LD, printer, telephone, home automation products, pager, air conditioner, PPC remote control, fax machine, musical instrument, and other applications.

The MN101C77 series brings to embedded microcontroller applications flexible, optimized hardware configurations and a simple efficient instruction set. The MN101C77C has an internal 48 KB of ROM and 3 KB of RAM. Peripheral functions include 5 external interrupts, 17 internal interrupts including NMI, independent 6 timer counters, 4 sets of serial interfaces, A/D converter, D/A converter, watchdog timer, automatic data transfer, synchronous output, buzzer output, and remote control output. The configuration of this microcontroller is well suited for application such as a system controller in a camera, VCR selection timer, CD player, or MD.

With two oscillation systems (max.20 MHz/32 kHz) contained on the chip, the system clock can be switched to high speed oscillation (**NORMAL mode**), or to low speed oscillation (**SLOW mode**). The system clock is generated by dividing the oscillation clock. The best operation clock for the system can be selected by switching its frequency by software. There are 2 choices for high speed oscillation : the normal mode, which has a system clock based on the clock (fosc/2) divided by 2, and the 2x-speed mode, which has a system clock based on the same cycle clock (fosc).

On the normal mode, when the oscillation source(fosc) is 8 MHz, **minimum instructions execution time** is for 250 ns, and when fosc is 20 MHz, it is 100 ns. On the 2x-speed mode, CPU is operated with the same cycle to the external clock, when fosc is 8 MHz, minimum instructions execution time is 125 ns. The packages are 64-pin LQFP and 64-pin TQFP (under development).

1-1-2 Product Summary

This manual describes the following models of the MN101C77 series. These products have same peripheral functions. (Refer to chapter 18 Flash EEPROM for Flash version.)

Table 1-1-1 Product Summary

Model	ROM Size	RAM Size	Classification
MN101C77C	48 KB	3 KB	Mask ROM version
MN101CF77G	128 KB	6 KB	Flash EEPROM version

1-2 Hardware Functions

CPU Core **MN101C Core**

- LOAD-STORE architecture (3-stage pipeline)
- Half-byte instruction set / Handy addressing
- Memory addressing space is 256 KB
- Minimum instructions execution time (3.0 V to 3.6 V for Flash version)

High speed oscillation

[normal]	0.10 µs	/	20 MHz	(2.5 V to 3.6 V)
	0.20 µs	/	10 MHz	(2.1 V to 3.6 V)
	0.50 µs	/	4 MHz	(1.8 V to 3.6 V)
[2x-speed]	0.119 µs	/	8.39 MHz	(2.5 V to 3.6 V)
Low speed oscillation	61.04 µs	/	32.768 kHz	(1.8 V to 3.6 V)

- Operation modes

NORMAL mode (High speed oscillation)
SLOW mode (Low speed oscillation)
HALT mode
STOP mode
(The operation clock can be switched in each mode.)

Memory bank Data memory space expansion by bank form (4 banks unit : 64 KB / 1 bank)

- Bank for source address / Bank for destination address

ROM correction Max.3 parts in program can be corrected

Internal memory **ROM 48 KB (Flash version 128 KB)**
RAM 3 KB (Flash version 6 KB)

Interrupts **17 Internal interrupts**

<Non-maskable interrupt (NMI)>
- Incorrect code execution interrupt and Watchdog timer interrupt

< Timer interrupts >
- Timer 0 interrupt (8-bit timer)
- Timer 1 interrupt (8-bit timer)
- Timer 4 interrupt (8-bit timer)
- Timer 5 interrupt (8-bit timer)
- Timer 6 interrupt (8-bit timer)
- Time base interrupt (8-bit timer)
- Timer 7 interrupt (16-bit timer)
- Match interrupt for Timer 7 compare register 2

< Serial interface interrupts >
- Serial interface 0 reception interrupt (Full-Duplex UART)
- Serial interface 0 transmission interrupt (synchronous + Full-Duplex UART)
- Serial interface 1 reception interrupt (Full-Duplex UART)
- Serial interface 1 transmission interrupt (synchronous + Full-Duplex UART)
- Serial interface 3 interrupt (synchronous + single master IIC)
- Serial interface 4 interrupt (slave IIC)

< A/D interrupt >
- A/D converter interrupt

< Automatic transfer controller(ATC) interrupt >
- ATC 1 interrupt

5 External interrupts (with/without noise filter)
- IRQ0 : Edge selectable. Both edges interrupt.
- IRQ1 : Edge selectable. Both edges interrupt. AC zero cross detector.
- IRQ2 : Edge selectable. Both edges interrupt.
- IRQ3 : Edge selectable. Both edges interrupt.
- IRQ4 : Edge selectable. Both edges interrupt. Key interrupt function.

Timers

7 timers (6 can operate independently)

- 8-Bit timer for general use	2 sets
- 8-Bit timer for general use (UART baud rate timer)	2 sets
- 8-Bit free-running timer	1 set
Time base timer	1 set
- 16-Bit timer for general use	1 set

Timer 0 (8-Bit timer for general use)
- Square wave output (Timer pulse output), PWM output, Event count, Remote control carrier output, Simple pulse width measurement
- Clock source
  fosc, fosc/4, fosc/16, fosc/32, fosc/64, fs/2, fs/4, fx, external clock

Timer 1 (8-Bit timer for general use)
- Square wave output (Timer pulse output), Event count, 16-Bit cascade connection function (connected to timer 0), Timer synchronous output
- Clock source
  fosc, fosc/4, fosc/16, fosc/64, fosc/128, fs/2, fs/8, fx, external clock

Timer 4 (8-Bit timer for general use or UART baud rate timer)

- Square wave output (Timer pulse output), PWM output, Event count
  Simple pulse width measurement, Serial interface transfer clock
- Clock source
  fosc, fosc/4, fosc/16, fosc/32, fosc/64, fs/2, fs/4, fx, external clock

Timer 5 (8-Bit timer for general use or UART baud rate timer)

- Square wave output (Timer pulse output), PWM output, Event count,
  Remote control carrier output, Simple pulse width measurement,
  Serial interface transfer clock
- Clock source
  fosc, fosc/4, fosc/16, fosc/32, fosc/64, fs/2, fs/4, fx, external clock

Timer 6 (8-Bit free-running timer, Time base timer)

❑ **8-Bit free-running timer**

- Clock source
  fosc, fosc/2^{12}, fosc/2^{13}, fs, fx, fx/2^{12}, fx/2^{13}

❑ **Time base timer**

- Interrupt generation cycle
  fosc/2^{7}, fosc/2^{8}, fosc/2^{9}, fosc/2^{10}, fosc/2^{13}, fosc/2^{15},
  fx/2^{7}, fx/2^{8}, fx/2^{9}, fx/2^{10}, fx/2^{13}, fx/2^{15}

Timer 7 (16-Bit timer for general use)

- Clock source
  fosc, fosc/2, fosc/4, fosc/16, fs, fs/2, fs/4, fs/16,
  1/1, 1/2, 1/4, 1/16 of the external clock
- Hardware organization

Compare register with double buffer	2 sets
Input capture register	1 set
Timer interrupt	2 vectors

- Timer functions
  Square wave output (Timer pulse output), Event count,
  High precision PWM output (Cycle/Duty variable continuously),
  Timer synchronous output, Input capture function (Both edges
  can be operated)
- Real time output control
  PWM output is controlled in real time by the external interrupt 0 (IRQ0).
  At the interrupt enable edge of the external interrupt 0 (IRQ0), PWM output
  (Timer output) is controlled in 3 values ; "fixed high", "fixed low",
  "Hi-z".

Watchdog timer

- Watchdog timer frequency can be selected from $fs/2^{16}$, $fs/2^{18}$ or $fs/2^{20}$.

Remote control output

Based on the timer 0, and timer 3 output, a remote control carrier with duty cycle of 1/2 or 1/3 can be output.

Synchronous output

Timer synchronous output, Interrupt synchronous output

- Port 6 outputs the latched data, on the event timing of the synchronous output signal of timer 1, 5, or 7, or of the external interrupt 2 (IRQ 2).

Buzzer output Output frequency can be selected from $fosc/2^9$, $fosc/2^{10}$, $fosc/2^{11}$, $fosc/2^{12}$, $fosc/2^{13}$, $fosc/2^{14}$, $fx/2^3$, $fx/2^4$.

Automatic transfer controller (ATC)

Data in the whole memory space (256 KB) can be transferred.

- External interrupt start / internal event start / software start
- Max. 255 bytes continuous transfer
- Support serial interface sequence transmission / reception
- Burst transfer (interrupt shutdown is built-in)

A/D converter **10 bits X 7 channels input**

D/A converter **8 bits X 2 channels input**

Serial interface **4 types**

Serial interface 0 (Full-Duplex UART / Synchronous serial interface)

❑ **Synchronous serial interface**

- Transfer clock source
  fosc/2, fosc/4, fosx/16, fosc/64, fs/2, fs/4
  1/2 of UART baud rate timer (timer 5) output
- MSB/LSB can be selected as the first bit to be transferred. Any transfer size from 1 to 8 bits can be selected.
- Sequence transmission, sequence reception or both are available.

❑ **Full-Duplex UART (Baud rate timer : Timer 5)**

- Parity check, Overrun error, Framing error detection
- Transfer size 7 to 8 bits can be selected.

[Note : When Matsushita standard serial writer is used for flash memory version, serial interface 0 is used for program transfer.]

Serial interface 1 (Full-Duplex UART / Synchronous serial interface)

❑ **Synchronous serial interface**

- Transfer clock source
  fosc/2, fosc/4, fosx/16, fosc/64, fs/2, fs/4
  1/2 of UART baud rate timer (timer 4) output
- MSB/LSB can be selected as the first bit to be transferred. Any transfer size 1 to 8 bits can be selected.
- Sequence transmission, sequence reception or both are available.

❑ **Full-Duplex UART (Baud rate timer : Timer 4)**

- Parity check, Overrun error, Framing error detection
- Transfer size 7 to 8 bits can be selected.

Serial interface 3 (Single master IIC / Synchronous serial interface)

❑ **Synchronous serial interface**

- Transfer clock source
  fosc/2, fosc/4, fosc/16, fosc/32, fs/2, fs/4, 1/2 of timer 5 output
- MSB/LSB can be selected as the first bit to be transferred. Any transfer size 1 to 8 bits can be selected.
- Sequence transmission, sequence reception or both are available.

❑ **Single master IIC**

- IIC communication for single master (9-bit transfer)

Serial interface 4 (Slave IIC)

❑ **IIC slave serial interface**

- IIC high-speed transfer mode (400 kbps) is available.
- 7 bits or 10 bits slave address setting is available.
- Compatible with general call communication mode

LED driver **8 pins**

Port		
	I/O ports	**53 pins**
	- LED (large current) driver pin	8 pins
	- Serves as external interrupt	5 pins
	Special pins	**10 pins**
	- Analog reference voltage input pin	2 pins
	- Operation mode input pin	1 pin
	- Reset input pin	1 pin
	- Power pin	2 pins
	- Oscillation pin	4 pins

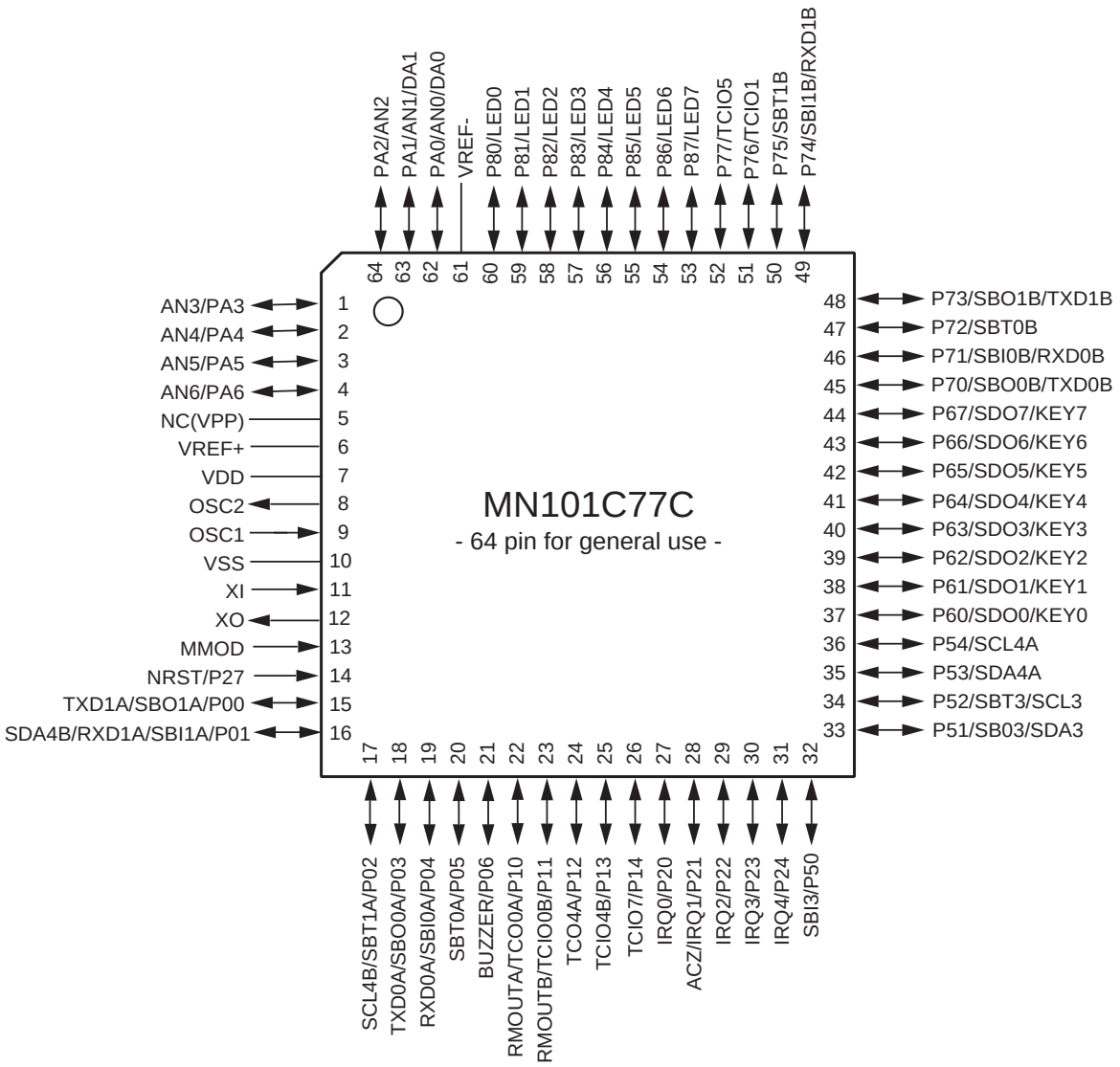
Package **64-pin LQFP (14 mm square / 0.8 mm pitch)**
64-pin TQFP (10 mm square / 0.5 mm pitch)

On Flash version MN101CF77G, NC pin cannot be used as user pin as it is used as V_{PP} pin. Refer to chapter 18 Flash EEPROM when designing your board for compatibility with Flash version.

Set V_{REF}+ to V_{DD}, V_{REF}- to V_{SS} even when A/D converter is not used.

1-3 Pin Description

1-3-1 Pin Configuration



On Flash version of MN101CF77G, NC pin is VPP.

Figure 1-3-1 Pin Configuration (64 LQFP/64TQFP : Top view)

1-3-2 Pin Specification

Table 1-3-2 Pin Specification

Pin	Function		Input/output	Direction control	Pin control	Descreption	
P00	SBO1A	TXD1A	in/out	P0DIR0	P0PLU0	SBO1A : Serial Interface 1 transmission data output	TXD1A : UART 1 transmission data output
P01	SBI1A	RXD1A	in/out	P0DIR1	P0PLU1	SBI1A : Serial Interface 1 reception data input	RXD1A : UART 1 reception data output
	SDA4B					SDA4B : Serial Interface 4 data I/O	
P02	SBT1A	SCL4B	in/out	P0DIR2	P0PLU2	SBT1A : Serial 1 clock I/O	SCL4B : Serial Interface 4 clock I/O
P03	SBO0A	TXD0A	in/out	P0DIR3	P0PLU3	SBO0A : Serial 0 transmission data output	TXD0A : UART 0 transmission data output
P04	SBI0A	RXD0A	in/out	P0DIR4	P0PLU4	SBI0A : Serial 0 reception data input	RXD0A : UART 0 reception data input
P05	SBT0A		in/out	P0DIR5	P0PLU5	SBT0A : Serial 0 clock I/O	
P06	BUZZER		in/out	P0DIR6	P0PLU6	BUZZER : Buzzer output	
P10	TCO0A	RMOUTA	in/out	P1DIR0	P1PLU0	TCIO0A : Timer 0 output	RMOUTA : Remote control carrier output
P11	TCIO0B	RMOUTB	in/out	P1DIR1	P1PLU1	TCIOOB : Timer 0 I/O	RMOUTB : Remote control carrier output
P12	TCO4A		in/out	P1DIR2	P1PLU2	TCIO4A : Timer 4 I/O	
P13	TCIO4B		in/out	P1DIR3	P1PLU3	TCIO4B : Timer 4 I/O	
P14	TCIO7		in/out	P1DIR4	P1PLU4	TCIO7 : Timer 7 I/O	
P20	IRQ0		in/out	P2DIR0	P2PLU0	IRQ0 : External interrupt 0	
P21	IRQ1	ACZ	in/out	P2DIR1	P2PLU1	IRQ1 : External interrupt 1	ACZ : AC zero bolt detection input
P22	IRQ2		in/out	P2DIR2	P2PLU2	IRQ2 : External interrupt 2	
P23	IRQ3		in/out	P2DIR3	P2PLU3	IRQ3 : External interrupt 3	
P24	IRQ4		in/out	P2DIR4	P2PLU4	IRQ4 : External interrupt 4	
P27	NRST		in/out	-	-	NRST : Reset	
P50	SBI3		in/out	P5DIR0	P5PLU0	SBO3 : Serial 3 reception data output	
P51	SBO3	SDA3	in/out	P5DIR1	P5PLU1	SBI3 : Serial interface 3 ransmission data input	SDA3 : Serial Interface 3 data I/O
P52	SBT3	SCL3	in/out	P5DIR2	P5PLU2	SBT3 : Serial interface 3 clock I/O	SCL3 : Serial Interface 3 clock I/O
P53	SDA4A		in/out	P5DIR3	P5PLU3	SDA4A : Serial interface 4 data I/O	
P54	SCL4A		in/out	P5DIR4	P5PLU4	SCL4A : Serial interface 4 clock I/O	
P60	SDO0	KEY0	in/out	P6DIR0	P6PLU0	SDO0 : Timer synchronous output 0	KEY0 : KEY interrupt input 0
P61	SDO1	KEY1	in/out	P6DIR1	P6PLU1	SDO1 : Timer synchronous output 1	KEY1 : KEY interrupt input 1
P62	SDO2	KEY2	in/out	P6DIR2	P6PLU2	SDO2 : Timer synchronous output 2	KEY2 : KEY interrupt input 2
P63	SDO3	KEY3	in/out	P6DIR3	P6PLU3	SDO3 : Timer synchronous output 3	KEY3 : KEY interrupt input 3
P64	SDO4	KEY4	in/out	P6DIR4	P6PLU4	SDO4 : Timer synchronous output 4	KEY4 : KEY interrupt input 4
P65	SDO5	KEY5	in/out	P6DIR5	P6PLU5	SDO5 : Timer synchronous output 5	KEY5 : KEY interrupt input 5
P66	SDO6	KEY6	in/out	P6DIR6	P6PLU6	SDO6 : Timer synchronous output 6	KEY6 : KEY interrupt input 6
P67	SDO7	KEY7	in/out	P6DIR7	P6PLU7	SDO7 : Timer synchronous output 7	KEY7 : KEY interrupt input 7
P70	SBO0B	TXD0B	in/out	P7DIR0	P7PLUD0	SBO0B : Serial interface 0 transmission data output	TXD0B : UART 0 transmission data output
P71	SBI0B	RXD0B	in/out	P7DIR1	P7PLUD1	SBI0B : Serial interface 0 reception data input	RXD0B : UART 0 reception data output
P72	SBT0B		in/out	P7DIR2	P7PLUD2	SBT0B : Serial interface 0 clock I/O	
P73	SBO1B	TXD1B	in/out	P7DIR3	P7PLUD3	SBO1B : Serial interface 1 transmission data output	TXD1B : UART 1 transmission data output
P74	SBI1B	RXD1B	in/out	P7DIR4	P7PLUD4	SBI1B : Serial interface 1 reception data input	RXD1B : UART 1 reception data output
P75	SBT1B		in/out	P7DIR5	P7PLUD5	SBT1B : Serial interface 1 clock I/O	
P76	TCIO1		in/out	P7DIR6	P7PLUD6	TCIO1 : Timer 1 I/O	
P77	TCIO5		in/out	P7DIR7	P7PLUD7	TCIO5 : Timer 5 I/O	
P80	LED0		in/out	P8DIR0	P8PLU0	LED0 : LED driving pin 0	
P81	LED1		in/out	P8DIR1	P8PLU1	LED1 : LED driving pin 1	
P82	LED2		in/out	P8DIR2	P8PLU2	LED2 : LED driving pin 2	
P83	LED3		in/out	P8DIR3	P8PLU3	LED3 : LED driving pin 3	
P84	LED4		in/out	P8DIR4	P8PLU4	LED4 : LED driving pin 4	
P85	LED5		in/out	P8DIR5	P8PLU5	LED5 : LED driving pin 5	
P86	LED6		in/out	P8DIR6	P8PLU6	LED6 : LED driving pin 6	
P87	LED7		in/out	P8DIR7	P8PLU7	LED7 : LED driving pin 7	
PA0	AN0	DA0	in/out	PADIR0	PAPLUD0	AN0 : Analog 0 input	DA0 : DA0 output
PA1	AN1	DA1	in/out	PADIR1	PAPLUD1	AN1 : Analog 1 input	DA1 : DA1 output
PA2	AN2		in/out	PADIR2	PAPLUD2	AN2 : Analog 2 input	
PA3	AN3		in/out	PADIR3	PAPLUD3	AN3 : Analog 3 input	
PA4	AN4		in/out	PADIR4	PAPLUD4	AN4 : Analog 4 input	
PA5	AN5		in/out	PADIR5	PAPLUD5	AN5 : Analog 5 input	
PA6	AN6		in/out	PADIR6	PAPLUD6	AN6 : Analog 6 input	

1-3-3 Pin Functions

Table 1-3-3 Pin Function Summary (1/6)

Name	No.	I/O	Function	Other Function	Description
VDD VSS	7 10		Power supply pin		Supply 1.8 V to 3.6 V to VDD and 0 V to VSS.
OSC1 OSC2	9 8	Input Output	Clock input pin Clock output pin		Connect these oscillation pins to ceramic or crystal oscillators for high-frequency clock operation. If the clock is an external input, connect it to OSC1 and leave OSC2 open. The chip will not operate with an external clock when using either the STOP or SLOW modes.
XI XO	11 12	Input Output	Clock input pin Clock output pin		Connect these oscillation pins to ceramic oscillators or crystal oscillators for low-frequency clock operation. If the clock is an external input, connect it to XI and leave XO open. The chip will not operate with an external clock when using the STOP mode. If these pins are not used, connect XI to VSS and leave XO open.
NRST	14	I/O	Reset pin	P27	This pin resets the chip when power is turned on, is allocated as P27 and contains an internal pull-up resistor. Setting this pin low initializes the internal state of the device. Thereafter, setting the input to high releases the reset. The hardware waits for the system clock to stabilize, then processes the reset interrupt. Also, if ""0"" is written to P27 and the reset is initiated by software, a low level will be output. The output has an n-channel open-drain configuration. If a capacitor is to be inserted between NRST and VDD, it is recommended that a discharge diode be placed between NRST and VDD.
P00 P01 P02 P03 P04 P05 P06	15 16 17 18 19 20 21	I/O	I/O port 0	SBO1A, TXD1A SBI1A, RXD1A SDA4B SBT1A, SCL4B SBO0A, TXD0A SBI0A, RXD0A SBT0A BUZZER	7-Bit CMOS tri-state I/O port. Each bit can be set individually as either an input or output by the P0DIR register. A pull-up resistor for each bit can be selected individually by the P0PLU register. At reset, the input mode is selected and pull-up resistors are disabled (high impedance output).
P10 P11 P12 P13 P14	22 23 24 25 26	I/O	I/O port 1	TCO0A, RMOUTA TCIO0B, RMOUTB TCO4A TCIO4B TCI07	5-Bit CMOS tri-state I/O port. Each bit can be set individually as either an input or output by the P1DIR register. A pull-up resistor for each bit can be selected individually by the P1PLU register. At reset, the input mode is selected and pull-up resistors are disabled (high impedance output).

Table 1-3-4 Pin Function Summary (2/6)

Name	No.	I/O	Function	Other Function	Description
P20	27	I/O	I/O port 2	IRQ0	5-Bit CMOS tri-state I/O port. A pull-up resistor for each bit can be selected individually by the P2PLU register. At reset, pull-up resistors are disabled (high impedance output).
P21	28			IRQ1, ACZ	
P22	29			IRQ2	
P23	30			IRQ3	
P24	31			IRQ4	
P27	14	Input	I/O port 2	NRST	P27 has an n-channel open-drain configuration. When "0" is written and the reset is initiated by software, a low level will be output.
P50	32	I/O	I/O port 5	SBI3	5-Bit CMOS tri-state I/O port. Each bit can be set individually as either an input or output by the P5DIR register. A pull-up resistor for each bit can be selected individually by the P5PLU register. At reset, the P50t o P54 input mode is selected and pull- up resistors are disabled. (high impedance output)
P51	33			SBO3,	
P52	34			SBT3	
P53	35			SDA4A	
P54	36			SCL4A	
P60	37	I/O	I/O port 6	SDO0, KEY0	8-Bit CMOS tri-state I/O port. Each bit can be set individually as either an input or output by the P6DIR register. A pull-up resistor for each bit can be selected individually by the P6PLU register. At reset, the P60 to P67 input mode is selected and pull- up resistors are disabled. (high impedance output)
P61	38			SDO1, KEY1	
P62	39			SDO2, KEY2	
P63	40			SDO3, KEY3	
P64	41			SDO4, KEY4	
P65	42			SDO5, KEY5	
P66	43			SDO6, KEY6	
P67	44			SDO7, KEY7	
P70	45	I/O	I/O port 7	SBO0B, TXD0B	8-Bit CMOS tri-state I/O port. Each bit can be set individually as either an input or output by the P7DIR register. A pull-up/pull-down resistor for each bit can be selected individually by the P7PLU register. However, pull-up and pull-down resistors cannot be mixed. At reset, the P70to P77 input mode is selected and pull- up resistors are disabled. (high impedance output)
P71	46			SBI0B, RXD0B	
P72	47			SBT0B	
P73	48			SBO1B, TXD1B	
P74	49			SBI1B, RXD1B	
P75	50			SBT1B	
P76	51			TCI01	
P77	52			TCI05	
P80	60	I/O	I/O port 8	LED0	8-Bit CMOS tri-state I/O port. Each bit can be set individually as either an input or output by the P8DIR register. A pull-up resistor for each bit can be selected individually by the P8PLU register. When configured as outputs, these pins can drive LEDs directly. At reset, the P80to P87 input mode is selected and pull- up resistors are disabled. (high impedance output)
P81	59			LED1	
P82	58			LED2	
P83	57			LED3	
P84	56			LED4	
P85	55			LED5	
P86	54			LED6	
P87	53			LED7	
PA0	62	I/O	I/O port A	AN0, DA0	6-Bit I/O port. A pull-up or pull-down resistor for each bit can be selected individually by the PAPLUD resister. However, pull-up and pull-down resistors cannot be mixed. At reset, the PA0 to PA6 input mode is selected and pull- up resistors are disabled. (high impedance output)
PA1	63			AN1, DA1	
PA2	64			AN2	
PA3	1			AN3	
PA4	2			AN4	
PA5	3			AN5	
PA6	4			AN6	

Table 1-3-5 Pin Function Summary (3/6)

Name	No.	I/O	Function	Other Function	Description
SBO0A SBO0B SBO1A SBO1B SBO3	18 48 15 45 33	Output	Serial interface transmission data output pins	P03, TXD0A P70, TXD0B P00, TXD1A P73, TXD1B P51, SDA3	Transmission data output pins for serial interfaces 0 , 1, 3. The output configuration, either CMOS push-pull or n-channel open-drain can be selected. Pull-up resistors can be selected by the P0PLU register, the P5PLU register and the P7PLUD register. Select output mode by the P0DIR register, the P5DIR register and the P7DIR register, and serial data output mode by serial mode register 1 (SC0MD1, SC1MD1, SC3MD1). These can be used as normal I/O pins when the serial interface is not used.
SBI0A SBI0B SBI1A SBI1B SBI3	19 49 16 46 32	Input	Serial interface reception data input pins	P04, RXD0A P71, RXD0B P01, RXD1A SDA4A P74, RXD1B P50	Reception data input pins for serial interfaces 0, 1, 3. Pll-up resistors can be selected by the P0PLU register, the P5PLU register and the P7PLUD register. Select input mode by the P0DIR register, the P5DIR register, the P7DIR register and serial input mode by the serial mode register 1 (SC0MD1, SC1MD1, SC3MD1). These can be used as normal I/O pins when the serial interface is not used.
SBT0A SBT0B SBT1A SBT1B SBT3	20 50 17 47 34	I/O	Serial interface clock I/O pins	P50 P72 P02, SCL4A P75 P52, SCL3	Clock I/O pins for serial interfaces 0, 1,3. The output configuration, either CMOS push-pull or n-channel open-drain can be selected. Pull-up resistors can be selected by the P0PLU resister and the P5PLU register and the P7PLUD register. Select clock I/O for each communication mode by the P0DIR register, the P5DIR register, the P7DIR register and serial mode register 1 (SC0MD1, SC1MD1, SC3MD1). These can be used as normal I/O pins when the serial interface is not used.
TXD0A TXD0B TXD1A TXD1B	18 48 15 45	Output	UART transmission data output pins	SBO0A, P03 SBO0B, P70 SBO1A, P00 SBO1B, P73	In the serial interface in UART mode, these pins are configured as the transmission data output pins. The output configuration, either CMOS push-pull or n-channel open-drain can be selected. Pull-up resistors can be selected by the P0PLU register and the P7PLUD register. Select output mode by the P0DIR register and the P7DIR register, and serial data output by serial interface 1 mode register 1 (SC0MD1, SC1MD1). These can be used as normal I/O pins when the serial interface is not used.

Table 1-3-6 Pin Function Summary (4/6)

Name	No.	I/O	Function	Other Function	Description
RXD0A RXD0B RXD1A RXD1B	19 49 16 46	Input	UART reception data input pin	SBI0A, P04 SBI0B, P71 SBI1A, P01 SDA4A SBI1B, P74	In the serial interface in UART mode, these pins are configured as the received data input pin. Pull-up resistors can be selected by the P0PLU register and P7PLUD register. Set this pin to the input mode by the P0DIR register and the P7DIR register, and to the serial input mode by the serial interface1 mode register 1 (SC0MD1, SC1MD1). This can be used as normal I/O pin when the serial interface is not used.
TCO0A TCI00B TCI01 TCO4A TCI04B TCI05	22 23 51 24 25 52	I/O	Timer I/O pins	P10, RMOUT P11 P12 P13 P37 P77	Event counter clock input pins, overflow pulse and PWM signal output pins for 8-bit timers 0 , 1, 4, 5. To use these pins as event clock inputs, configure them as inputs by the P1DIR and P7DIR register. When the pins are used as inputs, pull-up resistors can be specified by the P1PLU, P7PLUD register. For overflow pulse, PWM signal output, select the special function pin by the port 1 output mode register (P1OMD) and set to the output mode by the P1DIR register. When not used for timer I/O, these can be used as normal I/O pins.
SDA4A SDA4B	16 35	I/O	Serial interface data I/O pins	P01, SBI1A RXD1A P53	Reception data input pins for serial interfaces 4. During data communications, select n-channel open-drain to comply with IIC communication standard. Pull-up resistors can be selected by the P0PLU register and the P5PLU register. During data communications, select output mode by the P0DIR register and the P5DIR register. These can be used as normal I/O pins when the serial interface is not used.
SCL4A SCL4B	17 36	I/O	Serial interface 4 clock I/O pins	P02, SBT1A, P54	Clock I/O pins for serial interfaces 4. During data communications, select n-channel open-drain to comply with IIC communication standard. Pull-up resistors can be selected by the P0PLU resister and the P5PLU register. During data communications, select output mode by the P0DIR register and the P5DIR register. These can be used as normal I/O pins when the serial interface is not used.
RMOUT	22	I/O	Remote control transmission signal output pin	P10,TCO0A	Output pin for remote control transmission signal with a carrier signal. For remote control carrier output, select the special function pin by the port 1 output mode register (P1OMD) and set to the output mode by the P1DIR register. Also, set to the remote control carrier output by the remote control carrier output control register (RMCTR). This can be used as a normal I/O pin when remote control is not used.

Table 1-3-7 Pin Function Summary (5/6)

Name	No.	I/O	Function	Other Function	Description
BUZZER	21	Output	Buzzer output	P06	Piezoelectric buzzer driver pin. The driving frequency can be selected by the DLYCTR register. Select output mode by the P0DIR register and select P06 buzzer output by the DLYCTR register. When not used for buzzer output, this pin can be used as a normal I/O pin.
TCI07	26	I/O	Timer I/O pin	P14	Event counter clock input pin, overflow pulse and PWM signal output pin for 16-bit timer 7. To use this pin as event clock input, configure this as input by the P1DIR register. In the input mode, pull-up resistors can be selected by the P1PLU register. For overflow pulse, PWM signal output, select the special function pin by the port 1 output mode register (P1OMD), and set to the output mode by the P1DIR register. When not used for timer I/O, this can be used as normal I/O pin.
VREF+ VREF-	6 61	- -	+ power supply for A/D converter - power supply for A/D converter		Reference power supply pins for the A/D converter. Normally, the values of VDD=VREF+ and VSS=VREF- are used. When they are not used, the values should be VREF+=VDD and VREF-=VSS.
AN0 AN1 AN2 AN3 AN4 AN5 AN6	62 63 64 1 2 3 4	Input	Analog input pins	PA0, DA0 PA1, DA1 PA2 PA3 PA4 PA5 PA6	Analog input pins for an 7-channel, 10-bit A/D converter. When not used for analog input, these pins can be used as normal I/O pins.
DA0 DA1	62 63	Output	Analog output pins	PA0, AN0 PA1, AN1	Analog output pins for an 2-channel, 8-bit D/A converter. When not used for analog output, these pins can be used as normal I/O pins.
IRQ0 IRQ1 IRQ2 IRQ3 IRQ4	27 28 29 30 31	Input	External interrupt input pins	P20 P21, ACZ P22 P23 P24	External interrupt input pins. The valid edge for IRQ0 to 4 can be selected with the IRQnICR register. IRQ1 is an external interrupt pin that is able to determine AC zero crossings. Both edge for IRQ0 to 4 are valid for interrupt. When these are not used for interrupts, these can be used as normal input pins.
ACZ	28	Input	AC zero-cross detection input pin	P21, IRQ1	An input pin for an AC zero-cross detection circuit. The AC zero-cross detection circuit outputs a high level when the input is at an intermediate level. It outputs a low level at all other times. ACZ input signal is connected to the P21 input circuit and the IQR1 interrupt circuit. When the AC zero-cross detection circuit is not used, this pin can be used as a normal P21 input.

Table 1-3-8 Pin Function Summary (6/6)

Name	No.	I/O	Function	Other Function	Description
KEY0	37	I/O	Key interrupt input pins	P60, SDO0	Input pins for interrupt based on ORed result of pin inputs. Key input pin for 2 bits can be selected individually by the key interrupt control register (P6MD). When not used for KEY input, these pins can be used as normal I/O pins.
KEY1	38			P61, SDO1	
KEY2	39			P62, SDO2	
KEY3	40			P63, SDO3	
KEY4	41			P64, SDO4	
KEY5	42			P65, SDO5	
KEY6	43			P66, SDO6	
KEY7	44			P67, SDO7	
MMOD	17	Input	Memory mode switching input pins		This pin sets the memory expansion mode. Always set the input low.

1-4 Block Diagram

1-4-1 Block Diagram

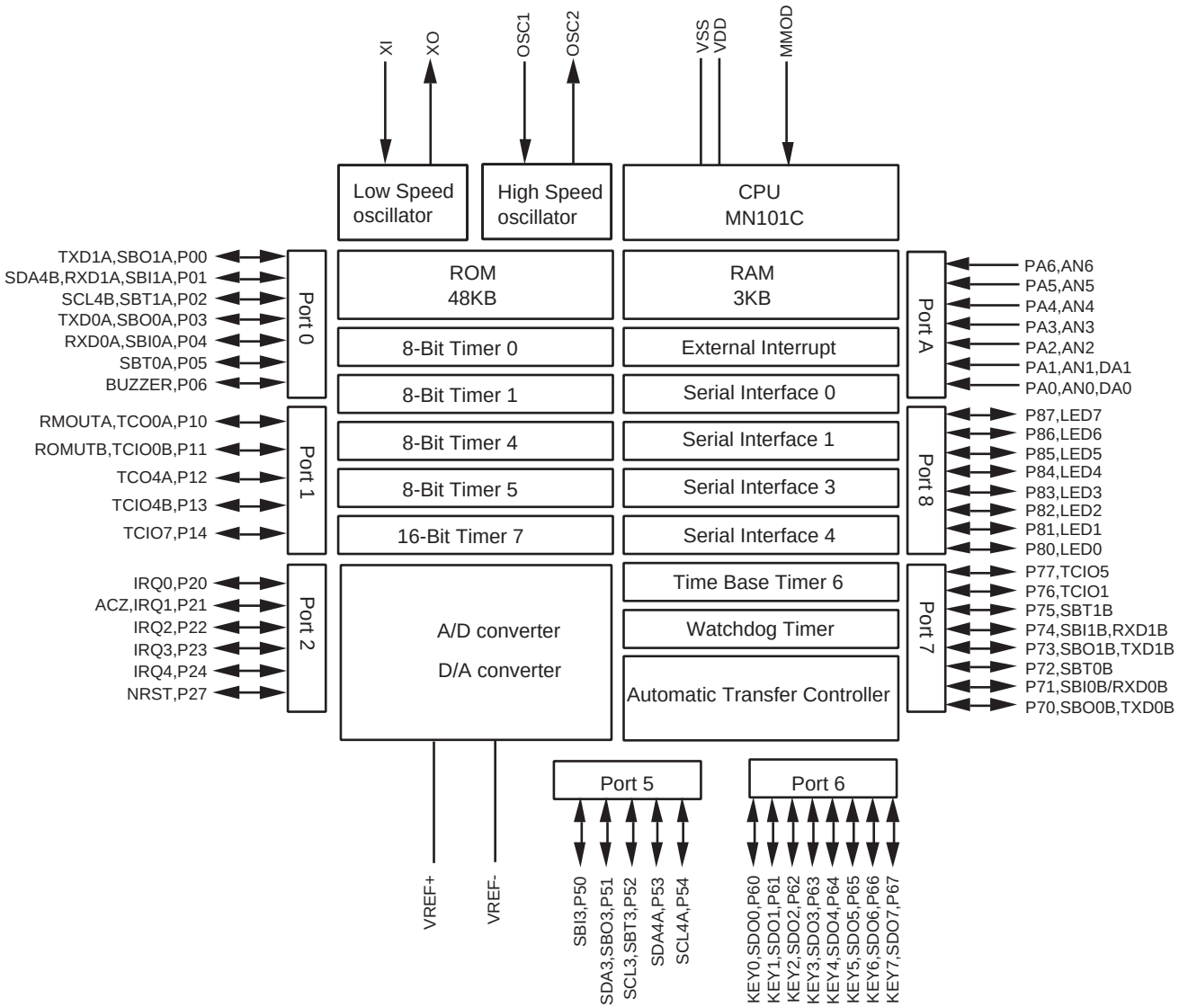


Figure 1-4-1 Block Diagram

1-5 Electrical Characteristics

This LSI user's manual describes the standard specification. System clock (fs) is 1/2 of high speed oscillation at NORMAL mode, or 1/4 of low speed oscillation at SLOW mode. Please ask our sales offices for its own product specifications.

Contents \ Model	MN101C77
Structure	CMOS integrated circuit
Application	General purpose
Function	8-Bit single-chip microcontroller

1-5-1 Absolute Maximum Ratings*2,*3 (voltages referenced to Vss)

	Parameter		Symbol	Rating	Unit
1	Power supply voltage		V_{DD}	- 0.3 to +4.6	V
2	Input clamp voltage		Ic	-500 to +500	µA
3	Input pin voltage		V_I	-0.3 to V_{DD} +0.3	V
4	Output pin voltage		V_O	-0.3 to V_{DD} +0.3	
5	I/O pin voltage		V_{IO}	-0.3 to V_{DD} +0.3	
6	Peak output current	Port 8 *4	I_{OL1} (peak)	30	mA
7		Other than Port 8	I_{OL2} (peak)	10	
8			I_{OH} (peak)	-10	
9	Average output current *1	Port 8 *4	I_{OL1} (avg)	20	
10		Other than Port 8	I_{OL2} (avg)	5	
11			I_{OH} (avg)	-5	
12	Power dissipation		P_D	300	mW
13	Operating ambient temperature		T_{opr}	-40 to +85	°C
14	Storage temperature		T_{stg}	-40 to +125 *5	

*1 Applied to any 100 ms period.

*2 Connect at least one bypass capacitor of 0.1 µF or larger between the power supply pin and the ground for latch-up prevention.

*3 The absolute maximum ratings are the limit values beyond which the LSI may be damaged and proper operation is not assured.

*4 Applied when P8LED register outputs LED.

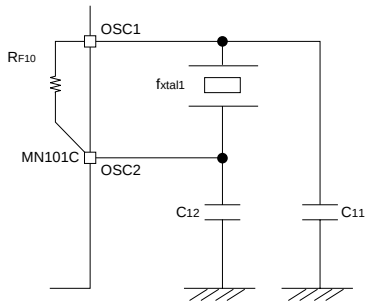
*5 -40 to + 98 (°C) for the Flash EEPROM version.

1-5-2 Operating Conditions [NORMAL mode : fs=fosc/2, SLOW mode : fs=fx/2]

T_a=-40 °C to +85 °C V_{DD}=1.8 V to 3.6 V, V_{SS}=0 V

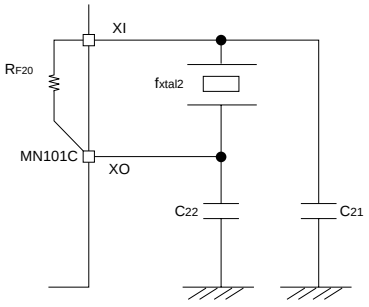
	Parameter	Symbol	Conditions	Rating			Unit
				MIN	TYP	MAX	
Power supply voltage							
1	Power supply voltage	V_{DD1}	$f_{osc} \leq$ 20.00 MHz $f_s = f_{osc}/2$	2.5		3.6	V
2		V_{DD2}	$f_{osc} \leq$ 10.00 MHz $f_s = f_{osc}/2$	2.1		3.6	
3		V_{DD3}	$f_{osc} \leq$ 4.00 MHz $f_s = f_{osc}/2$	1.8		3.6	
4		V_{DD4}	fx = 32.768 kHz $f_s = f_{osc}/2$	1.8		3.6	
5	Voltage to maintain RAM data	V_{DD5}	During STOP mode	1.8		3.6	
Operation speed *1							
6	Minimum instruction execution time	t_{c1}	V_{DD} = 2.5 V to 3.6 V	0.1			µs
7		t_{c2}	V_{DD} = 2.1 V to 3.6 V	0.2			
8		t_{c3}	V_{DD} = 1.8 V to 3.6 V	0.5			
9		t_{c4}	V_{DD} = 1.8 V to 3.6 V		61.04		
Crystal osillator 1 Figure 1-5-1							
10	Crystal frequency	f_{xtal1}	V_{DD} = 2.5 V to 3.6 V	1.0		20.0	MHz
11	External capasitors	C_{11}			47		pF
12		C_{12}			47		
13	Internal feedback resistor	R_{F10}	V_{DD} = 3.3 V		1000		kΩ
Crystal osillator 2 Figure 1-5-2							
14	Crystal frequency	f_{xtal2}	V_{DD}=1.8 V to 3.6 V		32.768		kHz
15	External capasitors	C_{21}			22		pF
16		C_{22}			22		
17	Internal feedback resistor	R_{F20}	V_{DD}=3.3 V		6.0		MΩ

*1 tc1, tc2, tc3 : 1/2 of high speed oscillation
tc4 : 1/2 of high speed oscillation



The feedback resistor is built-in.

Figure 1-5-1 Crystal Oscillator 1



The feedback resistor is built-in.

Figure 1-5-2 Crystal Oscillator 2

T_a=-40 °C to +85 °C V_{DD}=1.8 V to 3.6 V V_{SS}=0 V

Parameter		Symbol	Conditions	Rating			Unit
				MIN	TYP	MAX	
External clock input 1 OSC1 (OSC2 is opened)							
18	Clock frequency	f_{osc}		1.0		20.0	MHz
19	High level pulse width	t_{wh1}	*1 Figure 1-5-3	20.0			ns
20	Low level pulse width	t_{wl1}		20.0			
21	Rising time	t_{wr1}	Figure 1-5-3			5.0	
22	Falling time	t_{wf1}				5.0	
External clock input 2 XI (XO is opened)							
23	Clock frequency	f_x			32.768		kHz
24	High level pulse width	t_{wh2}	*1 Figure 1-5-4	3.5			µs
25	Low level pulse width	t_{wl2}		3.5			
26	Rising time	t_{wr2}	Figure 1-5-4			20	ns
27	Falling time	t_{wf2}				20	

*1 The clock duty rate should be 45% to 55%.

Certain operating conditions differ between the mask ROM version and the Flash version. Refer to chapter 18 Flash EEPROM for electrical characteristics of the Flash version.

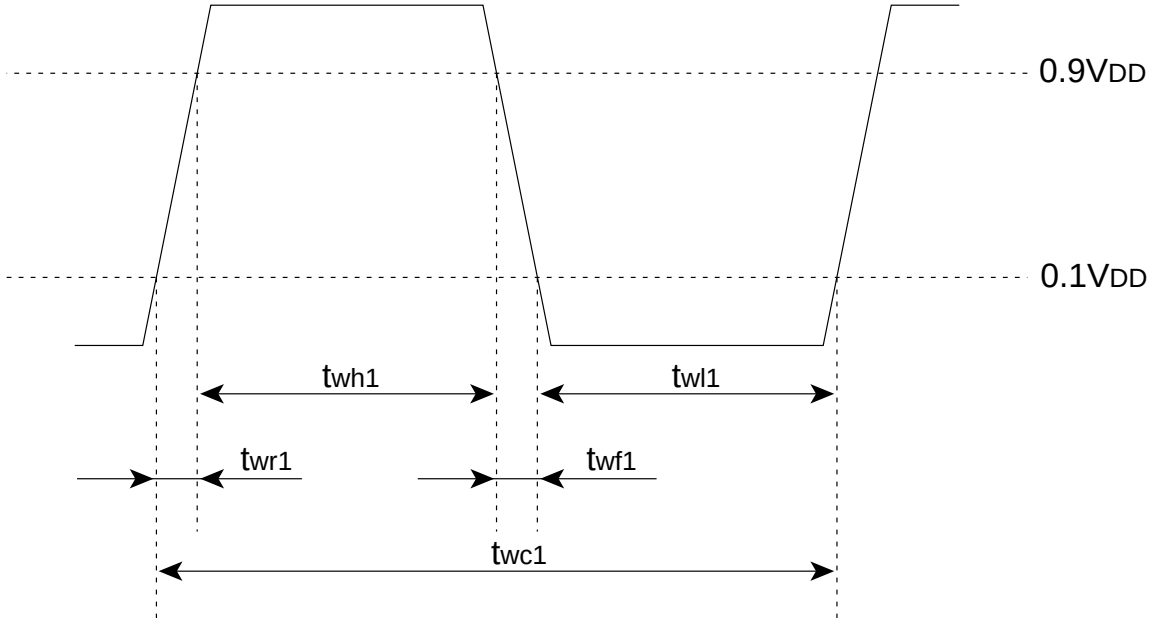


Figure 1-5-3 OSC1 Timing Chart

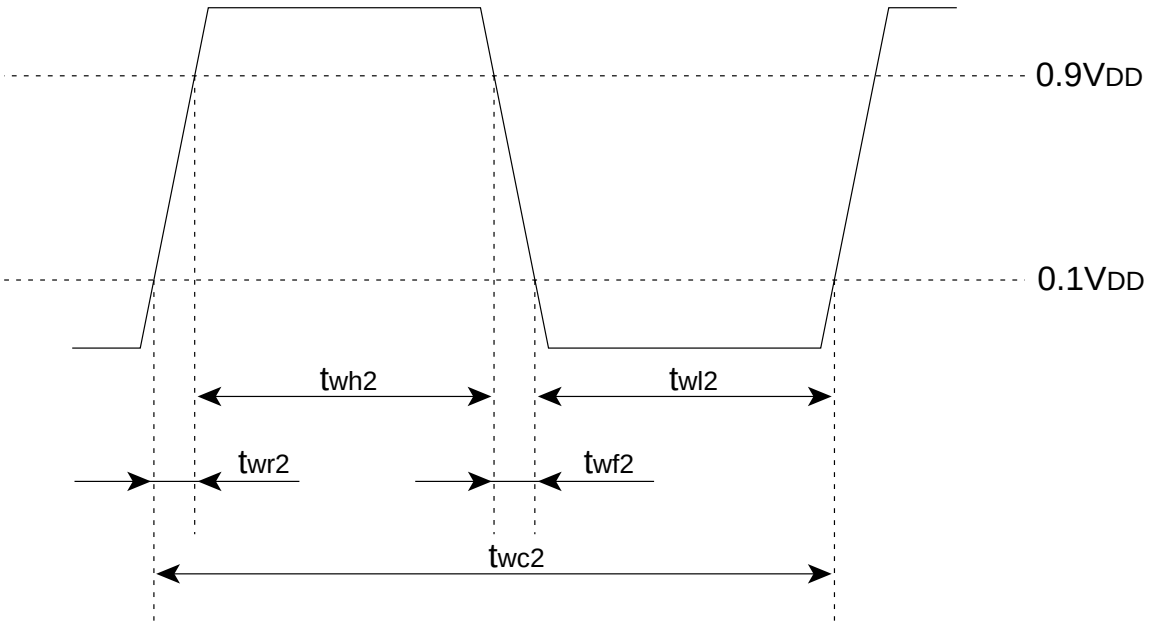


Figure 1-5-4 XI Timing Chart

1-5-3 DC Characteristics

T_a=-40 °C to +85 °C V_{DD}=1.8 V to 3.6 V V_{SS}=0 V

	Parameter	Symbol	Conditions	Rating			Unit
				MIN	TYP	MAX	
Power supply current (not load at output pin) *1							
1	Power supply current	I_{DD1}	f_{osc}=20.00 MHz,V_{DD}=3.3 V [$f_s = f_{osc}/2$]		6	12	mA
2		I_{DD2}	f_{osc}=8.39 MHz,V_{DD}=3.3 V [$f_s = f_{osc}/2$]		3	6	
3		I_{DD3}	f_x=32.768 kHz,V_{DD}=3.3 V [$f_s = f_x/2$] Ta=25 °C		10	20	µA
4		I_{DD4}	f_x=32.768 kHz,V_{DD}=3.3 V [$f_s = f_x/2$] Ta=-40 °C to +85 °C			40	
5	Supply current during HALT1 mode	I_{DD5}	f_x=32.768 kHz,V_{DD}=3.3 V Ta=25 °C		5	10	
6		I_{DD6}	f_x=32.768 kHz,V_{DD}=3.3 V Ta=-40 °C to +85 °C			40	
7	Supply current during STOP mode	I_{DD7}	V_{DD}=3.3 V Ta=25 °C		0	2	
8		I_{DD8}	V_{DD}=3.3 V Ta=-40 °C to +85 °C			30	

*1 Measured under conditions of Ta=25 °C, without load.

- The supply current during operation, I_{DD1}(I_{DD2}), is measured under the following conditions: After all I/O pins are set to input mode and the oscillation is set to <NORMAL mode>, the MMOD pin is connected to V_{SS} level, the input pins are connected to V_{DD} level, and a 20 MHz (8.39 MHz) square wave of V_{DD} and V_{SS} amplitude is input to the OSC1 pin.
- The supply current during operation, I_{DD3}(I_{DD4}), is measured under the following conditions: After all I/O pins are set to input mode and the oscillation is set to <SLOW mode>, the MMOD pin is connected to V_{SS} level, the input pins are connected to V_{DD} level, and a 32.768 kHz square wave of V_{DD} and V_{SS} amplitude is input to the XI pin.
- The supply current during HALT mode, I_{DD5}(I_{DD6}), is measured under the following conditions: After all I/O pins are set to input mode and the oscillation is set to <HALT mode>, the MMOD pin is connected to V_{SS} level, the input pins are connected to V_{DD} level and an 32.768 kHz square wave of V_{DD} and V_{SS} amplitude is input to the XI pin.
- The supply current during STOP mode, I_{DD7}(I_{DD8}), is measured under the following conditions: After the oscillation is set to <STOP mode>, the MMOD pin is connected to V_{SS} level, the input pins are connected to V_{DD} level, and the OSC1 and XI pins are unconnected.

T_a = -40 °C to +85 °C V_{DD}=1.8 V to 3.6 V V_{SS}=0 V

Parameter		Symbol	Conditions	Rating			Unit
				MIN	TYP	MAX	
Input pin 1 MMOD							
9	Input high voltage	V_{IH1}		0.8V_{DD}		V_{DD}	V
10	Input low voltage	V_{IL1}		0		0.2V_{DD}	
11	Input leakage current	I_{LK1}	V_{IN}=0 V to V_{DD}			±10	µA
Input pin 2 P21 (at used as ACZ)							
12	Input high voltage 1	V_{DHH}	V_{DD}=3.3 V Figure 1-5-5	2.9		V_{DD}	V
13	Input low voltage 1	V_{DLH}		V_{SS}		2.1	
14	Input high voltage 2	V_{DHL}		1.1		V_{DD}	
15	Input low voltage 2	V_{DLL}		V_{SS}		0.4	
16	Input leakage current	I_{LK2}	V_{IN}=0 V to V_{DD}			±10	µA
17	Rising time	t_{rs}	Figure 1-5-5	30			µs
18	Falling time	t_{fs}		30			

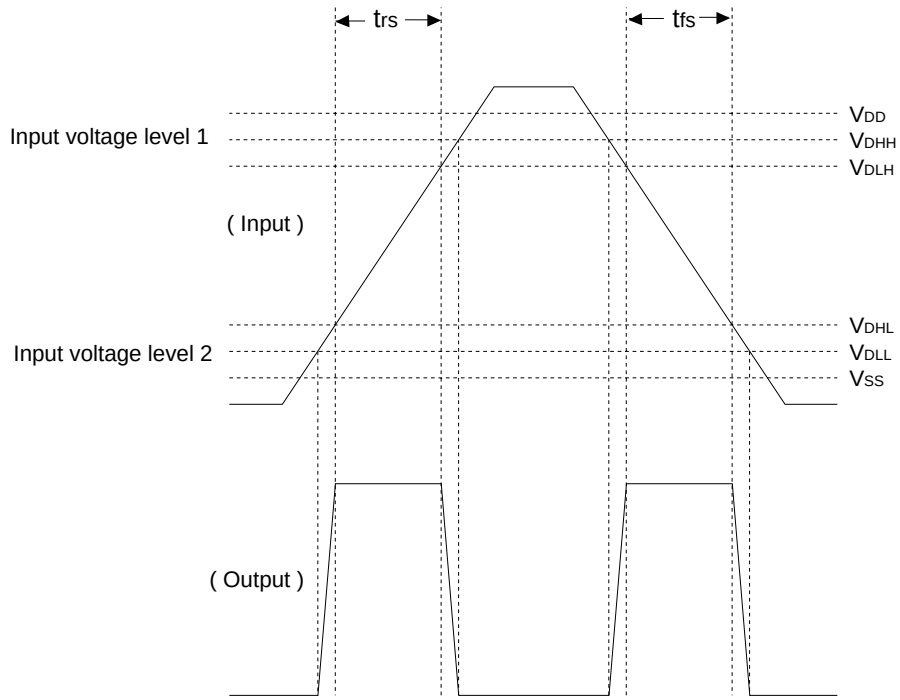


Figure 1-5-5 AC Zero-Cross Detector

T_a=-40 °C to +85 °C V_{DD}=1.8 V to 3.6 V V_{SS}=0 V

	Parameter	Symbol	Conditions	Rating			Unit
				MIN	TYP	MAX	
Input pin 3 P27 (NRST)							
19	Input high voltage	V_{IH3}		0.8V_{DD}		V_{DD}	V
20	Input low voltage	V_{IL3}		0		0.2V_{DD}	
21	Input high current	I_{IH3}	VDD=3.3 V,V_{IN}=V_{SS} Pull-up resistor is built-in	-30	-100	-300	µA
I/O pin 4 PA0 to PA6							
22	Input high voltage	V_{IH4}		0.8V_{DD}		V_{DD}	V
23	Input low voltage	V_{IL4}		0		0.2V_{DD}	
24	Input leakage current	I_{LK4}	V_{IN}=0 V to V_{DD}			±2	µA
25	Input high current	I_{IH4}	V_{DD}=3.3 V,V_{IN}=V_{SS} Pull-up resistor is ON	-30	-100	-300	
26	Input low current	I_{IL4}	V_{DD}=3.3 V,V_{IN}=V_{DD} Pull-down resistor is ON	30	100	300	
27	Output high voltage	V_{OH4}	V_{DD}=3.3 V, I_{OH}=-2.0 mA	2.7			V
28	Output low voltage	V_{OL4}	V_{DD}=3.3 V, I_{OL}=2.0 mA			0.4	
I/O pin 5 P00 to P06, P10 to P14, P20 to P24, P50 to P54, P60 to P67							(Schmitt trigger input)
29	Input high voltage	V_{IH5}		0.8V_{DD}		V_{DD}	V
30	Input low voltage	V_{IL5}		0		0.2V_{DD}	
31	Input leakage current	I_{LK5}	V_{IN}=0 V to V_{DD}			±10	µA
32	Input high current	I_{IH5}	V_{DD}=3.3 V,V_{IN}=V_{SS} Pull-up resistor is ON	-30	-100	-300	
33	Output high voltage	V_{OH5}	V_{DD}=3.3 V, I_{OH}=-2.0 mA	2.7			V
34	Output low voltage	V_{OL5}	V_{DD}=3.3 V, I_{OL}=2.0 mA			0.4	
I/O pin 6 P70 to P77							(Schmitt trigger input)
35	Input high voltage	V_{IH6}		0.8V_{DD}		V_{DD}	V
36	Input low voltage	V_{IL6}		0		0.2V_{DD}	
37	Input leakage current	I_{LK6}	V_{IN}=0 V to V_{DD}			±10	µA
38	Input high current	I_{IH6}	V_{DD}=3.3 V,V_{IN}=V_{SS} Pull-up resistor is ON	-30	-100	-300	
39	Input low current	I_{IL6}	V_{DD}=3.3 V,V_{IN}=V_{DD} Pull-down resistor is ON	30	100	300	
40	Output high voltage	V_{OH6}	V_{DD}=3.3 V, I_{OH}=-2.0 mA	2.7			V
41	Output low voltage	V_{OL6}	V_{DD}=3.3 V, I_{OL}=2.0 mA			0.4	

Ta=-40 °C to +85 °C VDD=1.8 V to 3.6 V VSS=0 V

Parameter		Symbol	Conditions	Rating			Unit
				MIN	TYP	MAX	
I/O pin 7 P80 to P87							
42	Input high voltage	V_{IH7}		$0.8V_{DD}$		V_{DD}	V
43	Input low voltage	V_{IL7}		0		$0.2V_{DD}$	
44	Input leakage current	I_{LK7}	V_{IN}=0 V to V_{DD}			±10	µA
45	Input high current	I_{IH7}	V_{DD}=3.3 V,V_{IN}=V_{SS} Pull-up resistor is ON	-30	-100	-300	
46	Output high voltage	V_{OH7}	V_{DD}=3.3 V, I_{OH}=-2.0 mA	2.7			V
47	Output low voltage	V_{OL7}	V_{DD}=3.3 V, I_{OL}=2.0 mA			0.4	
48	Output low voltage (LED)	V_{OLL7}	V_{DD}=3.3 V, I_{OLL}=15.0 mA			1.0	

1-5-4 A/D Converter Characteristics *2

T_a=-40 °C to +85 °C V_{DD}= 3.3 V V_{SS}=0 V

	Parameter	Symbol	Conditions	Rating			Unit
				MIN	TYP	MAX	
1	Resolution					10	Bits
2	Non-linearity error 1		V_{DD} = 3.3 V,V_{SS} = 0 V V_{REF+} = 3.3 V,V_{REF-} = 0 V T_{AD} = 800 ns			±3	LSB
3	Differential non-linearity error 1					±3	
4	Non-linearity error		V_{DD} = 3.3 V,V_{SS} = 0 V V_{REF+} = 3.3 V,V_{REF-} = 0 V T_{AD} = 15.26 µs			±5	
5	Differential non-linearity error 2					±5	
6	Zero transition voltage		V_{DD} = 3.3 V,V_{SS} = 0 V V_{REF+} = 3.3 V,V_{REF-} = 0 V T_{AD} = 800 ns		25	80	mV
7	Full-scale transition voltage			3220	3275		
8	A/D conversion time		T_{AD} = 800 ns	9.6			µs
9			T_{AD} = 15.26 µs			183	
10	Sampling time		T_{AD} = 1.0 µs	2		18	
11			T_{AD} = 15.26 µs		30.5		
12	Reference voltage	V_{REF+}	*1	V_{REF-}		V_{DD}	V
13		V_{REF-}	*1	V_{SS}		0.5	
14	Analog input voltage			V_{REF-}		V_{REF+}	
15	Analog input leakage current		unselected channel V_{ADIN} = 0 V to V_{DD}			±2	µA
16	Reference voltage pin input leakage current		Lader resistor OFF $V_{REF-} \leq V_{REF+} \leq V_{DD}$			±10	
17	Ladder resistance	R_{ladd}	V_{DD} = 3.3 V	20	50	80	kΩ

*1 Set the potential difference between V_{REF+} and V_{REF-} over 2 V.

*2 The value is measured with A/D Converter, not with D/A Converter.

1-5-5 D/A Converter Characteristics *2

T_a = -40 °C to +85 °C V_{DD} = 3.3 V V_{SS} = 0 V

	Parameter	Symbol	Conditions	Rating			Unit
				MIN	TYP	MAX	
1	Resolution *1					8	Bits
2	Reference voltage low level	V_{REF-}		0		0.5	V
3	Reference voltage high level	V_{REF+}		2.0		V_{DD}	
4	Zero-scale output voltage *1	V_{ZS}	V_{REF+} = 3.3 V, V_{REF-} = 0 V D7 to D0=ALL"L"		0.0	0.05	
5	Full-scale output voltage *1	V_{FS}	V_{REF+} = 3.3 V, V_{REF-} = 0 V D7 to D0=ALL"H"	3.20	3.29		
6	Analog output resistance (minimum reference resistance) *1	R_{OUT}		7.0	11.0	15.0	kΩ
7	Non-linearity error	N_{LE}	V_{REF+} = 3.3 V, V_{REF-} = 0 V		±0.5	±1.0	LSB
8	Differenctial non-linearity error *1	D_{NLE}	V_{REF+} = 3.3 V, V_{REF-} = 0 V		±0.5	±1.5	
9	Settling time *1	T_{SET}	External capacitor CL = 35 pF All bits are set to ON or OFF			2.0	µs

*1 The standard value is guaranteed under condition of V_{DD}=V_{REF+}=3.3 V, V_{REF}-=0.0 V .

*2 The value is measured with D/A Converter, not with A/D Converter.

1-6 Precautions

1-6-1 General Usage

■Connection of V_{DD} pin, and V_{SS} pin

All V_{DD} pins should be connected directly to the power supply and all Vss pins should be connected to ground in the external. The following shows the correct connections and the incorrect connections. Please consider the LSI chip orientation before mounting it on the printed circuit board. Incorrect connection may lead a fusion and break a micro controller.

■Cautions for Operation

(1) If you install the product close to high-field emissions (under the cathode ray tube, etc), shield the package surface to ensure normal performance.

(2) Please consider the operation temperature. The guaranteed operation temperature differs on each model. For example, if temperature is over the operating condition, its operation may be executed wrongly.

(3) Please consider the operation voltage. The guaranteed operation voltage differs on each model.
-If the operation voltage is over the operation range, it can be shortened the length of its life.
-If the operation voltage is below the operating range, its operation may be executed wrongly.

1-6-2 Unused Pins

■Unused Pins (only for input)

Insert 10 kΩ to 100 kΩ resistor to unused pins (only for input) for pull-up or pull-down. If the input is unstable, Pch transistor and Nch transistor of input inverter are on, and through current goes to the input circuit. That increases current consumption and causes power supply noise.

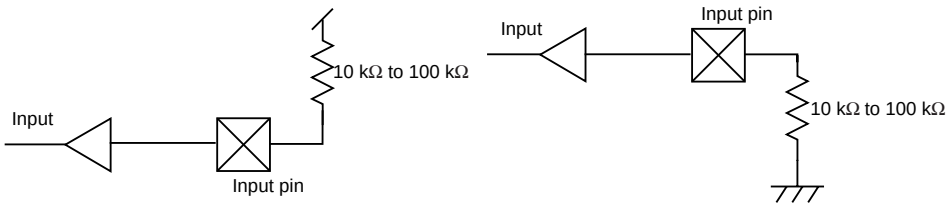


Figure 1-6-1 Unused Pins (only for input)

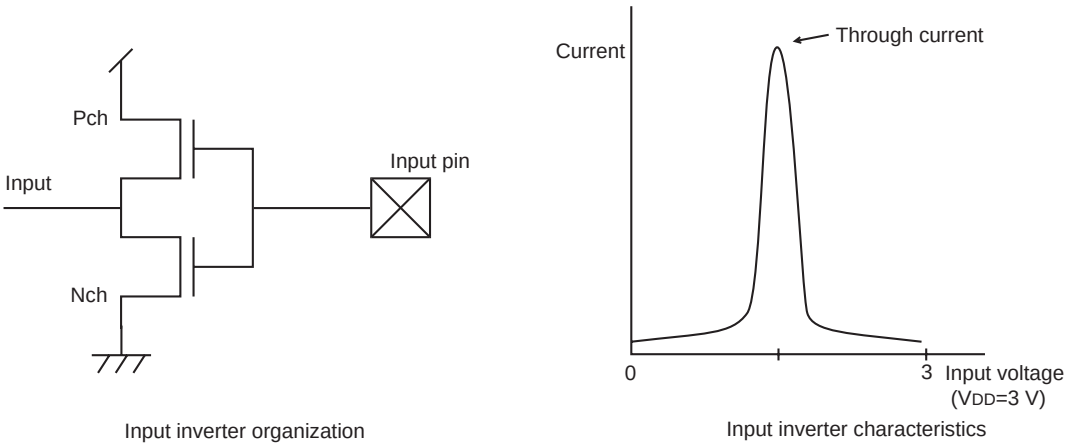


Figure 1-6-2 Input Inverter Organization and Characteristics

■Unused pins (for I/O)

Unused I/O pins should be set according to pins' condition at reset. If the output is high impedance (Pch / Nch transistor : output off) at reset, to stabilize input, set 10 kΩ to 100 kΩ resistor to be pull-up or pull-down. If the output is on at reset, set them open.

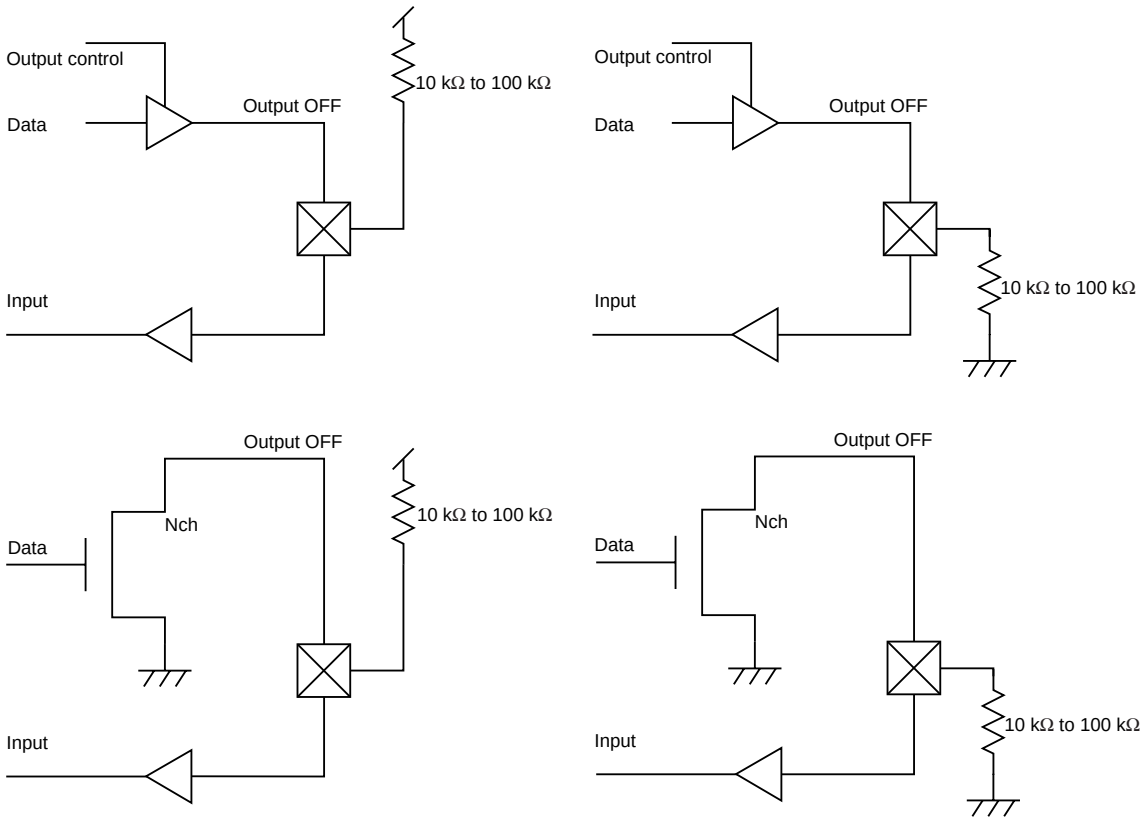


Figure 1-6-3 Unused I/O pins (high impedance output at reset)

1-6-3 Power Supply

■The Relation between Power Supply and Input Pin Voltage

Input pin voltage should be supplied only after power supply is on. If the input pin voltage is applied supplies before power supply is on, a latch up occurs and causes the destruction of micro controller by a large current flow.

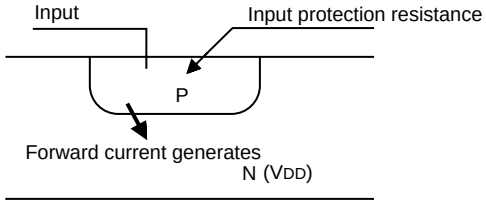
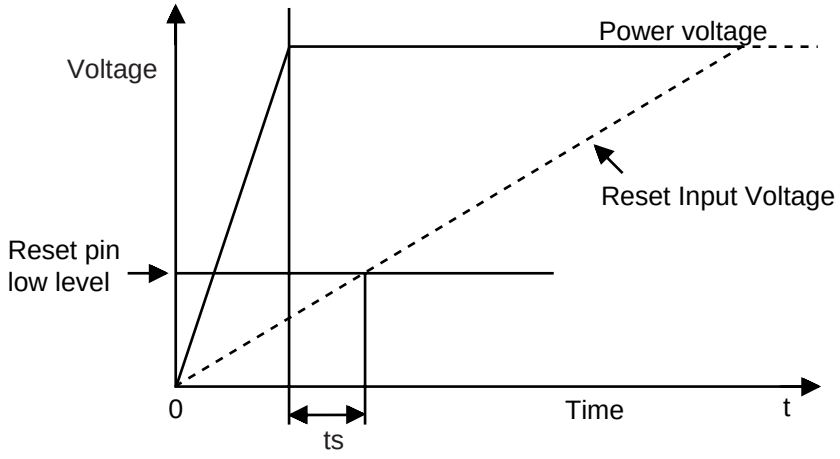


Figure 1-6-4 Power Supply and Input Pin Voltage

■The Relation between Power Supply and Reset Input Voltage

After power supply is on, reset pin voltage should be low for sufficient time, ts, before rising , in order to be recognized as a reset signal.



[☞ Chapter 2. 2-8 Reset]

Figure 1-6-5 Power Supply and Reset Input Voltage

1-6-4 Power Supply Circuit

■Cautions for Setting Power Supply Circuit

The CMOS logic microcontroller is high speed and high density. So, the power circuit should be designed, taking into consideration of AC line noise, ripple caused by LED driver. Figure 1-6-6 shows an example for emitter follower type power supply circuit.

■An example for Emitter Follower Type Power Supply Circuit

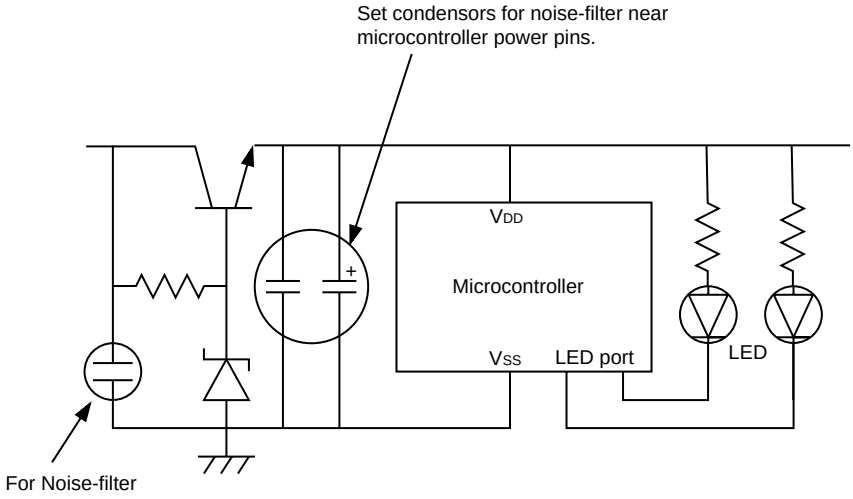
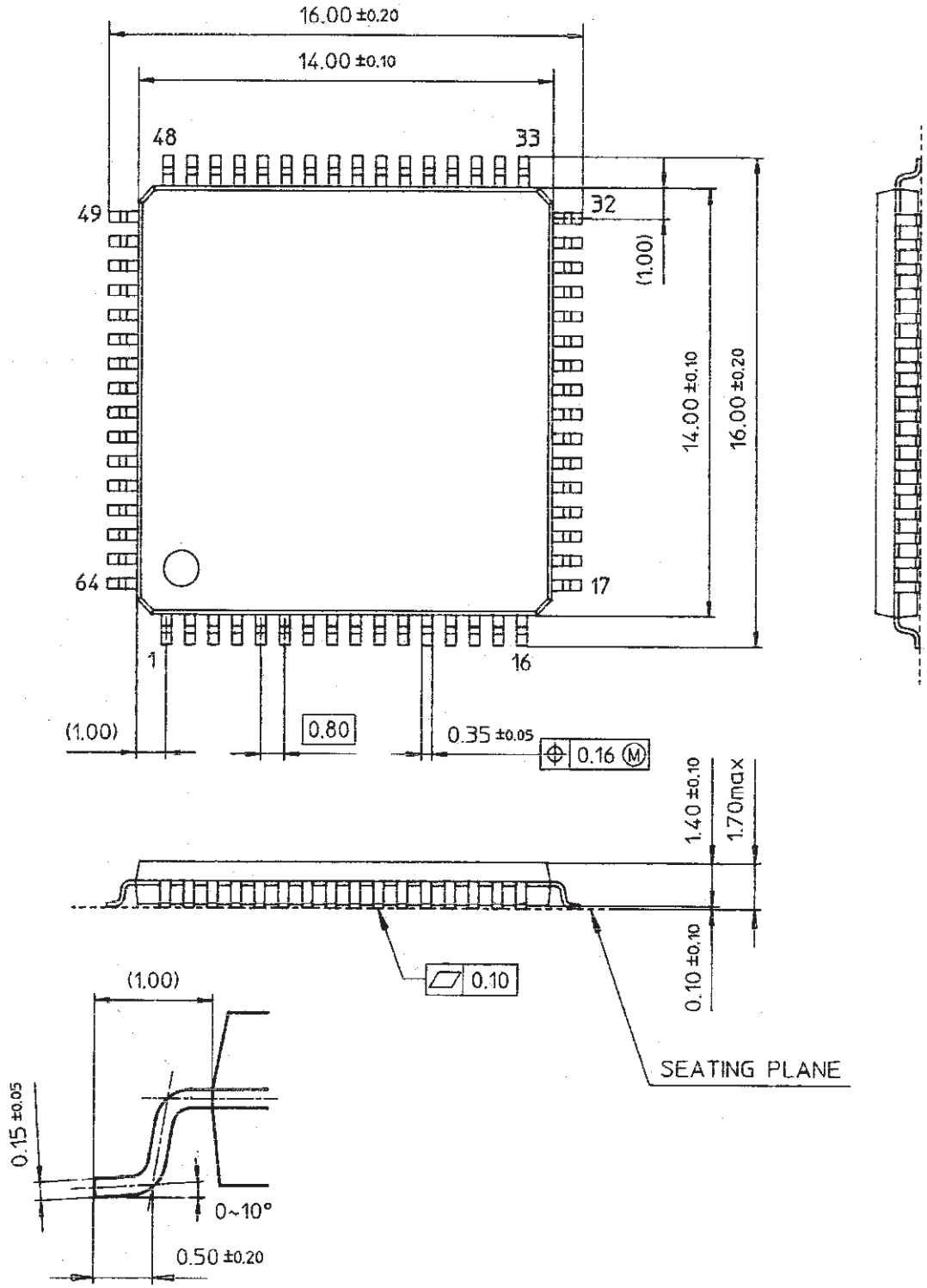


Figure 1-6-6 An Example for Emitter follower type Power Supply Circuit

1-7 Package Dimension

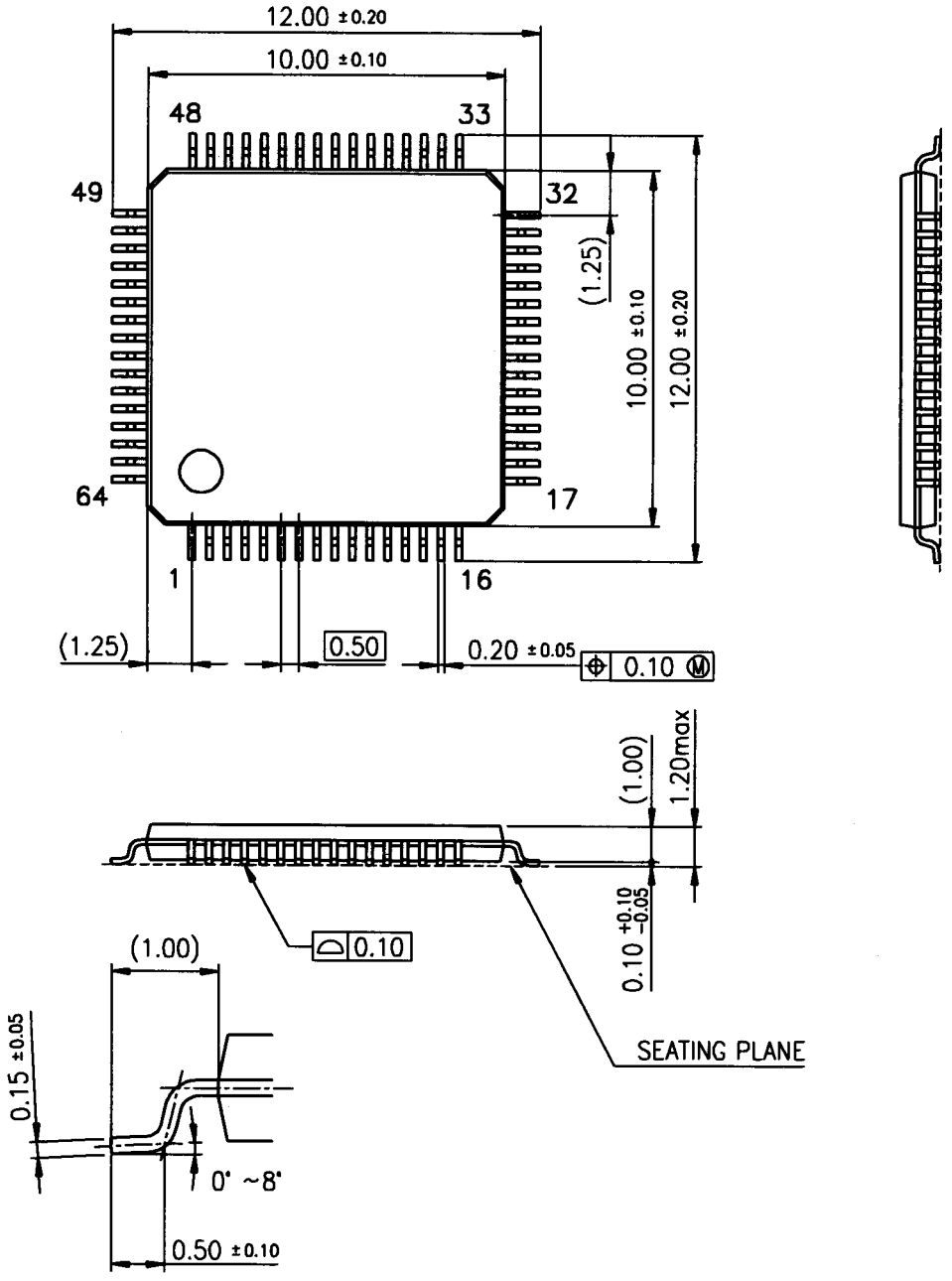
Package Code : LQFP064-P-1414

Units : mm



Package Code : TQFP064-P-1010C

Units : mm



Chapter 2 CPU Basics

2

2-1 Overview

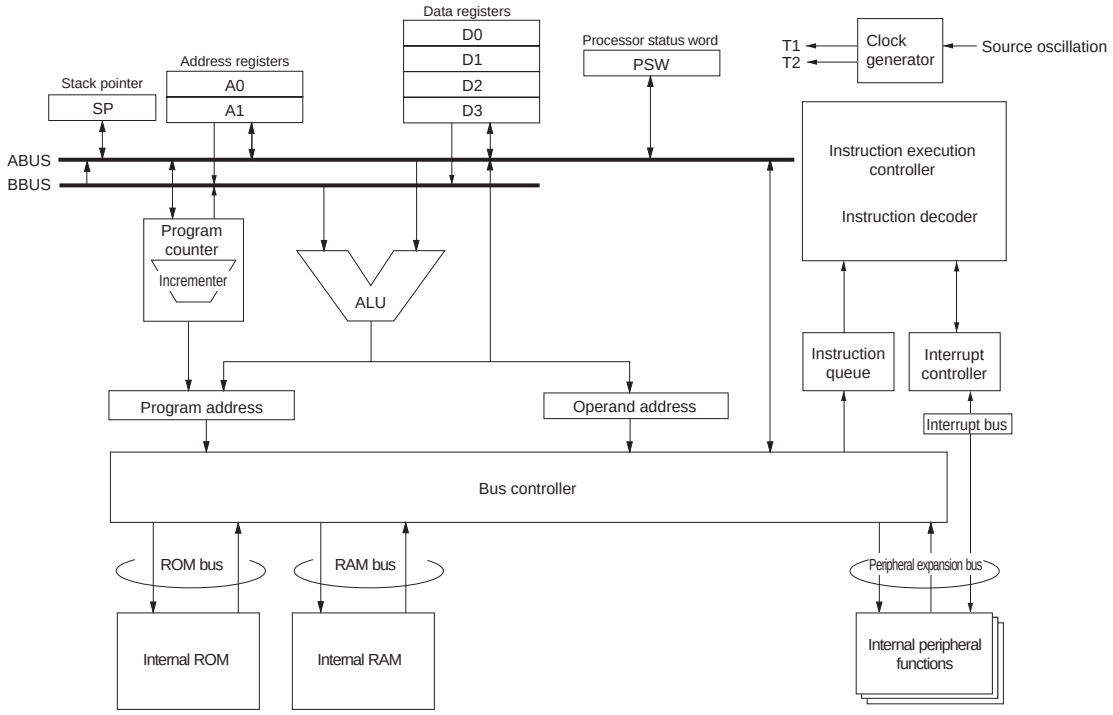
The MN101C CPU has a flexible optimized hardware configuration. It is a high speed CPU with a simple and efficient instruction set. Specific features are as follows:

1. Minimized code sizes with instruction lengths based on 4-bit increments
   The series keeps code sizes down by adopting a basic instruction length of one byte and variable instruction lengths based on 4-bit increments.
2. Minimum execution instruction time is one system clock cycle.
3. Minimized register set that simplifies the architecture and supports C language
   The instruction set has been determined, depending on the size and capacity of hardware, after an analysis of embedded application programing code and creation code by C language compiler. Therefore, the set is simple instruction using the minimal register set required for C language compiler. [☞ "MN101C LSI User's Manual" (Architecture Instructions)]

Table 2-1-1 Basic Specifications

Structure	Load / store architecture	
	Six registers	Data : 8-bit x 4 Address : 16-bit x 2
	Other	PC : 19-bit PSW : 8-bit SP : 16-bit
Instructions	Number of instructions	37
	Addressing modes	9
	Instruction length	Basic portion : 1 byte (min.) Extended portion : 0.5-byte x n ($0 \leq n \leq 9$)
Basic performance	Instruction execution	Min. 1 cycle
	Inter-register operation	Min. 2 cycles
	Load / store	Min. 2 cycles
	Conditional branch	2 to 3 cycles
Pipeline	3-stage (instruction fetch, decode, execution)	
Address space	256 KB (max. 64 KB for data)	
External bus	Address	18-bit (max.)
	Data	8-bit
	Minimum bus cycle	1 system clock cycle
Interrupt	Vector interrupt	3 interrupt levels
Low-power dissipation mode	STOP mode HALT mode	

2-1-1 Block Diagram



Clock generator	Uses a clock oscillator circuit driven by an external crystal or ceramic resonator to supply clock signals to CPU blocks.
Program counter	Generates addresses for the instructions to be inserted into the instruction queue. Normally incremented by sequencer indication, but may be set to branch destination address or ALU operation result when branch instructions or interrupts occur.
Instruction queue	Stores up to 2 bytes of pre-fetched instructions.
Instruction decoder	Decodes the instruction queue, sequentially generates the control signals needed for instruction execution, and executes the instruction by controlling the blocks within the chip.
Instruction execution controller	Controls CPU block operations in response to the result decoded by the instruction decoder and interrupt requests.
ALU	Executes arithmetic operations, logic operations, shift operations, and calculates operand addresses for register relative indirect addressing mode.
Internal ROM, RAM	Assigned to the execution program, data and stack region.
Address register	Stores the addresses specifying memory for data transfer. Stores the base address for register relative indirect addressing mode.
Data register	Holds data for operations. Two 8-bit registers can be connected to form a 16-bit register.
Interrupt controller	Detects interrupt requests from peripheral functions and requests CPU shift to interrupt processing.
Bus controller	Controls connection of CPU internal bus and CPU external bus. Includes bus usage arbitration function.
Internal peripheral functions	Includes peripheral functions (timer, serial interface, A/D converter, D/A converter, etc.) Peripheral functions vary with model.

Figure 2-1-1 Block Diagram and Function

2-1-2 CPU Control Registers

This LSI locates the peripheral circuit registers in memory space (x'03F00' to x'03FFF') with memory-mapped I/O. CPU control registers are also located in this memory space.

Table 2-1-2 CPU Control Registers

Registers	Address	R/W	Function	Pages
CPUM	x'03F00'	R/W *1	CPU mode control register	II - 21,25
MEMCTR	x'03F01'	R/W	Memory control register	II - 16
RCCTR	x'03F0E'	R/W	ROM correction control register	II - 32
SBNKR	x'03F0A'	R/W	Bank register for source address	II - 28
DBNKR	x'03F0B'	R/W	Bank register for destination address	II - 28
OSCMD	x'03F2D'	R/W	Oscillation frequency control register	II - 25
RCnAP	x'03FC7' to x'03FCF'	R/W	ROM correction address setting register	II - 33, 34
Reserved	x'03FE0'	-	For debugger	-
NMICR	x'03FE1'	R/W	Non - maskable interrupt control register [☞ Chapter 3]	III - 16
xxxICR	x'03FE2' to x'03FFE'	R/W	Maskable interrupt control register [☞ Chapter 3]	III - 17 to 37
Reserved	x'03FFF'	-	Reserved (For reading interrupt vector data on interrupt process)	-

R/W : Readable / Writable

*1 a part of bit is only readable

2-1-3 Instruction Execution Controller

The instruction execution controller consists of four blocks: memory, instruction queue, instruction registers, and instruction decoder.

Instructions are fetched in 1-byte units, and temporarily stored in the 2-byte instruction queue. Transfer is made in 1-byte or half-byte units from the instruction queue to the instruction register to be decoded by the instruction decoder.

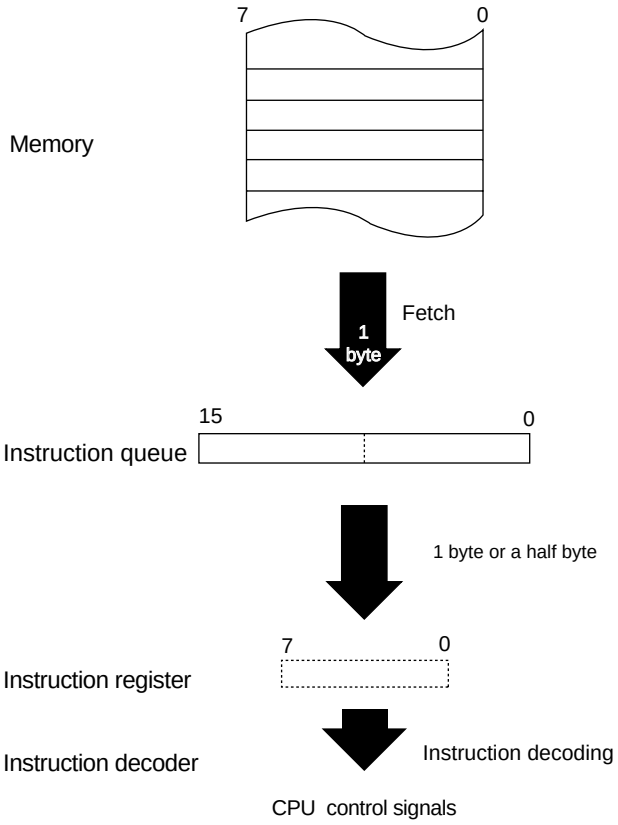


Figure 2-1-2 Instruction Execution Controller Configuration

2-1-4 Pipeline Process

Pipeline process means that reading and decoding are executed at the same time on different instructions, then instructions are executed without stopping. Pipeline process makes instruction execution continual and speedy. This process is executed with instruction queue and instruction decoder.

Instruction queue is buffer that fetches the second instruction in advance. That is controlled to fetch the next instruction when instruction queue is empty at each cycle on execution. At the last cycle of instruction execution, the first word (operation code) of executed instruction is stored to instruction register. At that time, the next operand or operation code is fetched to instruction queue, so that the next instruction can be executed immediately, even if register direct (da) or immediate (imm) is needed at the first cycle of the next instruction execution. But on some other instruction such as branch instruction, instruction queue becomes empty on the time that the next operation code to be executed is stored to instruction register at the last cycle. Therefore, only when instruction queue is empty, and direct address (da) or immediate data (imm) are needed, instruction queue keeps waiting for a cycle.

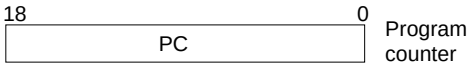
Instruction queue is controlled automatically by hardware so that there is no need to be controlled by software. But when instruction execution time is estimated, operation of instruction queue should be into consideration. Instruction decoder generates control signal at each cycle of instruction execution by micro program control. Instruction decoder uses pipeline process to decode instruction queue at one cycle before control signal is needed.

2-1-5 Registers for Address

Registers for address include program counter (PC), address registers (A0, A1), and stack pointer (SP).

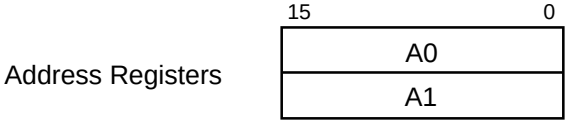
■Program Counter (PC)

This register gives the address of the currently executing instruction. It is 19 bits wide to provide access to a 256 KB address space in half byte(4-bit increments). The LSB of the program counter is used to indicate half byte instruction. The program counter after reset is stored from the value of vector table at the address of 4000.



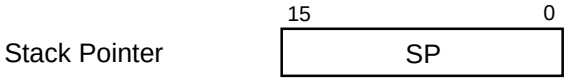
■Address Registers (A0, A1)

These registers are used as address pointers specifying data locations in memory. They support the operations involved in address calculations (i.e. addition, subtraction and comparison). Those pointers are 2 bytes data. Transfers between these registers and memory are always in 16-bit units. Either odd or even address can be transferred. At reset, the value of address register is undefined.



■Stack Pointer (SP)

This register gives the address of the byte at the top of the stack. It is decremented during push operations and incremented during pop operations. Ar reset, the value of SP is undefined.



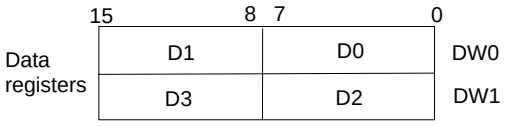
2-1-6 Registers for Data

Registers for data include four data registers (D0, D1, D2, D3).

■Data Registers (D0, D1, D2, D3)

Data registers D0 to D3 are 8-bit general-purpose registers that support all arithmetic, logical and shift operations. All registers can be used for data transfers with memory.

The four data registers may be paired to form the 16-bit data registers DW0 (D0+D1) and DW1 (D2+D3). At reset, the value of Dn is undefined.



2-1-7 Processor Status Word

Processor status word (PSW) is an 8-bit register that stores flags for operation results, interrupt mask level, and maskable interrupt enable. PSW is automatically pushed onto the stack when an interrupt occurs and is automatically popped when return from the interrupt service routine.

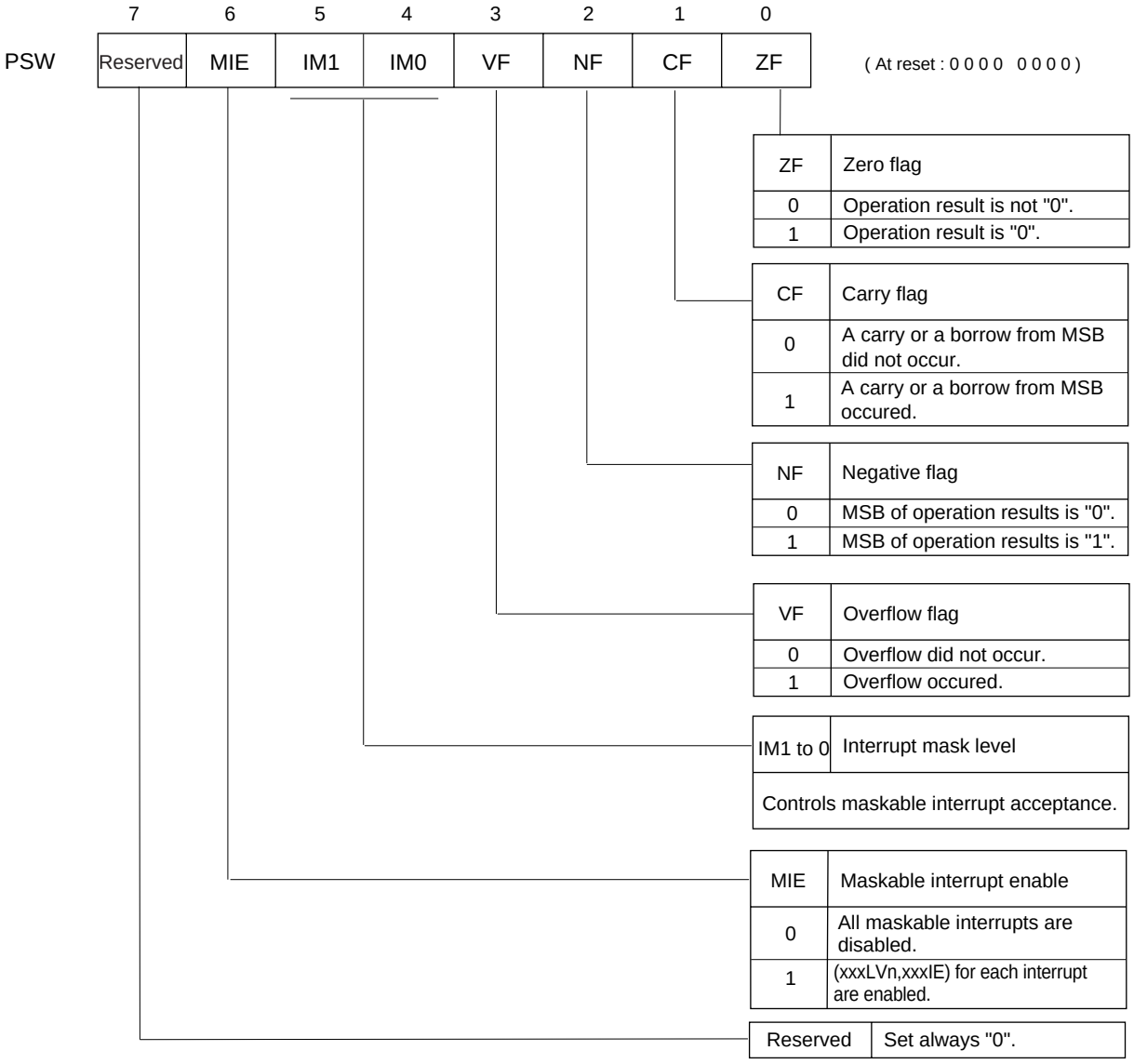


Figure 2-1-3 Processor Status Word(PSW)

■Zero Flag (ZF)
Zero flag (ZF) is set to "1", when all bits are '0' in the operation result. Otherwise, zero flag is cleared to "0".

■Carry Flag (CF)
Carry flag (CF) is set to "1", when a carry from or a borrow to the MSB occurs. Carry flag is cleared to "0", when no carry or borrow occurs.

■Negative Flag (NF)
Negative flag (NF) is set to "1" when MSB is '1' and reset to "0" when MSB is '0'. Negative flag is used to handle a signed value.

■Overflow Flag (VF)
Overflow flag (VF) is set to "1", when the arithmetic operation results overflow as a signed value. Otherwise, overflow flag is cleared to "0".
Overflow flag is used to handle a signed value.

■Interrupt Mask Level (IM1 and IM0)
Interrupt mask level (IM1 and IM0) controls the maskable interrupt acceptance in accordance with the interrupt factor interrupt priority for the interrupt control circuit in the CPU. The two-bit control flag defines levels '0' to '3'. Level 0 is the highest mask level. The interrupt request will be accepted only when the level set in the interrupt level flag (xxxLVn) of the interrupt control register (xxxICR) is higher than the interrupt mask level. When the interrupt is accepted, the level is reset to IM1-IM0, and interrupts whose mask levels are the same or lower are rejected during the accepted interrupt processing.

Table 2-1-3 Interrupt Mask Level and Interrupt Acceptance

	Interrupt mask level		Priority	Acceptable interrupt levels
	IM1	IM0		
Mask level 0	0	0	High	Non-maskable interrupt (NMI) only
Mask level 1	0	1	.	NMI, Level 0
Mask level 2	1	0	.	NMI, Level 0 to 1
Mask level 3	1	1	Low	NMI, Level 0 to 2

■Maskable Interrupt Enable (MIE)
Maskable interrupt enable flag (MIE) enables/disables acceptance of maskable interrupts by the CPU's internal interrupt acceptance circuit. A '1' enables maskable interrupts; a '0' disables all maskable interrupts regardless of the interrupt mask level (IM1-IM0) setting in PSW.
This flag is not changed by interrupts.

2-1-8 Addressing Modes

The MN101C77G series supports the nine addressing modes.

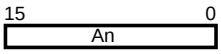
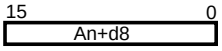
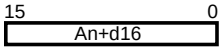
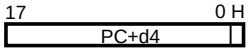
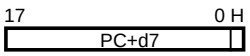
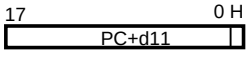
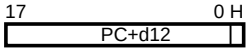
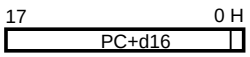
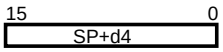
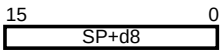
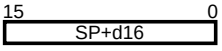
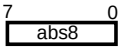
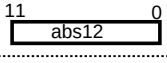
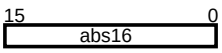
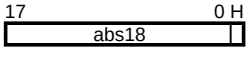
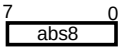
Each instruction uses a combination of the following addressing modes.

1) Register direct
2) Immediate
3) Register indirect
4) Register relative indirect
5) Stack relative indirect
6) Absolute
7) RAM short
8) I/O short
9) Handy

These addressing modes are well-suited for C language compilers. All of the addressing modes can be used for data transfer instructions. In modes that allow half-byte addressing, the relative value can be specified in half-byte (4-bit) increments, so that instruction length can be shorter. Handy addressing reuses the last memory address accessed and is only available with the MOV and MOVW instructions. Combining handy addresssing with absolute addressing reduces code size. For transfer data between memory, 7 addressing modes ; register indirect, register relative indirect, stack relative indirect, absolute, RAM short, I/O short, handy can be used. For operation instruction, register direct and immediate can be used. Refer to instruction's manual for the MN101C series.

This LSI is designed for 8-bit data access. It is possible to tranfer data in 16-bit increments with odd or all even addresses.

Table 2-1-4 Addressing Modes

Addressing mode		Effective address	Explanation
Register direct	Dn/DWn An/SP PSW	-	Directly specifies the register. Only internal registers can be specified.
Immediate	imm4/imm8 imm16	-	Directly specifies the operand or mask value appended to the instruction code.
Register indirect	(An)		Specifies the address using an address register.
Register relative indirect	(d8, An)		Specifies the address using an address register with 8-bit displacement.
	(d16, An)		Specifies the address using an address register with 16-bit displacement.
	(d4, PC) (branch instructions only)	 * 1	Specifies the address using the program counter with 4-bit displacement and H bit.
	(d7, PC) (branch instructions only)	 * 1	Specifies the address using the program counter with 7-bit displacement and H bit.
	(d11, PC) (branch instructions only)	 * 1	Specifies the address using the program counter with 11-bit displacement and H bit.
	(d12, PC) (branch instructions only)	 * 1	Specifies the address using the program counter with 12-bit displacement and H bit.
	(d16, PC) (branch instructions only)	 * 1	Specifies the address using the program counter with 16-bit displacement and H bit.
Stack relative indirect	(d4, SP)		Specifies the address using the stack pointer with 4-bit displacement.
	(d8, SP)		Specifies the address using the stack pointer with 8-bit displacement.
	(d16, SP)		Specifies the address using the stack pointer with 16-bit displacement.
Absolute	(abs8)		Specifies the address using the operand value appended to the instruction code. Optimum operand length can be used to specify the address.
	(abs12)		
	(abs16)		
	(abs18) (branch instructions only)	 * 1	
RAM short	(abs8)		Specifies an 8-bit offset from the address x'00000'.
I/O short	(io8)		Specifies an 8-bit offset from the top address (x'03F00') of the special function register area.
Handy	(HA)	-	Reuses the last memory address accessed and is only available with the MOV and MOVW instructions. Combined use with absolute addressing reduces code size.

* 1 H: half-byte bit

2-2 Memory Space

2-2-1 Memory Mode

ROM is the read only area and RAM is the memory area which contains readable/writable data. In addition to these, peripheral resources such as memory-mapped special registers are allocated. The MN101C series supports single chip mode in its memory model.

Table 2-2-1 Memory Mode Setup

Memory mode	MMOD pin	EXMEM flag in (MEMCTR register)	EXADV3 to 1 flag in (EXADV register)
Single chip mode	L	0	-

MMOD pin should be fixed to "L" level.

Set the CS1EXT flag of the memory area control register (AREACTR) to "0" in single-chip mode.

2-2-2 Single-chip Mode

In single-chip mode, the system consists of only internal memory. This is the optimized memory mode and allows construction of systems with the highest performance.

The single-chip mode uses only internal ROM and internal RAM. The MN101C series devices offer up to 12 KB of RAM and up to 240 KB of ROM. This LSI offers 3 KB of RAM and 48 KB of ROM.

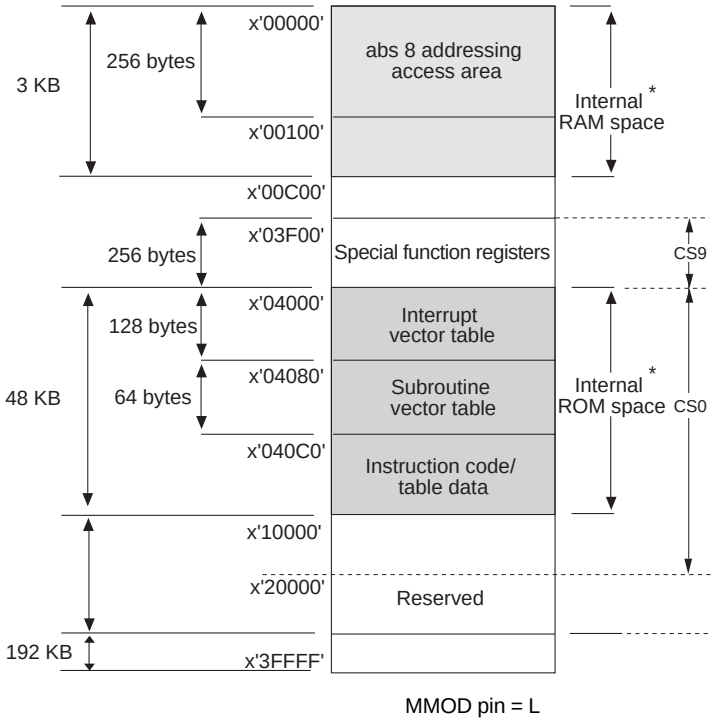


Figure 2-2-1 Single-chip Mode

* Differs depending upon the model. [☞ Table 2-2-2. Internal ROM/ Internal RAM]

Model	Internal ROM		Internal RAM	
	Address	bytes	Address	bytes
MN101C77C	X'04000' to X'0FFFF'	48 K	X'00000' to X'00BFF'	3 K
MN101CF77G	X'04000' to X'23FFF'	128 K	X'00000' to X'017FF'	6 K

Table 2-2-2. Internal ROM / Internal RAM

2-2-3 Special Function Registers

The MN101C series locates the special function registers (I/O spaces) at the addresses x'03F00' to x'03FFF' in memory space. The special function registers of this LSI are located as shown below.

Table 2-2-3 Register Map

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	
03F0X	CPUM	MEM CTR	WDCTR	AREACTR	Reserved	CSMD01	CSMD23	CSMD45	CSMD67	CSMD89	SBNKR	DBNKR	Reserved	Reserved	RCCTR	Reserved	CPU mode, memory control
03F1X	P0OUT	P1OUT	P2OUT			P5OUT	P6OUT	P7OUT	P8OUT					P8LED	P6SYO	Reserved	Port output
03F2X	P0IN	P1IN	P2IN			P5IN	P6IN	P7IN	P8IN		PAIN	KEYCNT		OSCMD	FLOAT	P1OMD	Port input
03F3X	P0DIR	P1DIR	P2DIR			P5DIR	P6DIR	P7DIR	P8DIR		PADIR		PAIMD	SC4ODC1	P6IMD	SC4ODC0	I/O mode control
03F4X	P0PLU	P1PLU	P2PLU			P5PLU	P6PLU	P7PLUD	P8PLU		PAPLUD		Reserved	DLYCTR	Reserved	Reserved	Resistor control
03F5X	TM0BC	TM1BC	TM0OC	TM1OC	TM0MD	TM1MD	CK0MD	CK1MD							Reserved	Reserved	Timer control
03F6X	TM4BC	TM5BC	TM4OC	TM5OC	TM4MD	TM5MD	CK4MD	CK5MD	TM6BC	TM6OC	TM6MD	TBCLR			RMCTR	PSCMD	
03F7X	TM7BCL	TM7BCH	TM7OC1L	TM7OC1H	TM7PR1L	TM7PR1H	TM7ICL	TM7ICH	TM7MD1	TM7MD2	TM7OC2L	TM7OC2H	TM7PR2L	TM7PR2H	P1TCNT	Reserved	
03F8X														NFCTR1	NFCTR0	EDGDT	Interrupt I/F control
03F9X	RXBUF0	TXBUF0	SC0MD0	SC0MD1	SC0MD2	SC0MD3	SC0ODC	SC0CKS	RXBUF1	TXBUF1	SC1MD0	SC1MD1	SC1MD2	SC1MD3	SC1ODC	SC1CKS	Serial I/F control
03FAX				SC4AD0	SC4AD1	SC4TXB		Reserved	SC3MD0	SC3MD1	SC3CTR	SC3TRB	SC4STR	SC4RXB	SC3ODC	SC3CKS	
03FBX	ANCTR0	ANCTR1	ANCTR2	ANBUF0	ANBUF1	Reserved					RC1APL	RC1APM	RC1APH	RC2APL	DACTR	DADR01	Analog I/F control
03FCX	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	RC0APL	RC0APM	RC0APH	RC1APL	RC1APM	RC1APH	RC2APL	RC2APM	RC2APH	ROM correction control
03FDX	AT1CNT0	AT1CNT1	AT1TRC	AT1 MAP0L	AT1 MAP0M	AT1 MAP0H	AT1 MAP1L	AT1 MAP1M	AT1 MAP1H								ATC control
03FEX	Reserved	NMICR	IRQ0ICR	IRQ1ICR	IRQ2ICR	IRQ3ICR	IRQ4ICR	Reserved		TM0ICR	TM1ICR	Reserved	Reserved	TM4ICR	TM5ICR	TM6ICR	Interrupt control
03FFX	TBICR	TM7ICR	T7OC2 ICR	SC4ICR	SC0RICR	SC0TICR	SC1RICR	SC1TICR	Reserved	SC3ICR	ADICR		ATC1ICR			Reserved	

Note) Do not access to the reserved registers with instructions.

2-3 Bus Interface

2-3-1 Bus Controller

The MN101C series provides separate buses to the internal memory and internal peripheral circuits to reduce bus line loads and thus realize faster operation.

There are three such buses: ROM bus, RAM bus, and peripheral expansion bus (I/O bus). They connect to the internal ROM, internal RAM, and internal peripheral circuits respectively. The bus control block controls the parallel operation of instruction read and data access. A functional block diagram of the bus controller is given below.

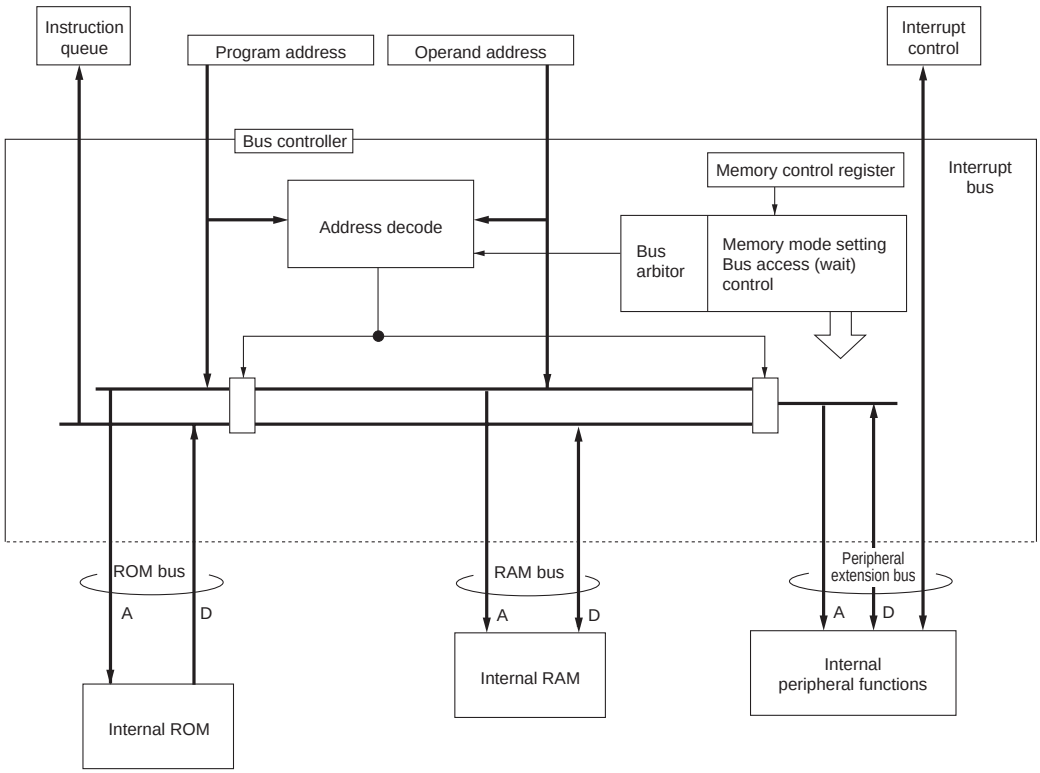


Figure 2-3-1 Functional Block Diagram of the Bus Controller

2-3-2 Control Registers

Bus interface is controlled by these 8 bytes of registers : the memory control register (MEMCTR), memory area control register (AREACTR) and bus mode control register (CSMDn).

■Memory Control Register (MEMCTR)

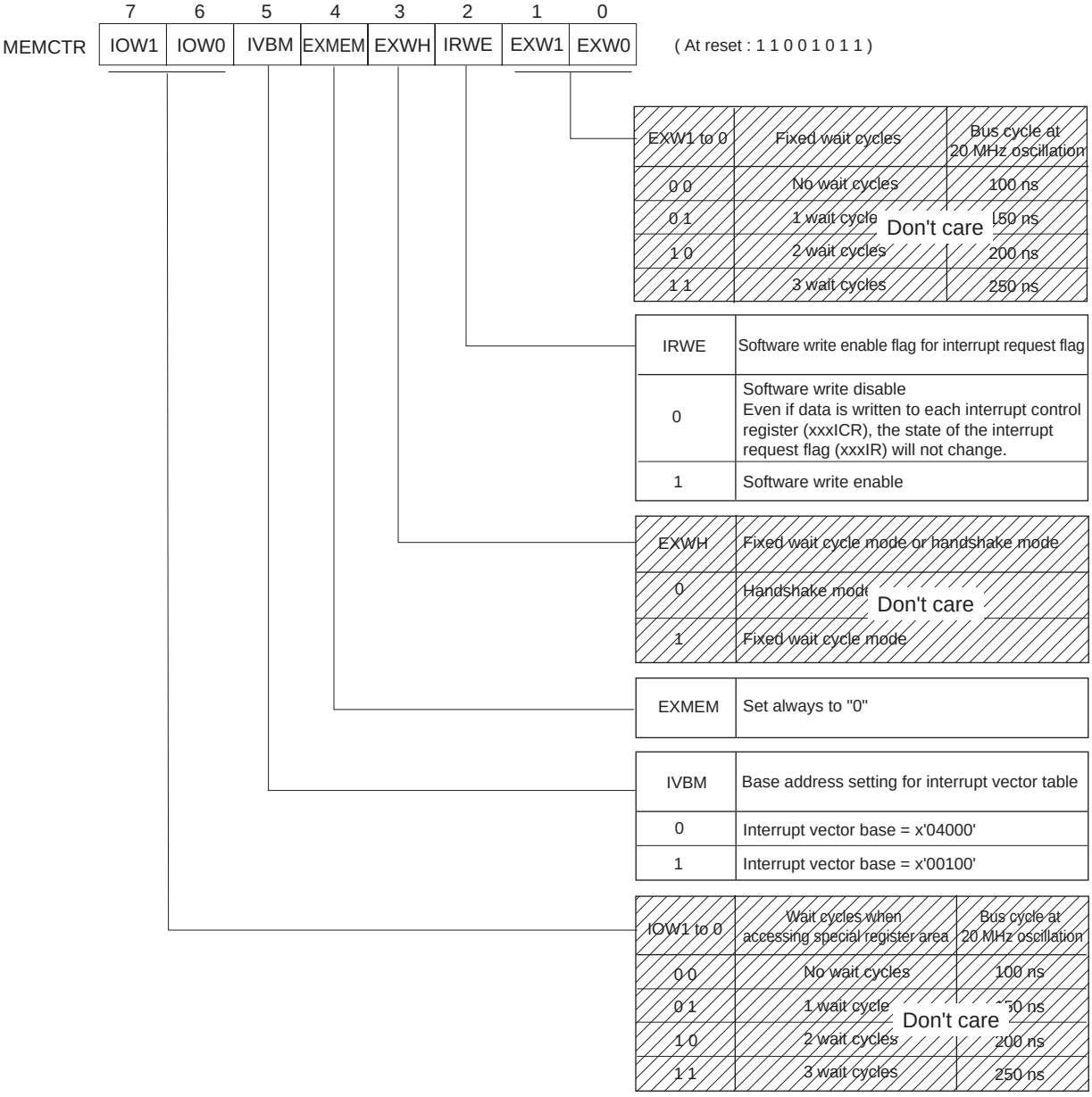


Figure 2-3-2 Memory Control Register (MEMCTR: x'03F01' R/W)

EXW1 to 0, EXWH and IOW1 to 0 flags of the memory control register (MEMCTR) need not to be set. Set wait cycle with bus mode control register (CSMDn).

■Memory Area Control Register (AREACTR)

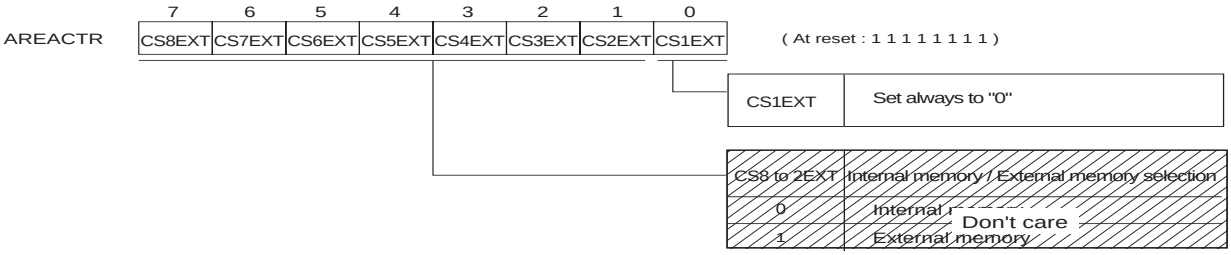


Figure 2-3-3 Memory Area Control Register (AREACTR : x'03F03', R/W)

In CS0 area, MMOD pin selects internal ROM/external memory. In CS9 area, only external memory can be selected as internal memory is not available.

> The MN101CF77 contains internal memory in CSI area. Therefore, set the CS1EXT flag of the memory area control register (AREACTR) to "0" . When CS1EXT flag is not set to "0", the data cannot be accessed to 112KB (x'04000' to x'1FFFF') of internal ROM space.

■Bus Mode Control Register (CSMDn)

	7	6	5	4	3	2	1	0	
CSMD01 (X'03F05')	CS1MD	CS1W2	CS1W1	CS1W0	-	CS0W2	CS0W1	CS0W0	(At reset: 0110-110)
CSMD23 (X'03F06')	CS3MD	CS3W2	CS3W1	CS3W0	CS2MD	CS2W2	CS2W1	CS2W0	(At reset: 01100110)
CSMD45 (X'03F07')	CS5MD	CS5W2	CS5W1	CS5W0	CS4MD	CS4W2	CS4W1	CS4W0	(At reset: 01100110)
CSMD67 (X'03F08')	CS7MD	CS7W2	CS7W1	CS7W0	CS6MD	CS6W2	CS6W1	CS6W0	(At reset: 01100110)
CSMD89 (X'03F09')	RESERVED	CS9W2	CS9W1	CS9W0	CS8MD	CS8W2	CS8W1	CS8W0	(At reset: 11100110)

Set always "1"

CSnW2 to 0	Wait mode selection
000	Fixed 0 wait mode
001	Fixed 1 wait mode
010	Fixed 2 wait mode
011	Fixed 3 wait mode
100	Fixed 4 wait mode
101	Fixed 5 wait mode
110	Fixed 6 wait mode
111	Handshake mode

CSnMD	Bus mode selection
0	101C bus mode
1	CSIC bus mode

Figure 2-3-4 Bus Mode Control Register (CSMDn : x'03F05' to x'03F09', R/W)

Select 101C bus mode for the area (CS1 to CS8) where internal memory is set with the memory area control register.

Only 101C bus mode is available in CS0 memory area, and only CSIC bus mode is available in CS9 memory area.

For the area where CSIC bus mode is selected with the bus mode control register (CSMDn), set always more than fixed 2 wait cycle and do not use fixed 0 or 1 wait cycle.

2-4 Standby Function

2-4-1 Overview

This LSI has two sets of system clock oscillator (high speed oscillation, low speed oscillation) for two CPU operating modes (NORMAL and SLOW), each with two standby modes (HALT and STOP). Power consumption can be decreased with using those modes.

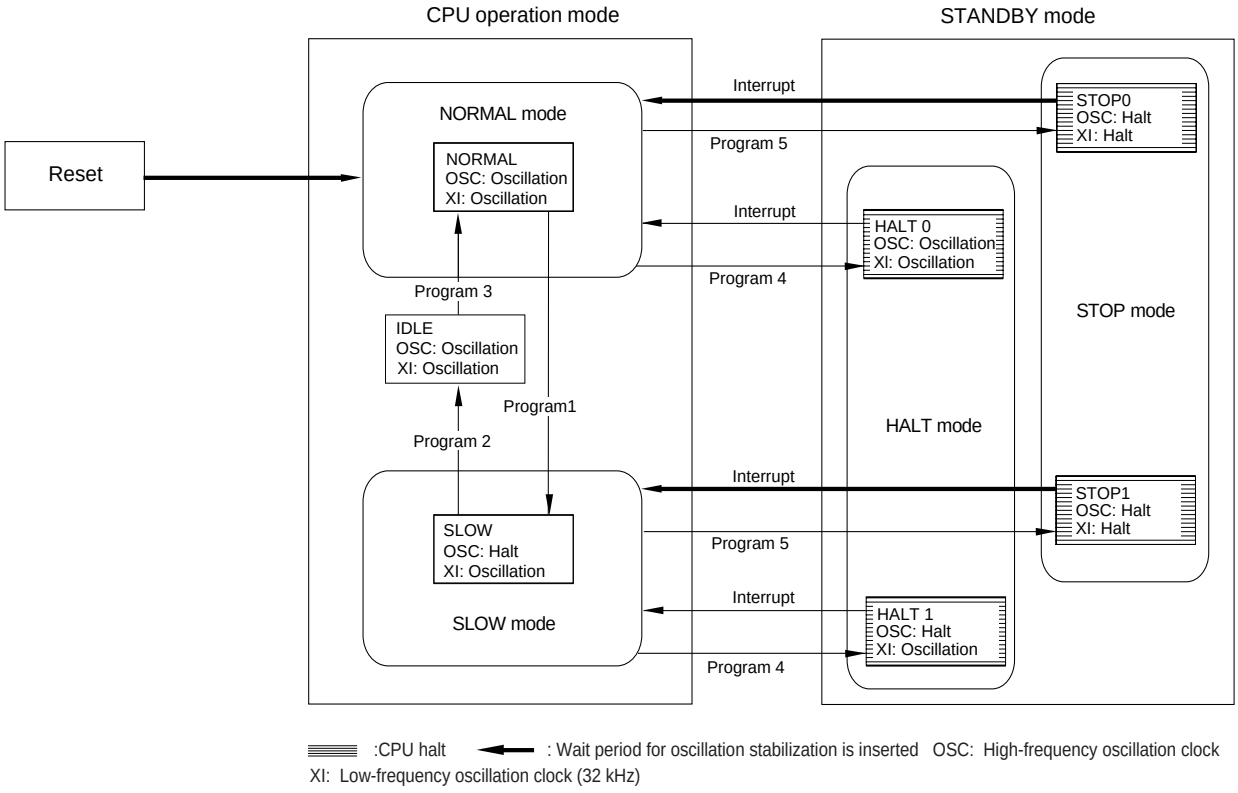


Figure 2-4-1 Transition Between Operation Modes

■HALT Modes (HALT0, HALT1)

– The CPU stops operating. But both of the oscillators remain operational in HALT0 and only the high-frequency oscillator stops operating in HALT1.
– An interrupt returns the CPU to the previous CPU operating mode that is, to NORMAL from HALT0 or to SLOW from HALT1.

■STOP Modes (STOP0, STOP1)

– The CPU and both of the oscillators stop operating.
– An interrupt restarts the oscillators and, after allowing time for them to stabilize, returns the CPU to the previous CPU operating mode - that is, to NORMAL from STOP0 or to SLOW from STOP1.

■SLOW Mode

– This mode executes the software using the low-frequency clock. Since the high-frequency oscillator is turned off, the device consumes less power while executing the software.

■IDLE Mode

– This mode allows time for the high-frequency oscillator to stabilize when the software is changing from SLOW to NORMAL mode.

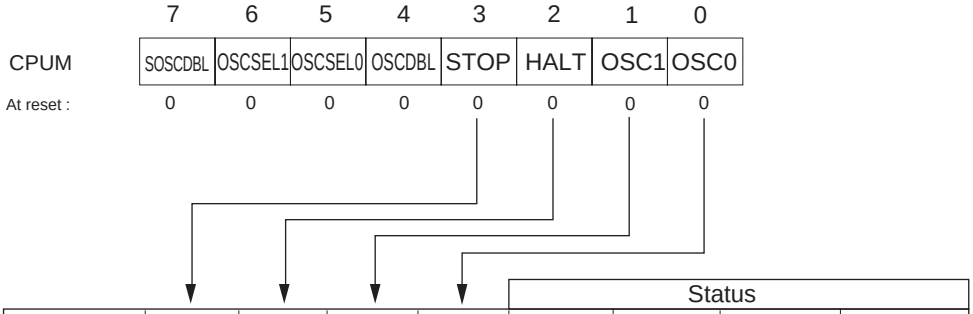
To reduce power dissipation in STOP and HALT modes, it is necessary to check the stability of both the output current from pins and port level of input pins. For output pins, the output level should match the external level or direction control should be changed to input mode. For input pins, the external level should be fixed.

This LSI has two system clock oscillation circuits. OSC is for high-frequency operation (NORMAL mode) and XI is for low-frequency operation (SLOW mode). Transition between NORMAL and SLOW modes or to standby mode is controlled by the CPU mode control register (CPUM). Reset and interrupts are the return factors from standby mode. A wait period is inserted for oscillation stabilization at reset and when returning from STOP mode, but not when returning from HALT mode. High/low-frequency oscillation mode is automatically returned to the same state as existed before entering standby mode.

To stabilize the synchronization at the moment of switching clock speed between high speed oscillation (fosc) and low speed oscillation (fx), fosc should be set to 2.5 times or higher frequency than fx.

2-4-2 CPU Mode Control Register

Transition from one mode to another mode is controlled by the CPU mode control register (CPUM).



Operation mode	STOP	HALT	OSC1	OSC0	Status: OSC1 /OSC0	Status: XI/XO	Status: System clock	Status: CPU
NORMAL	0	0	0	0	Oscillation	Oscillation	OSCI	Operating
IDLE	0	0	0	1	Oscillation	Oscillation	XI	Operating
SLOW	0	0	1	1	Halt	Oscillation	XI	Operating
HALT0	0	1	0	0	Oscillation	Oscillation	OSCI	Halt
HALT1	0	1	1	1	Halt	Oscillation	XI	Halt
STOP0	1	0	0	0	Halt	Halt	Halt	Halt
STOP1	1	0	1	1	Halt	Halt	Halt	Halt

Figure 2-4-2 Operating Mode and Clock Oscillation (CPUM : x'3F00', R/W)

The procedure for transition from NORMAL to HALT or STOP mode is given below.

(1) If the return factor is a maskable interrupt, set the MIE flag in the PSW to "1" and set the interrupt mask (IM) to a level permitting acceptance of the interrupt.
(2) Clear the interrupt request flag (xxxIR) in the maskable interrupt control register (xxxICR) , set the interrupt enable flag (xxxIE) for the return factor, and set the IE flag in the PSW.
(3) Set CPUM to HALT or STOP mode.

Set the IRWE flag of the memory control register (MEMCTR) to clear interrupt request flag by software.

System clock (fs) is changed depending on CPU operation mode.
In NORMAL mode, HALT0 mode, fs is based on fosc (high speed oscillation). In SLOW mode, IDLE mode, HALT1 mode, fs is based on fx (low speed oscillation).
[☞ Chapter 2. 2-5 Clock Switching]

2-4-3 Transition between SLOW and NORMAL

This LSI has two CPU operating modes, NORMAL and SLOW. Transition from SLOW to NORMAL requires passing through IDLE mode.

A sample program for transition from NORMAL to SLOW mode is given below.

```
Program 1
        MOV   x'3', D0          ; Set SLOW mode.
        MOV   D0, (CPUM)
```

Transition from NORMAL to SLOW mode, when the low-frequency clock has fully stabilized, can be done by writing to the CPU mode control register. In this case, transition through IDLE is not needed.

For transition from SLOW to NORMAL mode, the program must maintain the idle state until high-frequency clock oscillation is fully stable. In IDLE mode, the CPU operates on the low-frequency clock.

For transition from SLOW to NORMAL, oscillation stabilization waiting time is required same as that after reset. Software must count that time.
We recommend selecting the oscillation stabilization time after consulting with oscillator manufacturers.

Sample program for transition from SLOW to NORMAL mode is given below.

```
Program 2
                MOV         x'01', D0           ; Set IDLE mode.
                MOV         D0, (CPUM)
```

```
Program 3
        MOV     x'0B', D0       ; A loop to keep approx. 6.7 ms with low-frequency clock (32 kHz)
LOOP    ADD     -1, D0          ; operation when changed to high-frequency clock (20 MHz).
        BNE     LOOP            ;
        SUB     D0, D0          ;
        MOV     D0, (CPUM)      ;  Set NORMAL mode.
```

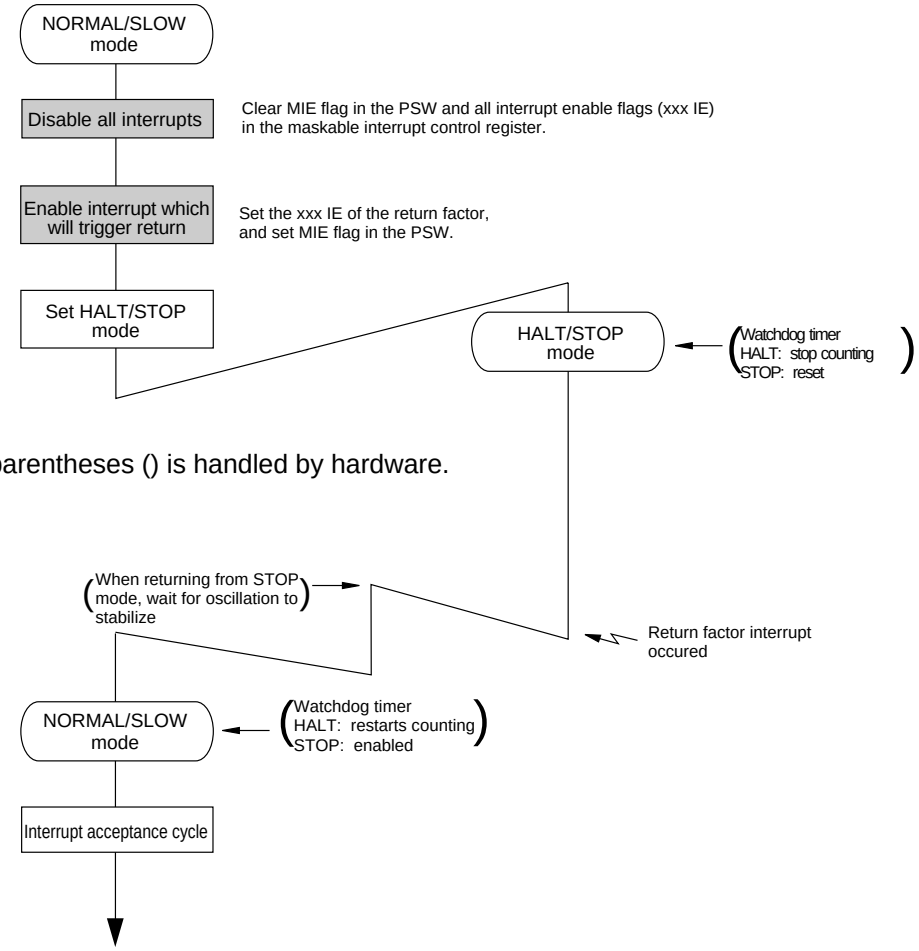
2-4-4 Transition to STANDBY Modes

The program initiates transitions from a CPU operating mode to the corresponding STANDBY (HALT/STOP) modes by specifying the new mode in the CPU mode control register (CPUM). Interrupts initiate the return to the former CPU operating mode.

Before initiating a transition to a STANDBY mode, however, the program must

(1) Set the maskable interrupt enable flag (MIE) in the processor status word (PSW) to '0' to disable all maskable interrupts temporarily.

(2) Set the interrupt enable flags (xxxIE) in the interrupt control registers (xxxICR) to '1' or '0' to specify which interrupts do and do not initiate the return from the STANDBY mode. Set MIE '1' to enable those maskable interrupts.



Processing inside parentheses () is handled by hardware.

Figure 2-4-3 Transition to/from STANDBY Mode

If the interrupt is enabled but interrupt priority level of the interrupt to be used is not equal to or higher than the mask level in PSW before transition to HALT or STOP mode, it is impossible to return to CPU operation mode by maskable interrupt.

■Transition to HALT modes

The system transfers from NORMAL mode to HALT0 mode, and from SLOW mode to HALT1 mode. The CPU stops operating, but the oscillators remain operational. There are two ways to leave a HALT mode: a reset or an interrupt. A reset produces a normal reset; an interrupt, an immediate return to the CPU state prior to the transition to the HALT mode. The watchdog timer, if enabled, resumes counting.

Program 4

```
        MOV     x'4',  D0      ; Set HALT mode.
        MOV     D0,  (CPUM)
        NOP                    ; After written in CPUM, some NOP
        NOP                    ; instructions (three or less) are
        NOP                    ; executed.
```

■Transition to STOP mode

The system transfers from NORMAL mode to STOP0 mode, and from SLOW mode to STOP1 mode. In both cases, oscillation and the CPU are both halted. There are two ways to leave a STOP mode: a reset or an interrupt.

Program 5

```
        MOV     x'8',  D0      ; Set STOP mode
        MOV     D0,  (CPUM)
        NOP                    ; After written in CPUM, some NOP
        NOP                    ; instructions (three or less) are
        NOP                    ; executed.
```

Right after the instruction of the transition to HALT, STOP mode, NOP instruction should be inserted 3 times.

2-5 Clock Switching

This LSI can select the best operation clock for system by switching clock cycle division factor by program. Division factor is determined by both flags of the CPU mode control register (CPUM) and the Oscillator frequency control register (OSCMD). At the highest-frequency, CPU can be operated in the same clock cycle to the external clock hence providing wider operating frequency range.

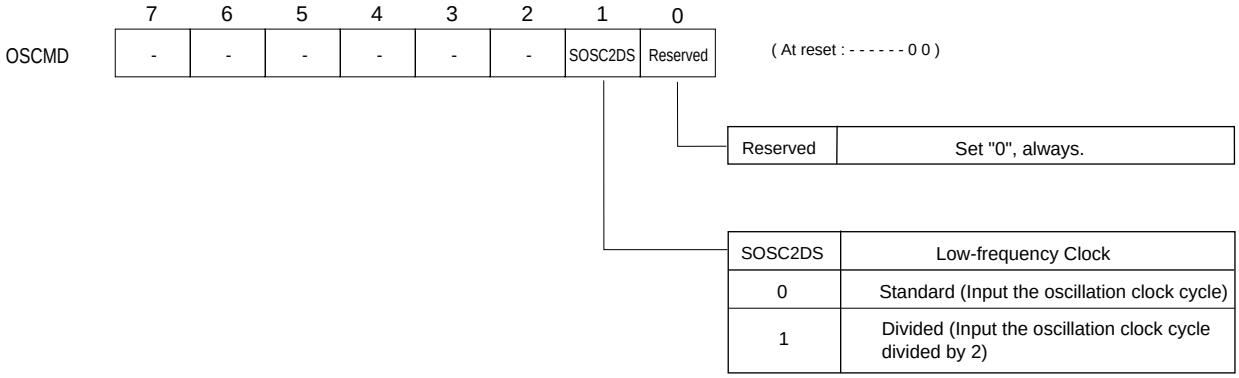


Figure 2-5-1 Oscillator Frequency Control Register (OSCMD : x'03F2D', R/W)

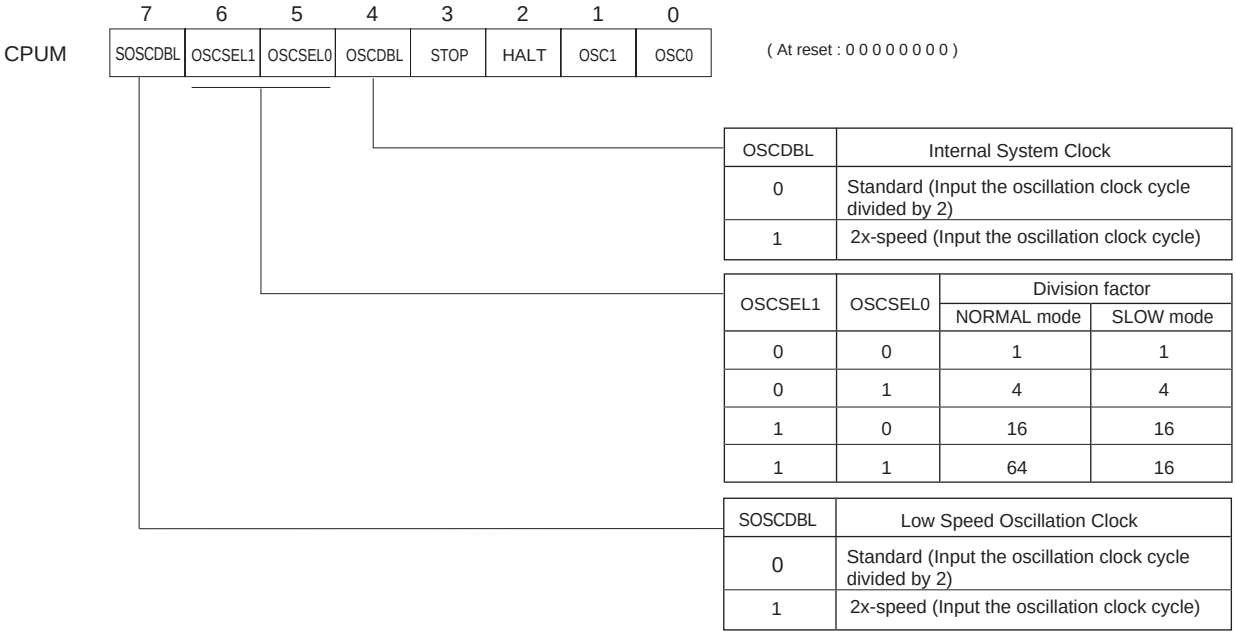


Figure 2-5-2 CPU Mode Control Register (CPUM : x'03F00', R/W)

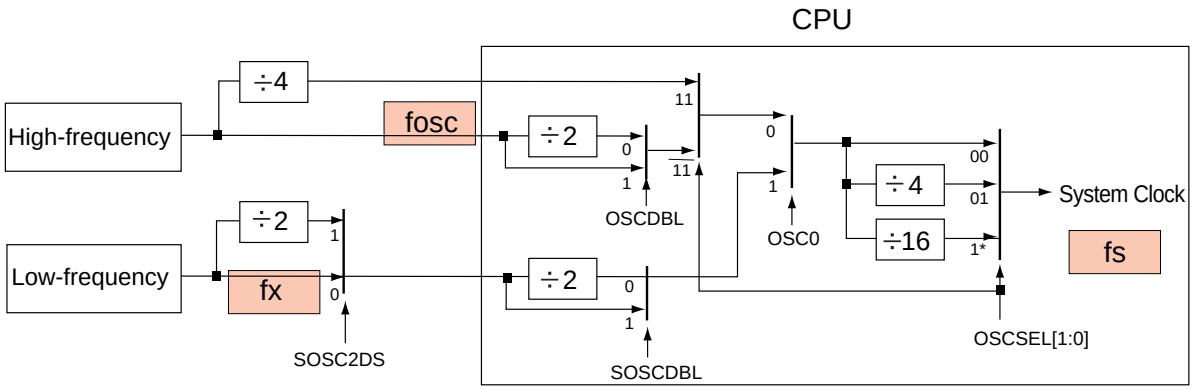


Figure 2-5-3 Clock Switching Circuit

OSCSEL1	OSCSEL0	OSCDBL	Division factor for High-frequency (OSC) Input (NORMAL mode)
0	0	0	2
0	0	1	1
0	1	0	8
0	1	1	4
1	0	0	32
1	0	1	16
1	1	0	64
1	1	1	64

Figure 2-5-4 Setting Division Factor at NORMAL mode by combination of OSCSEL and OSCDBL

OSCSEL1	OSCSEL0	SOSCDBL	SOSC2DS	Division factor for Low-frequency (XI / XO) Input (SLOW mode)
0	0	0	0	2
0	0	0	1	4
0	0	1	0	1
0	0	1	1	2
0	1	1	0	4

Figure 2-5-5 Setting Division Factor at SLOW mode by combination of OSCSEL and SOSC2DS

On clock switching, set each flag of OSCDBL, OSCSEL, SOSCSEL and OSC0, individually. Even if those flags are mapped on the same special functions register, set twice.

Set the OSC0 flag to "0" (NORMAL mode) before switching of division factor for low-frequency input.

Set the division factor in SLOW mode only to 1 to 4 division and do not set other values.

2-6 Bank Function

2-6-1 Overview

CPU of MN101C00 series has basically 64 KB memory address space. On this LSI, address space can be expanded up to 4 banks (256 KB) based on units of 64 KB, by bank function.

2-6-2 Bank Setting

Bank function can be used by setting the proper bank area to the bank register for source address (SBNKR) or the bank register for destination address (DBNKR). At reset, both of the SBNKR register and the DBNKR register indicate bank 0. Bank function is valid after setting any value except "00" to the SBNKR register or the DBNKR register.
When the both registers of SBNKR and DBNKR are operated at interrupt processing, pushing onto the stack or popping are necessary.

Table 2-6-1 Address Range

SBA1 (DBA1)	SBA0 (DBA0)	Bank area	Address range
0	0	Bank 0	x'00000' to x'0FFFF'
0	1	Bank 1	x'10000' to x'1FFFF'
1	0	Bank 2	x'20000' to x'2FFFF'
1	1	Bank 3	x'30000' to x'3FFFF'

When bank area is changed at interrupt processing, pushing onto the stack or popping must be done by program, if it necessary.

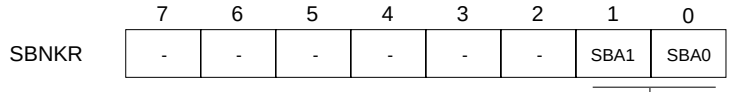
The stack area should be set in the area of bank 0, always. Furnished C compiler does not support bank function.

During bank function is valid, I/O short instruction should be used for access to the special function register area (x'03F00' to x'03FFF'). For access to the memory space x'13F00' to x'13FFF', x'23F00' to x'23FFF' and x'33F00' to x'33FFF', both instructions of register indirect and register relative indirect should be used. [☞ Chapter 2 2-1-8. Addressing Modes]

■Bank Register for Source Address

The SBNKR register is used to specify bank area for loading instruction from memory to register. Once this register is specified, bank control is valid for all addressing modes except I/O short instruction and stack relative indirect instruction.

[☞ Chapter 2 2-1-8. Addressing modes]



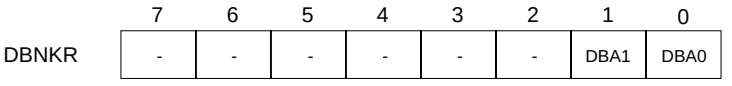
SBA1	SBA0	Bank for source address selection
0	0	bank 0
0	1	bank 1
1	0	bank 2
1	1	bank 3

Figure 2-6-1 Bank Register for Source Address (SBNKR:x'03F0A', R/W)

■Bank Register for Destination Address

The DBNKR register is used to specify bank area for storing instruction from register to memory. Once this register is specified, bank control is valid for all addressing modes except I/O short instruction,stack relative indirect instruction and bit manipulation instruction.

[☞ Chapter 2 2-1-8. Addressing modes]



DBA1	DBA0	Bank for destination address selection
0	0	bank0
0	1	bank1
1	0	bank2
1	1	bank3

Figure 2-6-2 Bank Register for Destination Address (DBNKR:x'03F0B', R/W)

Read, modify, write instruction such as bit manipulation (BSET, BCLR, BTST) depend on the value of the SBNKR register, both of for reading and writing.

2-6-3 Bank Memory Space

When bank function is used, the memory space, where CPU can access as data, shows as the following hatched part.

■Single Chip Mode

In single chip mode used internal ROM and internal RAM, an expanded bank area (bank 1, 2 and a part of bank 3) is in the memory space of internal ROM. In the expanded bank area, reading out of table data is enable, but rewrite is disable.

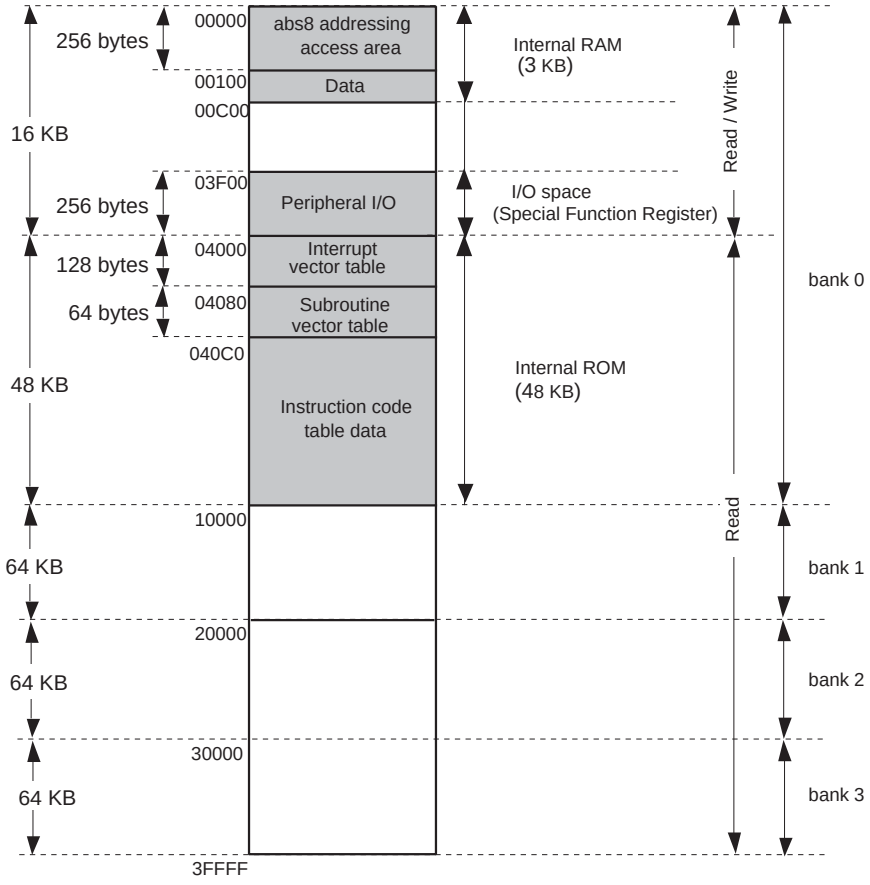


Figure 2-6-3 Single Chip Mode

Differs depending upon the model. [☞Table 2-2-2. Internal ROM/ Internal RAM]

2-7 ROM Correction

2-7-1 Overview

This LSI can correct and change max. 3 parts in a program on mask ROM with ROM correction function. The correct program is read from the external to the RAM space by using the external EEPROM or by using the serial transmission. This function is valid to the system with the external EEPROM.

2-7-2 Correction Sequence

Program is corrected as following steps.

(1) The instruction execution address is compared to the correction address.
(2) Program counter is branched indirectly to the RAM address (the head address of the correct program) stored to the RC vector table (RCnV(L), RCnV(H)), after matching the above addresses. This instruction needs 6 cycle.
(3) The corrected program at the RAM area is executed.
(4) Program counter is branched back to the program at ROM area.

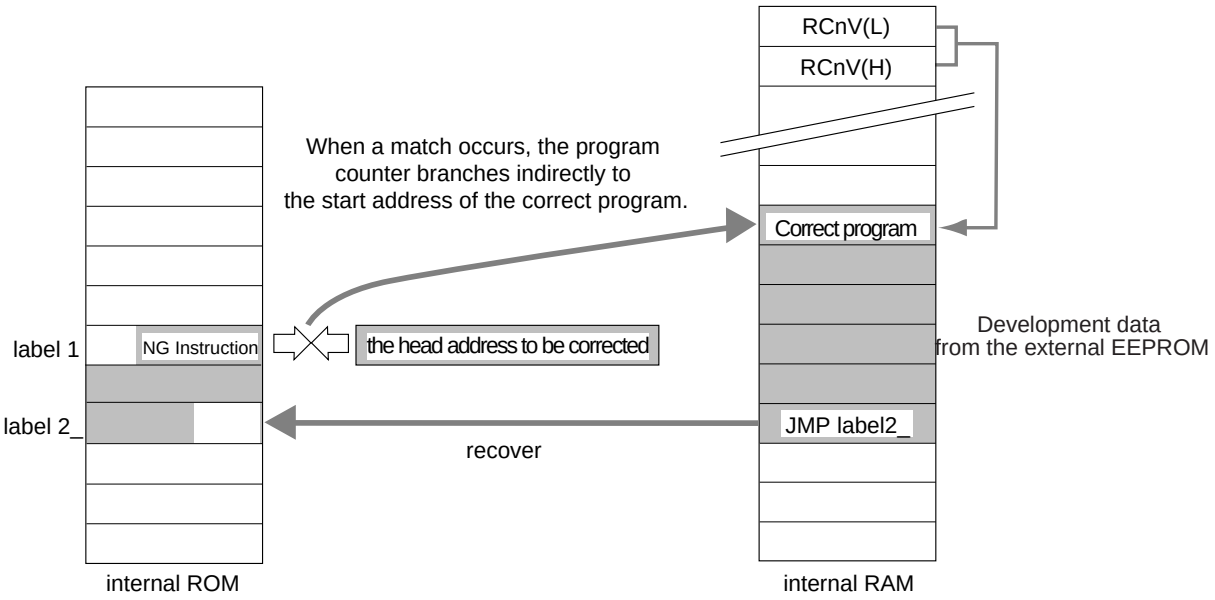


Figure 2-7-1 ROM Correction

The ROM correction setup procedure is as follows.

(1) Set the head address of the program to be corrected to the ROM correction address setting register (RCnAPH/M/L).
(2) Set the correct program at RAM area.
(3) Set the head address of the correct program to RC vector table (RCnV(L), RCnV(H)).
(4) Set the RCnEN flag of ROM correction control register (RCCTR) to enable the ROM correction.

When the instruction of the corrected program head address is the half-byte instruction, the ROM correction checks the execution instruction of the half-byte. Therefore, set the address by a byte to the ROM correction address setting register.

When the instruction of the corrected program last address is the half-byte instruction, the recover address should be set by half byte.

2-7-3 ROM Correction Control Register

ROM correction control register (RCCTR) and ROM correction address setting register (RCnAPL, RCnAPM, RCnAPH) control the ROM correction.

ROM correction control register (RCCTR) enables/disables the ROM correction function to 3 parts of the program to be corrected. When the RCnEN flag is set, the ROM correction is activated. And when the ROM address (the instruction execution address) reaches the set address to the ROM correction address setting register, it branches indirectly to the RAM address set on the RC vector table (RCnV(L), RCnV(H)). Set the RCnEN flag after setting the ROM correction address setting register.

■ROM Correction Control Register(RCCTR)

	7	6	5	4	3	2	1	0	
RCCTR	-	-	-	-	-	RC2EN	RC1EN	RC0EN	(At reset : - - - - - 0 0 0)

RC0EN	ROM correction control at 1st address
0	Disable
1	Enable

RC1EN	ROM correction control at 2nd address
0	Disable
1	Enable

RC2EN	ROM correction control at 3rd address
0	Disable
1	Enable

Figure 2-7-2 ROM Correction Control Regiser (RCCTR : x'03F0E', R/W)

This register set the head address, which instructions to be corrected are stored to. Once the instruction execution address reaches to the set value to this register, program counter branches indirectly to the set address to the RC vector table (RCnV(L), RCnV(H)). When the ROM correction should be valid, set the RCnEN flag of the ROM correction control register (RCCTR) after setting the address to this register.

■ROM Correction Address 0 Setting Register (RC0AP)

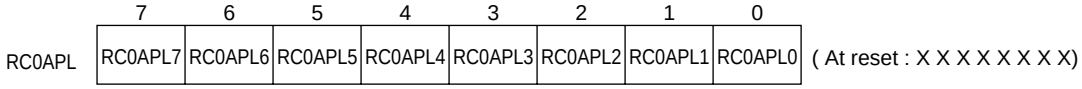


Figure 2-7-3 ROM Correction Address 0 Setting Register (lower 8 bits) (RC0APL : x'03FC7', R/W)

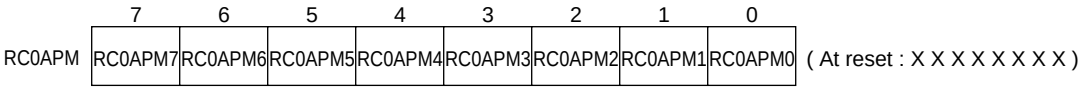


Figure 2-7-4 ROM Correction Address 0 Setting Register (middle 8 bits) (RC0APM : x'03FC8', R/W)

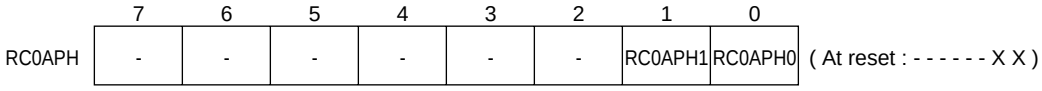


Figure 2-7-5 ROM Correction Address 0 Setting Register (upper 2 bits) (RC0APH : x'03FC9', R/W)

■ROM Correction Address 1 Setting Register (RC1AP)

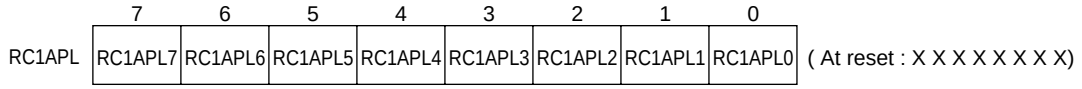


Figure 2-7-6 ROM Correction Address 1 Setting Register (lower 8 bits) (RC1APL : x'03FCA', R/W)

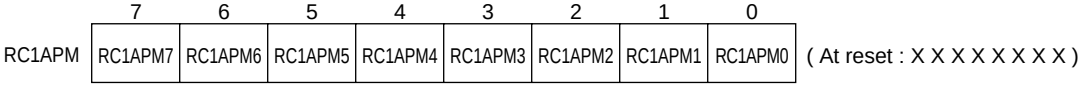


Figure 2-7-7 ROM Correction Address 1 Setting Register (middle 8 bits) (RC1APM : x'03FCB', R/W)

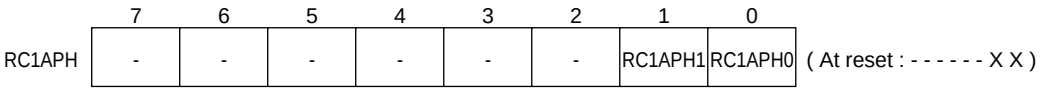


Figure 2-7-8 ROM Correction Address 1 Setting Register (upper 2 bits) (RC1APH : x'03FCC', R/W)

■ROM Correction Address 2 Setting Register (RC2AP)

	7	6	5	4	3	2	1	0	
RC2APL	RC2APL7	RC2APL6	RC2APL5	RC2APL4	RC2APL3	RC2APL2	RC2APL1	RC2APL0	(At reset : X X X X X X X X)

Figure 2-7-9 ROM Correction Address 2 Setting Register (lower 8 bits) (RC2APL : x'03FCD', R/W)

	7	6	5	4	3	2	1	0	
RC2APM	RC2APM7	RC2APM6	RC2APM5	RC2APM4	RC2APM3	RC2APM2	RC2APM1	RC2APM0	(At reset : X X X X X X X X)

Figure 2-7-10 ROM Correction Address 2 Setting Register (middle 8 bits) (RC2APM : x'03FCE', R/W)

	7	6	5	4	3	2	1	0	
RC2APH	-	-	-	-	-	-	RC2APH1	RC2APH0	(At reset : - - - - - - X X)

Figure 2-7-11 ROM Correction Address 2 Setting Register (upper 2 bits) (RC2APH : x'03FCF', R/W)

Do not set the same address to more than two RCnAP (H/M/L) register. If there are several registers set the same address, the order of priority is as follows :

RC0AP > RC1AP > RC2AP

Here is the correspondence of the ROM correction address setting register, a ROM correction control flag of ROM correction control register and the RC rector table.

Table 2-7-1 Correspondence

ROM Correction address setting register		ROM correction control flag	RC-vector table	
Register	Address		Vector	Address
RC0APL	x'3FC7'	RC0EN	RC0V(L)	x'0010'
RC0APM	x'3FC8'		RC0V(H)	x'0012'
RC0APH	x'3FC9'			
RC1APL	x'3FCA'	RC1EN	RC1V(L)	x'0014'
RC1APM	x'3FCB'		RC1V(H)	x'0011'
RC1APH	x'3FCC'			
RC2APL	x'3FCD'	RC2EN	RC2V(L)	x'0013'
RC2APM	x'3FCE'		RC2V(H)	x'0015'
RC2APH	x'3FCF'			

2-7-4 ROM Correction Setup Example

■Initial Routine with ROM Correction

The following routine should be set to correct the program. Also store the ROM correction setup and the correct program to the external EEPROM, in advance.

Here is the steps for ROM correction execution.

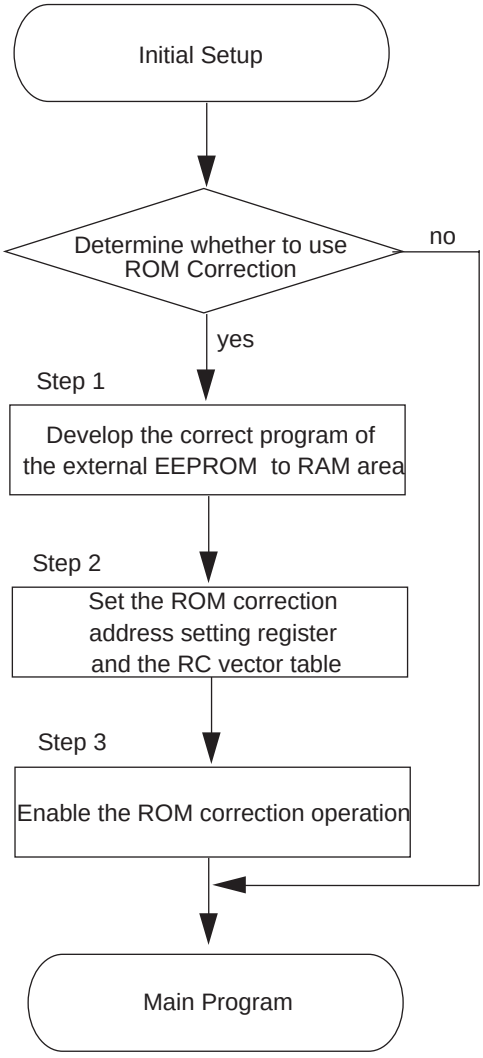
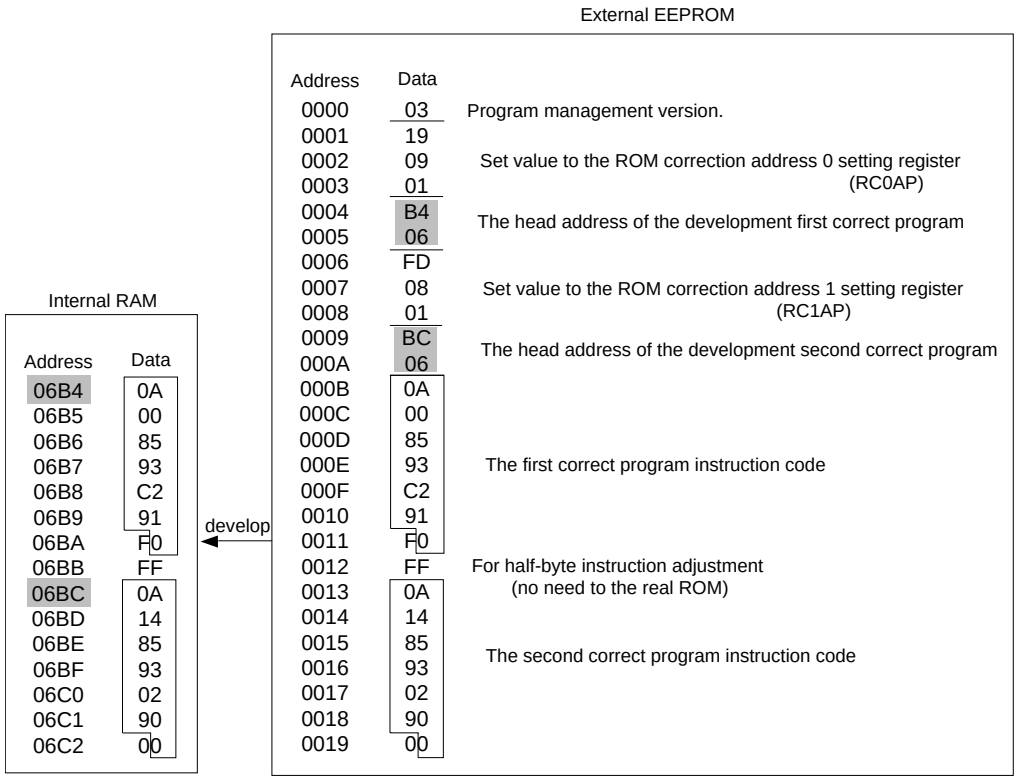


Figure 2-7-12 Initial Routine for ROM Correction

■ROM Correction Setup Example

The setup procedure with ROM correction to correct 2 parts of the program is shown below.
For the step to execute the ROM correction, refer to figure 2-7-12. Initial Routine for ROM correction on the previous page.

(STEP 1) Develop the correct program of the external EEPROM to RAM area.



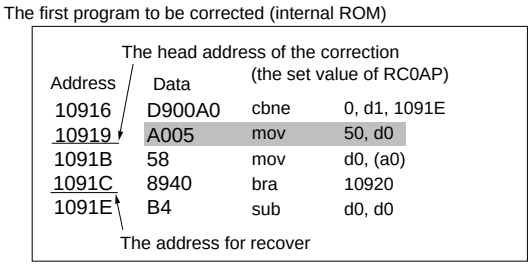
(STEP 2) Set the ROM correction address setting register and the RC vector table.

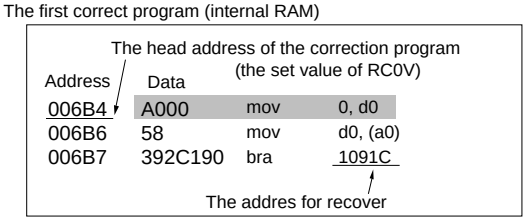
[Setup for the first correction]
Set the head address of the program to be corrected at first to the ROM correction address 0 setting register (RC0AP).

RC0APL = x'19'
RC0APM = x'09'
RC0APH = x'01'

Set the internal RAM address x'06B4' that stored the first correct program to the RC vector table address (RC0V(L), RC0V(H).

RC0V(L) = x'B4'
RC0V(H) = x'06'





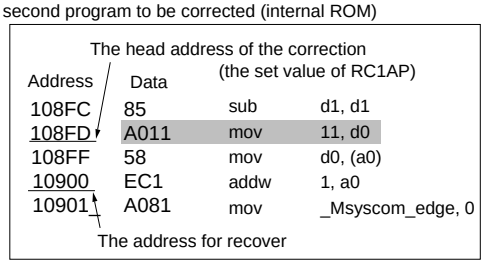
[Setup for the second correction]
Set the head address of the program to be corrected at second to the ROM correction address 1 setting register (RC1AP).

RC1APL = x'FD'
RC1APM = x'08'
RC1APH = x'01'

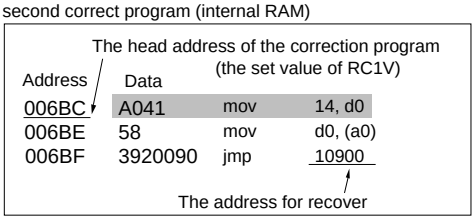
Set the internal RAM address x'06BC' that stored the second correct program to the RC vector table address (RC1V(L), RC1V(H).

RC1V(L) = x'BC'
RC1V(H) = x'06'

The second program to be corrected (internal ROM)



The second correct program (internal RAM)



(STEP 3) Set the bit 0 (RC0EN) and the bit 1 (RC1EN) of the ROM correction control register (RCCTR) to "1".

After the main program is started, the instruction fetched address and the set address to the ROM correction address setting register (RCnAP) are always compared, then once they are matched program counter indirectly branches to the address in RAM area, that are stored to the RC vector table (RCnV).

The correction program in RAM area is executed.

Program counter recovers to the program in ROM area.

2-8 Reset

2-8-1 Reset operation

The CPU contents are reset and registers are initialized when the NRST pin is pulled to low.

■Initiating a Reset

There are two methods to initiate a reset.

(1) Drive the NRST pin low.
NRST pin should be held "low" for more than OSC 4 clock cycles (200 ns at 20 MHz).

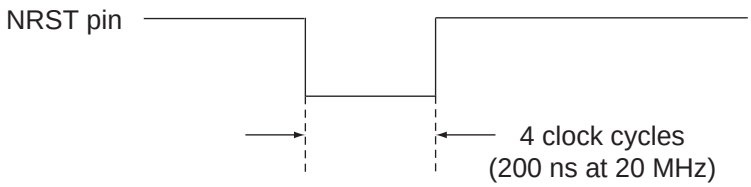


Figure 2-8-1 Minimum Reset Pulse Width

(2) Setting the P2OUT7 flag of the P2OUT register to "0" outputs low level at P27 (NRST) pin. And transferring to reset by program (software reset) can be executed. If the internal LSI is reset and register is initiated, the P2OUT7 flag becomes "1" and reset is released.
[☞ Chapter 4. 4-4-2 Registers]

On MN101C77 series, the starting mode is NORMAL mode that high oscillation is the base clock.

When NRST pin is connected to low power voltage detection circuit that gives pulse for enough low level time at sudeen unconnected. And reset can be generated even if NRST pin is held "low" for less than OSC 4 clock cycles, take notice of noise.

■Sequence at Reset

(1) When reset pin comes to high level from low level, the innternal 14-bit counter (It can be used as watchdog timer, too.) starts its operation by system clock. The period from starting its count from its overflow is called oscillation stabilization wait time.

(2) During reset, internal register and special function register are initiated.

(3) After oscillation stabilization wait time, internal reset is released and program is started from the address written at address X '4000' at interrupt rector table.

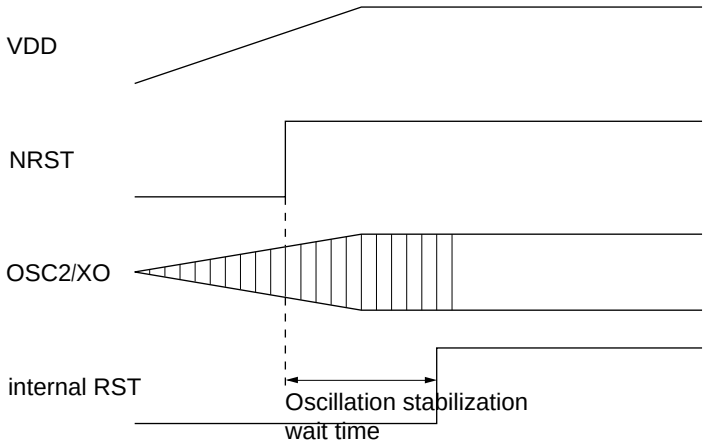


Figure 2-8-2 Reset Released Sequence

2-8-2 Oscillation Stabilization Wait time

Oscillation stabilization wait time is the period from the stop of oscillation circuit to the stablization for oscillation. Oscillation stabilization wait time is automatically inserted at releasing from reset and at recovering from STOP mode. At recovering from STOP mode the oscillation stabilization wait time control register (DLYCTR) is set to select the oscillation stabilization wait time. At releasing from reset, oscillation stabilization wait time is fixed.

The timer that counts oscillation stabilization wait time is also used as a watchdog timer. That is used as a runaway detective timer at anytime except at releasing from reset and at recovering from STOP mode. Watchdog timer is initiated at reset and at STOP mode and starts counting from the initialize value (x'0000') when system clock (fs) is as clock source. After oscillation stabilization wait time, it continues counting as a watchdog timer. [☞ Chapter 9 Watchdog timer]

■Block Diagram of Oscillation Stabilization Wait Time (watchdog timer)

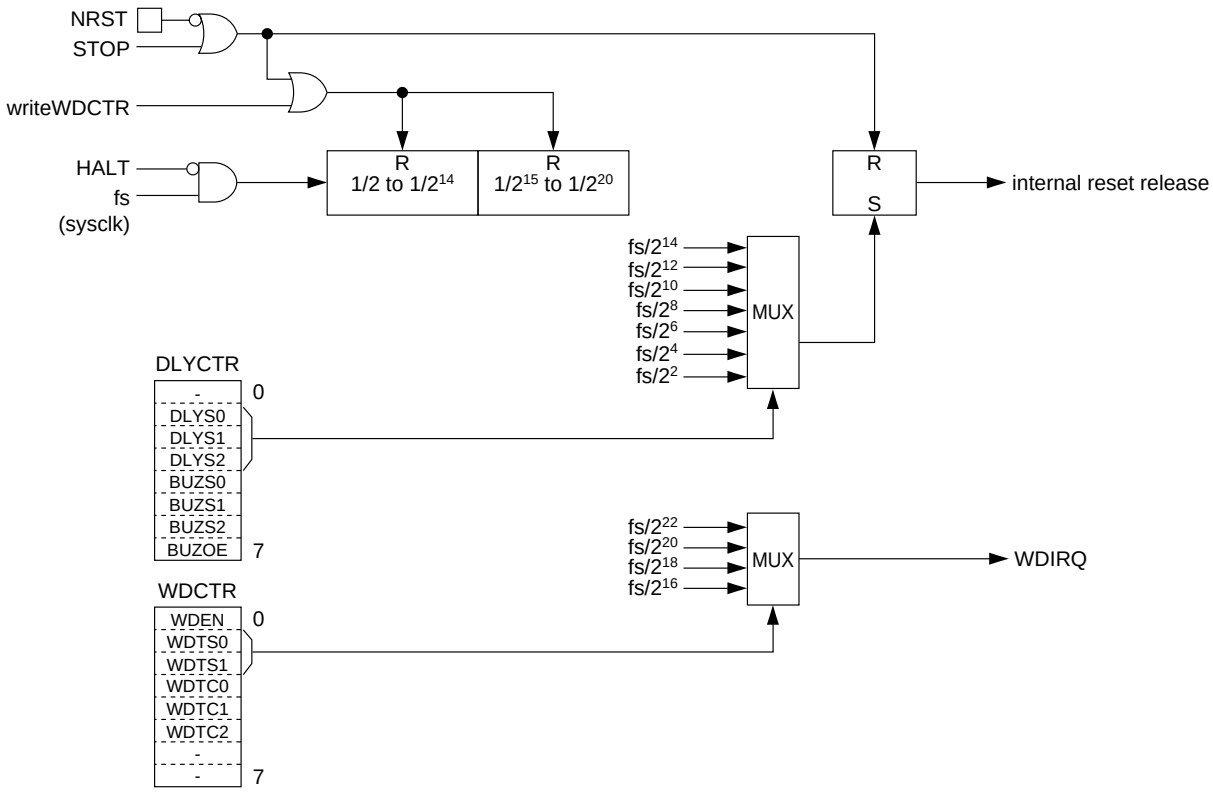


Figure 2-8-3 Block Diagram of Osillation Stabilization Wait Time (watchdog timer)

■Oscillation Stabilization Wait Time Control Register

	7	6	5	4	3	2	1	0
DLYCTR	BUZOE	BUZS2	BUZS1	BUZS0	DLYS2	DLYS1	DLYS0	-

(At reset: 0 0 0 0 0 0 0 -)

DLYS2	DLYS1	DLYS0	Oscillation stabilization wait period selection
0	0	0	$fs/2^{14}$
		1	$fs/2^{12}$
	1	0	$fs/2^{10}$
		1	$fs/2^{8}$
1	0	0	$fs/2^{6}$
		1	$fs/2^{4}$
	1	0	$fs/2^{2}$
		1	Reserved

Note : After reset is released, the oscillation stabilization wait period is fixed at $fs/2^{14}$.

BUZS2	BUZS1	BUZS0	Buzzer output frequency selection
0	0	0	$fosc/2^{14}$
		1	$fosc/2^{13}$
	1	0	$fosc/2^{12}$
		1	$fosc/2^{11}$
1	0	0	$fosc/2^{10}$
		1	$fosc/2^{9}$
	1	0	$fx/2^{4}$
		1	$fx/2^{3}$

BUZOE	P06 output selection
0	P06 port data output
1	P06 buzzer output

Figure 2-8-4 Oscillation Stabilization Wait Time Control Register (DLYCTR : x'03F4D', R/W)

■Control the Oscillation Stabilization Wait Time

At recovering from STOP mode, the bit 3-2 (DLYS1, DLYS0) of the oscillation stabilization wait time control register can be set to select the oscillation stabilization wait time from 2^{14}, 2^{10}, 2^{6}, 2^{2} x system clock. The DLYCTR register is also used for controlling of buzzer functions.

[☞ Chapter 10 Buzzer]

At releasing from reset, the oscillation stabilization wait time is fixed to "2^{14} x system clock". System clock is determined by the CPU mode control register (CPUM).

2-9 Register Protection

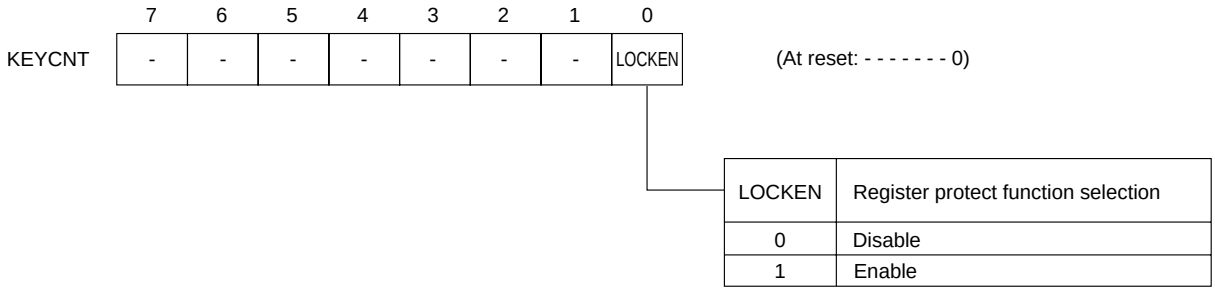
2-9-1 Overview

This LSI features a function to protect important register data. When this function is enabled, data is rewritten only when write is done for several times to a register and other write is disabled. Registers with this function are as follows.

CPU mode control register (CPUM: x'03F00')
Memory control register (MEMCTR: x'03F01')

2-9-2 Setting of the Register Protection Function

Set the L0CKEN flag of the key control register (KEYCNT) to "1" to enable the register protection function.



LOCKEN	Register protect function selection
0	Disable
1	Enable

Figure 2-9-1 Key Control Register (KEYCNT: x'03F2B', R/W)

2-9-3 Rewrite Procedure

Write 03 to the CPUM register:

```
LOOP    MOV   x'**',  (CPUM)
        MOV   x'03',  (CPUM)
        CBNE  x'03',  (CPUM),   LOOP
```

** indicates Don't care

・Interrupts may change the procedure of the program and disable sequence writes. Make sure that write is done properly or disable interrupts during write.
・Write to a register is executed even when several writes, which include access to RAM area (x'00000' to x'02FFF) are done.

Chapter 3 Interrupts

3-1 Overview

This LSI speeds up interrupt response with circuitry that automatically loads the branch address to the corresponding interrupt service routine from an interrupt vector table : reset, non-maskable interrupts (NMI), 16 maskable peripheral interrupts, and 5 external interrupts.

For interrupts other than reset, the interrupt processing sequence consists of interrupt request, interrupt acceptance, and hardware processing. After the interrupt is accepted, the program counter (PC) and processor status word (PSW) and handy addressing data (HA) are saved onto the stack. And an interrupts handler ends by restoring, using the POP instruction and other means, the contents of any registers used during processing and then executing the return from interrupt (RTI) instruction to return to the point at which execution was interrupted. Max.12 machine cycles before execution, and max 11 machine cycles after execution.

Each interrupt has an interrupt control register, which controls the interrupts. Interrupt control register consists of the interrupt level field (LV1-0), interrupt enable flag (IE), and interrupt request flag (IR).

Interrupt request flag (IR) is set to "1" by an interrupt request, and cleared to "0" by the interrupt acceptance. This flag is managed by hardware, but can be rewritten by software.

Interrupt enable flag (IE) is the flag that enables interrupts in the group. There is no interrupt enable flag in non-maskable interrupt (NMI). Once this interrupt request flag is set, it is accepted without any conditions. Interrupt enable flag is set in maskable interrupt. Interrupt enable flag (IE) of each maskable interrupt is valid when the maskable interrupt enable flag (MIE flag) of PSW is "1".

Maskable interrupts have had vector numbers by hardware, but their priority can be changed by setting interrupts level field. There are three hierarchical interrupt levels. If multiple interrupts have the same priority, the one with the lowest vector number takes priority. Maskable interrupts are accepted when its level is higher than the interrupt mask level (IM1-0) of PSW. Non-maskable interrupts are always accepted, regardless of the interrupt mask level.

3-1-1 Functions

Table 3-1-1 Interrupt Functions

Interrupt type	Reset (interrupt)	Non-maskable interrupt	Maskable interrupt
Vector number	0	1	2 to 28
Table address	x'04000'	x'04004'	x'04008' to x'04070'
Starting address	Address specified by vector address		
Interrupt level	-	-	Level 0 to 2 (set by software)
Interrupt factor	External RST pin input	Errors detection, PI interrupt	External pin input Internal peripheral function
Generated operation	Direct input to CPU core	Input to CPU core from non-maskable interrupt control register (NMICR)	Input interrupt request level set in interrupt level flag (xxxL Vn) of maskable interrupt control register (xxxICR) to CPU core.
Accept operation	Always accepts	Always accepts	Acceptance only by the interrupt control of the register (xxxICR) and the interrupt mask level in PSW.
Machine cycles until acceptance	12	12	12
PSW status after acceptance	All flags are cleared to "0".	The interrupt mask level flag in PSW is cleared to "00".	Values of the interrupt level flag (xxxLVn) are set to the interrupt mask level (masking all interrupt requests with the same or the lower priority.)

3-1-2 Block Diagram

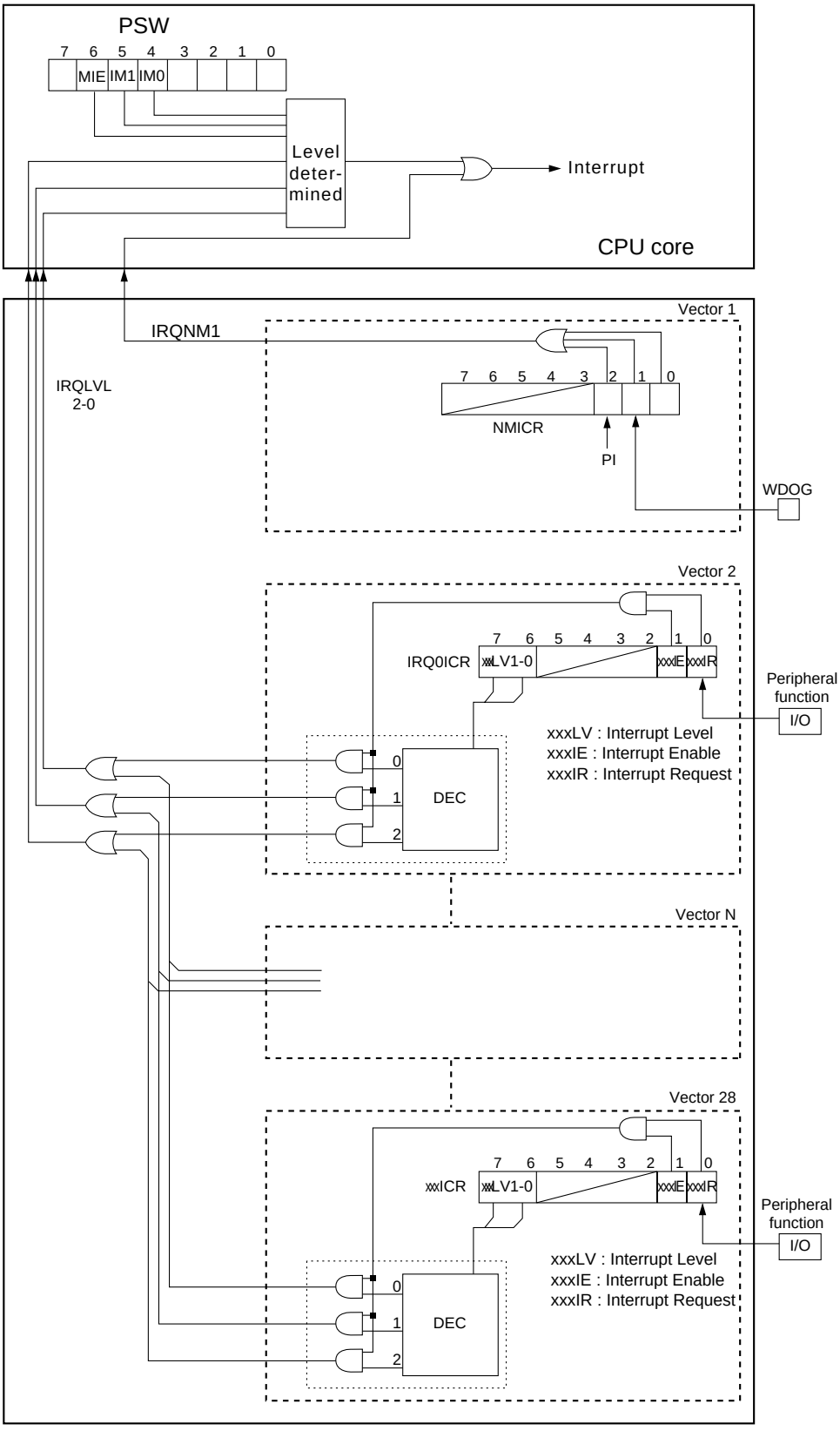


Figure 3-1-1 Interrupt Block Diagram

3-1-3 Operation

■Interrupt Processing Sequence

For interrupts other than reset, the interrupt processing sequence consists of interrupt request, interrupt acceptance, and hardware processing. The program counter (PC) and processor status word (PSW) and handy addressing data (HA) are saved onto the stack, and execution branches to the address specified by the corresponding interrupt vector.

An interrupt handler ends by restoring the contents of any registers used during processing and then executing the return from interrupt (RTI) instruction to return to the point at which execution was interrupted.

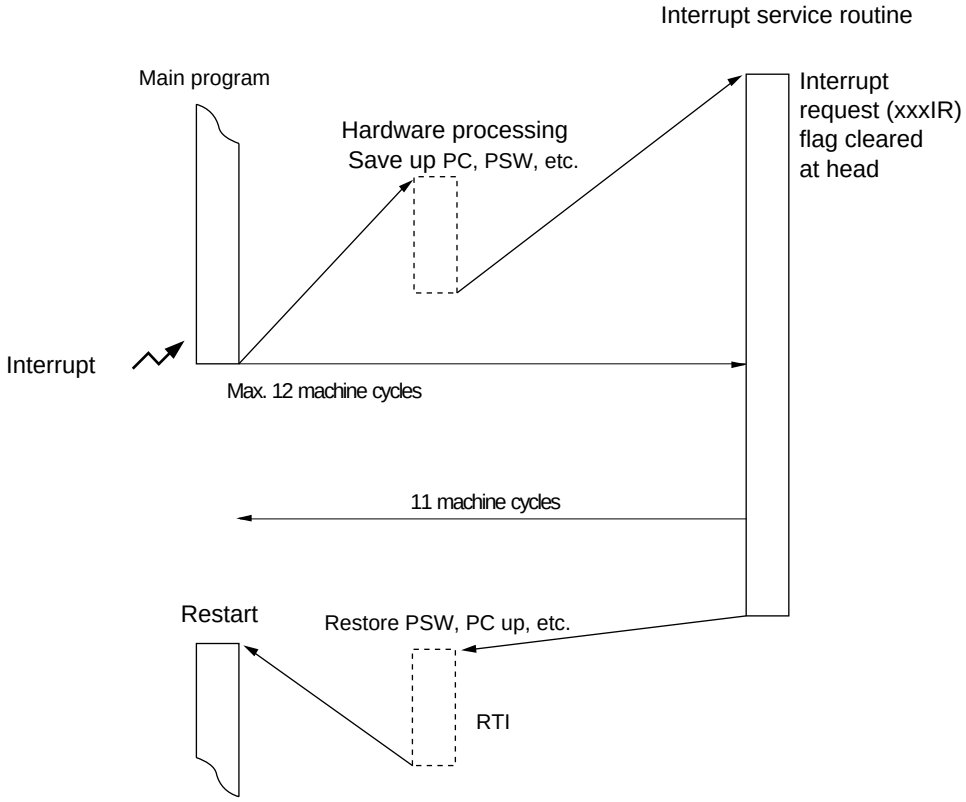


Figure 3-1-2 Interrupt Processing Sequence (maskable interrupts)

■Interrupt Sources and Vector Addresses

Here is the list of interrupt vector address and interrupt group.

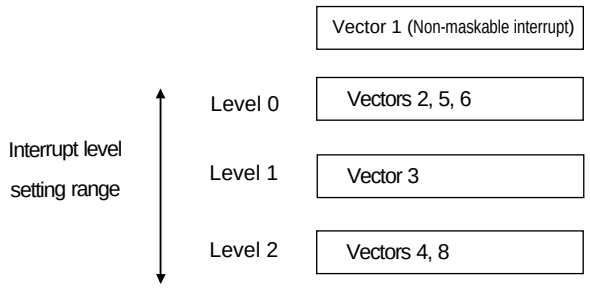
Table 3-1-2 Interrupt Vector Address and Interrupt Group

Vector Number	Vector Address	Interrupt group (Interrupt source)		Control Register (address)	
0	x'04000'	Reset	-	-	-
1	x'04004'	Non-maskable interrupt	NMI	NMICR	x'03FE1'
2	x'04008'	External interrupt 0	IRQ0	IRQ0ICR	x'03FE2'
3	x'0400C'	External interrupt 1	IRQ1	IRQ1ICR	x'03FE3'
4	x'04010'	External interrupt 2	IRQ2	IRQ2ICR	x'03FE4'
5	x'04014'	External interrupt 3	IRQ3	IRQ3ICR	x'03FE5'
6	x'04018'	External interrupt 4	IRQ4	IRQ4ICR	x'03FE6'
7	x'0401C'	Reserved	-	-	-
8	x'04020'	Reserved	-	-	-
9	x'04024'	Timer 0 interrupt	TM0IRQ	TM0ICR	x'03FE9'
10	x'04028'	Timer 1 interrupt	TM1IRQ	TM1ICR	x'03FEA'
11	x'0402C'	Reserved	-	-	-
12	x'04030'	Reserved	-	-	-
13	x'04034'	Timer 4 interrupt	TM4IRQ	TM4ICR	x'03FED'
14	x'04038'	Timer 5 interrupt	TM5IRQ	TM5ICR	x'03FEE'
15	x'0403C'	Timer 6 interrupt	TM6IRQ	TM6ICR	x'03FEF'
16	x'04040'	Time base interrupt	TBIRQ	TBICR	x'03FF0'
17	x'04044'	Timer 7 interrupt	TM7IRQ	TM7ICR	x'03FF1'
18	x'04048'	Timer 7 compare2-match	T7OC2IRQ	T7OC2ICR	x'03FF2'
19	x'0404C'	Serial interface 4 interrupt	SC4IRQ	SC4ICR	x'03FF3'
20	x'04050'	Serial interface 0 reception interrupt	SC0RIRQ	SC0RICR	x'03FF4'
21	x'04054'	Serial interface 0 transmission interrupt	SC0TIRQ	SC0TICR	x'03FF5'
22	x'04058'	Serial interface 1 reception interrupt	SC1RIRQ	SC1RICR	x'03FF6'
23	x'0405C'	Serial interface 1 transmission interrupt	SC1TIRQ	SC1TICR	x'03FF7'
24	x'04060'	Reserved	-	-	-
25	x'04064'	Serial interface 3 interrupt	SC3IRQ	SC3ICR	x'03FF9'
26	x'04068'	A/D converter interrupt	ADIRQ	ADICR	x'03FFA'
27	x'0406C'	Reserved	-	-	-
28	x'04070'	ATC1 interrupt	ATC1IRQ	ATC1ICR	x'03FFC'
29	x'04074'	Reserved	-	-	-
30	x'04078'	Reserved	-	-	-

For unused interrupts and reserved interrupts, set the address on which the RTI instruction is described to the corresponded address.

■Interrupt Level and Priority

This LSI allocated vector numbers and interrupt control registers (except reset interrupt) to each interrupt. The interrupt level (except reset interrupt, non-maskable interrupt) can be set by software, per each interrupt group. There are three hierarchical interrupt levels. If multiple interrupts have the same priority, the one with the lowest vector number takes priority. For example, if a vector 3 set to level 1 and a vector 4 set to level 2 request interrupts simultaneously, vector 3 interrupt will be accepted.



Priority	Interrupt vector No.
1	Vector 1
2	Vector 2
3	Vector 5
4	Vector 6
5	Vector 3
6	Vector 4
7	Vector 8

Figure 3-1-3 Interrupt Priority Outline

■Determination of Interrupt Acceptance

The following is the procedure from interrupt request input to acceptance.

(1) The interrupt request flag (xxxIR) in the corresponding external interrupt control register(IRQnICR) or internal interrupt control register (xxxICR) is set to '1'.

(2) An interrupt request is input to the CPU, If the interrupt enable flag (xxxIE) in the same register is '1'.

(3) The interrupt level (IL) is set for each interrupt. The interrupt level (IL) is input to the CPU.

(4) The interrupt request is accepted, if IL has higher priority than IM and MIE is '1
[☞ Chapter 2. 2-1-7 Processor Status Word]

(5) After the interrupt is accepted, the hardware resets the interrupt request flag (xxxIR) in the interrupt control register (xxxICR) to '0'.

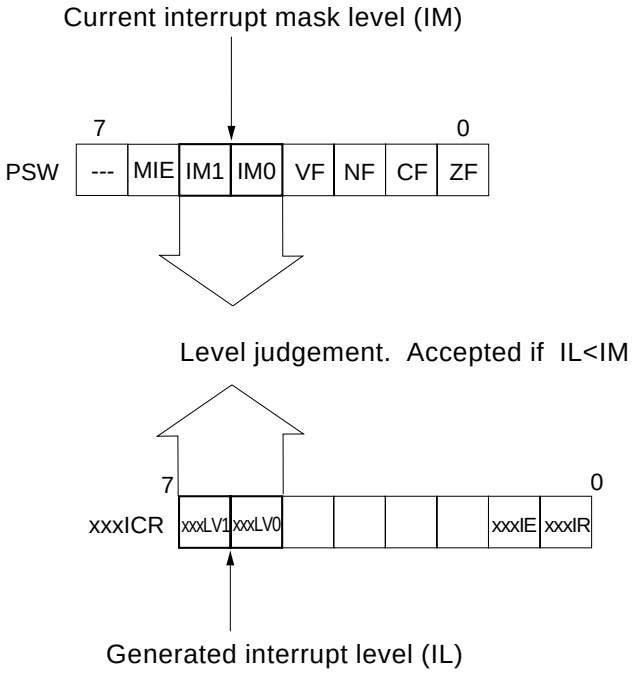


Figure 3-1-4 Determination of Interrupt Acceptance

The corresponding interrupt enable flag (xxxIE) is not cleared to "0", even if the interrupt is accepted.

When the setting is as xxxLV=1, XXXLV0=1, the interrupt of that vector is disabled, regardless of the value of xxxIE, xxxIR.

MIE='0' and interrupts are disabled when:

- MIE in the PSW is reset to '0' by a program
- Reset is detected

MIE='1' and interrupts are enabled when:

- MIE in the PSW is set to '1' by a program

The interrupt mask level (IM=IM1 - IM0) in the processor status word (PSW) changes when:

- The program alters it directly,
- A reset initializes it to 0 (00b),
- The hardware accepts and thus switches to the interrupt level (IL) for a maskable interrupt, or
- Execution of the RTI instruction at the end of an interrupt service routine restores the processor status word (PSW) and thus the previous interrupt mask level.

The maskable interrupt enable (MIE) flag in the processor status word (PSW) is not cleared to "0".

Non-maskable interrupts have priority over maskable ones.

■Interrupt Acceptance Operation

When accepting an interrupt, this LSI hardware saves the handy address register, the return address from the program counter, and the processor status word (PSW) to the stack and branches to the interrupt handler using the starting address in the vector table.

The following is the hardware processing sequence after by interrupt acceptance.

1. The stack pointer (SP) is updated.
   (SP-6 → SP)
2. The contents of the handy address register (HA) are saved to the stack.
   Upper half of HA → (SP+5)
   Lower half of HA → (SP+4)
3. The contents of the program counter (PC), the return address, are saved to the stack.
   PC bits 18, 17, and 0 → (SP+3)
   PC bits 16-9 → (SP+2)
   PC bits 8-1 → (SP+1)
4. The contents of the PSW are saved to the stack.
   PSW → (SP)
5. The interrupt level (xxxLVn) for the interrupt is copied to the interrupt mask (IMn) in the PSW.
   Interrupt level (xxxLVn) → IMn
6. The hardware branches to the address in the vector table.

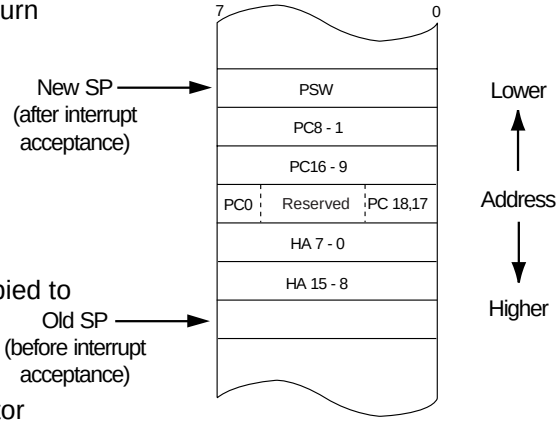


Figure 3-1-5 Stack Operation during interrupt acceptance

■Interrupt Return Operation

An interrupt handler ends by restoring, using the POP instruction and other means, the contents of any registers used during processing and then executing the return from interrupt (RTI) instruction to return to the point at which execution was interrupted.

The following is the processing sequence after the RTI instruction.

1. The contents of the PSW are restored from the stack. (SP)
2. The contents of the program counter (PC), the return address, are restored from the stack. (SP+1 to SP+3)
3. The contents of the handy address register (HA) are restored from the stack. (SP+4, SP+5)
4. The stack pointer is updated. (SP+6 → SP)
5. Execution branches to the address in the program counter.

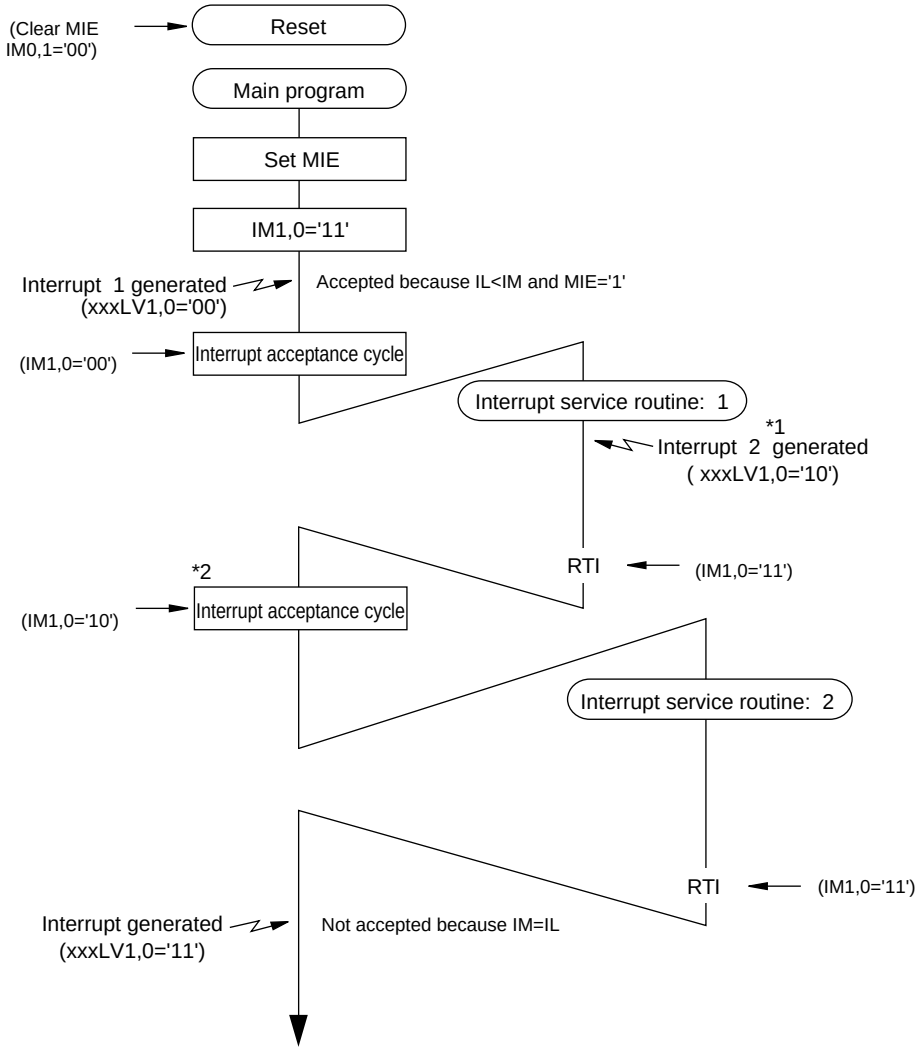
The handy address register is an internal register used by the handy addressing function. The hardware saves its contents to the stack to prevent the interrupt from interfering with operation of the function.

Registers such as data register, or address register are not saved, so that PUSH instruction should be used to save data register or address register onto the stack, if neccessary.

The address bp6 to bp2, when program counter (PC) are saved to the stack, are reserved. Do not change by program.

■Maskable Interrupt

Figure 3-1-6 shows the processing flow when a second interrupt with a lower priority level (xxxLV1-xxxLV0='10') arrives during the processing of one with a higher priority level (xxxLV1-xxxLV0='00').



Parentheses ( ) indicate hardware processing.

*1 If during the processing of the first interrupt, an interrupt request with an interrupt level (IL) numerically lower than the interrupt mask (IM) arrives, it is accepted as a nested interrupt. If IL ≥ IM, however, the interrupt is not accepted.

*2 The second interrupt, postponed because its interrupt level (IL) was numerically greater than the interrupt mask (IM) for the first interrupt service routine, is accepted when the first interrupt handler returns.

Figure 3-1-6 Processing Sequence for Maskable Interrupts

■Multiplex Interrupt

When an MN101C77 series device accepts an interrupt, it automatically disables acceptance of subsequent interrupts with the same or lower priority level. When the hardware accepts an interrupt, it copies the interrupt level (xxxLVn) for the interrupt to the interrupt mask (IM) in the PSW. As a result, subsequent interrupts with the same or lower priority levels are automatically masked. Only interrupts with higher priority levels are accepted. The net result is that interrupts are normally processed in decreasing order of priority. It is, however, possible to alter this arrangement.

1. To disable interrupt nesting
   - Reset the MIE bit in the PSW to "0."
   - Raise the priority level of the interrupt mask (IM) in the PSW.
2. To enable interrupts with lower priority than the currently accepted interrupt
   - Lower the priority level of the interrupt mask (IM) in the PSW.

Multiplex interrupts are only enabled for interrupts with levels higher than the PSW interrupt mask level (IM).

It is possible to forcibly rewrite IM to accept an interrupt with a priority lower than the interrupt being processed, but be careful of stack overflow.

Do not operate the maskable interrupt control register (xxxICR) when multiple interrupts are enabled. If operation is necessary, first clear the PSW MIE flag to disable interrupts.

Figure 3-1-7 shows the processing flow for multiple interrupts (interrupt 1: xxxLV1-xxxLV0='10', and interrupt 2: xxxLV1-xxxLV0='00').

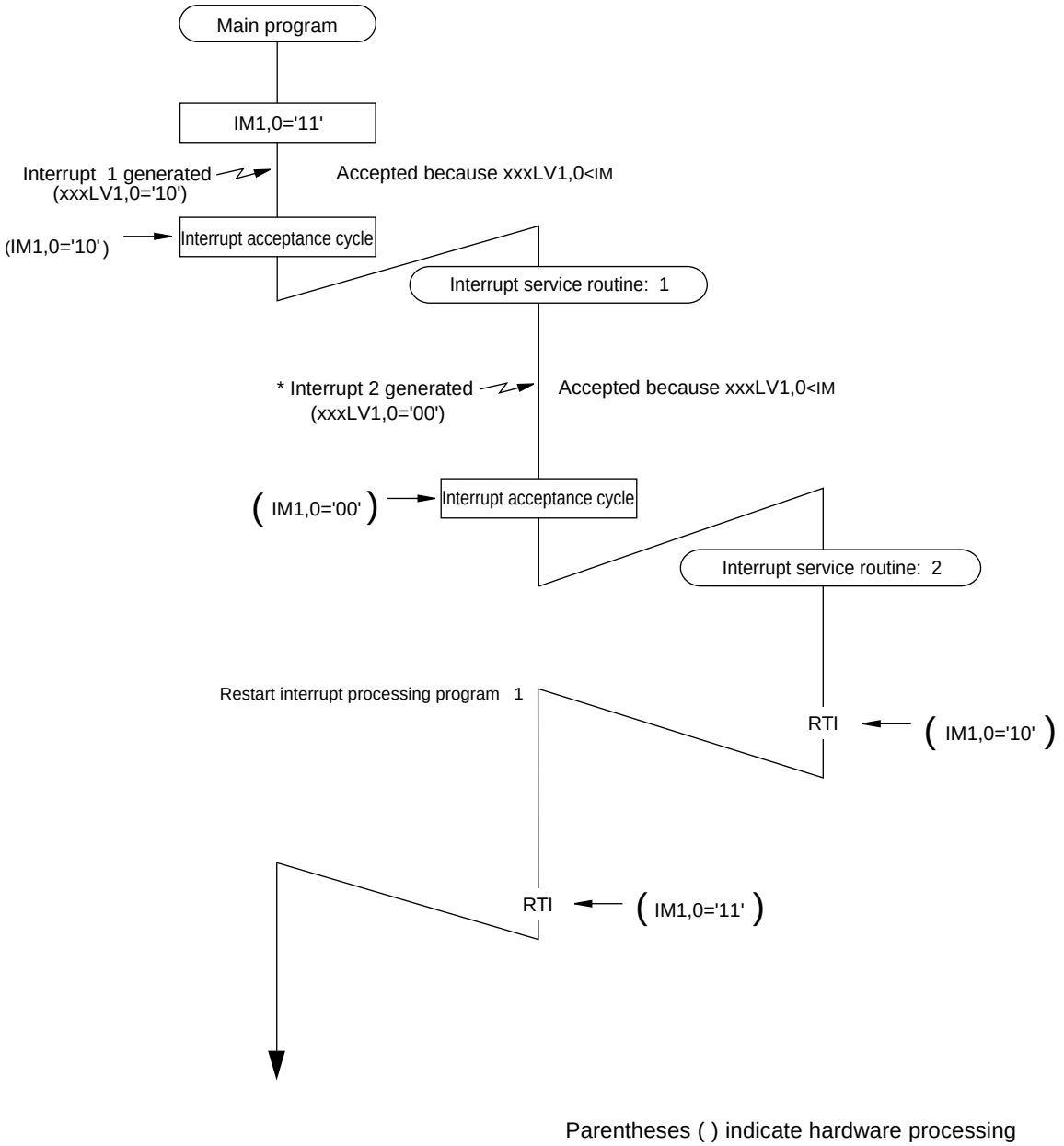


Figure 3-1-7 Processing Sequence with Multiple Interrupts Enabled

3-1-4 Interrupt Flag Setup

■ Interrupt request flag (IR) setup by the software

The interrupt request flag is operated by the hardware. That is set to "1" when any interrupt factor is generated, and cleared to "0" when the interrupt is accepted. If you want to operate it by the software, the IRWE flag of MEMCTR should be set to "1".

■ Interrupt flag setup procedure

A setup procedure of the interrupt request flag set by the hardware and the software shows as follows ;

Setup Procedure	Description
(1) Disable all maskable interrupts. PSW bp6 : MIE = 0	(1) Clear the MIE flag of PSW to disable all maskable interrupts. This is necessary, especially when the interrupt control register is changed.
(2) Select the interrupt factor.	(2) Select the interrupt factor such as interrupt edge selection, or timer interrupt cycle change.
(3) Enable the interrupt request flag to be rewritten. MEMCTR (x'3F01') bp2 : IRWE = 1	(3) Set the IRWE flag of MEMCTR to enable the interrupt request flag to be rewritten. This is necessary only when the interrupt request flag is changed by the software.
(4) Rewrite the interrupt request flag. xxxICR bp0 : xxxIR	(4) Rewrite the interrupt request flag (xxxIR) of the interrupt control register (xxxICR).
(5) Disable the interrupt request flag to be rewritten. MEMCTR (x'3F01') bp2 : IRWE = 0	(5) Clear the IRWE flag so that interrupt request flag can not be rewritten by the software.
(6) Set the interrupt level. xxxICR bp7-6 : xxxLV1-0 PSW bp5-4 : IM1-0	(6) Set the interrupt level by the xxxLV1-0 flag of the interrupt control register (xxxICR). Set the IM1-0 flag of PSW when the interrupt acceptance level of CPU should be changed.
(7) Enable the interrupt. xxxICR bp1 : xxxIE = 1	(7) Set the xxxIE flag of the interrupt control register (xxxICR) to enable the interrupt.
(8) Enable all maskable interrupts. PSW bp6 : MIE = 1	(8) Set the MIE flag of PSW to enable maskable interrupts.

3-2 Control Registers

3-2-1 Registers List

Table 3-2-1 Interrupt Control Registers

Register	Address	R/W	Functions	Page
NMICR	x'03FE1'	R/W	Non-maskable interrupt control register	III - 16
IRQ0ICR	x'03FE2'	R/W	External interrupt 0 control register	III - 17
IRQ1ICR	x'03FE3'	R/W	External interrupt 1 control register	III - 18
IRQ2ICR	x'03FE4'	R/W	External interrupt 2 control register	III - 19
IRQ3ICR	x'03FE5'	R/W	External interrupt 3 control register	III - 20
IRQ4ICR	x'03FE6'	R/W	External interrupt 4 control register	III - 21
TM0ICR	x'03FE9'	R/W	Timer 0 interrupt control register (Timer 0 interrupt)	III - 23
TM1ICR	x'03FEA'	R/W	Timer 1 interrupt control register (Timer 1 interrupt)	III - 24
TM4ICR	x'03FED'	R/W	Timer 4 interrupt control register (Timer 4 interrupt)	III - 27
TM5ICR	x'03FEE'	R/W	Timer 5 interrupt control register (Timer 5 interrupt)	III - 28
TM6ICR	x'03FEF'	R/W	Timer 6 interrupt control register (Timer 6 interrupt)	III - 29
TBICR	x'03FF0'	R/W	Time base interrupt control register (Time base period)	III - 30
TM7ICR	x'03FF1'	R/W	Timer 7 interrupt control register (Timer 7 interrupt)	III - 31
T7OC2ICR	x'03FF2'	R/W	Timer 7 compare register2-match interrupt control register	III - 32
SC0RICR	x'03FF4'	R/W	Serial interface 0 interrupt control register (Serial interface 0 reception)	III - 33
SC0TICR	x'03FF5'	R/W	Serial interface 0 interrupt control register (Serial interface 0 transmission)	III - 34
SC1RICR	x'03FF6'	R/W	Serial interface 1 interrupt control register (Serial interface 1 reception)	III - 35
SC1TICR	x'03FF7'	R/W	Serial interface 1 interrupt control register (Serial interface 1 transmission)	III - 36
SC3ICR	x'03FF9'	R/W	Serial interface 3 interrupt control register (Serial interface 3 interrupt)	III - 38
SC4ICR	x'03FF3'	R/W	Serial interface 4 interrupt control register (Serial interface 4 interrupt)	III - 39
ADICR	x'03FFA'	R/W	A/D conversion interrupt control register (A/D converter interrupt)	III - 40
ATC1ICR	x'03FFC'	R/W	ATC1 interrupt control register(ATC interrupt)	III - 41

Writing to the interrupt control register should be done after that all maskable interrupts are set to be disabled by the MIE flag of the PSW register.

If the interrupt level flag (xxxLVn) is set to "level 3", its vector is disabled, regardless of interrupt enable flag and interrupt request flag.

3-2-2 Interrupt Control Registers

The interrupt control registers include the maskable interrupt control registers (xxxICR) and the non-maskable interrupt control register (NMICR).

■Non-Maskable Interrupt Control Register (NMICR address: x'03FE1')

The non-maskable interrupt control register (NMICR) stores the non maskable interrupt request. When the non-maskable interrupt request is generated, the interrupt is accepted regardless of the interrupt mask level (IMn) of PSW. The hardware then branches to the address stored at location x'04004' in the interrupt vector table. The watchdog timer overflow interrupt request flag (WDIR) is set to "1" when the watchdog timer overflows. The program interrupt request flag (PIR) is set to "1" when the undefined instruction is executed.

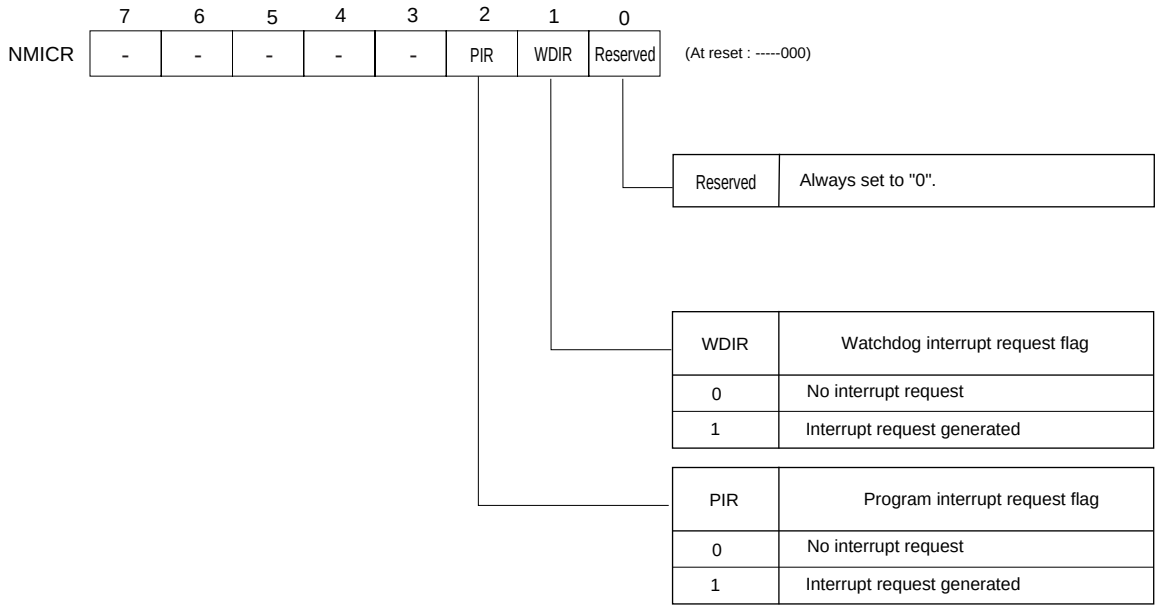


Figure 3-2-1 Non-Maskable Interrupt Control Register (NMICR:x'03FE1', R/W)

On this LSI, when undefined instruction is decoded, the program interrupt request flag (PIR) is set to "1", and the non-maskable interrupt is generated.
If the PIR flag setup is confirmed by the non-maskable interrupt service routine, the reset via the software is recommended, When software reset, the reset pin (p27) outputs "0".

Once the WDIR flag becomes "1" after non-maskable interrupt happens, only the program can clear it to "0".

■External Interrupt 0 Control Register (IRQ0ICR)

The external interrupt 0 control register (IRQ0ICR) controls interrupt level of the external interrupt 0, active edge, interrupt enable and interrupt request. Interrupt control register should be operated when the maskable interrupt enable flag (MIE) of PSW is "0".

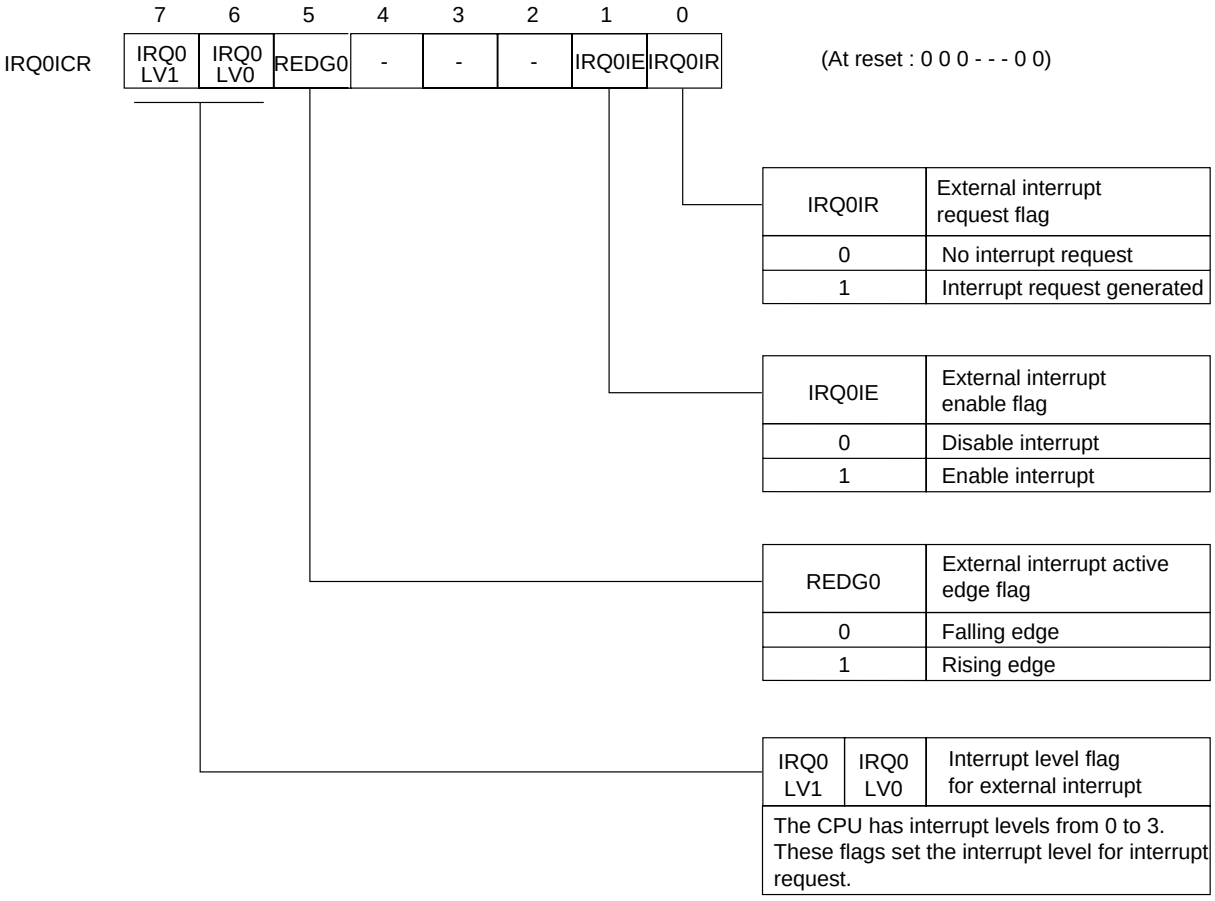


Figure 3-2-2 External Interrupt 0 Control Register (IRQ0ICR : x'03FE2', R/W)

■External Interrupt 1 Control Register (IRQ1ICR)

The external interrupt 1 control register (IRQ1ICR) controls interrupt level of external interrupt 1, active edge, interrupt enable and interrupt request. Interrupt control register should be operated when the maskable interrupt enable flag (MIE) of PSW is "0".

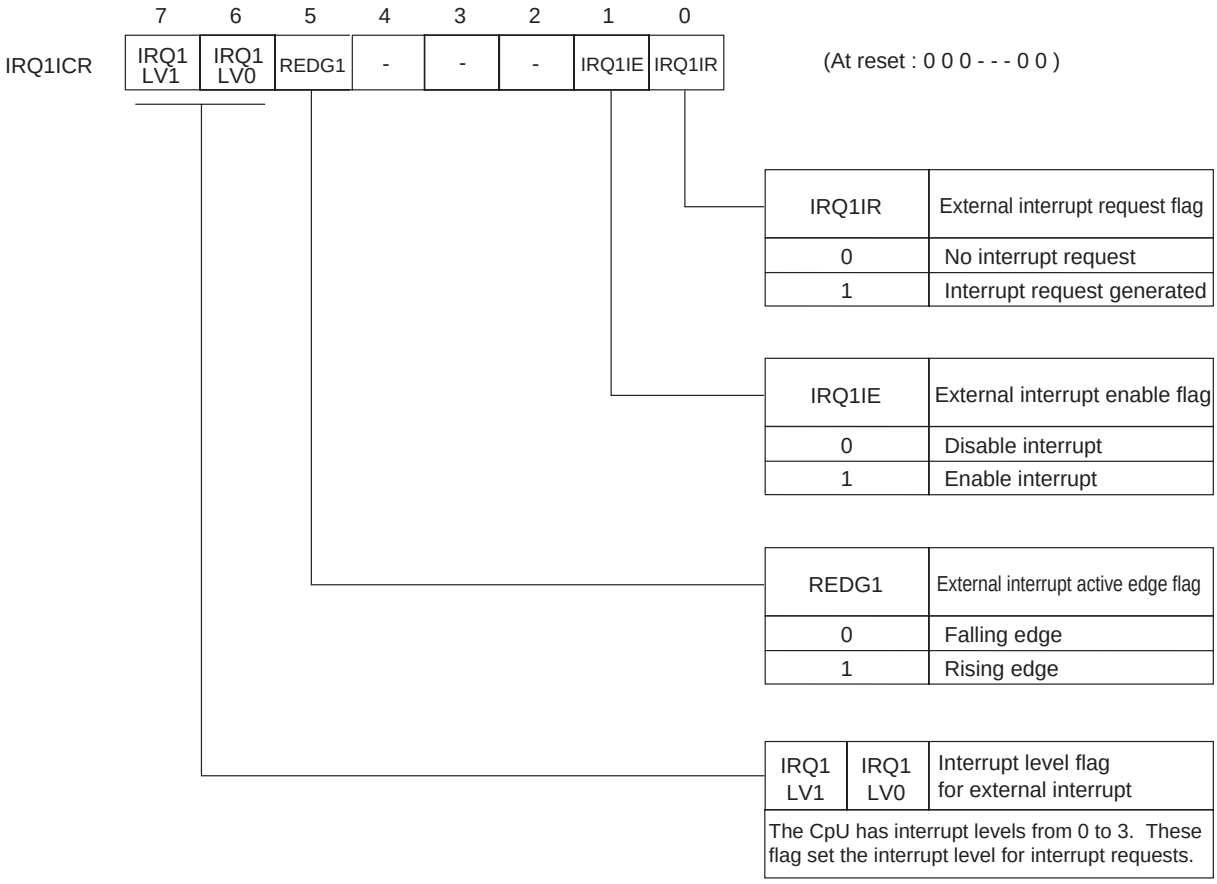


Figure 3-2-3 External Interrupt 1 Control Register (IRQ1ICR : x'03FE3', R/W)

■External Interrupt 2 Control Register (IRQ2ICR)

The external interrupt 2 control register (IRQ2ICR) controls interrupt level of external interrupt 2, active edge, interrupt enable and interrupt request. Interrupt control register should be operated when the maskable interrupt enable flag (MIE) of PSW is "0".

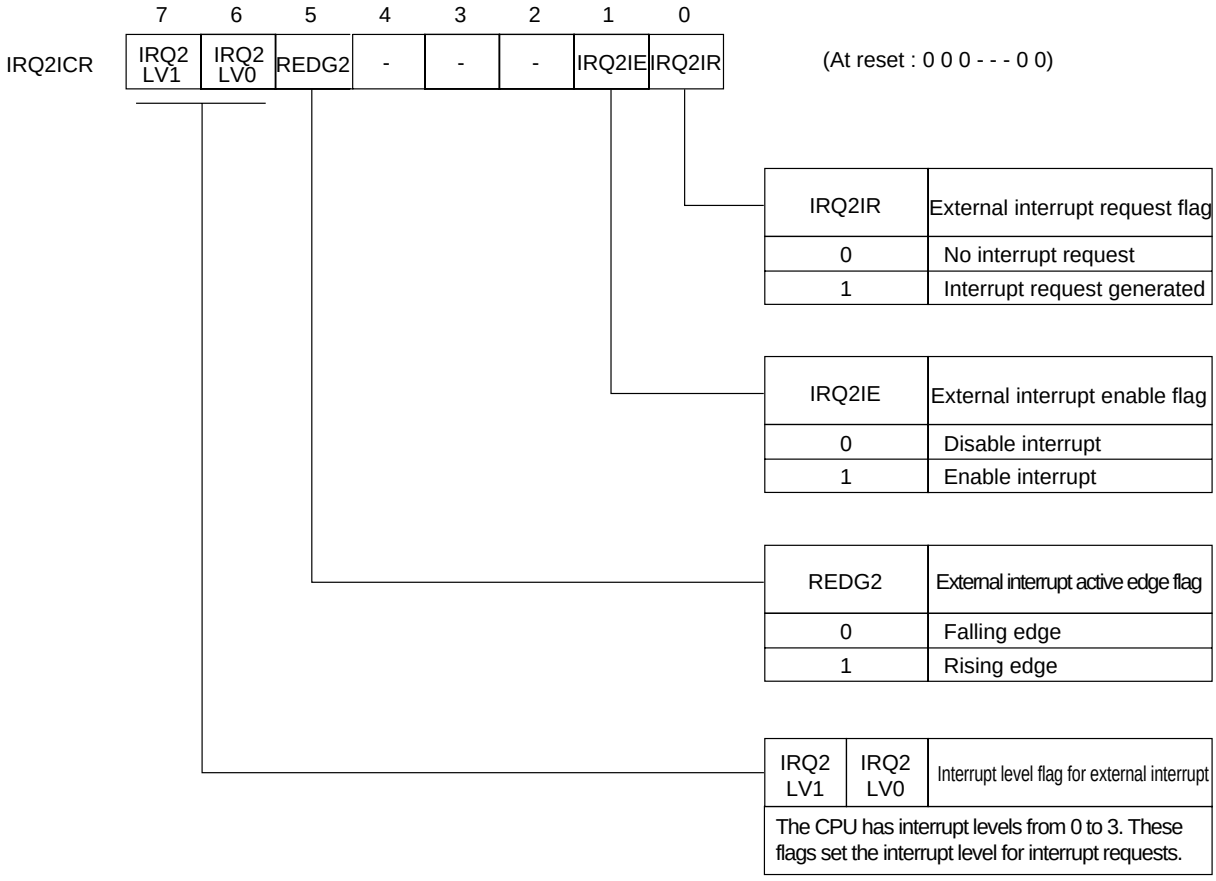


Figure 3-2-4 External Interrupt 2 Control Register (IRQ2ICR : x'03FE4', R/W)

■External Interrupt 3 Control Register (IRQ3ICR)

The external interrupt 3 control register (IRQ3ICR) controls interrupt level of external interrupt 3, active edge, interrupt enable flag and interrupt request. Interrupt control register should be operated when the maskable interrupt enable flag (MIE) of PSW is "0".

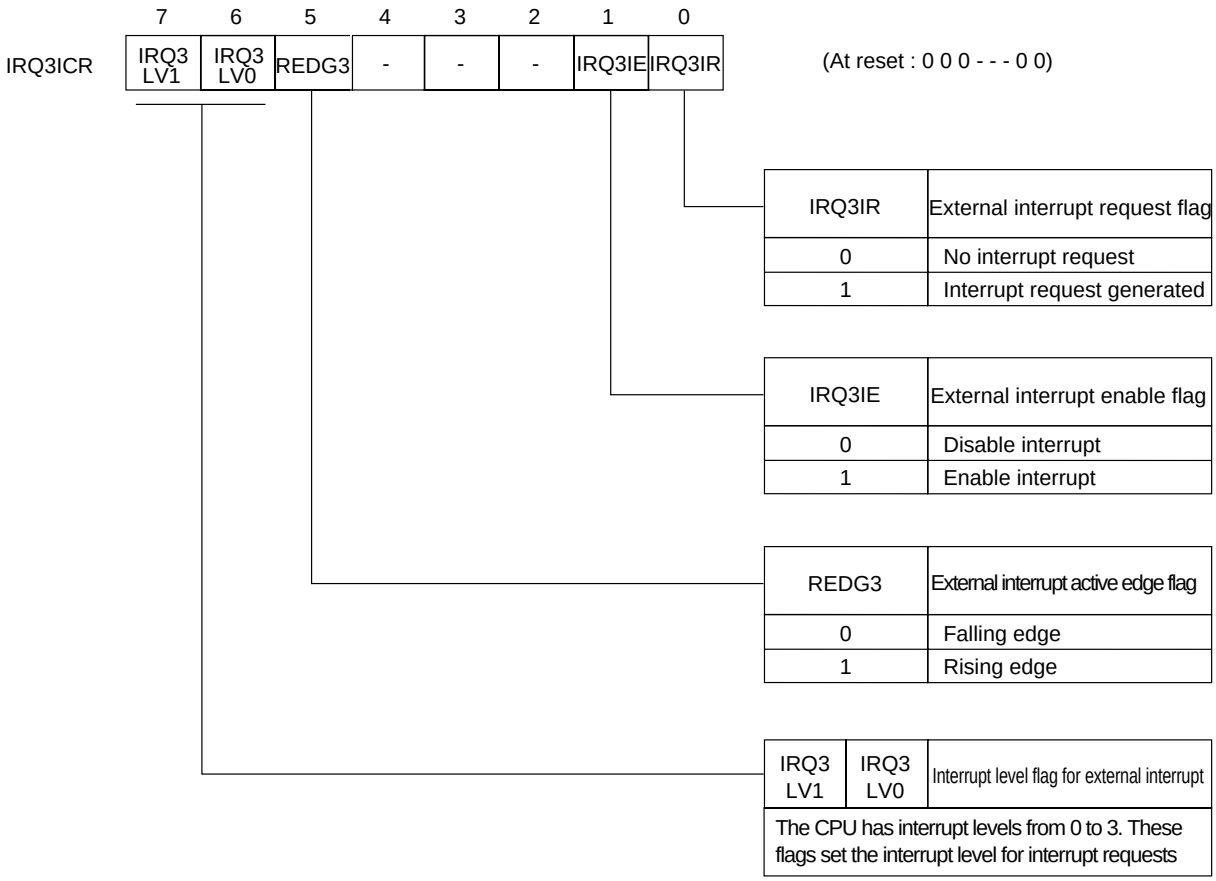


Figure 3-2-5 External Interrupt 3 Control Register (IRQ3ICR : x'03FE5', R/W)

■External Interrupt 4 Control Register (IRQ4ICR)

The external interrupt 4 control register (IRQ4ICR) controls interrupt level of external interrupt 4, active edge, interrupt enable flag and interrupt request. Interrupt control register should be operated when the maskable interrupt enable flag (MIE) of PSW is "0".

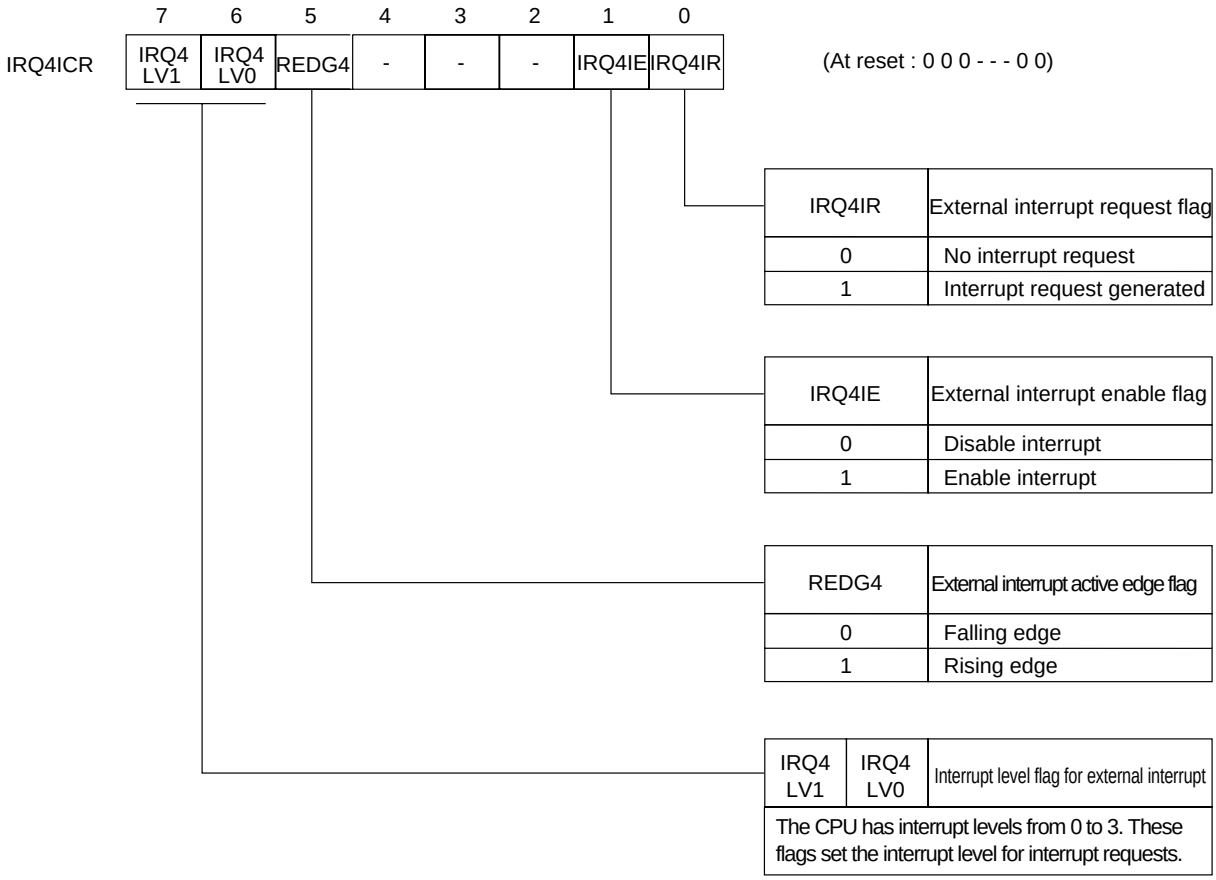


Figure 3-2-6 External Interrupt 4 Control Register (IRQ4ICR : x'03FE6', R/W)

■Timer 0 Interrupt Control Register (TM0ICR)

The timer 0 interrupt control register (TM0ICR) controls interrupt level of timer 0 interrupt, interrupt enable flag and interrupt request. Interrupt control register should be operated when the maskable interrupt enable flag (MIE) of PSW is "0".

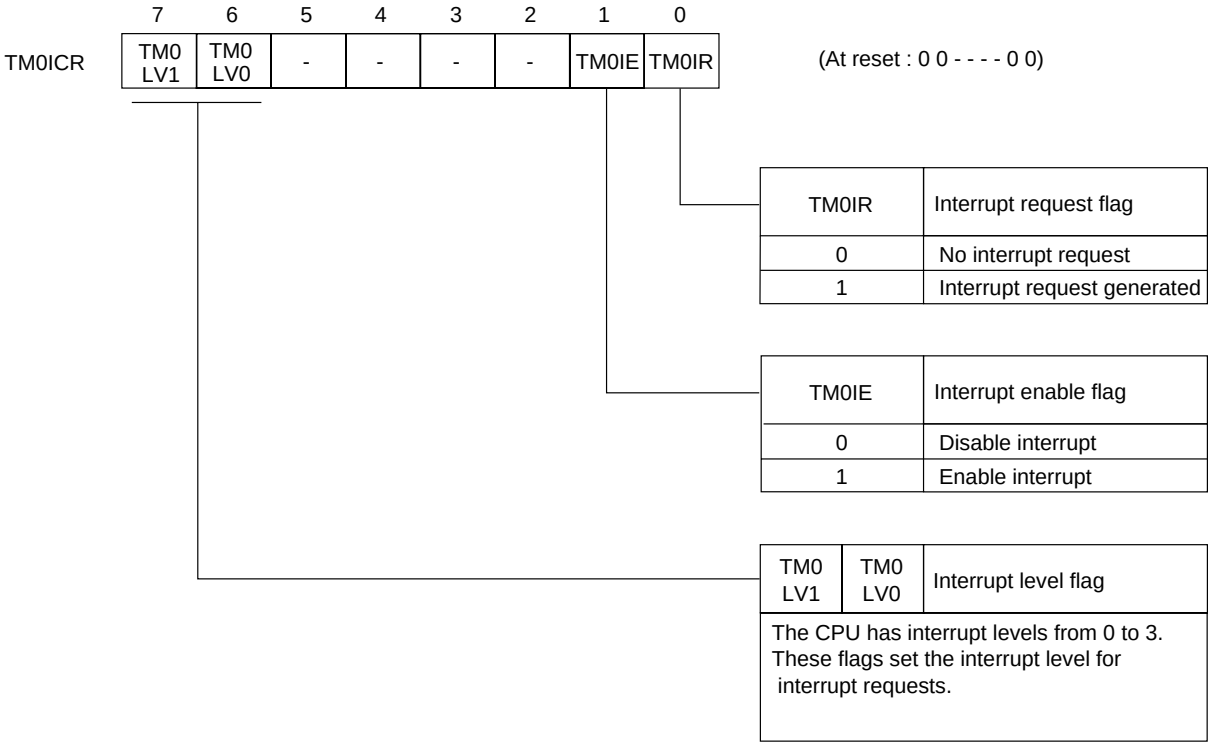


Figure 3-2-8 Timer 0 Interrupt Control Register (TM0ICR : x'03FE9', R/W)

■Timer 1 Interrupt Control Register (TM1ICR)

The timer 1 interrupt control register (TM1ICR) controls interrupt level of timer 1 interrupt, interrupt enable flag and interrupt request. Interrupt control register should be operated when the maskable interrupt enable flag (MIE) of PSW is "0".

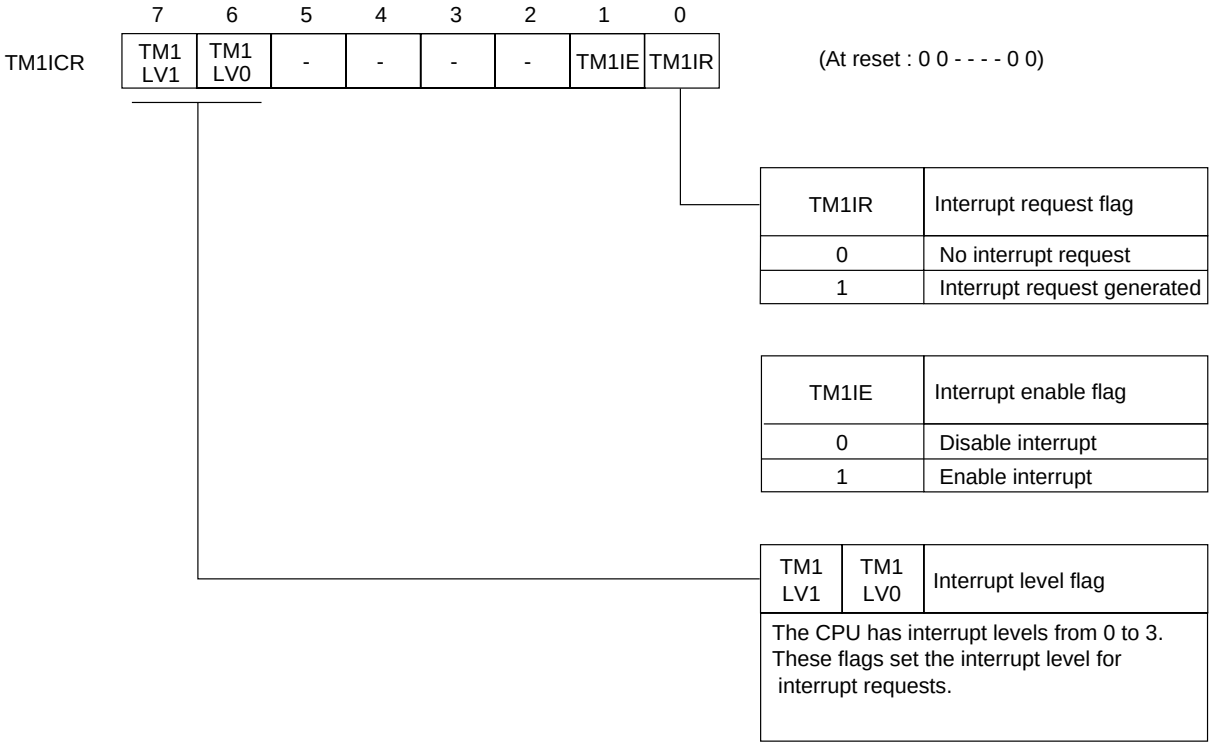


Figure 3-2-9 Timer 1 Interrupt Control Register (TM1ICR : x'03FEA', R/W)

■Timer 4 Interrupt Control Register (TM4ICR)

The timer 4 interrupt control register (TM4ICR) controls interrupt level of timer 4 interrupt, interrupt enable flag and interrupt request. Interrupt control register should be operated when the maskable interrupt enable flag (MIE) of PSW is "0".

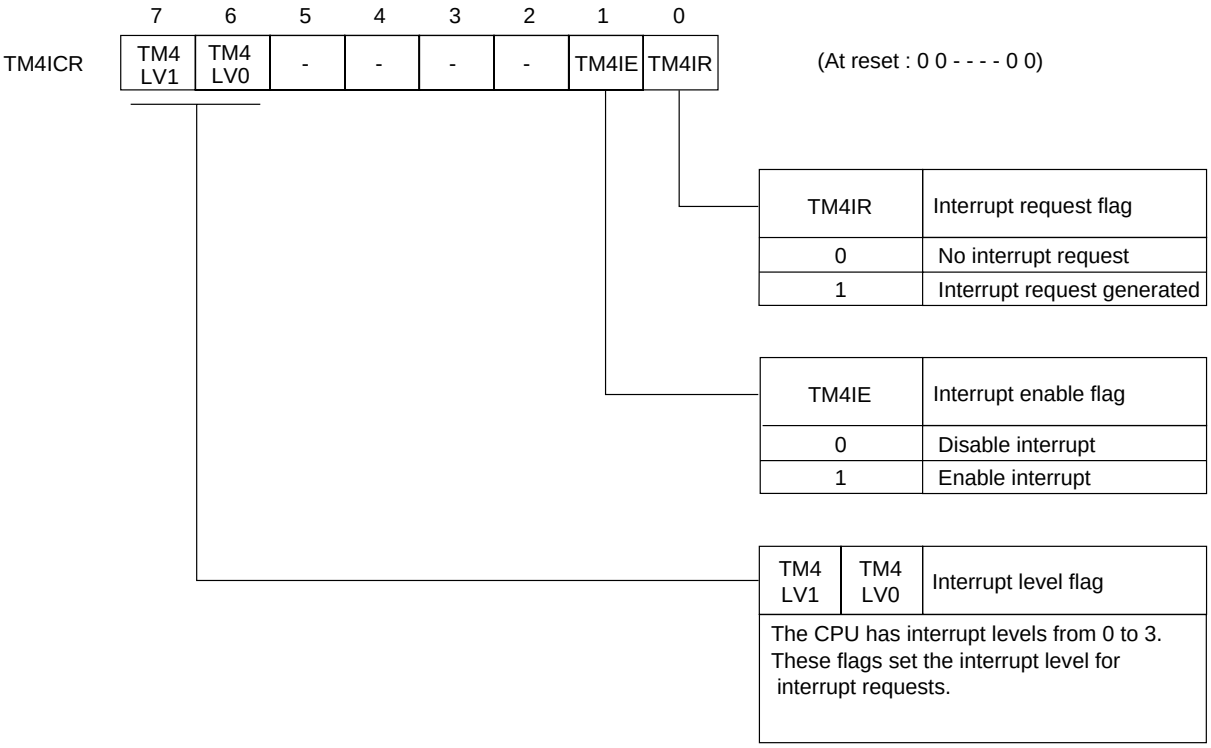


Figure 3-2-12 Timer 4 Interrupt Control Register (TM4ICR : x'03FED', R/W)

■Timer 5 Interrupt Control Register (TM5ICR)

The timer 5 interrupt control register (TM5ICR) controls interrupt level of timer 5 interrupt, interrupt enable flag and interrupt request. Interrupt control register should be operated when the maskable interrupt enable flag (MIE) of PSW is "0".

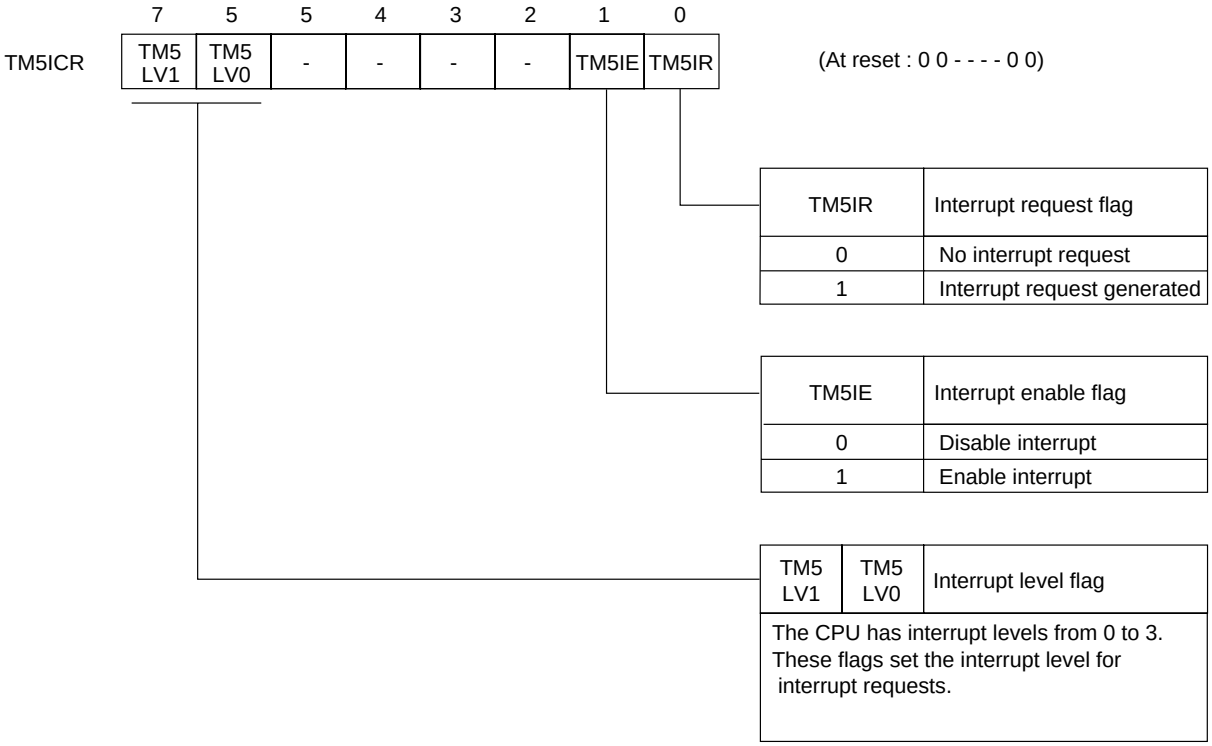


Figure 3-2-13 Timer 5 Interrupt Control Register (TM5ICR : x'03FEE', R/W)

■Timer 6 Interrupt Control Register (TM6ICR)

The timer 6 interrupt control register (TM6ICR) controls interrupt level of timer 6 interrupt, interrupt enable flag and interrupt request. Interrupt control register should be operated when the maskable interrupt enable flag (MIE) of PSW is "0".

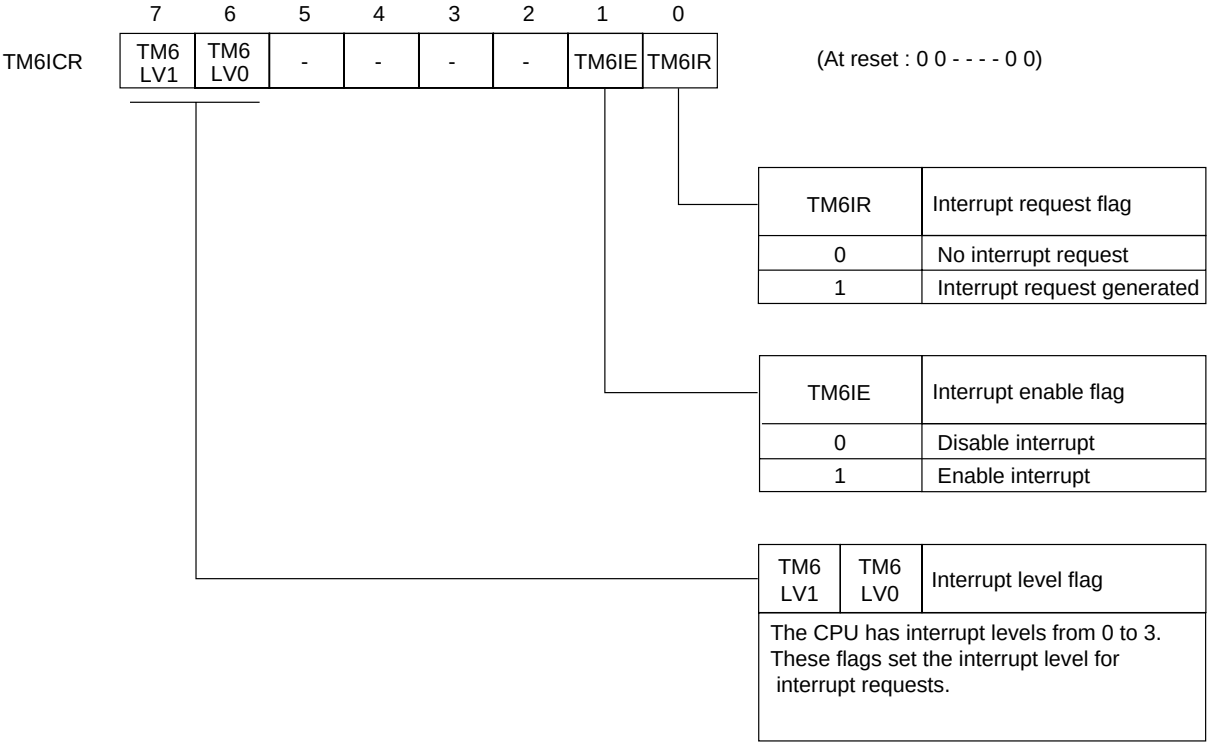


Figure 3-2-14 Timer 6 Interrupt Control Register (TM6ICR : x'03FEF', R/W)

■Time Base Interrupt Control Register (TBICR)

The time base interrupt control register (TBICR) controls interrupt level of time base interrupt, interrupt enable flag and interrupt request. Interrupt control register should be operated when the maskable interrupt enable flag (MIE) of PSW is "0".

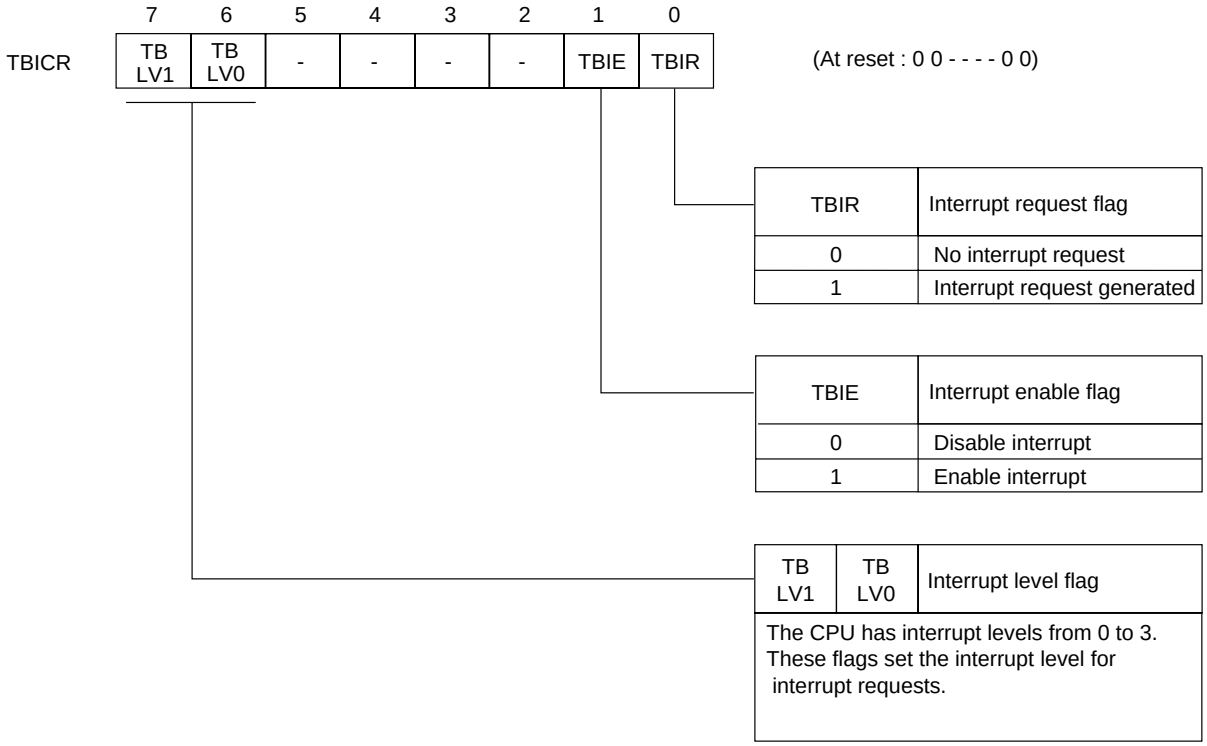


Figure 3-2-15 Time Base Interrupt Control Register (TBICR : x'03FF0', R/W)

■Timer 7 Interrupt Control Register (TM7ICR)

The timer 7 interrupt control register (TM7ICR) controls interrupt level of timer 7 interrupt, interrupt enable flag and interrupt request. Interrupt control register should be operated when the maskable interrupt enable flag (MIE) of PSW is "0".

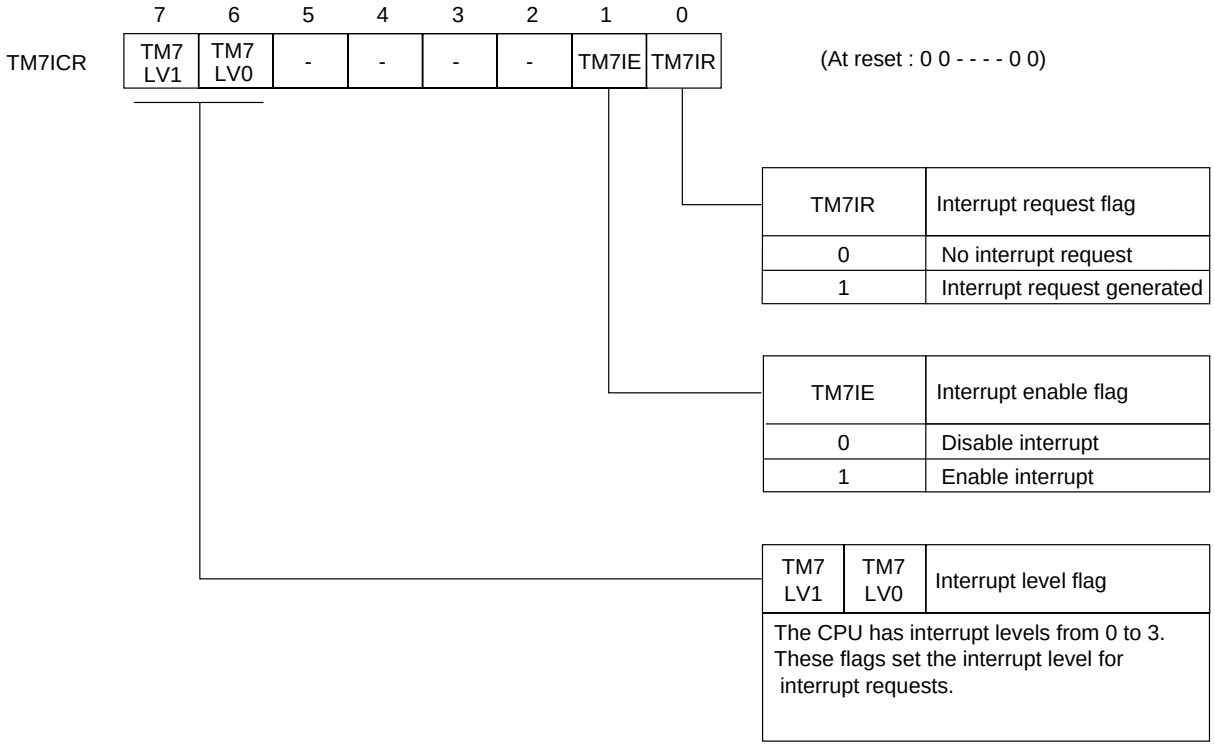


Figure 3-2-16 Timer 7 Interrupt Control Register (TM7ICR : x'03FF1', R/W)

■Timer 7 Compare Register 2-match Interrupt Control Register (TOC2ICR)

The timer 7 compare register 2-match interrupt control register (TOC2ICR) controls interrupt level of timer 7 compare register 2-match interrupt , interrupt enable flag and interrupt request. Interrupt control register should be operated when the maskable interrupt enable flag (MIE) of PSW is "0".

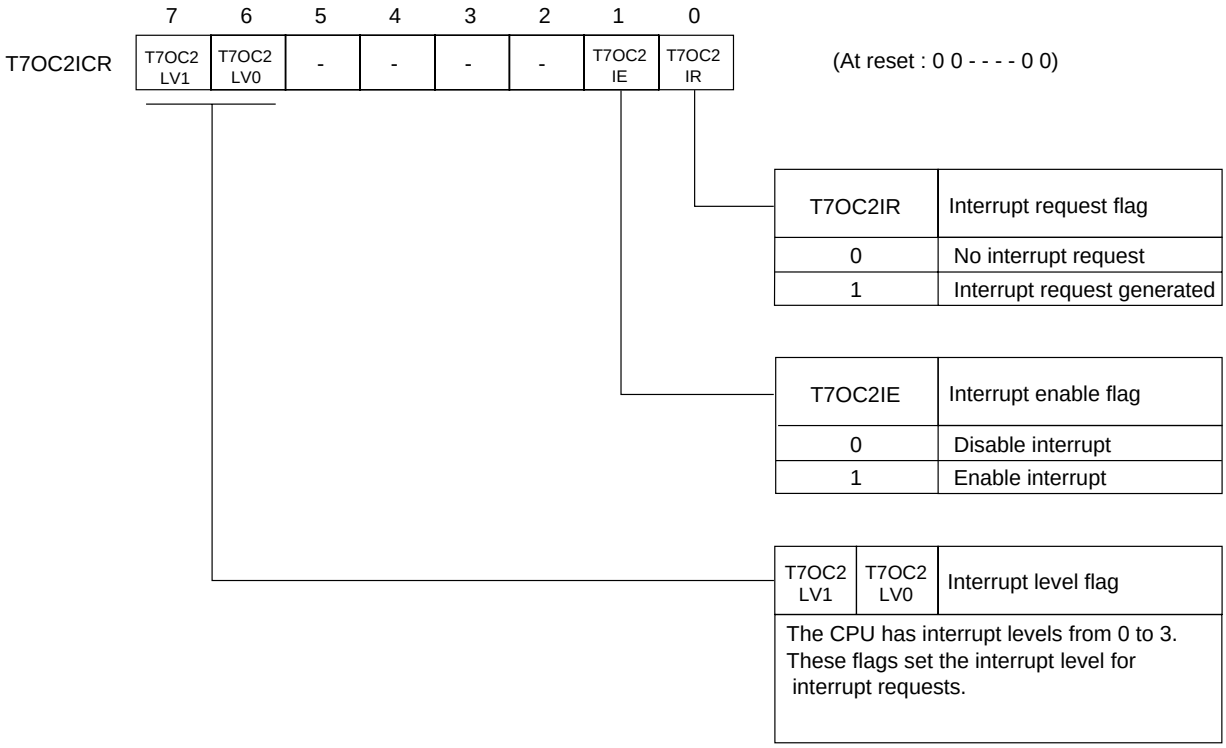


Figure 3-2-17 Timer 7 Compare Register 2-match Interrupt Control Register (TMOC2ICR : x'03FF2', R/W)

■Serial Interface 0 Reception Interrupt Control Register (SC0RICR)

The serial Interface 0 reception interrupt control register (SC0RICR) controls interrupt level of serial Interface 0 reception interrupt, interrupt enable flag and interrupt request. Interrupt control register should be operated when the maskable interrupt enable flag (MIE) of PSW is "0".

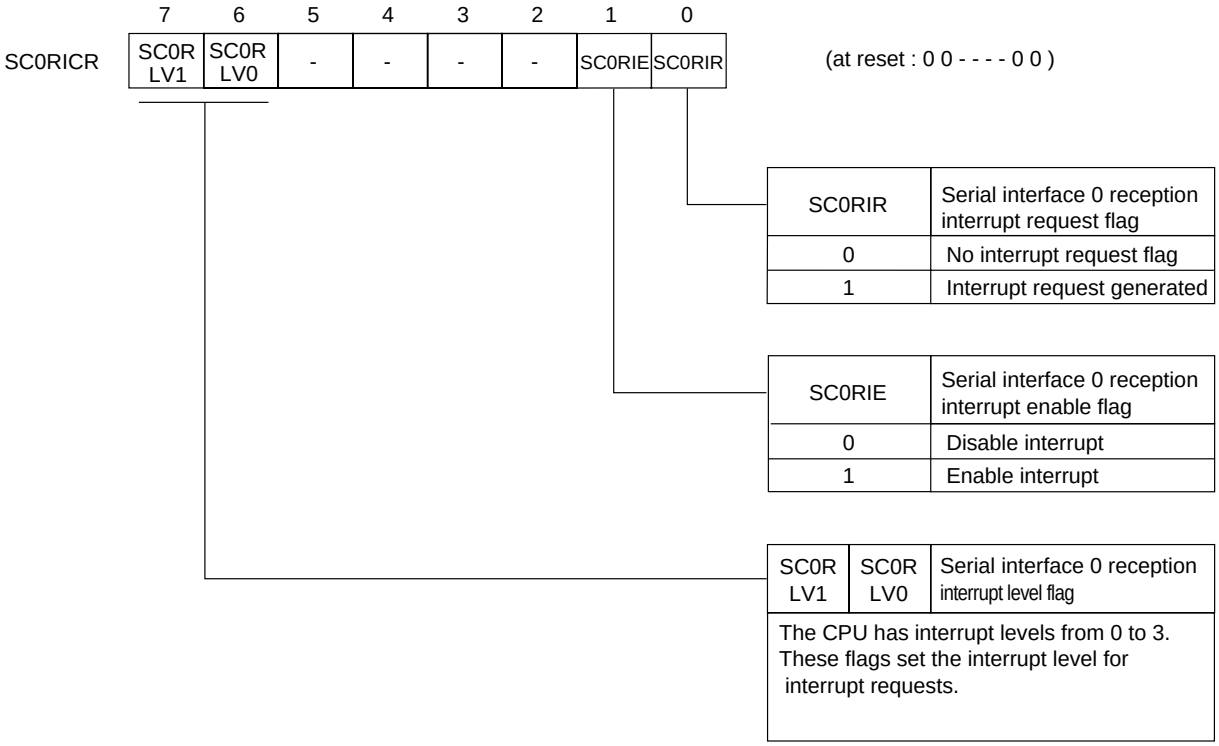


Figure 3-2-18 Serial Interface 0 Reception Interrupt Control register (SC0RICR:x'03FF4',R/W)

■Serial Interface 0 Transmission Interrupt Control Register (SC0TICR)

The serial Interface 0 transmission interrupt control register (SC0TICR) controls interrupt level of serial Iinterface 0 transmission interrupt, interrupt enable flag and interrupt request. Interrupt control register should be operated when the maskable interrupt enable flag (MIE) of PSW is "0".

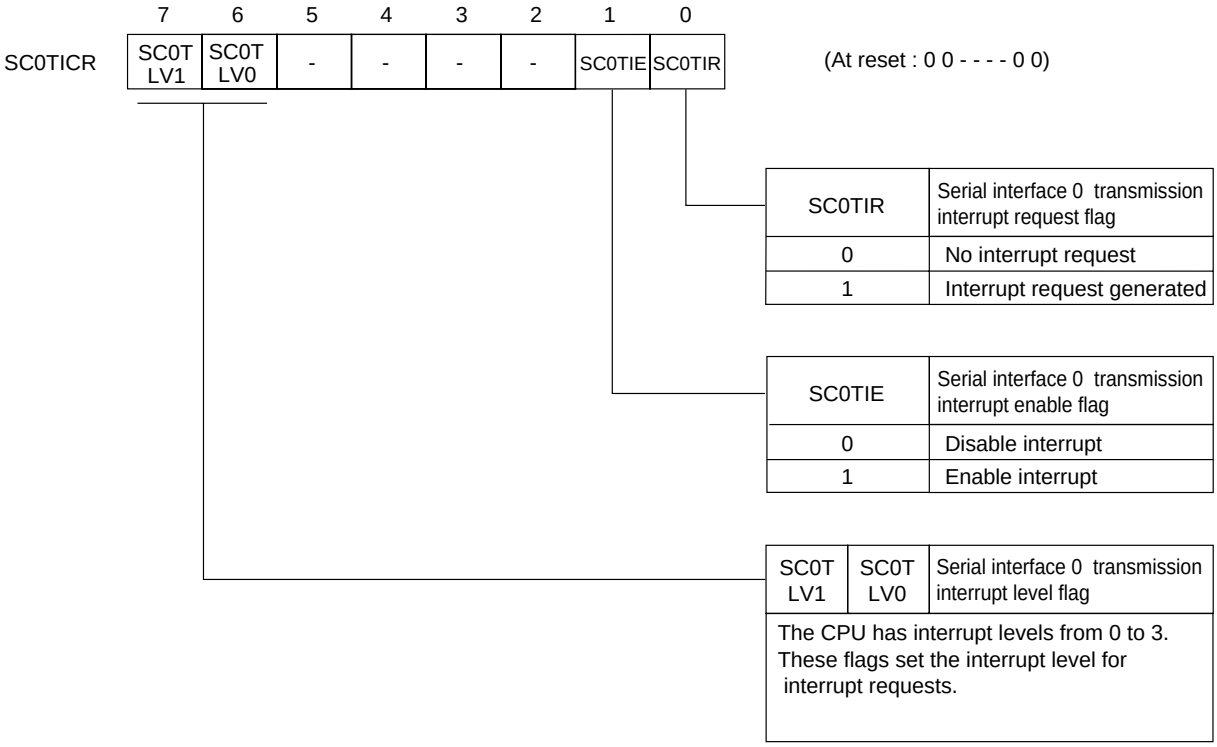


Figure 3-2-19 Serial Interface 0 Transmission Interrupt Control Register (SC0TICR : x'03FF5', R/W)

■Serial Interface 1 Reception Interrupt Control Register (SC1ICR)

The serial Interface 1 reception interrupt control register (SC1ICR) controls interrupt level of serial Interface 1 reception interrupt, interrupt enable flag and interrupt request. Interrupt control register should be operated when the maskable interrupt enable flag (MIE) of PSW is "0".

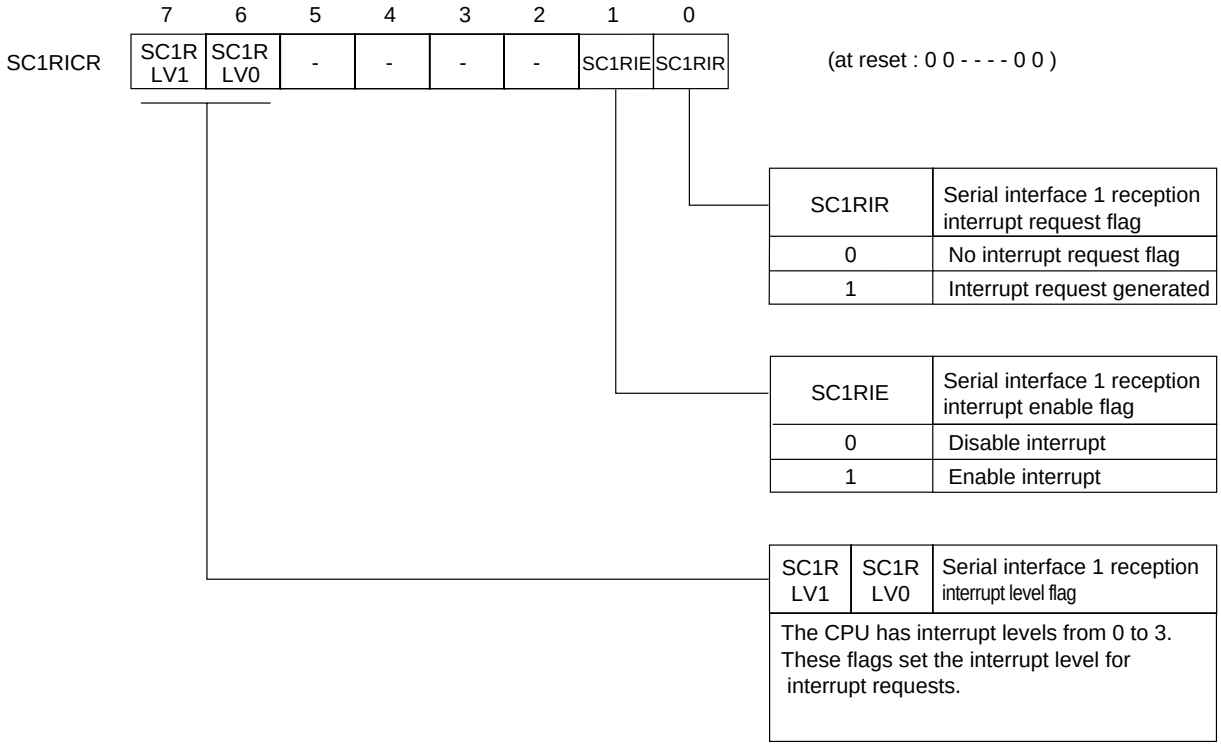


Figure 3-2-20 Serial Interface 1 Reception Interrupt Control Register (SC1ICR : x'03FF6', R/W)

■Serial Interface 1 Transmission Interrupt Control Register (SC1TICR)

The serial Interface 1 transmission interrupt control register (SC1TICR) controls interrupt level of serial Iinterface 1 transmission interrupt, interrupt enable flag and interrupt request. Interrupt control register should be operated when the maskable interrupt enable flag (MIE) of PSW is "0".

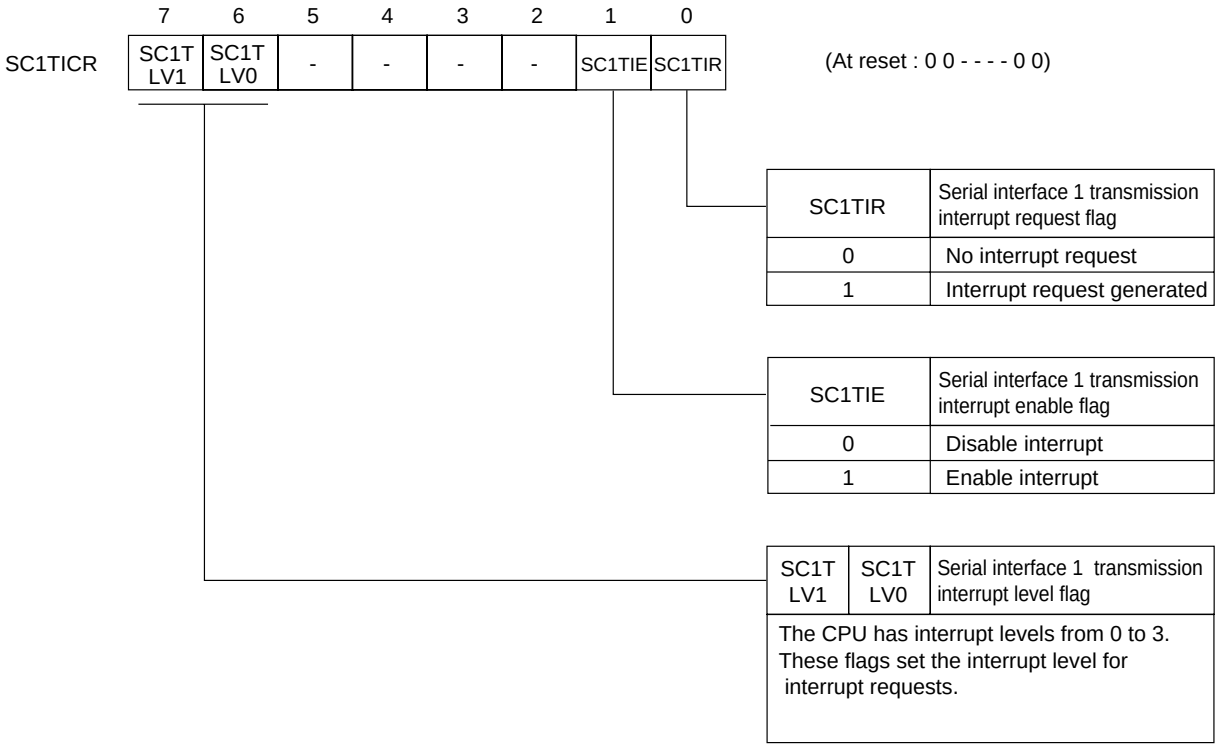


Figure 3-2-21 Serial Interface 1 Transmission Interrupt Control Register (SC1TICR : x'03FF7', R/W)

■Serial Interface 3 Interrupt Control Register (SC3ICR)

The serial interface 3 interrupt control register (SC3ICR) controls interrupt level of serial interface 3 interrupt, interrupt enable flag and interrupt request. Interrupt control register should be operated when the maskable interrupt enable flag (MIE) of PSW is "0".

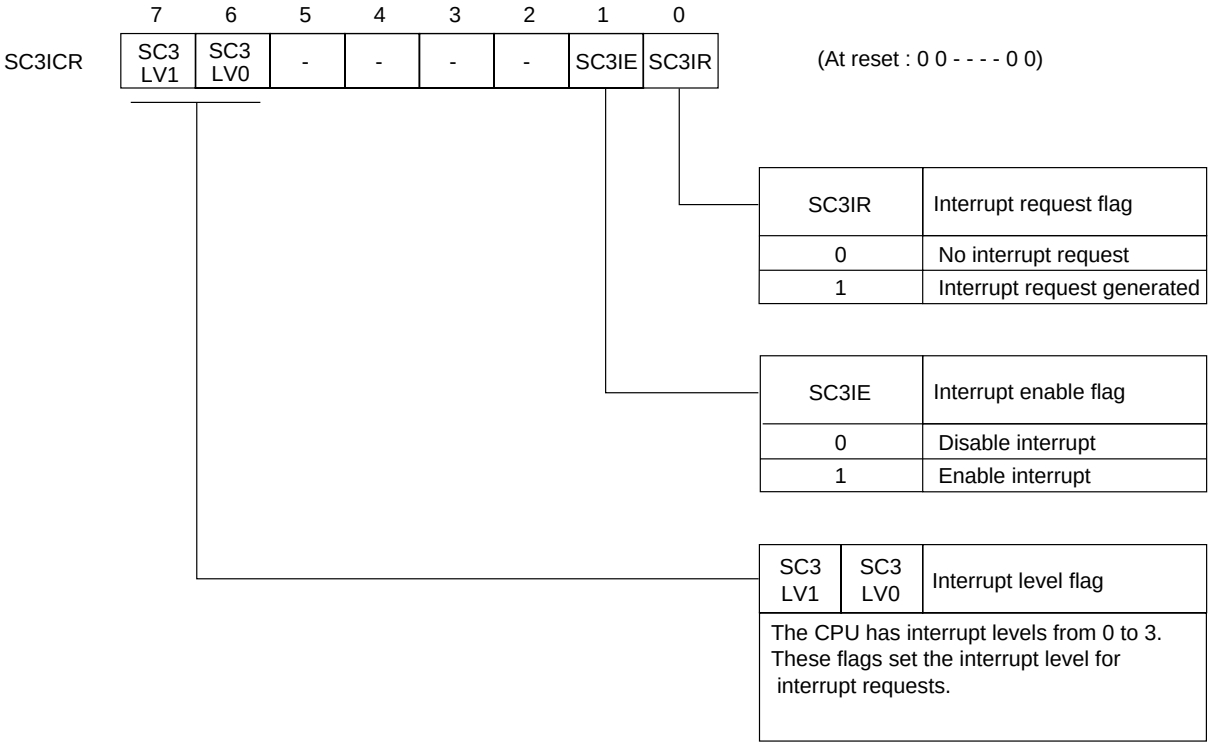


Figure 3-2-23 Serial Interface 3 Interrupt Control Register (SC3ICR : x'03FF9', R/W)

■Serial Interface 4 Interrupt Control Register (SC4ICR)

The serial interface 4 interrupt control register (SC4ICR) controls interrupt level of serial interface 4 interrupt, interrupt enable flag and interrupt request. Interrupt control register should be operated when the maskable interrupt enable flag (MIE) of PSW is "0".

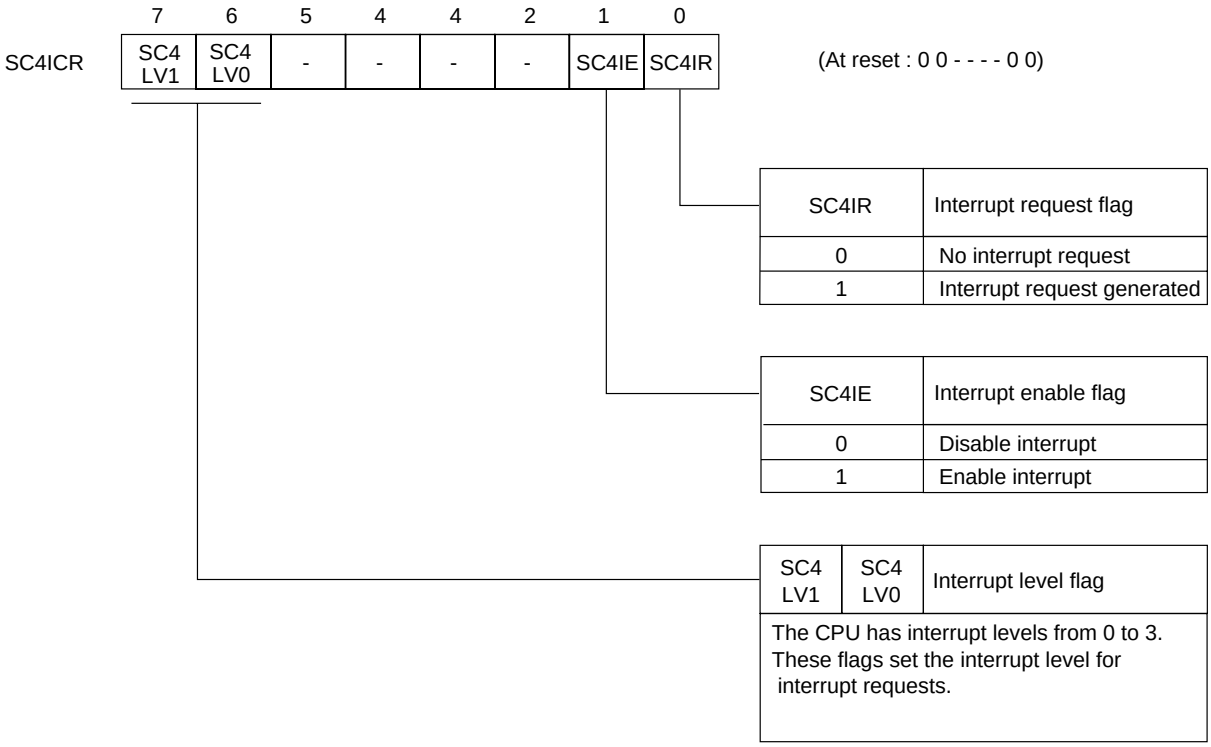


Figure 3-2-24 Serial Interface 4 Interrupt Control Register (SC4ICR : x'03FF3', R/W)

■A/D Converter Interrupt Control Register (ADICR)

The A/D converter interrupt control register (ADICR) controls interrupt level of A/D converter interrupt, interrupt enable flag and interrupt request. Interrupt control register should be operated when the maskable interrupt enable flag (MIE) of PSW is "0".

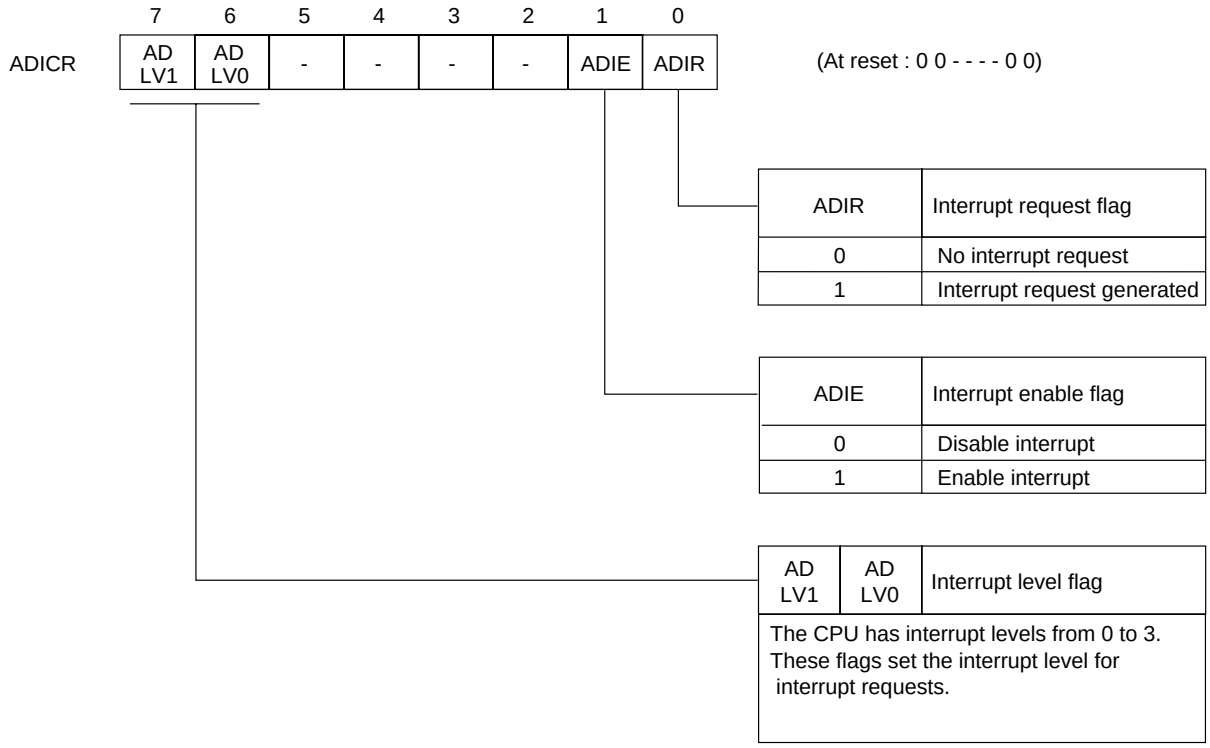


Figure 3-2-25 A/D Converter Interrupt Control Register (ADICR : x'03FFA', R/W)

■ATC 1 Interrupt Control Register (ATC1ICR)

The ATC 1 interrupt control register (ATC1ICR) controls interrupt level of ATC 1 interrupt, interrupt enable flag and interrupt request. Interrupt control register should be operated when the maskable interrupt enable flag (MIE) of PSW is "0".

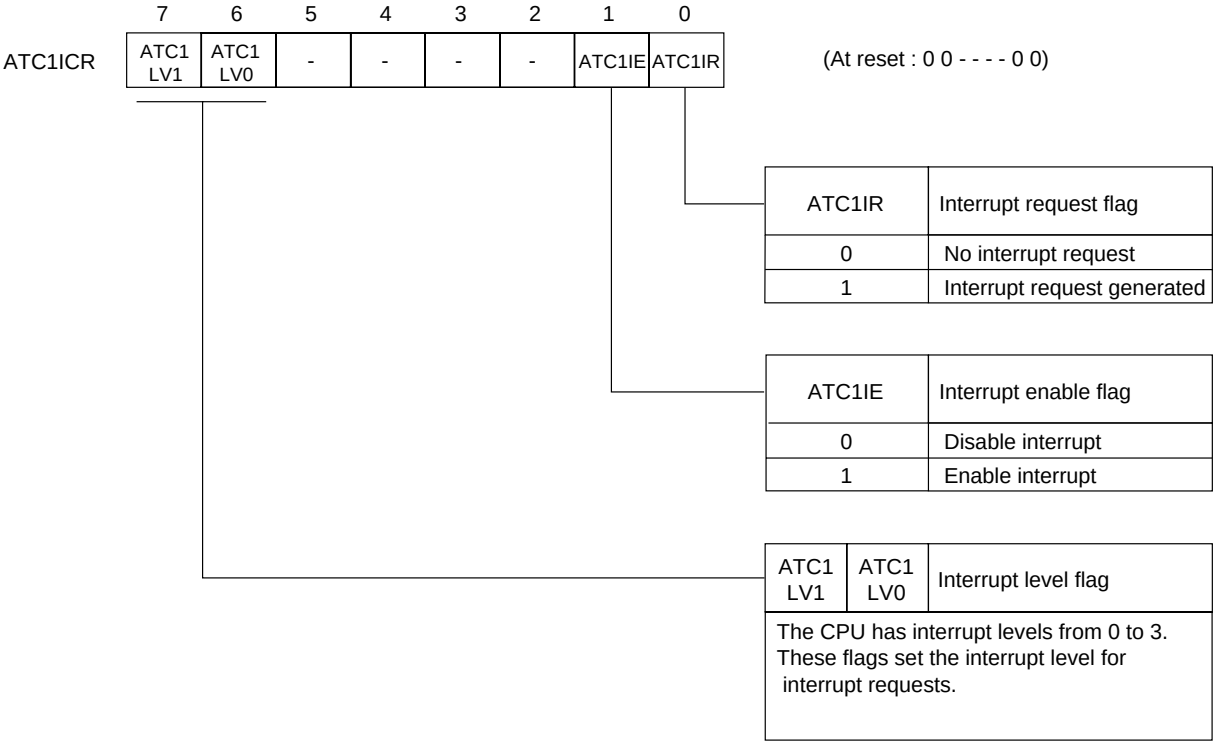


Figure 3-2-26 ATC1 Interrupt Control Register (ATC1ICR : x'03FFC', R/W)

3-3 External Interrupts

There are 5 external interrupts in this LSI. The circuit (external interrupt interface) for the external interrupt input signal, is built-in between the external interrupt input pin and the interrupt controller block. This external interrupt interface can manage to do with any kind of external interrupts.

3-3-1 Overview

Table 3-3-1 shows the list of functions which external interrupts 0 to 4 can be used.

Table 3-3-1 External Interrupt Functions

	External interrupt 0 (IRQ0)	External interrupt 1 (IRQ1)	External interrupt 2 (IRQ2)	External interrupt 3 (IRQ3)	External interrupt 4 (IRQ4)
External interrupt input pin	P20	P21	P22	P23	P24, P60-P67
Programmable active edge interrupt	√	√	√	√	√ (P24)
Both edges interrupt	√	√	√	√	√
Key input interrupt	-	-	-	-	√ (P60-P67)
Noise filter built-in	√	√	√	√	√
AC zero cross detection	-	√	-	-	-

3-3-2 Block Diagram

■External Interrupt 0 Interface, External Interrupt 1 Interface, Block Diagram

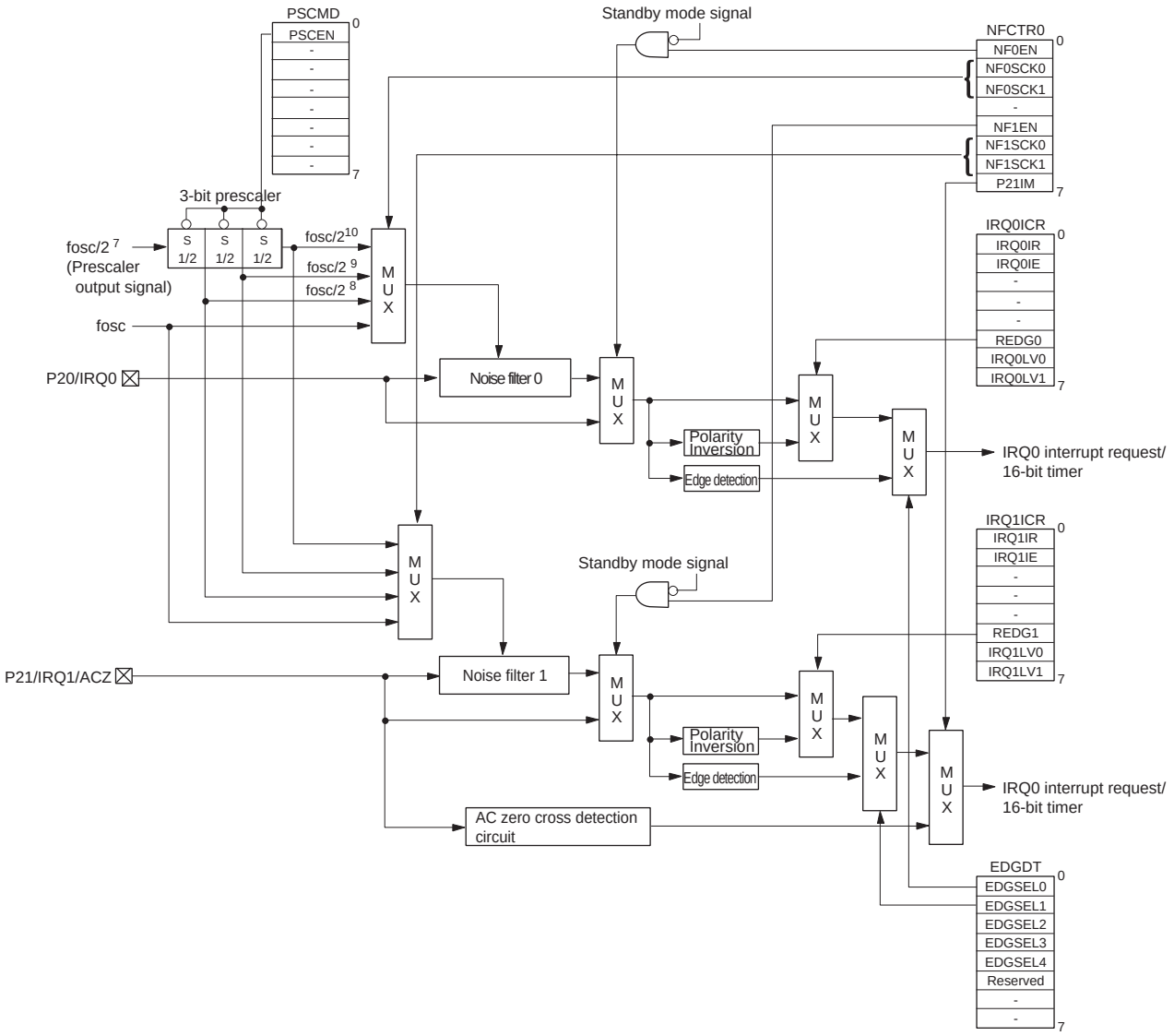


Figure 3-3-1 External Interrupt 0 Interface and External Interrupt 1 Interface Block Diagram

■External Interrupt 2 Interface, External Interrupt 3 Interface, Block Diagram

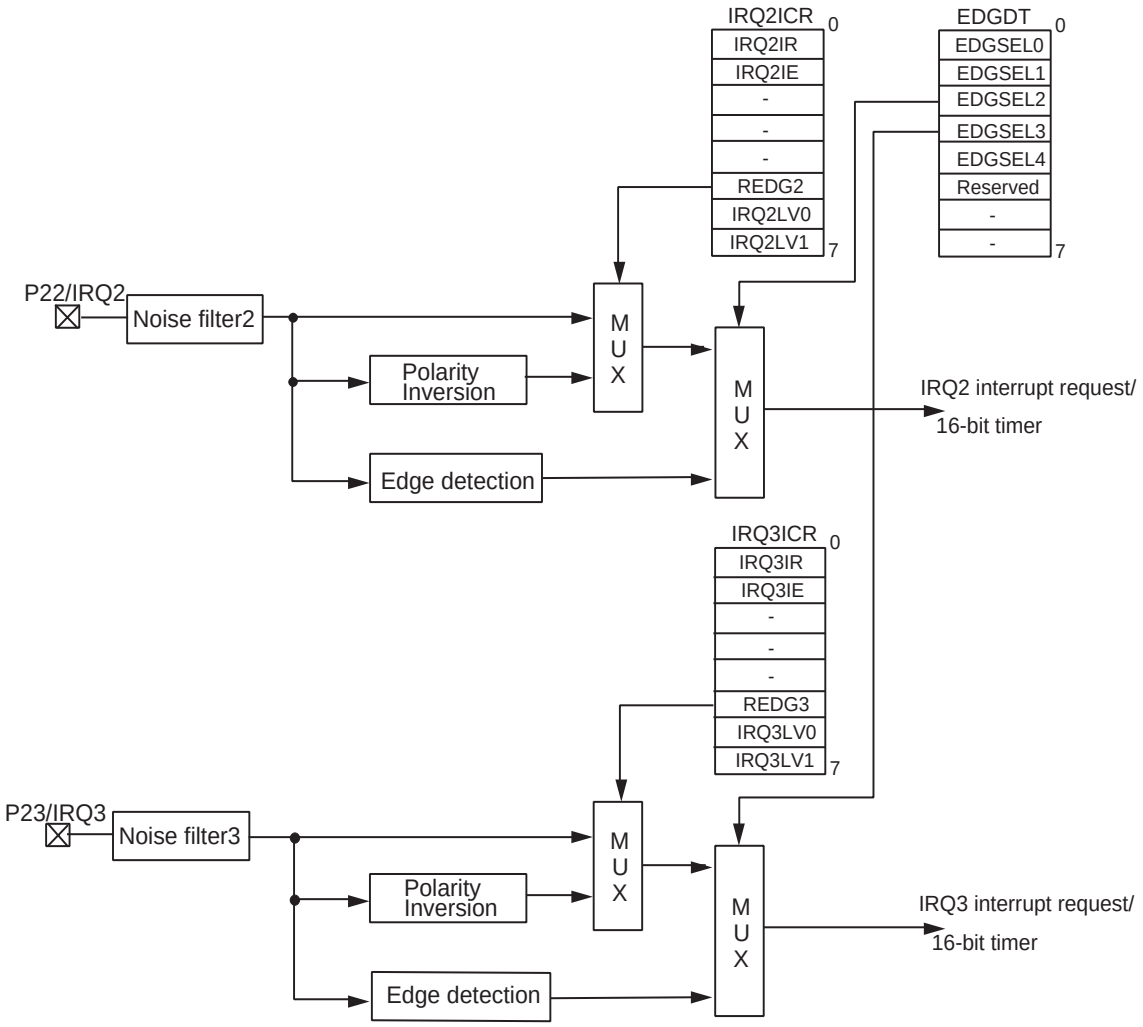


Figure 3-3-2 External Interrupt 2 Interface and External Interrupt 3 Interface, Block Diagram

■External Interrupt 4 Interface Block Diagram

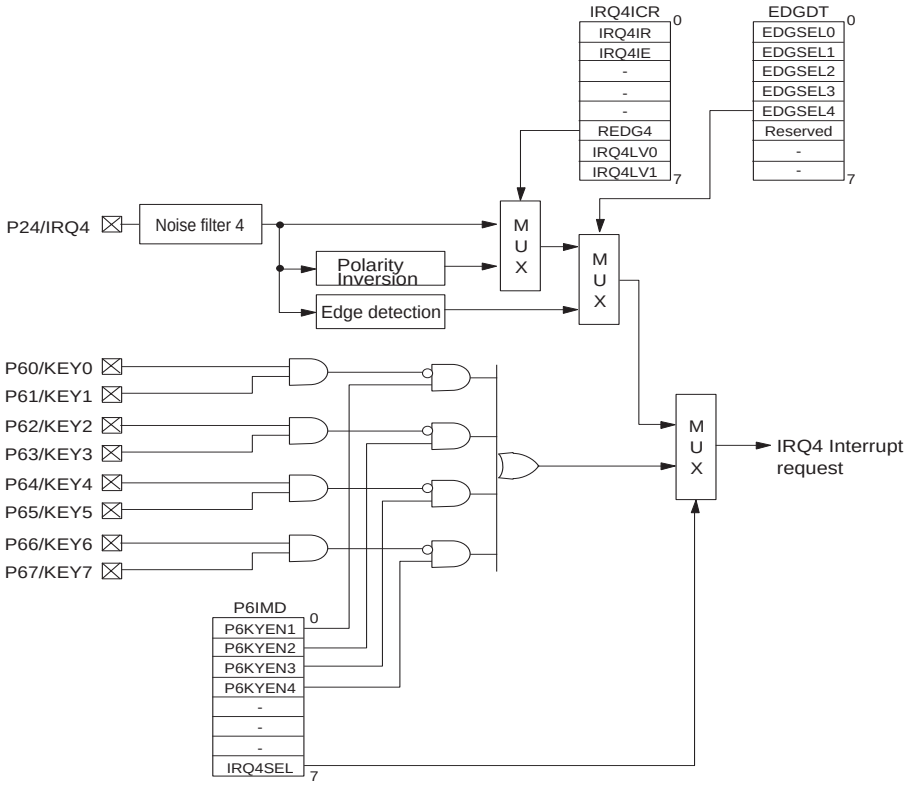


Figure 3-3-3 External Interrupt 4 Interface Block Diagram

3-3-3 Control Registers

The external interrupt input signal, which operated in each external interrupt 0 to 4 interface generate interrupt requests.

External interrupt 0 to 4 interface are controlled by the external interrupt control register (IRQnICR) and the both edges interrupt control register (EDGDT). And external interrupt interface 0 to 1 are controlled by the noise filter control register (NFCTR0), external interrupt interface 2 to 4 are controlled by the noise filter control register (NFCTR1), and external interrupt interface 4 is controlled the port 6 key interrupt control register (P6IMD).

Table 3-3-2 shows the list of registers, control external interrupt 0 to 4.

Table 3-3-2 External Interrupt Control Register

External Interrupt	Register	Address	R/W	Function	Page
External interrupt 0	IRQ0ICR	x'03FE2'	R/W	External interrupt 0 control register	III -17
	EDGDT	x'03F8F'	R/W	Both edges interrupt control register	III -49
	NFCTR0	x'03F8E'	R/W	Noise filter control register 0	III -47
External interrupt 1	IRQ1ICR	x'03FE3'	R/W	External interrupt 1 control register	III -18
	EDGDT	x'03F8F'	R/W	Both edges interrupt control register	III -49
	NFCTR0	x'03F8E'	R/W	Noise filter control register 0	III -47
External interrupt 2	IRQ2ICR	x'03FE4'	R/W	External interrupt 2 control register	III -19
	EDGDT	x'03F8F'	R/W	Both edges interrupt control register	III -49
	NFCTR1	x'03F8D'	R/W	Noise filter control register 1	III -48
External interrupt 3	IRQ3ICR	x'03FE5'	R/W	External interrupt 3 control register	III -20
	EDGDT	x'03F8F'	R/W	Both edges interrupt control register	III -49
	NFCTR1	x'03F8D'	R/W	Noise filter control register 1	III -48
External interrupt 4	IRQ4ICR	x'03FE6'	R/W	External interrupt 4 control register	III -21
	EDGDT	x'03F8F'	R/W	Both edges interrupt control register	III -49
	P6IMD	x'03F3E'	R/W	Port 6 key interrupt control register	III -50
	NFCTR1	x'03F8D'	R/W	Noise filter control register 1	III -48

R/W : Readable / Writable.

■Noise Filter Control Register 0 (NFCTR0)

The noise filter control register (NFCTR0) sets the noise remove function for IRQ0 and IRQ1 and also selects the sampling cycle of noise remove function. And this register also set the AC zero cross detection function for IRQ1.

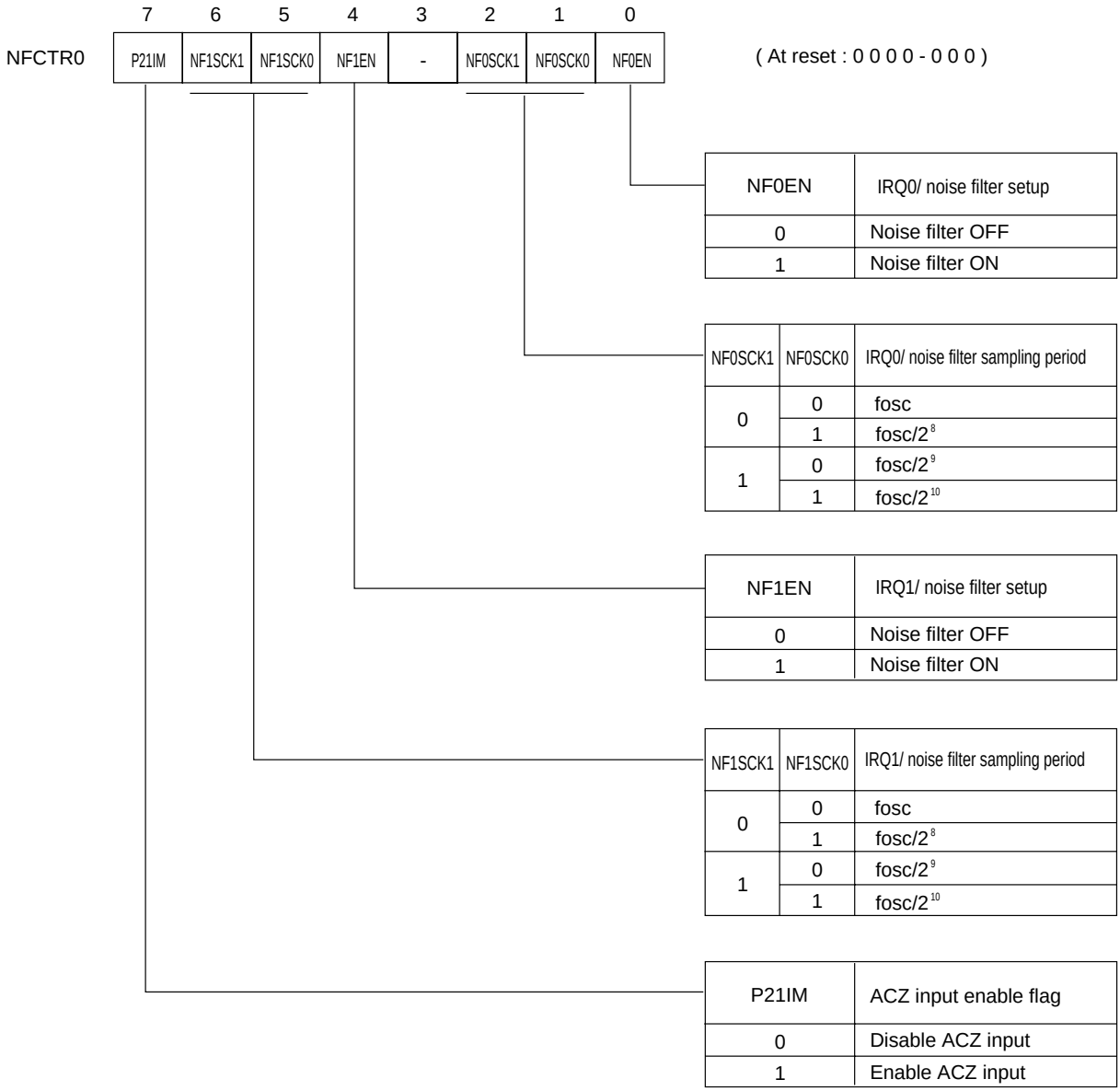


Figure 3-3-4 Noise Filter Control Register 0 (NFCTR0 : x'03F8E', R/W)

■Noise Filter Control Register 1 (NFCTR1)

The noise filter control register (NFCTR1) sets the noise remove function for IRQ2 to IRQ4.

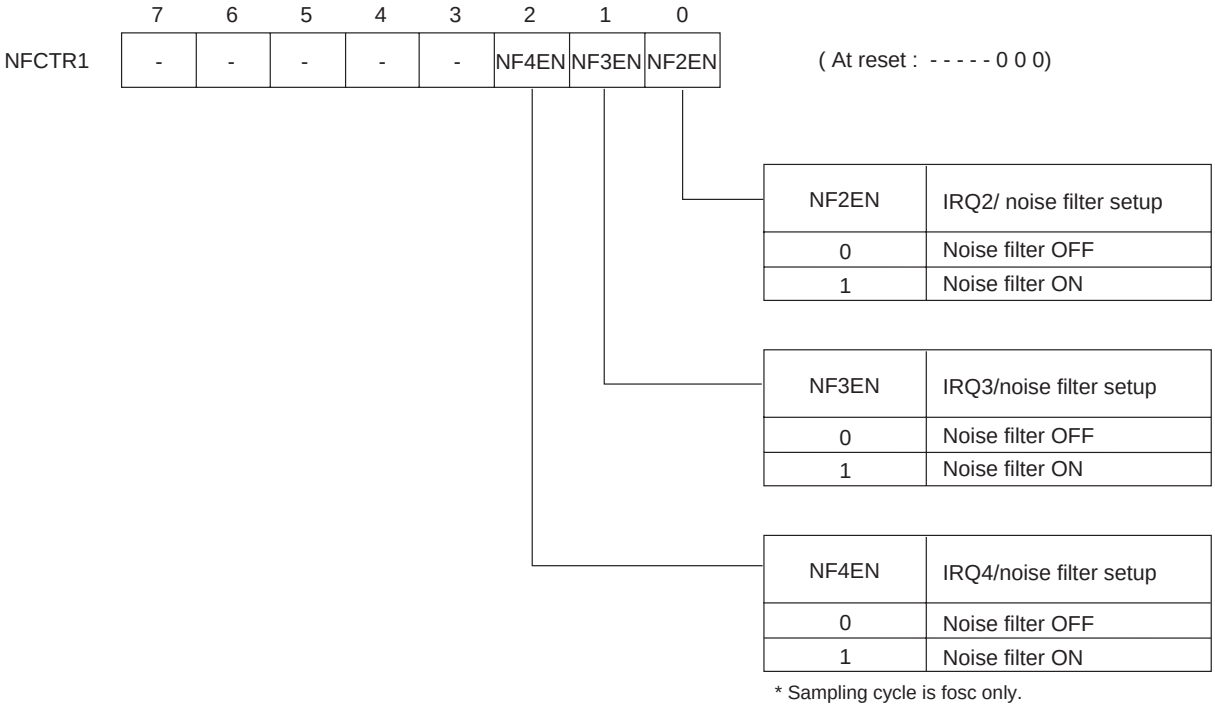


Figure 3-3-5 Noise Filter Control Register 1 (NFCTR1 : x'03F8D', R/W)

■Both Edges Interrupt Control Register (EDGDT)

The both edges interrupt control register (EDGDT) selects interrupt edges of IRQ0 to IRQ4. Interrupts are generated at both edges, or at single edge. The external interrupt control register (IRQ0ICR to IRQ4ICR) specifies whether interrupts are generated.

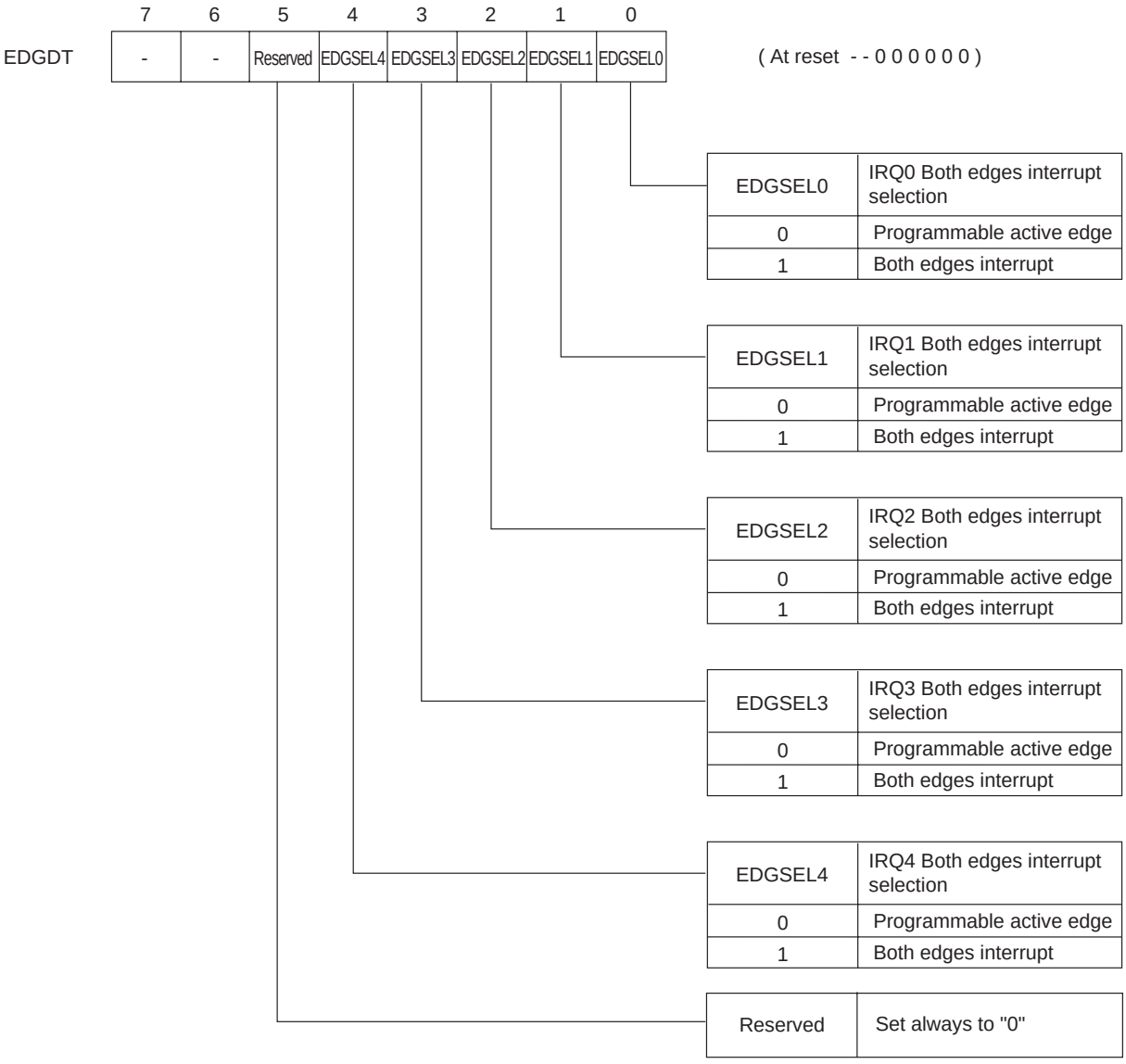


Figure 3-3-6 Both Edges Interrupt Control Register (EDGDT : x'03F8F', R/W)

■Port 6 Key Interrupt Control Register (P6IMD)

The port 6 key interrupt control register (P6IMD) selects if key interrupt is approved, and if external interrupt IRQ4 is approved. Also, this register selects, by 2 bits, which pin on port 6 approved key interrupt.

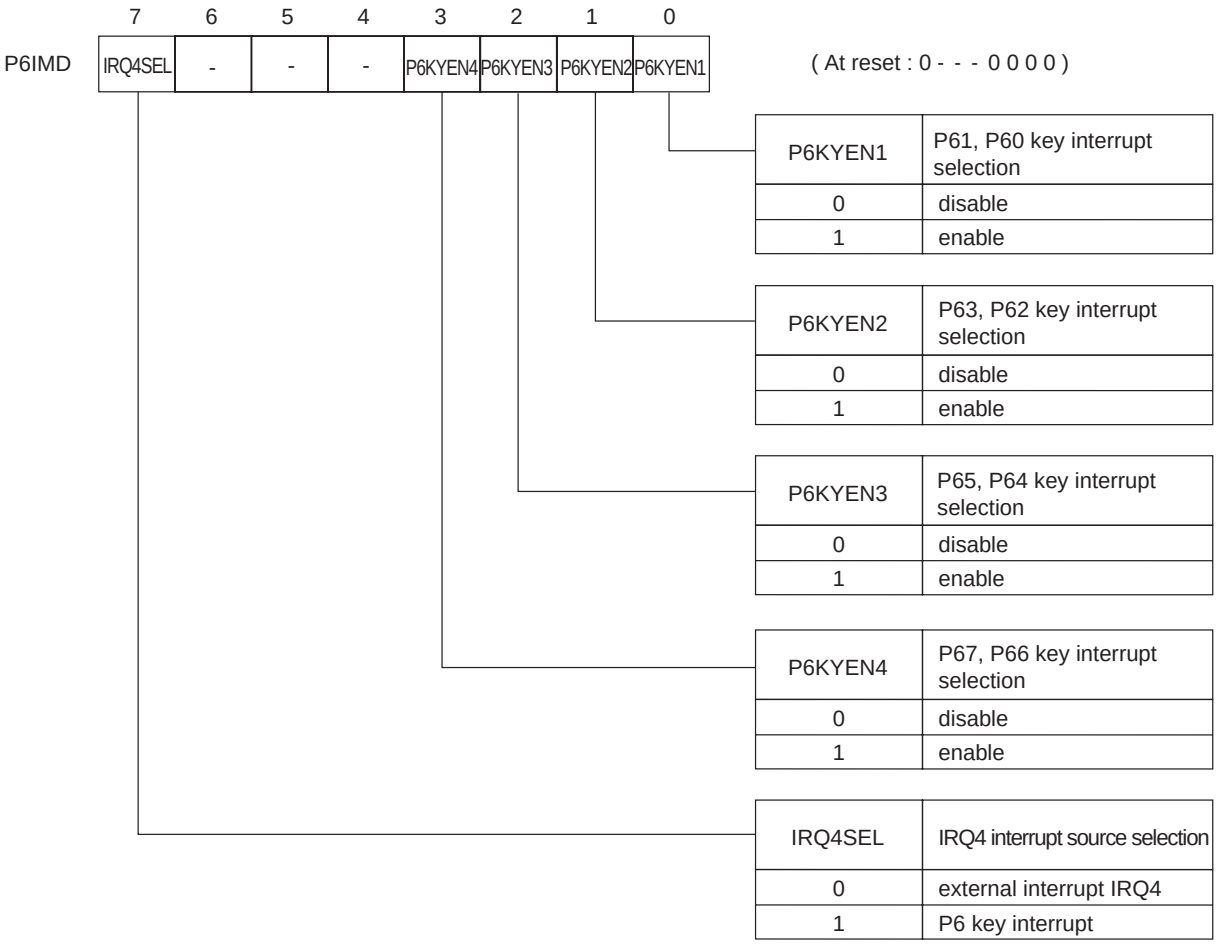


Figure 3-3-7 Port 6 Key Interrupt Control Register (P6IMD : x'03F3E', R/W)

3-3-4 Programmable Active Edge Interrupt

■Programmable Active Edge Interrupts (External interrupts 0 to 4)
Through register settings, external interrupts 0 to 5 can generate interrupt at the selected edge either rising or falling edge.

■Programmable Active Edge Interrupt Setup Example (External interrupt 0 to 4)
External interrupt 4 (IRQ4) is generated at the rising edge of the input signal from P24.
The table below provides a setup example for IRQ4.

Setup Procedure	Description
(1) Specify the interrupt active edge. IRQ4ICR (x'3FE6') bp5 : REDG4 = 1	(1) Set the REDG4 flag of the external interrupt 4 control register (IRQ4ICR) to "1" to specify the rising edge as the active edge for interrupts.
(2) Set the interrupt level. IRQ4ICR (x'3FE6') bp7-6 : IRQ4LV1-0= 10	(2) Set the interrupt priority level in the IRQ4LV1-0 flag of the IRQ4ICR register. If the interrupt request flag has been already set, clear it. [☞ Chapter 3. 3-1-4 Interrupt flag setup]
(3) Enable the interrupt. IRQ4ICR (x'3FE6') bp1 : IRQ4IE = 1	(3) Set the IRQ4IE flag of the IRQ4ICR register to "1" to enable the interrupt.

External interrupt 4 is generated at the rising edge of the input signal from P24.

The Interrupt request flag can be set to "1" at switching the interrupt edge, so specify the interrupt active edge before the interrupt permission.

The external interrupt pin is recommended to be pull-up in advance.

When the programmable active edge interrupt is specified for external interrupt 0 to 4 (IRQ0 to IRQ4), set the EDGSELn flag of the both edge interrupt control register (EDGDT) to "0".

3-3-5 Both Edges Interrupt

■Both Edges Interrupt (External interrupts 0 to 4)

Both edges interrupt can generate interrupt at both the falling edge and the rising edge by the input signal from external input pins. CPU also can be returned from standby mode by both edges interrupt.

■Both Edges Interrupt Setup Example (External interrupts 0 to 4)

External interrupt 2 (IRQ2) is generated at the both edges of the input signal from P22 pin.
An example setup procedure, with a description of each step is shown below.

Setup Procedure	Description
(1) Select the both edges interrupt. EDGDT (x'3F8F') bp2 : EDGSEL2 = 1	(1) Set the EDGSEL2 flag of the both edges interrupt control register (EDGDT) to "1" to select the both edges interrupt.
(2) Set the interrupt level. IRQ2ICR (x'3FE4') bp7-6 : IRQ2LV1- 0 = 10	(2) Set the interrupt level by the IRQ2LV1-0 flag of the IRQ2ICR register. The interrupt request flag of the IRQ2ICR register may be set, so make sure to clear the interrupt request flag (IRQ2IR). [☞ Chapter 3 3-1-4 Interrupt flag setup]
(3) Enable the interrupt. IRQ2ICR (x'3FE4') bp1 : IRQ2IE = 1	(3) Set the IRQ2IE flag of the IRQ2ICR register to "1" to enable the interrupt.

At the both edge of the input signal from P22 pin, an external interrupt 2 is generated .

When the both edge interrupt is selected, the interrupt request generates at the both edge, regardless of the REDGn flag of the external interrupt control register (IRQnICR).

The interrupt request flag may be set to "1" at switching the interrupt edge. So, clear the interrupt request flag before the interrupt enable. Also, select the both edge interrupt before the interrupt enable.

The external interrupt pin is recommended to be pull-up, in advance.

3-3-6 Key Input Interrupt

■Key Input Interrupt (External interrupt 4)

This LSI can set port 6 pin (P60 to P67) by 2 bits to key input pin. Key input interrupt can generate an interrupt at the falling edge, if at least 1 key input pin outputs low level.

Key input pin should be pull-up in advance.

When key input interrupt is used, set the IRQ4SEL flag of the port6 key interrupt control register (P6IMD) to "1".

When key input interrupt is used, set the REDG4 flag of the external interrupt 4 control register (IRQ4ICR) to "0" (falling edge).

■Key Input Interrupt Setup Example (External interrupt 4)

After P60 to P63 of port 6 are set to key input pins and key is input (low level), the external interrupt 4 (IRQ4) is generated. An example setup procedure, with a description of each step is shown below.

Setup Procedure	Description
(1) Set the key input pin to input. P6DIR (x'3F36') bp3-0 : P6DIR3-0 = 0000	(1) Set the P6DIR3-0 flag of the port 6 direction control register (P6DIR) to "0000" to set P60 to P63 pins to input pins.
(2) Set the pull-up resistance. P6PLU (x'3F46') bp3-0 : P6PLU3-0 = 1111	(2) Set the P6PLU 3-0 flag of the port 6 pull-up resistance control register (P6PLU) to"1111" to add the pull-up resistance to P60 to P63 pins.
(3) Select the key input interrupt. P6IMD (x'3F3E') bp7 : IRQ4SEL = 1	(3) Set the IRQ4SEL flag of the port 6 key interrupt control register (P6IMD) to "1" to select the external interrupt 4 source to the port 6 key interrupt.
(4) Select the key input pin. P6IMD (x'3F3E') bp1-0 : P6KYEN2-1= 11	(4) Set the P6KYEN 2-1 flag of the port 6 key interrupt control register (P6IMD) to "11" to set P60 to P63 pins to key input pins.
(5) Set the interrupt level. IRQ4ICR (x'3FE6') bp7-6 : IRQ4LV1-0= 10	(5) Set the interrupt level by the IRQ4LV1-0 flag of the IRQ4ICR register. If the interrupt request flag has been already set, clear the it. [☞ Chapter 3 3-1-4. Interrupt flag setup]
(6) Enable the interrupt. IRQ4ICR (x'3FE6') bp1 : IRQ4IE = 1	(6) Set the IRQ4IE flag of the IRQ4ICR register to "1" to enable the interrupt.

Note : The above (3) and (4) are set at the same time.

If there is at least one input signal, from the P60 to P63 pins, shows low level, the external interrupt 4 is generated at the falling edge.

The setup of the key input should be done before the interrupt is enabled.

3-3-7 Noise Filter

■Noise Filter (External interrupts 0 to1)
Noise filter reduce noise by sampling the input waveform from the external interrupt pins (IRQ0, IRQ1). Its sampling cycle can be selected from 4 types (fosc, fosc/2^8, fosc/2^9, fosc/2^{10}).

■Noise Remove Selection (External interrupts 2 to 4)
Noise filter reduce noise by sampling the input waveform from the external interrupt pins (IRQ2 to IRQ4). Its sampling cycle is fosc.

■Noise Remove Selection (External interrupts 0 to 4)
Noise remove function can be selected by setting the NFnEN flag of the noise filter control register (NFCTR) to "1".

Table 3-3-3 Noise Remove Function

NFnEN	0	1
IRQ0 input (P20)	IRQ0 Noise filter OFF	IRQ0 Noise filter ON
IRQ1 input (P21)	IRQ1 Noise filter OFF	IRQ1 Noise filter ON
IRQ2 input (P22)	IRQ2 Noise filter OFF	IRQ2 Noise filter ON
IRQ3 input (P23)	IRQ3 Noise filter OFF	IRQ3 Noise filter ON
IRQ4 input (P24)	IRQ4 Noise filter OFF	IRQ4 Noise filter ON

■Sampling Cycle Setup (External interrupts 0 and 1)
The sampling cycle of noise remove function can be set by the NFnSCK 1- 0 flag of the NFCTR register.

Table 3-3-4 Sampling Cycle / Time of Noise Remove Function

NFnCKS1	NFnCKS0	Sampling cycle	High-Speed oscillation			
			fosc=20 MHz		fosc=8 MHz	
0	0	fosc	20 MHz	50 ns	8 MHz	125 ns
	1	fosc/2^8	78.13 kHz	12.80 μs	31.25 kHz	32 μs
1	0	fosc/2^9	39.06 kHz	25.60 μs	15.62 kHz	64 μs
	1	fosc/2^{10}	19.53 kHz	51.20 μs	7.81 kHz	128 μs

■Noise Remove Function Operation (External interrupts 0 to 4)

After sampling the input signal to the external interrupt pins (IRQ0 to IRQ4) by the set sampling time, if the same level comes continuously three times, that level is sent to the inside of LSI. If the same level does not come continuously three times, the previous level is sent. It means that only the signal with the width of more than " Sampling time X 3 sampling clock " can pass through the noise filter, and other much narrower signals are removed, because those are regarded as noise.

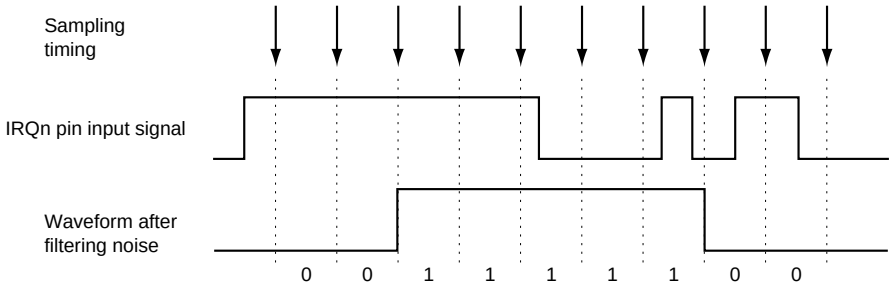


Figure 3-3-8 Noise Remove Function Operation

Noise filter can not be used at STOP mode, HALT mode and SLOW mode.

■Noise Filter Setup Example (External interrupt 0 and 1)

Noise remove function is added to the input signal from P20 pin to generate the external interrupt 0 (IRQ0) at the rising edge. The sampling clock is set to fosc, and the operation state is fosc = 20 MHz. An example setup procedure, with a description of each step is shown below.

Setup Procedure	Description
(1) Specify the interrupt active edge. IRQ0ICR (x'3FE2') bp5 : REDG0 = 1	(1) Set the REDG0 flag of the external interrupt 0 control register (IRQ0ICR) to "1" to specify the interrupt active edge to the rising edge.
(2) Select the sampling clock. NFCTR0 (x'3F8E') bp2-1 : NF0SCK1-0 = 00	(2) Select the sampling clock to fosc by the NF0SCK 1-0 flag of the noise filter control register (NFCTR0).
(3) Set the noise filter operation. NFCTR0 (x'3F8E') bp0 : NF0EN = 1	(3) Set the NF0EN flag of the NFCTR0 register to "1" to add the noise filter operation.
(4) Set the interrupt level. IRQ0ICR (x'3FE2') bp7-6 : IRQ0LV1-0= 10	(4) Set the interrupt level by the IRQ0LV 1- 0 flag of the IRQ0ICR register. If the interrupt request flag has been already set, clear the request flag. [☞ Chapter 3 3-1-4. Interrupt flag setup]
(5) Enable the interrupt. IRQ0ICR (x'3FE2') bp1 : IRQ0IE = 1	(5) Set the IRQ0IE flag of the IRQ0ICR register to "1" to enable the interrupt.

Note : The above (2) and (3) are set at the same time.

The input signal from the P20 pin generates the external interrupt 0 at the rising edge of the signal, after passing through the noise filter.

The setup of the noise filter should be done before the interrupt is enabled.

The external interrupt pins are recommended to be pull-up in advance.

3-3-8 AC Zero-Cross Detector

This LSI has AC zero-cross detector circuit. The P21 / ACZ pin is the input pin of AC zero-cross detector circuit. AC zero-cross detector circuit output the high level when the input level is at the middle, and outputs the low level at other level.

■AC Zero-Cross Detector (External interrupt 1)
AC zero-cross detector sets the IRQ1 pin to the high level when the input signal (P21/ACZ pin) is at intermediate range. At the other level, IRQ1 pin is set to the low level. AC zero-cross can be detected by setting the P21IM flag of the noise filter control register (NFCTR) to "1".

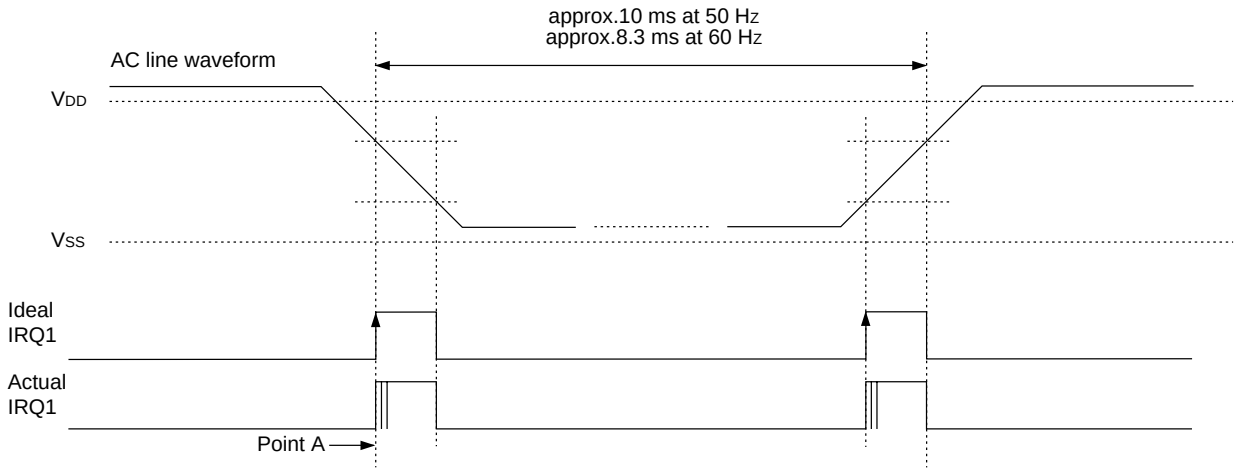


Figure 3-3-9 AC Line Waveform and IRQ1 Generation Timing

Actual IRQ1 interrupt request is generated several times at crossing the 1/2 V_{DD} of AC line waveform. So, the filtering operation by the program is needed.

The interrupt request is generated at the rising edge of the AC zero-cross detector signal.

■AC Zero-Cross Detector Setup Example (External interrupt 1)

AC zero-cross detector generates the external interrupt 1 (IRQ1) by using P21/ACZ pin.
An example setup procedure, with a description of each step is shown below.

Setup Procedure	Description
(1) Select the AC zero-cross detector signal. NFCTR0 (x'3F8E') bp7 : P21IM = 1	(1) Set the P21IM flag of the noise filter control register (NFCTR0) to "1" to select the AC zero-cross detector signal as the external interrupt 1 generation factor.
(2) Set the interrupt level. IRQ1ICR (x'3FE3') bp7-6 : IRQ1LV1-0= 10	(2) Set the interrupt level by the IRQ1LV 1-0 flag of the IRQ1ICR register. If the interrupt request flag has been already set, clear the interrupt flag. [☞ Chapter 3 3-1-4. Interrupt flag setup]
(3) Enable the interrupt. IRQ1ICR (x'3FE3') bp1 : IRQ1IE = 1	(3) Set the IRQ1IE flag of the IRQ1ICR register to "1" to enable the interrupt.

When the input signal level from P21/ACZ pin crosses 1/2 V_{DD}, the external interrupt 1 is generated.

Chapter 4 I/O Ports

4-1 Overview

4-1-1 I/O Port Diagram

A total of 54 pins on this LSI, including those shared with special function pins, are allocated for the 8 I/O ports of ports 0 to 2, ports 5 to 8 and port A. Each I/O port is assigned to its corresponding special function register area in memory. I/O ports are operated in byte or bit units in the same way as RAM.

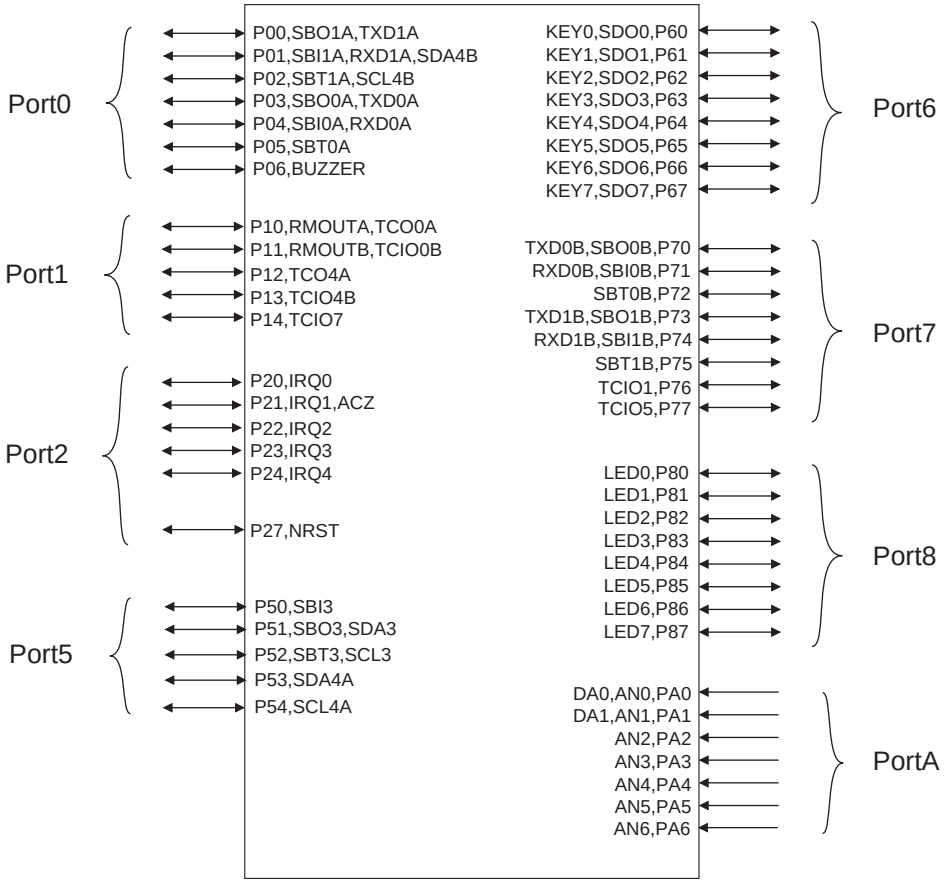


Figure 4-1-1 I/O Port Functions

4-1-2 I/O Port Status at Reset

Table 4-1-1 I/O Port Status at Reset (Single chip mode)

Port Name	I/O mode	Pull-up / Pull-down resistor	I/O port, special functions
Port 0	Input mode	No pull-up resistor	I/O port
Port 1	Input mode	No pull-up resistor	I/O port
Port 2	Input mode	P27 : Pull-up resistor Others : No pull-up resistor	I/O port
Port 5	Input mode	No pull-up resistor	I/O port
Port 6	Input mode	No pull-up resistor	I/O port
Port 7	Input mode	No pull-up / pull-down resistor	I/O port
Port 8	Input mode	No pull-up resistor	I/O port
Port A	Input mode	No pull-up / pull-down resistor	I/O port

4-1-3 Control Registers

Ports 0 to 2, ports 5 to 8 and port A are controlled by the data output register (PnOUT), the data input register (PnIN), the I/O direction control register (PnDIR), the pull-up resistor control register (PnPLU) and the pull-up / pull-down resistor control resister (PnPLUD) and registers (P1OMD, P1TCNT, PAIMD, FLOAT) that control special function pin.

Table 4-1-3 shows the registers to control ports 0 to 2, Ports 5 to 8 and Port A ;

Table 4-1-2 I/O Port Control Registers List (1/2)

	Register	Address	R/W	Function	Page
Port 0	P0OUT	x'03F10'	R/W	Port 0 output register	IV-7
	P0IN	x'03F20'	R	Port 0 input register	IV-7
	P0DIR	x'03F30'	R/W	Port 0 direction control register	IV-7
	P0PLU	x'03F40'	R/W	Port 0 pull-up resistor control register	IV-7
Port 1	P1OUT	x'03F11'	R/W	Port 1 output register	IV-13
	P1IN	x'03F21'	R	Port 1 input register	IV-13
	P1DIR	x'03F31'	R/W	Port 1 direction control register	IV-13
	P1PLU	x'03F41'	R/W	Port 1 pull-up resistor control register	IV-13
	P1OMD	x'03F2F'	R/W	Port 1 output mode register	IV-14
	P1TCNT	x'03F7E'	R/W	Port 1 output control register	IV-14
Port 2	P2OUT	x'03F12'	R/W	Port 2 output register	IV-17
	P2IN	x'03F22'	R	Port 2 input register	IV-17
	P2DIR	x'03F32'	R/W	Port 2 direction control register	IV-17
	P2PLU	x'03F42'	R/W	Port 2 pull-up resistor control register	IV-17
Port 5	P5OUT	x'03F15'	R/W	Port 5 output register	IV-21
	P5IN	x'03F25'	R	Port 5 input register	IV-21
	P5DIR	x'03F35'	R/W	Port 5 direction control register	IV-21
	P5PLU	x'03F45'	R/W	Port 5 pull-up resistor control register	IV-21
Port 6	P6OUT	x'03F16'	R/W	Port 6 output register	IV-27
	P6IN	x'03F26'	R	Port 6 input register	IV-27
	P6DIR	x'03F36'	R/W	Port 6 direction control register	IV-27
	P6PLU	x'03F46'	R/W	Port 6 pull-up resistor control register	IV-27
	P6SYO	x'03F1E'	R/W	Port 6 synchronous output control register	IV-28

Table 4-1-3 I/O Port Control Registers List (2/2)

	Register	Address	R/W	Function	Page
Port 7	P7OUT	x'03F17'	R/W	Port 7 output register	IV-31
	P7IN	x'03F27'	R	Port 7 input register	IV-31
	P7DIR	x'03F37'	R/W	Port 7 direction control register	IV-31
	P7PLUD	x'03F47'	R/W	Port 7 pull-up / pull-down resistor control register	IV-31
Port 8	P8OUT	x'03F18'	R/W	Port 8 output register	IV-38
	P8IN	x'03F28'	R	Port 8 input register	IV-38
	P8DIR	x'03F38'	R/W	Port 8 direction control register	IV-38
	P8PLU	x'03F48'	R/W	Port 8 pull-up resistor control register	IV-38
	P8LED	x'03F1D'	R/W	Port 8 LED control register	IV-39
Port A	PAOUT	x'03F1A'	R/W	Port A output register	IV-42
	PAIN	x'03F2A'	R	Port A input register	IV-42
	PADIR	x'03F3A'	R/W	Port A direction control register	IV-42
	PAPLUD	x'03F4A'	R/W	Port A pull-up / pull-down resistor control register	IV-42
	PAIMD	x'03F3C'	R/W	Port A input control register	IV-43
Pin Control	FLOAT	x'03F2E'	R/W	Pull-up / Pull-down resistor selection, pin control register	IV-28, 32, 43

4-2 Port 0

4-2-1 Description

■General Port Setup
Each bit of the port 0 control I/O direction register (P0DIR) can be set individually to set each pin as input or output. The control flag of the port 0 direction control register (P0DIR) should be set to "1" for output mode, and "0" for input mode.

To read input data of pin, set the control flag of the port 0 direction control register (P0DIR) to "0" and read the value of the port 0 input register (P0IN).

To output data to pin, set the control flag of the port 0 direction control register (P0DIR) to "1" and write the value of the port 0 output register (P0OUT).

Each bit can be set individually whether pull-up resistor is added or not, by the port 0 pull-up resistor control register (P0PLU). Set the control flag of the port 0 pull-up resistor control register (P0PLU) to "1" to add pull-up resistor.

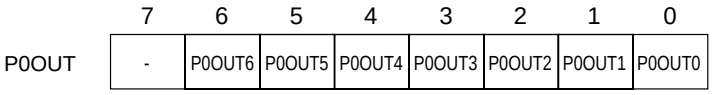
■Special Function Pin Setup
P00 to P02 are used as I/O pin for serial interface 0, as well. P00 is output pin of the serial interface 1 transmission data. The SC1SBOS flag of the serial interface 1 mode register 1 (SC1MD1) is set to "1" for serial data output. P01 is the input pin of the serial interface 1 reception data. P02 is I/O pin of the serial interface 1 clock. The SC1SBTS flag of serial interface 1 mode register 1 (SC1MD1) is set to "1" for serial clock output.

P03 to P05 are used as I/O pin for serial interface 0, as well. P03 is output pin of the serial interface 0 transmission data. The SC0SBOS flag of the serial interface 0 mode register 1 (SC0MD1) is set to "1" for serial data output. P04 is the serial interface 0 reception data input pin. P05 is I/O pin of the serial interface 0 clock. The SC0SBTS flag of serial interface 0 mode register 1 (SC0MD1) is set to "1" for serial clock output pin.

P01 to P02 are used as I/O pin for serial interface 4, as well. P01 is data I/O pin of the serial interface 4. The SELI2C flag of the serial interface 4 address register 1 (SC4AD1) is set to "1" for serial data output pin. P02 is the serial interface 4 clock I/O pin. The SELI2C flag of serial interface 4 address register 1 (SC4AD1) is set to "1" for serial clock I/O.

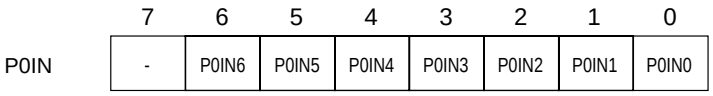
P06 is used as buzzer output pin, as well. When the bp7 of the oscillation stabilization control register (DLYCTR) is "1", buzzer output is enabled.

4-2-2 Registers



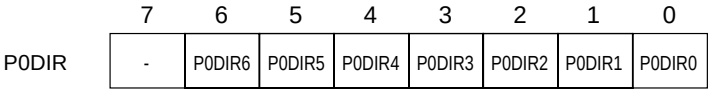
P0OUT	Output data
0	L(V_{SS} level)
1	H(V_{DD} level)

Port 0 output register (P0OUT : x'03F10', R/W)



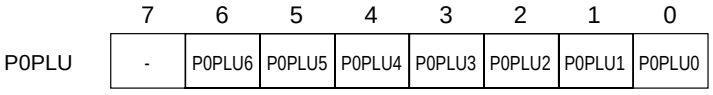
P0IN	Input data
0	Pin is low(V_{SS} level).
1	Pin is high(V_{DD} level).

Port 0 input register (P0IN : x'03F20', R)



P0DIR	I/O mode selection
0	Input mode
1	Output mode

Port 0 direction control register (P0DIR : x'03F30', R/W)



P0PLU	Pull-up resistor selection
0	No pull-up resistor
1	Pull-up resistor

Port 0 pull-up resistor control register (P0PLU : x'03F40', R/W)

Figure 4-2-1 Port 0 Registers

4-2-3 Block Diagram

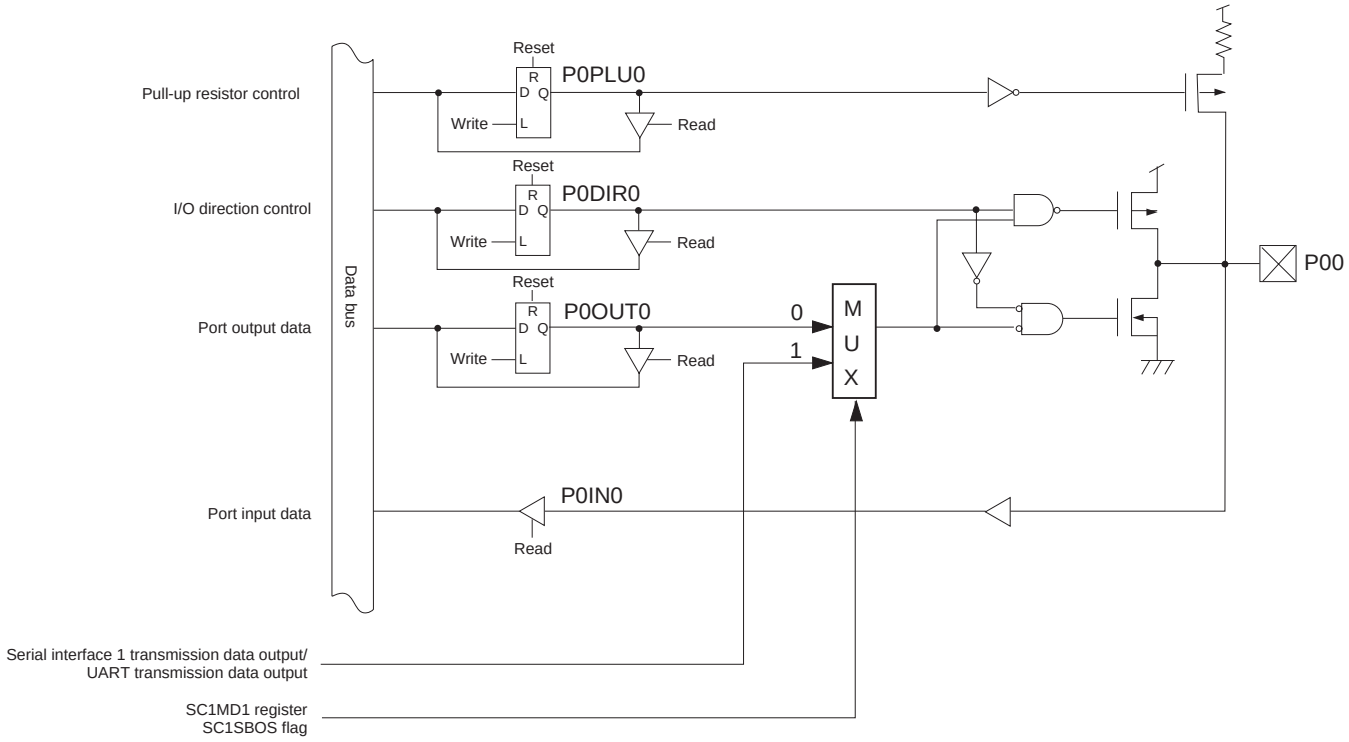


Figure 4-2-2 Block diagram (P00)

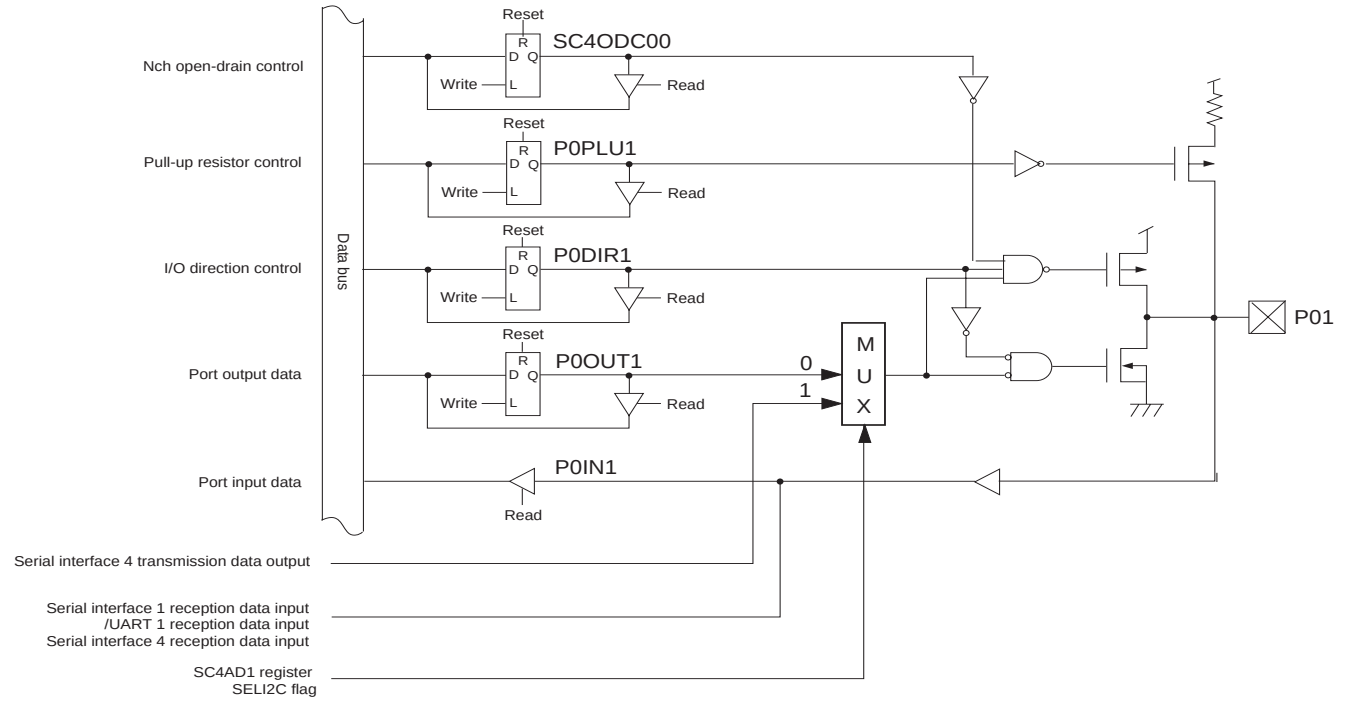


Figure 4-2-3 Block diagram (P01)

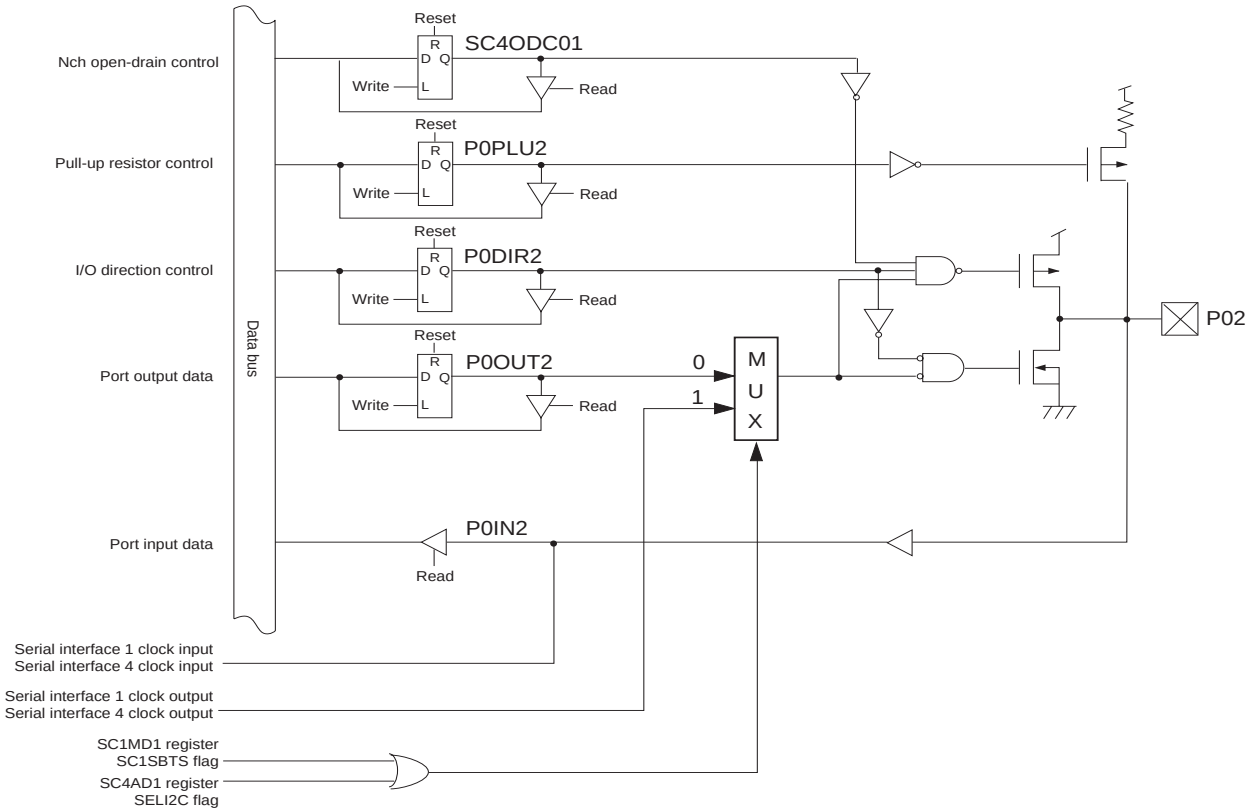


Figure 4-2-4 Block diagram (P02)

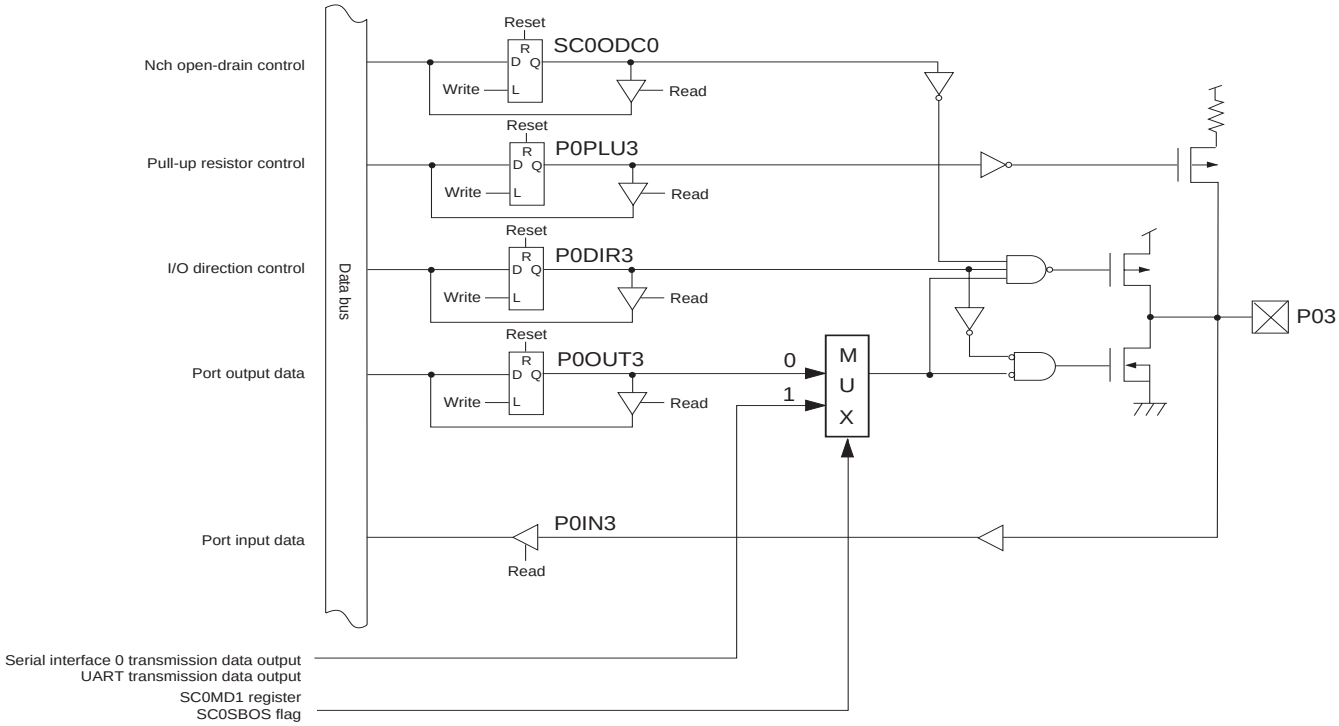


Figure 4-2-5 Block diagram (P03)

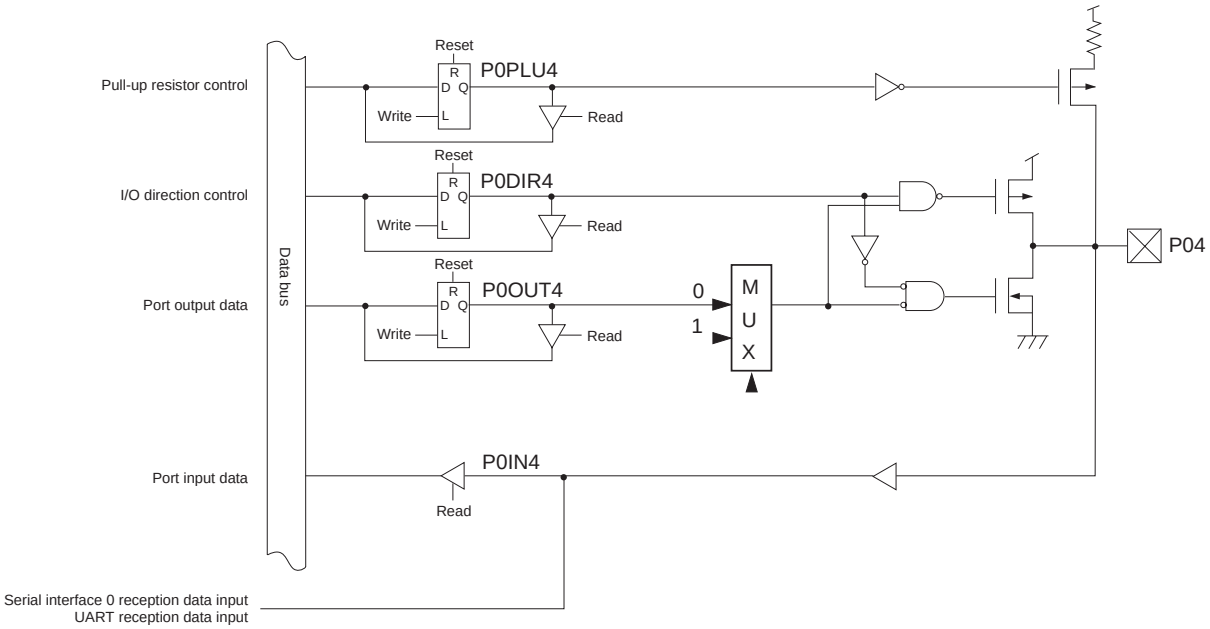


Figure 4-2-6 Block Diagram (P04)

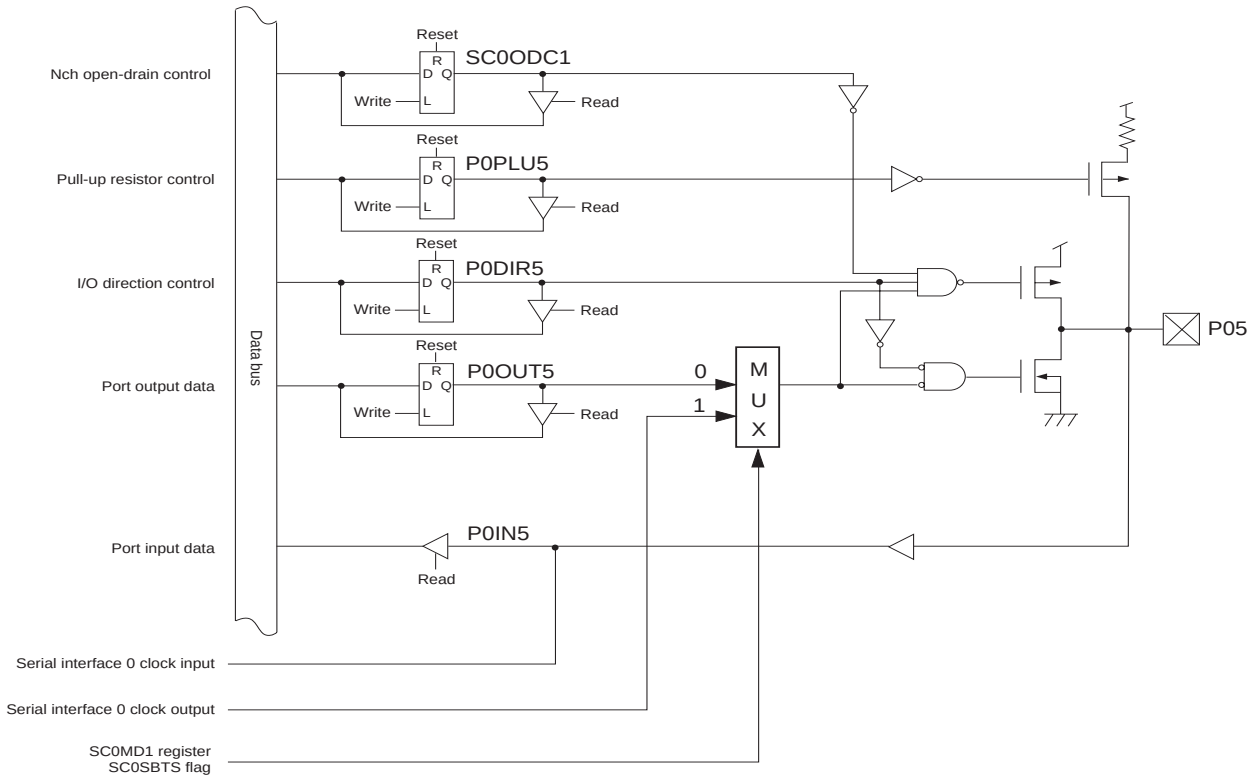


Figure 4-2-7 Block Diagram (P05)

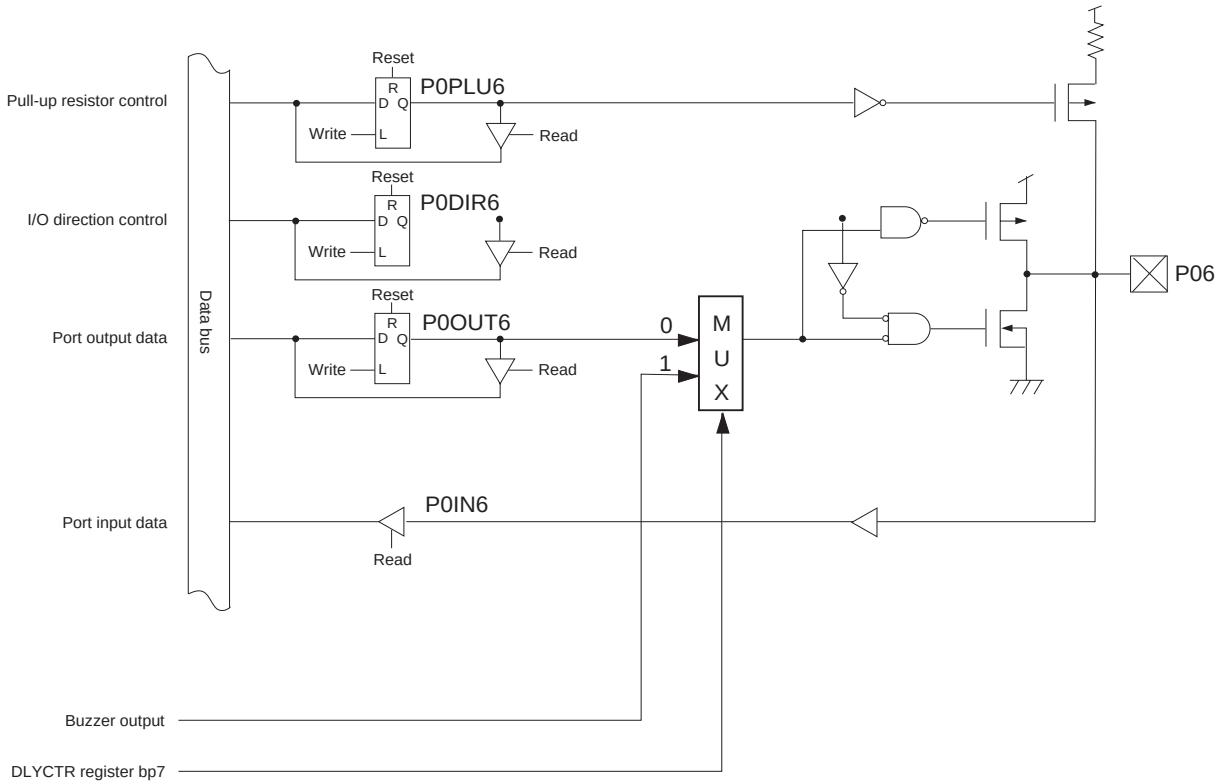


Figure 4-2-8 Block Diagram (P06)

4-3 Port 1

4-3-1 Description

■General Port Setup

Each bit of the port 1 control I/O direction register (P1DIR) can be set individually to set pins as input or output. The control flag of the port 1 direction control register (P1DIR) should be set to "1" for output mode, and "0" for input mode.

To read input data of pin, set the control flag of the port 1 direction control register (P1DIR) to "0" and read the value of the port 1 input register (P1IN).

To output data to pin, set the control flag of the port 1 direction control register (P1DIR) to "1" and write the value of the port 1 output register (P1OUT).

Each bit can be set individually whether pull-up resistor is added or not, by the port 1 pull-up resistor control register (P1PLU). Set the control flag of the port 1 pull-up resistor control register (P1PLU) to "1" to add pull-up resistor.

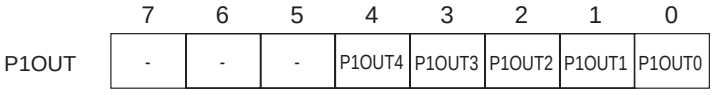
■Special Function Pin Setup

P10, P12 and P14 have real time output control function. P10, P12, and P14 can be used as I/O ports and also switched to 3 types of pin output; "High", "Low", and "Hi-z". P10 is controlled with bp1, bp0, P12 is controlled with bp3, bp2 and P14 is controlled with bp5, bp4 of the port 1 output control register (P1TCNT). When these flags are set to "00", these pins are used as I/O ports. When the pins are set to "01", "High" is output, to "10", "Low" is output and to "11", "High-z" is output.

Also, P10 to P14 are used as timer I/O pin, as well. P10 is used as remote control carrier output pin, as well. The port 1 output mode register (P1OMD) can select P10 to P14 output mode by each bit. When port 1 output mode register (P1OMD) is "1", special function data is output, and when it is "0", they are used as general port.

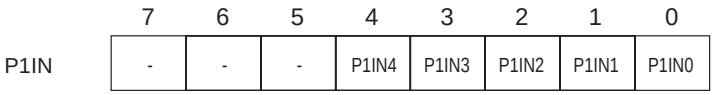
For more information, refer to 4-12 Real Time Output Control Function [p.IV-45].

4-3-2 Registers



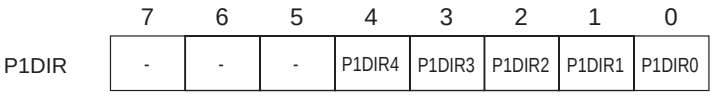
P1OUT	Output data
0	Low (VSS level)
1	High (VDD level)

Port 1 output register (P1OUT : x'03F11', R/W)



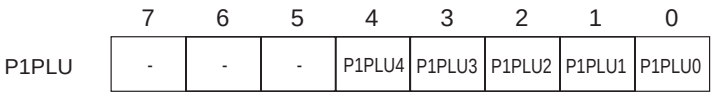
P1IN	Input data
0	Pin is low(VSS level).
1	Pin is high(VDD level).

Port 1 input register (P1IN : x'03F21', R)



P1DIR	I/O mode selection
0	Input mode
1	Output mode

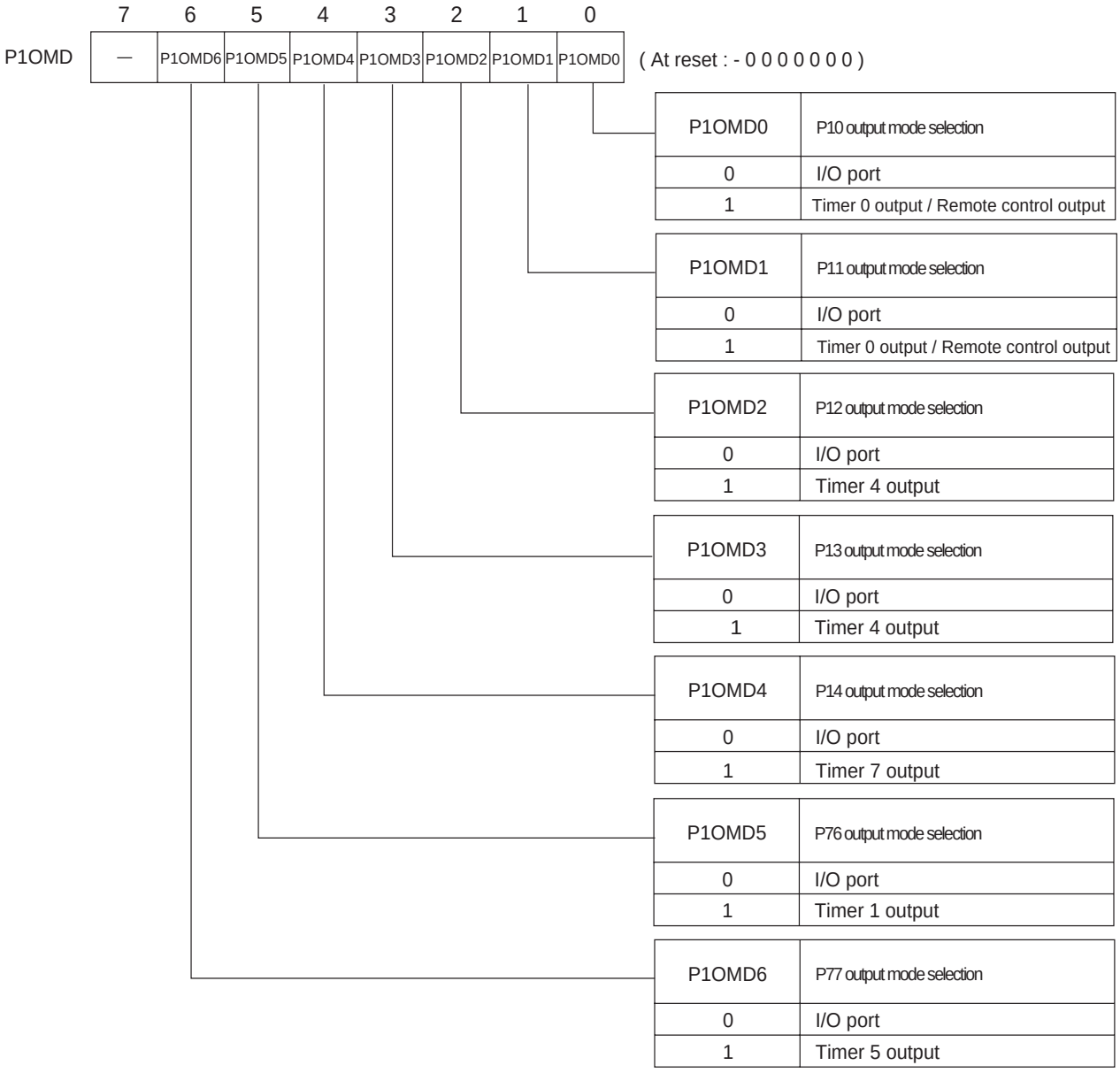
Port 1 direction control register (P1DIR : x'03F31', R/W)



P1PLU	Pull-up resistor selection
0	No pull-up resistor
1	Pull-up resistor

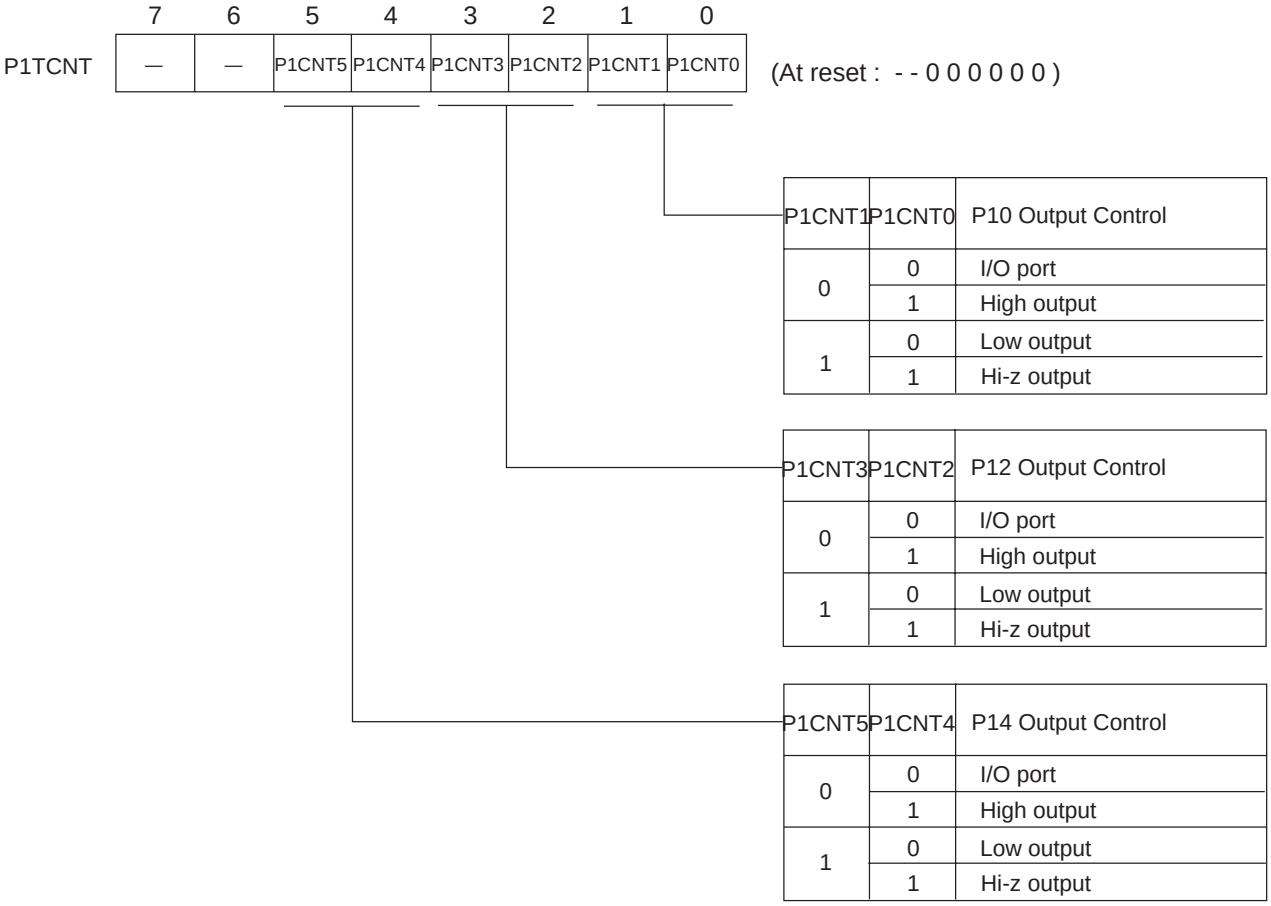
Port 1 pull-up resistor control register (P1PLU : x'03F41', R/W)

Figure 4-3-1 Port 1 Registers (1/3)



Port 1 output mode register (P1OMD: X'03F2F', R/W)

Figure 4-3-2 Port 1 Registers (2/3)



P10 Output Control register (P1TCNT : X'03F7E', R/W)

Figure 4-3-3 Port 1 Registers (3/3)

4-3-3 Block Diagram

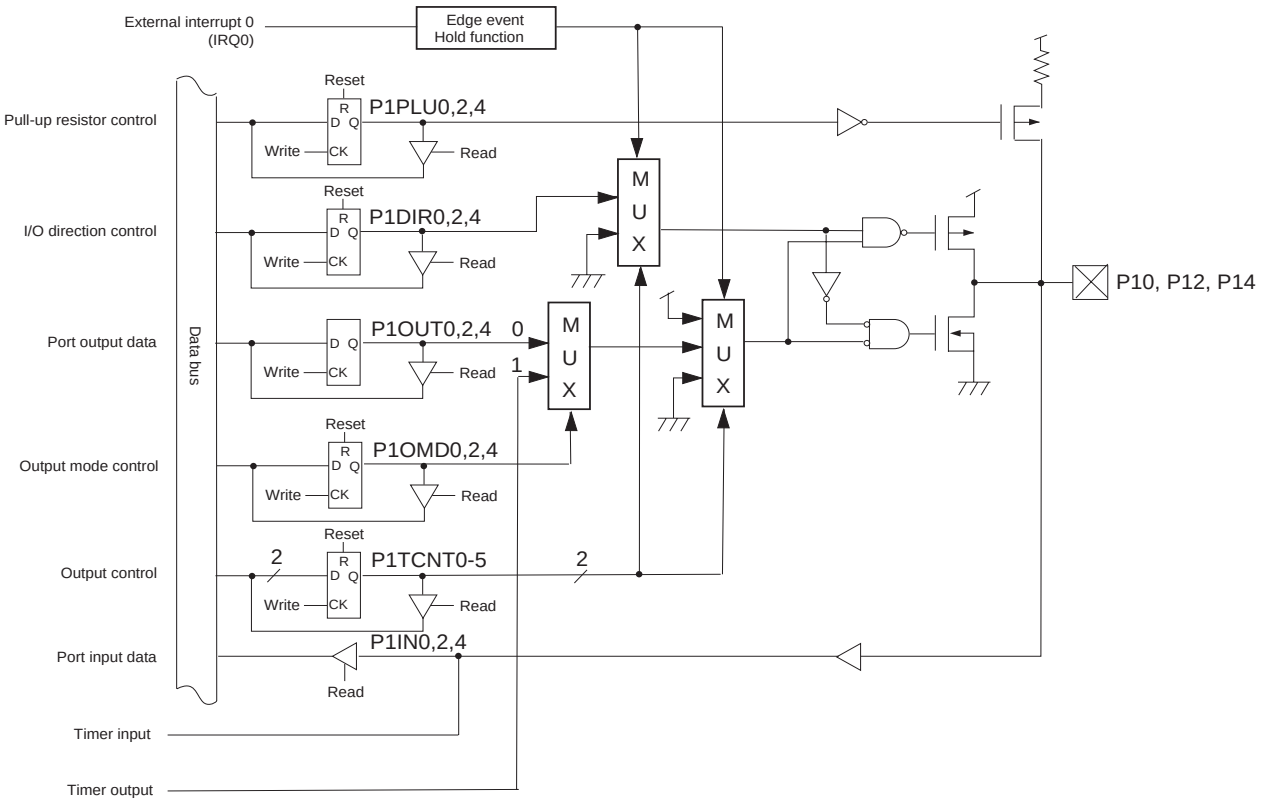


Figure 4-3-4 Block Diagram (P10, P12, P14)

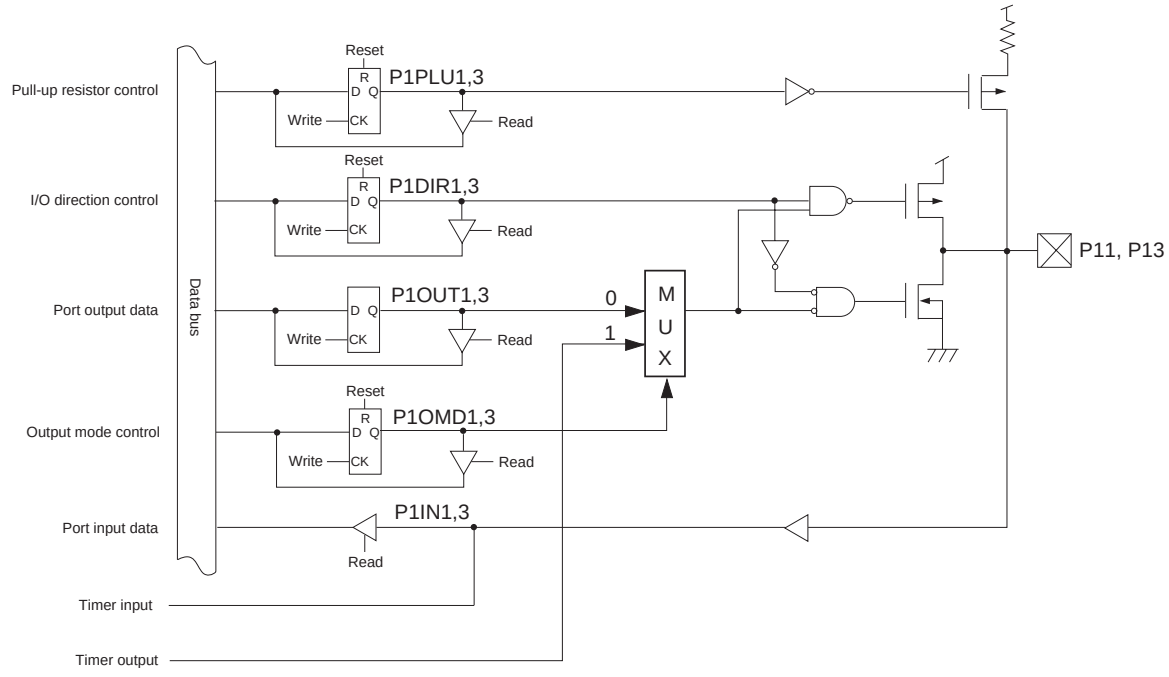


Figure 4-3-5 Block Diagram (P11, P13)

4-4 Port 2

4-4-1 Description

■General Port Setup
Each bit of the port 2 control I/O direction register (P2DIR) can be set individually to set pins as input or output. The control flag of the port 2 direction control register (P2DIR) should be set to "1" for output mode, and "0" for input mode.

To read input data of pin, set the control flag of the port 2 direction control register (P2DIR) to "0" and read the value of the port 2 input register (P2IN).

To output data to pin, set the control flag of the port 2 direction control register (P2DIR) to "1" and write the value of the port 2 output register (P2OUT).

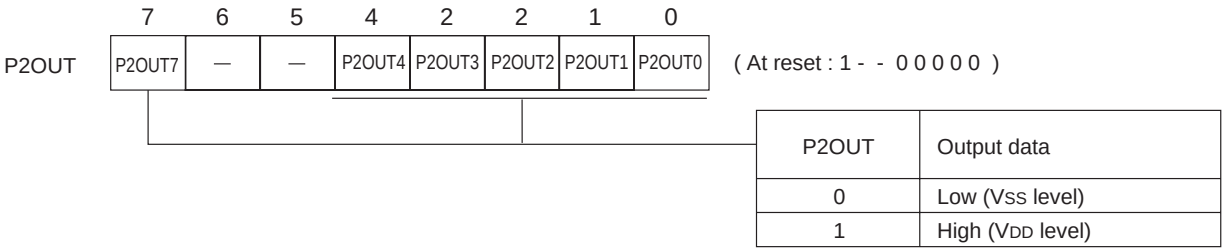
P27 is reset pin. When the software is reset, write the bp7 of the port 2 output register (P2OUT) to "0".

Except P27, each bit can be set individually whether pull-up resistor is added or not, byt the port 2 pull-up resistor control register (P2PLU). When the control flag of the port 2 pull-up resistor control register (P2PLU) is set to "1", pull-up resistor is added. P27 is always added pull-up resistor.

■Special Function Pin Setup
P20 to P24 are used as external interrupt pins, as well.

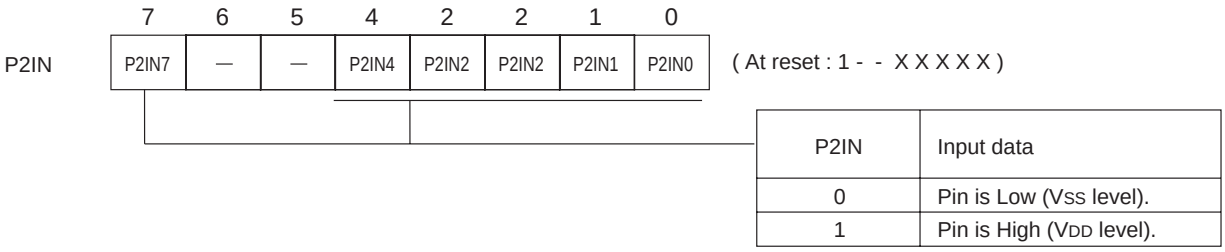
P21 is used as an input pin for external interrupt and AC zero-cross. To read data of AC zero-cross, set the bp7 of the noise filter control register (NFCTR0) to "1" and read the value of the port 2 input register (P2IN).

4-4-2 Registers



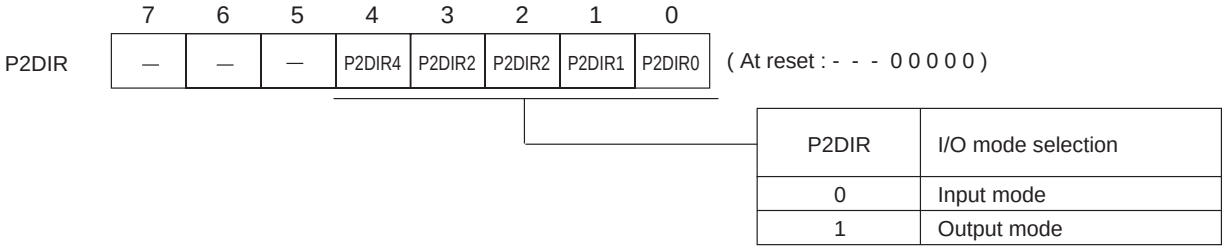
P2OUT	Output data
0	Low (VSS level)
1	High (VDD level)

Port 2 output register(P2OUT : x'02F12', R/W)



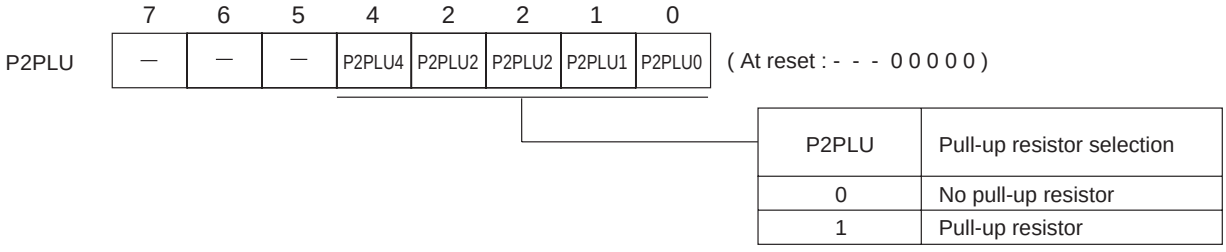
P2IN	Input data
0	Pin is Low (VSS level).
1	Pin is High (VDD level).

Port 2 input register(P2IN : x'02F22', R)



P2DIR	I/O mode selection
0	Input mode
1	Output mode

Port 2 direction control register (P2DIR : x'02F32', R/W)



P2PLU	Pull-up resistor selection
0	No pull-up resistor
1	Pull-up resistor

Port 2 pull-up resistor control register(P2PLU : x'02F42', R/W)

Figure 4-4-1 Port 2 Registers

4-4-3 Block Diagram

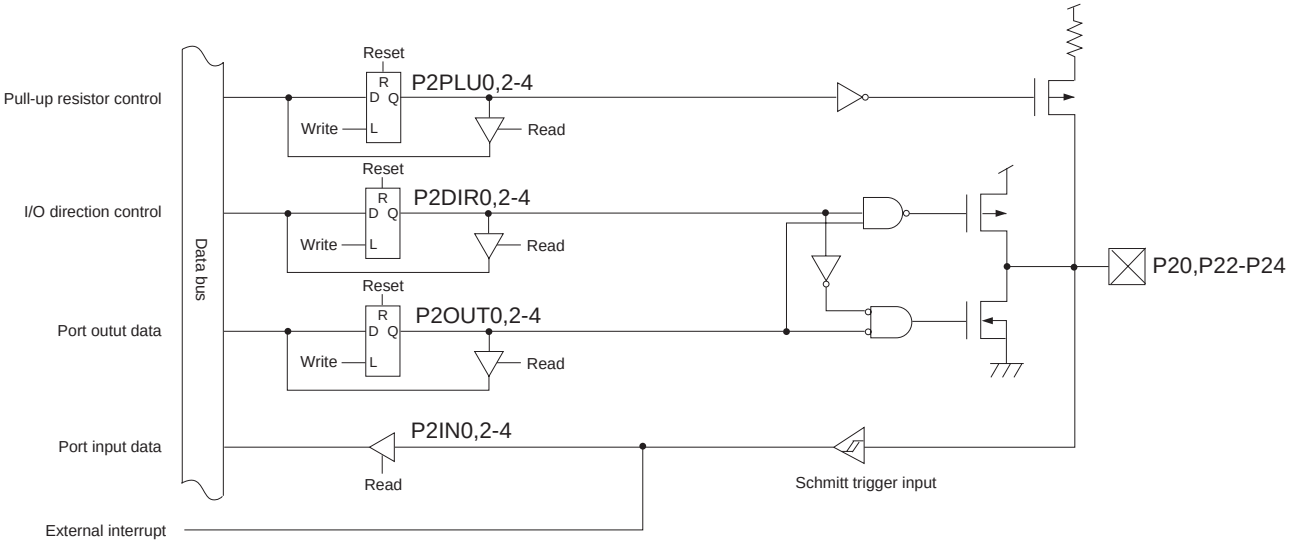


Figure 4-4-2 Block Diagram (P20, P22 to P24)

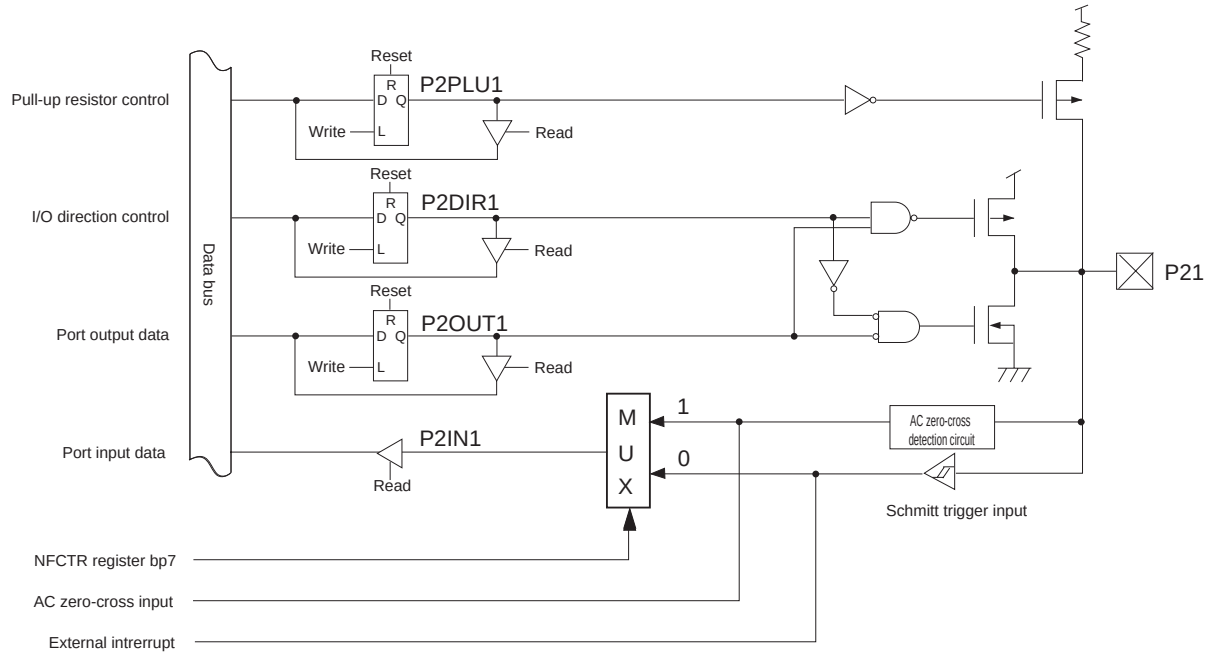


Figure 4-4-3 Block Diagram (P21)

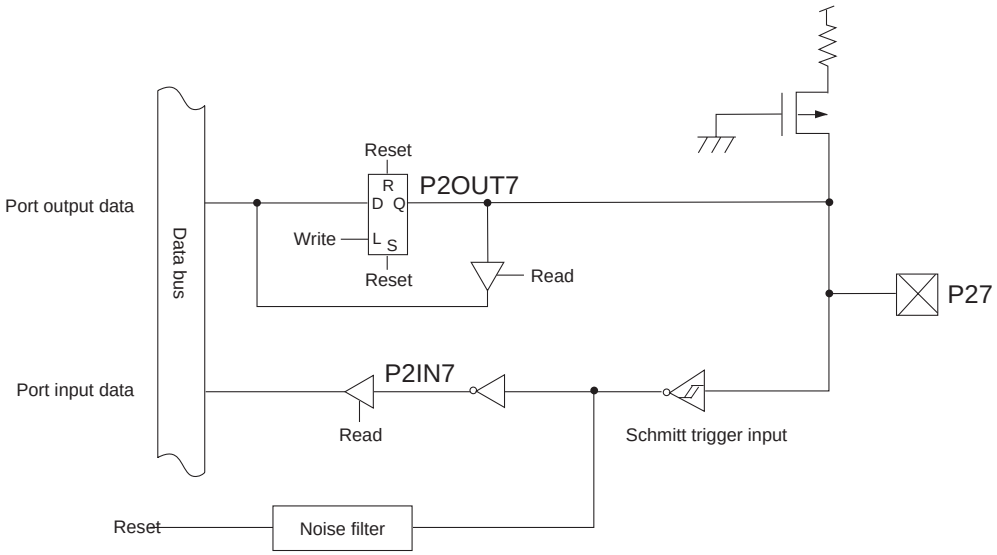


Figure 4-4-4 Block Diagram (P27)

4-5 Port 5

4-5-1 Description

■General Port Setup

Each bit of the port 5 control I/O direction register (P5DIR) can be set individually to set pins as input or output. The control flag of the port 5 direction control register (P5DIR) is set to "1" for output mode, and "0" for input mode.

To read input data of pin, set the control flag of the port 5 direction control register (P5DIR) to "0" and read the value of the port 5 input register (P5IN).

To output data to pin, set the control flag of the port 5 direction control register (P5DIR) to "1" and write the value of the port 5 output register (P5OUT).

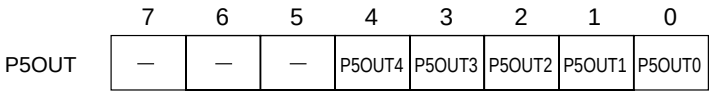
Each pin can be set individually whether pull-up resistor is added or not, by the port 5 pull-up resistor control register (P5PLU). Set the control flag of the port 5 pull-up resistor control register (P5PLU) to "1" to add pull-up resistor.

■Special Function Pin Setup

P50 to P52 are used as I/O pin for the serial interface 3, as well. P51 is output pin of the serial interface 3 transmission data. When the SC3SBOS flag of the serial interface 3 mode register 1 (SC3MD1) is "1", P51 is serial data output pin. P50 is the input pin of the serial interface 3 reception data. P52 is I/O pin of the serial interface 3 clock. When the SC3SBTS flag of serial interface 3 mode register 1 (SC3MD1) is "1", P52 is serial clock output pin.

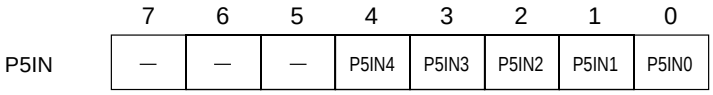
IP53 to P54 are used as I/O pin for the serial interface 4, as well. P53 is data I/O pin of the serial interface 4. When the SELI2C flag of the serial interface 4 address register 1 (SC4AD1) is "1", P53 is serial interface 4 I/O pin. P54 is the serial interface 4 clock I/O pin. When the SELI2C flag of serial interface 4 address register 1 (SC4AD1) is "1", P54 is serial clock I/O pin.

4-5-2 Registers



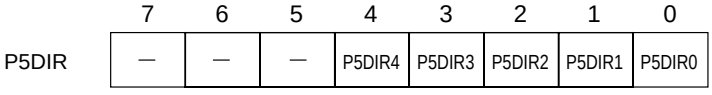
P5OUT	Output data
0	Low (VSS level)
1	High (VDD level)

Port 5 output register (P5OUT : x'03F15', R/W)



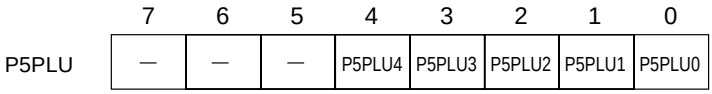
P5IN	Input data
0	Pin is Low (VSS level).
1	Pin is High (VDD level).

Port 5 input register (P5IN : x'03F25', R)



P5DIR	I/O mode selection
0	Input mode
1	Output mode

Port 5 direction control register (P5DIR : x'03F35', R/W)



P5PLU	Pull-up resistor selection
0	No pull-up resistor
1	Pull-up resistor

Port 5 pull-up resistor control register (P5PLU : x'03F45', R/W)

Figure 4-5-1 Port 5 Registers

4-5-3 Block Diagram

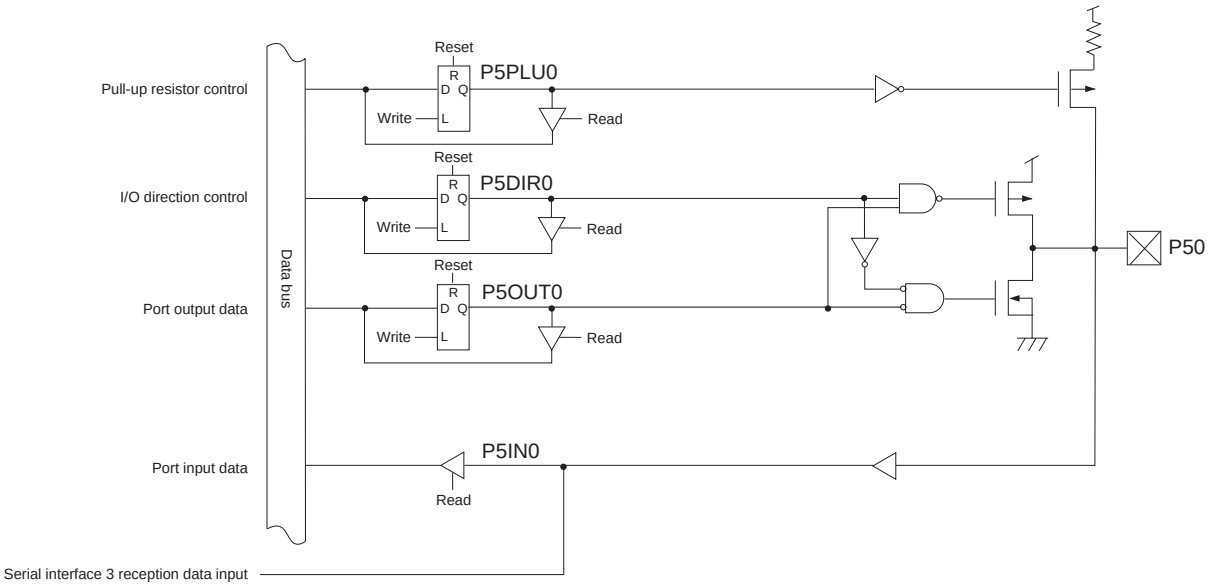


Figure 4-5-2 Block Diagram (P50)

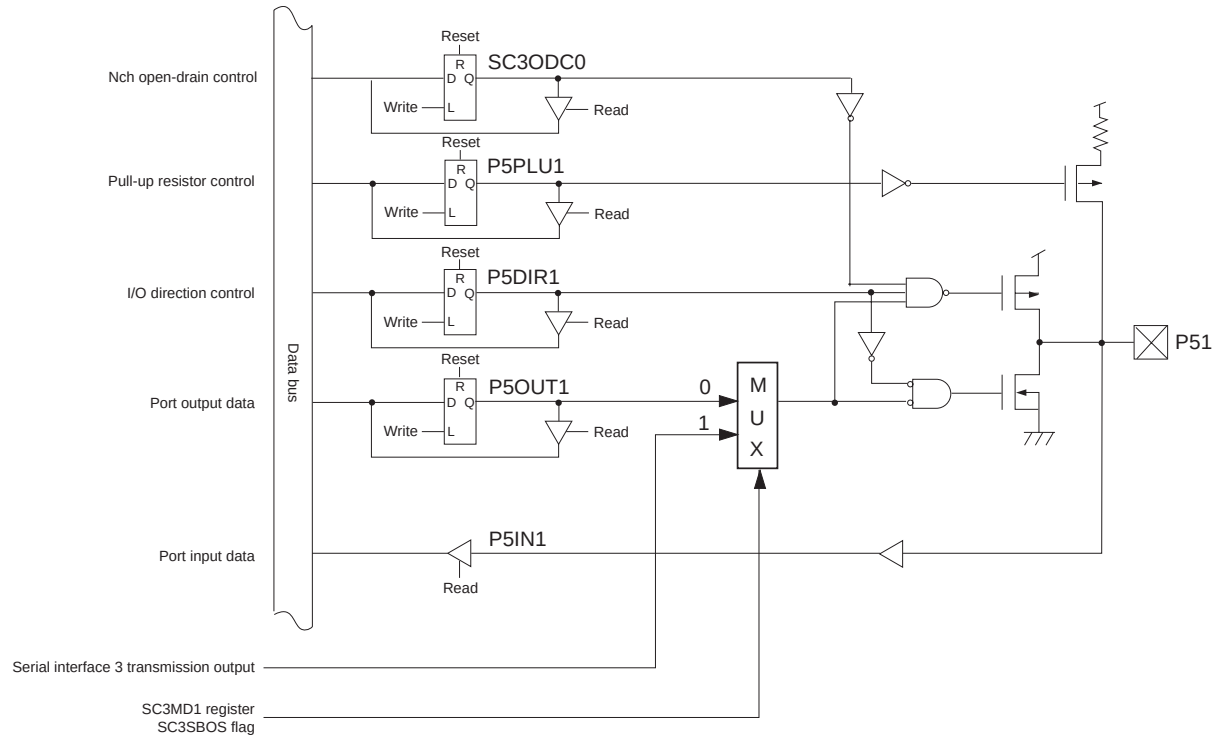


Figure 4-5-3 Block Diagram (P51)

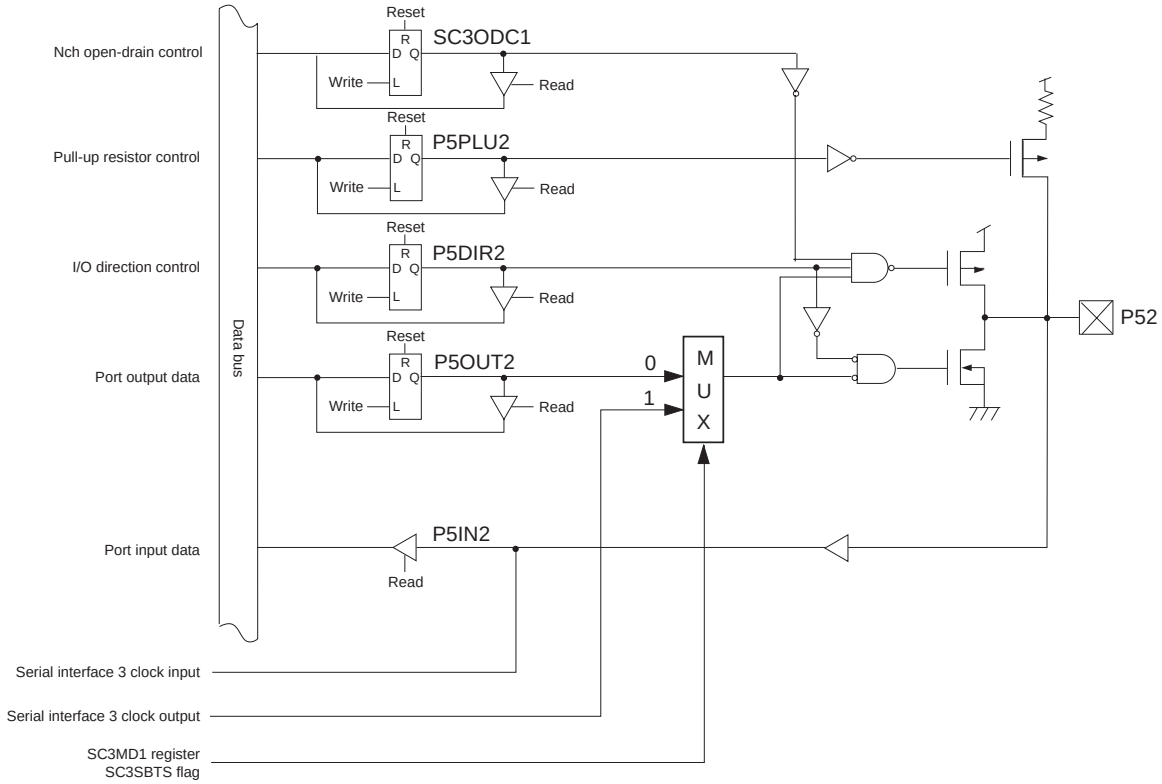


Figure 4-5-4 Block Diagram (P52)

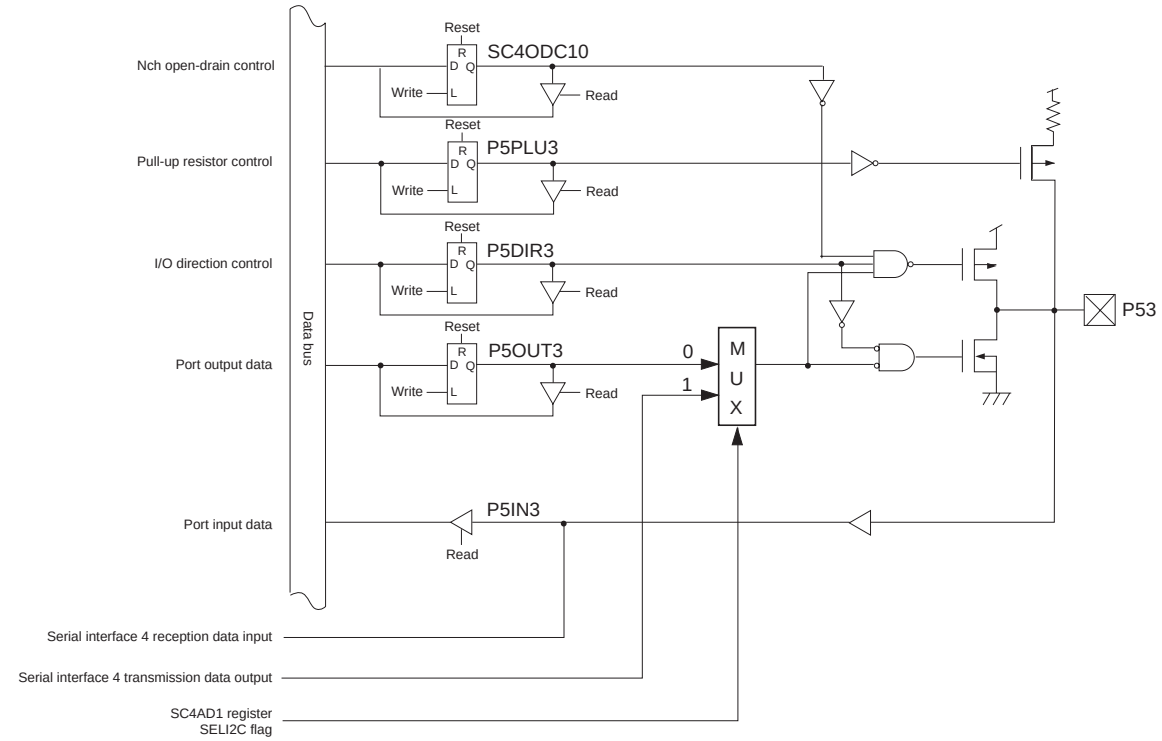


Figure 4-5-5 Block Diagram (P53)

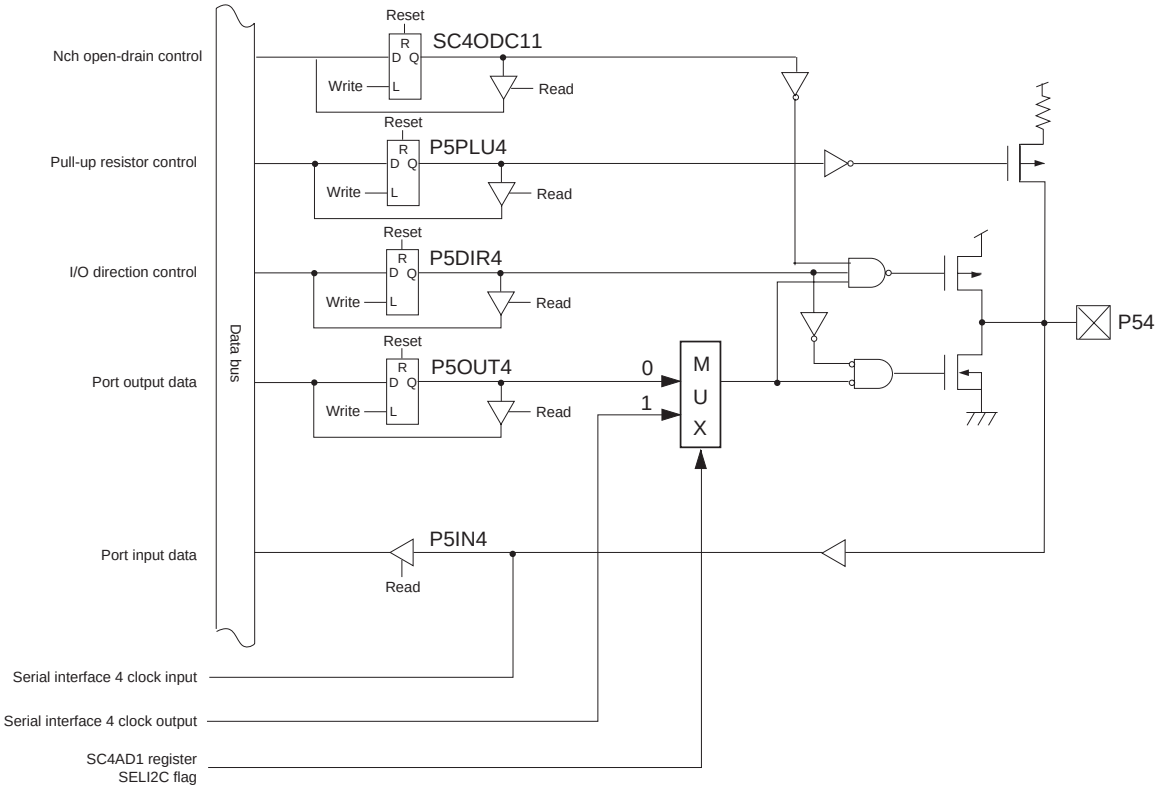


Figure 4-5-6 Block Diagram (P54)

4-6 Port 6

4-6-1 Description

■General port Setup

Each bit of the port 6 control I/O direction register (P6DIR) can be set individually to set pins as input or output. The control flag of the port 6 direction control register (P6DIR) is set to "1" for output mode, and "0" for input mode.

To read input data of pin, set the control flag of the port 6 direction control register (P6DIR) to "0" and read the value of the port 6 input register (P6IN).

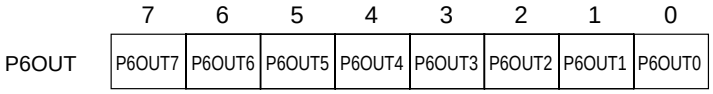
To output data to pin, set the control flag of the port 6 direction control register (P6DIR) to "1" and write the value of the port 6 output register (P6OUT).

Each bit can be set individually whether pull-up resistor is added or not, by the port 6 pull-up resistor control register (P6PLU). Set the control flag of the port 6 pull-up resistor control register (P6PLU) to "1" to add pull-up resistor.

■Special Function Pin Setup

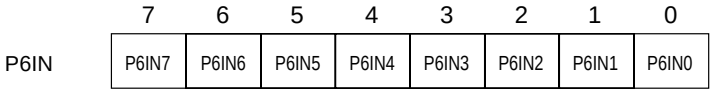
P60 to P67 are used as input pin for the key interrupt, as well. Each bit can be set individually as synchronous output by the port 6 synchronous output control register (P6SYO). The port 6 synchronous output control register (P6SYO) is set to "1" for synchronous output, and "0" for general port. The pin control register (FLOAT) can select the event that generates synchronous output. When the bp1, bp0 of the pin control register (FLOAT) is "00", the external interrupt 2 (IRQ2) is selected, "01" for the timer 7 interrupt, "10" for the timer2 interrupt, and "11" for the timer 1 interrupt.

4-6-2 Registers



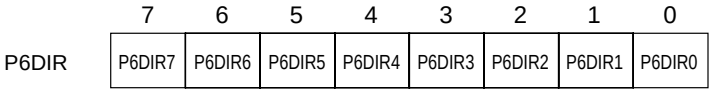
P6OUT	Output data
0	Low (V_{SS} level)
1	High (V_{DD} level)

Port 6 output register (P6OUT : x'03F16', R/W)



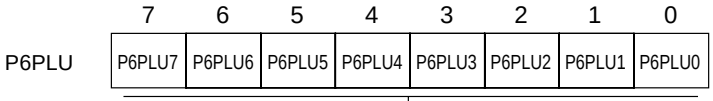
P6IN	Input data
0	Pin is Low (V_{SS} level).
1	Pin is High (V_{DD} level).

Port 6 intput register (P6IN : x'03F26', R)



P6DIR	I/O mode selection
0	Input mode
1	Output mode

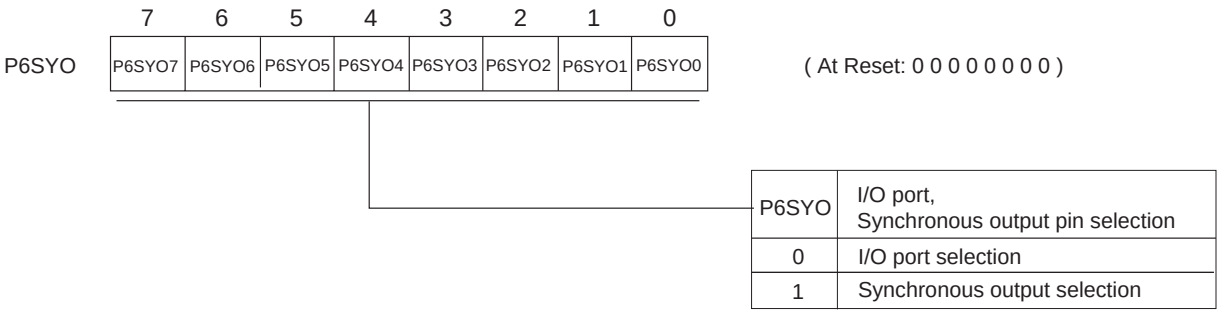
Port 6 direction control register (P6DIR : x'03F36', R/W)



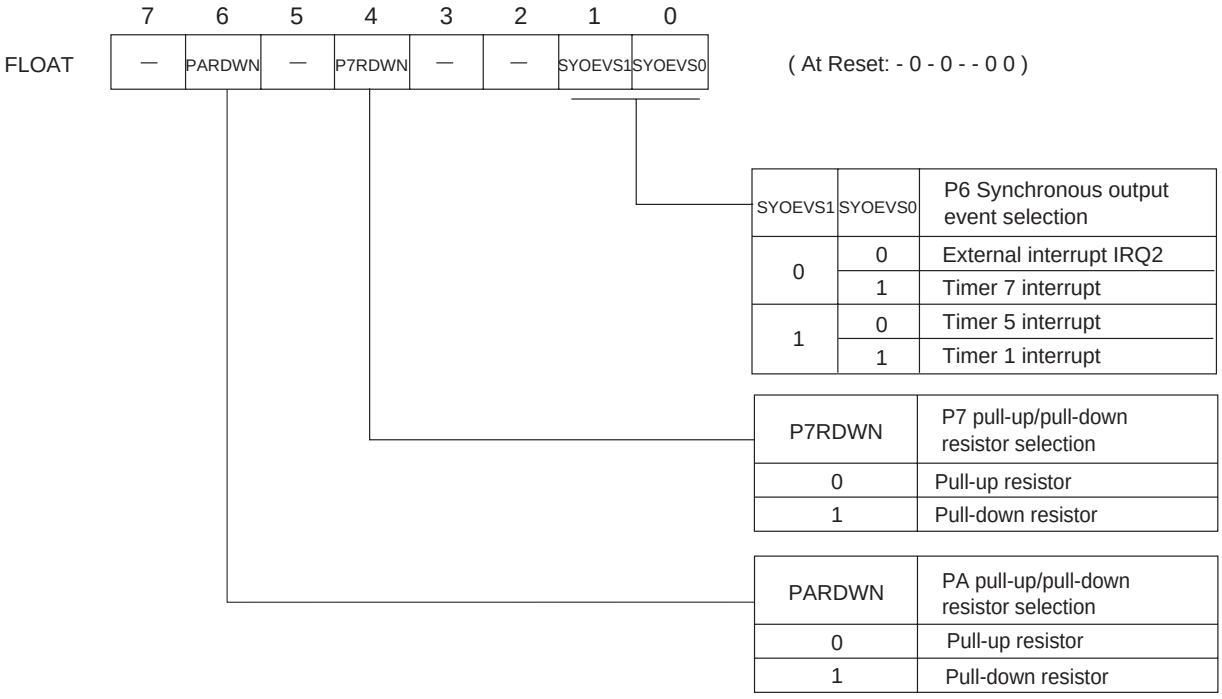
P6PLU	Pull-up resistor selection
0	No pull-up resistor
1	Pull-up resistor

Port 6 pull-up resistor control register (P6PLU : x'03F46', R/W)

Figure 4-6-1 Port 6 Registers (1/2)



Port 6 Synchronous Output Control Register (P6SYO:X'03F1E', R/W)



Pull-up/pull-down resistor selection, pin control register (FLOAT: X'03F2E', R/W)

Figure 4-6-2 Port 6 Registers (2/2)

4-6-3 Block Diagram

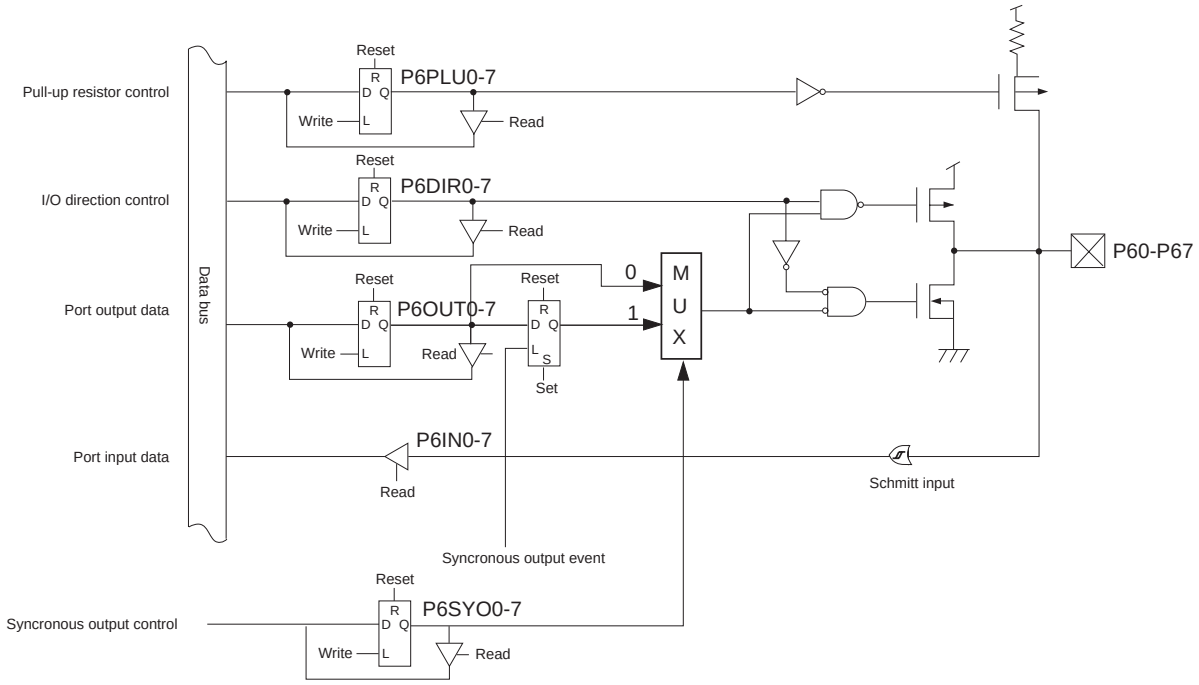


Figure 4-6-3 Block Diagram (P60 to P67)

4-7 Port 7

4-7-1 Description

■General Port Setup

Each bit of the port 7 control I/O direction register (P7DIR) can be set individually to set pins as input or output. The control flag of the port 5 direction control register (P7DIR) is set to "1" for output mode, and "0" for input mode.

To read input data of pin, set the control flag of the port 7 direction control register (P7DIR) to "0" and read the value of the port 7 input register (P7IN).

To output data to pin, set the control flag of the port 7 direction control register (P7DIR) to "1" and write the value of the port 7 output register (P7OUT).

Each pin can be set individually whether pull-up / pull-down resistor is added or not, by the port 7 pull-up / pull-down resistor control register (P7PLUD). Set the control flag of the port 7 pull-up / pull-down resistor control register (P7PLUD) to "1" to add pull-up or pull-down resistor. The pull-up / pull-down resistor selection register (FLOAT) select if pull-up resistor or pull-down resistor is added. The bp4 of the pull-up / pull-down resistor control register (FLOAT) is set to "1" for pull-down resistor, set to "0" for pull-up resistor.

■Special Function Pin Setup

P70 to P72 are used as I/O pin for the serial interface 0, as well. P70 is output pin of the serial interface 1 transmission data. The SC0SBOS flag of the serial interface 0 mode register 1 (SC0MD1) is set to "1" for serial data output. P71 is the input pin of the serial interface 0 reception data. P72 is I/O pin of the serial interface 0 clock. The SC3SBTS flag of serial interface 0 mode register 1 (SC0MD1) is set to "1"for serial clock output

P73 to P75 are used as I/O pin for the serial interface 1, as well. P73 is output pin of the serial interface 1 transmission data. The SC1SBOS flag of the serial interface 1 mode register 1 (SC1MD1) is set to "1" for serial data output. P74 is the input pin of the serial interface 1 reception data. P75 is I/O pin of the serial interface 1 clock. The SC1SBTS flag of serial interface 1 mode register 1 (S10MD1) is set to "1"for serial clock output

P76 to P77 are used as timer I/O pin, as well. Each bit can be set individually as output mode by the port 1 output mode register (P1OMD). The port 1 output mode register (P1OMD) is set to "1" for timer output, and "0" for general port.

4-7-2 Registers

	7	6	5	4	3	2	1	0	
P7OUT	P7OUT7	P7OUT6	P7OUT5	P7OUT4	P7OUT3	P7OUT2	P7OUT1	P7OUT0	(At reset : 0 0 0 0 0 0 0 0)

P7OUT	Output data
0	Low (V_{SS} level)
1	High (V_{DD} level)

Port 7 output register (P7OUT : x'03F17', R/W)

	7	6	5	4	3	2	1	0	
P7IN	P7IN7	P7IN6	P7IN5	P7IN4	P7IN3	P7IN2	P7IN1	P7IN0	(At reset : X X X X X X X X)

P7IN	Input data
0	Pin is Low (V_{SS} level).
1	Pin is High (V_{DD} level).

Port 7 input register (P7IN : x'03F27', R)

	7	6	5	4	3	2	1	0	
P7DIR	P7DIR7	P7DIR6	P7DIR5	P7DIR4	P7DIR3	P7DIR2	P7DIR1	P7DIR0	(At reset : 0 0 0 0 0 0 0 0)

P7DIR	I/O mode selection
0	Input mode
1	Output mode

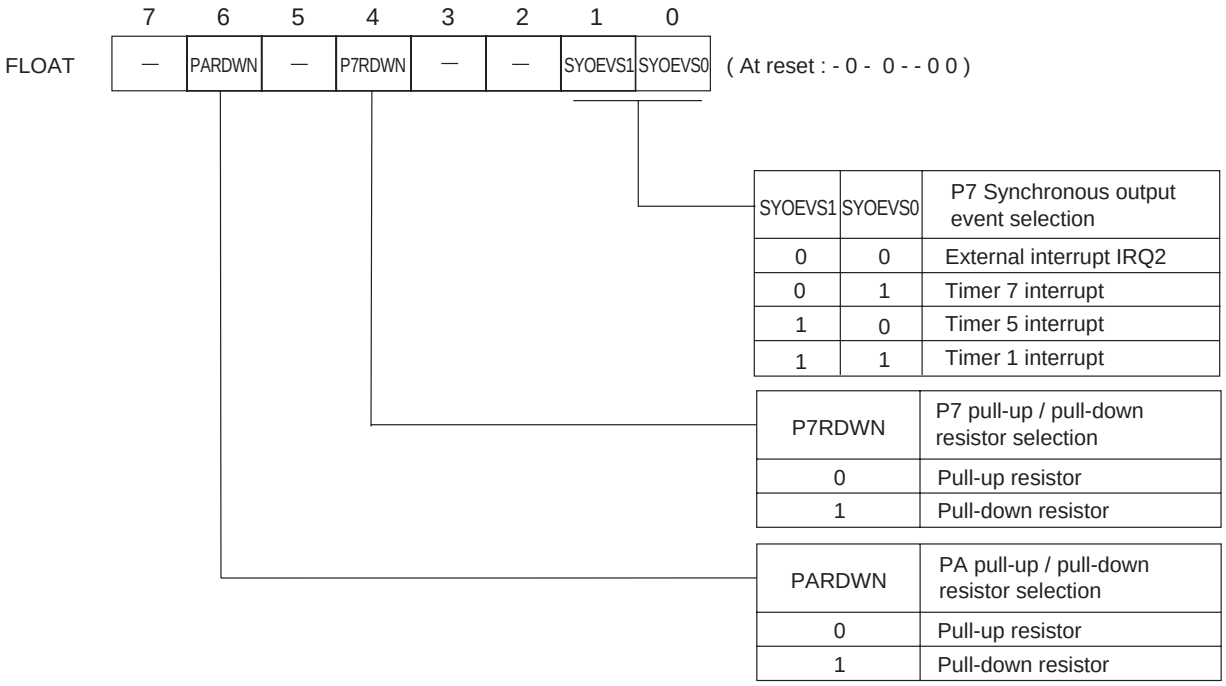
Port 7 direction control register (P7DIR : x'03F37', R/W)

	7	6	5	4	3	2	1	0	
P7PLUD	P7PLUD7	P7PLUD6	P7PLUD5	P7PLUD4	P7PLUD3	P7PLUD2	P7PLUD1	P7PLUD0	(At reset : 0 0 0 0 0 0 0 0)

P7PLUD	Pull-up (or Pull-down) resistor selection
0	No pull-up (or pull-down) resistor
1	Pull-up (or Pull-down) resistor

Port 7 pull-up / pull-down resistor control register (P7PLUD : x'03F47', R/W)

Figure 4-7-1 Port 7 Registers (1/2)



Pull-up / Pull-down resistor selection, Pin control register (FLOAT : x'03F2E', R/W)

Figure 4-7-2 Port 7 Registers (2/2)

4-7-3 Block Diagram

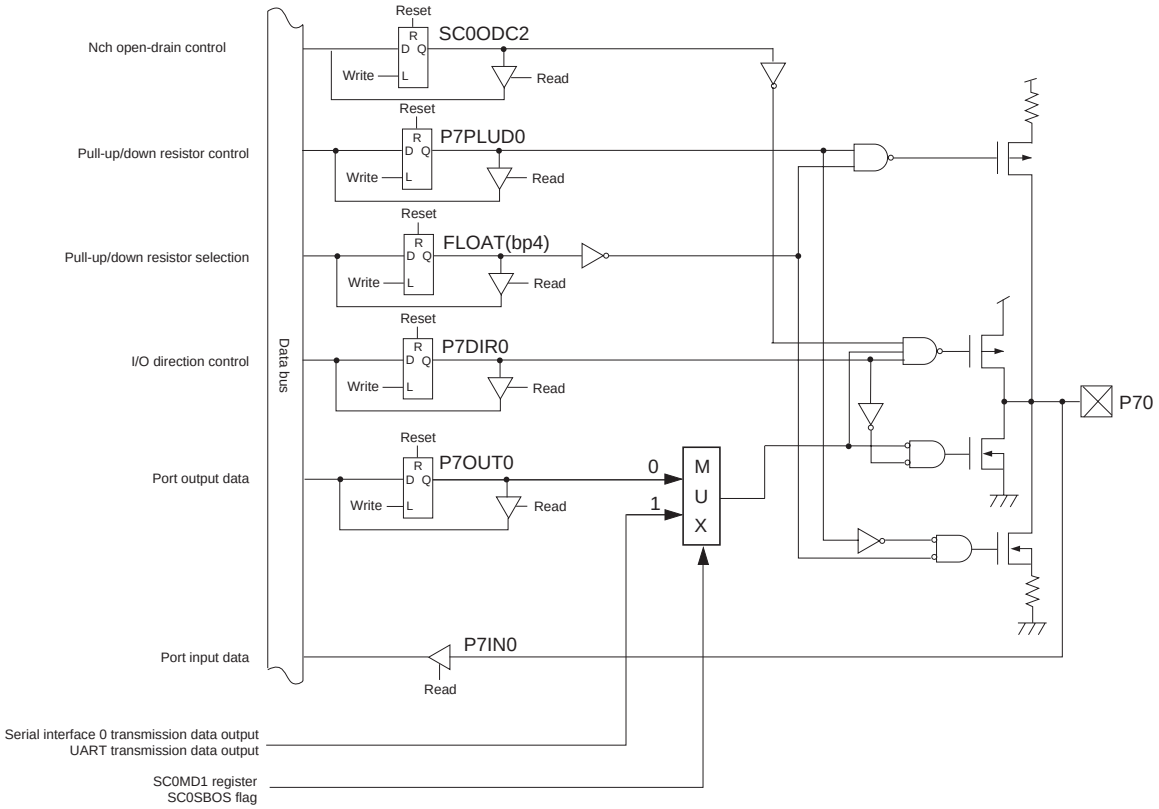


Figure 4-7-3 Block Diagram (P70)

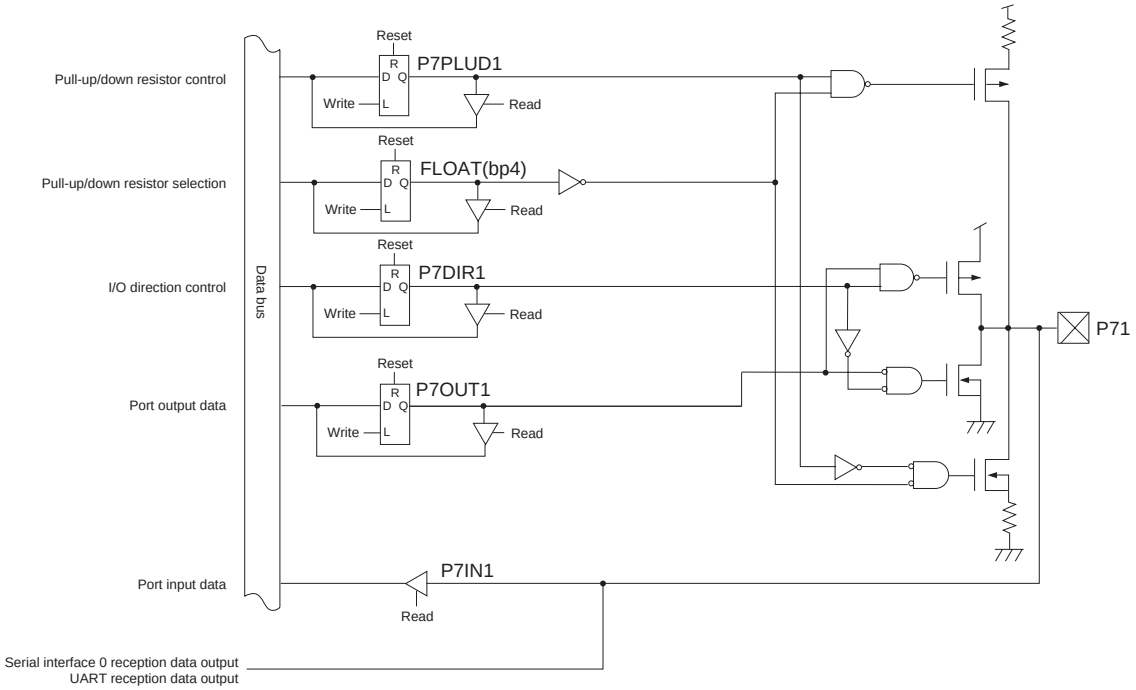


Figure 4-7-4 Block Diagram (P71)

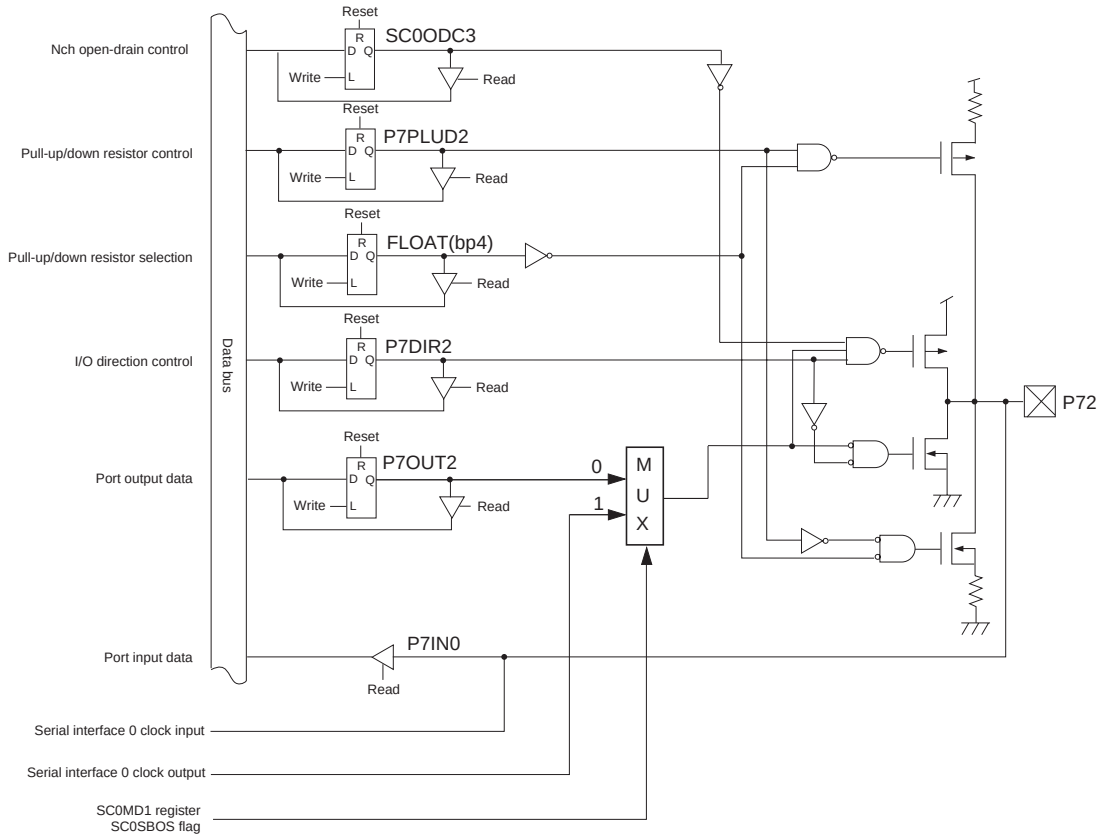


Figure 4-7-5 Block Diagram (P72)

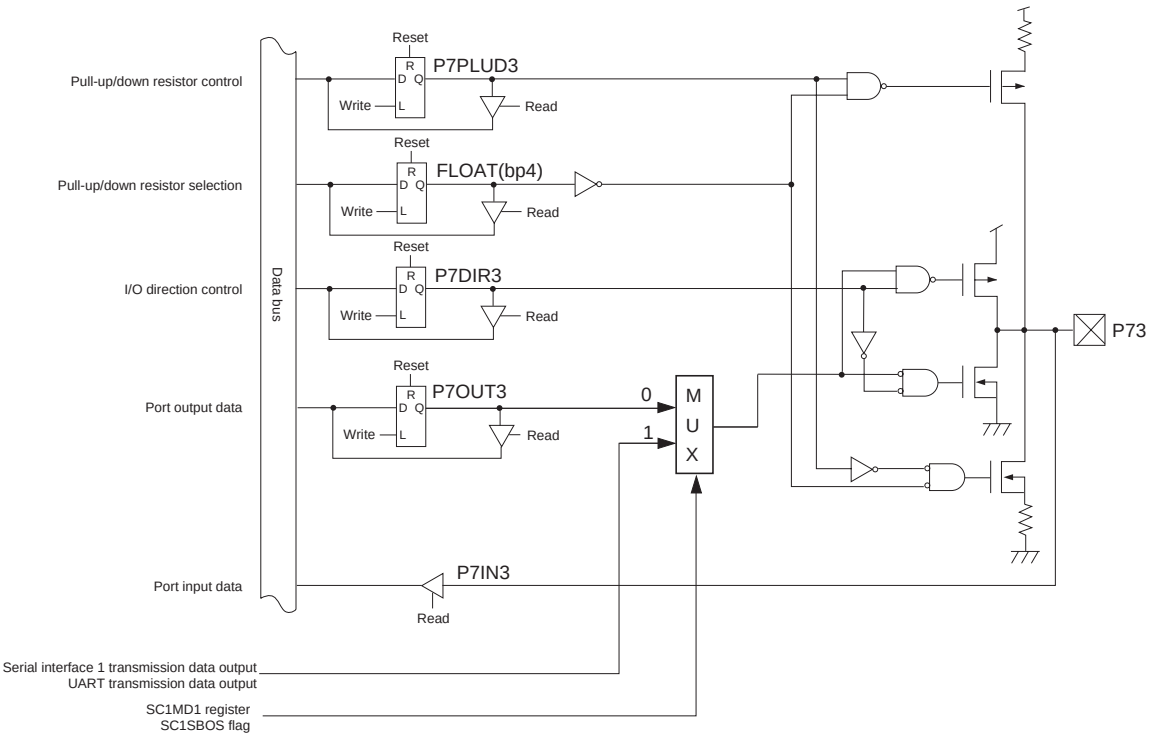


Figure 4-7-6 Block Diagram (P72)

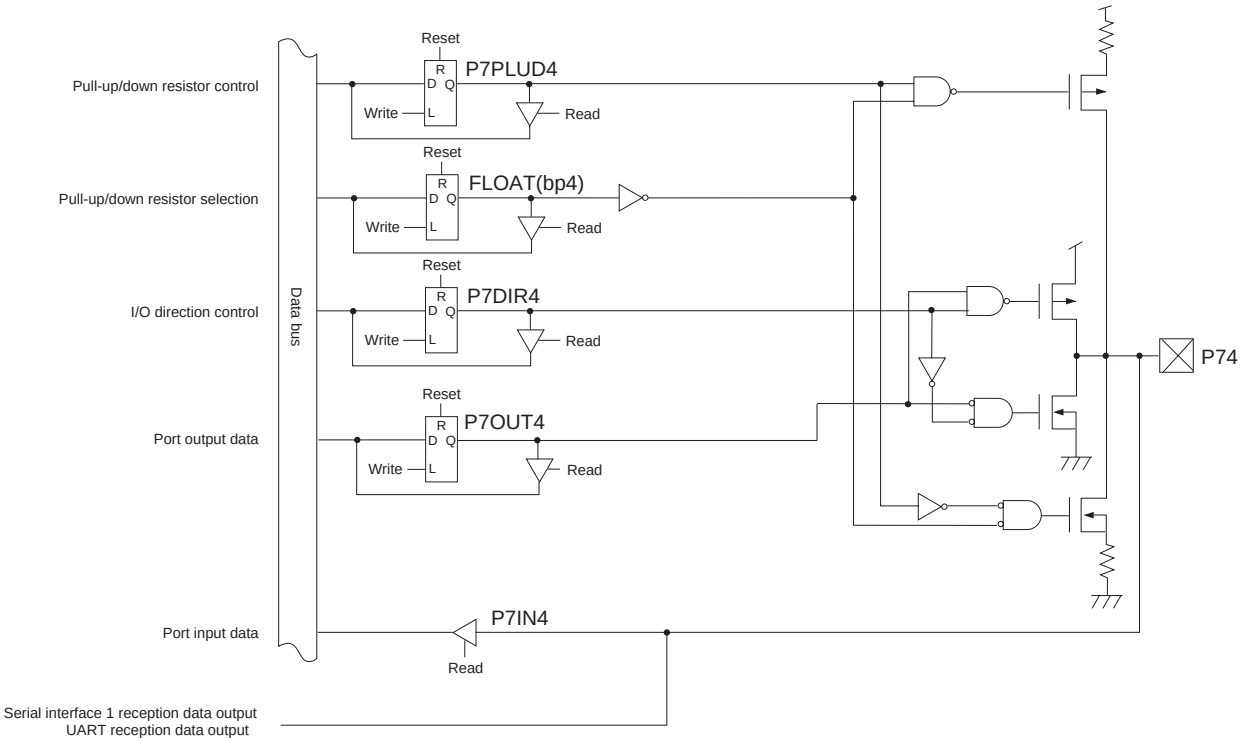


Figure 4-7-7 Block Diagram (P74)

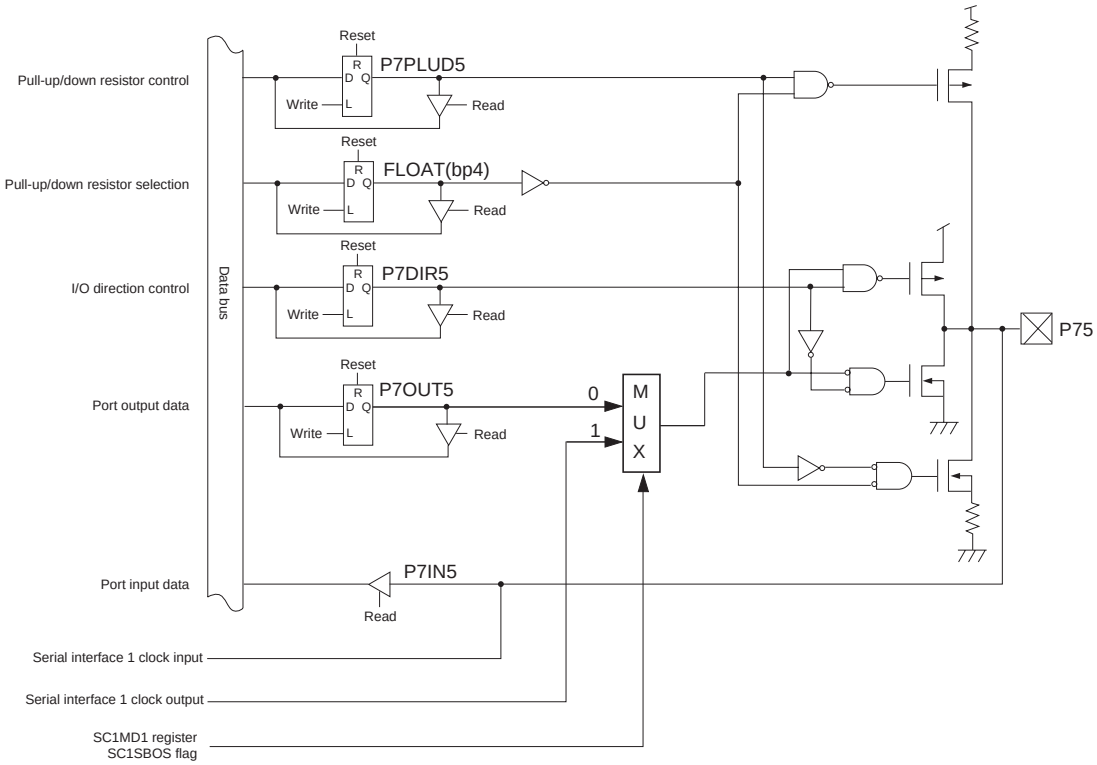


Figure 4-7-8 Block Diagram (P75)

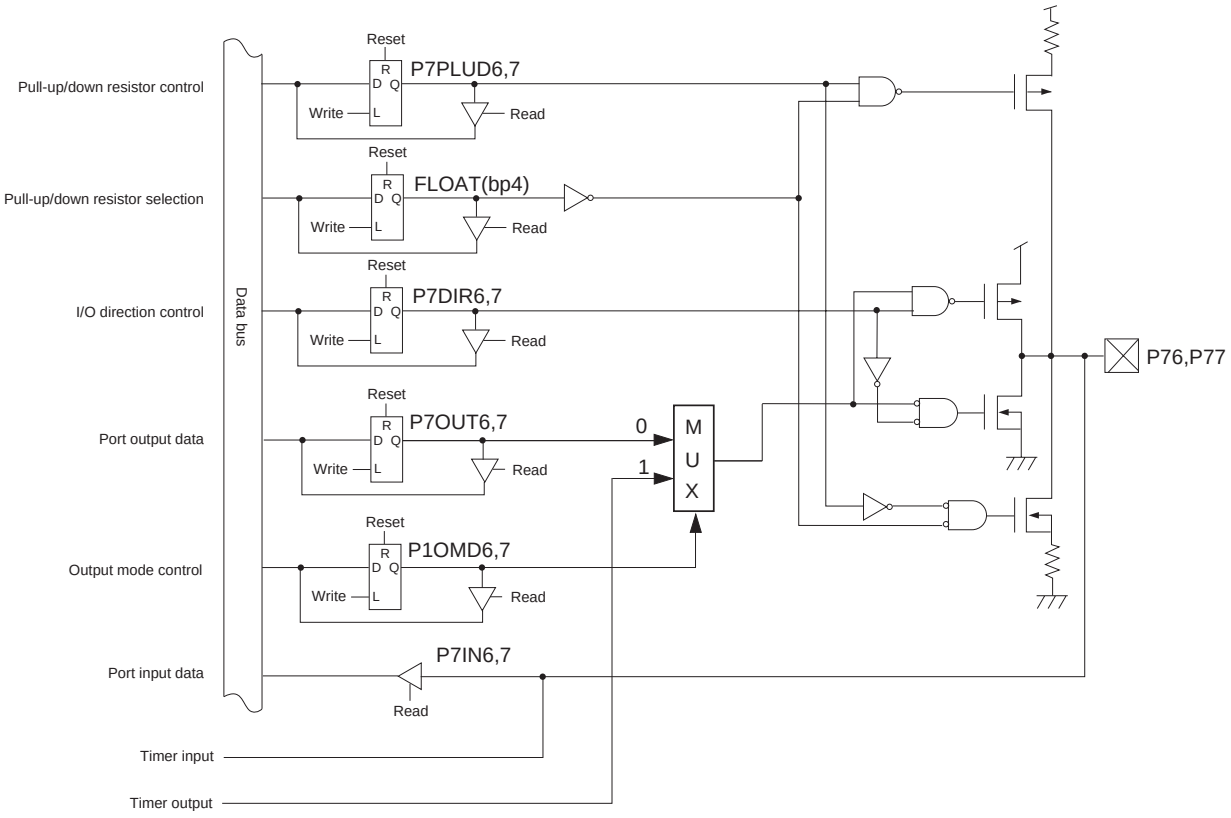


Figure 4-7-9 Block Diagram (P76, P77)

4-8 Port 8

4-8-1 Description

■General Port Setup
Each bit of the port 8 control I/O direction register (P8DIR) can be set individually to set each pin as input or output. The control flag of the port 8 direction control register (P8DIR) is set to "1" for output mode, and "0" for input mode.

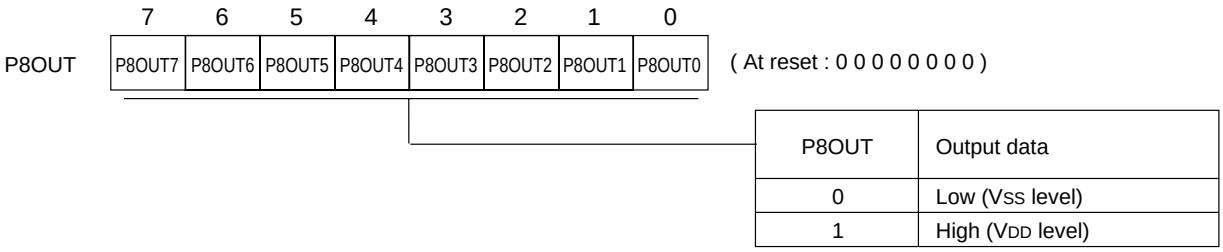
To read input data of pin, set the control flag of the port 8 direction control register (P8DIR) to "0" and read the value of the port 8 input register (P8IN).

To output data to pin, set the control flag of the port 8 direction control register (P8DIR) to "1" and write the value of the port 8 output register (P8OUT).

Each pin can be set individually whether pull-up resistor is added or not, by the port 8 pull-up resistor control register (P8PLU). Set the control flag of the port 8 pull-up resistor control register (P8PLU) to "1" to add pull-up resistor.

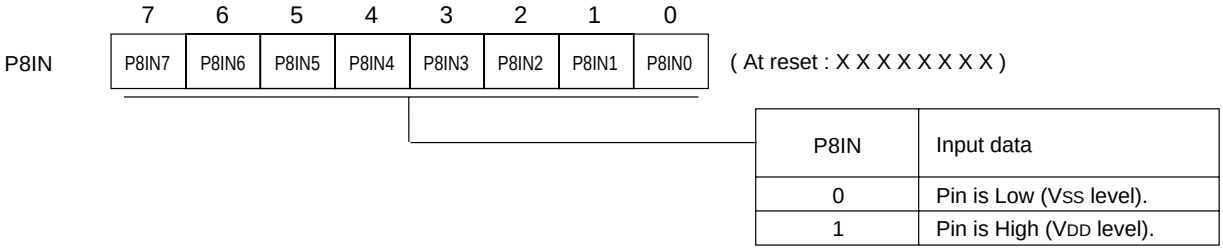
■ Special Function Pin Setup
P80 to P87 are used as LED driving pins, as well.

4-8-2 Registers



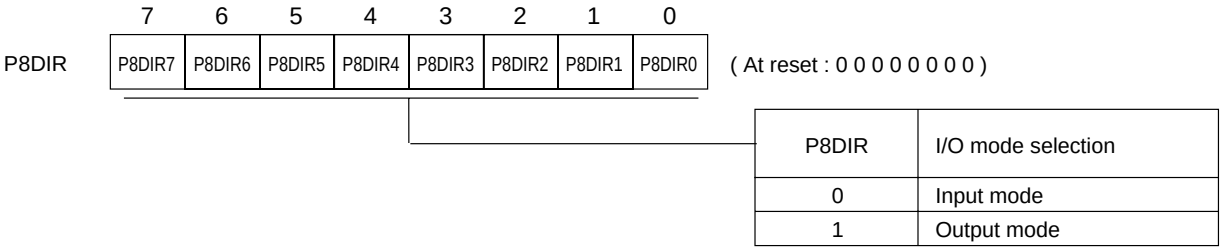
P8OUT	Output data
0	Low (VSS level)
1	High (VDD level)

Port 8 output register (P8OUT : x'03F18', R/W)



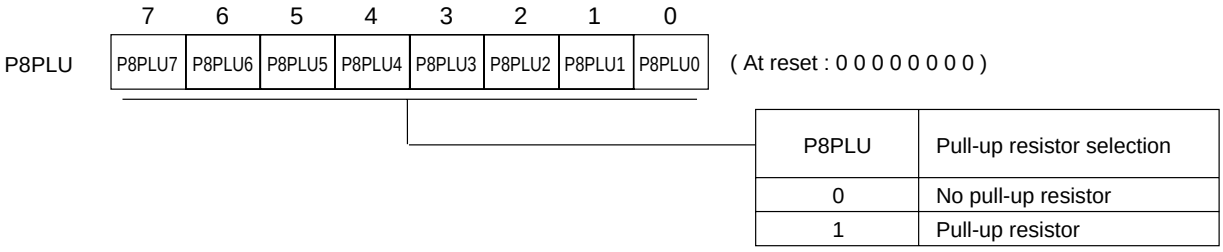
P8IN	Input data
0	Pin is Low (VSS level).
1	Pin is High (VDD level).

Port 8 input register (P8IN : x'03F28', R)



P8DIR	I/O mode selection
0	Input mode
1	Output mode

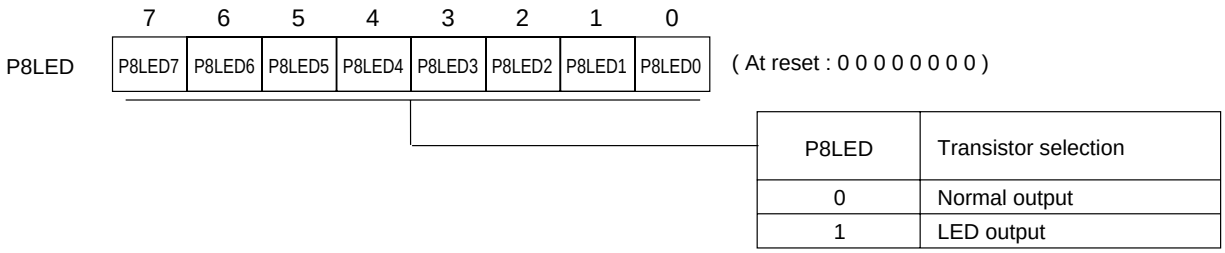
Port 8 direction control register (P8DIR : x'03F38', R/W)



P8PLU	Pull-up resistor selection
0	No pull-up resistor
1	Pull-up resistor

Port 8 pull-up resistor control register (P8PLU : x'03F48', R/W)

Figure 4-8-1 Port 8 Registers (1/2)



Port 8 LED Control register (P8LED : x'03F1D', R/W)

Figure 4-8-2 Port 8 Registers (2/2)

4-8-3 Block Diagram

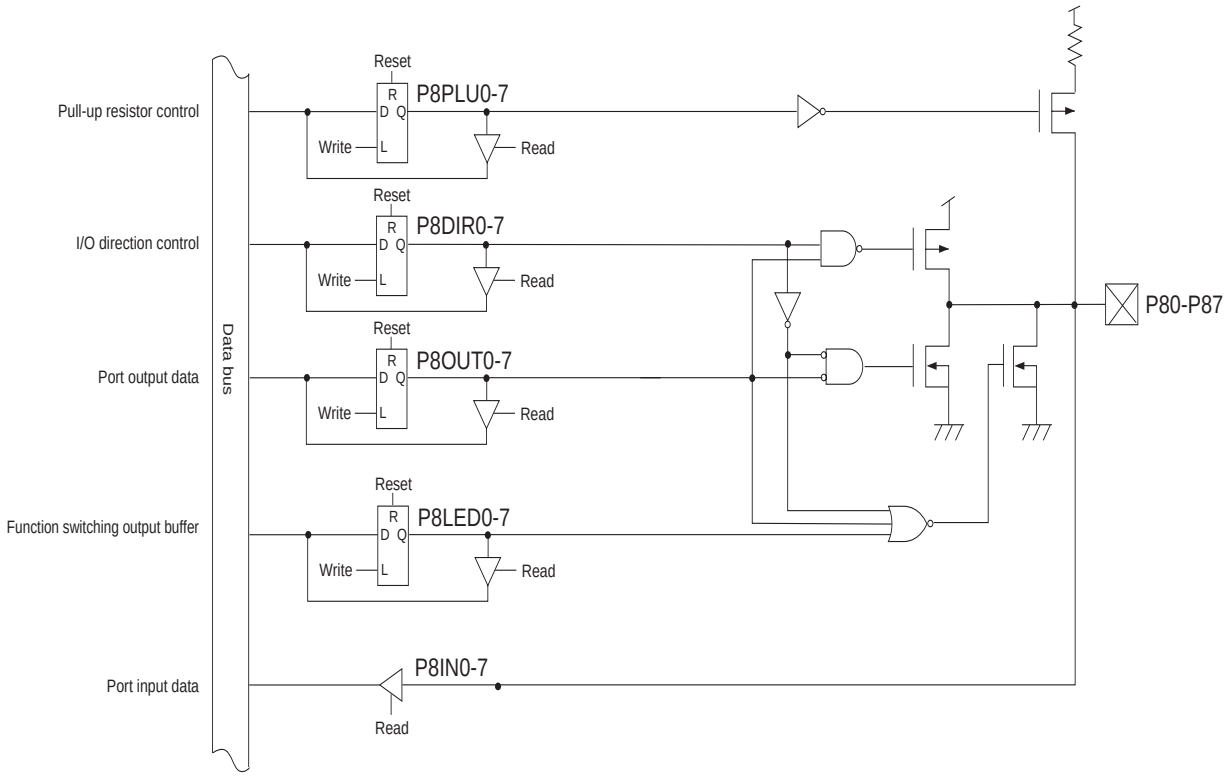


Figure 4-8-3 Block Diagram (P80 to P87)

4-9 Port A

4-9-1 Description

■General Port Setup

Each bit of the port A control I/O direction register (PADIR) can be set individually to set each pin as input or output. The control flag of the port A direction control register (PADIR) should be set to "1" for output mode, and "0" for input mode.

To read input data of pin, set the control flag of the port A direction control register (PADIR) to "0" and read the value of the port 0 input register (P0IN).

To output data to pin, set the control flag of the port A direction control register (P0DIR) to "!" and write the value of the port 0 output register (P0OUT).

Each bit can be set individually whether pull-up / pull-down resistor is added or not, by the port A pull-up / pull-down resistor control register (PAPLUD). Set the control flag of the port A pull-up / pull-down resistor control register (PAPLUD) to "1" to add pull-up or pull-down resistor. The pull-up / pull-down resistor selection register (FLOAT) select if pull-up resistor or pull-down resistor is added. The bp6 of the pull-up / pull-down resistor control register (FLOAT) is set to "1" for pull-down resistor, set to "0" for pull-up resistor.

■Special Function Pin Setup

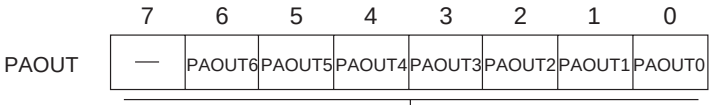
PA0 to PA6 are used as input pins for analog. Each bit can be set individually as an input by the port A input mode register (PAIMD). When they are used as analog input pins, set the port A input mode register (PAIMD) to "1". Then, the value of the port A input register (PAIN) is read out "0".

By setting the control flag of the PAIMD register to "1", the through current is not occurred when input voltage is at intermediate level.

PA0 to PA1 is used as DA output pin, as well. By the setting of DA control register (DACTR), PA0 to PA1 can be used as DA0, DA1 output pin during DA converting. As for the rest, PA0 to PA1 can be used as general port. During DA converting, the port A input register (PAIN) indicates "1".

To prevent the through current, add the pull-up resistor when PA0 to PA1 are used as output pin for DA and analog output is not used.

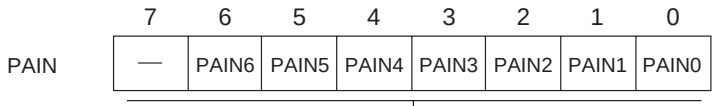
4-9-2 Registers



(At reset : - 0 0 0 0 0 0 0)

PAOUT	Output data
0	Low (Vss level)
1	High (Vdd level)

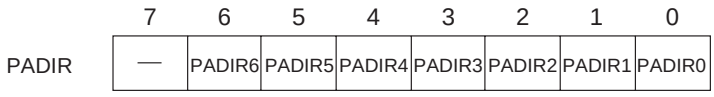
Port A output register (PAOUT: X'03F1A', R/W)



(At reset : X X X X X X X X)

PAIN	Input data
0	Pin is low (Vss level)
1	Pin is high (Vdd level)

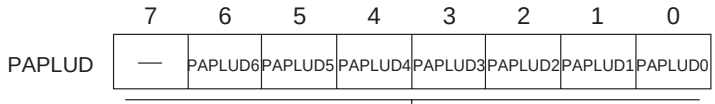
Port A intput register (PAIN: X'03F2A', R)



(At reset : - 0 0 0 0 0 0 0)

PADIR	I/O mode selection
0	Input mode
1	Output mode

Port A direction control register (PADIR: X'03F3A', R/W)

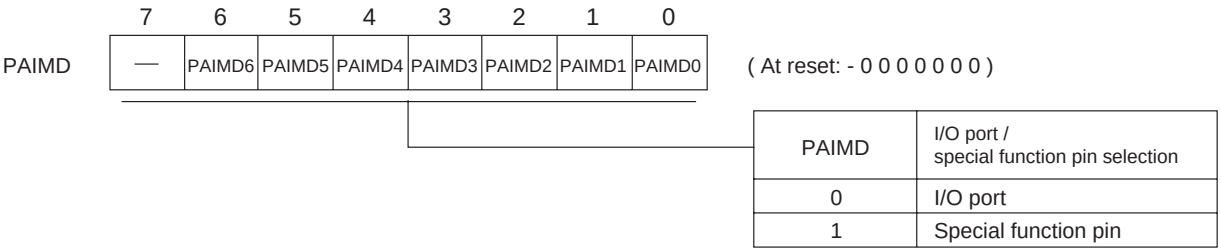


(At reset : - 0 0 0 0 0 0 0)

PAPLUD	Pull-up (or pull-down) resistor selection
0	No pull-up (or pull-down) resistor
1	Pull-up (or Pull-down) resistor

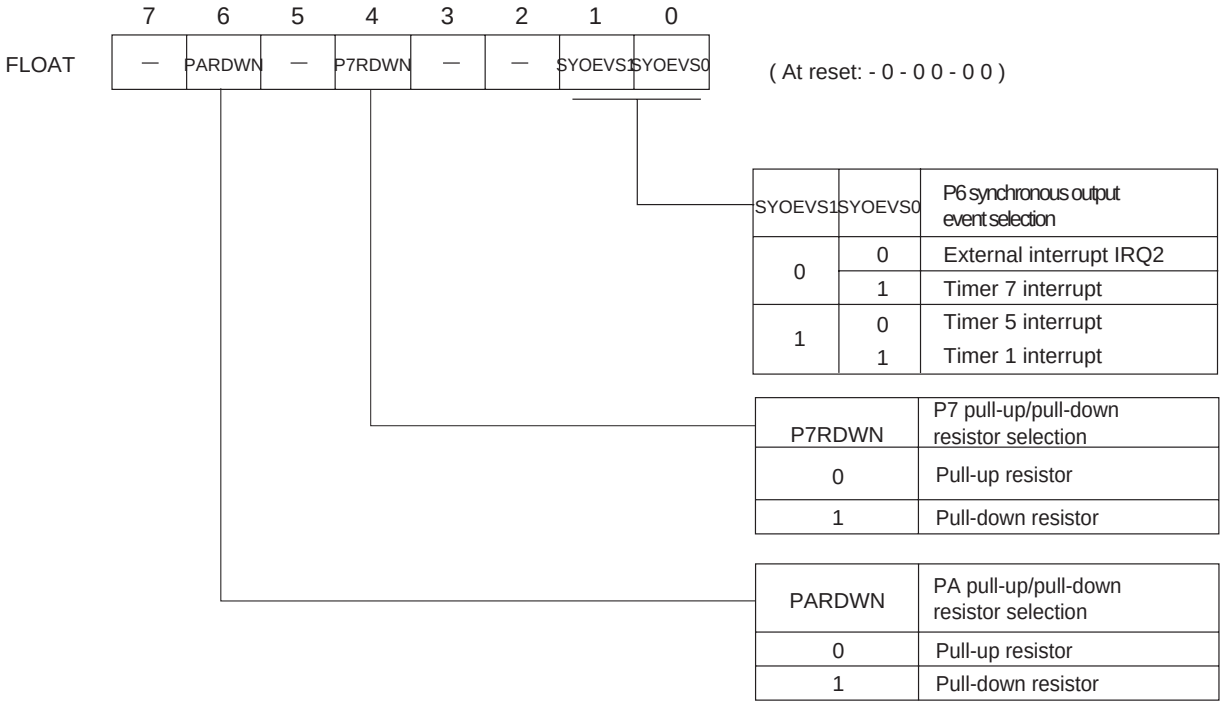
Port A pull-up/pull-down resistor control register (PAPLUD: X'03F4A', R/W)

Figure 4-9-1 Port A Registers (1/2)



PAIMD	I/O port / special function pin selection
0	I/O port
1	Special function pin

Port A Input control register (PAIMD: X'03F3C', R/W)



SYOEVS1	SYOEVS0	P6 synchronous output event selection
0	0	External interrupt IRQ2
	1	Timer 7 interrupt
1	0	Timer 5 interrupt
	1	Timer 1 interrupt

P7RDWN	P7 pull-up/pull-down resistor selection
0	Pull-up resistor
1	Pull-down resistor

PARDWN	PA pull-up/pull-down resistor selection
0	Pull-up resistor
1	Pull-down resistor

Pull-up/pull-down resistor selection, Pin control register (FLOAT: X'03F2E', R/W)

Figure 4-9-2 Port A Registers (2/2)

4-9-3 Block Diagram

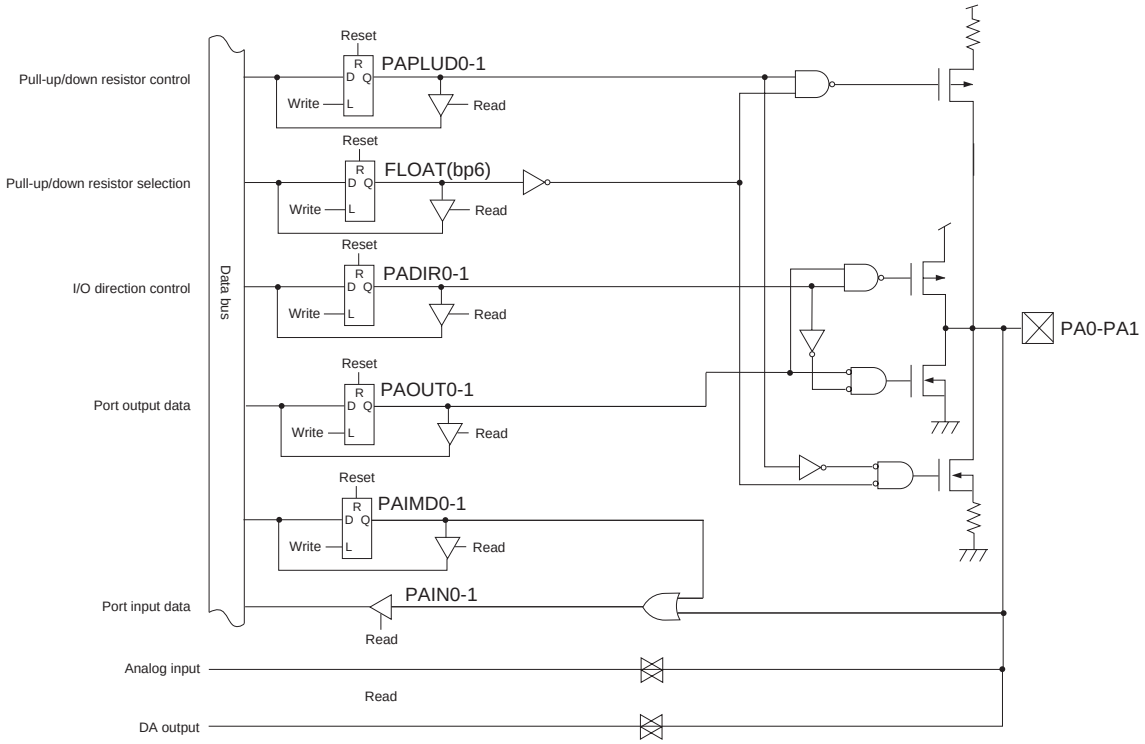


Figure 4-9-3 Block Diagram (PA0 to PA1)

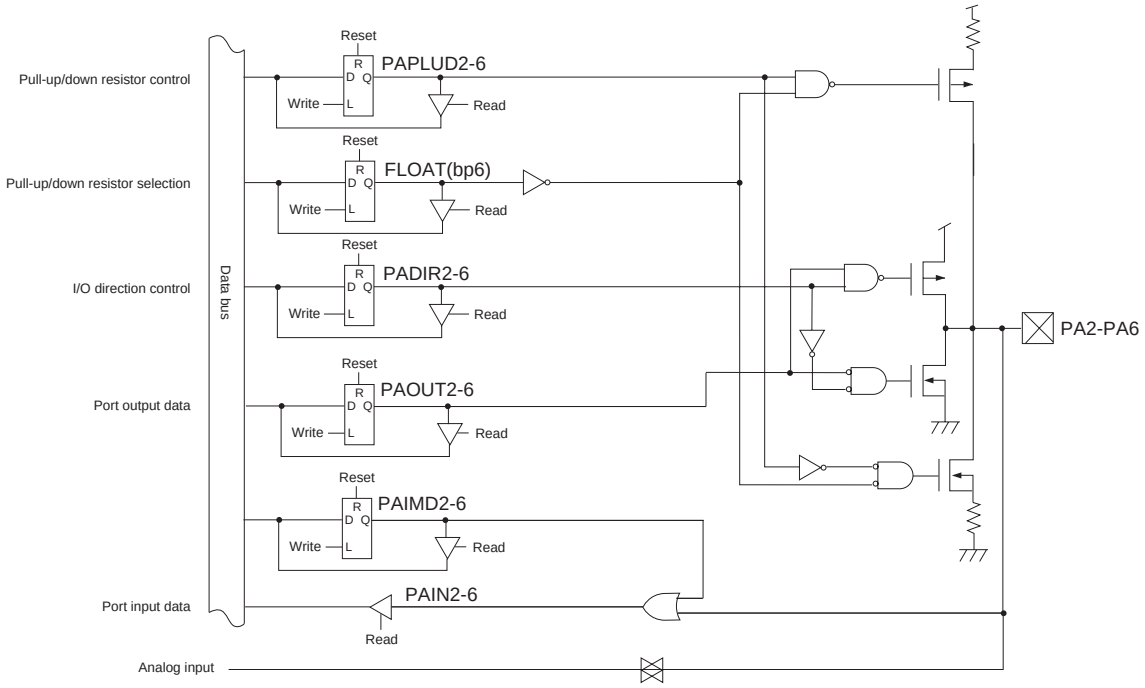


Figure 4-9-4 Block Diagram (PA2 to PA6)

4-10 Real Time Output Control (Port 1)

P10 , P12 and P14 has a real time output function that can switch pin's output at the falling edge of the external interrupt 0 pin (P20/IRQ0).

Real time control can change timer output signal (PWM output, timer pulse output, remote control carrier output), without setting on the program, in synchronization with external event. Output levels to be switched at event generation are 3 ; "0", "1" and "high impedance (Hi-z)".

4-10-1 Registers

Table 4-10-1 shows the real time output control register of port 1.

Table 4-10-1 Real Time Output Control Registers

	Register	Address	R/W	Function	Page
Port 1	P1OUT	x'03F11'	R/W	Port 1 output register	IV - 13
	P1OMD	x'03F2F'	R/W	Port 1 output mode register	IV - 14
	P1DIR	x'03F31'	R/W	Port 1 direction control register	IV - 13
	P1PLU	x'03F41'	R/W	Port 1 pull-up control register	IV - 13
	P1TCNT	x'03F7E'	R/W	Port 1 output control register	IV - 14

4-10-2 Operation

■Real Time Output Pin Setup

The real time output pin is set by the port 1 output control register(P1TCNT). The selectable pins are P10, P12 and P14. Those can be specified by each pin. Select the output mode by the port 1 direction control register (P1DIR).

There are 3 output levels ; "0", "1" and "High impedance(Hi-z)". Those are switched at the falling edge of the external interrupt 0 pin (P20/IRQ0). At high impedance, port becomes input mode.

The real time control changes the timer output signal (PWM output, timer pulse output, remote control carrier output) in synchronization with the external event, but it is also valid on normal port output.

When the I/O port (disable the real time control) is selected by the port 1 output control register (P1TCNT), the output level is not changed even if the switching event is generated. When it is used as general port, set this mode.

■Real Time Output Control Operation

After the port 1 output control register (P1TCNT) is set, the function selected by the port 1 output mode register (P1OMD) is output from the pin until the falling edge at the external interrupt 0 pin (P20/IRQ0) is generated.

Once the falling edge of the external interrupt 0 is generated, the pin's output is switched to the set level. The event of the falling edge is stored to the edge event save function shown at the figure 4-3-4. Block diagram (P10, P12, P14), and the set level of the port 1 output control register (P1TCNT) is output until the event data is cleared.

■Release Real Time Output (Clear the edge event save function)

Writing data to the port 1 output register (P1OUT) after event is generated, makes the event data of the edge event save function cleared. And all pins' output data become the former data before event is generated. If the event is generated again, all pins' output level of the port 1 output control register (P1TCNT).

Set the pin's output to "I/O port (disable the real time control)" by setting the port 1 output control register (P1TCNT) to stop the real time control.

The active edge of IRQ0 is only falling edge, regardless of its setting at the external interrupt 0 control register (IRQ0ICR).

Write to the port 1 output register (P1OUT) to clear the event data of the edge event save function, before the real time output control function is used.

■Timing

P1n output (n=0, 2, 4) : Timer output
P1TCNT set level : "0" (Low) output

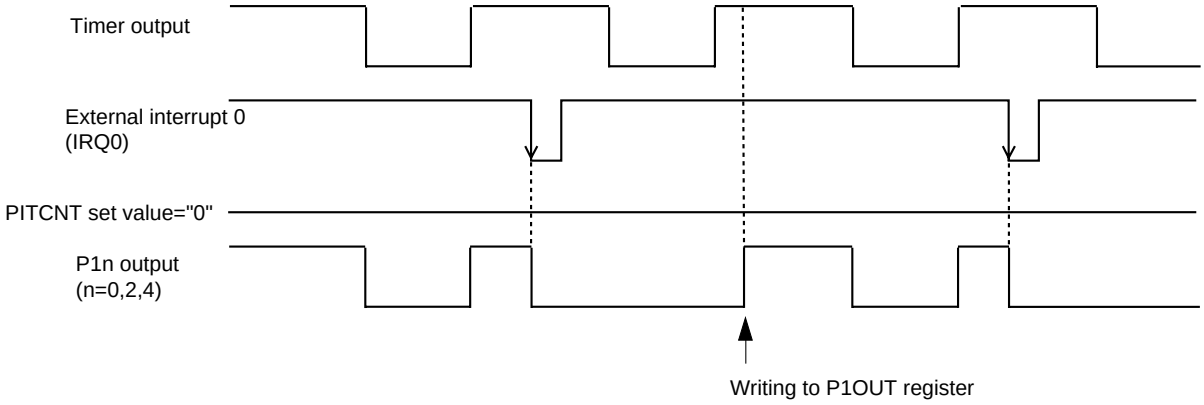


Figure 4-10-1 Real Time Output Control Timing

4-11 Synchronous output (Port 6)

Port 6 has the synchronous output function that outputs the any set data to pins, in synchronization with the generation of the specified event. Synchronous event is selected from the external interrupt 2 (P22/IRQ2), timer 1 interrupt, timer 5 interrupt or timer 7 interrupt signal.

4-11-1 Block Diagram

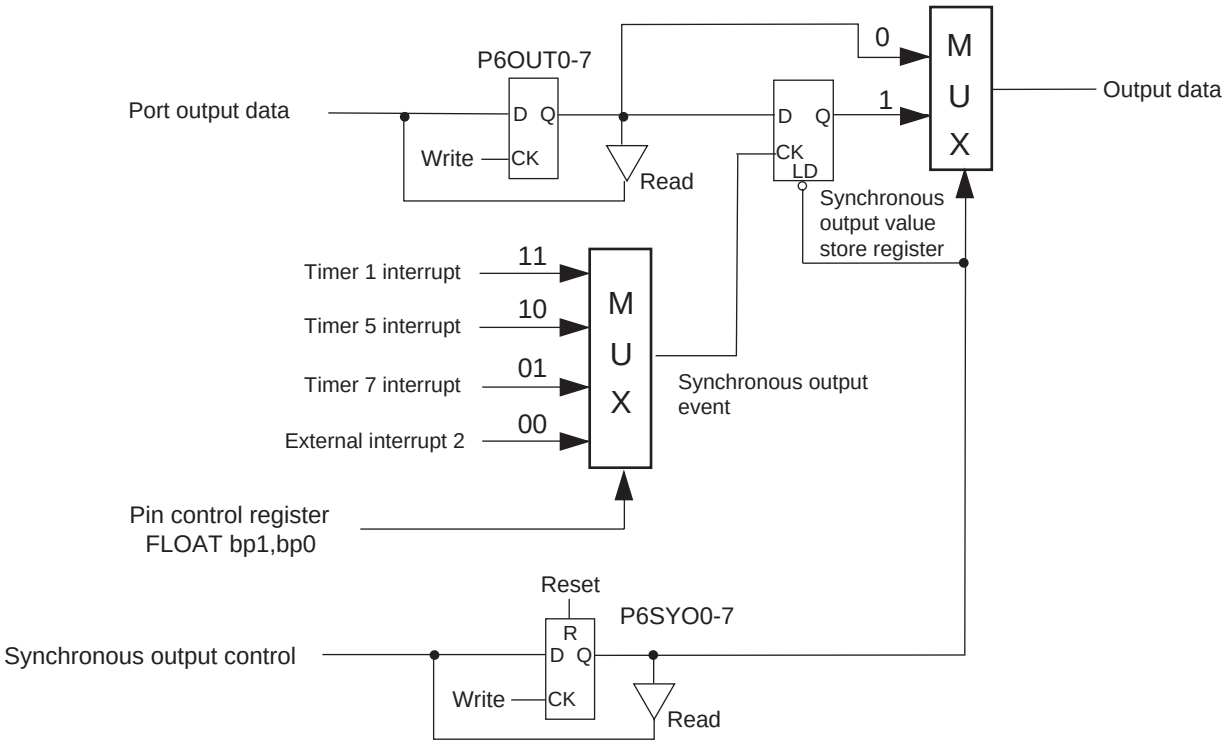


Figure 4-11-1 Synchronous Output Control Block Diagram

4-11-2 Registers

Table 4-11-1 shows the synchronous output control registers of port 6.

Table 4-11-1 Synchronous Output Control Registers

	Register	Address	R/W	Function	Page
Port 6	FLOAT	x'03F2E'	R/W	Pin control register 1	IV - 41
	P6SYO	x'03F1F'	R/W	Synchronous output control register	IV - 42
	P6DIR	x'03F36'	R/W	Port 6 direction control register	IV - 40
	P6PLU	x'03F46'	R/W	Port 6 Pull-up/pull-down control register	IV - 40
	P6OUT	x'03F16'	R/W	Port 6 output register	IV - 40

4-11-3 Operation

■Synchronous Output Setup

The synchronous output control register (P6SYO) selects the synchronous output pin of the port 6, in each bit.

The synchronous output event is selected by the pin control register (FLOAT).

Table 4-11-2 Synchronous Output Event

		Page
Synchronous output port	Port 6	IV - 26
Output event	External interrupt 2	III - 19, 49
	(IRQ2)	VI - 33
	Timer 1	VI - 33
	Timer 5	VI - 33
	Timer7	VII - 31

When the external interrupt 2 (IRQ2) is selected, the interrupt edge should be specified. The interrupt edge can be specified by the external interrupt 2 control register (IRQ2ICR) or the both edges interrupt control register (EDGDT). The synchronous output recognizes the generation of the specified edge as an event.

■Synchronous Output Operation

When the synchronous output control register (P6SYO) is set to disable the synchronous output (I/O port), the port 6 is functioned as a general port. When the port 6 is set to disable the synchronous output, the same value to the port 6 output register (P6OUT) is always loaded to the synchronous output value stored register. (Figure 4-11-1. Block Diagram)

After the output mode is selected by the port 6 direction control register (P6DIR), if the synchronous output is enabled by the synchronous output control register (P6SYO), the value of the synchronous output value stored register is output from pins. If the synchronous output event that is set by the pin control register (FLOAT) is never generated, the synchronous output value stored register holds the same value when the synchronous output event is enabled.

Store the value that should be output from pin after the synchronous output event is generated, to the port 6 output register (P6OUT). Once the synchronous output event that is set by the pin control register (FLOAT) is generated, the data of the synchronous output value stored register is switched to the data of the port 6 output register (P6OUT), and the output value from pin is changed.

Before the synchronous output is enabled by the synchronous output control register (P6SYO), set the initial value of the synchronous output to the port 7 output register (P6OUT), in advance.

■Port 6 Synchronous Output (External interrupt 2 IRQ2))

The synchronous output timing when the synchronous output event is set at the falling edge of the external interrupt 2, is shown below. The latched data on port 6 is output in synchronization with the falling edge of the IRQ2.

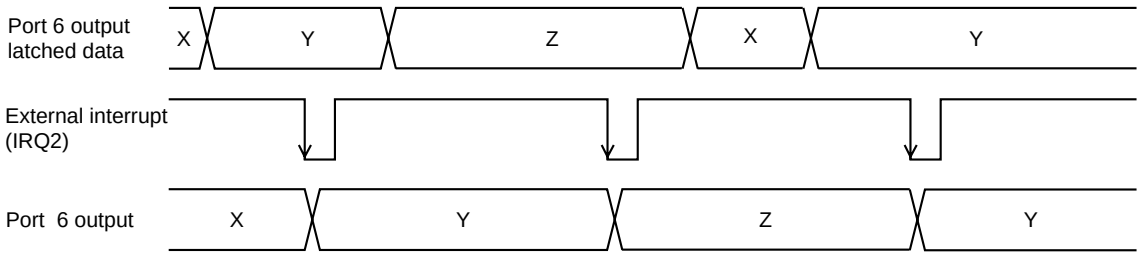


Figure 4-11-2 Synchronous Output Timing by Event Generation (IRQ2)

■Port 6 Synchronous Output (Timers 1,5 and 7)

The timer interrupt flag TMnIRQ is generated when binary counter and compare register are matched. The latched data on port 6 is output from the port 6 in synchronization with the rising edge of the TMnIRQ. About the setting of each timer operation, refer to chapter 6. 8-Bit timers, and chapter 7. 16-Bit timers.

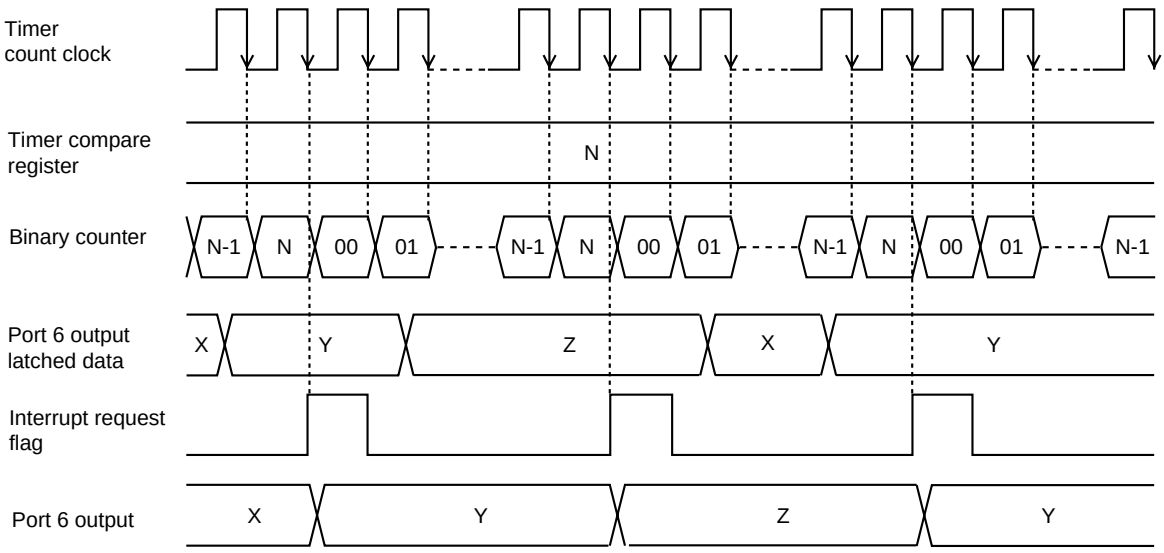


Figure 4-11-3 Synchronous Output Timing by Event Generation (Timers 1, 5 and 7)

4-11-4 Setup Example

A setup example of the port 6 synchronous output by the external interrupt 2 (IRQ2) is shown as follows. As it is operated, the initial output data of port 6 is "55", the synchronous output data is "AA", and the rising edge of the IRQ2 is selected at the synchronous event.

An example setup procedure, with description of each step is shown below.

Setup Procedure	Description
(1) Select the synchronous output event. FLOAT (x'3F2E') bp1-0 :SYOEVS1-0 = 00	(1) Set the SYOEVS1-0 flag of the FLOAT register to "00" to set the synchronous output event to the IRQ2.
(2) Specify the interrupt edge. IRQ2ICR(x'3FE4') bp5 : REDG2 = 1 EDGDT(x'3F8F') bp2 : EDGSEL2 = 0	(2) Set the REDG2 flag of the IRQ2ICR register to "1" to set the active edge of the IRQ2 at the rising edge. Set the EDGSEL2 flag of the EDGDT register "0" to select the programmable active edge interrupt.
(3) Set the initial output data. P6OUT(x'3F16') bp7-0 : P6OUT7-0 = x'55'	(3) Set the initial output data "55" to the P6OUT register. Port 6 outputs "55".
(4) Set the synchronous output pin. P6SYO(x'3F1E') bp7-0 : P6SYO7-0 = x'FF' P6DIR(x'3F36') bp7-0 : P6DIR7-0 = x'FF'	(4) Set port 6 to synchronous output pin by setting the P6SYO7-0 flag of the P6SYO register to "FF". Select the output mode by setting the P6DIR7-0 flag of the P6DIR register to "FF".
(5) Set the synchronous output data. P6OUT(x'3F16') bp7-0 : P6OUT7-0 = x'AA'	(5) Set the synchronous output data "AA" to the P6OUT register.
(6) Event is generated. Rising edge is generated at P22.	(6) Port 6 outputs "AA" at the rising edge of IRQ2.

Chapter 5 Prescaler

5

5-1 Overview

This LSI has 2 prescalers that can be used by its peripheral functions at the same time. Each of them count with fosc or fs as a base clock. Its hardware is constructed as follows ;

Prescaler 0 (fosc count)	7 bit prescaler
Prescaler 1 (fs count)	3 bit prescaler

Prescaler 0 outputs fosc/2, fosc/4, fosc/16, fosc/32, fosc/64, fosc/128 as cycle clock. Prescaler 1 outputs fs/2, fs/4, fs/8 as cycle clock. Prescaler is used when cycle clock based fosc and fs is used on the following peripheral functions ;

External interrupt 0 interface (with noise filter)
External interrupt 1 interface (with noise filter)
Timer 0 (8-Bit timer counter)
Timer 1 (8-Bit timer counter)
Timer 4 (8-Bit timer counter)
Timer 5 (8-Bit timer counter)
Serial interface 0 (Clock synchronous / Duplex UART)
Serial interface 1 (Clock synchronous / Half-duplex UART)
Serial interface 3 (Clock synchronous / Single master IIC)

About fosc, fs, refer to chapter 2. 2-5 Clock Switching [p.II-32].

5-1-1 Peripheral Functions

Table 5-1-1 shows several kinds of clock source that can be selected by each peripheral functions from prescaler output.

Table 5-1-1 Peripheral Functions Used with Prescaler Output

Clock source selection	Peripheral functions								
	External interrupt 0	External interrupt 1	Timer 0	Timer 1	Timer 4	Timer 5	Serial interface 0	Serial interface 1	Serial interface 3
fosc/2	-	-	-	-	-	-	√	√	√
fosc/4	-	-	√	√	√	√	√	√	√
fosc/16	-	-	√	√	√	√	√	√	√
fosc/32	-	-	√	-	√	√	-	-	√
fosc/64	-	-	√	√	√	√	√	√	-
fosc/128	√	√	-	√	-	-	-	-	-
fs/2	-	-	√	√	√	√	√	√	√
fs/4	-	-	√	-	√	√	√	√	√
fs/8	-	-	-	√	-	-	-	-	-
Timer 4 output	-	-	-	-	-	-	-	√	-
Timer 5 output	-	-	-	-	-	-	√	-	√

5-1-2 Block Diagram

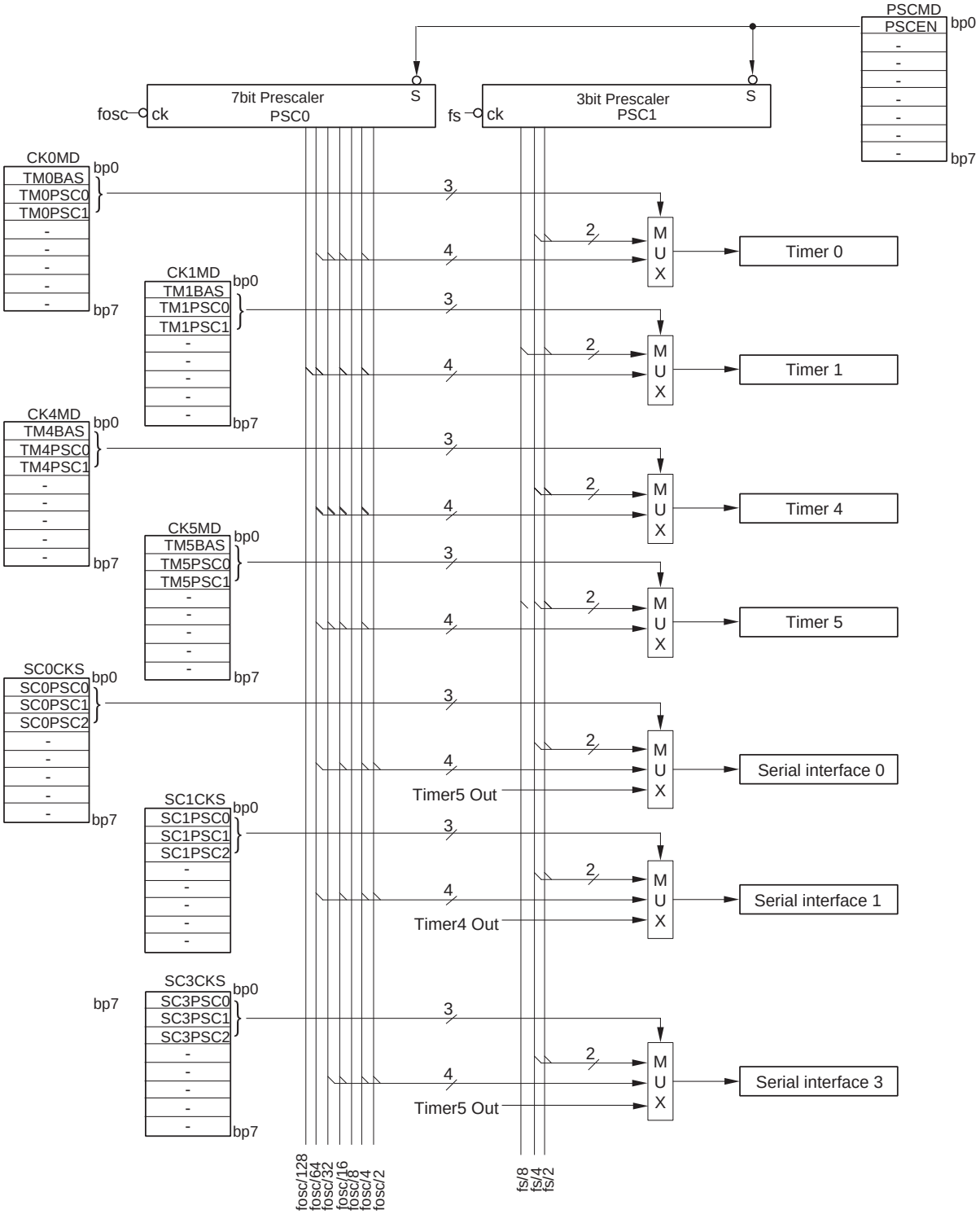


Figure 5-1-1 Prescaler Block Diagram

5-2 Control Register

5-2-1 Registers List

Table 5-2-1 shows registers to control prescaler.

Table 5-2-1 Prescaler Control Registers

Register	Address	R/W	Function	Page
PSCMD	x'03F6F'	R/W	Prescaler control register	V-6
CK0MD	x'03F56'	R/W	Timer 0 prescaler selection register	V-7
CK1MD	x'03F57'	R/W	Timer 1 prescaler selection register	V-7
CK4MD	x'03F66'	R/W	Timer 4 prescaler selection register	V-8
CK5MD	x'03F67'	R/W	Timer 5 prescaler selection register	V-8
SC0CKS	x'03F97'	R/W	Serial interface 0 transfer clock selection register	V-9
SC1CKS	x'03F9F'	R/W	Serial interface1 transfer clock selection register	V-9
SC3CKS	x'03FAF'	R/W	Serial interface 3 transfer clock selection register	V-10

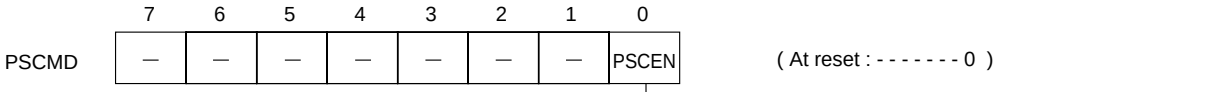
R/W : Readable/Writable

5-2-2 Control Registers

Registers that select prescaler outputs cycle clock and prescaler operation control, consists of the prescaler control register (PSCMD), the timer prescaler selection register (CKnMD) and the serial transfer clock selection register (SCnCKS).

The prescaler control register controls if counting of prescaler is permitted or not.

■Prescaler Control Register (PSCMD)



PSCEN	Prescaler 0, 1 count control
0	Disable the count
1	Enable the count

Figure 5-2-1 Prescaler Control Register (PSCMD : x'03F6F', R/W)

The timer prescaler selection register selects the count clock that used in 8-bit timer.

■Timer 0 Prescaler Selection Register (CK0MD)

	7	6	5	4	3	2	1	0	
CK0MD	—	—	—	—	—	TM0PSC1	TM0PSC0	TM0BAS	(At reset : - - - - - X X X)

TM0PSC1	TM0PSC0	TM0BAS	Clock source selection
0	0	0	fosc/4
	1		fosc/16
1	0		fosc/32
	1		fosc/64
-	0	1	fs/2
	1		fs/4

Figure 5-2-2 Timer 0 Prescaler Selection Register (CK0MD : x'03F56', R/W)

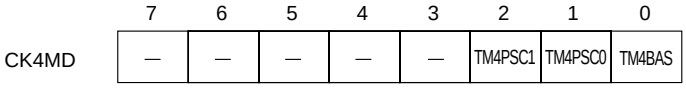
■Timer 1 prescaler selection register (CK1MD)

	7	6	5	4	3	2	1	0	
CK1MD	—	—	—	—	—	TM1PSC1	TM1PSC0	TM1BAS	(At reset : - - - - - X X X)

TM1PSC1	TM1PSC0	TM1BAS	Clock source selection
0	0	0	fosc/4
	1		fosc/16
1	0		fosc/64
	1		fosc/128
-	0	1	fs/2
	1		fs/8

Figure 5-2-3 Timer 1 Prescaler Selection Register (CK1MD : x'03F57', R/W)

■Timer 4 Prescaler Selection Register (CK4MD)

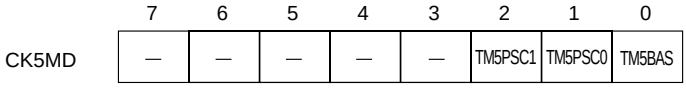


(At reset : - - - - - X X X)

TM4PSC1	TM4PSC0	TM4BAS	Clock source selection
0	0	0	fosc/4
	1		fosc/16
1	0		fosc/32
	1		fosc/64
-	0	1	fs/2
	1		fs/4

Figure 5-2-4 Timer 4 Prescaler Selection Register (CK4MD : x'03F66', R/W)

■Timer 5 Prescaler Selection Register (CK5MD)



(At reset : - - - - - X X X)

TM5PSC1	TM5PSC0	TM5BAS	Clock source selection
0	0	0	fosc/4
	1		fosc/16
1	0		fosc/32
	1		fosc/65
-	0	1	fs/2
	1		fs/4

Figure 5-2-5 Timer 5 Prescaler Selection Register (CK5MD : x'03F67', R/W)

The serial interface transfer clock selection register (SCnCKS) selects the transfer clock used for serial data transfer.

■Serial Interface 0 Transfer Clock Selection Register (SC0CKS)

	7	6	5	4	3	2	1	0	
SC0CKS	—	—	—	—	Reserved	SC0PSC2	SC0PSC1	SC0PSC0	(At reset : - - - - 0 X X X)

SC0PSC2	SC0PSC1	SC0PSC0	Clock source selection
0	0	0	fosc/2
		1	fosc/4
	1	0	fosc/16
		1	fosc/64
1	0	0	fs/2
		1	fs/4
	1	X	Timer 5 output

Reserved	Set always to "0"

Figure 5-2-6 Serial Interface 0 Transfer Clock Selection Register (SC0CKS : x'03F97', R/W)

■Serial Interface 1 Transfer Clock Selection Register (SC1CKS)

	7	6	5	4	3	2	1	0	
SC1CKS	—	—	—	—	Reserved	SC1PSC2	SC1PSC1	SC1PSC0	(At reset : - - - - 0 X X X)

SC1PSC2	SC1PSC1	SC1PSC0	Clock source selection
0	0	0	fosc/2
		1	fosc/4
	1	0	fosc/16
		1	fosc/64
1	0	0	fs/2
		1	fs/4
	1	X	Timer 4 output

Reserved	Set always to "0"

Figure 5-2-7 Serial Interface 1 Transfer Clock Selection Register (SC1CKS : x'03F9F', R/W)

■Serial Interface 3 Transfer Clock Selection Register (SC3CKS)

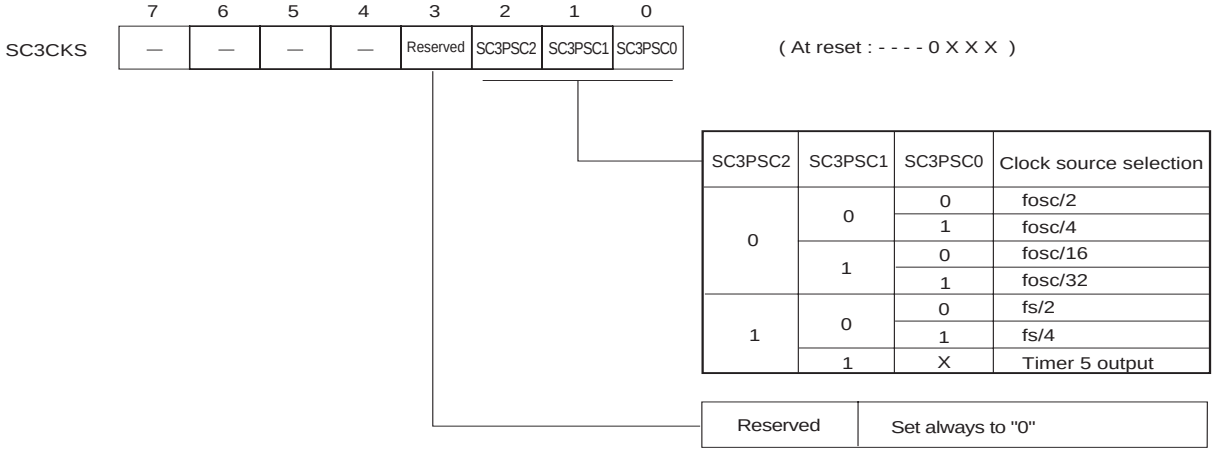


Figure 5-2-8 Serial Interface 3 Transfer Clock Selection Register (SC3CKS : x'03FAF', R/W)

5-3 Operation

5-3-1 Operation

■Prescaler Operation (Prescaler 0 to 1)
Prescaler 0 is a 7-bit and prescaler 1 is a 3-bit free-running counter that divides the base clock. This prescaler can be started or stopped by the PSCEN flag of the prescaler control register (PSCMD).

■Count Timing of Prescaler Operation (Prescaler 0 and 1)
Prescaler 0 counts up at the falling edge of fosc.
Prescaler 1 counts up at the falling edge of fs.

■Peripheral Functions with Prescaler Output Cycle Clock
Table 5-3-1 shows the prescaler output clock source that the peripheral functions can be used, and the registers that control the clock source selection.

Table 5-3-1 Peripheral Functions Used with Prescaler Output Cycle Clock

Peripheral functions		Control register
External interrupt 0	Noise filter sampling clock	-
External interrupt 1	Noise filter sampling clock	-
Timer 0	Count clock	CK0MD
Timer 1	Count clock	CK1MD
Timer 4	Count clock	CK4MD
Timer 5	Count clock	CK5MD
Serial 0	Transfer clock	SC0CKS
Serial 1	Transfer clock	SC1CKS
Serial 3	Transfer clock	SC3CKS

When the prescaler output clock source is used, counting of prescaler should be enabled before starting the peripheral functions.

5-3-2 Setup Example

■Prescaler Setup Example (Timer 0 count clock)
Select the clock of fosc/16 that is output from the prescaler 0, to the count clock of the timer 0.
An example setup procedure , with a description of each step is shown below.

Setup Procedure	Description
(1) Select the prescaler output. CK0MD (x'3F56') bp2-1 : TM0PSC1-0 = 01 bp0 : TM0BAS = 0 (2) Enable the prescaler output. PSCMD (x'3F6F') bp0 : PSCEN = 1	(1) Select the prescaler output to fosc/16 by the TM0PSC1-0, TM0BAS flag of the timer 0 prescaler selection register (CK0MD). (2) Enable the prescaler counting by setting the PSCEN flag of the prescaler control register (PSCMD) to "1".

Enable the prescaler counting by the PSCEN flag of the prescaler control register (PSCMD). The prescaler counting is started after it is enabled.
Start the timer operation after the prescaler is set. Also, the selection of the prescaler output should be set by the timer mode register.

Chapter 6 8-bit Timers

6

6-1 Overview

This LSI contains two general purpose 8-bit timers (Timers 0 and 1) and two 8-bit timers (Timers 4 and 5) that can be also used as baud rate timer. The general purpose 8-bit timers can be used as 16-bit timers with cascade connection.
In a cascade connecion, timers 0, 4 and 5 form the "timer 0", or the lower 8 bits of 16-bit counter, and timers 1 form the "timer 1", or the upper 8 bits. Timers 4 and 5 cannot be cascaded.

Fosc or fs can be selected as the clock source for each timer by using the prescaler. Also, remote control output circuit is built in.

6-1-1 Functions

Table 6-1-1 shows functions of each timer.

Table 6-1-1 Timer Functions

	Timer 0 (8 bit)	Timer 1 (8 bit)	Timer 4 (8 bit)	Timer 5 (8 bit)
Interrupt source	TM0IRQ	TM1IRQ	TM4IRQ	TM5IRQ
Timer operation	√	√	√	√
Event count	√	√	√	√
Timer pulse output	√	√	√	√
PWM output	√	-	√	√
Synchronous output	-	√	-	-
Serial transfer clock output	-	-	√	√
Pulse width measurement	√	-	√	√
Cascade connection	√		-	-
Premote control carrier output	√	-	-	√
Clock source	fosc fosc/4 fosc/16 fosc/32 fosc/64 fs/2 fs/4 fx TM0IO input	fosc fosc/4 fosc/16 fosc/64 fosc/128 fs/2 fs/8 fx TM1IO input	fosc fosc/4 fosc/16 fosc/32 fosc/64 fs/2 fs/4 fx TM4IO input	fosc fosc/4 fosc/16 fosc/32 fosc/64 fs/2 fs/4 fx TM5IO input

fosc: Machine clock (High speed oscillation)
fx: Machine clock (Low speed oscillation)
fs: System clock [☞ Chapter 2 2.5 Clock Switching]
-When timer 4 and 5 are used as a transfer clock for serial interface 1 function, it is not used as a general timer.

6-1-2 Block Diagram

■Timers 0 and 1 Block Diagram

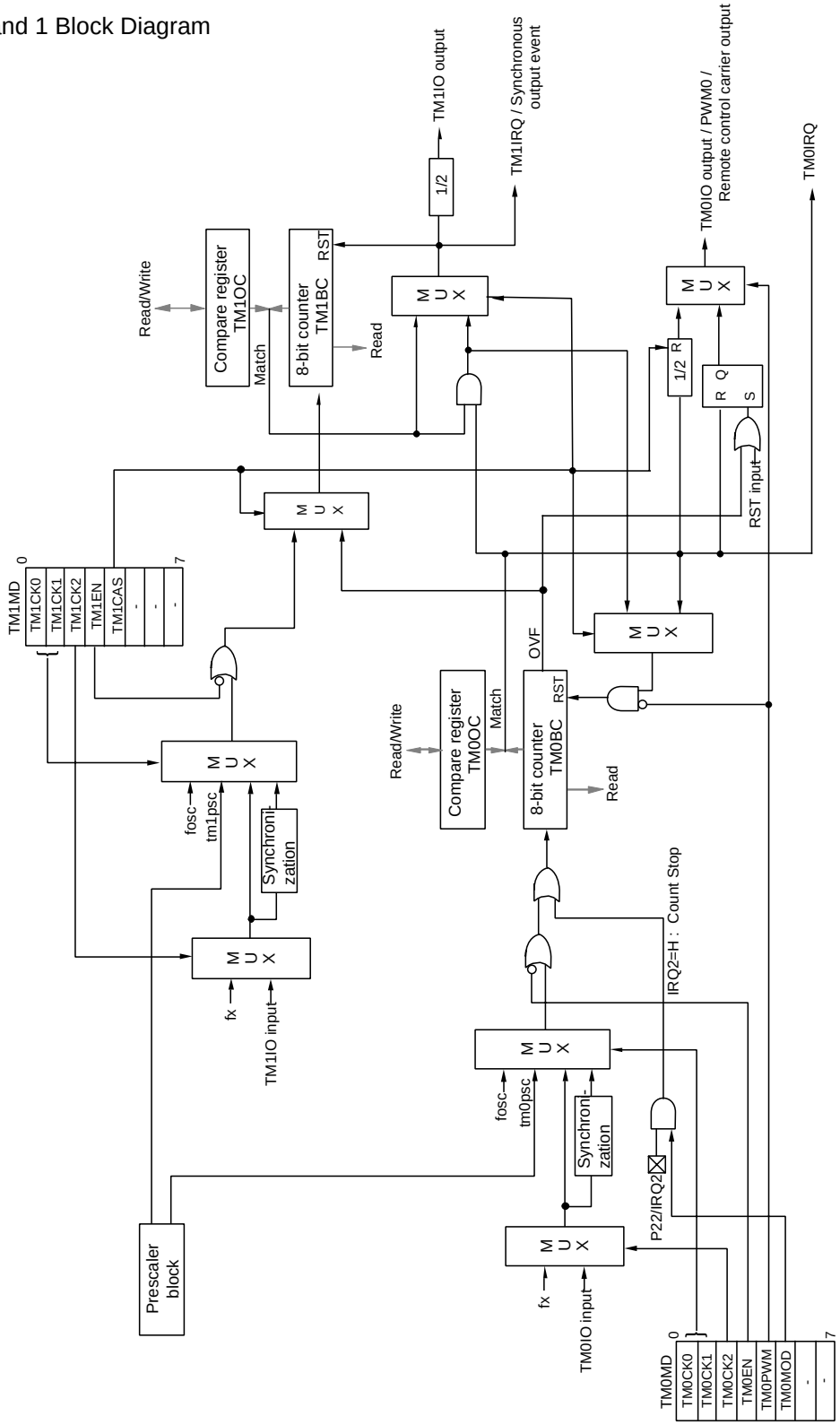


Figure 6-1-1 Timers 0 and 1 Block Diagram

■Timer 4 and 5 Block Diagram

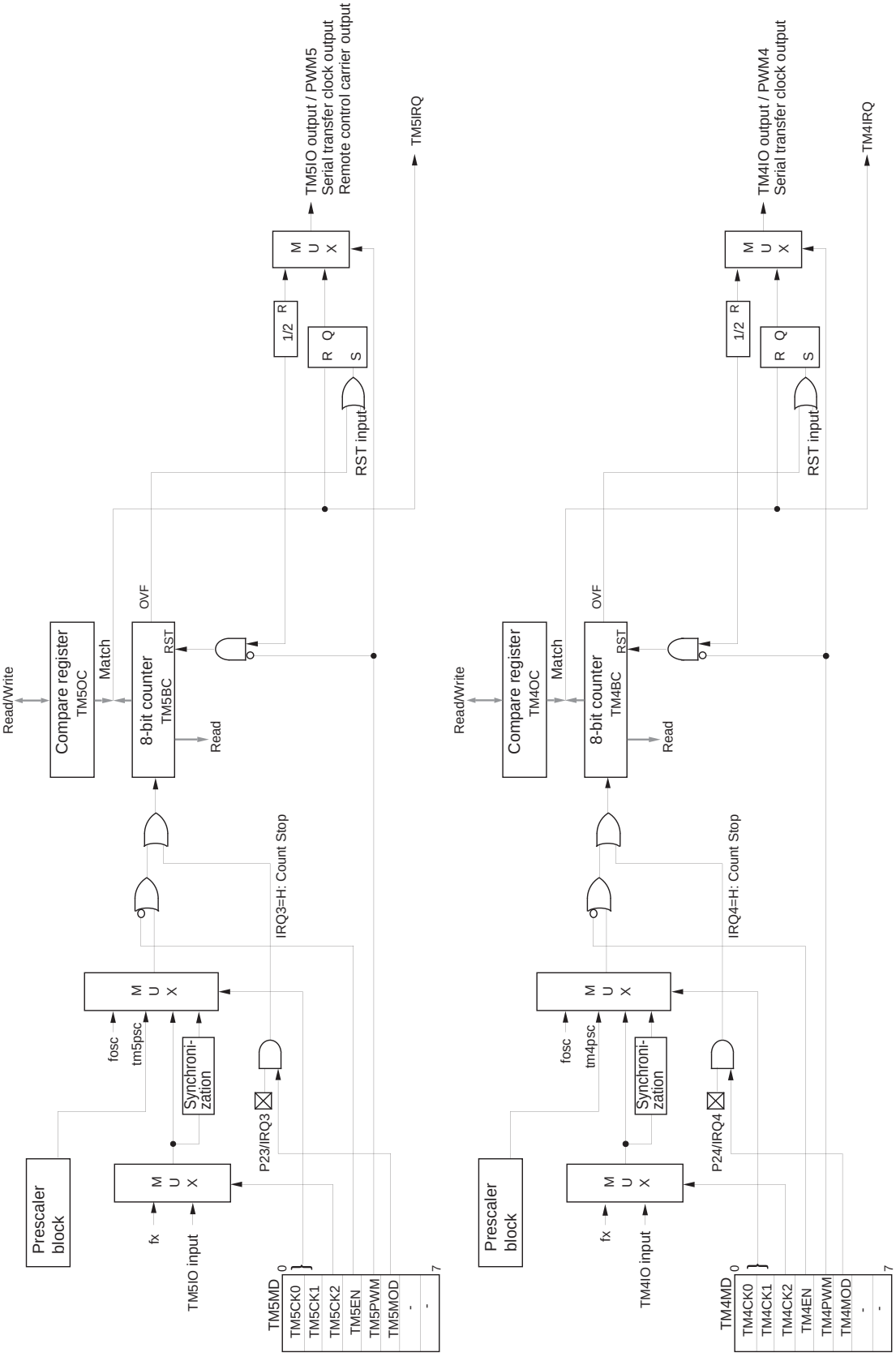


Figure 6-1-2 Timer 4 and 5 Block Diagram

■Remote Control Carrier Output Block Diagram

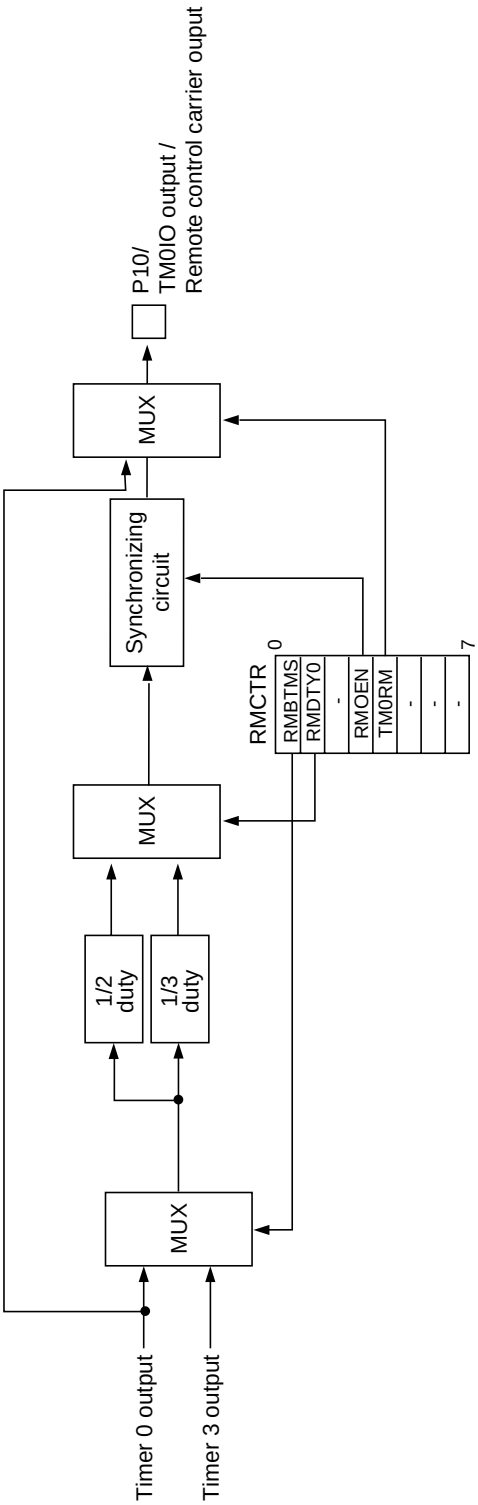


Figure 6-1-3 Remote Control Carrier Output Block Diagram

6-2 Control Registers

Timers 0, 1, 4 and 5 consist of the binary counter (TMnBC) and the compare register (TMnOC). And they are controlled by the mode register (TMnMD).
When the prescaler output is selected as the count clock source of timers 0, 1 4 and 5, they should be controlled by the prescaler control register (PSCMD) and the prescaler selection register (CKnMD). Remote control carrier output is controlled by the remote control carrier output control register (RMCTR).

6-2-1 Registers

Table 6-2-1 shows registers that control timers 0, 1, 4, 5 and remote control carrier output

Table 6-2-1 8-bit Timer Control Registers

	Register	Address	R/W	Function	Page
Timer 0	TM0BC	x'03F50'	R	Timer 0 binary counter	VI-9
	TM0OC	x'03F52'	R/W	Timer 0 compare register	VI-8
	TM0MD	x'03F54'	R/W	Timer 0 mode register	VI-10
	CK0MD	x'03F56'	R/W	Timer 0 prescaler selection register	V-7
	PSCMD	x'03F6F'	R/W	Prescaler control register	V-6
	TM0ICR	x'03FE9'	R/W	Timer 0 interrupt control register	III-22
	P1OMD	x'03F2F'	R/W	Port 1 output mode register	IV-14
	P1DIR	x'03F31'	R/W	Port 1 direction control register	IV-13
Timer 1	TM1BC	x'03F51'	R	Timer 1 binary counter	VI-9
	TM1OC	x'03F53'	R/W	Timer 1 compare register	VI-8
	TM1MD	x'03F55'	R/W	Timer 1 mode register	VI-11
	CK1MD	x'03F57'	R/W	Timer 1 prescaler selection register	V-7
	PSCMD	x'03F6F'	R/W	Prescaler control register	V-6
	TM1ICR	x'03FEA'	R/W	Timer 1 interrupt control register	III-23
	P1OMD	x'03F2F'	R/W	Port 1 output mode register	IV-14
	P7DIR	x'03F37'	R/W	Port 7 direction control register	IV-31

	Register	Address	R/W	Function	Page
Timer 4	TM4BC	x'03F60'	R	Timer 4 binary counter	VI-9
	TM4OC	x'03F62'	R/W	Timer 4 compare register	VI-8
	TM4MD	x'03F64'	R/W	Timer 4 mode register	VI-12
	CK4MD	x'03F66'	R/W	Timer 4 prescaler selection register	V-8
	PSCMD	x'03F6F'	R/W	Prescaler control register	V-6
	TM4ICR	x'03FED'	R/W	Timer 4 interrupt control register	III-24
	P1OMD	x'03F2F'	R/W	Port 3 output mode register	IV-14
	P1DIR	x'03F31'	R/W	Port 1 direction control register	IV-13
Timer 5	TM5BC	x'03F60'	R	Timer 4 binary counter	VI-9
	TM5OC	x'03F62'	R/W	Timer 4 compare register	VI-8
	TM5MD	x'03F64'	R/W	Timer 4 mode register	VI-13
	CK5MD	x'03F66'	R/W	Timer 4 prescaler selection register	V-8
	PSCMD	x'03F6F'	R/W	Prescaler control register	V-6
	TM5ICR	x'03FED'	R/W	Timer 4 interrupt control register	III-25
	P1OMD	x'03F2F'	R/W	Port 1 output mode register	IV-14
	P7DIR	x'03F37'	R/W	Port 7 direction control register	IV-31
Remote control carrier output	RMCTR	x'03F6E'	R/W	Remote control carrier output control register	VI-14

R/W : Readable / Writable

R : Readable only

6-2-2 Programmable Timer Registers

Each of timers 0, 1, 4 and 5 has 8-bit programmable timer registers. Programmable timer register consists of compare register and binary counter.

Compare register is 8-bit register which stores the value to be compared to binary counter.

■Timer 0 Compare Register (TM0OC)

	7	6	5	4	3	2	1	0	
TM0OC	TM0OC7	TM0OC6	TM0OC5	TM0OC4	TM0OC3	TM0OC2	TM0OC1	TM0OC0	(At reset : X X X X X X X X)

Figure 6-2-1 Timer 0 Compare Register (TM0OC : x'03F52', R/W)

■Timer 1 Compare Register (TM1OC)

	7	6	5	4	3	2	1	0	
TM1OC	TM1OC7	TM1OC6	TM1OC5	TM1OC4	TM1OC3	TM1OC2	TM1OC1	TM1OC0	(At reset : X X X X X X X X)

Figure 6-2-2 Timer 1 Compare Register (TM1OC : x'03F53', R/W)

■Timer 4 Compare Register (TM4OC)

	7	6	5	4	3	2	1	0	
TM4OC	TM4OC7	TM4OC6	TM4OC5	TM4OC4	TM4OC3	TM4OC2	TM4OC1	TM4OC0	(At reset : X X X X X X X X)

Figure 6-2-3 Timer 4 Compare Register (TM4OC : x'03F62', R/W)

■Timer 5 Compare Register (TM5OC)

	7	6	5	4	3	2	1	0	
TM5OC	TM5OC7	TM5OC6	TM5OC5	TM5OC5	TM5OC3	TM5OC2	TM5OC1	TM5OC0	(At reset : X X X X X X X X)

Figure 6-2-4 Timer 5 Compare Register (TM5OC : x'03F63', R/W)

Binary counter is 8-bit up counter. If any data is written to compare register during counting is stopped, binary counter is cleared to x'00'.

■Timer 0 Binary Counter (TM0BC)

	7	6	5	4	3	2	1	0	
TM0BC	TM0BC7	TM0BC6	TM0BC5	TM0BC4	TM0BC3	TM0BC2	TM0BC1	TM0BC0	(At reset : X X X X X X X X)

Figure 6-2-5 Timer 0 Binary Counter (TM0BC : x'03F50', R)

■Timer 1 Binary Counter (TM1BC)

	7	6	5	4	3	2	1	0	
TM1BC	TM1BC7	TM1BC6	TM1BC5	TM1BC4	TM1BC3	TM1BC2	TM1BC1	TM1BC0	(At reset : X X X X X X X X)

Figure 6-2-6 Timer 1 Binary Counter (TM1BC : x'03F51', R)

■Timer 4 Binary Counter (TM4BC)

	7	6	5	4	3	2	1	0	
TM4BC	TM4BC7	TM4BC6	TM4BC4	TM4BC4	TM4BC3	TM4BC2	TM4BC1	TM4BC0	(At reset : X X X X X X X X)

Figure 6-2-7 Timer 4 Binary Counter (TM4BC : x'03F60', R)

■Timer 5 Binary Counter (TM5BC)

	7	6	5	4	3	2	1	0	
TM5BC	TM5BC7	TM5BC6	TM5BC5	TM5BC5	TM5BC3	TM5BC2	TM5BC1	TM5BC0	(At reset : X X X X X X X X)

Figure 6-2-8 Timer 5 Binary Counter (TM5BC : x'03F61', R)

6-2-3 Timer Mode Registers

Timer mode register is readable/writable register that controls timers 0, 1, 4 and 5.

■Timer 0 Mode Register (TM0MD)

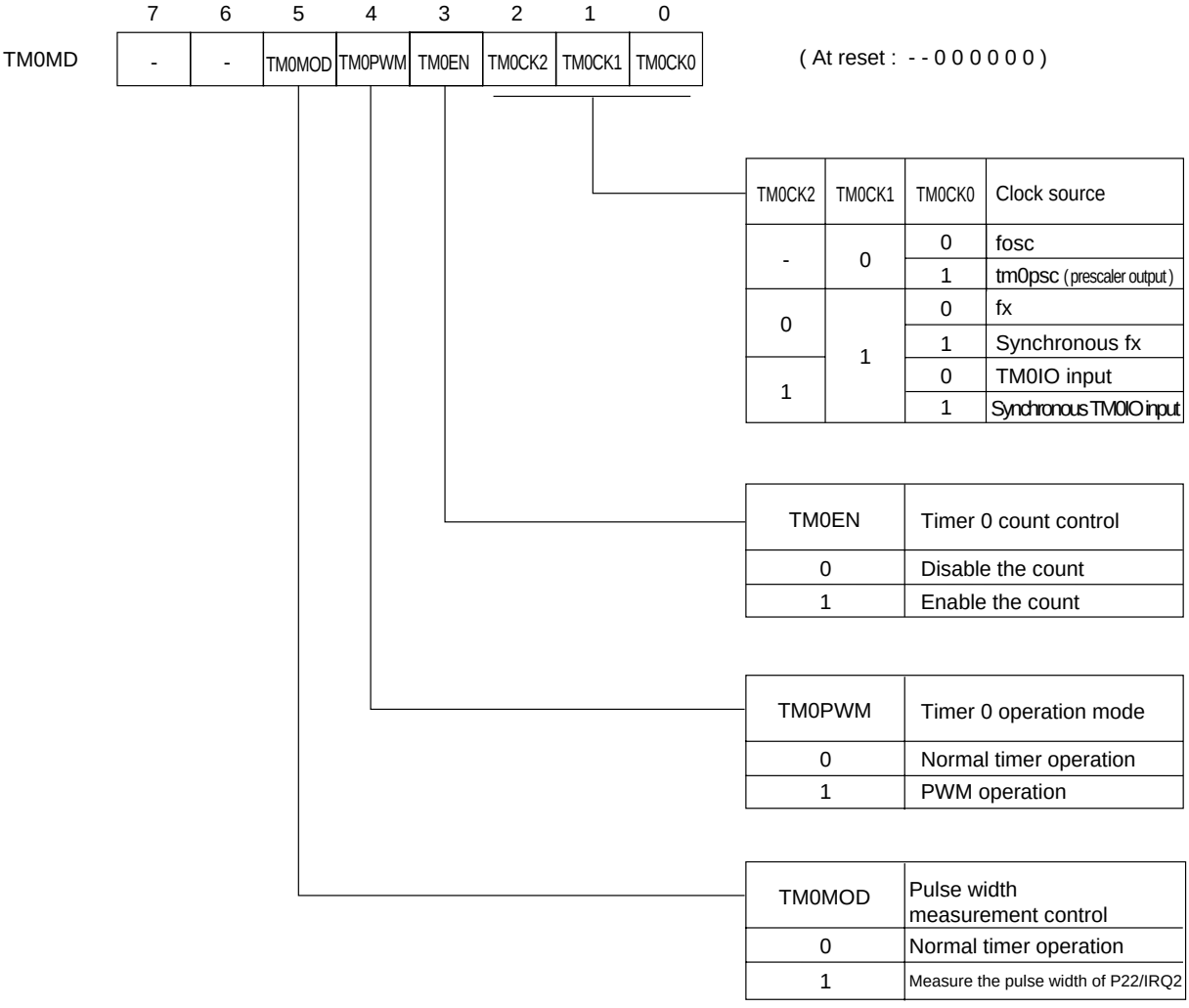


Figure 6-2-9 Timer 0 Mode Register (TM0MD : x'03F54', R/W)

■Timer 1 Mode Register (TM1MD)

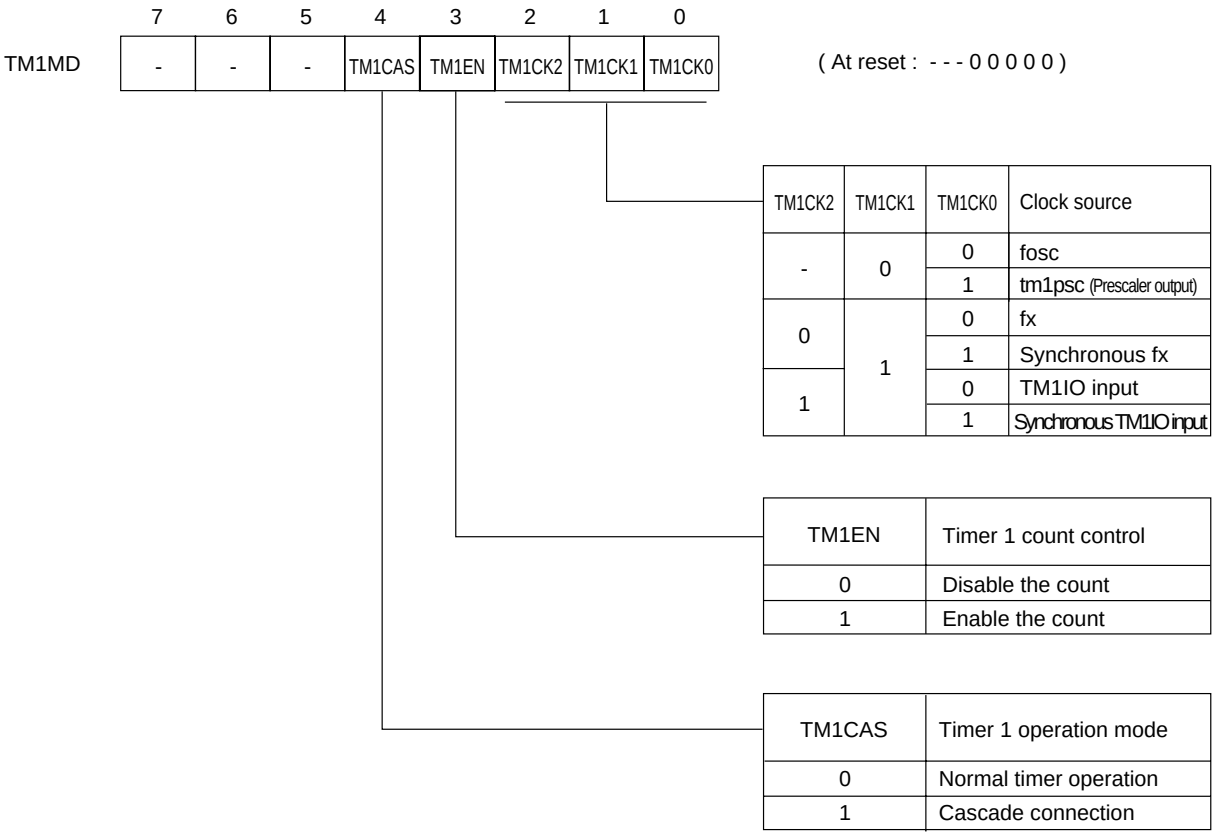


Figure 6-2-10 Timer 1 Mode Register (TM1MD : x'03F55', R/W)

■Timer 4 Mode Register (TM4MD)

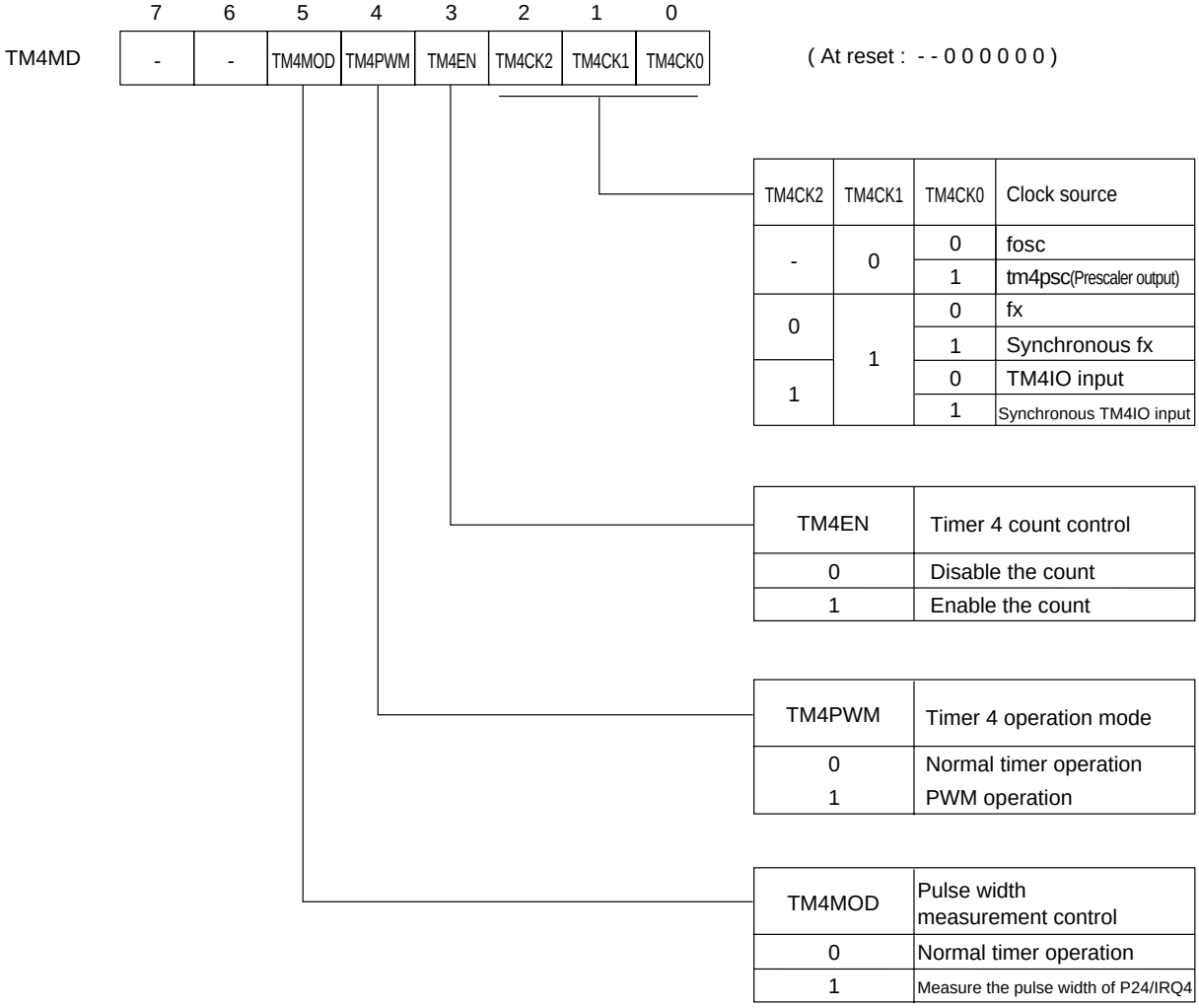


Figure 6-2-11 Timer 4 Mode Register (TM4MD : x'03F64', R/W)

■Timer 5 Mode Register (TM5MD)

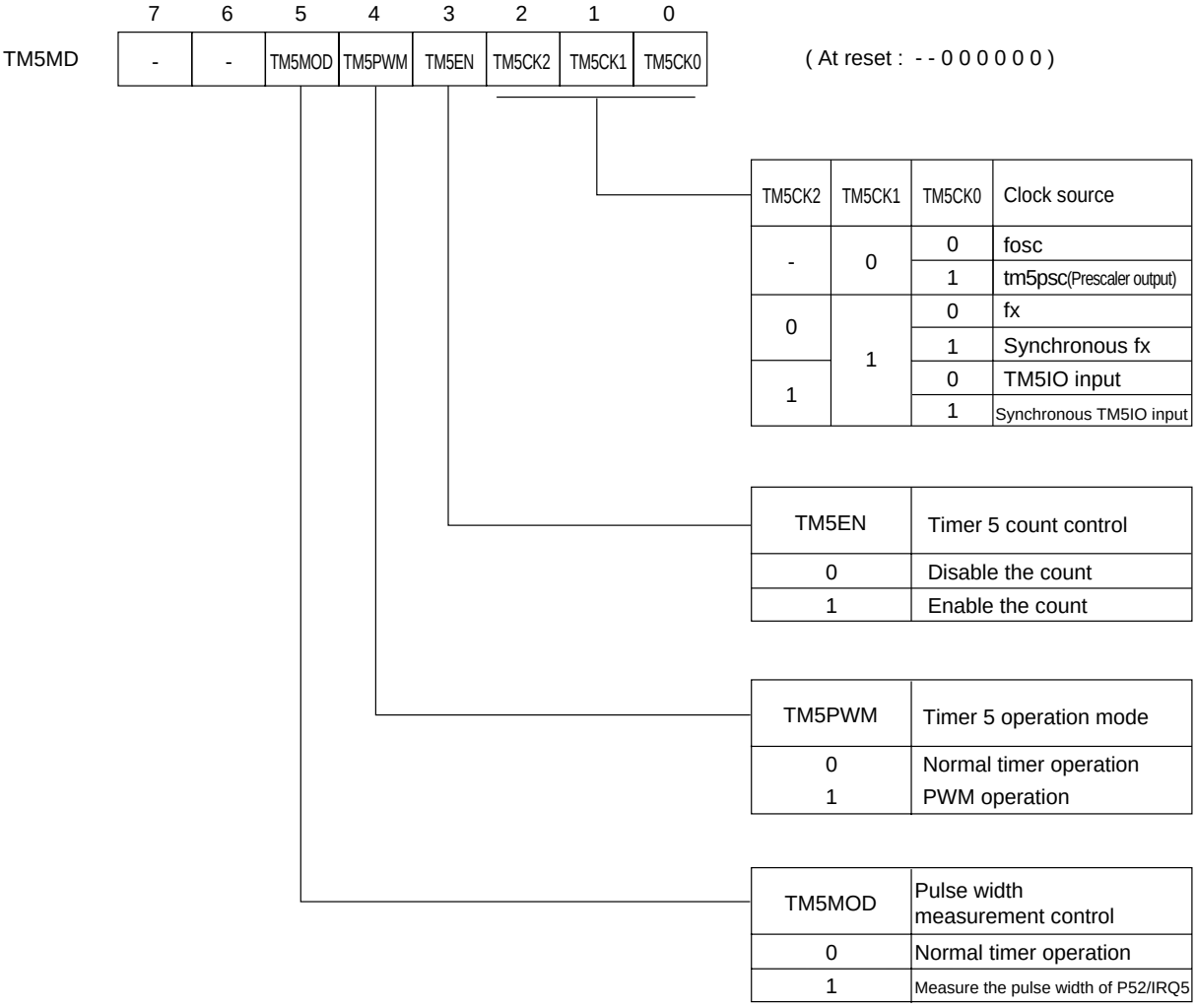


Figure 6-2-12 Timer 5 Mode Register (TM5MD : x'03F65', R/W)

■Remote Control Carrier Output Control Register (RMCTR)

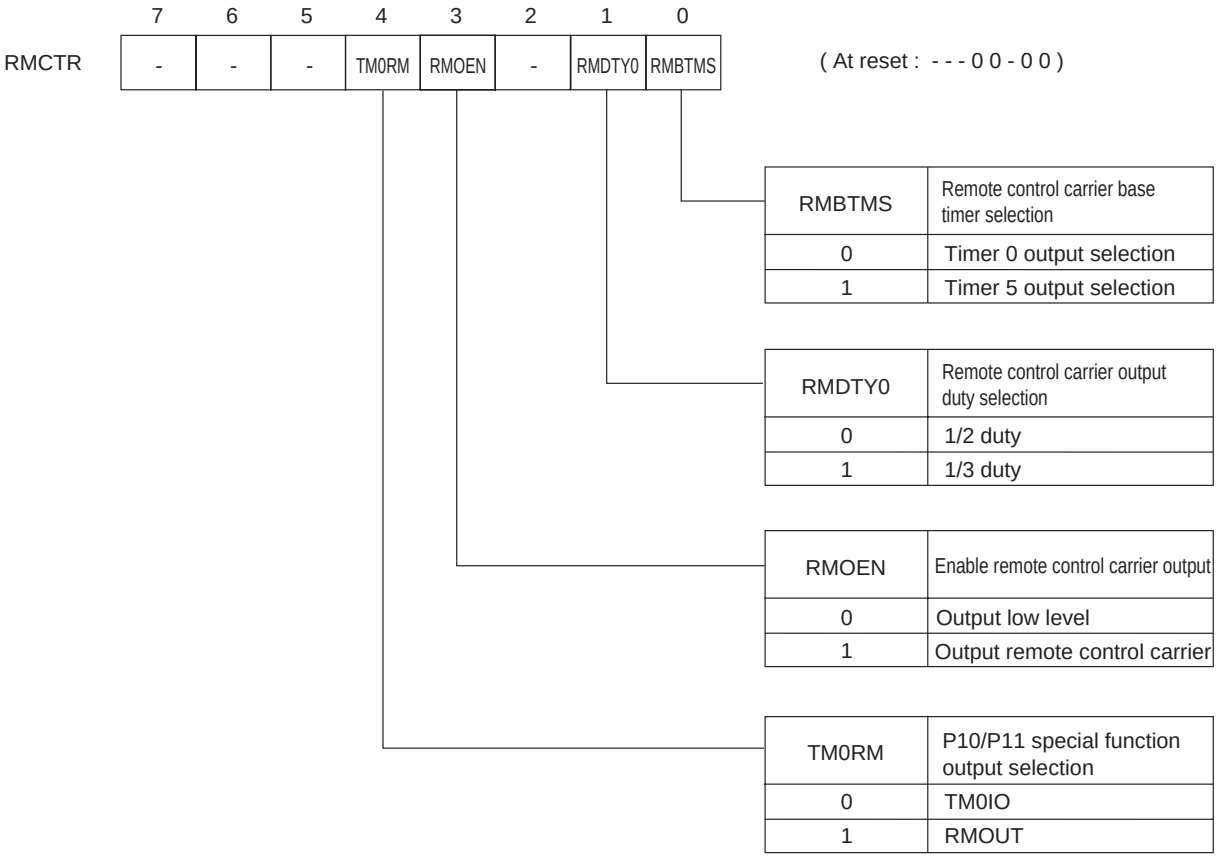


Figure 6-2-13 Remote Control Carrier Output Control Register (RMCTR : x'03F6E', R/W)

6-3 8-bit Timer Count

6-3-1 Operation

The timer operation can constantly generate interrupts.

■8-bit Timer Operation (Timers 0, 1, 4 and 5)
The generation cycle of timer interrupts is set by the clock source selection and the setting value of the compare register (TMnOC), in advance. If the binary counter (TMnBC) reaches the setting value of the compare register, an interrupt is generated at the next count clock, then binary counter is cleared and counting is restarted from x'00'.
Table 6-3-1 shows clock source that can be selected.

Table 6-3-1 Clock Source (Timers 0, 1, 4 and 5) at Timer Operation

Clock source	1 count time	Timer 0 (8 Bit)	Timer 1 (8 Bit)	Timer 4 (8 Bit)	Timer 5 (8 Bit)
fosc	50 ns	√	√	√	√
fosc/4	200 ns	√	√	√	√
fosc/16	800 ns	√	√	√	√
fosc/32	1.6 µs	√	-	√	√
fosc/64	3.2 µs	√	√	√	√
fosc/128	6.4 µs	-	√	-	-
fs/2	200 ns	√	√	√	√
fs/4	400 ns	√	-	√	√
fs/8	800 ns	-	√	-	-
fx	30.5 µs	√	√	√	√
Notes : as fosc = 20 MHz fx = 32.768 kHz fs = fosc/2 = 10 MHz					

■Count Timing of Timer Operation (Timers 0, 1, 4 and 5)

Binary counter counts up with selected clock source as a count clock.

The basic operation of the whole function of 8-bit timer is as follows ;

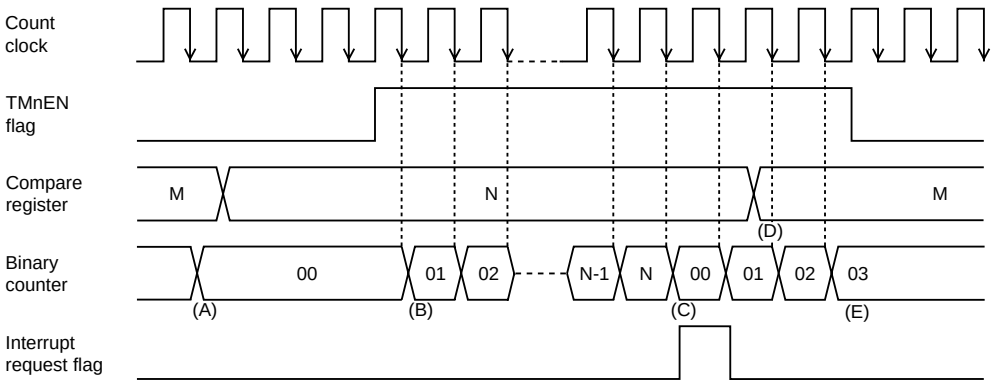


Figure 6-3-1 Count Timing of Timer Operation (Timers 0, 1, 4 and 5)

(A) If the value is written to the compare register during the TMnEN flag is "0", the binary counter is cleared to x'00', at the writing cycle.

(B) If the TMnEN flag is "1", the binary counter is started to count.
The counter starts to count up at the falling edge of the count clock.

(C) If the binary counter reaches the value of the compare register, the interrupt request flag is set at the next count clock, then the binary counter is cleared to x'00' and the counting is restarted.

(D) Even if the compare register is rewritten during the TMnEN flag is "1", the binary counter is not changed.

(E) If the TMnEN flag is "0", the binary counter is stopped.

When the binary counter reaches the value in the compare register, the interrupt request flag is set and the binary counter is cleared, at the next count clock. So set the compare register as:
Compare register setting = (count till the interrupt request - 1)

If the compare register is set the smaller than the binary counter during the count operation, the binary counter counts up to the overflow, at first.

If the interrupt is enabled, the timer interrupt request flag should be cleared before timer operation is started.

The timer n interrupt request generation (at TMnOC = x'00') has the same waveform at TMnOC = x'01'.

6-3-2 Setup Example

■Timer Operation Setup Example (Timers 0, 1, 4 and 5)

Timer function can be set by using timer 0 that generates the constant interrupt. By selecting fs/4 (at fosc = 20 MHz) as a clock source, interrupt is generated every 250 clock cycles (100 µs).

An example setup procedure, with a description of each step is shown below.

Setup Procedure	Description
(1) Stop the counter. TM0MD (x'3F54') bp3 :TM0EN = 0	(1) Set the TM0EN flag of the timer 0 mode register (TM0MD) to "0" to stop the counting of timer 0.
(2) Select the normal timer operation. TM0MD (x'3F54') bp4 :TM0PWM = 0 bp5 :TM0MOD = 0	(2) Set the TM0PWM flag and TM0MOD flag of the TM0MD register to "0" to select the normal timer operation.
(3) Select the count clock source. TM0MD (x'3F54') bp2-0 :TM0CK2-0 = 001	(3) Select the prescaler output to the clock source by the TM0CK2-0 flag of the TM0MD register.
(4) Select the prescaler output and enable the counting. CK0MD (x'3F56') bp2-1 :TM0PSC1-0 = 01 bp0 :TM0BAS = 1 PSCMD (x'3F6F') bp0 :PSCEN = 1	(4) Select fs/4 to the prescaler output by the TM0PSC1-0, TM0BAS flag of the timer 0 prescaler selection register (CK0MD). Also, set the PSCEN flag of the prescaler control register (PSCMD) to "1" to enable the counting of the prescaler.
(5) Set the cycle of the interrupt generation. TM0OC (x'3F52') = x'F9'	(5) Set the value of the interrupt generation cycle to the timer 0 compare register (TM0OC). The cycle is 250, so that the setting value is set to 249 (x'F9'). At that time, the timer 0 binary counter (TM0BC) is initialized to x'00'.
(6) Set the interrupt level. TM0ICR (x'3FE9') bp7-6 :TM0LV1-0 = 10	(6) Set the interrupt level by the TM0LV1-0 flag of the timer 0 interrupt control register (TM0ICR). If the interrupt request flag may be already set, clear the request flag. [☞ Chapter 3 3-1-4. Interrupt flag setting]

Setup Procedure	Description
(7) Enable the interrupt. TM0ICR (x'3FE9') bp1 :TM0IE = 1	(7) Set the TM0IE flag of the TM0ICR register to "1" to enable the interrupt.
(8) Start the timer operation. TM0MD (x'3F54') bp3 :TM0EN = 1	(8) Set the TM0EN flag of the TM0MD register to "1" to start the timer 0.

The TM0BC starts to count up from 'x00'. When the TM0BC reaches the setting value of the TM0OC register, the timer 0 interrupt request flag is set at the next count clock, then the value of the TM0BC becomes x'00' and restart to count up.

When the TMnEN flag of the TMnMD register is changed at the same time to other bit, binary counter may start to count up by the switching operation.

If fx is selected as the count clock source, when the binary counter is read at operation, uncertain value on counting up may be read. To prevent this, select the synchronous fx as the count clock source.
In this case the timer n counter counts up in synchronization with system clock, therefore the correct value is always read.
But, if the synchronous fx is selected as the count clock source, CPU mode cannot return from STOP/HALT mode.

6-4 8-bit Event Count

6-4-1 Operation

Event count operation has 2 types ; TMnIO input and synchronous TMnIO input can be selected as the count clock.

■8-bit Event Count Operation

Event count means that the binary counter (TMnBC) counts the input signal from external to the TMnIO pin. If the value of the binary counter reaches the setting value of the compare register (TMnOC), interrupts can be generated at the next count clock.

Table 6-4-1 Event Count Input Clock

	Timer 0	Timer 2	Timer 4	Timer 5
Event Input	TM0IO input (P11)	TM1IO input (P76)	TM4IO input (P13)	TM5IO input (P77)
	Synchronous TM0IO input	Synchronous TM1IO input	Synchronous TM4IO input	Synchronous TM5IO input

■Count Timing of TMnIO Input (Timers 0, 1, 4 and 5)

When TMnIO input is selected, TMnIO input signal is directly input to the count clock of the timer n. The binary counter counts up at the falling edge of the TMnIO input signal.

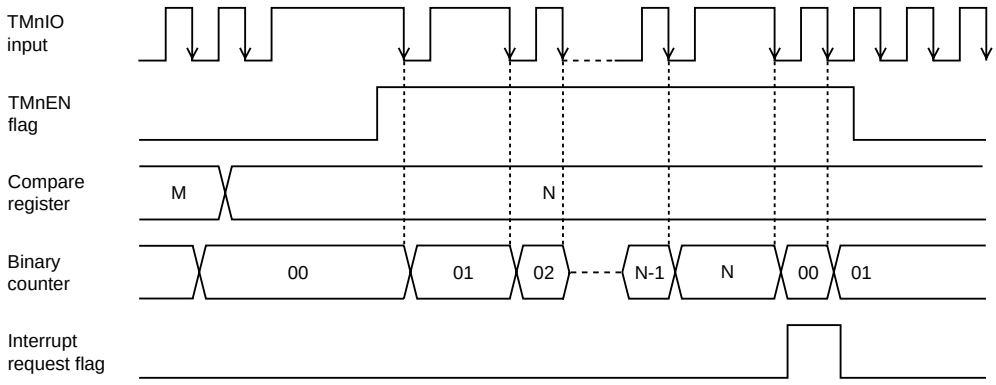


Figure 6-4-1 Count Timing of TMnIO Input (Timers 0, 1, 4 and 5)

When the TMnIO input is selected for count clock source and the value of the timer n binary counter is read during operation, incorrect value at count up may be read out. To prevent this, use the event count by synchronous TMnIO input, as the following page.

■Count Timing of Synchronous TMnIO Input (Timers 0, 1, 4 and 5)

If the synchronous TMnIO input is selected, the synchronizing circuit output signal is input to the timer n count clock. The synchronizing circuit output signal is changed at the falling edge of the system clock after TMnIO input signal is changed.

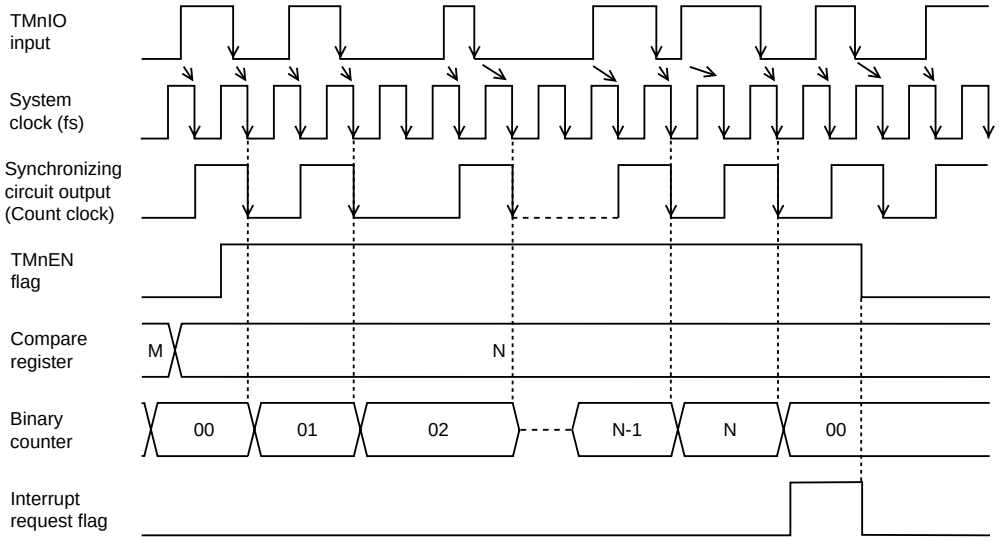


Figure 6-4-2 Count Timing of Synchronous TMnIO Input (Timers 0, 1, 4 and 5)

When the synchronous TMnIO input is selected as the count clock source, the timer n counter counts up in synchronization with system clock, therefore the correct value is always read.

But, if the synchronous TMnIO is selected as the count clock source, CPU mode cannot return from STOP/HALT mode.

6-4-2 Setup Example

■Event Count Setup Example (Timers 0, 1, 4 and 5)

If the falling edge of the TM0IO input pin signal is detected 5 times with using timer 0, an interrupt is generated.

An example setup procedure, with a description of each step is shown below.

Setup Procedure	Description
(1) Stop the counter. TM0MD (x'3F54') bp3 :TM0EN = 0	(1) Set the TM0EN flag of the timer 0 mode register (TM0MD) to "0" to stop timer 0 counting.
(2) Set the special function pin to input. P1DIR (x'3F31') bp0 :P1DIR1 = 0	(2) Set the P1DIR1 flag of the port 1 direction control register (P1DIR) to "0" to set P11 pin to input mode. If it needs, pull up resistor should be added. [☞ Chapter 4. I/O Ports]
(3) Select the normal timer operation. TM0MD (x'3F54') bp4 :TM0PWM = 0 bp5 :TM0MOD = 0	(3) Set the TM0PWM flag and TM0MOD flag of the TM0MD register to "0" to select the normal timer operation.
(4) Select the count clock source. TM0MD (x'3F54') bp2-0 :TM0CK2-0 = 110	(4) Select the clock source to TM0IO input by the TM0CK2-0 flag of the TM0MD register.
(5) Set the interrupt generation cycle. TM0OC (x'3F52') = x'04'	(5) Set the timer 0 compare register (TM0OC) the interrupt generation cycle. Counting is 5, so the setting value should be 4. At that time, the timer 0 binary counter (TM0BC) is initialized to x'00'.
(6) Set the interrupt level. TM0ICR (x'3FE9') bp7-6 :TM0LV1-0 = 10	(6) Set the interrupt level by the TM0LV1-0 flag of the timer 0 interrupt control register (TM0ICR). If the interrupt request flag may be already set, cancel all existing interrupt requests. [☞ Chapter 3 3-1-4. Interrupt Flag Setup]

Setup Procedure	Description
(7) Enable the interrupt. TM0ICR (x'3FE9') bp1 :TM0IE = 1	(7) Set the TM0IE flag of the TM0ICR register to "1" to enable the interrupt.
(8) Start the event counting. TM0MD (x'3F54') bp3 :TM0EN = 1	(8) Set the TM0EN flag of the TM0MD register to 1 to start timer 0.

Every time TM0BC detects the falling edge of TM0IO input , TM0BC counts up from 'x00'. When TM0BC reaches the setting value of theTM0OC register, the timer 0 interrupt request flag is set at the next count clock, then the value of TM0BC becomes x'00' and counting up is restarted.

6-5 8-bit Timer Pulse Output

6-5-1 Operation

The TMnIO pin can output a pulse signal with any cycle.

■Operation of Timer Pulse Output (Timers 0, 1, 4 and 5)
The timers can output 2 x cycle signal, compared to the setting value in compare register (TMnOC). Output pins are as follows ;

Table 6-5-1 Timer Pulse Output Pins

	Timer 0	Timer 1	Timer 4	Timer 5
Pulse output pin	TM0IO output (P10, P11)	TM1IO output (P76)	TM4IO output (P12, P13)	TM5IO output (P77)

■Count Timing of Timer Pulse Output (Timers 0, 1, 4 and 5)

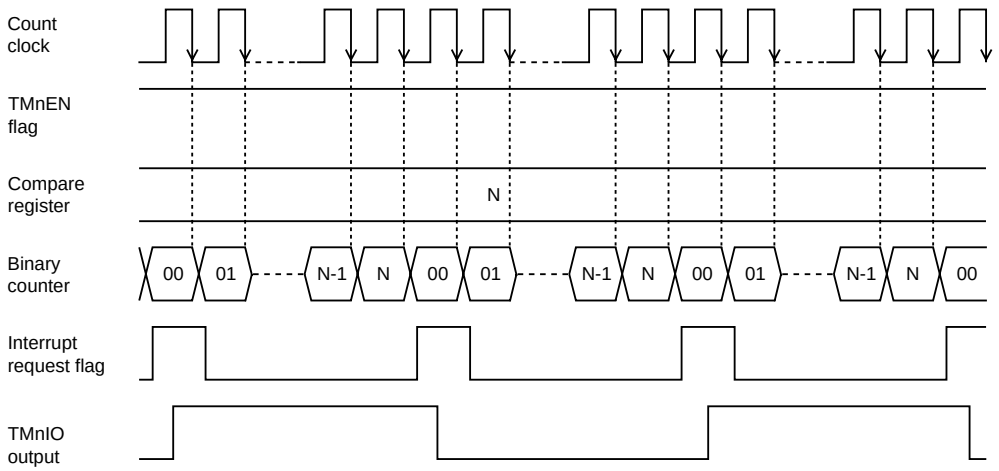


Figure 6-5-1 Count Timing of Timer Pulse Output (Timers 0, 1, 4 and 5)

The TMnIO pin outputs 2 x cycle, compared to the value in the compare register. If the binary counter reaches the compare register, and the binary counter is cleared to x'00', TMnIO output is inverted. The inversion of the timer output is changed at the rising edge of the count clock. This is happened to form waveform inside to correct the output cycle.

6-5-2 Setup Example

■Timer Pulse Output Setup Example (Timers 0, 1, 4 and 5)
TM0IO (P10) pin outputs 50 kHz pulse by using timer 0. For this, select fosc as clock source, and set a 1/2 cycle (100 kHz) for the timer 0 compare register (at fosc=20 MHz).
An example setup procedure, with a description of each step is shown below.

Setup Procedure	Description
(1) Stop the counter. TM0MD (x'3F54') bp3 :TM0EN = 0	(1) Set the TM0EN flag of the timer 0 mode register (TM0MD) to "0" to stop timer 0 counting.
(2) Set the special function pin to the output mode. P1OMD (x'3F2F') bp0 :P1OMD0 = 1 P1DIR (x'3F31') bp0 :P1DIR0 = 1	(2) Set the P1OMD0 flag of the port 1 output mode register (P1OMD) to "1" to set P10 the special function pin. Set the P1DIR0 flag of the port 1 direction control register (P1DIR) to "1" to set output mode. If it needs, pull-up resister should be added. [☞ Chapter 4. I/O Ports]
(3) Select the normal timer operation. TM0MD (x'3F54') bp4 :TM0PWM = 0 bp5 :TM0MOD = 0	(3) Set the TM0PWM flag and TM0MOD flag of the TM0MD register to "0" to select the normal timer operation.
(4) Select the count clock source. TM0MD (x'3F54') bp2-0 :TM0CK2-0 = 000	(4) Select fosc for the clock source by the TM0CK2-0 flag of the TM0MD register.
(5) Set the timer pulse output cycle. TM0OC (x'3F52') = x'C7'	(5) Set the timer 0 compare register (TM0OC) to the 1/2 of the timer pulse output cycle. The setting value should be 200-1=199(x'C7'), because 100 kHz is divided by 20 MHz. At that time, the timer 0 binary counter (TM0BC) is initialized to x'00'.
(6) Start the timer operation. TM0MD (x'3F54') bp3 :TM0EN = 1	(6) Set the TM0EN flag of the TM0MD register to "1" to start timer 0.

TM0BC counts up from x'00'. If TM0BC reaches the setting value of the TM0OC register, then TM0BC is cleared to x'00', TM0IO output signal is inverted and TM0BC restarts to count up from x'00'.

At TMnOC = x'00', timer pulse output has the same waveform to at x'01'.

If any data is written to compare register binary counter is stopped, timer output is reset to "L".

Set the compare register value as follows.

$$\text{The compare register value} = \frac{\text{The timer pulse output cycle}}{\text{The count clock cycle x 2}} - 1$$

6-6 8-bit PWM Output

The TMnIO pin outputs the PWM waveform, which is determined by the match timing for the compare register and the overflow timing of the binary counter.

6-6-1 Operation

■Operation of 8-bit PWM Output (Timers 0, 4 and 5)

The PWM waveform with any duty cycle is generated by setting the duty cycle of PWM "H" period to the compare register (TMnOC). The cycle is the period from the full count to the overflow of the 8-bit timer. Table 6-6-1 shows PWM output pins ;

Table 6-6-1 Output Pins of PWM Output

	Timer 0	Timer 4	Timer 5
PWM output pin	TM0IO output pin (P10, P11)	TM4IO output pin (P12, P13)	TM5IO output pin (P52)

■Count Timing of PWM Output (at normal) (Timers 0, 4 and 5)

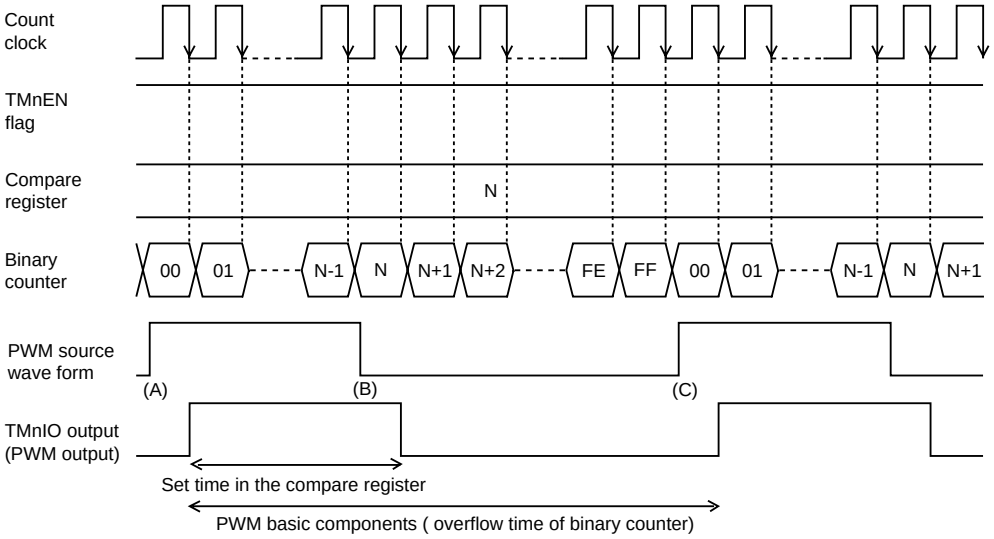


Figure 6-6-1 Count Timing of PWM Output (at Normal)

PWM source waveform,

(A) is "H" while counting up from x'00' to the value stored in the compare register.

(B) is "L" after the match to the value in the compare register, then the binary counter continues counting up till the overflow.

(C) is "H" again, if the binary counter overflow.

The PWM outputs the PWM source waveform with 1 count clock delay. This is happened, because the waveform is created inside to correct the output cycle.

■Count Timing of PWM Output (when the compare register is x'00') (Timers 0, 4 and 5)
Here is the count timing when the compare register is set to x'00' ;

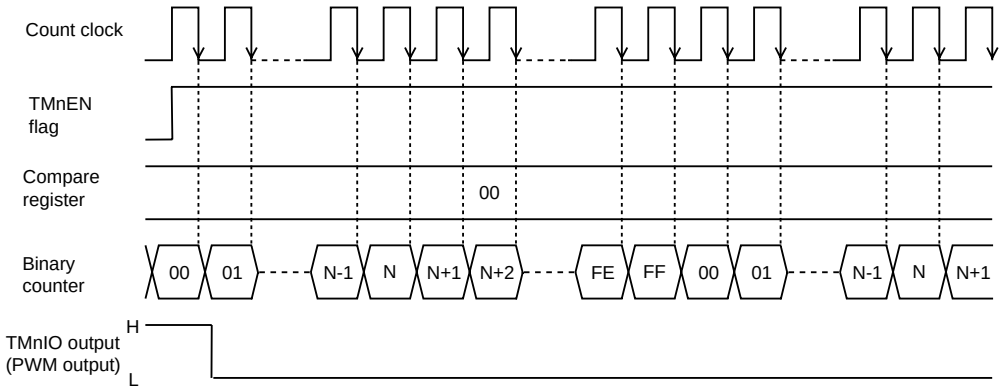


Figure 6-6-2 Count Timing of PWM Output (when compare register is x'00')

When TMnEN flag is stopped ("0") PWM output is "H".

■Count Timing of PWM Output (when the compare register is x'FF') (Timers 0, 4 and 5)
Here is the count timing when the compare register is set to x'FF' ;

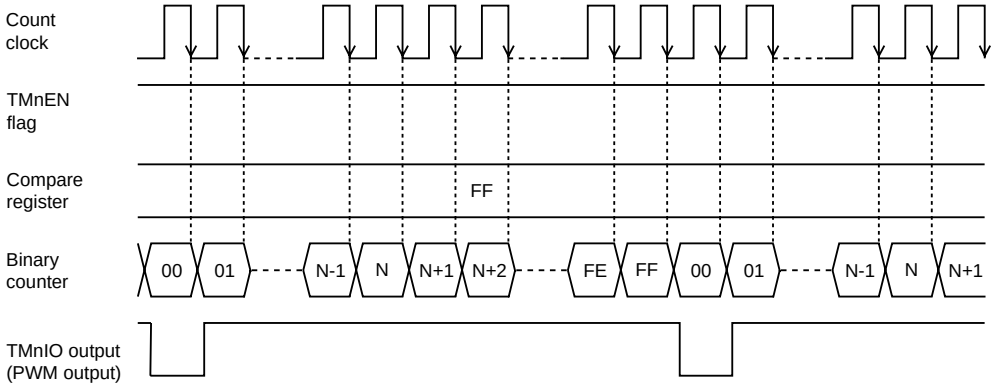


Figure 6-6-3 Count Timing of PWM Output (when compare register is x'FF')

6-6-2 Setup Example

■PWM Output Setup Example (Timers 0, 4 and 5)

The 1/4 duty cycle PWM output waveform is output from the TM0IO output pin at 128 Hz by using timer 0 (at fx=32.768 kHz). Cycle period of PWM output waveform is decided by the overflow of the binary counter. "H" period of the PWM output waveform is decided by the setting value of the compare register. An example setup procedure, with a description of each step is shown below.

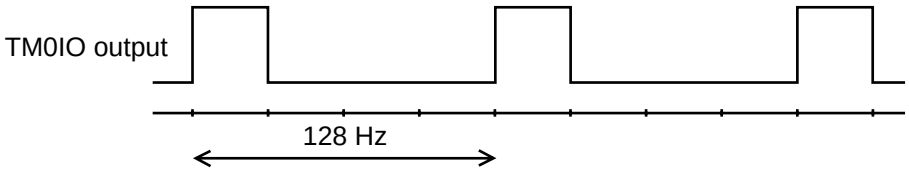


Figure 6-6-4 Output Waveform of TM0IO Output Pin

Setup Procedure	Description
(1) Stop the counter. TM0MD (x'3F54') bp3 :TM0EN = 0	(1) Set the TM0EN flag of the timer 0 mode register (TM0MD) to "0" to stop the timer 0 counting.
(2) Set the special function pin to the output mode. P1OMD (x'3F2F') bp0 :P1OMD0 = 1 P1DIR (x'3F31') bp0 :P1DIR0 = 1	(2) Set the P1OMD0 flag of the port 1 output mode register (P1OMD) to "1" to set P10 pin to the special function pin. Set the P1DIR0 flag of the port 1 direction control register (P1DIR) to "1" for the output mode. If it needs, pull up resistor should be added. [☞ Chapter 4. I/O Ports]
(3) Select the PWM operation. TM0MD (x'3F54') bp4 :TM0PWM = 1 bp5 :TM0MOD = 0	(3) Set the TM0PWM flag of the TM0MD register to "1", the TM0MOD flag to "0" to select the PWM operation.
(4) Select the count clock source. TM0MD (x'3F54') bp2-0 :TM0CK2-0 = 010	(4) Select "fx" for the clock source by the TM0CK2-0 flag of the TM0MD register.

Setup Procedure	Description
(5) Set the period of PWM "H" output. TM0OC (x'3F52') = x'40'	(5) Set the "H" period of PWM output to the timer 0 compare register (TM0OC). The setting value is set to 256 / 4 = 64 (x'40'), because it should be the 1/4 duty of the full count (256). At that time, the timer 0 binary counter (TM0BC) is initialized to x'00'.
(6) Start the timer operation. TM0MD (x'3F54') bp3 :TM0EN = 1	(6) Set the TM0EN flag of the TM0MD register to "1" to operate timer 0.

TM0BC counts up from x'00'. PWM source waveform outputs "H" till TM0BC reaches the setting value of the TM0OC register, and outputs "L" after that. Then, TM0BC continues counting up, and PWM source waveform outputs "H" again, once overflow happens, and TM0BC restarts counting up from x'00'. TM0IO pin outputs the PWM source waveform with 1 count clock delay.

The initial setting of PWM output is changed from "L" output to "H" output at the selection of PWM operation by the TMnPWM flag of the TMnMD register.

6-7 8-bit Timer Synchronous Output

6-7-1 Operation

When the binary counter of the timer reaches the set value of the compare register, the latched data is output from port 6 at the next count clock.

■Synchronous Output Operation by 8-bit timer (Timer 1, Timer 5)
The port 6 latched data is output from the output pin at the interrupt request generation by the match of the binary counter and the compare register.
Only port 6 can perform synchronous output operation, and individual pins can be set. 8-bit timers that have synchronous output operation are timer 1 and timer 5.

Table 6-7-1 Synchronous Output Port (Timer 1, Timer 5)

	Timer 1	Timer 5
Synchronous output port	Port 6	Port 6

■Count Timing of Synchronous Output (Timer 1, Timer 5)

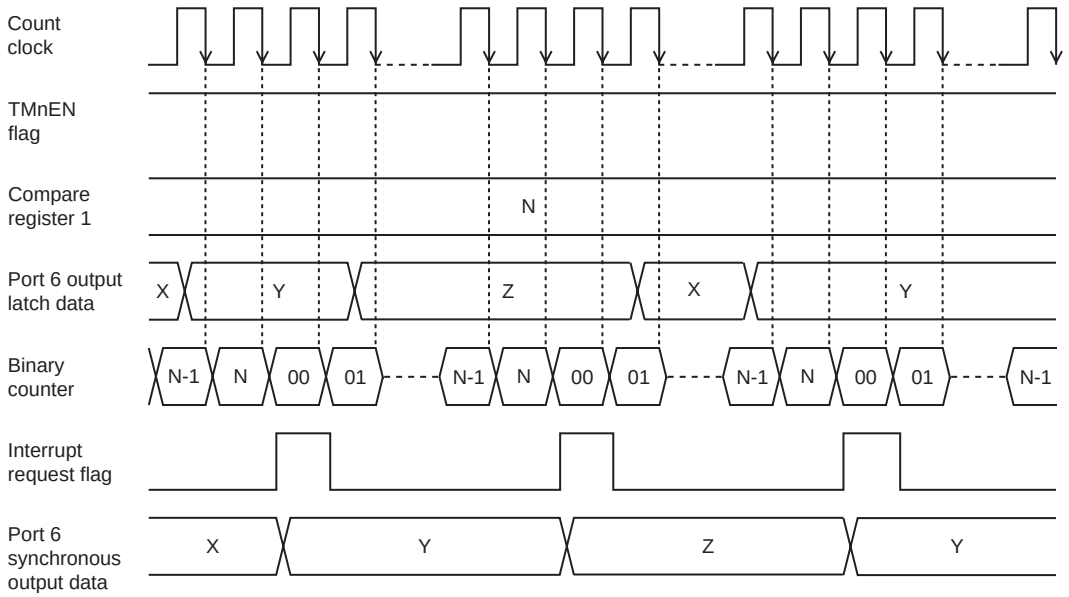


Figure 6-7-1 Count Timing of Synchronous Output (Timer 1, Timer5)

The port 6 latched data is output from the output pin in synchronization with the interrupt request generation by the match of binary counter and compare register.

6-7-2 Setup Example

■Synchronous Output Setup Example (Timer 1, Timer 5)

Setup example that latch data of port 6 is output constantly (100 µs) by using timer 1 from the synchronous output pin is shown below. The clock source of timer 1 is selected fs/8 (at fosc=8 MHz).

An example setup procedure, with a description of each step is shown below.

Setup Procedure	Description
(1) Start the counter. TM1MD (x'3F55') bp3 :TM1EN = 0	(1) Set the TM1EN flag of the timer 1 mode register (TM1MD) to "0" to stop the timer 1 counting.
(2) Select the synchronous output event. FLOAT (x'3F2E') bp1-0 :SYOEVS1-0 = 11	(2) Set the SYOEVS1-0 flag of the pin control register (FLOAT) to "11" to set the synchronous output event to timer 1 interrupt.
(3) Set the synchronous output pin. P6SYO (x'3F1E') = x'FF' P6DIR (x'3F36') = x'FF'	(3) Set the port 6 synchronous output control register (P6SYO) to x'FF' to set the synchronous output pin. (P67 to P60 are synchronous output pin.) Set the port 6 direction control register (P6DIR) to x'FF' to set port 6 to output mode. If it needs, pull up resistor should be added. [☞ Chapter 4. I/O Ports]
(4) Select the normal timer operation. TM1MD (x'3F55') bp4 :TM1CAS = 0	(4) Set the TM1CAS flag of the TM1MD register to "0" to select the normal timer operation.
(5) Select the count clock source. TM1MD (x'3F55') bp2-0 :TM1CK2-0 = 001	(5) Select the prescaler output for clock source by TM1CK2-0 flag of the TM1MD register.
(6) Select the prescaler output and enable counting. CK1MD (x'3F57') bp2-1 :TM1PSC1-0 = 01 bp0 :TM1BAS = 1 PSCMD (x'3F6F') bp0 :PSCEN = 1	(6) Select fs/8 for the prescaler output by TM1BAS flag, TM1PSC1-0 of the timer 1 prescaler selection register (CK1MD). Also, set the PSCEN flag of the prescaler control register (PSCMD) to "1" to enable the prescaler counting.

Setup Procedure	Description
(7) Set the synchronous output event generation cycle. TM1OC(x'3F53') = x'63'	(7) Set the synchronous output generation cycle to the timer 1 compare register (TM1OC). The setting value is set to 100-1=99(x'63'), because 1 MHz is divided by 10 kHz. At that time, the timer 1 binary counter (TM1BC) is initialized to x'00'.
(8) Start the timer operation. TM1MD(x'3F55') bp3 :TM1EN = 1	(8) Set the TM1EN flag of the TM1MD register to "1" to start timer 1.

TM1BC counts up from x'00'. If any data is written to the port 6 output register (P6OUT), the data of port 6 is output from the synchronous output pin in every time an interrupt request is generated by the match of TM1BC and the set value of the TM1OC register.

6-8 Serial Interface Transfer Clock Output

6-8-1 Operation

Serial interface transfer clock can be created by using the timer output signal.

■Serial InterfaceTransfer Clock Operation by 8-bit Timer (Timers 4 and 5)
Timer 4 output can be used as a transfer clock source for serial interface 1. Timer 5 output can be used as a transfer clock source for serial interface 0.

Table 6-8-1 Timer for Serial Interface Transfer Clock

Serial transfer clock	Timer 4	Timer 5
Serial interface 0	-	√
Serial interface 1	√	-
Serial interface 3	-	√

■Timing of Serial Interface Transfer Clock (Timers 4 and 5)

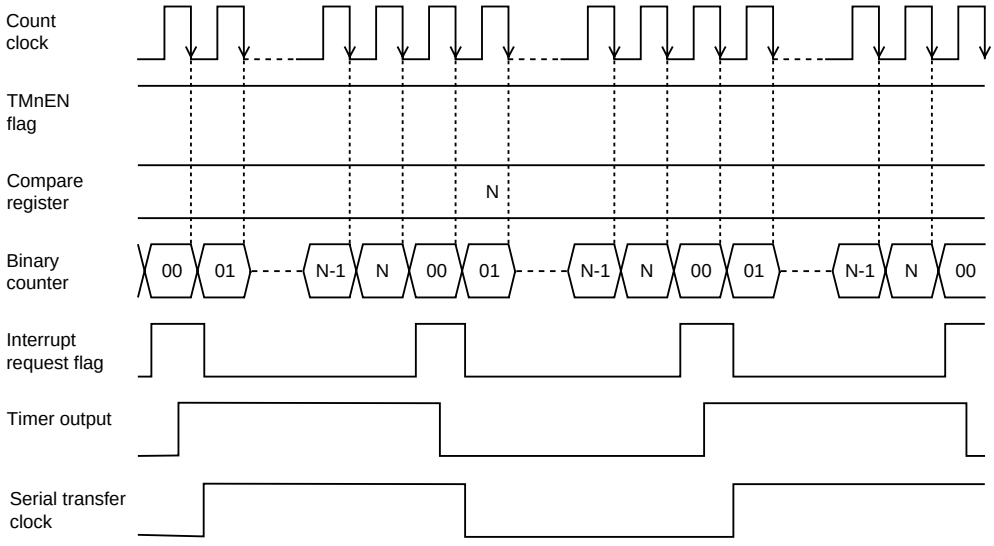


Figure 6-8-1 Timing of Serial Interface Transfer Clock (Timers 4 and 5)

The timer output is synchronized to the serial transfer clock by the timer count clock, and its frequency is 1/2 of the set frequency by the compare register.
Other count timings are same to the timing of timer operation. For the baud rate calculation and the serial interface setup, refer to chapter 11. Serial Interface 0 and 1.

6-8-2 Setup Example

■Serial Interface Transfer Clock Setup Example (Timer 4)

How to create a transfer clock for half duplex UART (Serial interface 1) using with timer 4 is shown below. The baud rate is selected to be 300 bps, the source clock of timer 4 is selected to be fs/4 (at fosc=8 MHz).

An example setup procedure, with a description of each step is shown below.

Setup Procedure	Description
(1) Stop the counter. TM4MD (x'3F64') bp3 :TM4EN = 0	(1) Set the TM4EN flag of the timer 4 mode register (TM4MD) to "0" to stop timer 4 counting.
(2) Select the normal timer operation. TM4MD (x'3F64') bp4 :TM4PWM = 0 bp5 :TM4MOD = 0	(2) Set the TM4PWM flag and TM4MOD flag of the TM4MD register to "0" to select the normal timer operation.
(3) Select the count clock source. TM4MD (x'3F64') bp2-0 :TM4CK2-0 = 001	(3) Select the clock source to prescaler output by the TM4CK2-0 flag of the TM4MD register.
(4) Select the prescaler output and enable counting. CK4MD (x'3F66') bp2-1 :TM4PSC1-0 = 01 bp0 :TM4BAS = 1 PSCMD (x'3F6F') bp0 :PSCEN = 1	(4) Select the prescaler output to fs/4 by the TM4PSC1-0, TM4BAS flag of the timer 4 prescaler selection register (CK4MD). Also, set the PSCEN flag of the prescaler control register (PSCMD) to "1" to enable the prescaler counting.
(5) Set the baud rate. TM4OC (x'3F62') = x'CF'	(5) Set the timer 4 compare register (TM4OC) to the value that baud rate comes to 300 bps. [☞ Chapter 12. Table 12-3-19] At that time, the timer 4 binary counter (TM4BC) is initialized to x'00'.
(6) Start the timer operation TM4MD (x'3F64') bp3 :TM4EN = 1	(6) Set the TM4EN flag of the TM4MD register to "1" to start timer 4.

TM4BC counts up from x'00'. Timer 4 output is the clock of the serial interface 1 at transmission and reception.

For the compare register setup value and the serial operation setup, refer to chapter 11. Serial Interface 0,1.

6-9 Simple Pulse Width Measurement

6-9-1 Operation

Timer measures the "L" duration of the pulse signal input from the external interrupt pin.

■Simple Pulse Width Measurement Operation by 8-bit Timer (Timers 0, 4 and 5)
During the input signal of the external interrupt pin (simple pulse width) is "L", the binary counter of the timer counts up. Pulse width "L" period can be measured by reading the count of timer. 8-bit timers that have the simple pulse width measurement function are timers 0, 4 and 5.

Table 6-9-1 Simple Pulse Width Measurement Able Pins (Timers 0, 4 and 5)

	Timer 0	Timer 4	Timer 5
Simple pulse width measurement enable pin	External interrupt 2 (P22/IRQ2)	External interrupt 4 (P24/IRQ4)	External interrupt 5 (P23/IRQ3)

■Count Timing of Simple Pulse Width Measurement (Timer 0, Timer 4, Timer 5)

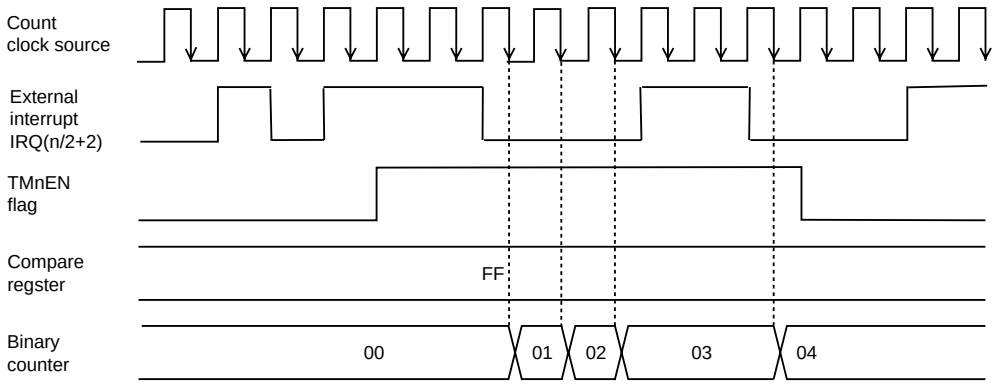


Figure 6-9-1 Count Timing at Measurement of Simple Pulse Width (Timer 0, Timer 4, Timer 5))

During the input signal of the external interrupt pin for simple pulse width measurement is "L" at TMnEN flag operation ("1"), timer counts up.

6-9-2 Setup Example

■Set up Example of Simple Pulse Width Measurement by 8-bit Timer (Timers 0, 4 and 5)
The pulse width of 'L" period of the external interrupt 2 (IRQ2) input signal is measured by timer 0. The clock source of timer 0 is selected to fosc.
An example setup procedure, with a description of each step is shown below.

Setup Procedure	Description
(1) Stop the counter. TM0MD (x'3F54') bp3 :TM0EN = 0	(1) Set the TM0EN flag of the timer 0 mode register (TM0MD) to stop timer 0 counting.
(2) Set the pulse width measurement operation. TM0MD (x'3F54') bp4 :TM0PWM = 0 bp5 :TM0MOD = 1	(2) Set the TM0PWM flag of the TM0MD register to "0" and TM0MOD flag to "1" to enable the timer operation during "L" period to be measured.
(3) Select the count clock source. TM0MD (x'3F54') bp2-0 : TM0CK2-0 = 000	(3) Set the clock source to fosc by the TM0CK2-0 flag of the TM0MD register.
(4) Set the compare register. TM0OC (X'3F52') = x'FF'	(4) Set the timer 0 compare register (TM0OC) to the bigger value than ("L"period of measured pulse width / the cycle of fosc). At that time, the timer 0 binary counter (TM0BC) is initialized to x'00'.
(5) Set the interrupt level IRQ2ICR (x'3FE4') bp7-6 :IRQ2LV1-0 = 10	(5) Set the interrupt level by the IRQ2LV1-0 flag of the external interrupt 2 control register (IRQ2ICR). If interrupt request flag is already set, clear all interrupt request flags. [☞ Chapter 3. 3-1-4 Interrupt Flag Setup]
(6) Set the interrupt valid edge. IRQ2ICR (x'3FE4') bp5 :REDG2 = 1	(6) Set the REDG2 flag of the IRQ2ICR register to "1" to specify the interrupt valid edge to the rising edge.

Setup Procedure	Description
(7) Enable the interrupt. IRQ2ICR (x'3FE4') bp1 :IRQ2IE = 1	(7) Set the IRQ2IE flag of the IRQ2ICR register to "1" to enable the interrupt.
(8) Enable the timer operation. TM0MD (x'3F54') bp3 :TM0EN = 1	(8) Set the TM0EN flag of the TM0MD register to "1" to enable timer 0 operation.

TM0BC starts to count up with negative edge of the external interrupt 2 (IRQ2) input as a trigger. Timer 0 continues to count up during "L" period of IRQ2 input, then stop the counting with positive edge of IRQ2 input as a trigger. At the same time, reading the value of TM0BC by interrupt handling can detects "L" period.

6-10 Cascade Connection

6-10-1 Operation

Cascading timers 0 and 1 form a 16-bit timer.

■8-bit Timer Cascade Connection Operation (Timer 0 + Timer 1)
Timer 0 and timer 1 are combined to be a 16-bit timer. Cascading timer is operated at clock source of timer 0 which is lower 8 bits.

Table 6-10-1 Timer Functions at Cascade Connection

	Timer 0 + Timer 1 (16 Bit)
Interrupt source	TM1IRQ
Timer operation	√
Event count	√ (TM0IO input)
Timer pulse output	√ (TM1IO output)
PWM output	-
Synchronous output	√
Serial Interface transfer clock output	-
Pulse width measurement	√
Remote control carrier output	-
Clock source	fosc fosc/4 fosc/16 fosc/32 fosc/64 fs/2 fs/4 fx TM0IO input
fosc : Machine clock (High speed oscillation) fx : Machine clock (Low speed oscillation) fs : System clock [☞ Chapter 2 2-5 Clock Switching]	

At cascade connection, the binary counter and the compare register are operated as a 16 bit register. At operation, set the TMnEN flag of the upper and lower 8-bit timers to "1" to be operated.
Also, the clock source is the one which is selected in the lower 8-bit timer.
Other setup and count timing is the same to the 8-bit timer at independently operation.

When timer 0 and timer 1 are used in cascade connection, timer 1 interrupt request flag is used. Timer pulse output of timer 0 is "L" fixed output.
An interrupt request of timer 0 is not generated, and the timer 0 interrupt should be disabled.

At the cascade connection, if the binary counter should be cleared by rewriting the compare register, the TMnEN flags of the lower and upper 8 bits timers mode registers should be set to "0" to stop the counting, then rewrite the compare register.

6-10-2 Setup Example

■Cascade Connection Timer Setup Example (Timer 0 + Timer 1)

Setting example of timer function that an interrupt is constantly generated by cascade connection of timer 0 and timer 1, as a 16-bit timer is shown. An interrupt is generated in every 2500 cycles (1 ms) by selecting source clock to fs/4 (fosc=20 MHz at operation).

An example setup procedure, with a description of each step is shown below.

Setup Procedure	Description
(1) Stop the counter. TM0MD (x'3F54') bp3 :TM0EN = 0 TM1MD (x'3F55') bp3 :TM1EN = 0	(1) Set the TM0EN flag of the timer 0 mode register (TM0MD) to "0", the TM1EN flag of the timer 1 mode register to "0" to stop timer 0 and timer 1 counting.
(2) Select the normal operation lower timer. TM0MD (x'3F54') bp4 :TM0PWM = 0 bp5 :TM0MOD = 0	(2) Set both of the TM0PWM flag and TM0MOD flag of the TM0MD register to "0" to select the normal operation of timer 0.
(3) Set the cascade connection. TM1MD (x'3F55') bp4 :TM1CAS = 1	(3) Set the TM1CAS flag of the TM1MD register to "1" to connect timer 1 and timer 0 in cascade connection.
(4) Select the count clock source. TM0MD (x'3F54') bp2-0 :TM0CK2-0 = 001	(4) Set the clock source to prescaler output by the TM0CK2-0 flag of the TM0MD register.
(5) Select the prescaler output and enable counting. CK0MD (x'3F56') bp2-1 :TM0PSC1-0= 01 bp0 :TM0BAS = 1 PSCMD (x'3F6F') bp0 :PSCEN = 1	(5) Set the prescaler output to fs/4 by the TM0PSC1-0, TM0BAS flag of the timer 0 prescaler selection register (CK0MD). Also, set the PSCEN flag of the prescaler control register (PSCMD) to "1" to enable the prescaler counting.
(6) Set the interrupt generation cycle TMnOC(x'3F53', x'3F52')=x'09C3'	(6) Set the timer 1 compare register + timer 0 compare register (TM1OC + TM0OC) to the interrupt generation cycle (x'09C3' : 2500 cycles - 1). At that time, timer 1 binary counter + timer 0 binary counter (TM1BC + TM0BC) are initialized to x'0000'.

Setup Procedure	Description
(7) Disable the lower timer interrupt. TM0ICR (x'3FE9') bp1 :TM0IE = 0	(7) Set the TM0IE flag of the timer 0 interrupt control register (TM0ICR) to "0" to disable the interrupt.
(8) Set the level of the upper timer interrupt. TM1ICR (x'3FEA') bp7-6 :TM1LV1-0 = 10	(8) Set the interrupt level by the TM1LV1-0 flag of the timer 1 interrupt control register (TM1ICR). If any interrupt request flag may be already set, clear all request flags. [☞ Chapter 3 3-1-4. Interrupt Flag Setup]
(9) Enable the upper timer interrupt. TM1ICR (x'3FEA') bp1 :TM1IE = 1	(9) Set the TM1IE flag of the TM1ICR register to "1" to enable the interrupt.
(10) Start the upper timer operation. TM1MD (x'3F55') bp3 :TM1EN = 1	(10) Set the TM1EN flag of the TM1MD register to "1" to start timer 1.
(11) Start the lower timer operation. TM0MD (x'3F54') bp3 :TM0EN = 1	(11) Set the TM0EN flag of the TM0MD register to "1" to start timer 0.

TM1BC + TM0BC counts up from x'0000' as a 16-bit timer. When TM1BC + TM0BC reaches the set value of TM1OC + TM0OC register, the timer 1 interrupt request flag is set to "1" at the next count clock, and the value of TM1BC + TM0BC becomes x'0000' and counting up is restarted.

Use a 16-bit access instruction to set the (TM1OC + TM0OC) register.

Start the upper timer operation before the lower timer operation.

6-11 Remote Control Carrier Output

6-11-1 Operation

Carrier pulse for remote control can be generated.

■Operation of Remote Control Carrier Output (Timer 0, Timer 5)

Remote control carrier pulse is based on output signal of timer 0 or timer 5. Duty cycle is selected from 1/2, 1/3. RMOUT (P10/P11) outputs remote control carrier output signal.

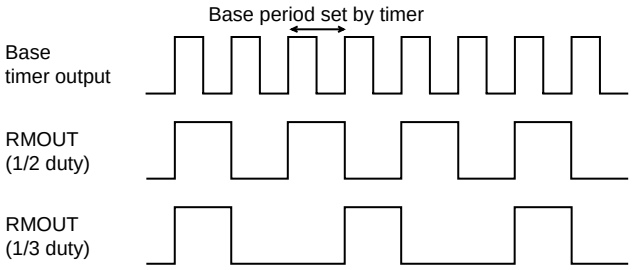


Figure 6-11-1 Duty Cycle of Remote Control Carrier Output Signal

■Count Timing of Remote Control Carrier Output (Timer 0, Timer 5)

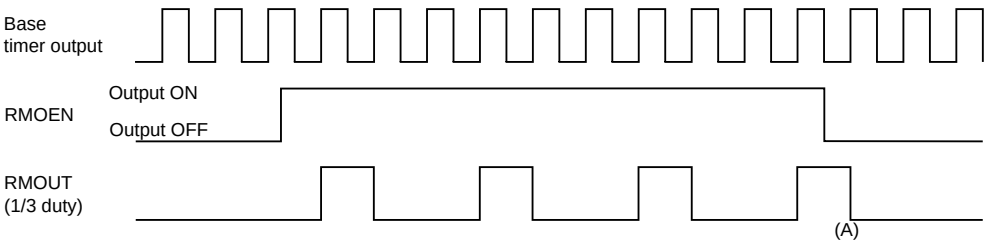


Figure 6-11-2 Count Timing of Remote Control Carrier Output Function (Timer 0, Timer 5)

(A) Even if the RMOEN flag is off when the carrier output is high, the carrier waveform is held by the synchronizing circuit.

Before the RMOEN flag is switched to on, set the P1OMD0 flag or P1OMD1 flag of the P1OMD register to "1". After it is switched to off, set it to "0".

When the RMOEN flag is changed, do not change the base cycle and its duty at the same time. If they are changed at the same time, the carrier wave form is not output properly.

6-11-2 Setup Example

■Remote Control Carrier Output Setup Example (Timer 0, Timer 5)

Here is the setting example that the RMOUT pin outputs the 1/3 duty carrier pulse signal with "H" period of 36.7 kHz, by using timer 0. The source clock of timer 0 is set to fosc (at 8 MHz).

An example setup procedure, with a description of each step is shown below.

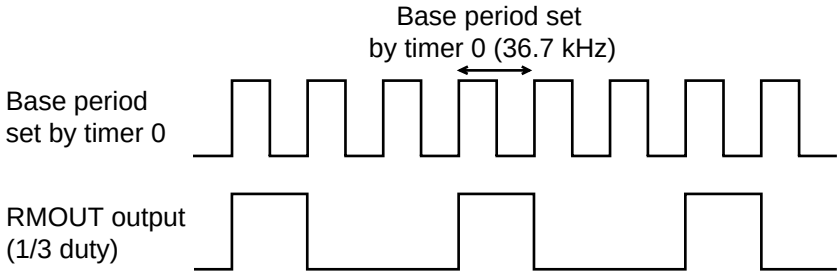


Figure 6-11-3 Output Wave Form of RMOUT Output Pin

Setup Procedure	Description
(1) Disable the remote control carrier output. RMCTR (x'3F6E') bp3 : RMOEN = 0	(1) Set the RMOEN flag of the remote control carrier output control register (RMCTR) to "0" to disable the remote control carrier output.
(2) Select the base cycle setting timer. RMCTR (x'3F6E') bp0 : RMBTMS = 0	(2) Set the RMBTMS flag of the RMCTR register to "0" to set the timer as a base cycle setting timer.
(3) Select the carrier output duty. RMCTR (x'3F6E') bp1 : RMDTY0 = 1	(3) Set the RMDTY0 flag of the RMCTR register to "1" to select 1/3 duty.
(4) Stop the counter. TM0MD (x'3F54') bp3 : TM0EN = 0	(4) Set the TM0EN flag of the timer 0 mode register (TM0MD) to stop the timer 0 counting.
(5) Set the remote control carrier output of the special function pin. P1OMD (x'3F2F') bp0 : P1OMD0 = 1 P1DIR (x'3F31') bp0 : P1DIR0 = 1 RMCTR (x'3F6E') bp4 :TM0RM = 1	(5) Set the P1OMD0 flag of the port 1 output mode register (P1OMD) to "1" to set P10 pin as a special function pin. Set the P1DIR0 flag of the port 1 direction control register (P1DIR) to "1" for output mode. Set the TM0RM flag of the RMCTR register to "1" to select the remote control carrier output.

Setup Procedure	Description
(6) Select the normal timer operation. TM0MD (x'3F54') bp4 : TM0PWM = 0 bp5 : TM0MOD = 0	(6) Set both of the TM0MOD flag and TM0PWM flag of the TM0MD register to "0" to select normal timer operation.
(7) Select the count clock source. TM0MD (x'3F54') bp2-0 : TM0CK2-0 = 000	(7) Select fosc to clock source by the TM0CK2-0 flag of the TM0MD register.
(8) Set the base cycle of remote control carrier. TM0OC (x'3F52') = x'6C'	(8) Set the base cycle of remote control carrier by writing x'6C' to the timer 0 compare register (TM0OC). The set value should be (8 MHz/ 73.4 kHz) - 1 = 108(x'6C') 8 MHz is divided to be 73.4 kHz, 2 times 36.7 kHz.
(9) Start the timer operation. TM0MD (x'3F54') bp3 : TM0EN = 1	(9) Set the TM0EN flag of the TM0MD register to "1" to stop the timer 0 counting.
(10) Enable the remote control carrier output. RMCTR (x'3F6E') bp3 : RMOEN = 1	(10) Set the RMOEN flag of the RMCTR register to "1" to enable the remote control carrier output.

TM0BC counts up from x'00'. Timer 0 outputs the base cycle pulse set in TM0OC. Then, the 1/3 duty remote control carrier pulse signal is output. If the RMOEN flag of the RMCTR register is set to "0", the remote control carrier pulse signal output is stopped.

Chapter 7 16-bit Timer

7

7-1 Overview

This LSI contains a general-purpose 16-bit timer (Timer 7). Its compare register is double buffer type. Timer 7 (high function 16-bit timer) has 2 sets of compare registers with double buffering. Also, as an independent interrupt it has a timer 7 interrupt and a timer 7 compare register 2 match interrupt.

7-1-1 Functions

Table 7-1-1 shows the functions of timer 7.

Table 7-1-1 16-bit Timer Functions

	Timer 7 (High precision 16-bit timer)
Interrupt source	TM7IRQ T7OC2IRQ
Timer operation	√
Event count	√
Timer pulse output	√
PWM output (duty is changeable)	√
High precision PWM output (duty and cycle are changeable)	√
Synchronous output	√
Capture function	√
Pulse width measurement	√
Clock source	fosc fosc/2 fosc/4 fosc/16 fs fs/2 fs/4 fs/16 TM7IO input TM7IO input/2 TM7IO input/4 TM7IO input/16
fosc : Machine clock (High speed oscillation) fs : System clock [☞ Chapter 2 2-5 Clock Switching]	

7-1-2 Block Diagram

■Timer 7 Block Diagram

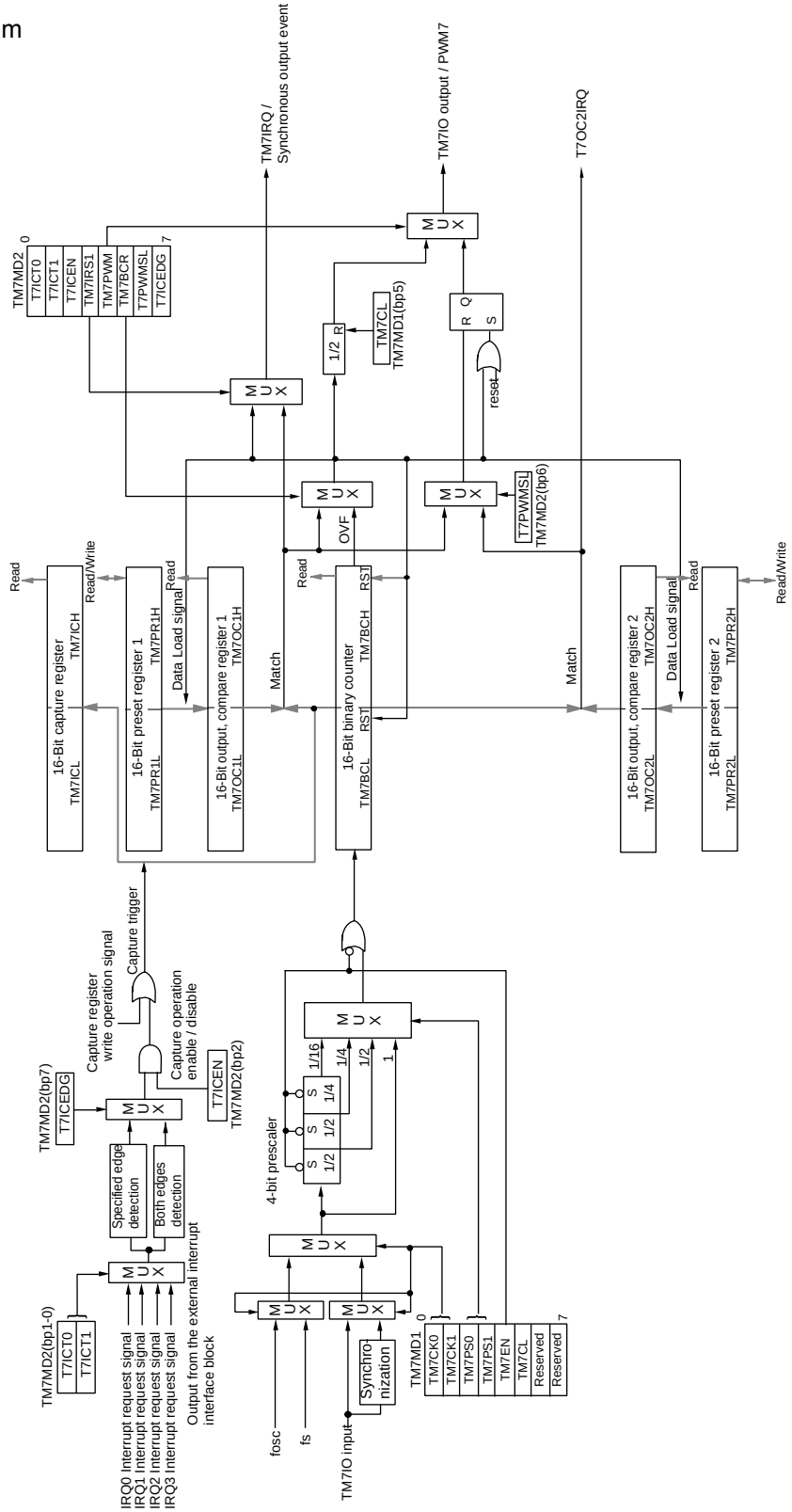


Figure 7-1-1 Timer 7 Block Diagram

7-2 Control Registers

Timer 7 contains the binary counter (TM7BC), the compare register 1 (TM7OC1), and its double buffer preset register (TM7PR1), the compare register 2 (TM7OC2) and its double buffer preset register 2 (TM7PR2), the capture register (TM7IC). The mode register 1 (TM7MD1) and the mode register 2 (TM7MD2) controls timer 7.

7-2-1 Registers

Table 7-2-1 shows the registers that control timer 7.

Table 7-2-1 16-bit Timer Control Registers

	Register	Address	R/W	Function	Page
Timer 7	TM7BCL	x'03F70'	R	Timer 7 binary counter (lower 8 bits)	VII - 7
	TM7BCH	x'03F71'	R	Timer 7 binary counter (upper 8 bits)	VII - 7
	TM7OC1L	x'03F72'	R	Timer 7 compare register 1 (lower 8 bits)	VII - 5
	TM7OC1H	x'03F73'	R	Timer 7 compare register 1 (upper 8 bits)	VII - 5
	TM7PR1L	x'03F74'	R/W	Timer 7 preset register 1 (lower 8 bits)	VII - 6
	TM7PR1H	x'03F75'	R/W	Timer 7 preset register 1 (upper 8 bits)	VII - 6
	TM7ICL	x'03F76'	R	Timer 7 capture regsiter (lower 8 bits)	VII - 7
	TM7ICH	x'03F77'	R	Timer 7 capture register (upper 8 bits)	VII - 7
	TM7MD1	x'03F78'	R/W	Timer 7 mode register 1	VII - 8
	TM7MD2	x'03F79'	R/W	Timer 7 mode register 2	VII - 9
	TM7OC2L	x'03F7A'	R	Timer 7 compare register 2 (lower 8 bits)	VII - 5
	TM7OC2H	x'03F7B'	R	Timer 7 compare register 2 (upper 8 bits)	VII - 5
	TM7PR2L	x'03F7C'	R/W	Timer 7 preset register 2 (lower 8 bits)	VII - 6
	TM7PR2H	x'03F7D'	R/W	Timer 7 preset register 2 (upper 8 bits)	VII - 6
	TM7ICR	x'03FF1'	R/W	Timer 7 interrupt control register	III - 31
	T7OC2ICR	x'03FF2'	R/W	Timer 7 compare register 2 match interrupt contro	III - 32
	P1OMD	x'03F2F'	R/W	Port 1 output mode register	IV - 14
	P1DIR	x'03F31'	R/W	Port 1 direction control register	IV - 13

R/W : Readable/Writable

R : Readable only

7-2-2 Programmable Timer Registers

Timer 7 has a 16-bit programmable timer register. It contains a compare register, a preset register, a binary counter and a capture register. Each register has 2 sets of 8-bit register. Operate by 16-bit access.

Compare register is a 16-bit register stores the value that compared to binary counter. The compared value that written to the preset register in advance is loaded.

■Timer 7 Compare Register 1 (TM7OC1)

	7	6	5	4	3	2	1	0	
TM7OC1L	TM7OC1L7	TM7OC1L6	TM7OC1L5	TM7OC1L4	TM7OC1L3	TM7OC1L2	TM7OC1L1	TM7OC1L0	(At reset : X X X X X X X X)

Figure 7-2-1 Timer 7 Compare Register 1 Lower 8 bits (TM7OC1L : x'03F72', R)

	7	6	5	4	3	2	1	0	
TM7OC1H	TM7OC1H7	TM7OC1H6	TM7OC1H5	TM7OC1H4	TM7OC1H3	TM7OC1H2	TM7OC1H1	TM7OC1H0	(At reset : X X X X X X X X)

Figure 7-2-2 Timer 7 Compare Register 1 Upper 8 bits (TM7OC1H : x'03F73', R)

■Timer 7 Compare Register 2 (TM7OC2)

	7	6	5	4	3	2	1	0	
TM7OC2L	TM7OC2L7	TM7OC2L6	TM7OC2L5	TM7OC2L4	TM7OC2L3	TM7OC2L2	TM7OC2L1	TM7OC2L0	(At reset : X X X X X X X X)

Figure 7-2-3 Timer 7 Compare Register 2 Lower 8 bits (TM7OC2L : x'03F7A', R)

	7	6	5	4	3	2	1	0	
TM7OC2H	TM7OC2H7	TM7OC2H6	TM7OC2H5	TM7OC2H4	TM7OC2H3	TM7OC2H2	TM7OC2H1	TM7OC2H0	(At reset : X X X X X X X X)

Figure 7-2-4 Timer 7 Compare Register 2 Upper 8 bits (TM7OC2H : x'03F7B', R)

The timer 7 preset register 1 and 2 are buffer registers of the timer 7 compare register 1 and 2. If the set value is written to the timer 7 preset register 1 and 2 when the counting is stopped, the same set value is loaded to the timer 7 compare register 1 and 2. If the set value is written to the timer 7 preset register 1 and 2 when the counting is operated, the set value of the timer 7 preset register 1 and 2 is loaded to the timer 7 compare register 1 and 2 at the timing that the timer 7 binary counter is cleared.

■Timer 7 Preset Register 1 (TM7PR1)

	7	6	5	4	3	2	1	0	
TM7PR1L	TM7PR1L7	TM7PR1L6	TM7PR1L5	TM7PR1L4	TM7PR1L3	TM7PR1L2	TM7PR1L1	TM7PR1L0	(At reset : X X X X X X X X)

Figure 7-2-5 Timer 7 Preset Register 1 Lower 8 bits (TM7PR1L : x'03F74', R/W)

	7	6	5	4	3	2	1	0	
TM7PR1H	TM7PR1H7	TM7PR1H6	TM7PR1H5	TM7PR1H4	TM7PR1H3	TM7PR1H2	TM7PR1H1	TM7PR1H0	(At reset : X X X X X X X X)

Figure 7-2-6 Timer 7 Preset Register 1 Upper 8 bits (TM7PR1H : x'03F75', R/W)

■Timer 7 Preset Register 2 (TM7PR2)

	7	6	5	4	3	2	1	0	
TM7PR2L	TM7PR2L7	TM7PR2L6	TM7PR2L5	TM7PR2L4	TM7PR2L3	TM7PR2L2	TM7PR2L1	TM7PR2L0	(At reset : X X X X X X X X)

Figure 7-2-7 Timer 7 Preset Register 2 Lower 8 bits (TM7PR2L : x'03F7C', R/W)

	7	6	5	4	3	2	1	0	
TM7PR2H	TM7PR2H7	TM7PR2H6	TM7PR2H5	TM7PR2H4	TM7PR2H3	TM7PR2H2	TM7PR2H1	TM7PR2H0	(At reset : X X X X X X X X)

Figure 7-2-8 Timer 7 Preset Register 2 Upper 8 bits (TM7PR2H : x'03F7D', R/W)

When data load timing from 16-bit timer preset register to compare register matches to write timing to preset register with instruction, correct value may not be loaded to the compare register. Therefore, write to preset register should be done while timer is stopped or within timer interrupt processing.
And use MOVW instruction for write to preset register.

Binary counter is a 16-bit up counter. If any data is written to a preset register when the counting is stopped, the binary counter is cleared to x'0000'.

■Timer 7 Binary Counter (TM7BC)

	7	6	5	4	3	2	1	0	
TM7BCL	TM7BCL7	TM7BCL6	TM7BCL5	TM7BCL4	TM7BCL3	TM7BCL2	TM7BCL1	TM7BCL0	(At reset : X X X X X X X X)

Figure 7-2-9 Timer 7 Binary Counter Lower 8 bits (TM7BCL : x'03F70', R)

	7	6	5	4	3	2	1	0	
TM7BCH	TM7BCH7	TM7BCH6	TM7BCH5	TM7BCH4	TM7BCH3	TM7BCH2	TM7BCH1	TM7BCH0	(At reset : X X X X X X X X)

Figure 7-2-10 Timer 7 Binary Counter Upper 8 bits (TM7BCH : x'03F71', R)

Input capture register is a register that holds the value loaded from a binary counter by capture trigger. Capture trigger is generated by an input signal from an external interrupt pin, and when an arbitrary value is written to an input capture register (Directly writing to the register by program is disable.).

■Timer 7 Input Capture Register (TM7IC)

	7	6	5	4	3	2	1	0	
TM7ICL	TM7ICL7	TM7ICL6	TM7ICL5	TM7ICL4	TM7ICL3	TM7ICL2	TM7ICL1	TM7ICL0	(At reset : X X X X X X X X)

Figure 7-2-11 Timer 7 Input Capture Register Lower 8 bits (TM7ICL : x'03F76', R)

	7	6	5	4	3	2	1	0	
TM7ICH	TM7ICH7	TM7ICH6	TM7ICH5	TM7ICH4	TM7ICH3	TM7ICH2	TM7ICH1	TM7ICH0	(At reset : X X X X X X X X)

Figure 7-2-12 Timer 7 Input Capture Register Upper 8 bits (TM7ICH : x'03F77', R)

7-2-3 Timer Mode Registers

This is a readable / writable register that controls timer 7.

■Timer 7 Mode Register 1 (TM7MD1)

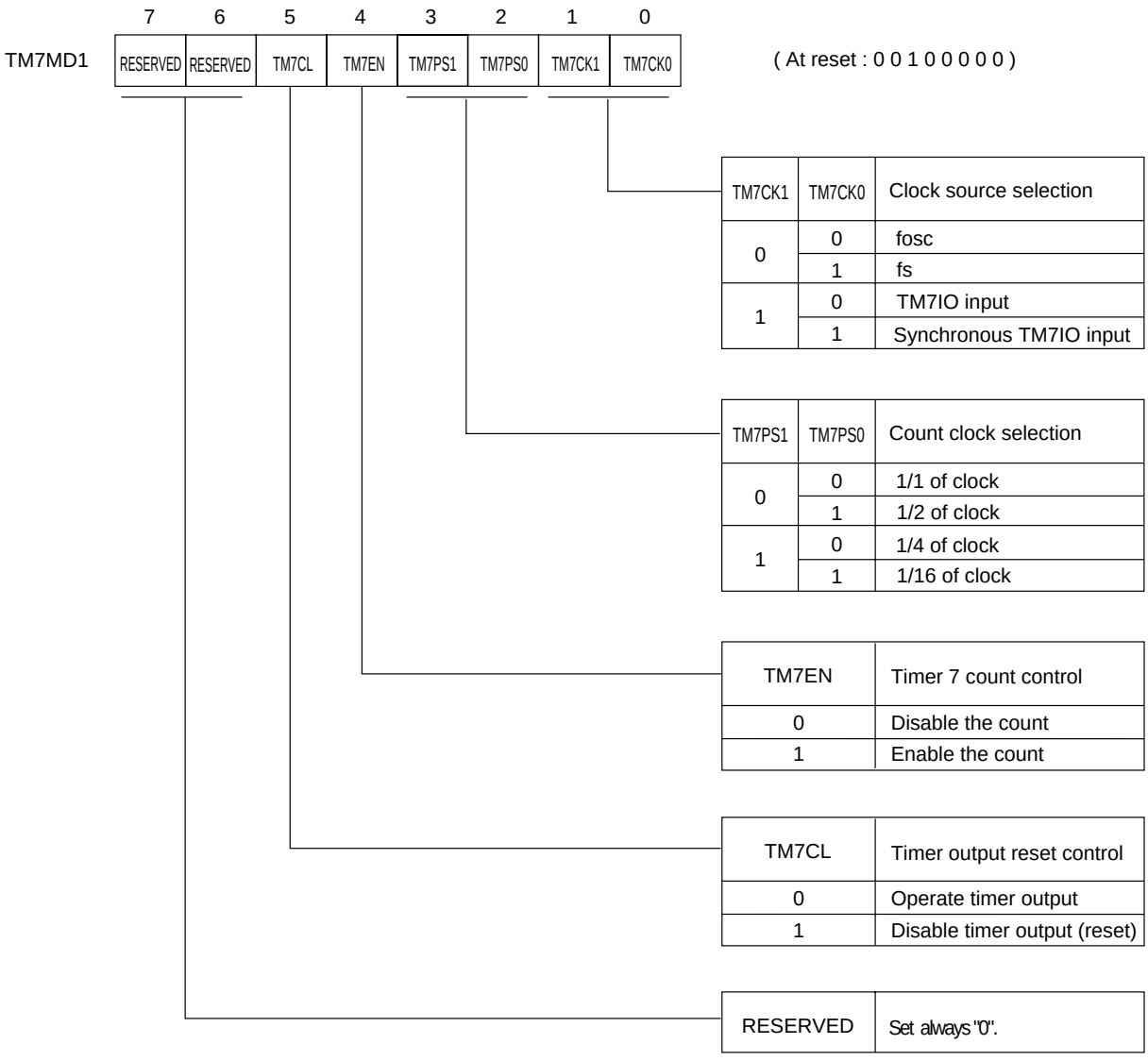
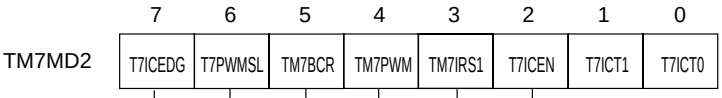


Figure 7-2-13 Timer 7 Mode Register 1 (TM7MD1 : x'03F78', R/W)

■Timer 7 Mode Register 2 (TM7MD2)



T7ICT1	T7ICT0	Capture trigger selection
0	0	IRQ0 (External interrupt 0)
	1	IRQ1 (External interrupt 1)
1	0	IRQ2 (External interrupt 2)
	1	IRQ3 (External interrupt 3)

T7ICEN	Input capture operation enable flag
0	Disable capture operation
1	Enable capture operation

TM7IRS1	Timer 7 interrupt source selection
0	Counter clear
1	Match of BC and OC1

TM7PWM	Timer output waveform selection
0	Timer output
1	PWM output

TM7BCR	Timer 7 counter clear source selection
0	Full count OVF
1	Match of BC and OC1

T7PWMSL	PWM mode selection
0	Set duty by OC1
1	Set duty by OC2

T7ICEDG	Capture trigger edge selection
0	Both edges selection
1	Specified edge selection

Figure 7-2-14 Timer 7 Mode Register 2 (TM7MD2 : x'03F79', R/W)

7-3 16-bit Timer Count

7-3-1 Operation

The timer operation can constantly generate interrupts.

■16-bit Timer Operation (Timer 7)
The generation cycle of an timer interrupt is set by the clock source selection and the set value of the compare register 1 (TM7OC1), in advance. When the binary counter (TM7BC) reaches the set value of the compare register 1, the timer 7 interrupt request is generated at the next count clock. There are 2 sources ; the TM7OC1 compare match or the full count over flow, to be selected to clear the binary counter. After the binary counter is cleared to x'0000, the counting up is restarted from x'0000'.

Table 7-3-1 16-bit Timer Interrupt Source and Binary Counter Clear Source (Timer 7)

TM7MD2 register		Interrupt source	Binary counter clear source
TM7IRS1 flag	TM7BCR flag		
1	1	TM7OC1 compare match	TM7OC1 compare match
0	1	TM7OC1 compare match	TM7OC1 compare match
1	0	TM7OC1 compare match	full count over flow
0	0	full count over flow	full count over flow

Timer 7 can generate another set of an independent interrupt (Timer 7 compare register 2 match interrupt) by the set value of the timer 7 compare register (TM7OC2). At that timer, the binary counter is cleared as the above setup.

The compare register is double buffer type. So, when the value of the preset register is changed during the counting, the changed value is stored to the compare register as the binary counter is cleared. This function can change its value of the compare register constantly, without disturbing the cycle during timer operation (Reload function).

When the CPU reads the 16-bit binary counter (TM7BC), the read data is treated as 8-bits unit data even if it is a 16-bit MOVW instruction. As a result, it will read the data incorrectly if a carry from the lower 8 bits to the upper 8 bits occurs during counting.

To read the correct value of the 16-bit counting (TM7BC), use the writing program function to the input capture register (TM7IC). By writing to the TM7IC, the counting data of TM7BC can be stored to TM7IC to read out the correct counting data during operation.

[☞ Chapter 7-9-1. Operation (p.VII-34)]

Table 7-3-2 shows the clock source that can be selected.

Table 7-3-2 Clock Source at Timer Operation(Timer 7)

Clock source	1 count time
fosc	50 ns
fosc/2	100 ns
fosc/4	200 ns
fosc/16	800 ns
fs	100 ns
fs/2	200 ns
fs/4	400 ns
fs/16	1.6 μs
Notes : as fosc = 20 MHz fx = 32.768 kHz fs = fosc/2 = 10 MHz	

■Count Timing of Timer Operation (Timer 7)

The binary counter counts up with the selected clock source as the count clock.

The basic operation of the whole function of 16-bit timer is as follows ;

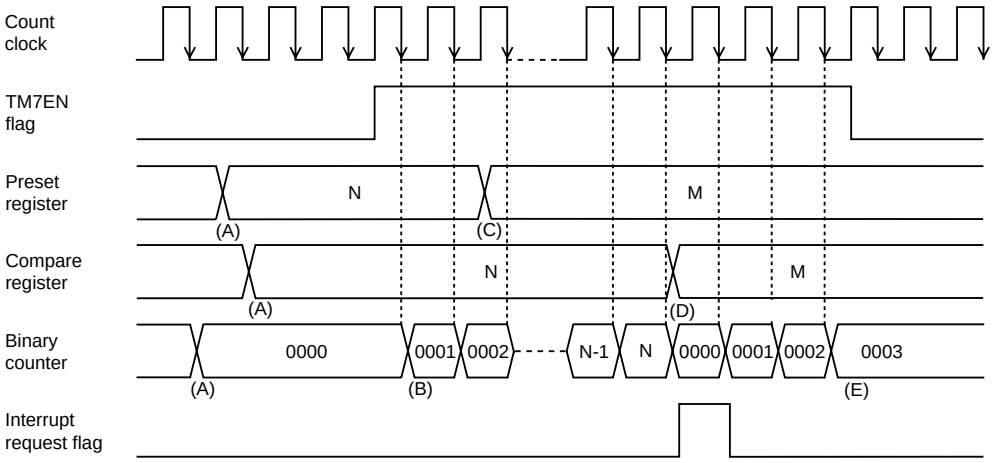


Figure 7-3-1 Count Timing of Timer Operation (Timer 7)

(A) When any data is written to the preset register as the TM7EN flag is stopped ("0"), the same value is loaded at the writing cycle and the binary counter is cleared to x'0000'.

(B) If the TM7EN flag is "1", the binary counter starts counting. The counting is happened at the falling edge of the count clock.

(C) Even if the preset register is rewritten as the TM7EN flag is "1", the binary counter is not changed.

(D) If the binary counter reaches the value of the compare register 1, the set value of the preset register is loaded to the compare register at the next count clock. And the interrupt request flag is set at the next count clock, and the binary counter is cleared to x'0000' to restart counting up.

(E) If the TM7EN flag is"0", the binary counter is stopped.

When the binary counter reaches the value of the compare register, the interrupt request flag is set and the binary counter is cleared, at the next count clock. So, set the compare register as; (the set value of the compare register) = (count till the interrupt request - 1)

When the timer 7 compare register 2 match interrupt is generated and the TM7OC1 compare match is selected as a binary counter clear source, the set value of the compare register 2 should be smaller than the set value of the compare register 1.

If the interrupt is enabled, the timer interrupt request flag should be cleared before timer operation is started.

At TM7OC=x'0000', x'0001', the timer n interrupt request generation has the same waveform.

7-3-2 Setup Example

■Timer Operation Setup Example (Timer 7)
Timer 7 generates an interrupt constantly for timer function. Fosc/2 (fosc=20 MHz) is selected as a clock source to generate an interrupt every 1000 cycles (100 µs).
An example setup procedure, with a description of each step is shown below.

Setup Procedure	Description
(1) Stop the counter. TM7MD1 (x'3F78') bp4 : TM7EN = 0	(1) Set the TM7EN flag of the timer 7 mode register 1 (TM7MD1) to "0" to stop timer 7 counting.
(2) Select the timer clear source. TM7MD2 (x'3F79') bp5 : TM7BCR = 1	(2) Set the TM7BCR flag of the timer 7 mode register 2 (TM7MD2) to "1" to select the compare match as a binary counter clear source.
(3) Select the count clock source. TM7MD1 (x'3F78') bp1-0 : TM7CK1-0 = 00 bp3-2 : TM7PS1-0 = 01	(3) Select fosc as a clock source by the TM7CK1-0 flag of the TM7MD1 register. Also select 1/2 fosc as a count clock source by TM7PS1-0 flag.
(4) Set the interrupt generation cycle. TM7PR1 (x'3F75', x'3F74')=x'03E7	(4) Set the interrupt generation cycle to the timer 7 preset register 1 (TM7PR1). The cycle is 1000. The set value should be 1000-1=999(x'03E7'). At that time, the same value is loaded to the timer 7 compare register 1 (TM7OC1), and the timer 7 binary counter (TM7BC) is initialized to x'0000'.
(5) Set the interrupt level. TM7ICR (x'3FF1') bp7-6 : TM7LV1-0 = 10	(5) Set the interrupt level by the TM7LV1-0 flag of the timer 7 interrupt control register (TM7ICR). If the interrupt request flag may be already set, clear the request flag. [☞ Chapter 3 3-1-4. Interrupt Flag Setup]
(6) Enable the interrupt. TM7ICR (x'3FF1') bp1 : TM7IE = 1	(6) Set the TM7IE flag of the TM7ICR register to "1" to enable the interrupt.

Setup Procedure	Description
(7) Start the timer operation. TM7MD1 (x'3F78') bp4 : TM7EN = 1	(7) Set the TM7EN flag of the TM7MD1 register to "1" to start timer 7.

TM7BC counts up from x'0000'. When TM7BC reaches the set value of the TM7OC1 register, the timer 7 interrupt request flag is set to "1" at the next count clock and the TM7BC becomes x'0000' and counts up, again.

When the TM7EN flag of the TM7MD register is changed at the same time to other bits, the binary counter may count up by the switching operation.

Write to preset register should be done while timer is stopped or within timer interrupt processing.
And use MOVW instruction for write to preset register.

7-4 16-bit Event Count

7-4-1 Operation

Event count operation has 2 types ; TM7IO input and synchronous TM7IO input can be selected as the count clock. Each type can select 1/1, 1/2, 1/4 or 1/6 as a count clock source.

■16-bit Event Count Operation (Timer 7)
Event count means that the binary counter (TM7BC) counts the input signal from external to the TM7IO pin. If the value of the binary counter reaches the setting value of the compare register (TM7OC), interrupts can be generated at the next count clock.

Table 7-4-1 Event Count Input Clock

	Timer 7
Event input	TM7IO input (P14)
	Synchronous TM7IO input

As an actual count clock, a signal divided 1, 2, 4, or 16 is selected.

■Count Timing of TM7IO Input (Timer 7)
When TM7IO input is selected, TM7IO input signal is directly input to the count clock of the timer 7. The binary counter counts up at the falling edge of the TM7IO input signal or at the falling edge of the TM7IO input signal that passed the divider.

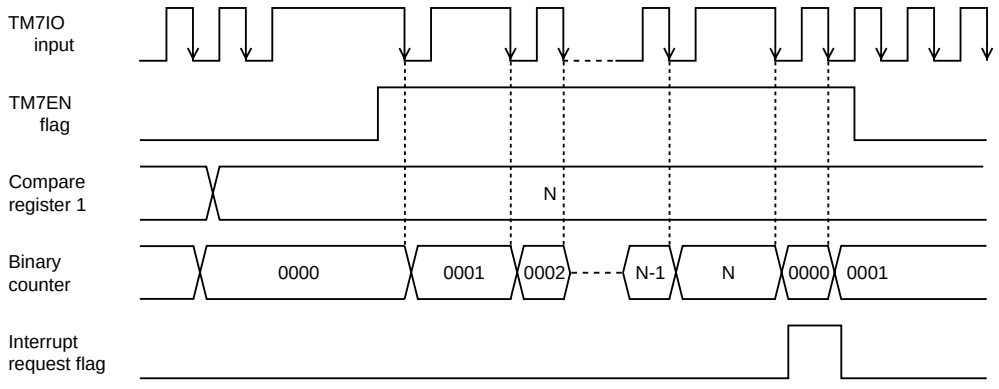


Figure 7-4-1 Count Timing TM7IO Input (Timer 7)

If the binary counter is read out at operation, incorrect data at counting up may be read. To prevent this, use the event count by the synchronous TM7IO input as the following page.

■Count Timing of Synchronous TM7IO Input (Timer 7)

If the synchronous TM7IO input is selected, the synchronizing circuit output signal is input to the count clock. The synchronizing circuit output signal is changed at the falling edge of the system clock after the TM7IO input signal is changed. The binary counter counts up at the falling edge of the synchronizing circuit output signal or the synchronizing circuit output signal that passed through the divide-by circuit.

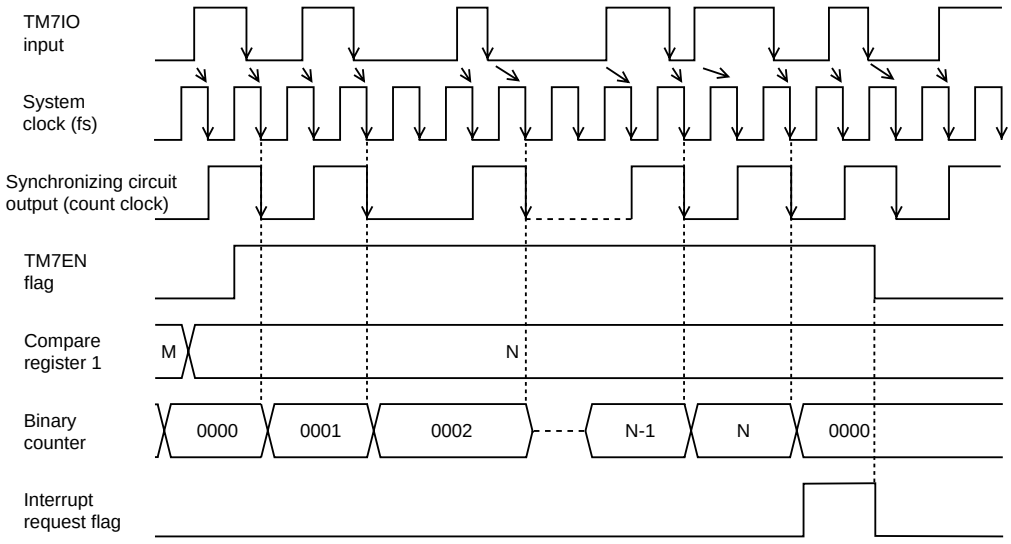


Figure 7-4-2 Count Timing of Synchronous TM7IO Input (Timer 7)

When the synchronous TM7IO input is selected as the count clok source, the timer 7 counter counts up in synchronization with the system clock. Therefore, the correct value is always read. But, if the synchronous TM7IO is selected as the count clock source, CPU mode cannot return from STOP/HALT mode.

7-4-2 Setup Example

■Event Count Setup Example (Timer 7)

If the falling edge of the TM7IO input pin signal is detected 5 times with using timer 7, an interrupt is generated. An example setup procedure, with a description of each step is shown below.

Setup Procedure	Description
(1) Stop the counter. TM7MD1 (x'3F78') bp4 : TM7EN = 0	(1) Set the TM7EN flag of the timer 7 mode register 1 (TM7MD1) to "0" to stop timer 7 counting.
(2) Set the special function pin to input mode. P1DIR (x'3F31') bp4 : P1DIR4 = 0	(2) Set the P1DIR4 flag of the port 1 direction control register (P1DIR) to "0" to set P14 pin to input mode. If it needs, pull-up resistor should be added. [☞ Chapter 4 I/O Ports]
(3) Select the condition for timer clear. TM7MD2 (x'3F79') bp5 : TM7BCR = 1	(3) Set the TM7BCR flag of the timer 7 mode register 2 (TM7MD2) to "1" to select the compare match as a clear source of binary counter.
(4) Select the count clock source. TM7MD1 (x'3F78') bp1-0 : TM7CK1-0 = 10 bp3-2 : TM7PS1-0 = 00	(4) Select the TM7IO input as a clock source by the TM7CK1-0 flag of the TM7MD1 register. Also, select 1/1(no division) as a count clock source by the TM7PS1-0 flag.
(5) Set the interrupt generation cycle. TM7PR1 (x'3F75', x'3F74')=x'0004'	(5) Set the interrupt generation cycle to the timer 7 preset register 1 (TM7PR1). The set value should be 4, because the counting is 5 times. At that time, the same value is loaded to the timer 7 compare register 1 (TM7OC1), and the timer 7 binary counter (TM7BC) is initialized to x'0000'.

Setup Procedure	Description
(6) Set the interrupt level. TM7ICR (x'3FF1') bp7-6 :TM7LV1-0 = 10	(6) Set the interrupt level by the TM7LV1-0 flag of the timer 7 interrupt control register (TM7ICR). If any interrupt request flag may be already set, clear those request flags. [☞ Chapter 3 3-1-4. Interrupt Flag Setup]
(7) Enable the interrupt. TM7ICR (x'3FF1') bp1 : TM7IE = 1	(7) Set the TM7IE flag of the TM7ICR register to "1" to enable interrupt.
(8) Start the event count. TM7MD1 (x'3F78') bp4 : TM7EN = 1	(8) Set the TM7EN flag of the TM7MD 1 register to "1" to start timer 7.

Every time TM7BC detects the falling edge of the TM7IO input, TM7BC counts up from x'0000'. When the TM7BC reaches the setting value of the TM7OC1 register, the timer 7 interrupt request flag is set at the next count clock, then the value of TM7BC becomes x'0000' and counting up is restarted.

7-5 16-bit Timer Pulse Output

7-5-1 Operation

TM7IO pin can output a pulse signal with an arbitrary frequency.

■16-bit Timer Pulse Output Operation (Timer 7)
The timers can output 2 x cycle signal, compared to the setting value to the compare register 1 (TM7OC1) or 1/2 the frequency of the 16-bit full count.
Output pin are as follows.

Table 7-5-1 Timer Pulse Output Pin

	Timer 7
Pulse output pin	TM7IO output (P14)

Table 7-5-2 shows the timer interrupt generation sources and the flags that control the timer pulse output cycle.

Table 7-5-2 16-bit Timer Interrupt Generation Source and Timer Pulse Output Cycle (Timer 7)

TM7MD2 register		Interrupt source	Timer pulse output cycle
TM7IRS1 flag	TM7BCR flag		
1	1	TM7OC1 compare match	set value of TM7OC1 x 2
0	1	TM7OC1 compare match	set value of TM7OC1 x 2
1	0	TM7OC1 compare match	full count of TM7BC x 2
0	0	full count over flow	full count of TM7BC x 2

■Count Timing of Timer Pulse Output (Timer 7)

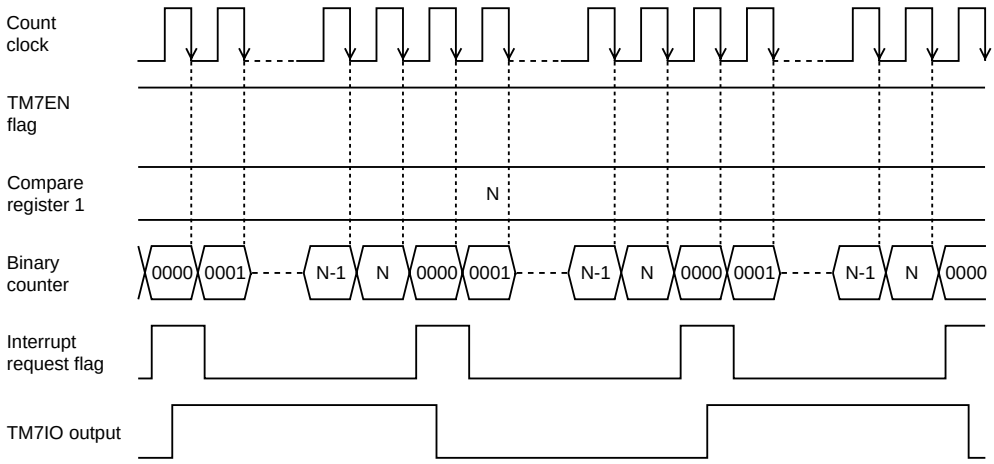


Figure 7-5-1 Count Timing of Timer Pulse Output (Timer 7)

The TM7IO pin outputs 2 x cycle, compared to the value in the compare register 1. If the binary counter reaches the compare register, and the binary counter is cleared to x'0000' or the full count overflow, the TM7IO output (timer output) is inverted. The inversion of the timer output is changed at the rising edge of the count clock. This is happened to form the waveform inside to correct the output cycle.

In the initial state after releasing reset, the timer pulse output is reset, and low output is fixed. Therefore, release the reset of the timer pulse output by setting the TM7CL flag of the TM7MD1 register to "0".

7-5-2 Setup Example

■Timer Pulse Output Setup Example (Timer 7)
TM7IO pin outputs 50 kHz pulse by using timer 7. For this, select fosc as clock source, and set a 1/2 cycle (100 kHz) for the timer 7 compare register (at fosc=20 MHz).
An example setup procedure, with a description of each step is shown below.

Setup Procedure	Description
(1) Stop the counter. TM7MD1 (x'3F78') bp4 : TM7EN = 0	(1) Set the TM7EN flag of the timer 7 mode register 1 (TM7MD1) to "0" to stop timer 7 counting.
(2) Set the special function pin to output mode. P1OMD (x'3F2F') bp4 : P1OMD4 = 1 P1DIR (x'3F31') bp4 : P1DIR4 = 1	(2) Set the P1OMD4 flag of the port 1 output mode register (P1OMD) to "1" to set P14 pin as the special function pin. Set the P1DIR4 flag of the port 1 direction control register (P1DIR) to "1" to set output mode. If it needs, pull-up resistor should be added. [☞ Chapter 4 I/O Ports]
(3) Set the timer pulse output. TM7MD2 (x'3F79') bp4 : TM7PWM = 0	(3) Set the TM7PWM flag of the timer 7 mode register 2 (TM7MD2) to "0" to select the timer pulse output.
(4) Select the condition for timer clear. TM7MD2 (x'3F79') bp5 : TM7BCR = 1	(4) Set the TM7BCR flag of the TM7MD2 register to "1" to select the compare match as a clear source of a binary counter .
(5) Select the count clock source. TM7MD1 (x'3F78') bp1-0 : TM7CK1-0 = 00 bp3-2 : TM7PS1-0 = 00	(5) Select fosc as an clock source by the TM7CK1-0 flag of the TM7MD1 register. Also, select 1/1 frequency as an count clock source by the TM7PS1-0 flag.

Setup Procedure	Description
(6) Set the timer pulse output cycle. TM7PR1 (X'3F75', X'3F74')=x'00C7'	(6) Set the 1/2 frequency of the timer pulse output cycle to the timer 7 preset register 1 (TM7PR1). To be 100 kHz by a divided 20 MHz, set as follows ; 200 - 1 = 199 (x'C7') At that time, the same value is loaded to the timer 7 compare register 1 (TM7OC1) and the timer 7 binary counter (TM7BC) is initialized to x'0000'.
(7) Release the reset of the timer pulse output. TM7MD1 (x'3F78') bp5 : TM7CL = 0	(7) Set the TN7CL flag of the TM7MD 1 register to "0" to enable the timer pulse output.
(8) Start the timer operation. TM7MD1 (x'3F78') bp4 : TM7EN = 1	(8) Set the TM7EN flag of the TM7MD1 register to "1" to start timer 7.

TM7BC counts up from x'0000'. If TM7BC reaches the set value of the TM7OC1 register and TM7BC is cleared to x'0000', the signal of the TM7IO output is inverted and TM7BC counts up from x'0000', again.

At TM7OC1 = x'0000' and x'0001', the timer pulse output has the same waveform.

Either binary counter stops or operates, the timer output is "L", when the TM7CL flag of the TM7MD2 register is set to "1".

Set the compare register value as follows.

$$\text{The compare register value} = \frac{\text{The timer pulse output cycle}}{\text{The count clock cycle x 2}} - 1$$

Write to preset register should be done while timer is stopped or within timer interrupt processing.
And use MOVW instruction for write to preset register.

7-6 16-bit Standard PWM Output

(Only duty can be changed consecutively)

The TM7IO pin outputs the standard PWM output, which is determined by the over flow timing of the binary counter, and the match timing of the timer binary counter and the compare register.

7-6-1 Operation

■16-bit Standard PWM Output (Timer 7)

PWM waveform with an arbitrary duty is generated by setting a duty of PWM "H" period to the compare register 1 (TM7OC1). Its cycle is the time of the 16-bit timer full count over flow.

Table 7-6-1 shows the PWM output pin.

Table 7-6-1 PWM Output Pin

	Timer 7
PWM output pin	TM7IO output pin (P14)

■Count Timing of Standard PWM Output (at Normal)(Timer 7)

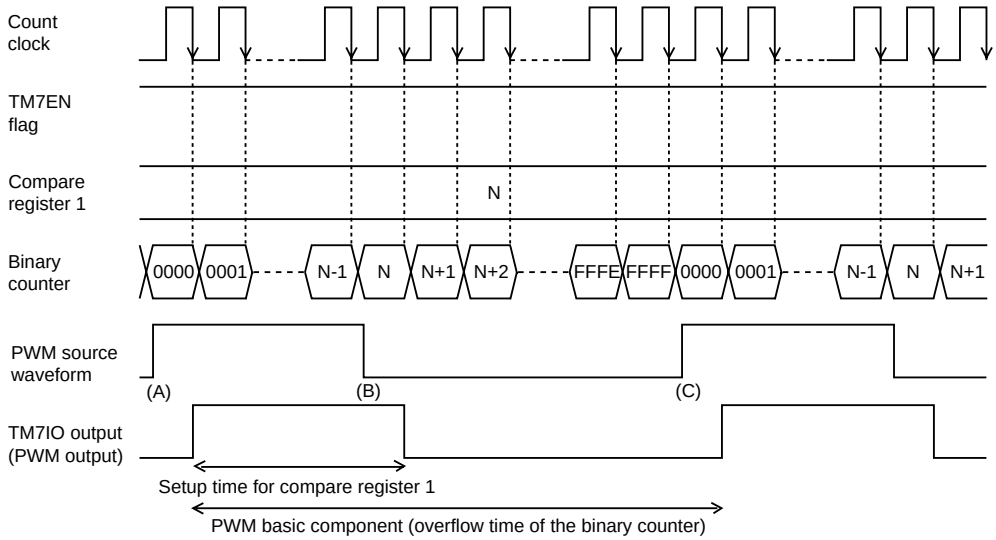


Figure 7-6-1 Count Timing of Standard PWM Output (at Normal)

PWM source waveform,

(A) shows "H" till the binary counter reaches the compare register from x'0000'.

(B) shows "L" after the compare match, then the binary counter counts up till the over flow.

(C) shows "H", again if the binary counter becomes overflow.

The PWM output form pins is 1 count clock delay of PWM source waveform. This is happened to correct the output cycle.

■Count Timing of Standard PWM Output (when Compare Register 1 is x'0000')(Timer 7)
Here is the count timing at setting x'0000' to the compare register 1.

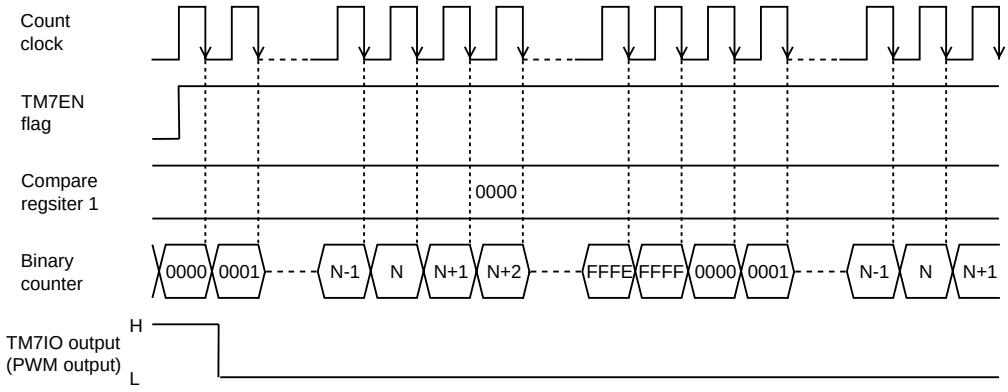


Figure 7-6-2 Count Timing of Standard PWM Output (when Compare Register 1 is x'0000')

PWM output shows "H ", when TM7EN flag is stopped (at "0").

■Count Timing of Standard PWM Output (when Compare Register 1 is x'FFFF')(Timer 7)
Here is the count timing at setting x'FFFF' to the compare register 1.

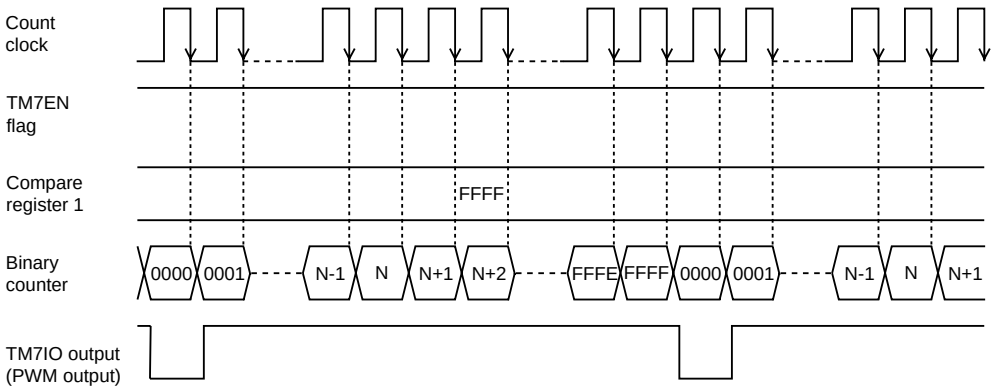


Figure 7-6-3 Count Timing of Standard PWM Output (when Compare Register 1 is x'FFFF')

When the standard PWM output is operated, set the TM7BCR flag of the TM7MD2 register to "0" to select the full count over flow as a binary counter clear source and a PWM output setup ("H" output) source.

By setting the T7PWMSL flag of the TM7MD2 register, the TM7OC1 compare match or the TM7OC2 compare match can be selected as a PWM output reset ("L" output) source.

7-6-2 Setup Example

■Standard PWM Output Setup Example (Timer 7)

The TM7IO output pin outputs the 1/4 duty PWM output waveform at 305.18 Hz with timer 7. The high frequency oscillation (fosc) is set to be operated at 20 MHz. One cycle of the PWM output waveform is decided by the overflow of a binary counter. "H" period of the PWM output waveform is decided by the set value of a compare register 1.

An example setup procedure, with a description of each step is shown below.

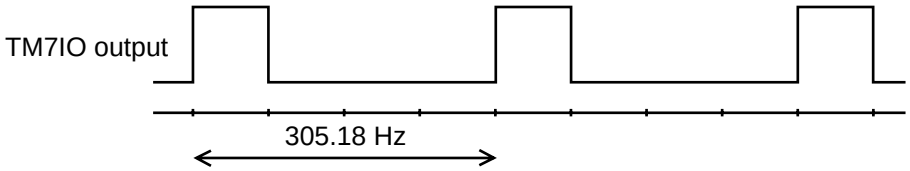


Figure 7-6-4 Output Waveform of TM7IO Output Pin

Setup Procedure	Description
(1) Stop the counter. TM7MD1 (x'3F78') bp4 : TM7EN = 0	(1) Set the TM7EN flag of the timer 7 mode register 1 (TM7MD1) to "0" to stop timer 7 counting.
(2) Set the special function pin to output mode. P1OMD (x'3F2F') bp4 : P1OMD4 = 1 P1DIR (x'3F31') bp4 : P1DIR4 = 1	(2) Set the P1OMD4 flag of the port 1 output mode register (P1OMD) to "1" to set the P14 pin as a special function pin. Set the P1DIR4 flag of the port 1 direction control register (P1DIR) to "1" to set output mode. Add pull-up resistor, if it necessary. [☞ Chapter 4 I/O Ports]
(3) Set the PWM output. TM7MD2 (x'3F79') bp4 : TM7PWM = 1	(3) Set the TM7PWM flag of the timer 7 mode register 2 (TM7MD2) to "1" to select the PWM output.
(4) Set the standard PWM output operation. TM7MD2 (x'3F79') bp5 : TM7BCR = 0	(4) Set the TM7BCR flag of the TM7MD2 register to "0" to select the full count over flow as a binary counter clear source.

Setup Procedure	Description
(5) Select the count clock source. TM7MD1 (x'3F78') bp1-0 : TM7CK1-0 = 00 bp3-2 : TM7PS1-0 = 00	(5) Select fosc at clock source by the TM7CK1-0 flag of the TM7MD1 register. Also, select 1/1 frequency (no division) at count clock source by the TM7PS1-0 flag.
(6) Set "H" period of the PWM output. TM7PR1 (x'3F75', x'3F74')=x'4000'	(6) Set "H" period of the PWM output to the timer 7 preset register 1 (TM7PR1). To be a 1/4 duty of the full count (65536), set as follows ; 65536 / 4 = 16384 (x'4000') At that time, the same value is loaded to the timer 7 compare register 1 (TM7OC1) and the timer 7 binary counter (TM7BC) is initialized to x'0000'.
(7) Start the timer operation. TM7MD1 (x'3F78') bp4 : TM7EN = 1	(7) Set the TM7EN flag of the TM7MD1 register to "1" to start timer 7.

TM7BC counts up from x'0000'. The PWM source waveform outputs "H" until TM7BC reaches the set value of the TM7OC1 register, then, after the match it outputs "L". After that, TM7BC continues to count up, once overflow happens, the PWM source waveform outputs "H" again, and TM7BC counts up from x'0000', again. TM7IO pin outputs one count clock delay of the PWM source waveform.

In the initial state of the PWM output, it is changed to "H" output from "L" output as the PWM operation is selected by the TM7PWM flag of the TM7MD2 register.

Write to preset register should be done while timer is stopped or within timer interrupt processing.
And use MOVW instruction for write to preset register.

7-7 16-bit High Precision PWM Output

(Cycle/Duty can be changed consecutively)

The TM7IO pin outputs high precision PWM output, which is determined by the match timing of the timer binary counter and the compare register 1 and the match timing of the binary counter and the compare register 2.

7-7-1 Operation

■16-bit High Precision PWM Output Operation (Timer 7)

The PWM waveform with any cycle/duty is generated by setting the cycle of PWM to the compare register 1 (TM7OC1) and setting the duty of the "H" period to the compare register 2 (TM7OC2). The 16-bit timer that high precision PWM output operation function can be used is timer 7.

■Count Timing of High Precision PWM Output (at Normal) (Timer 7)

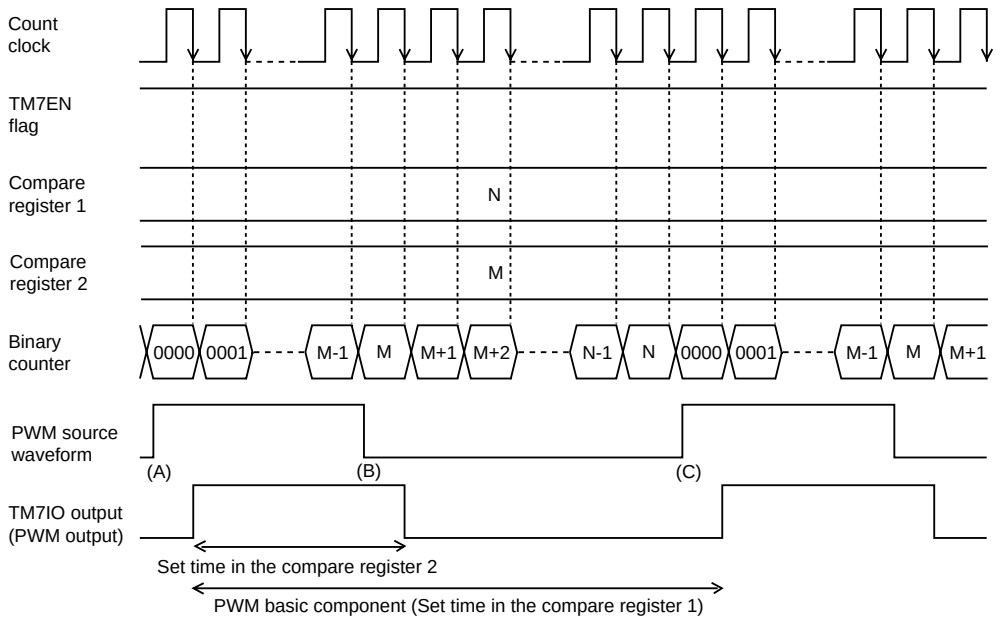


Figure 7-7-1 Count Timing of High Precision PWM Output (at Normal)

PWM source waveform,

(A) is "H" until the binary counter reaches the compare register from x'0000'.

(B) is "L" after the TM7OC2 compare match, then the binary counter counts up till the binary counter reaches the TM7OC1 compare register to be cleared.

(C) is "H", again if the binary counter is cleared.

The PWM output from pin is 1 count clock delay of PWM source waveform. This is happened to form inside to correct the output cycle.

■Count Timing of High Precision PWM Output (When compare register 2 is x'0000'l) (Timer 7)
Here is the count timing as the compare register 2 is set to x'0000' ;

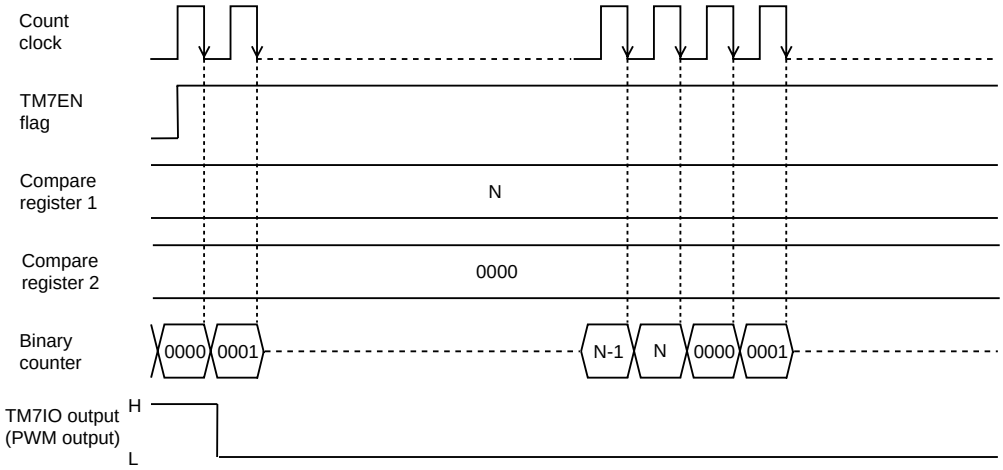


Figure 7-7-2 Count Timing of High Precision PWM Output (When compare register 2 is x'0000')

When the TM7EN flag is stopped (at "0"), the PWM output signal is "H".

■Count Timing of High Precision PWM Output (at compare register 2 = compare register 1) (Timer 7)
Here is the count timing as the compare register 2 is set the same value to the compare register 1 ;

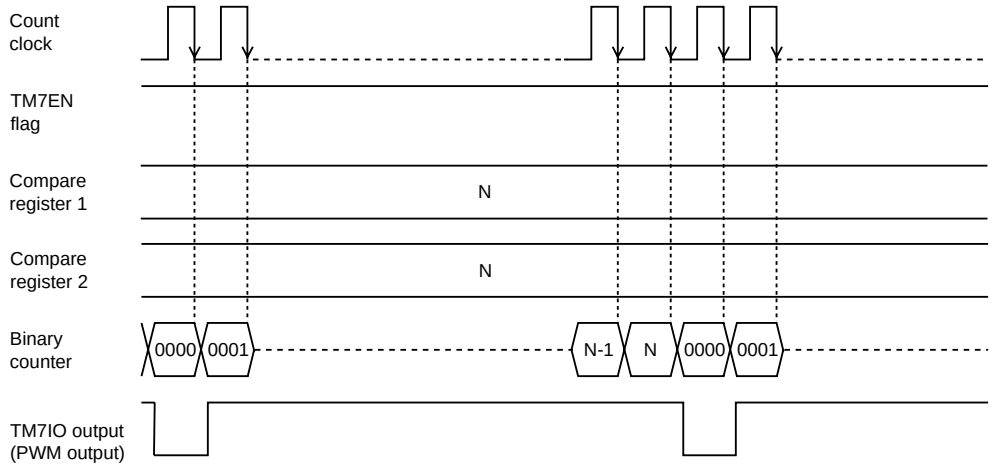


Figure 7-7-3 Count Timing of High Precision PWM Output (at compare register 2=compare register 1)

For the high precision PWM output, set the TMBCR flag of the TM7MD2 register to "1" to select the TM7OC1 compare match as a clear source of the binary counter and as a setup ("H" output) source of the PWM output. Also, set the T7PWMSL flag to "1" to select the TM7OC2 compare match as a reset ("L" output) source of the PWM output.

7-7-2 Setup Example

■High Precision PWM Output Setup Example (Timer 7)

The TM7IO output pin outputs the 1/4 duty PWM output waveform at 400 Hz with timer 7. Select fosc/2 (at fosc = 20 MHz) as a clock source. One cycle of the PWM output waveform is decided by the set value of a compare register 1. "H" period of the PWM output waveform is decided by the set value of a compare register 2.

An example setup procedure, with a description of each step is shown below.

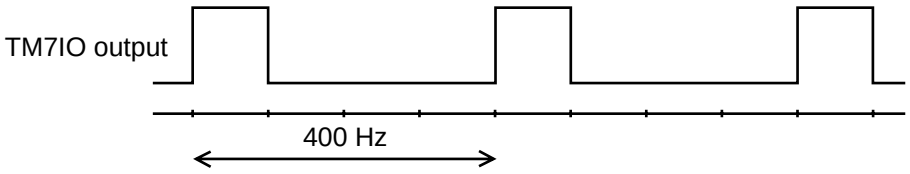


Figure 7-7-4 Output Waveform of TM7IO Output Pin

Setup Procedure	Description
(1) Stop the counter. TM7MD1 (x'3F78') bp4 : TM7EN = 0	(1) Set the TM7EN flag of the timer 7 mode register 1 (TM7MD1) to "0" to stop timer 7 counting.
(2) Set the special function pin to output mode. P1OMD (x'3F2F') bp4 :P1OMD4 = 1 P4DIR (x'3F31') bp4 : P1DIR4 = 1	(2) Set the P1OMD4 flag of the port 1 output mode register (P1OMD) to "1" to set the P14 pin as a special function pin. Set the P1DIR4 flag of the port 1 direction control register (P1DIR) to "1" for output mode. Add pull-up resistor, if it necessary. [☞ Chapter 4 I/O Ports]
(3) Set the PWM output. TM7MD2 (x'3F79') bp4 : TM7PWM = 1	(3) Set the TM7PWM flag of the timer 7 mode register 2 (TM7MD2) to "1" to select the PWM output.
(4) Set the high precision PWM output operation. TM7MD2 (x'3F79') bp5 : TM7BCR = 1 bp6 : T7PWMSL = 1	(4) Set the TM7BCR flag of the TM7MD2 register to "1" to select the TM7OC1 compare match as a clear source of binary counter. Also, set the T7PWMSL flag to "1" to select the TM7OC2 compare match as a duty decision source of the PWM output.

Setup Procedure	Description
(5) Select the count clock source. TM7MD1 (x'3F78') bp1-0 : TM7CK1-0 = 00 bp3-2 : TM7PS1-0 = 01	(5) Select fosc as clock source by the TM7CK1-0 flag of the TM7MD1 register. Also, select 1/2 dividing as count clock source by the TM7PS1-0 flag.
(6) Set the PWM output cycle. TM7PR1 (x'3F75',x'3F74') = x'61a7'	(6) Set the PWM output cycle to the timer 7 preset register 1 (TM7PR1). To be 400 Hz by divided 10 MHz, set as follows : 25000 - 1 = 24999 (x'61a7') At that time, the same value is loaded to the timer 7 compare register 1 (TM7OC1), and the timer 7 binary counter (TM7BC) is initialized to x'0000'.
(7) Set the "H" period of the PWM output. TM7PR2 (x'3F7D',x'3F7C')=x'186a'	(7) Set the "H" period of the PWM output to the timer 7 preset register 2 (TM7PR2). To be a 1/4 duty of 25000 dividing, set as follows ; 25000 / 4 = 6250 (x'186a') At that time, the same value is loaded to the timer 7 compare register 2 (TM7OC2).
(8) Start the timer operation. TM7MD1 (x'3F78') bp4 : TM7EN = 1	(8) Set the TM7EN flag of the TM7MD1 register to "1" to start timer 7.

TM7BC counts up from x'0000'. The PWM source waveform outputs "H" until TM7BC matches the set value of the TM7OC2 register. Once they matches, it outputs "L". After that, TM7BC continues to count up, once TM7BC matches the TM7OC1 register to be cleared, the PWM source waveform outputs "H" again and TM7BC counts up from x'0000' again. TM7IO pin outputs one count clock delay of the PWM source waveform.

In the initial state of the PWM output, it is changed from "L" output to "H" output as the PWM output is selected by the TM7PWM flag of the TM7MD register.

Set as the set value of TM7OC2 ≤ the set value of TM7OC1. If it is set as the set value of TM7OC2 > the set value of TM7OC1, the PWM output is a "H" fixed output.

Write to preset register should be done while timer is stopped or within timer interrupt processing.
And use MOVW instruction for write to preset register.

7-8 16-bit Timer Synchronous Output

7-8-1 Operation

When the binary counter of the timer reaches the set value of the compare register, the latched data is output from port 6 at the next count clock.

■Synchronous Output Operation by 16-bit Timer (Timer 7)
The port 6 latched data is output from the output pin at the interrupt request generation by the match of the binary counter (TM7OC1) or by the full count overflow.
Only port 6 can perform synchronous output operation, and individual pins can be set.

■Count Timing of Synchronous Output (Timer 7)

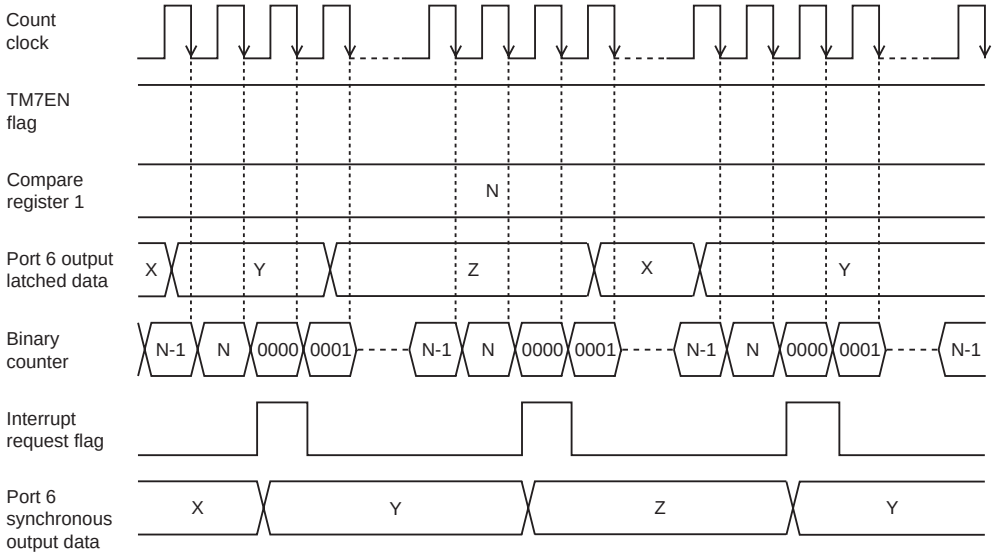


Figure 7-8-1 Count Timing of Synchronous Output (Timer 7)

The port 6 latched data is output from the output pin in synchronization with the interrupt request generation by the match of a binary counter and a compare register 1.

7-8-2 Setup Example

■Synchronous Output Setup Example (Timer 7)

Setup example that latched data of port 6 is output constantly (100 µs) by using timer 7 from the synchronous output pin is shown below. The clock source of timer 7 is selected fs/4 (at fosc=8 MHz).

An example setup procedure, with a description of each step is shown below.

Setup Procedure	Description
(1) Stop the counter. TM7MD1 (x'3F78') bp4 : TM7EN = 0	(1) Set the TM7EN flag of the timer 7 mode register 1 (TM7MD1) to "0" to stop timer 7 counting.
(2) Select the synchronous output event. FLOAT (x'3F2E') bp1-0 : SYOEVS1-0 = 01	(2) Set the SYOEVS1-0 flag of the pin control register (FLOAT) to "01" to set the synchronous output event to the timer 7 interrupt.
(3) Set the synchronous output pin. P6SYO (x'3F1E') = x'FF' P6DIR(x'3F36') = x'FF'	(3) Set the port 6 synchronous output control register (P6SYO) to x'FF' to set the synchronous output pin. (P67 to P60 : Synchronous output pin) Set the port 6 direction control register (P6DIR) to x'FF' to set port 6 to output pin. If it needs, pull-up resistor should be added. [☞ Chapter 4 I/O Ports]
(4) Select the condition of timer clear. TM7MD2 (x'3F79') bp5 : TM7BCR = 1	(4) Set the TM7BCR flag of the TM7MD2 register to "1" to select the compare match as a clear source of the binary counter.
(5) Select the count clock source. TM7MD1 (x'3F78') bp1-0 : TM7CK1-0 = 01 bp3-2 : TM7PS1-0 = 10	(5) Select fs as a clock source by the TM7CK1-0 flag of the TM7MD 1 register. Also, select a 1/4 dividing as a clock source by the TM7PS1-0 flag.
(6) Set the synchronous output event generation cycle. TM7PR1 (x'3F75',x'3F74')=x'0063'	(6) Set the synchronous output event generation cycle to the timer 7 preset register 1 (TM7PR1). To be 10 kHz by dividing 1 MHz, set as follows ; 100 - 1 = 99 (x'0063') At that time, the same value is loaded to the timer 7 compare register 1 (TM7OC1), and TM7BC is initialized to x'0000'.

Setup Procedure	Description
(7) Start the timer operation. TM7MD1 (x'3F78') bp4 : TM7EN = 1	(7) Set the TM7EN flag of the TM7MD1 register to "1" to start timer 7.

TM7BC counts up from x'0000'. If any data is written to the port 6 output register (P6OUT), TM7BC reaches the set value of TM7OC1 register and the synchronous output pin outputs data of port 7 in every time an interrupt request is generated.

Write to preset register should be done while timer is stopped or within timer interrupt processing.
And use MOVW instruction for write to preset register.

7-9 16-bit Timer Capture

7-9-1 Operation

The value of a binary counter is stored to register at the timing of the external interrupt input signal, or the timing of writing operation with an arbitrary value to the capture register.

■Capture Operation with External Interrupt Signal as a Trigger (Timer 7)
Capture trigger of input capture function is generated at the external interrupt signal that passed through the external interrupt interface block. The capture trigger is selected by the timer 7 mode register 2 (TM7MD2) and the external interrupt control register (IRQ0ICR, IRQ1ICR, IRQ2ICR, IRQ3ICR).
Here are the capture trigger to be selected and the interrupt flag setup.

Table 7-9-1 Capture Trigger

Capture trigger source	Timer 7 mode register 2		External interrupt n control register (IRQnICR)	Both edges interrupt control register (EDGDT)		Interrupt starting edge of external interrupt n
	T7ICT1-0	T7ICEDG	REDGn (bp5)	EDGSEL3	EDGSEL2	
IRQ0 falling edge	00(IRQ0)	1	0	-	-	IRQ0 falling edge
IRQ0 rising edge	00(IRQ0)	1	1	-	-	IRQ0 rising edge
IRQ0 both edge	00(IRQ0)	0	0	-	-	IRQ0 falling edge
			1	-	-	IRQ0 rising edge
IRQ1 falling edge	01(IRQ1)	1	0	-	-	IRQ1 falling edge
IRQ1 rising edge	01(IRQ1)	1	1	-	-	IRQ1 rising edge
IRQ1 both edge	01(IRQ1)	0	0	-	-	IRQ1 falling edge
			1	-	-	IRQ1 rising edge
IRQ2 falling edge	10(IRQ2)	1	0	-	0	IRQ2 falling edge
IRQ2 rising edge	10(IRQ2)	1	1	-	0	IRQ2 rising edge
IRQ2 both edge(*)	10(IRQ2)	0	0	-	0	IRQ2 falling edge
			1	-	0	IRQ2 rising edge
IRQ3 falling edge	11(IRQ3)	1	0	0	-	IRQ3 falling edge
IRQ3 rising edge	11(IRQ3)	1	1	0	-	IRQ3 rising edge
IRQ3 both edge(*)	11(IRQ3)	0	0	0	-	IRQ3 falling edge
			1	0	-	IRQ3 rising edge

The external interrupt 2 (IRQ2) and the external interrupt 3 (IRQ3) has the function of both edges interrupt. But, that function cannot be used when the input capture should be generated at both edges. [table 7-9-1(*)]

When capture trigger is activated at both edges of an external interrupt, the high precision pulse width measurement that measures the width of "H" period and "L" period of input signal constantly, is possible

with the automatic data transfer function (ATC1). In the transfer mode 5 of ATC1, set the address of the input capture register TM7ICL to the memory pointer 1. The "H" period and "L" period of the input signal can be measured by transferring the value of the input capture register (TM7ICL, TM7ICH) to memory in every generation of a capture trigger.

An interrupt request and a capture trigger are generated at switching the valid edge of an external interrupt by program, when the setup is as follows ;

(1) at switching the valid edge from the falling to the rising, when the interrupt pin is "H" level.

(2) at switching the valid edge from the rising to the falling, when the interrupt pin is "L" level.

This is not happened, if the interrupt edge is switched after the generation of an valid edge interrupt set in advance. But when the both edges interrupt function is used, this may be happened. Be sure to consider the noise influence for operation of the interrupt flag on program.

[☞ Chapter 3 3-3-4. Programmable active Edge Interrupt]

■Capture Count Timing at a Both Edges of External Interrupt Signal is selected as a Trigger (Timer 7)

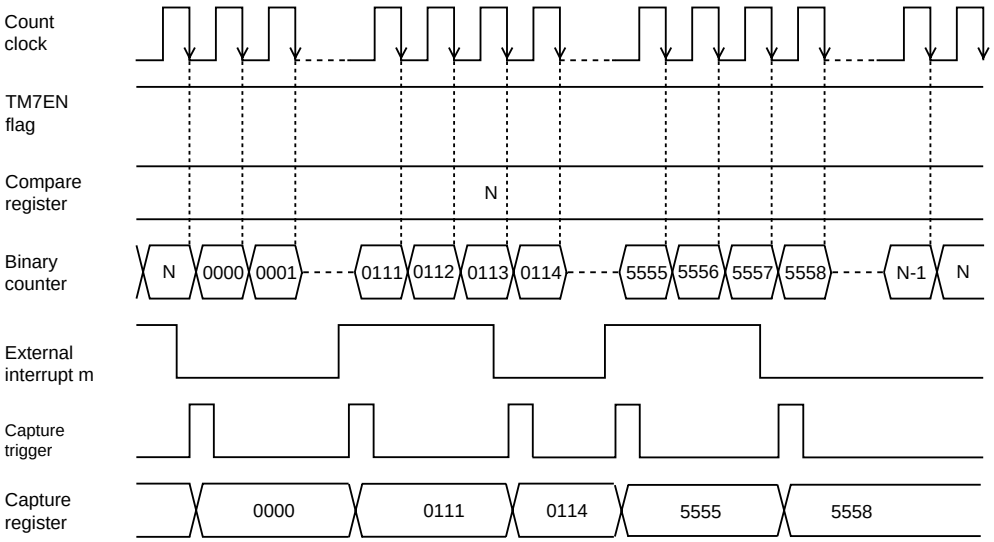


Figure 7-9-1 Capture Count Timing at an External Interrupt Signal is selected as a Trigger (Timer 7)

A capture trigger is generated at the both edges of the external interrupt m input signal. At the same timing, the value of a binary counter is stored to the input capture register. That value is decided by the value of a binary counter at the falling edge of a capture trigger. When the specified edge is selected as a capture trigger generation source, a capture trigger is generated at the interrupt generation specified edge, only. The other count timing is same to the count timing of the timer operation.

When the binary counter is used as a free counter that counts x'0000' to x'FFFF', set the compare register 1 to x'FFFF', or set the TM7BCR flag of the TM7MD2 register to "0".

Even if a capture trigger is generated before the value of the input capture register is read out, the value of the input capture register can be rewritten.

In the initial state after releasing the reset, the generation of trigger by the external interrupt signal is disabled. Set the T7ICEN flag of the TM7MD2 register to "1" to enable the trigger generation.

■Capture Operation that the writing to program is selected as a Trigger (Timer 7)

A capture trigger can be generated by writing an arbitrary value to the input capture register (TM7IC), and at the same timing, the value of the binary counter can be stored to the input capture register.

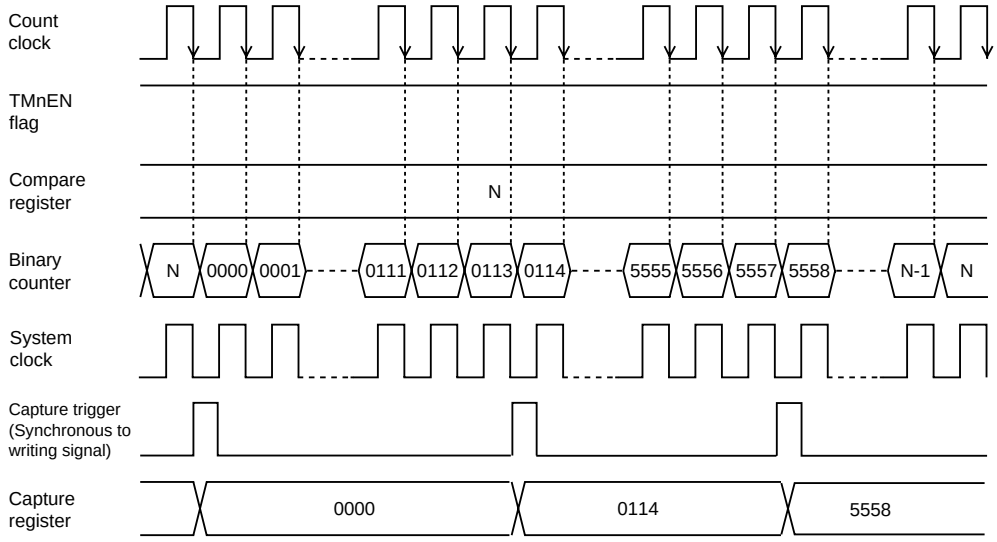


Figure 7-9-2 Capture Count Timing with a Writing Signal to Program as a Trigger (Timer 7)

A capture trigger is generated at the writing signal to the input capture register. The writing signal is generated at the last cycle of the writing instruction. At this timing, the value of the binary counter is stored to the input capture register. That value is decided by the value of the binary counter at the falling edge of the capture trigger. The other timing is same to the timer operation.

The writing to the input capture register to generate a capture trigger should be done with a 8-bit access instruction to the TM7ICL register or the TM7ICH register.
At this time, data is not actually written to the TM7IC register.

On hardware, there is no flag to disable the capture operation with the writing operation to the software as a trigger. Capture operation is enabled, regardless of the T7ICEN flag of the TM7MD2 register.

7-9-2 Setup Example

■Capture Function Setup Example (Timer 7)

Pulse width measurement is enabled by storing the value of the binary counter to the capture register at the interrupt generation edge of the external interrupt 0 input signal with timer 7. The interrupt generation edge is specified to be the rising edge.

An example setup procedure, with a description of each step is shown below.

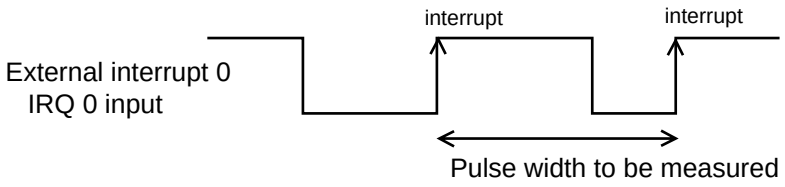


Figure 7-9-3 Pulse Width Measurement of External Interrupt 0

Setup Procedure	Description
(1) Stop the counter. TM7MD1 (x'3F78') bp4 : TM7EN = 0	(1) Set the TM7EN flag of the timer 7 mode register 1 (TM7MD1) to "0" to stop timer 7 counting.
(2) Select the condition for timer clear. TM7MD2 (x'3F79') bp5 : TM7BCR = 1	(2) Set the TM7BCR flag of the timer 7 mode register 2 (TM7MD2) to "1" to select the compare match as a clear source of binary counter.
(3) Select the count clock source. TM7MD1 (x'3F78') bp1-0 : TM7CK1-0 = 00 bp3-2 : TM7PS1-0 = 00	(3) Select fosc as clock source by the TM7CK1-0 flag of the TM7MD1 register. And select 1/1 (no dividing) of fosc as count clock source by the TM7PS1-0 flag.
(4) Select the capture trigger generation interrupt source. TM7MD2 (x'3F79') bp1-0 : T7ICT1-0 = 00	(4) Select the external interrupt 0 (IRQ0) input as a generation source of capture trigger by the T7ICT1-0 flag of the TM7MD2 register.
(5) Select the interrupt generation valid edge. IRQ0ICR (x'3FE2') bp5 : REDG0 = 1	(5) Set the REDG0 flag of the external interrupt 0 control register (IRQ0ICR) to "1" to select the rising edge as the interrupt generation valid edge.

Setup Procedure	Description
(6) Select the capture trigger generation edge. TM7MD2 (x'3F79') bp7 : T7ICEDG = 1	(6) Set the T7ICEDG flag of the TM7MD2 register to "1" to select the external interrupt valid edge as a generation source of capture trigger.
(7) Set the compare register. TM7PR1(x'3F75',x'3F74') = x'FFFF'	(7) Set the timer 7 preset register 1 (TM7PR1) to x'FFFF'. At that time, the same value is loaded to the timer 7 compare register 1 (TM7OC1), and the timer 7 binary counter (TM7BC) is initialized to x'0000'.
(8) Set the interrupt level. IRQ0ICR (x'3FE2') bp7-6 : IRQ0LV1-0= 10	(8) Set the interrupt level by the IRQ0LV1-0 flag of the IRQ0ICR register. If any interrupt request flag may be set already, clear them. [☞ Chapter 3 3-1-4. Interrupt Flag Setup]
(9) Enable the interrupt. IRQ0ICR (x'3FE2') bp1 : IRQ0IE = 1	(9) Enable the interrupt by setting the IRQ0IE flag of the IRQ0ICR register to "1".
(10) Enable the capture trigger generation. TM7MD2 (x'3F79') bp2 : T7ICEN = 1	(10) Enable the capture trigger generation by setting the T7ICEN flag of the TM7MD2 register to "1".
(11) Start the timer operation. TM7MD1 (x'3F78') bp4 : TM7EN = 1	(11) Set the TM7EN flag of the TM7MD1 register to "1" to start timer 7.

TM7BC counts up from x'0000'. At the timing of the rising edge of the external interrupt 0 input signal, the value of TM7BC is stored to the TM7IC register. And at that time, the pulse width between rising edges of the external interrupt input signal can be measured by reading the value of TM7IC register by the interrupt service routine, and by calculating the margin of the capture values (the values of the TM7IC register).

Chapter 8 Time Base Timer / 8-bit Free-running Timer

8-1 Overview

This LSI has a time base timer and a 8-bit free-running timer (timer 6).
Time base timer is a 15-bit timer counter. These timers can stop the timer counting only at stand-by mode (STOP mode).

8-1-1 Functions

Table 8-1-1 shows the clock sources and the interrupt generation cycles that timer 6 and time base timer can select.

Table 8-1-1 Clock Source and Generation Cycle

	Time base timer	Timer 6 (8-Bit free-running timer)
8-Bit timer operation	-	√
Interrupts / source	TBIRQ	TM6IRQ
Clock source	fosc fx	fosc fx fs fosc X $1/2^{12}$ (*1) fosc X $1/2^{13}$ (*1) fx X $1/2^{12}$ (*2) fx X $1/2^{13}$ (*2)
Interrupt generation cycle	fosc X $1/2^{7}$ (*1) fosc X $1/2^{8}$ (*1) fosc X $1/2^{9}$ (*1) fosc X $1/2^{10}$ (*1) fosc X $1/2^{13}$ (*1) fosc X $1/2^{15}$ (*1) fx X $1/2^{7}$ (*2) fx X $1/2^{8}$ (*2) fx X $1/2^{9}$ (*2) fx X $1/2^{10}$ (*2) fx X $1/2^{13}$ (*2) fx X $1/2^{15}$ (*2)	The interrupt generation cycle is decided by the arbitrary value written to TM6OC.
fosc : Machine clock (High speed oscillation) fx : Machine clock (Low speed oscillation) fs : System clock [☞ Chapter 2 2-5. Clock Switching] - *1 can be used as a clock source of time base timer is selected to 'fosc'. - *2 can be used as a clock source of time base timer is selected to 'fx'. - Time base timer and timer 6 cannot stop timer 6 counting.		

8-1-2 Block Diagram

■Timer 6, Time Base Timer Block Diagram

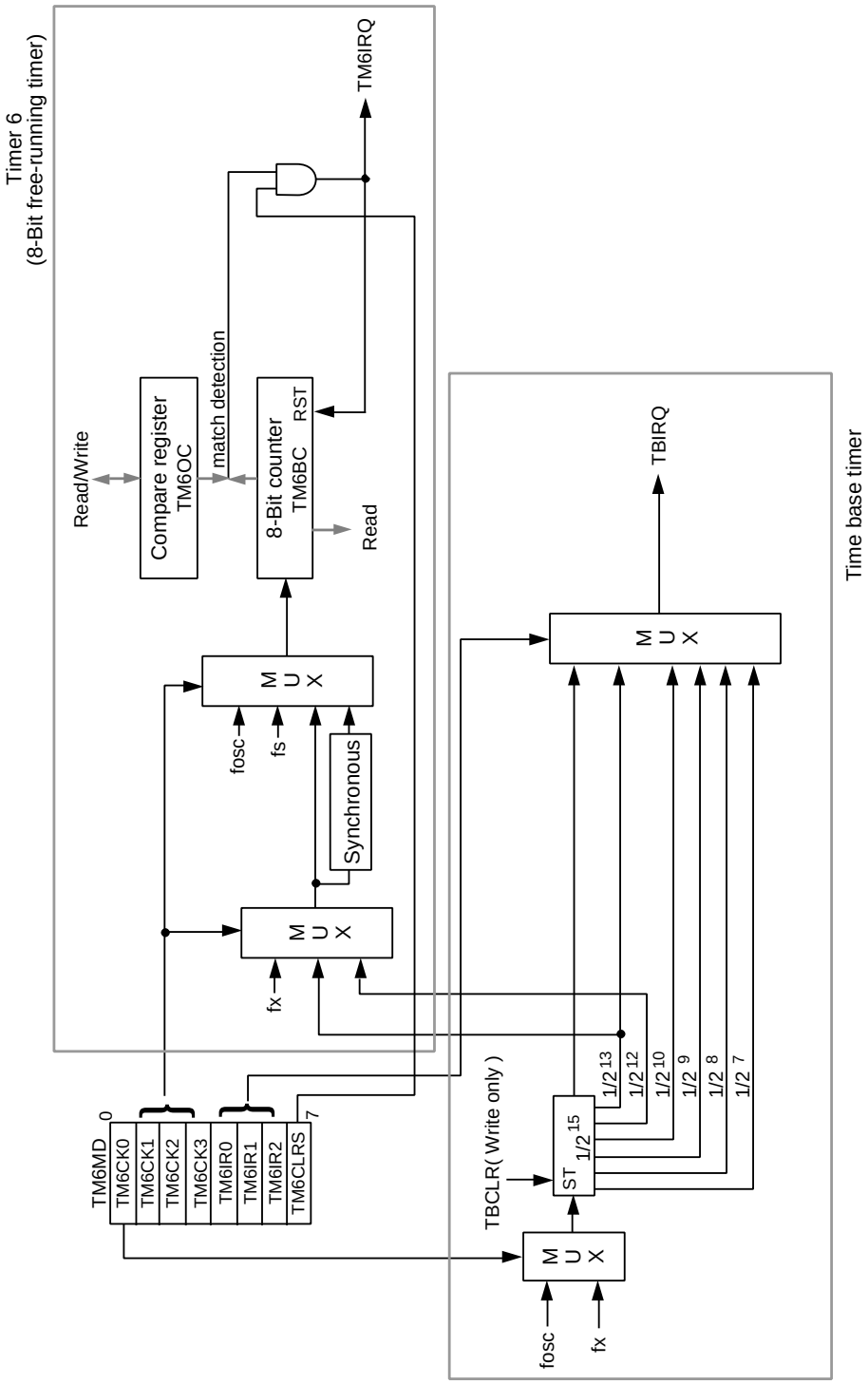


Figure 8-1-1 Block Diagram (Timer 6, Time Base Timer)

8-2 Control Registers

Timer 6 consists of binary counter (TM6BC), compare register (TM6OC), and is controlled by mode register (TM6MD). Time base timer is controlled by mode register (TM6MD) and time base timer clear register (TBCLR), too.

8-2-1 Control Registers

Table 8-2-1 shows the registers that control timer 6, time base timer.

Table 8-2-1 Control Registers

	Register	Address	R/W	Function	Page
Timer 6	TM6BC	x'03F68'	R	Timer 6 binary counter	VIII - 5
	TM6OC	x'03F69'	R/W	Timer 6 compare register	VIII - 5
	TM6MD	x'03F6A'	R/W	Timer 6 mode register	VIII - 6
	TM6ICR	x'03FEF'	R/W	Timer 6 interrupt control register	III - 28
Timer base timer	TM6MD	x'03F6A'	R/W	Timer 6 mode register	VIII - 6
	TBCLR	x'03F6B'	W	Time base timer clear control register	VIII - 5
	TBICR	x'03FF0'	R/W	Time base interrupt control register	III - 29

R/W : Readable / Writable
R : Readable only
W : Writable only

8-2-2 Programmable Timer Registers

Timer 6 is a 8-bit programmable counter.
Programmable counter consists of compare register (TM6OC) and binary counter (TM6BC).

Binary counter is a 8-bit up counter. When the TM6CLRS flag of the timer 6 mode register (TM6MD) is "0" and the interrupt cycle data is written to the compare register (TM6OC), the timer 6 binary counter (TM6BC) is cleared to x'00'.

■Timer 6 Binary Counter (TM6BC)

	7	6	5	4	3	2	1	0	
TM6BC	TM6BC7	TM6BC6	TM6BC5	TM6BC4	TM6BC3	TM6BC2	TM6BC1	TM6BC0	(At reset : X X X X X X X X)

Figure 8-2-1 Timer 6 Binary Counter (TM6BC : x'03F68', R)

■Timer 6 Compare Register (TM6OC)

	7	6	5	4	3	2	1	0	
TM6OC	TM6OC7	TM6OC6	TM6OC5	TM6OC4	TM6OC3	TM6OC2	TM6OC1	TM6OC0	(At reset : X X X X X X X X)

Figure 8-2-2 Timer 6 Compare Register (TM6OC : x'03F69', R/W)

Time base timer cannot stop counting but the software can reset its operation. Time base timer can be cleared by writing an arbitrary value to the time base timer clear control register (TBCLR).

■Time Base Timer Clear Control Register (TBCLR)

	7	6	5	4	3	2	1	0	
TBCLR	-	-	-	-	-	-	-	-	(For writing only)

Figure 8-2-3 Time Base Timer Clear Control Register (TBCLR : x'03F6B')

8-2-3 Timer Mode Registers

This is a readable / writable register that controls timer 6 and time base timer.

■Timer 6 Mode Register (TM6MD)

	7	6	5	4	3	2	1	0
TM6MD	TM6CLRS	TM6IR2	TM6IR1	TM6IR0	TM6CK3	TM6CK2	TM6CK1	TM6CK0

(At reset : 0 0 0 0 0 0 0 0)

TM6CKS0	Time base timer clock source
0	fosc
1	fx

TM6CK3	TM6CK2	TM6CK1	Timer 6 clock source
0	0	0	fosc
		1	fs
	1	0	fx
		1	Synchronous fx
1	0	0	Time base selection clock × $1/2^{13}$
		1	Synchronous time base selection clock × $1/2^{13}$
	1	0	Time base selection clock ×$1/2^{12}$
		1	Synchronous time base selection clock × $1/2^{12}$

TM6IR2	TM6IR1	TM6IR0	Time base timer interrupt cycle selection
0	0	0	Time base selection clock × $1/2^{7}$
		1	Time base selection clock × $1/2^{8}$
	1	0	Time base selection clock × $1/2^{9}$
		1	Time base selection clock × $1/2^{10}$
1	0	-	Time base selection clock × $1/2^{13}$
	1		Time base selection clock × $1/2^{15}$

TM6CLRS	Timer 6 binary counter clear
0	Enable the initialization of TM6BC as TM6OC is written
1	Disable the initialization of TM6BC as TM6OC is written

* TM6IRQ is disabled as TM6CLRS = 0,
TM6IRQ is enabled as TM6CLRS = 1.

Figure 8-2-4 Timer 6 Mode Register (TM6MD : x'03F6A', R/W)

8-3 8-bit Free-running Timer

8-3-1 Operation

■8-bit Free-running Timer (Timer 6)

The generation cycle of the timer interrupt is set by the clock source selection and the setting value of the compare register (TM6OC), in advance. If the binary counter (TM6BC) reaches the setting value of the compare register, an interrupt is generated at the next count clock, then the binary counter is cleared and counting is restarted from x'00'.

Table 8-3-1 shows clock source that can be selected.

Table 8-3-1 Clock Source at Timer Operation (Timer 6)

Clock source	1count time
fosc	50 ns
fx	30.5 µs
fs	100 ns
fosc X $1/2^{12}$	204.8 µs
fosc X $1/2^{13}$	409.6 µs
fx X $1/2^{12}$	125 ms
fx X $1/2^{13}$	250 ms
Notes : as fosc = 20(MHz) fx = 32.768(kHz) fs = fosc/2 = 10 MHz	

Timer 6 cannot stop its timer counting except at stanby mode (STOP mode).

■8-bit Free-running Timer as a 1 minute-timer, a 1 second-timer

Table 8-3-2 shows the clock source selection and the TM6OC register setup, when a 8-bit free-running timer is used as a 1 minute-timer, a 1 second-timer.

Table 8-3-2 1 minute-timer, 1 second-timer Setup (Timer 6)

Interrupt Generation Cycle	Clock Source	TM6OC Register
1 min	fx x $1/2^{13}$	X'EF'
1 s	fx x $1/2^{12}$	X'07'
	fx x $1/2^{13}$	X'03'
fx = 32.768(kHz)		

When the 1 minute-timer (1 min.) is set on Table 8-3-2, the bp1 waveform frequency (cycle) of the TM6BC register is 1 Hz (1 s). So, that can be used for adjusting the seconds.

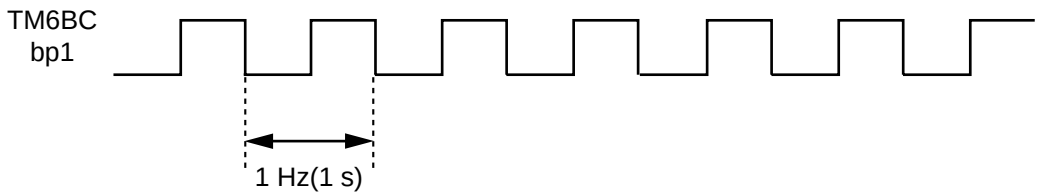


Figure 8-3-1 Waveform of TM6BC Register bp1 (Timer 6)

■Count Timing of Timer Operation (Timer 6)

Binary counter counts up with the selected clock source as a count clock.

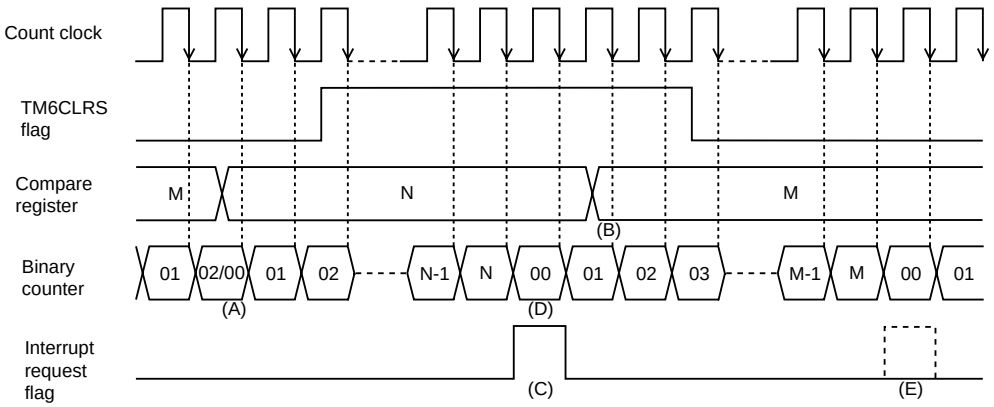


Figure 8-3-2 Count Timing of Timer Operation (Timer 6)

(A) When any data is written to the compare register as the TM6CLRS flag is "0", the binary counter is cleared to x'00'.

(B) Even if any data is written to the compare register as the TM6CLRS flag is "1", the binary counter is not changed.

(C) When the binary counter reaches the value of the compare register as the TM6CLRS flag is "1", an interrupt request flag is set at the next count clock.

(D) When an interrupt request flag is set, the binary counter is cleared to x'00' and restarts the counting.

(E) Even if the binary counter reaches the value of the compare register as the TM6CLRS flag is "0", no interrupt request flag is set.

When the binary counter reaches the value in the compare register, the inrerrupt request flag is set and the binary counter is cleared, at the next count clock.
So, set the compare register as :

Compare register setting = (count till the interrupt request - 1)

If fx is selected as the count clock source in timer 6, when the binary counter is read at operation, uncertain value on counting up may be read. To prevent this, select the synchronous fx as the count clock source.
But if the synchronous fx is selected as the count clock source, CPU mode cannot return from STOP/HALT mode.

If the compare register is set the smaller than the binary counter during the count operation, the binary counter counts up to the overflow, at first.

8-3-2 Setup Example

■Timer Operation Setup (Timer 6)

Timer 6 generates an interrupt constantly for timer function. Fs(fosc = 20 MHz) is selected as a clock source to generate an interrupt every 250 cycles (25 µs).

An example setup procedure, with a description of each step is shown below.

Setup Procedure	Description
(1) Enable the binary counter initialization. TM6MD (x'3F6A') bp7 : TM6CLRS = 0	(1) Set the TM6LRS flag of the timer 6 mode register (TM6MD) to "0". At that time, the initialization of the timer 6 binary counter (TM6BC) is enabled.
(2) Select the clock source. TM6MD (x'3F6A') bp3-1 : TM6CK3-1 = 001	(2) Clock source can be selected by the TM6CK3-1 flag of the TM6MD register. Actually, fs is selected.
(3) Set the interrupt generation cycle. TM6OC (X'3F69') = x'F9'	(3) Set the interrupt generation cycle to the timer 6 compare register (TM6OC). At that timer, TM6BC is initialized to x'00'.
(4) Enable the interrupt request generation. TM6MD (x'3F6A') bp7 : TM6CLRS = 1	(4) Set the TM6CLRS flag of the TM6MD register to "1" to enable the interrupt request generation.
(5) Set the interrupt level. TM6ICR (x'3FEF') bp7-6 : TM6LV1-0 = 01	(5) Set the interrupt level by the TM6LV1-0 flag of the timer 6 interrupt control register (TM6ICR). If the interrupt request flag may be already set, clear them. [☞ Chapter 3 3-1-4. Interrupt Flag Setup]
(6) Enable the interrupt. TM6ICR (x'3FEF') bp1 : TM6IE = 1	(6) Set the TM6IE flag of the TM6ICR register to "1" to enable the interrupt.

* the above steps (1), (2) can be set at once.

As TM6OC is set, TM6BC is initialized to x'00' to count up.
When TM6BC matches TM6OC, the timer 6 interrupt request flag is set to "1" at the next count clock and TM6BC is cleared to x'00' to restart counting.

If the TM6CLRS flag of the TM6MD register is set to "0", TM6BC can be initialized in every rewriting of TM6OC register, but in that state the timer 6 interrupt is disabled. If the timer 6 interrupt should be enabled, set the TM6CLRS flag to "1" after rewriting the TM6OC register.

On the timer 6 clock source selection, either the time base timer output or the time base timer synchronous output is selected, the clock setup of time base timer is needed.

8-4 Time Base Timer

8-4-1 Operation

■Time Base Timer (Time Base Timer)
The Interrupt is constantly generated.
Table 8-4-1 shows the interrupt generation cycle in combination with the clock source ;

Table 8-4-1 Time Base Timer Interrupt Generation Cycle

Selected clock source	Interrupt generation cycle	
fosc	fosc X $1/2^7$	6.4 µs
	fosc X $1/2^8$	12.8 µs
	fosc X $1/2^9$	25.6 µs
	fosc X $1/2^{10}$	51.2 µs
	fosc X $1/2^{13}$	409.6 µs
	fosc X $1/2^{15}$	1.64 ms
fx	fx X $1/2^7$	3.9 ms
	fx X $1/2^8$	7.8 ms
	fx X $1/2^9$	15.6 ms
	fx X $1/2^{10}$	31.2 ms
	fx X $1/2^{13}$	250 ms
	fx X $1/2^{15}$	1 s
fosc = 20(MHz) fx = 32.768(kHz)		

■Count Timing of Timer Operation (Time Base Timer)

The counter counts up with the selected clock source as a count clock.

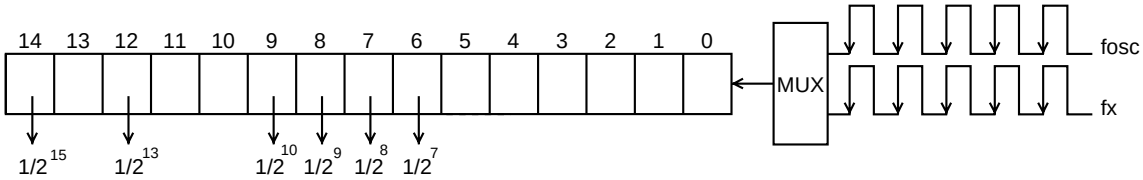


Figure 8-4-1 Count Timing of Timer Operation (Time Base Timer)

When the selected interrupt cycle has passed, the interrupt request flag of the time base interrupt control register (TBICR) is set to "1".

An interrupt may be generated at switching of the clock source. Enable interrupt after switching the clock source.

Time base timer cannot stop the operation.
The initialization can be done by writing an arbitrary value to the time base timer clear control register (TBCLR).

8-4-2 Setup Example

■Timer Operation Setup (Time Base Timer)
An interrupt can be generated constantly with time base timer in the selected interrupt cycle. The interrupt generation cycle is as fosc × $1/2^{13}$ (as 0.977 ms : fosc = 8.38 MHz) for generation interrupts.
An example setup procedure, with a description of each step is shown below.

Setup Procedure	Description
(1) Select the clock source. TM6MD (x'3F6A') bp0 : TM6CK0 = 0	(1) Select fosc as a clock source by the TM6CK0 flag of the timer 6 mode register (TM6MD).
(2) Select the interrupt generation cycle. TM6MD (x'3F6A') bp6-4 : TM6IR2-0 = 100	(2) Select the selected clock × $1/2^{13}$ as an interrupt generation cycle by the TM6IR2-0 flag of the TM6MD register.
(3) Initialize the time base timer. TBCLR (x'3F6B') = x'00'	(3) Write value to the time base timer clear control register (TBCLR) to initialize the time base timer. That makes the time base timer initialize.
(4) Set the interrupt level. TBICR (x'3FF0') bp7-6 : TBLV1-0 = 01	(4) Set the interrupt level by the TBLV1-0 flag of the time base interrupt control register (TBICR). If the interrupt request flag had already been set, clear it. [☞ Chapter 3 3-1-4. Interrupt Flag Setup]
(5) Enable the interrupt. TBICR (x'3FF0') bp1 : TBIE = 1	(5) Set the TBIE flag of the TBICR register to "1" to enable the interrupt.

* the above steps (1), (2) can be set at once.

When the selected interrupt generation cycle has passed, the interrupt request flag of the time base interrupt control register (TBICR) is set to "1".

Chapter 9 Watchdog Timer

9

9-1 Overview

This LSI has a watchdog timer. This timer is used to detect software processing errors. It is controlled by the watchdog timer control register (WDCTR). And, once an overflow of watchdog timer is generated, a watchdog interrupt (WDIRQ) is generated. If the watchdog interrupt is generated twice, consecutively, it is regarded to be an indication that the software cannot execute in the intended sequence; thus, a system reset is initiated by the hardware.

9-1-1 Block Diagram

■Watchdog Timer Block Diagram

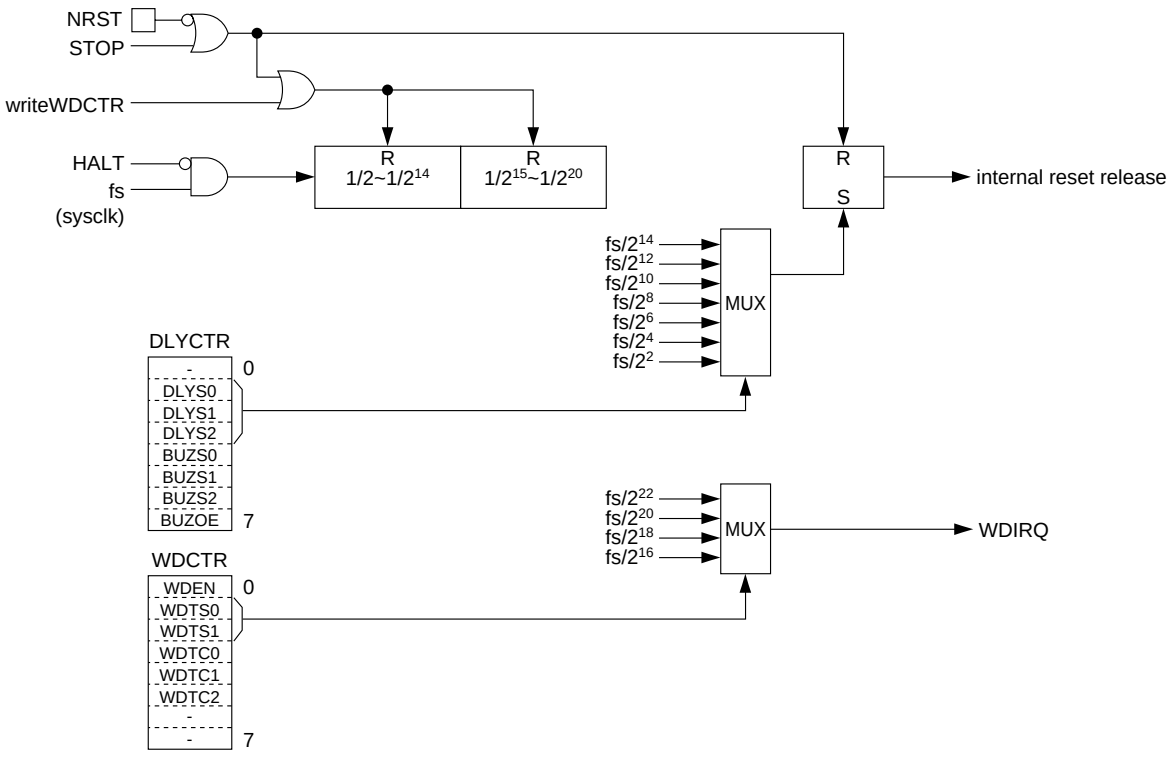


Figure 9-1-1 Block Diagram (Watchdog Timer)

The watchdog timer is also used as a timer to count the oscillation stabilization wait time. This is used as a watchdog timer except at recovering from STOP mode and at reset releasing.
The watchdog timer is initialized at reset or at STOP mode, and counts system clock (fs) as a clock source from the initial value (x'0000'). The oscillation stabilization wait time is set by the oscillation stabilization control register (DLYCTR). After the oscillation stabilization wait, counting is continued as a watchdog timer. [☞ Chapter 2 2-8. Reset]

9-2 Control Registers

The watchdog timer is controlled by the watchdog timer control register (WDCTR).

■Watchdog Timer Control Register (WDCTR)

	7	6	5	4	3	2	1	0	
WDCTR	-	-	WDTC2	WDTC1	WDTC0	WDTS1	WDTS0	WDEN	(At reset: - - 0 0 0 1 1 0)

WDEN	Watchdog timer enable
0	Watchdog timer disable/clear
1	Watchdog timer enable

WDTS1	WDTS0	Watchdog time-out period setup
0	0	2^{16} of system clock
	1	2^{18} of system clock
1	0	2^{20} of system clock
	1	2^{22} of system clock

WDTC2	WDTC1	WDTC0	Watchdog timer is cleared at the following cycle or more
0	0	0	Anytime
		1	2^{7} of system clock
	1	0	2^{9} of system clock
		1	2^{11} of system clock
1	0	0	2^{13} of system clock
		1	2^{15} of system clock
	1	0	2^{17} of system clock
		1	2^{19} of system clock

Figure 9-2-1 Watchdog Timer Control Register (WDCTR : x'03F02', R/W)

9-3 Operation

9-3-1 Operation

The watchdog timer counts system clock (fs) as a clock source. If the watchdog timer is overflowes, the watchdog interrupt (WDIRQ) is generated as an non maskable interrupt (NMI). At reset, the watchdog timer is stopped, but once the operation is enabled, it cannot be stopped except at reset. The watchdog timer control register (WDCTR) sets when the watchdog timer is released or how long the time-out period should be.

This watchdog timer can detect such that the watchdog timer clear is repeated in short cycle. If the watchdog timer clear is repeated in shorter cycle than the set time (the lowest value of watchdog timer clear possible), it is regarded as an error and the watchdog interrupt (WDIRQ) is generated.

If the watchdog interrupt (WDIRQ) is generated twice consecutively, it is regarded to be an indication that the software cannot execute in the intended sequence; thus, a system reset is initiated by the hardware.

The watchdog timer cannot stop, once it starts operation.

■Usage of Watchdog Timer

When the watchdog timer is used, constant clear in program is needed to prevent an overflow of the watchdog timer. As a result of the software failure, the software cannot execute in the intended sequence, thus the watchdog timer overflows and error is detected.

Programming of the watchdog timer is generally done in the last step of its programming.

■How to Detect Incorrect Code Execution

The watchdog timer is executed to be cleared in the certain cycle on the correct code execution. On this LSI, the watchdog timer detects errors when,

(1) the watchdog timer overflows.
(2) the watchdog timer clear happens in the shorter cycle than the watchdog timer clear possible lowest value, set in the watchdog timer control register (WDCTR).

When the watchdog timer detects any error, the watchdog interrupt (WDIRQ) is generated as a non maskable interrupt (NMI).

■How to Clear Watchdog Timer

The watchdog timer can be cleared by writing to the watchdog timer control register (WDCTR). The watchdog timer can be cleared regardless of the writing data to the register. The bit-set (BSET) that does not change the value is recommended.

■Watchdog Timer Period

The watchdog timer period is decided by the bp2, 1 (WDTS1-0) of the watchdog timer control register (WDCTR) and the system clock (fs). If the watchdog timer is not cleared till the set period of watchdog timer, that is regarded as an error and the watchdog interrupt (WDIRQ) of the non-maskable interrupt (NMI) is generated.

Table 9-3-1 Watchdog Timer Period

WDTS1	WDTS0	Watchdog time-out period
0	0	2^{16} X system clock
0	1	2^{18} X system clock
1	0	2^{20} X system clock
1	1	2^{22} X system clock

System clock is decided by the CPU mode control register (CPUM).

[☞ Chapter 2 2-5. Clock Switching]

The watchdog timer period is generally decided from the execution time for main routine of program. That should be set the longer period than the value of the execution time for main routine divided by natural number (1, 2, , ,). And insert the instruction of the watchdog timer clear to the main routine as that value makes the same cycle.

■The Lowest Value for Watchdog Timer Clear

The lowest value for watchdog timer clear is decided by the bp5, 4, 3 (WDTC2, WDTC1, WDTC0) of the watchdog timer control register (WDCTR).

Table 9-3-2 The Lowest Value for Watchdog Timer Clear

WDTC2	WDTC1	WATC0	Watchdog timer can be cleared at the following cycle or more
0	0	0	no limit
0	0	1	2^{7} X system clock
0	1	0	2^{9} X system clock
0	1	1	2^{11} X system clock
1	0	0	2^{13} X system clock
1	0	1	2^{15} X system clock
1	1	0	2^{17} X system clock
1	1	1	2^{19} X system clock

■Watchdog Timer and CPU Mode

The relation between this watchdog timer and CPU mode features are as follows ;

(1) In NORMAL, IDLE, SLOW mode, the system clock is counted.
(2) The counting is continued regardless of switching at NORMAL, IDLE, SLOW mode.
(3) In HALT mode, the watchdog timer is stopped.
(4) In STOP mode, the watchdog timer is cleared automatically by hardware.
(5) In STOP mode, the watchdog interrupt cannot be generated.
(6) After releasing reset or recovering from STOP, the counting is executed for the duration of the oscillation stabilization wait time.

Generally, in the system used STOP mode, if the STOP mode is done or not is divided on the program execution, but, in this case, the counting value of the watchdog timer differs. So, the watchdog interrupt should be prevented by setting the lowest value for watchdog timer clear.

9-3-2 Setup Example

The watchdog timer detects errors. On the following example, the watchdog timer period is set to $2^{18} \times$ system clock, the lowest value for watchdog timer clear is set to $2^9 \times$ system clock.
An example setup procedure, with a description of each step is shown below.

■Initial Setup Program (Watchdog Timer Initial Setup Example)

Setup Procedure	Description
(1) Set the time-out period. WDCTR (x'03F02') bp2-1 : WDTS1-0 = 01	(1) Set the WDTS1-0 flag of the watchdog timer control register (WDCTR) to "01" to select the time-out period to $2^{18} \times$ system clock.
(2) Set the lowest value for clear. WDCTR (x'03F02') bp5-3 : WDTC2-0 = 010	(2) Set the WDTC2-0 flag of the WDCTR register to "010" to select the lowest value for clear to $2^9 \times$ system clock.
(3) Start the watchdog timer operation. WDCTR (x'03F02') bp0 : WDEN = 1	(3) Set the WDEN flag of the WDCTR register to start the watchdog timer operation.

The command of setting the WDEN flag to "1" should be done on the last step of the initial setting. If the watchdog control register (WDCTR) is changed after starting the operation, the watchdog interrupt may be generated depending on the setting of the lowest value for clear.

■Main Routine Program (Watchdog Timer Constant Clear Setup Example)

Setup Procedure	Description
(1) Set the constant watchdog timer clear. Writing to WDCTR (x'03F02') (cf.) BSET (WDCTR) WDEN (bp0 : WDEN = 1)	(1) Clear the watchdog timer by the cycle from $2^9 \times$ system clock up to $2^{18} \times$ system clock. The watchdog timer clear should be inserted in the main routine, with the same cycle, and to be the set cycle. The recommended instruction is the bit-set (BSET), does not change value, for clear.

■Interrupt Service Routine Setup

Setup Procedure	Description
(1) Set the watchdog interrupt service routine. NMICR (x'03FE1') TBNZ (NMICR) WDIR, WDPRO	(1) If the watchdog timer overflows, the non maskable interrupt is generated. Confirm that the WDIR flag of the non maskable interrupt control register (NMICR) is "1" on the interrupt service routine, and manage the suitable execution.

The operation, just before the WDOG interrupt may be executed wrongly. Therefore, if the WDOG interrupt is generated, initialize the system.

Chapter 10 Buzzer

10-1 Overview

This LSI has a buzzer. It can output the square wave, having a frequency $1/2^9$ to $1/2^{14}$ of the high speed oscillation clock, or by $1/2^3$ to $1/2^4$ of the low speed oscillation clock.

10-1-1 Block Diagram

■Buzzer Block Diagram

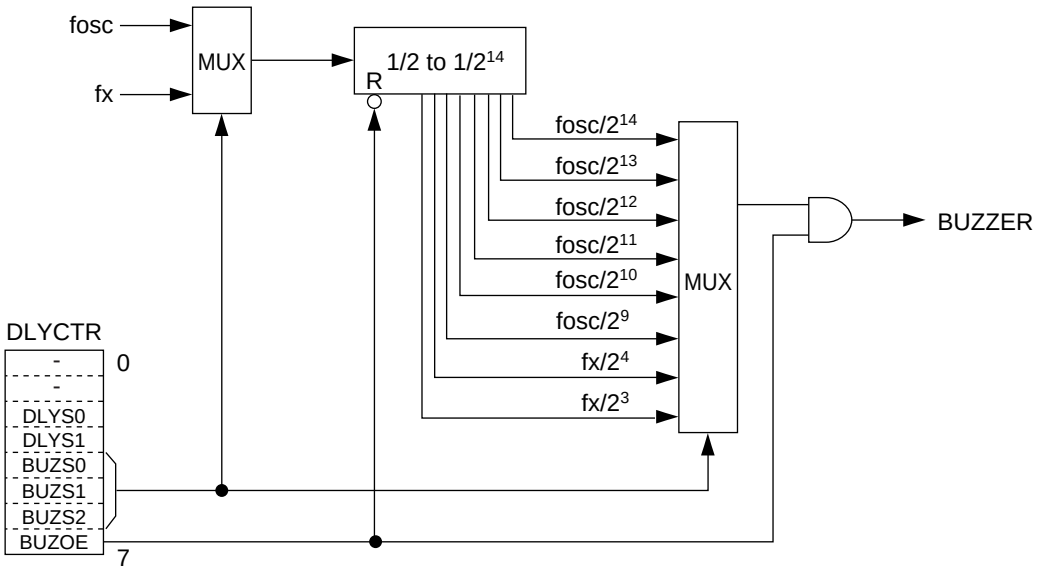


Figure 10-1-1 Block Diagram (Buzzer)

10-2 Control Register

■Oscillation Stabilization Wait Timer Control Register

	7	6	5	4	3	2	1	0
DLYCTR	BUZOE	BUZS2	BUZS1	BUZS0	DLYS2	DLYS1	DLYS0	-

(At reset : 0 0 0 0 0 0 0 -)

DLYS2	DLYS1	DLYS0	Oscillation stabilization wait period selection
0	0	0	$fs/2^{14}$
		1	$fs/2^{12}$
	1	0	$fs/2^{10}$
		1	$fs/2^{8}$
1	0	0	$fs/2^{6}$
		1	$fs/2^{4}$
	1	0	$fs/2^{2}$
		1	Reserved

Note : After reset is released, the oscillation stabilization wait period is fixed at 2^{14}/ fs.

BUZS2	BUZS1	BUZS0	Buzzer output frequency selection
0	0	0	$fosc/2^{14}$
		1	$fosc/2^{13}$
	1	0	$fosc/2^{12}$
		1	$fosc/2^{11}$
1	0	0	$fosc/2^{10}$
		1	$fosc/2^{9}$
	1	0	$fx/2^{4}$
		1	$fx/2^{3}$

BUZOE	P06 output selection
0	Port data output
1	Buzzer output

Figure 10-2-1 Oscillation Stabilization Wait Time Control Register (DLYCTR : x'03F4D', R/W)

10-3 Operation

10-3-1 Operation

■Buzzer

Buzzer outputs the square wave, having a frequency $1/2^9$ to $1/2^{14}$ of the high speed oscillation clock (fosc), or by $1/2^3$ to $1/2^4$ of the low speed oscillation clock (fx). The BUZS 2, 1, 0 flag of the oscillation stabilization wait control register (DLYCTR) set the frequency of buzzer output. The BUZOE flag of the oscillation stabilization wait control register (DLYCTR) sets buzzer output ON / OFF.

■Buzzer Output Frequency

The frequency of buzzer output is decided by the frequency of the high oscillation clock (fosc) or the low oscillation clock (fx) and the bit 6, 5, 4 (BUZS2, BUZS1, BUZS0) of the oscillation stabilization wait control register (DLYCTR).

Table 10-3-1 Buzzer Output Frequency

fosc	fx	BUZS2	BUZS1	BUZS0	Buzzer output frequency
20 MHz	-	0	0	0	1.22 kHz
20 MHz	-	0	0	1	2.44 kHz
20 MHz	-	0	1	0	4.88 kHz
8.38 MHz	-	0	1	0	2.05 kHz
8.38 MHz	-	0	1	1	4.09 kHz
2 MHz	-	1	0	0	1.95 kHz
2 MHz	-	1	0	1	3.91 kHz
-	32 kHz	1	1	0	2 kHz
-	32 kHz	1	1	1	4 kHz

10-3-2 Setup Example

Buzzer outputs the square wave of 2 kHz from P06 pin. It is used 8.38 MHz as the high oscillation clock (fosc).
An example setup procedure, with a description of each step is shown below.

Setup Procedure	Description
(1) Set the buzzer frequency. DLYCTR (x'3F4D') bp6-4 : BUZS2-0 = 010	(1) Set the BUZS2-0 flag of the oscillation stabilization wait control register (DLYCTR) to "010" to select fosc/2^{12} to the buzzer frequency. When the high oscillation clock fosc is 8.38 MHz, the buzzer output frequency is 2.05 kHz.
(2) Set P06 pin. P0OUT (x'3F10') bp6 : P0OUT6 = 0 P0DIR (x'3F30') bp6 : P0DIR6 = 1	(2) Set the output data P0OUT6 of P06 pin to "0", and set the direction control P0DIR6 of P06 pin to "1" to select output mode. P06 pin outputs low level.
(3) Buzzer output ON. DLYCTR (x'3F4D') bp7 : BUZOE = 1	(3) Set the BUZOE flag of the oscillation stabilization wait control register (DLYCTR) to "1" to output the square wave of the buzzer output frequency set by P06 pin.
(4) Buzzer output OFF. DLYCTR (x'3F4D') bp7 : BUZOE = 0	(4) Set the BUZOE flag of the oscillation stabilization wait control register (DLYCTR) to "0" to clear, and P06 pin outputs low level.

Chapter 11 Serial Interface 0,1

11

11-1 Overview

This LSI contains a serial interface 0 and 1 that can be used for both communication types of clock synchronous and UART (duplex). Also, the pins are changable to A (port 0) or B (port 7).

Table 11-1-1 Serial Interface 0, 1 used pins

	A (Port A)	B (Port 7)
Serial Interface 0	P03/SBO0A/TXD0A P04/SBI0A/RXD0A P05/SBT0A	P70/SBO0B/TXD0B P71/SBI0B/RXD0B P72/SBT0B
Serial Interface 1	P00/SBO1A/TXD1A P01/SBI1A/RXD1A P02/SBT1A	P73/SBO1B/TXD1B P74/SBI1B/RXD1B P75/SBT1B

On this text, if there are not much differences between port A and port B on the operation, port A and B are ommitted.

11-1-1 Functions

Table 11-1-1 shows functions of serial interface 0, 1.

Table 11-1-1 Serial Interface 0, 1 Functions

	Serial interface 0		Serial interface 1	
Communication style	clock synchronous	UART (duplex)	clock synchronous	UART (duplex)
Interrupt	SC0TIRQ	SC0TIRQ (on transmission completion) SC0RIRQ (on reception completion)	SC1TIRQ	SC1TIRQ (on transmission completion) SC1RIRQ (on reception completion)
Used pins	SBO0,SBI0,SBT0	TXD0,RXD0	SBO1,SBI1,SBT1	TXD1,RXD1
3 channels type	√	-	√	-
2 channels type	√ (SBO0, SBT0)	√	√ (SBO1, SBT1)	√
1 channel type	-	√ (TXD0)	-	√ 3 (TXD1)
Specification of transfer bit count / Frame selection	1 to 8 bits	7 bits + 1stop 7 bits + 2stops 8 bits + 1stop 8 bits + 2stops	1 to 8 bits	7 bits + 1stop 7 bits + 2stops 8 bits + 1stop 8 bits + 2stops
Selection of parity bit	-	√	-	√
Parity bit control	-	0 parity 1 parity odd parity even parity	-	0 parity 1 parity odd parity even parity
Selection of start condition	√	only ""enable start condition"" is available	√	only ""enable start condition"" is available
Specification of the first transfer bit	√	√	√	√
Specification of input edge / output edge	√	-	√	-
Continuous operation	√	√	√	√
Continuous operation (with ATC1)	√	√	√	√
Internal clock 1/8 dividing	√	only 1/8 dividing is available	√	only 1/8 dividing is available
Clock source	fosc/2 fosc/4 fosc/16 fosc/64 fs/2 fs/4 Timer 5 output External clock	fosc/2 fosc/4 fosc/16 fosc/64 fs/2 fs/4 Timer 5 output	fosc/2 fosc/4 fosc/16 fosc/64 fs/2 fs/4 Timer 4 output External clock	fosc/2 fosc/4 fosc/16 fosc/64 fs/2 fs/4 Timer 4 output
Maximum transfer rate	2.5 MHz	300 kbps (standard 300 bps to 38.4 kbps) (timer 5 output)	2.5 MHz	300 kbps (standard 300 bps to 38.4 kbps) (timer 4 output)

osc : Machine clock (High speed oscillation)
fs : System clock [☞ Chapter 2 2-5. Clock Switching]

11-1-2 Block Diagram

■Serial Interface 0 Block Diagram

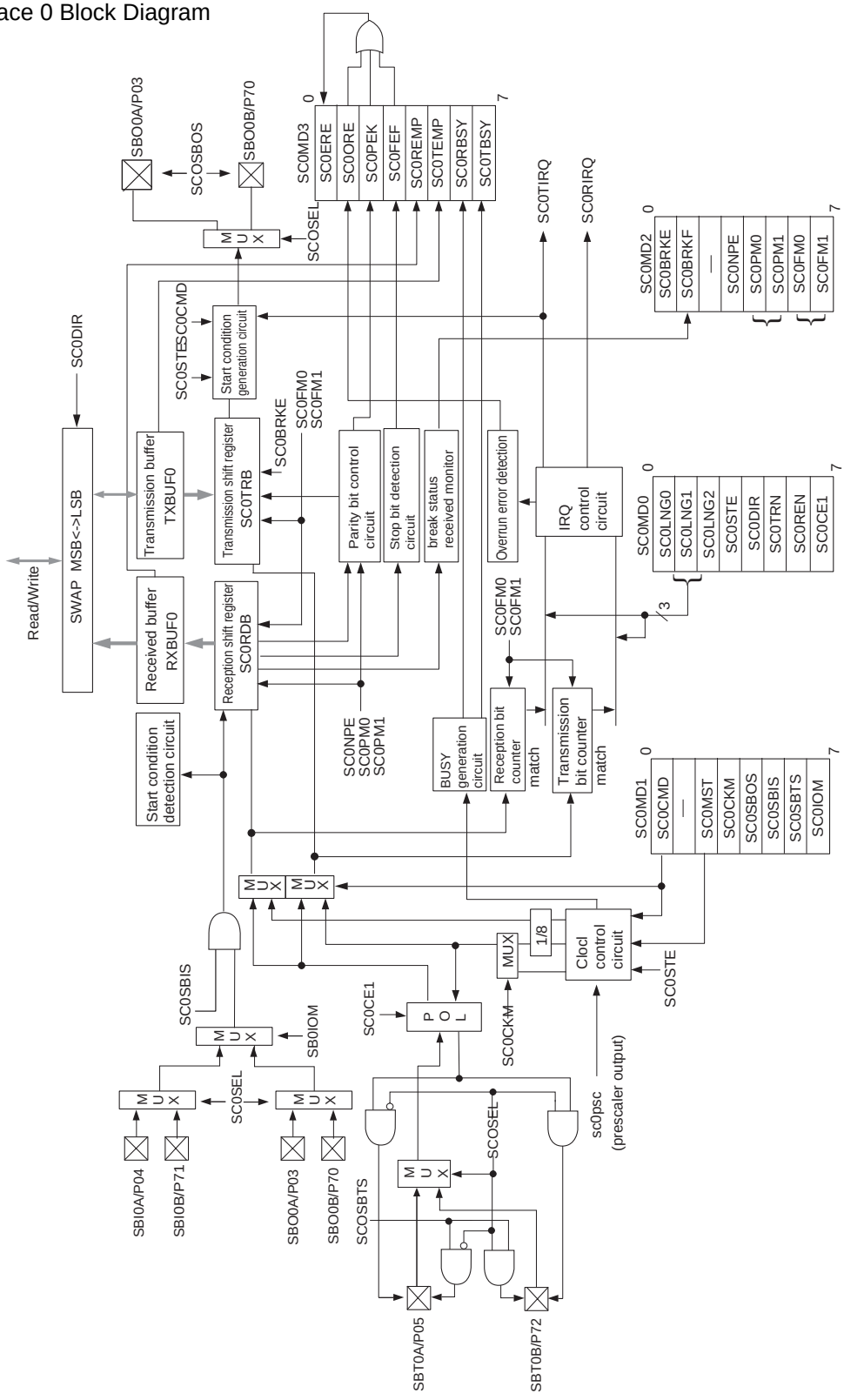


Figure 11-1-1 Serial Interface 0 Block Diagram

■Serial Interface 1 Block Diagram

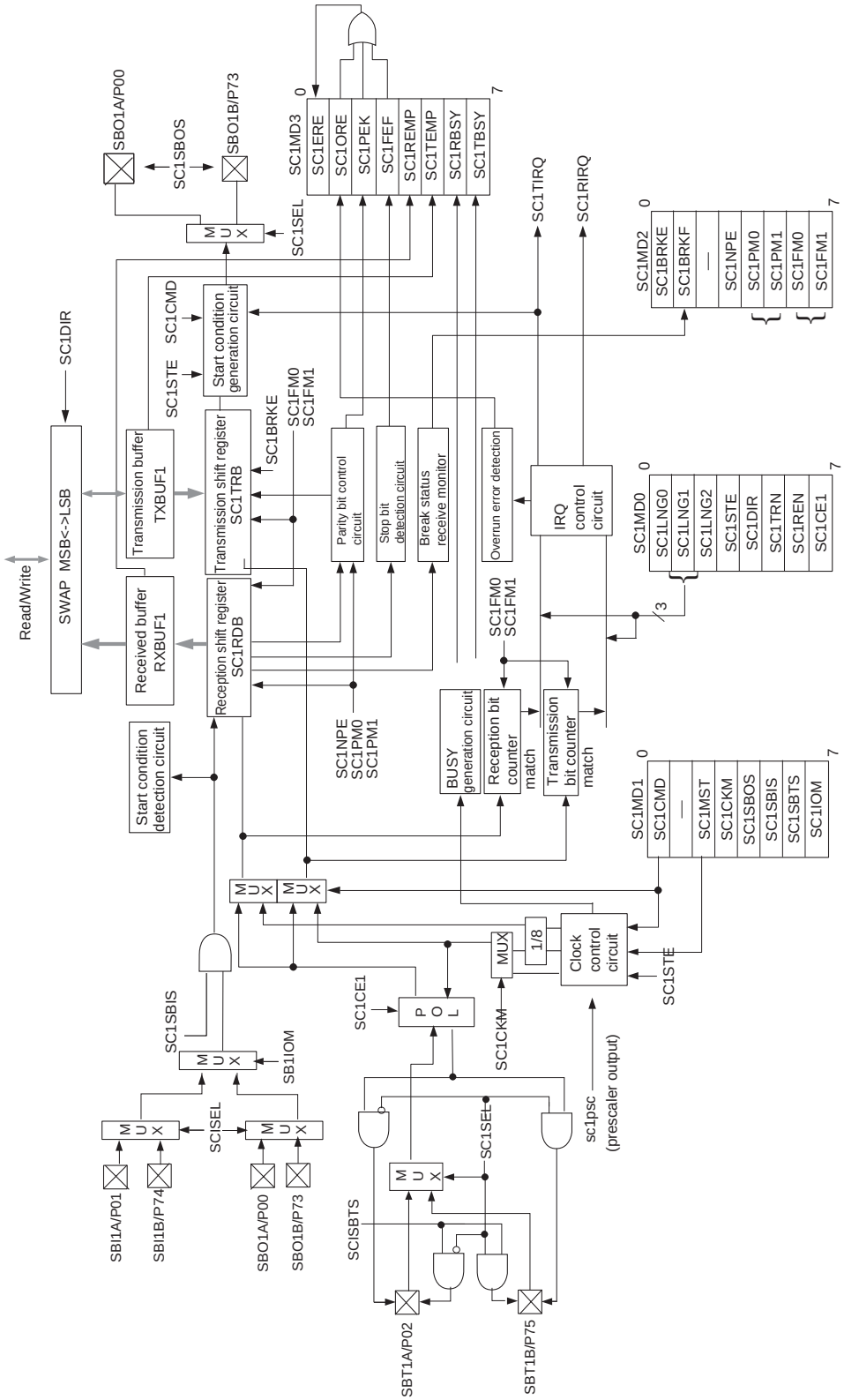


Figure 11-1-2 Serial Interface 1 Block Diagram

11-2 Control Registers

11-2-1 Registers

Table 11-2-1 shows registers to control serial interface 0, 1.

Table 11-2-1 Serial Interface 0, 1 Control Registers

	Register	Address	R/W	Function	Page
Serial interface 0	SC0MD0	x'03F92'	R/W	Serial interface 0 mode register 0	XI - 8
	SC0MD1	x'03F93'	R/W	Serial interface 0 mode register 1	XI - 9
	SC0MD2	x'03F94'	R/W	Serial interface 0 mode register 2	XI - 10
	SC0MD3	x'03F95'	R	Serial interface 0 mode register 3	XI - 11
	RXBUF0	x'03F90'	R	Serial interface 0 reception data buffer	XI - 7
	TXBUF0	x'03F91'	R/W	Serial interface 0 transmission data buffer	XI - 7
	SC0ODC	x'03F96'	R/W	Serial interface 0 port control register	XI - 12
	SC0CKS	x'03F97'	R/W	Serial interface 0 transfer clock selection register	XI - 13
	PSCMD	x'03F6F'	R/W	Prescaler control register	V - 6
	P0DIR	x'03F30'	R/W	Port 0 direction control register	IV - 7
	P0PLU	x'03F40'	R/W	Port 0 pull-up/down control register	IV - 7
	P7DIR	x'03F37'	R/W	Port 7 direction control register	IV - 31
	P7PLUD	x'03F47'	R/W	Port 7 pull-up/down control register	IV - 31
	SC0RICR	x'03FF4'	R/W	Serial interface 0 UART reception interrupt control register	III - 30
	SC0TICR	x'03FF5'	R/W	Serial interface 1 interrupt control register	III - 31
Serial interface 1	SC1MD0	x'03F9A'	R/W	Serial interface 1 mode register 0	XI - 15
	SC1MD1	x'03F9B'	R/W	Serial interface 1mode register 1	XI - 16
	SC1MD2	x'03F9C'	R/W	Serial interface 1 mode register 2	XI - 17
	SC1MD3	x'03F9D'	R	Serial interface 1 mode register 3	XI - 18
	RXBUF1	x'03F98'	R	Serial interface 1 reception data buffer	XI - 14
	TXBUF1	x'03F99'	R/W	Serial interface 1 transmission data buffer	XI - 14
	SC1ODC	x'03F9E'	R/W	Serial interface 1 port control register	XI - 19
	SC1CKS	x'03F9F'	R/W	Serial interface 1 transfer clock selection register	XI - 20
	PSCMD	x'03F6F'	R/W	Prescaler control register	V - 6
	P0DIR	x'03F30'	R/W	Port 0 direction control register	IV - 7
	P0PLU	x'03F40'	R/W	Port 0 pull-up control register	IV - 7
	P7DIR	x'03F37'	R/W	Port 7 direction control register	IV - 31
	P7PLUD	x'03F47'	R/W	Port 7 pull-up/down control register	IV - 31
	SC1RICR	x'03FF6'	R/W	Serial interface 1 UART reception interrupt control register	III - 32
	SC1TICR	x'03FF7'	R/W	Serial interface 1 interrupt control register	III - 33

R/W : Readable / Writable

R : Readable only

11-2-2 Serial Interface 0 Data Buffer Registers

Serial Interface 0 has each 8-bit data buffer register for transmission, and for reception.

■Serial Interface 0 Reception Data Buffer (RXBUF0)

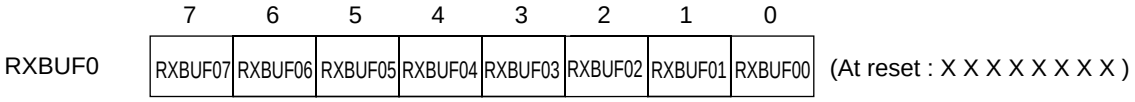


Figure 11-2-1 Serial Interface 0 Reception Data Buffer (RXBUF0 : x'03F90', R)

■Serial Interface 0 Transmissin Data Buffer (TXBUF0)

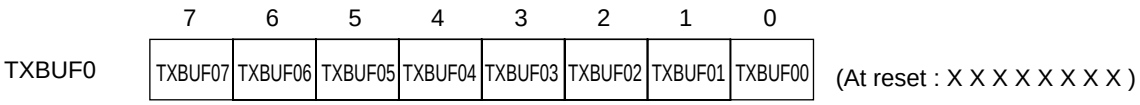


Figure 11-2-2 Serial Interface 0 Transmission Data Buffer (TXBUF0 : x'03F91', R/W)

11-2-3 Serial Interface 0 Mode Registers

■Serial Interface 0 Mode Register 0 (SC0MD0)

	7	6	5	4	3	2	1	0
SC0MD0	SC0CE1	SC0REN	SC0TRN	SC0DIR	SC0STE	SC0LNG2	SC0LNG1	SC0LNG0

(At reset : 0 0 0 0 0 1 1 1)

SC0LNG2	SC0LNG1	SC0LNG0	Synchronous serial transfer bit count
0	0	0	1bit
		1	2bit
	1	0	3bit
		1	4bit
1	0	0	5bit
		1	6bit
	1	0	7bit
		1	8bit

SC0STE	Synchronous serial transfer start condition
0	Disable start condition
1	Enable start condition

SC0DIR	First bit to be transferred
0	MSB first
1	LSB first

SC0TRN	Transmission data polarity change
0	Positive
1	Negative

SC0REN	Reception data polarity change
0	Positive
1	Negative

SC0CE1	Transmission data output edge	Reception data input edge
0	falling	rising
1	rising	falling

Figure 11-2-3 Serial Interface 0 Mode Register 0 (SC0MD0 : x'03F92', R/W)

■Serial Interface 0 Mode Register 1 (SC0MD1)

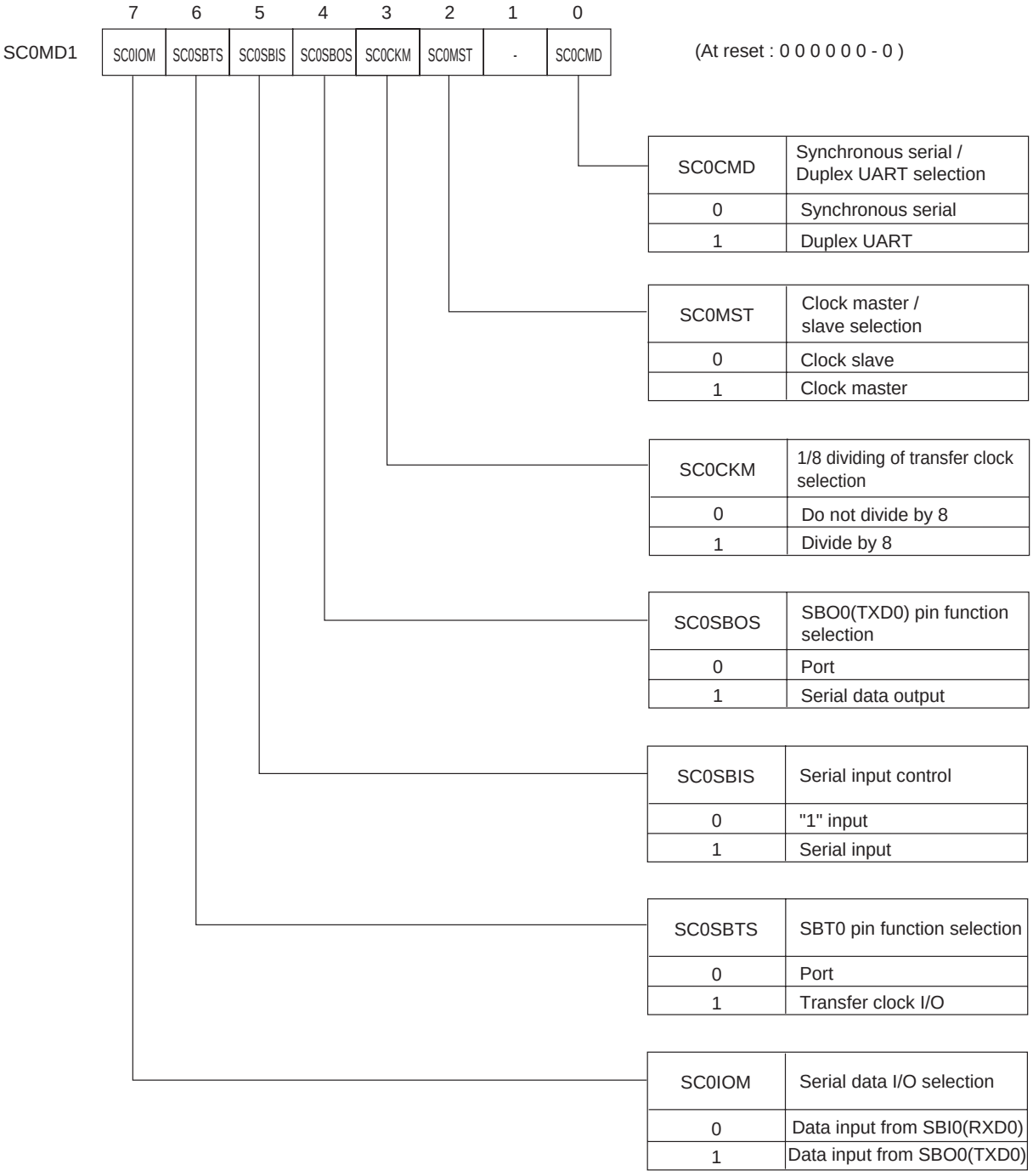


Figure 11-2-4 Serial Interface 0 Mode Register 1 (SC0MD1 : x'03F93', R/W)

■Serial Interface 0 Mode Register 2 (SC0MD2)

SC0BRKF flag is only for reading.

	7	6	5	4	3	2	1	0
SC0MD2	SC0FM1	SC0FM0	SC0PM1	SC0PM0	SC0NPE	-	SC0BRKF	SC0BRKE

(At reset : 0 0 0 0 0 - 0 0)

SC0BRKE	Break status transmit control
0	Data transmission
1	Break transmission

SC0BRKF (*)	Break status receive monitor
0	Data tramsmission
1	Break transmission

(*) Only read access is available.

SC0NPE	Parity enable
0	Enable parity bit
1	Disable parity bit

SC0PM1	SC0PM0	Added bit specification	
		Transmission	Reception
0	0	Add "0"	Check for "0"
	1	Add "1"	Check for "1"
1	0	Add odd parity	Check for odd parity
	1	Add even parity	Check for even parity

SC0FM1	SC0FM0	Frame mode specification
0	0	7 data bits + 1 stop bit
	1	7 data bits + 2 stop bits
1	0	8 data bits + 1 stop bit
	1	8 data bits + 2 stop bits

Figure 11-2-5 Serial Interface 0 Mode Register 2 (SC0MD2 : x'03F94', R/W)

■Serial Interface 0 Mode Register 3 (SC0MD3)

All flags are only for reading.

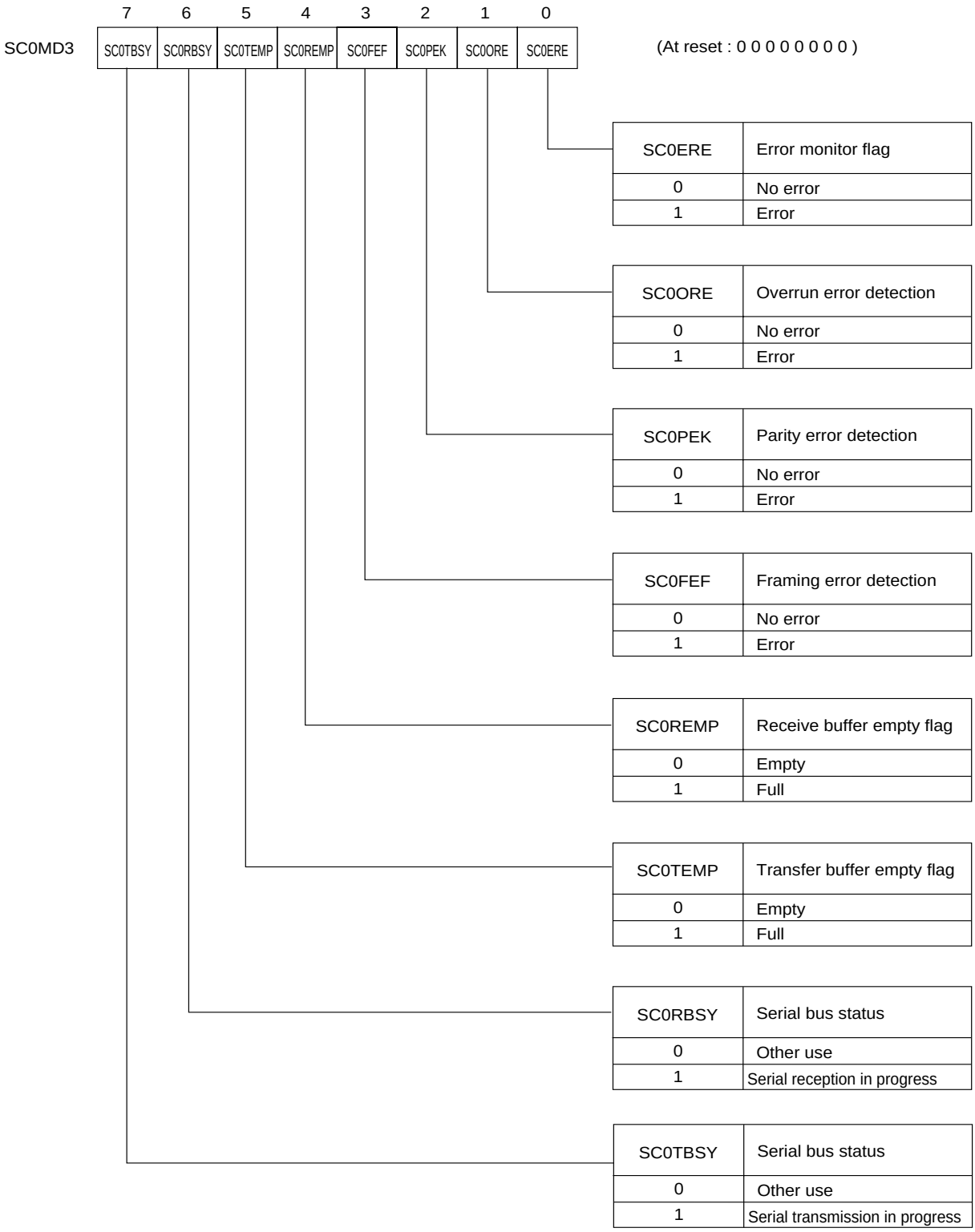


Figure 11-2-6 Serial Interface 0 Mode Register 3 (SC0MD3 : x'03F95', R)

■Serial Interface 0 Port Control Register (SC0ODC)

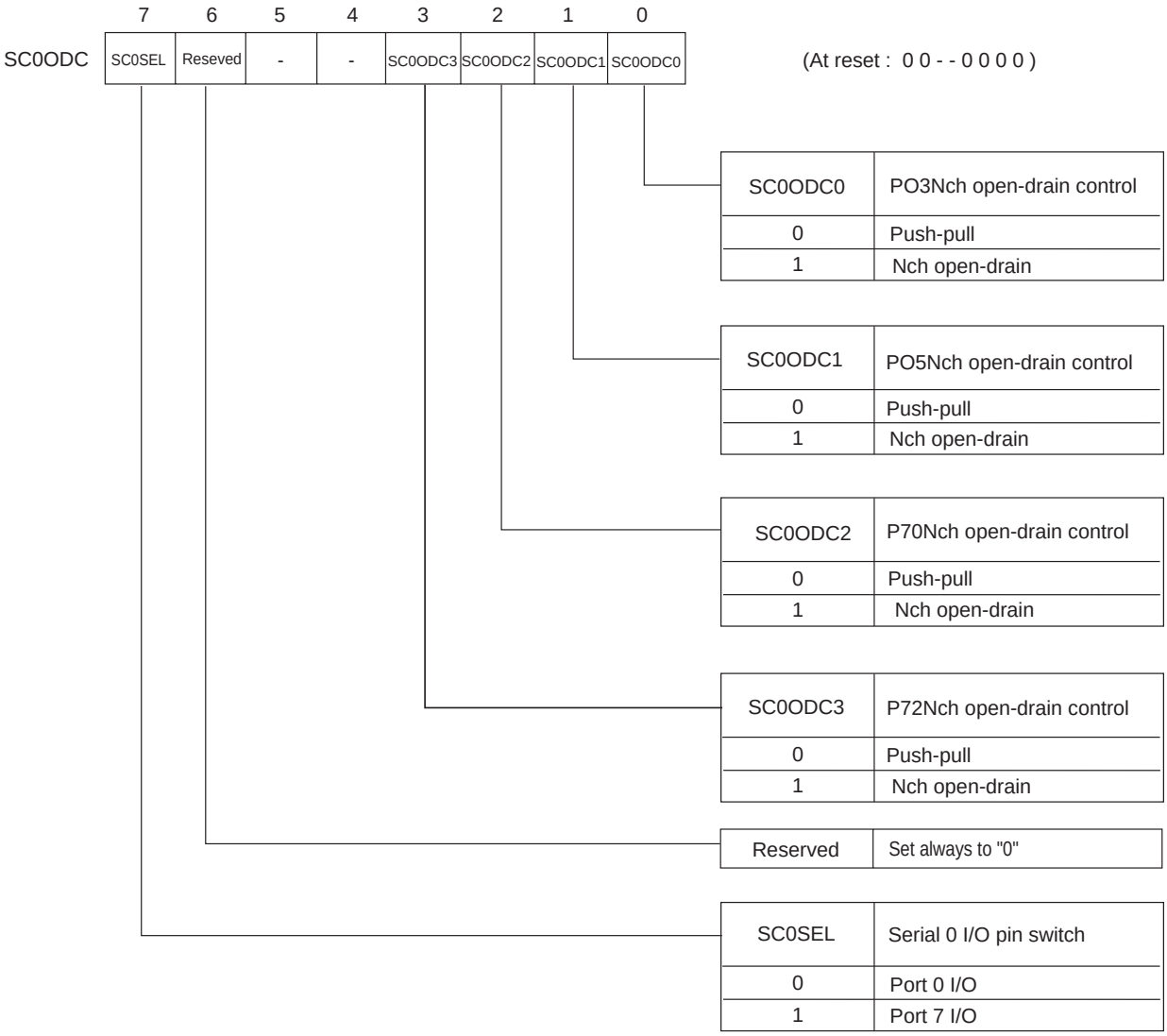


Figure 11-2-7 Serial Interface 0 Port Control Register (SC0ODC : x'03F96', R/W)

■Serial Interface 0 Transfer Clock Selection Register (SC0CKS)

	7	6	5	4	3	2	1	0	
SC0CKS	-	-	-	-	-	SC0PSC2	SC0PSC1	SC0PSC0	(At reset : - - - - - X X X)

SC0PSC2	SC0PSC1	SC0PSC0	Clock selection
0	0	0	fosc/2
		1	fosc/4
	1	0	fosc/16
		1	fosc/64
1	0	0	fs/2
		1	fs/4
	1	X	Timer 5 output

Figure 11-2-8 Serial Interface 0 Tranfer Clock Selection Register (SC0CKS : x'03F97', R/W)

11-2-4 Serial Interface 1 Data Buffer Registers

Serial Interface 1 has each 8-bit data buffer register for transmission, and for reception.

■Serial Interface 1 Reception Data Buffer (RXBUF1)

	7	6	5	4	3	2	1	0	
RXBUF1	RXBUF17	RXBUF16	RXBUF15	RXBUF14	RXBUF13	RXBUF12	RXBUF11	RXBUF10	(At reset : X X X X X X X X)

Figure 11-2-9 Serial Interface 1 Reception Data Buffer (RXBUF1 : x'03F98', R)

■Serial Interface 1 Transmissin Data Buffer (TXBUF1)

	7	6	5	4	3	2	1	0	
TXBUF1	TXBUF17	TXBUF16	TXBUF15	TXBUF14	TXBUF13	TXBUF12	TXBUF11	TXBUF10	(At reset : X X X X X X X X)

Figure 11-2-10 Serial Interface 1 Transmission Data Buffer (TXBUF1 : x'03F99', R/W)

11-2-5 Serial Interface 1 Mode Registers

■Serial Interface1 Mode Register 0 (SC1MD0)

	7	6	5	4	3	2	1	0
SC1MD0	SC1CE1	SC1REN	SC1TRN	SC1DIR	SC1STE	SC1LNG2	SC1LNG1	SC1LNG0

(At reset : 0 0 0 0 0 1 1 1)

SC1LNG2	SC1LNG1	SC1LNG0	Synchronous serial transfer bit count
0	0	0	1bit
		1	2bit
	1	0	3bit
		1	4bit
1	0	0	5bit
		1	6bit
	1	0	7bit
		1	8bit

SC1STE	Synchronous serial transfer start condition
0	Disable start condition
1	Enable start condition

SC1DIR	First bit to be transferred
0	MSB first
1	LSB first

SC1TRN	Transmission data polarity change
0	Positive
1	Negative

SC1REN	Reception data polarity change
0	Positive
1	Negative

SC1CE1	Transmission data output edge	Reception data input edge
0	falling	rising
1	rising	falling

Figure 11-2-11 Serial Interface 1 Mode Register 0 (SC1MD0 : x'03F9A', R/W)

■Serial Interface 1 Mode Register 1 (SC1MD1)

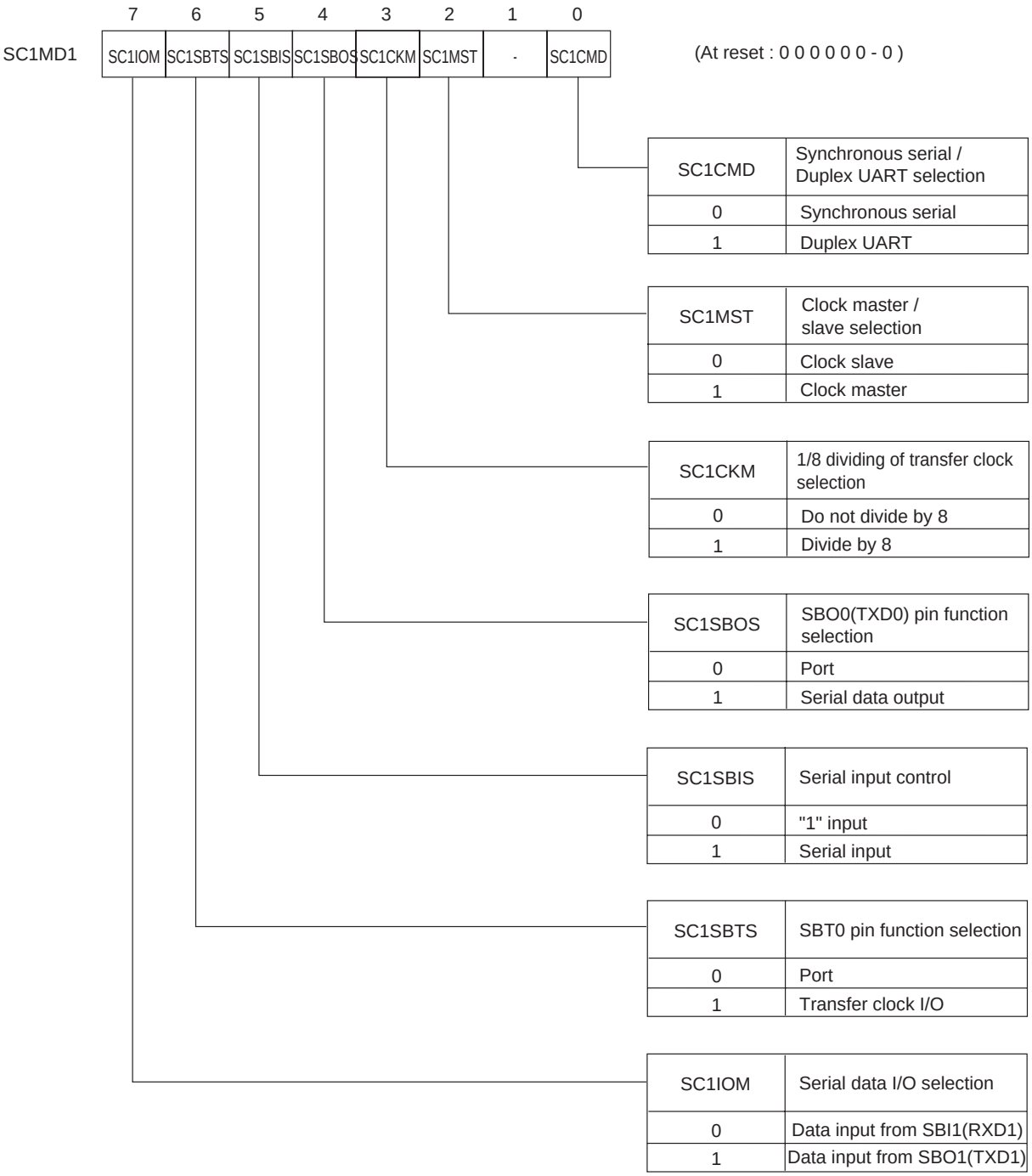
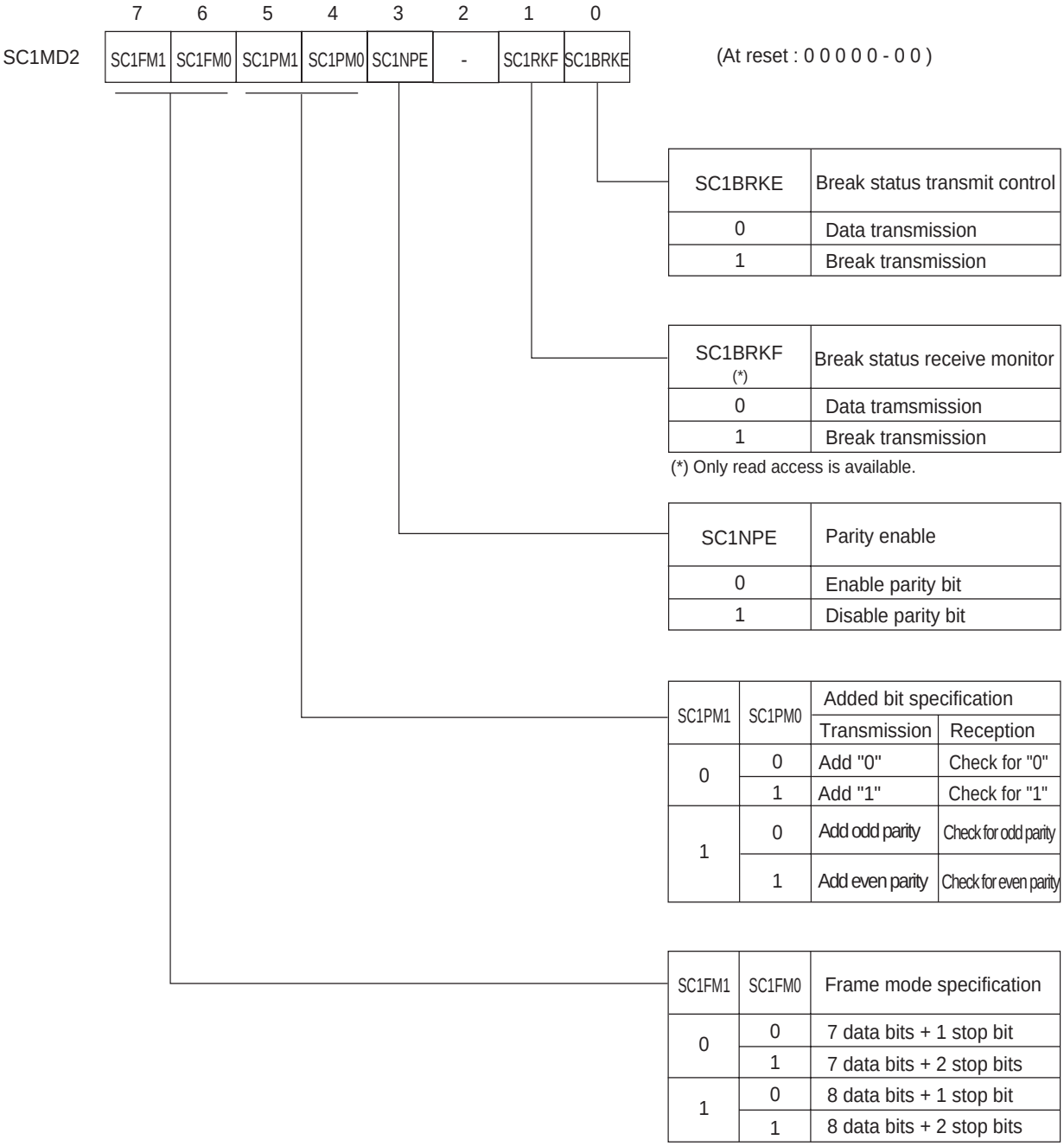


Figure 11-2-12 Serial Interface 1 Mode Register 1 (SC1MD1 : x'03F9B', R/W)

■Serial Interface 1 Mode Register 2 (SC1MD2)

SC1BRKF flag is only for reading.



SC1BRKE	Break status transmit control
0	Data transmission
1	Break transmission

SC1BRKF (*)	Break status receive monitor
0	Data tramsmission
1	Break transmission

(*) Only read access is available.

SC1NPE	Parity enable
0	Enable parity bit
1	Disable parity bit

SC1PM1	SC1PM0	Added bit specification	
		Transmission	Reception
0	0	Add "0"	Check for "0"
	1	Add "1"	Check for "1"
1	0	Add odd parity	Check for odd parity
	1	Add even parity	Check for even parity

SC1FM1	SC1FM0	Frame mode specification
0	0	7 data bits + 1 stop bit
	1	7 data bits + 2 stop bits
1	0	8 data bits + 1 stop bit
	1	8 data bits + 2 stop bits

Figure 11-2-13 Serial Interface 1 Mode Register 2 (SC1MD2 : x'03F9C', R/W)

■Serial Interface 1 Mode Register 3 (SC1MD3)

All flags are only for reading.

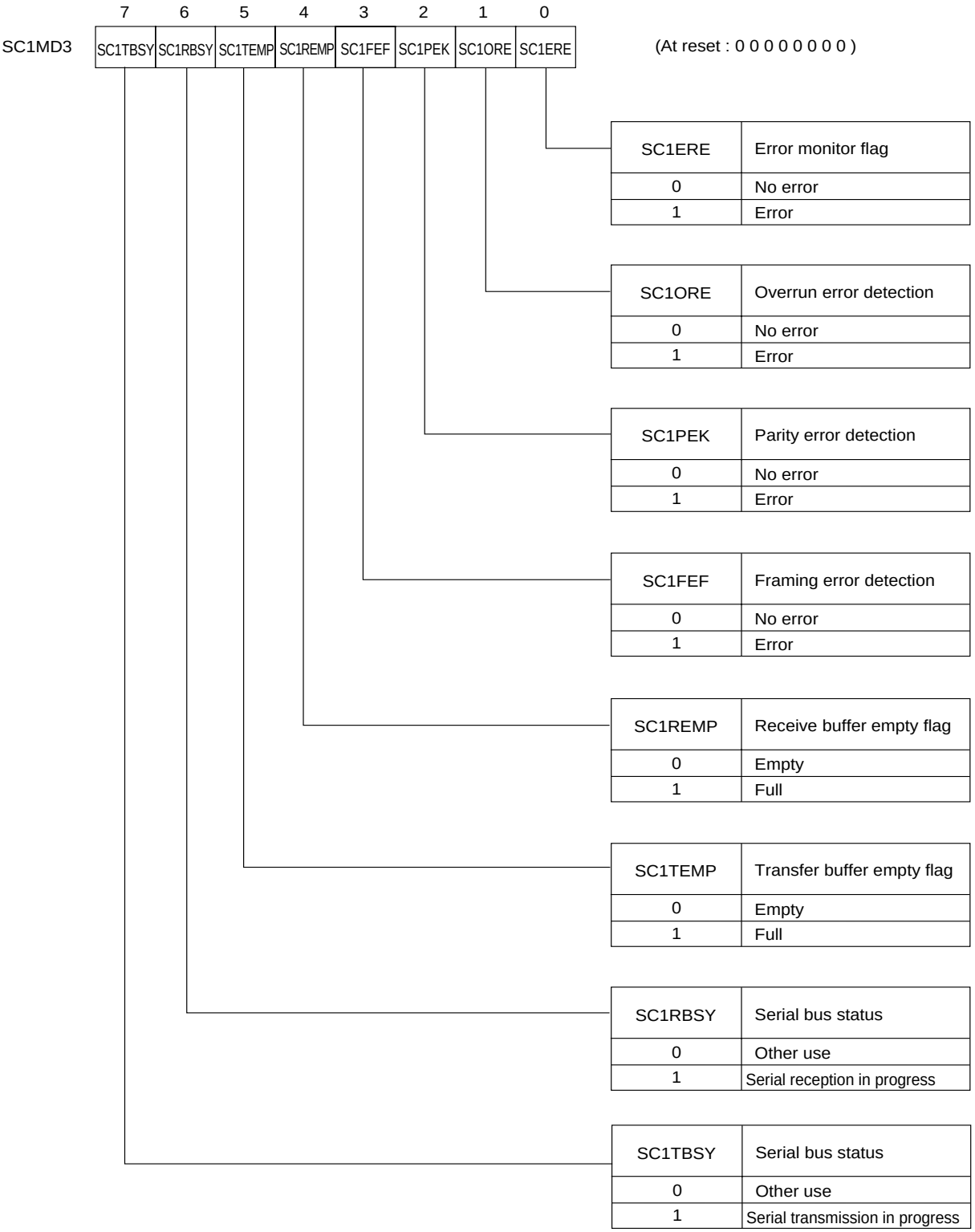


Figure 11-2-14 Serial Interface 1 Mode Register 3 (SC1MD3 : x'03F9D', R)

■Serial Interface 1 Port Control Register (SC1ODC)

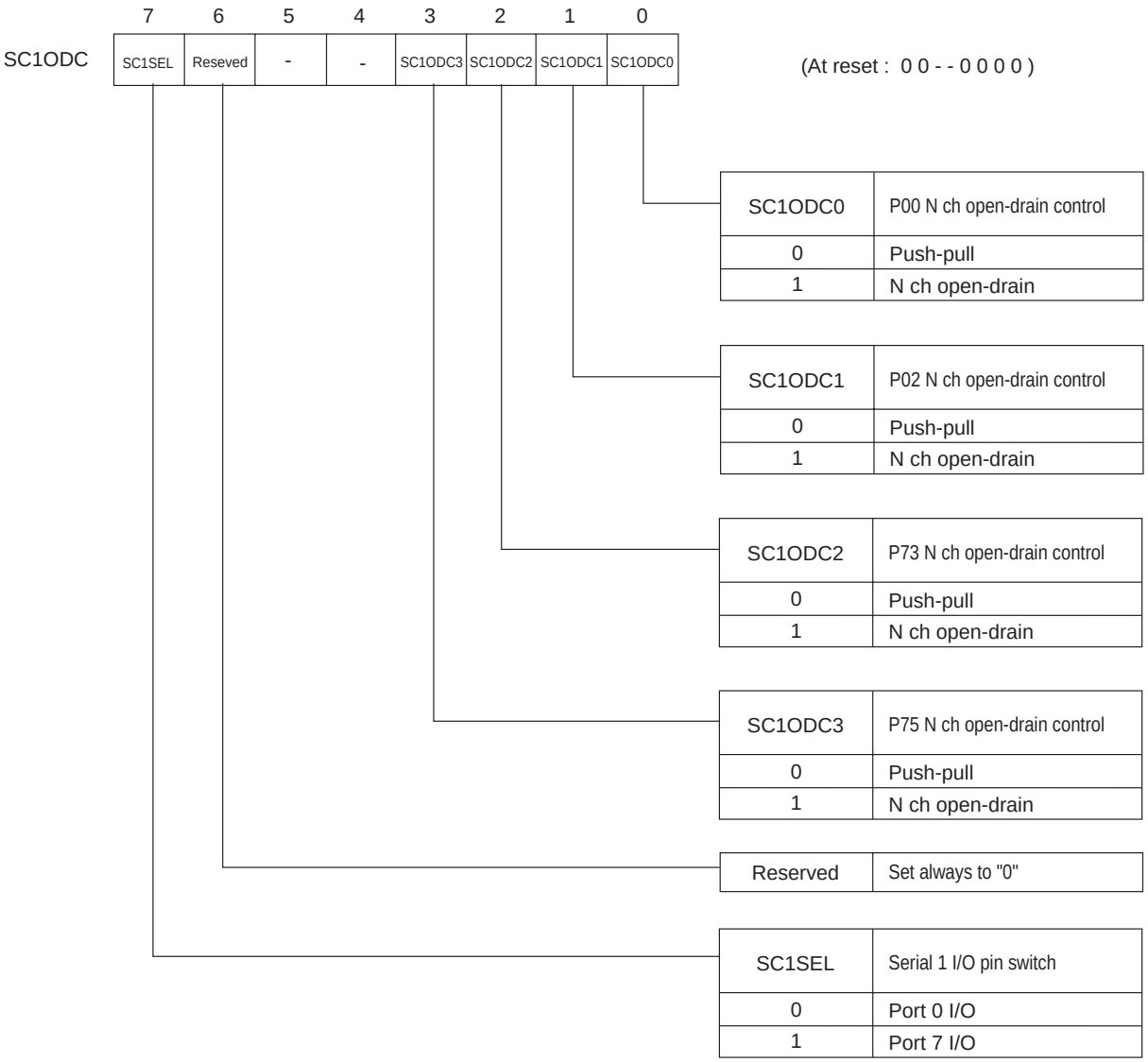


Figure 11-2-15 Serial Interface 1 Port Control Register (SC1ODC : x'03F9E', R/W)

When port 7 is used as a pin for serial interface 1 and port 0 is used as the general port, P00 or P02 should be used as input port.

■Serial Interface1 Transfer Clock Selection Register (SC1CKS)

	7	6	5	4	3	2	1	0	
SC1CKS	-	-	-	-	-	SC1PSC2	SC1PSC1	SC1PSC0	(At reset : - - - - - X X X)

SC1PSC2	SC1PSC1	SC1PSC0	Clock selection
0	0	0	fosc/2
		1	fosc/4
	1	0	fosc/16
		1	fosc/64
1	0	0	fs/2
		1	fs/4
	1	X	Timer 4 output

Figure 11-2-16 Serial Interface 1 Tranfer Clock Selection Register (SC1CKS : x'03F9F', R/W)

11-3 Operation

Serial Interface 0, 1 can be used for both clock synchronous and duplex UART.

11-3-1 Clock Synchronous Serial Interface

■Activation Factor for Communication

Table 11-3-1 shows activation factors for communication. At master, the transfer clock is generated by setting data to the transmission data buffer TXBUFn, or by receiving a start condition. Except during communication, the input signal from SBT0 pin is masked to prevent errors by noise or so. This mask can be released automatically by setting a data to TXBUFn(access to the TXBUFn register), or by inputting a start condition to the data input pin. Therefore, at slave, set data to TXBUFn, or input an external clock after a start condition is input.

Table 11-3-1 Synchronous Serial Interface Activation Factor

	Activation factor	
	Transmission	Reception
at master	Set transmission data	Set dummy data
		Input start condition
at slave	Input clock after transmission data is set	Input clock after dummy data is set
		Input clock after start condition is input

■Transfer Bit Setup

The transfer bit count is selected from 1 bit to 8 bits. Set them by the SCnLNG 2 to 0 flag of the SCnMD0 register (at reset : 111). The SCnLNG 2 to 0 flag holds the former set value until it is set again.

Except during communication, SBT pin is masked to prevent errors by noise. At slave communication, set data to TXBUFn or input a clock to SBT pin after a start condition is input.

■Start Condition Setup

The SCnSTE flag of the SCnMD0 register sets if a start condition is enabled or not. If a start condition is enabled, and received at communication, a bit counter is cleared to restart the communication. The start condition, if the SCnCE1 flag of the SCnMD0 register is set to "0", is regarded when a data line (SBI pin (with 3 channels) or SBO pin (with 2 channels) is changed from "H" to "L" as a clock line (SBT pin) is "H". Also, the start condition, if the SCnCE1 flag of the SCnMD0 register is set to "1", is regarded when a data line (SBI pin (with 3 channels) or SBO pin (with 2 channels) is changed from "H" to "L" as a clock line (SBT pin) is "L". Both the SCnSBOS flag and the SCnSBIS flag of the SCnMD1 register should be set to "0", before the start condition setup is changed

■First Transfer Bit Setup

The SCnDIR flag of the SCnMD0 register can set the first transfer bit. MSB first or LSB first can be selected.

■Transmission Data Buffer

The transmission data buffer, TXBUFn is the sub buffer that stores data to load the internal shift register. Data to be transfered should be set to the transmission data buffer, TXBUFn to load to the internal shift register automatically. The first data loading to the internal shift register is done at the same timing of the data setting to TXBUFn.

■Received Data Buffer

The received data buffer RXBUFn is the sub buffer that pushed the received data in the internal shift register. After the communication complete interrupt SCnIRQ is generated, data stored in the internal shift register is stored to the received data buffer RXBUFn automatically. RXBUFn can store data up to 1 byte. RXBUFn is rewritten in every communication complete, so read out data of RXBUFn till the next receive complete. The received data buffer empty flag SCnREMP is set to "1" at the same time SCnTIRQ is generated. SCnREMP is cleared to "0" after RXBUFn is read.

If a start condition is input to restart during communication, the transmission data is not valid. If the transmission should be operated again, set the transmission data to TXBUFn, again.

Start condition should be switched after both the SCnSBOS and the SCnSBIS flags of the SCnMD1 register are set to "0". If they are not set to "0", the switching is not valid.

RXBUFn is rewritten in every communication complete. At continuous communication, data of RXBUFn should be read out till the next reception complete.

■Tranfer Bit Count and First Transfer Bit

When the transfer bit is 1 bit to 7 bits, the data storing method to the transmission data buffer TXBUFn is different, depending on the first transfer bit selection. At MSB first, use the upper bits of TXBUFn for storing. When there are 6 bits to be transfered, as shown on figure 11-3-1, if data "A" to "F" are stored to bp2 to bp7 of TXBUFn, the transmission is operated from "F" to "A". At LSB first, use the lower bits of TXBUFn for storing. When there are 6 bits to be transfered, as shown on figure 11-3-2, if data "A" to "F" are stored to bp0 to bp5 of TXBUFn, the transmission is operated from "A" to "F".

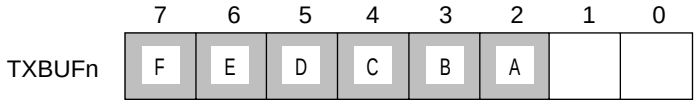


Figure 11-3-1 Transfer Bit Count and First Transfer Bit (starting with MSB)

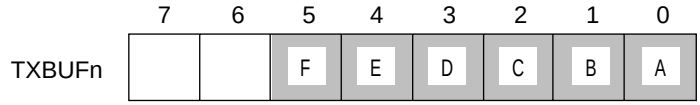


Figure 11-3-2 Transfer Bit Count and First Transfer Bit (starting with LSB)

■Receive Bit Count and First Transfer Bit

When the transfer bit count is 1 bit to 7 bits, the data storing method to the received data buffer RXBUFn is different depending on the first transfer bit selection. At MSB first, data are stored to the lower bits of RXBUFn. When there are 6 bits to be transfered, as shown on figure 11-3-3, if data "F" to "A" are stored to bp0 to bp5 of RXBUFn. At LSB first, data are stored to the upper bits of RXBUFn. When there are 6 bits to be transfered, as shown on figure 11-3-4, if data "A" to "F" are stored to bp2 to bp7 of RXBUFn.

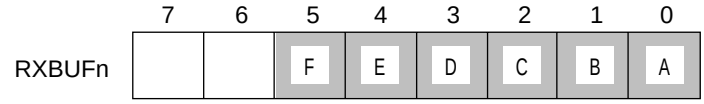


Figure 11-3-3 Receive Bit Count and Transfer First Bit (starting with MSB bit)

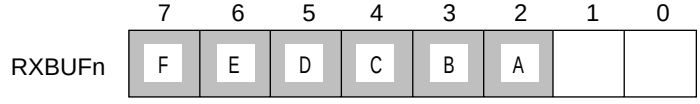


Figure 11-3-4 Receive Bit Count and Transfer First Bit (starting with LSB bit)

■Continuous Communication

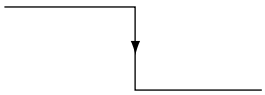
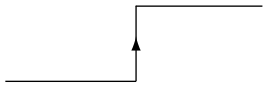
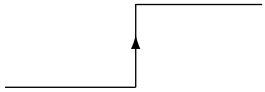
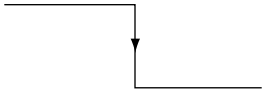
This serial has a function for continuous communication. If data is set to the transmission data buffer TXBUFn during communication, the transmission buffer empty flag SCnTEMP is automatically set to communicate continuously. Data setup to TXBUFn should be done till the communication complete interrupt SCnTIRQ is generated after the former data is set. At master communication, there is a suspension of communication for 3 transfer clocks till the next transmission clock is output after the SCnIRQ generation.

Also, the built-in automatic data transfer fuction ATC can activate. Data can be transfered continuously up to 255 bytes by ATC activation. In this case, there is a suspension of communication for up to 18 machine cycles + 2.5 transfer clocks. Refer to the transfer mode 8 to 9 in chapter 15, automatic transfer controller for ATC activation.

■Input Edge / Output Edge Setup

The SCnCE1 to 0 flag of the SCnMD0 register set an output edge of the transmission data, an input edge of the received data. As the SCnCE1 flag = "0", the transmission data is output at the falling edge, and as "1", output at the rising edge. As SCnCE1="0", the received data is received at the inversion edge to the output edge of transmission data, and as "1", stored at the same edge.

Table 11-3-2 Transmission Data Output Edge and Received Data Input Edge

SCnCE1	Transmission data output edge	Received data input edge
0		
1		

■Transmission/reception data polarity switching

Polarity of transmission/reception data can be switched by register setup. When SCnREN flag of the SCnMD0 register is set to "1", inverted input signal from data input pin is input to the reception shift register. When SCnTRN flag of the SCnMD0 register is set to "1", inverted signal set in the transfer buffer TXBUFn is output to the data output pin.

■Clock Setup

The SCnCKS register selects a clock source from the special prescaler and timer 4 output. The special prescaler starts its operation after the PSCMD (x'03F6F') register selects "prescaler operation". The SCnMST flag of the SCnMD1 register can select the internal clock (clock master), or the external clock (clock slave). Even if the external clock is selected, set the internal clock that has the same clock cycle or below to the external clock, by the SCnCKS register. That is happened, because the interrupt flag SCnTIRQ is generated by the internal clock. Here is the internal clock source that can be set by the SCnCKS register. Also, the SCnCKM flag of the SCnMD1 register can divide the internal clock by 8.

Table 11-3-3 Synchronous Serial Interface Internal Clock Source

	Serial interface 0	Serial interface 1
Internal clock	fosc/2	fosc/2
	fosc/4	fosc/4
	fosc/16	fosc/16
	fosc/64	fosc/64
	fs/2	fs/2
	fs/4	fs/4
	Timer 5 output	Timer 4 output

■Data Input Pin Setup

3 channels type (clock pin (SBT pin), data output pin (SBO pin), data input pin (SBI pin)) or 2 channels type (clock pin (SBT pin), data I/O pin (SBO pin)) can be selected as the communication. SBI pin can be used for only serial data input. SBO pin can be used for serial data input or output. The SCnIOM flag of the SCnMD1 register can select if the serial data is input from SBI pin or SBO pin. When "data input from SBO pin" is selected to set the 2 channels type, the PnDIR0 flag of the PnDIR register controls direction of SBO pin to switch transmission / reception. At that time, SBI pin is free to be used as a general port.

The transfer speed should be up to 2.5 MHz. If the transfer clock is over 2.5 MHz, the transmission data may not be sent correctly.

At reception, if SCnIOM of the SC0MD1 register is set to "1" and "serial data input from SBO" is selected, SBI pin is used as a general port.

■Received Buffer Empty Flag

When the reception is completed (the last data reception edge of the clock is input), data is stored to RXBUFn from the internal shift register, automatically. If data is stored to the shift register RXBUFn, the received buffer empty flag SCnREMP of the SCnMD3 register is set to "1". That indicates that the received data is going to be read. SCnREMP is cleared to "0" by reading out the data of RXBUFn.

■Transmission Buffer Empty Flag

If any data is set to TXBUFn again, during communication (after setting data to TXBUFn before generating the communication complete interrupt SCnIRQ), the transmission buffer empty flag SCnTEMP of the SCnMD3 register is set to "1". That indicates that the next transmission data is going to load. Data is loaded to the inside shift register from TXBUFn by generation of SCnTIRQ, and the next transfer is started as SCnTEMP is cleared to "0".

■Overrun Error and Error Monitor Flag

If, after reception complete, the next data has been already received before reading out the data of the received data buffer RXBUFn, overrun error is generated and the SCnORE flag of the SCnMD3 register is set to "1". And at the same time, the error monitor flag SCnERE is set to indicate that something wrong on reception. The SCnORE flag holds the status unless the data of RXBUFn is read out. SCnERE is cleared as SCnORE flag is cleared. These error flags are nothing to do with communication operation.

■Reception BUSY Flag

When any data is set to TXBUFn or when the SCnSBIS flag of the SCnMD1 register is "1" as start condition is input, the SCnRBSY flag of the SCnMD3 register is set to "1". And, on the generation of the communication complete interrupt SCnTIRQ, the flag is cleared to "0". And, during continuous communication, the SCnRBSY falg is always set. If the transmission buffer empty flag SCnTEMP is cleared to "0" as the communication complete interrupt SCnTIRQ is generated, SCnRBSY is cleared to "0". If the SCnSBIS flag is set to "0" during communication, the SCnRBSY flag is cleared to "0".

■Transmission BUSY Flag

When any data is set to TXBUFn or when the SCnSBOS flag of the SCnMD1 register is "1" as start condition is input, the SCnTBSY flag of the SCnMD3 register is set to "1". And, on the generation of the communication complete interrupt SCnTIRQ, the flag is cleared to "0". And, during continuous communication, the SCnTBSY flag is always set. If the transmission buffer empty flag SCnTEMP is cleared to "0" as the communication complete interrupt SCnTIRQ is generated, SCnTBSY is cleared to "0". If the SCnSBOS flag is set to "0" during communication, the SCnTBSY flag is cleared to "0".

■Emergency Reset

It is possible to shut down communication. For a forced reset, the SCnSBOS flag and the SCnSBIOS flag of the SCnMD1 register should be set to "0" (SBO pin : port, input data : "1" input). At forced reset, the status registers (the SCnBRKF flag of the SCnMD2 register, all flags of the SCnMD3 register) are initialized as they are set at reset, but the control register holds the setting value.

■Last Bit of Transfer Data

Table 11-3-4 shows the data output holding period of the last bit at transmission, and the minimum data input period of the last bit at reception. After data output holding period of the last bit, "H" is output.

Table 11-3-4 Last Bit Data Length of Transfer Data

	The last bit data holding period at transmission	The last data input period at reception
At master	1 bit data length	1 bit data length (Minimum)
At slave	[1 bit data length of external clock x 1/2] + [internal clocl frequency x (1/2 to 3/2)]	

■Other Control Flag Setup

Table 11-3-5 shows flags that are not used at clock synchronous communication. So, they are not needed to set or monitor.

Table 11-3-5 Other Control Flag

Register	Flag	Detail
SCnMD2	SCnBRKF	Brake status reception monitor
	SCnNPE	Parity is enabled
	SCnPM1 to 0	Added bit specification
	SCnFM1 to 0	Frame mode specification
SCnMD3	SCnPEK	Parity error detection
	SCnFEF	Frame error detection

■Trasnmission Timing

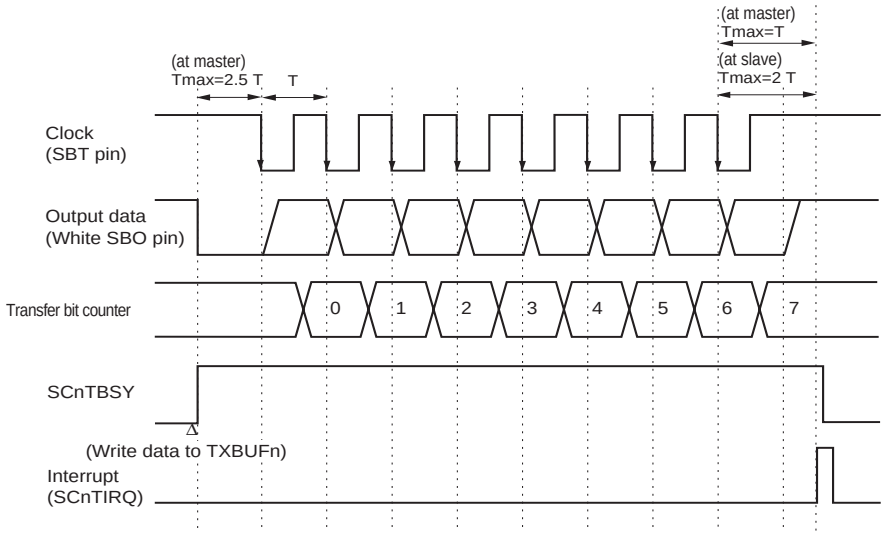


Figure 11-3-5 Transmission Timing (falling edge, start condition is enabled)

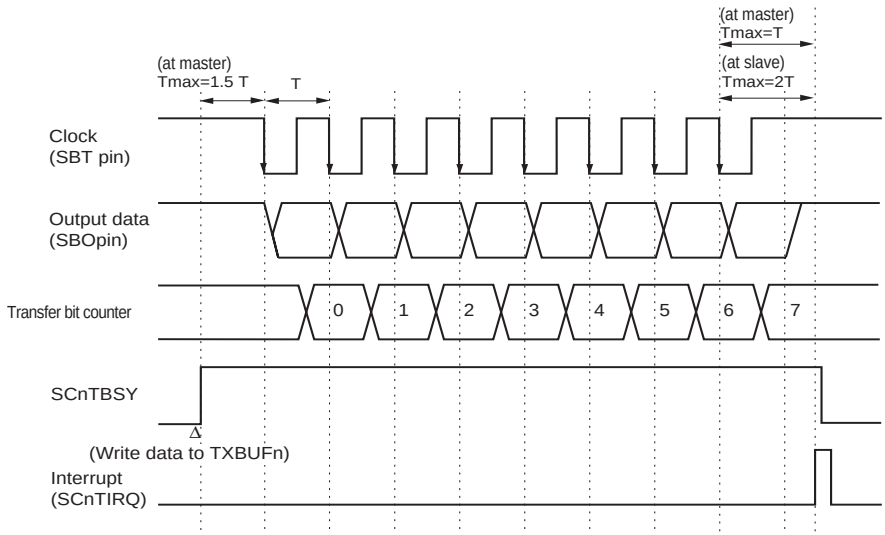


Figure 11-3-6 Transmission Timing (falling edge, start condition is disabled)

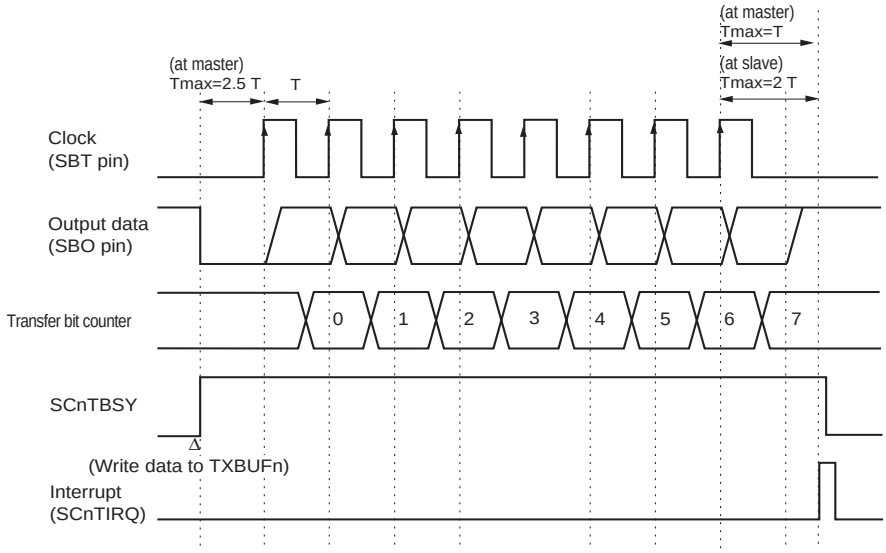


Figure 11-3-7 Transmission Timing (rising edge, start condition is enabled)

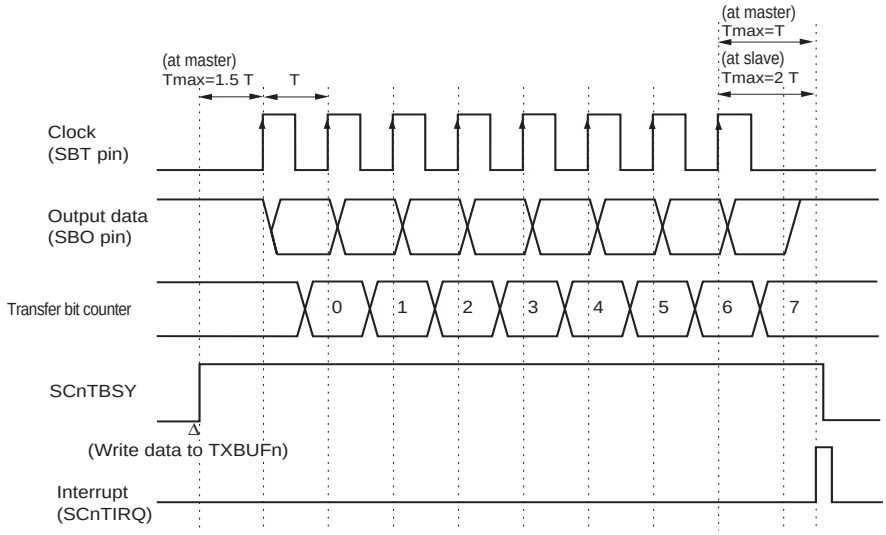


Figure 11-3-8 Transmission Timing (rising edge, start condition is disabled)

■Reception Timing

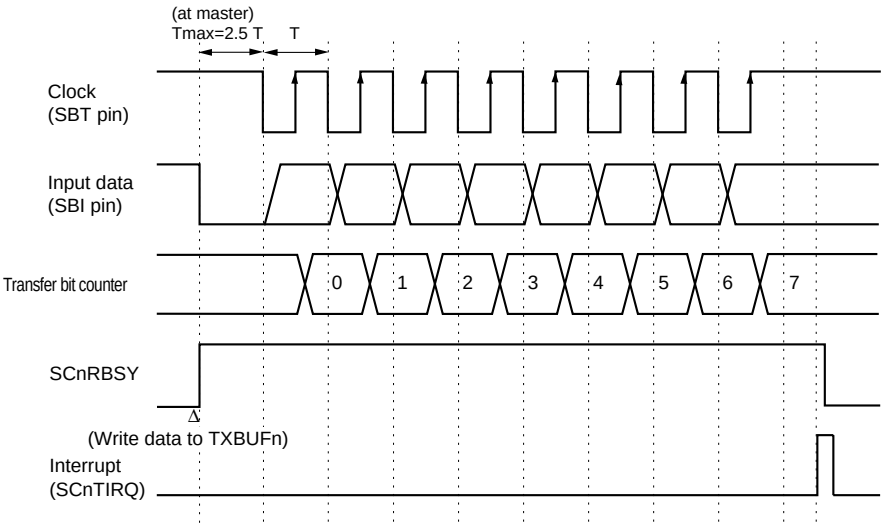


Figure 11-3-9 Reception Timing (rising edge, start condition is enabled)

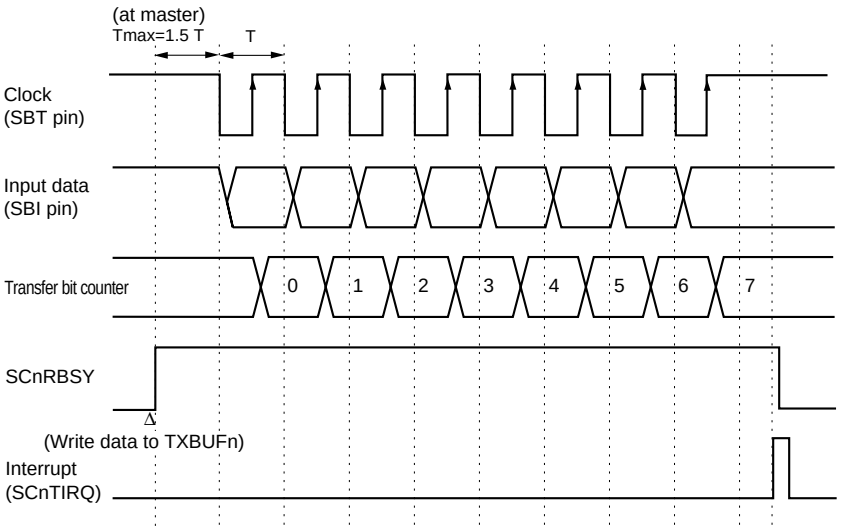


Figure 11-3-10 Reception Timing (rising edge, start condition is disabled)

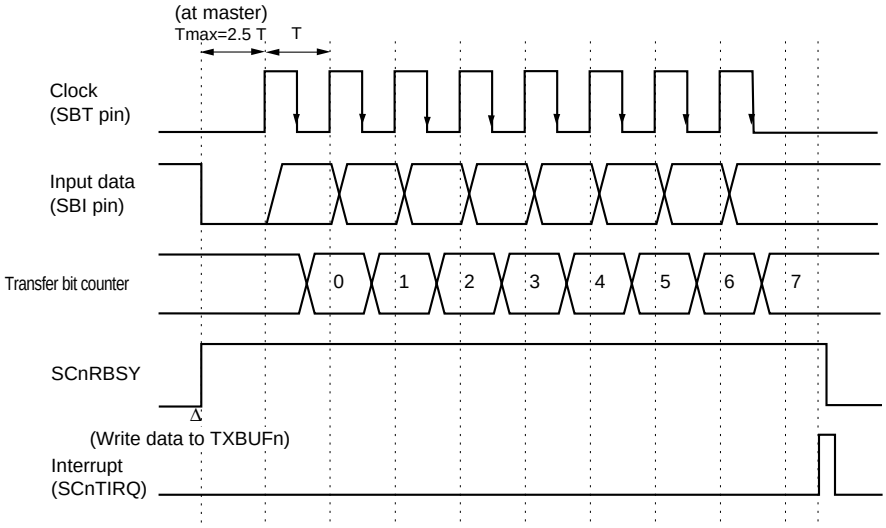


Figure 11-3-11 Reception Timing (falling edge, start condition is enabled)

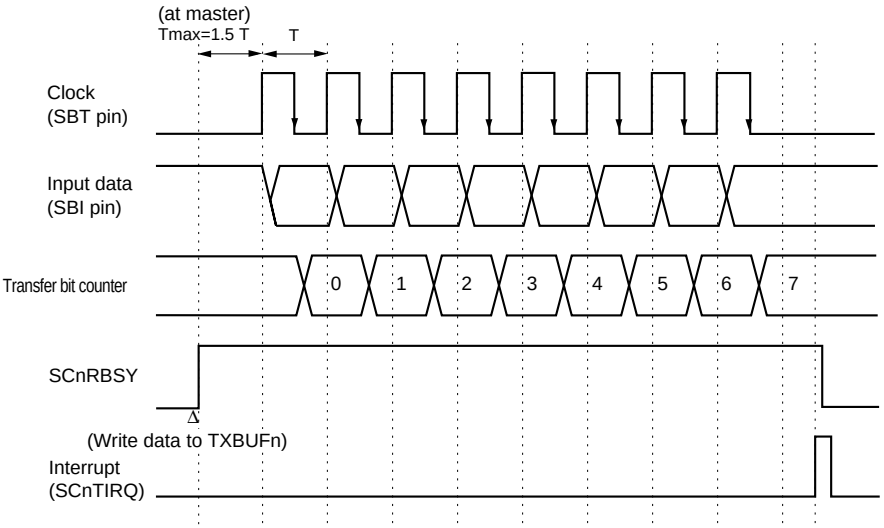


Figure 11-3-12 Reception Timing (falling edge, start condition is disabled)

■Transmission / Reception Timing

When transmission and reception are operated at the same time, set the SCnCE1 flag of the SCnMD0 register to "0" or "1". Data is received at the opposite edge of the transmission clock, so that the reception clock should be the opposite edge of the transmission clock from the other side.

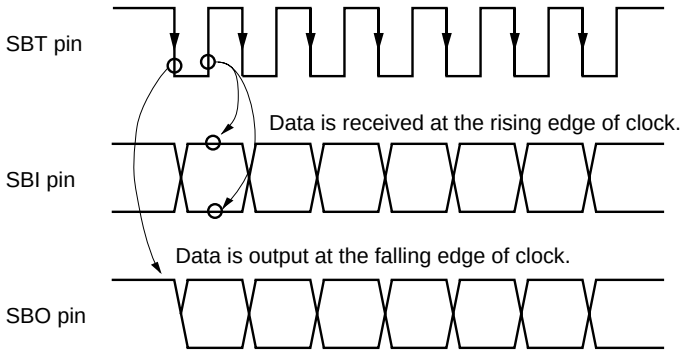


Figure 11-3-13 Transmission / Reception Timing (Reception : rising edge, Transmission : falling edge)

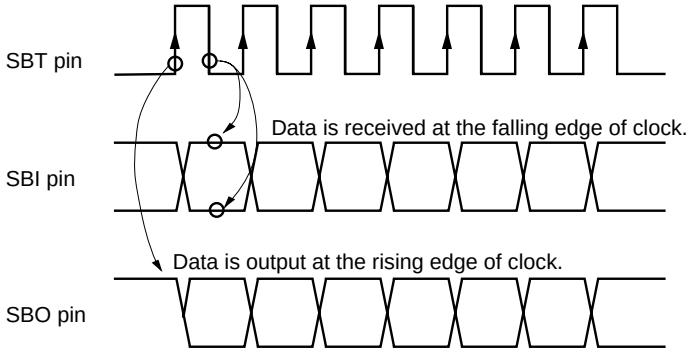


Figure 11-3-14 Transmission / Reception Timing (Reception : falling edge, Transmission : rising edge)

11-3-2 Serial interface 0 Synchronous Serial Interface Pin Setup

■Serial Interface 0 Pins Setup (3 channels, at transmission)

Table 11-3-6 shows the setup for synchronous serial interface pin with 3 channels (SBO0 pin, SBI0 pin, SBT0 pin) at transmission.

Table 11-3-6 Setup for Synchronous Serial Interface 0 Pin (3 channels, at transmission)

Setup item	Data output pin	Data input pin	Clock I/O pin	
	SBO0A pin/ SBO0B pin	SBI0A pin/ SBI0B pin	SBT0A pin/SBT0B pin	
			Internal clock	External clock
Port Pin	P03/P70	P04/P71	P05/P72	
Port Pin Setup	Select used pin (A, B)			
	SC0ODC (SC0SEL)			
SBI / SBO pin Setup	SBI0/SBO0 independent		-	
	SC0MD1 (SC0IOM)			
Function	Serial data output	"1" input	Serial clock I/O	Serial clock I/O
	SC0MD1(SC0SBOS)	SC0MD1(SC0SBIS)	SC0MD1 (SC0SBTS)	
Style	Push-pull / Nch open-drain	-	Push-pull / Nch open-drain	Push-pull / Nch open-drain
	SC0ODC(SC0ODC0) SC0ODC(SC0ODC2)		SC0ODC (SC0ODC1)/SC0ODC (SC0ODC3)	
I/O	Output mode	-	Output mode	Input mode
	P0DIR (P0DIR3) P7DIR (P7DIR0)		P0DIR (P0DIR5) P7DIR (P7DIR2)	
Pull-up (Pull-down) setup	Add/Not Add	-	Add/Not Add	Add/Not Add
	P0PLU (P0PLU3) P7PLUD(P7PLUD0)		P0PLU (P0PLU5) P7PLUD (P7PLUD2)	

Note) Select pull-up/down resistor with P7RDOWN flag of FLOAT register (x'03F2E')
[☞ Chapter4, 4.7.2 Register]

■Serial Interface 0 Pins Setup (3 channels, at reception)

Table 11-3-7 shows the setup for synchronous serial interface pin with 3 channels (SBO0 pin, SBI0 pin, SBT0 pin) at reception.

Table 11-3-7 Setup for Synchronous Serial Interface 0 Pin (3 channels, at reception)

Setup item	Data input pin		Clock I/O pin	
	SBO1A pin/ SBO1B pin	SBI1A pin/ SBI1B pin	SBT1A pin/SBT1B pin	
			Internal clock	External clock
Port Pin	P00/P73	P01/P74	P02/P75	
Port Pin Setup	Select used pin (A, B)			
	SC1ODC (SC1SEL)			
SBI / SBO pin Setup	SBI0/SBO0 connection		-	
	SC0MD1 (SC0IOM)			
Function	Port	Serial data input	Serial clock I/O	Serial clock I/O
	SC0MD1(SC0SBOS)	SC0MD1(SC0SBIS)	SC0MD1 (SC0SBTS)	
Style	-	-	Push-pull / Nch open-drain	Push-pull / Nch open-drain
			SC1ODC (SC1ODC1)/SC1ODC (SC1ODC3)	
I/O	-	Input mode	Output mode	Input mode
		P0DIR (P0DIR1) P7DIR (P7DIR4)	P0DIR (P0DIR2) P7DIR (P7DIR5)	
Pull-up (Pull-down) setup	-	-	Add/Not Add	Add/Not Add
			P0PLU (P0PLU2) P7PLUD (P7PLUD5)	

Note) Select pull-up/down resistor with P7RDOWN flag of FLOAT register (x'03F2E')
[☞ Chapter4, 4.7.2 Register]

■Serial Interface 0 Pins Setup (3 channels, at transmission / reception)

Table 11-3-8 shows the setup for synchronous serial interface pin with 3 lines (SBO0 pin, SBI0 pin, SBT0 pin) at transmission / reception.

Table 11-3-8 Setup for Synchronous Serial Interface 0 Pin (3 channels, at transmission / reception)

Setup item	Data input pin		Clock I/O pin	
	SBO0A pin/ SBO0B pin	SBI0A pin/ SBI0B pin	SBT0A pin/SBT0B pin	
			Internal clock	External clock
Port Pin	P03/P70	P04/P71	P05/P72	
Port Pin Setup	Select used pin (A, B)			
	SC0ODC (SC1SEL)			
SBI / SBO pin Setup	SBI0/SBO0 independent		-	
	SC0MD1 (SC0IOM)			
Function	Serial data output	Serial data input	Serial clock I/O	Serial clock I/O
	SC0MD1(SC0SBOS)	SC0MD1(SC0SBIS)	SC0MD1 (SC0SBTS)	
Style	Push-pull/ Nch open-drain	-	Push-pull / Nch open-drain	Push-pull / Nch open-drain
	SC0ODC (SC0ODC) SC0ODC (SC0ODC3)		SC0ODC (SC0ODC1)	
I/O	Output mode	Input mode	Output mode	Input mode
	P0DIR (P0DIR3) P7DIR (P7DIR0)	P0DIR (P0DIR4) P7DIR (P7DIR1)	P0DIR (P0DIR5) P7DIR (P7DIR2)	
Pull-up (Pull-down) setup	Add/Not Add	-	Add/Not Add	Add/Not Add
	P0PLU (P0PLU3) P7PLUD (P7PLUD0)		P0PLU (P0PLU5) P7PLUD (P7PLUD2)	

Note) Select pull-up/down resistor with P7RDOWN flag of FLOAT register (x'03F2E')
[☞ Chapter4, 4.7.2 Register]

■Serial Interface 0 Pins Setup (2 channels, at transmission)

Table 11-3-9 shows the setup for synchronous serial interface pin with 2 channels (SBO0 pin, SBT0 pin) at transmission. SBI0 pin can be used as a general port.

Table 11-3-9 Setup for Synchronous Serial Interface 0 Pin (2 channels, at transmission)

Setup item	Data output pin		Clock I/O pin	
	SBO0A pin/ SBO0B pin	SBI0A pin/ SBI0B pin	SBT0A pin/SBT0B pin	
			Internal clock	External clock
Port Pin	P03/P70		P05/P72	
Port Pin Setup	Select used pin (A, B)			
	SC0ODC (SC0SEL)			
SBI / SBO pin Setup	SBI0/SBO0 connection		-	
	SC0MD1 (SC0IOM)			
Function	Serial data output	"1" input	Serial clock I/O	Serial clock I/O
	SC0MD1(SC0SBOS)	SC0MD1(SC0SBIS)	SC0MD1 (SC0SBTS)	
Style	Push-pull / Nch open-drain	-	Push-pull / Nch open-drain	Push-pull / Nch open-drain
	SC0ODC(SC0ODC0) SC0ODC(SC0ODC2)		SC0ODC (SC0ODC1)/SC0ODC (SC0ODC3)	
I/O	Output mode	-	Output mode	Input mode
	P0DIR (P0DIR3) P7DIR (P7DIR0)		P0DIR (P0DIR5) P7DIR (P7DIR7)	
Pull-up (Pull-down) setup	Add/Not Add	-	Add/Not Add	Add/Not Add
	P0PLU (P0PLU3) P7PLUD(P7PLUD0)		P0PLU (P0PLU5) P7PLUD (P7PLUD2)	

Note) Select pull-up/down resistor with P7RDOWN flag of FLOAT register (x'03F2E')
[☞ Chapter4, 4.7.2 Register]

■Serial Interface 0 Pins Setup (2 channels, at reception)

Table 11-3-10 shows the setup for synchronous serial interface pin with 2 channels (SBO0 pin, SBT0 pin) at reception. SBI0 pin can be used as a general port.

Table 11-3-10 Setup for Synchronous Serial Interface 0 Pin (2 channels, at reception)

Setup item	Data input pin		Clock I/O pin	
	SBO0A pin/ SBO0B pin	SBI0A pin/ SBI0B pin	SBT0A pin/SBT0B pin	
			Internal clock	External clock
Port Pin	P03/P70		P05/P72	
Port Pin Setup	Select used pin (A, B)			
	SC0ODC (SC0SEL)			
SBI / SBO pin Setup	SBI0/SBO0 connection		-	
	SC0MD1 (SC0IOM)			
Function	Port	Serial data input	Serial clock I/O	Serial clock I/O
	SC0MD1(SC0SBOS)	SC0MD1(SC0SBIS)	SC0MD1 (SC0SBTS)	
Style	-	-	Push-pull / Nch open-drain	Push-pull / Nch open-drain
			SC0ODC (SC0ODC1)/SC0ODC (SC0ODC3)	
I/O	input mode	-	Output mode	Input mode
	P0DIR (P0DIR3) P7DIR (P7DIR0)		P0DIR (P0DIR5) P7DIR (P7DIR7)	
Pull-up (Pull-down) setup	-	-	Add/Not Add	Add/Not Add
			P0PLU (P0PLU5) P7PLUD (P7PLUD2)	

Note) Select pull-up/down resistor with P7RDOWN flag of FLOAT register (x'03F2E')
[☞ Chapter4, 4.7.2 Register]

11-3-3 Serial interface 1 Synchronous Serial Interface Pin Setup

■Serial Interface 1 Pins Setup (3 channels, at transmission)

Table 11-3-11 shows the setup for synchronous serial interface pin with 3 channels (SBO1 pin, SBI1 pin, SBT1 pin) at transmission.

Table 11-3-11 Setup for Synchronous Serial Interface 1 Pin (3 channels, at transmission)

Setup item	Data output pin	Data input pin	Clock I/O pin	
	SBO1A pin/ SBO1B pin	SBI1A pin/ SBI1B pin	SBT1A pin/SBT1B pin	
			Internal clock	External clock
Port Pin	P00/P73	P01/P74	P02/P75	
Port Pin Setup	Select used pin (A, B)			
	SC1ODC (SC1SEL)			
SBI / SBO pin Setup	SBI0/SBO0 independent		-	
	SC0MD1 (SC0IOM)			
Function	Serial data output	"1" input	Serial clock I/O	Serial clock I/O
	SC0MD1(SC0SBOS)	SC0MD1(SC0SBIS)	SC0MD1 (SC0SBTS)	
Style	Push-pull / Nch open-drain	-	Push-pull / Nch open-drain	Push-pull / Nch open-drain
	SC1ODC(SC1ODC0) SC1ODC(SC1ODC2)		SC1ODC (SC1ODC1)/SC1ODC (SC1ODC3)	
I/O	Output mode	-	Output mode	Input mode
	P0DIR (P0DIR0) P7DIR (P7DIR3)		P0DIR (P0DIR2) P7DIR (P7DIR5)	
Pull-up (Pull-down) setup	Add/Not Add	-	Add/Not Add	Add/Not Add
	P0PLU (P0PLU0) P7PLUD(P7PLUDD3)		P0PLU (P0PLU2) P7PLUD (P7PLUD5)	

Note) Select pull-up/down resistor with P7RDOWN flag of FLOAT register (x'03F2E')
[☞ Chapter4, 4.7.2 Register]

■Serial Interface 1 Pins Setup (3 channels, at reception)

Table 11-3-12 shows the setup for synchronous serial interface pin with 3 channels (SBO1 pin, SBI1 pin, SBT1 pin) at reception.

Table 11-3-12 Setup for Synchronous Serial Interface 1 Pin (3 channels, at reception)

Setup item	Data input pin		Clock I/O pin	
	SBO0A pin/ SBO0B pin	SBI0A pin/ SBI0B pin	SBT0A pin/SBT0B pin	
			Internal clock	External clock
Port Pin	P03/P70	P04/P71	P05/P72	
Port Pin Setup	Select used pin (A, B)			
	SC0ODC (SC0SEL)			
SBI / SBO pin Setup	SBI0/SBO0 independent		-	
	SC0MD1 (SC0IOM)			
Function	Port	Serial data input	Serial clock I/O	Serial clock I/O
	SC0MD1(SC0SBOS)	SC0MD1(SC0SBIS)	SC0MD1 (SC0SBTS)	
Style	-	-	Push-pull / Nch open-drain	Push-pull / Nch open-drain
			SC0ODC (SC0ODC1)/SC0ODC (SC0ODC3)	
I/O	-	Input mode	Output mode	Input mode
		P0DIR (P0DIR4) P7DIR (P7DIR1)	P0DIR (P0DIR5) P7DIR (P7DIR2)	
Pull-up (Pull-down) setup	-	-	Add/Not Add	Add/Not Add
			P0PLU (P0PLU5) P7PLUD (P7PLUD2)	

Note) Select pull-up/down resistor with P7RDOWN flag of FLOAT register (x'03F2E')
[☞ Chapter4, 4.7.2 Register]

■Serial Interface 1 Pins Setup (3 channels, at transmission / reception)

Table 11-3-13 shows the setup for synchronous serial interface pin with 3 lines (SBO1 pin, SBI1 pin, SBT1 pin) at transmission / reception.

Table 11-3-13 Setup for Synchronous Serial Interface 1 Pin (3 channels, at transmission / reception)

Setup item	Data output pin	Data input pin	Clock I/O pin	
	SBO0A pin/ SBO0B pin	SBI0A pin/ SBI0B pin	SBT0A pin/SBT0B pin	
			Internal clock	External clock
Port Pin	P03/P70	P04/P71	P05/P72	
Port Pin Setup	Select used pin (A, B)			
	SC0ODC (SC1SEL)			
SBI / SBO pin Setup	SBI0/SBO0 independent		-	
	SC0MD1 (SC0IOM)			
Function	Serial data output	Serial data input	Serial clock I/O	Serial clock I/O
	SC0MD1(SC0SBOS)	SC0MD1(SC0SBIS)	SC0MD1 (SC0SBTS)	
Style	Push-pull/ Nch open-drain	-	Push-pull / Nch open-drain	Push-pull / Nch open-drain
	SC0ODC (SC0ODC) SC0ODC (SC0ODC3)		SC0ODC (SC0ODC1)	
I/O	Output mode	Input mode	Output mode	Input mode
	P0DIR (P0DIR3) P7DIR (P7DIR0)	P0DIR (P0DIR4) P7DIR (P7DIR1)	P0DIR (P0DIR5) P7DIR (P7DIR2)	
Pull-up (Pull-down) setup	Add/Not Add	-	Add/Not Add	Add/Not Add
	P0PLU (P0PLU3) P7PLUD (P7PLUD0)		P0PLU (P0PLU5) P7PLUD (P7PLUD2)	

Note) Select pull-up/down resistor with P7RDOWN flag of FLOAT register (x'03F2E')

[☞ Chapter4, 4.7.2 Register]

■Serial Interface 1 Pins Setup (2 channels, at transmission)

Table 11-3-14 shows the setup for synchronous serial interface pin with 2 channels (SBO1 pin, SBT1 pin) at transmission. SBI1 pin can be used as a general port.

Table 11-3-14 Setup for Synchronous Serial Interface 1 Pin (2 channels, at transmission)

Setup item	Data output pin		Clock I/O pin	
	SBO1A pin/ SBO1B pin	SBI1A pin/ SBI1B pin	SBT1A pin/SBT1B pin	
			Internal clock	External clock
Port Pin	P00/P73		P02/P75	
Port Pin Setup	Select used pin (A, B)			
	SC1ODC (SC1SEL)			
SBI / SBO pin Setup	SBI0/SBO0 connection		-	
	SC0MD1 (SC0IOM)			
Function	Serial data output	"1" input	Serial clock I/O	Serial clock I/O
	SC0MD1(SC0SBOS)	SC0MD1(SC0SBIS)	SC0MD1 (SC0SBTS)	
Style	Push-pull / Nch open-drain	-	Push-pull / Nch open-drain	Push-pull / Nch open-drain
	SC1ODC(SC1ODC0) SC1ODC(SC1ODC2)		SC1ODC (SC1ODC1)/SC1ODC (SC1ODC3)	
I/O	Output mode	-	Output mode	Input mode
	P0DIR (P0DIR0) P7DIR (P7DIR3)		P0DIR (P0DIR2) P7DIR (P7DIR5)	
Pull-up (Pull-down) setup	Add/Not Add	-	Add/Not Add	Add/Not Add
	P0PLU (P0PLU0) P7PLUD(P7PLUD3)		P0PLU (P0PLU2) P7PLUD (P7PLUD5)	

Note) Select pull-up/down resistor with P7RDOWN flag of FLOAT register (x'03F2E')
[☞ Chapter4, 4.7.2 Register]

■Serial Interface 1 Pins Setup (2 channels, at reception)

Table 11-3-15 shows the setup for synchronous serial interface pin with 2 channels (SBO1 pin, SBT1 pin) at reception. SBI1 pin can be used as a general port.

Table 11-3-15 Setup for Synchronous Serial Interface 1 Pin (2 channels, at reception)

Setup item	Data input pin		Clock I/O pin	
	SBO1A pin/ SBO1B pin	SBI1A pin/ SBI1B pin	SBT1A pin/SBT1B pin	
			Internal clock	External clock
Port Pin	P00/P73		P02/P75	
Port Pin Setup	Select used pin (A, B)			
	SC1ODC (SC1SEL)			
SBI / SBO pin Setup	SBI0/SBO0 connection		-	
	SC0MD1 (SC0IOM)			
Function	Port	Serial data input	Serial clock I/O	Serial clock I/O
	SC0MD1(SC0SBOS)	SC0MD1(SC0SBIS)	SC0MD1 (SC0SBTS)	
Style	-	-	Push-pull / Nch open-drain	Push-pull / Nch open-drain
			SC1ODC (SC1ODC1)/SC1ODC (SC1ODC3)	
I/O	input mode	-	Output mode	Input mode
	P0DIR (P0DIR0) P7DIR (P7DIR3)		P0DIR (P0DIR2) P7DIR (P7DIR5)	
Pull-up (Pull-down) setup	-	-	Add/Not Add	Add/Not Add
			P0PLU (P0PLU2) P7PLUD (P7PLUD5)	

Note) Select pull-up/down resistor with P7RDOWN flag of FLOAT register (x'03F2E')
[☞ Chapter4, 4.7.2 Register]

11-3-4 Setup Example

■Transmission / Reception Setup Example

The setup example for clock synchronous serial communication with serial 0 is shown. Table 11-3-16 shows the conditions at transmission / reception.

Table 11-3-16 Setup Examples for Synchronous Serial Interface Transmission / Reception

Setup item	set to		Setup item	set to
SBI / SBO pin	Independent (with 3 channels)		Clock source	fs/2
Transfer bit count	8 bits		Used pin	A (port 0)
Start condition	none		Clock source 1/8 dividing	divided by 8
First transfer bit	MSB		SBT / SBO pin style	Nch open-drain
Input clock edge	falling edge		SBT pin pull-up resistor	Added
Output clock edge	rising edge		SBO pin pull-up resistor	Added
Clock	Internal clock		Serial 1 communication complete interrupt	Enable

An example setup procedure, with a description of each step is shown below.

Setup Procedure	Description
(1) Select the prescaler operation. PSCMD (x'3F6F') bp0 : PSCEN = 1	(1) Set the PSCEN flag of the PSCMD register to "1" to select "prescaler operation".
(2) Select the clock source. SC0CKS (x'3F97') bp2-0 : SC0PSC2-0 = 100	(2) Select the clcok source by the SC0CKS register. Set bp4-0 to "0100" to select "fs/2".
(3) Select the used pin. SC0ODC (x'3F96') bp7 : SC0SEL = 0	(2) Set the SC0SEL flag of the SC0ODC register to "0" to set I/O used pin to A (port 0).
(4) Control the pin type. SC0ODC (x'3F96') bp1-0 : SC0ODC1-0 = 11 P0PLU (x'3F40') bp5, 3 : P0PLU5, 3 = 1, 1	(4) Set the SC0ODC1-0 flag of the SC0ODC register to "11" to select "N-ch open drain" to the SBO/SBT pin. Set the P0PLU5, 3 flag of the P0PLU register to "1" to add pull-up resistor.
(5) Control the pin direction. P0DIR (x'3F30') bp5-3 : P0DIR5-3 = 101	5) Set the P0DIR5-3 flag of the port 0 pin direction control register (P0DIR) to "101" to set P03, P05 "output mode", and to set P04 "input mode".

Setup Procedure	Description
(6) Select the transfer bit count. SC0MD0(x'3F92')	(6) Set the SC0LNG2-0 flag of the serial 0 mode register (SC0MD0) to "111" to set the transfer bit count "8 bits".
(7) Select the start condition. SC0MD0 (x'3F92') bp3 : SC0STE = 0	(7) Set the SC0STE flag of the SC0MD0 register to "0" to disable start condition.
(8) Select the first bit to be transfered. SC0MD0 (x'3F92') bp4 : SC0DIR = 0	(8) Set the SC0DIR flag of the SC0MD0 register to "0" to set MSB as a transfer first bit.
(9) Select the transfer edge. SC0MD0 (x'3F92') bp7 : SC0CE1 = 1	(9) Set the SC0CE1 flag of the SC0MD0 register to "1" to set the transmission data output edge "rising" and the received data input edge "falling".
(10) Control the output data. SC0MD2 (x'3F94') bp0 : SC0BRKE = 0	(10) Set the SC0BRKE flag of the SC0MD2 register to "0" to select "serial data transmission".
(11) Set other mode registers. SC0MD2 (x'3F94') bp7-3	(11) No need at synchronous serial communication.
(12) Select the communication type. SC0MD1 (x'3F93') bp0 : SC0CMD = 0	(12) Set the SC0CMD flag of the SC0MD1 register to "0" to select "synchronous serial".
(13) Select the transfer clock. SC0MD1 (x'3F93') bp2 : SC0MST = 1 bp3 : SC0CKM = 1	(13) Set the SC0MST flag of the SC0MD1 register to "1" to select clock master (inside clock). Set the SC0CKM flag to "1" to select "divide by 8" for source clock.
(14) Control the pin function. SC0MD1 (x'3F93') bp4 : SC0SBOS = 1 bp5 : SC0SBIS = 1 bp6 : SC0SBTS = 1 bp7 : SC0IOM = 0	(14) Set the SC0SBOS, SC0SBIS, SC0SBTS flag of the SC0MD1 register to "1" to set SBO0A pin "serial data output", SBI0A pin "serial data input", and SBT0A pin "serial clock I/O". Set the SC0IOM flag "0" to set serial data input from SBI0A pin.

Setup Procedure	Description
(15) Set the interrupt level. SC0TICR(x'3FF5') bp7-6 : SC0TLV1-0 = 10	(15) Set the interrupt level by the SC0TLV1-0 flag of the serial 0 transmission interrupt control register (SC0TICR). (Set level 2.)
(16) Enable the interrupt. SC0TICR(x'3FF5') bp1 : SC0TIE = 1	(16) Set the SC0TIE flag of the SC0TICR register to "1" to enable interrupts. If any interrupt request flag (SC0TIR of the SC0TICR register) is already set, clear SC0TIR before an interrupt is enabled. [☞ Chapter 3 3-1-4. Interrupt Flag Setup]
(17) Start serial transmission. Transmission data→TXBUF0 (x'3F91') Received data→input to SBI0A pin.	(17) Set the transmission data to the serial transmission data buffer TXBUF0. Then, an internal clock is generated to start transmission / reception. After the transmission is finished, serial0 transmission interrupt SC0TIRQ is generated.

Note : In (6) to (9), (10) to (11), (12) to (14),each settings can be set at once.

When only reception with 3 channels is operated, set SCnSBOS of the SCnMD1 register to "0" and select a port. The SBO pin can be used as a general port.

When SBO / SBI pin are connected for communication with 2 lines, the SBO pin inputs / outputs serial data. The port direction control register PnDIR switches I/O. At reception, set SCnSBIS of the SCnMD1 register to "1", always, to select "serial data input". The SBI pin can be used as a general port.

It is possible to shut down communication. If the communication should be stopped by force, set SCnSBOS and SCnSBIS of the SCnMD1 register to "0".

Each flag should be set as the procedure in order. Activation for communication should be operated after all control registers (except Table 11-2-1 : TXBUFn, RXBUFn) are set.

Transfer rate of transfer clock that set by SCnCKS register should be under 2.5 MHz.

11-3-5 UART Serial Interface

Serial 0, 1 can be used for duplex UART communication. Table 11-3-17 shows UART serial interface functions.

Table 11-3-17 UART Serial Interface Functions

	Serial Interface 0	Serial Interface 1
Communication style	UART(duplex)	
Interrupt	SC0TIRQ(transmission) SC0RIRQ(reception)	SC1TIRQ(transmission) SC1RIRQ(reception)
Used pins	TXD0(output, input) RXD0(input)	TXD1(output, input) RXD1(input)
Specification the first transfer bit	MSB / LSB	
Selection of parity bit	√	
Parity bit control	0 parity 1 parity odd parity even parity	
Frame selection	7 bits + 1 stop 7 bits + 2 stops 8 bits + 1 stop 8 bits + 2 stops	
Continuous operation	√	
Continuous operation (with ATC)	√	
Maximum transfer rate	300 kbps (Standard 300 bps to 38.4 kbps) (with baud rate timer)	

■Activation Factor for Communication

At transmission, if any data is written to the transmission data buffer TXBUFn, a start condition is generated to start transfer. At reception, if a start condition is received, communication is started. At reception, if the data length of "L" for start bit is longer than 0.5 bit, that can be regarded as a start condition.

■Transmission

Data transfer is automatically started by writing data to the transmission data buffer TXBUFn. When the transmission has completed, the serial 0 transmission interrupt SCnTIRQ is generated.

■Reception

Once a start condition is received, reception is started after the transfer bit counter that counts transfer bit is cleared. When the reception is completed, the serial n reception interrupt SCnRIRQ is generated.

■Duplex communication

Duplex communication, that the transmission and reception can be operated independently at the same time is available. On duplex communication, the frame mode and parity bit of the used data on transmission / reception should have the same polarity.

■Transfer Bit Count Setup

The transfer bit count is automatically set after the frame mode is specified by the SCnFM1 to 0 flag of the SCnMD2 register. If the SCnCMD flag of the SCnMD1 register is set to "1", and UART communication is selected, the setup by the synchronous serial data transfer bit count selection flag SCnLNG2 to 0 is no more valid.

■Data Input Pin Setup

The communication mode can be selected from with 2 channels (data output pin (TXD pin), data input pin (RXD pin)), or with 1 channel (data I/O pin TXD pin). The RXD pin can be used only for serial data input. The TXD pin can be used for serial data input or output. The SCnIOM flag of the SCnMD1 register can specify which pin, RXD or TXD to input the serial data. "Data input from TXD pin" is selected to be with 1 channel communication, transmission / reception is switched by controlling TXD pin's direction by the PnDIR0 flag of the PnDIR register. At that time, the RXD pin can be used as a general port.

■Received Buffer Empty Flag

When the communication complete interrupt SCnRIRQ is generated, data is stored to RXBUFn from the internal shift register, automatically. If data is stored to the shift register RXBUFn, the recieved buffer empty flag SCnREMP of the SCnMD3 register is set to "1". This indicates that the reception data is going to be read. SCnREMP is cleared to "0" by reading data in RXBUFn.

■Reception BUSY flag

When the start condition is reagarded, the SCnRBSY flag of the SCnMD3 register is set to "1". That is cleared to "0" by the generation of the reception complete interrupt SCnRIRQ. If, during reception, the SCnSBIS flag is set to "0", the SCnRBSY flag is reset to "0".

■Transmission BUSY flag

When any data is set to TXBUFn, the SCnTBSY flag of the SCnMD3 register is set to "1". That is cleared to "0" by the generation of the transmission complete interrupt SCnTIRQ. During continuous communication the SCnTBSY flag is always set. If the transmission buffer empty flag SnTEMP is set to "0" as the transmission complete interrupt SCnTIRQ is generated, the SCnTBSY is cleared to "0". If the SCnSBOS flag is set to "0", the SCnTBSY flag is reset to "0".

■Frame Mode and Parity Check Setup

Figure 11-3-15 shows the data format at UART communication.

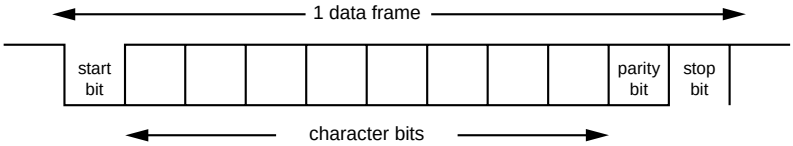


Figure 11-3-15 UART Serial Interface Transmission / Reception Data Format

The transmission / reception data consists of start bit, character bit, parity bit and stop bit.
Table 11-3-18 shows its kinds to be set.

Table 11-3-18 UART Serial Interface Transmission / Reception Data

Start bit	1 bit
Character bit	7, 8 bits
Parity bit	fixed to 0, fixed to 1, even, odd, none
Stop bit	1, 2 bits

The SCnFM1 to 0 flag of the SCnMD2 register sets the frame mode. Table 11-3-19 is shown the UART Serial Interface Frame Mode setting. If the SCnCMD flag of the SCnMD1 register is set to "1", and UART communication is selected, the transfer bit count on the SCnLNG2 to 0 flag of the SCnMD0 register is no more valid.

Table 11-3-19 UART Serial Interface Frame Mode

SCnMD2 register		Frame mode
SCnFM1	SCnFM0	
0	0	Character bit 7 bits + Stop bit 1 bit
0	1	Character bit 7 bits + Stop bit 2 bits
1	0	Character bit 8 bits + Stop bit 1 bit
1	1	Character bit 8 bits + Stop bit 2 bits

Parity bit is to detect wrong bits with transmission / reception data.
Table 11-3-20 shows kinds of parity bit. The SCnNPE, SCnPM1 to 0 flag of the SCnMD2 register set parity bit.

Table 11-3-20 Parity Bit of UART Serial Interface

SCnMD2 register			Parity bit	Setup
SCnNPE	SCnPM1	SCnPM0		
0	0	0	fixed to 0	Set parity bit to "0".
0	0	1	fixed to 1	Set parity bit to "1".
0	1	0	odd parity	Control that the total of "1" of parity bit and character bit should be odd.
0	1	1	even parity	Control that the total of "1" of parity bit and character bit should be even.
1	-	-	none	Do not add parity bit.

■Break Status Transmission Control Setup
The SCnBRKE flag of the SCnMD2 register generates the break status. If SCnBRKE is set to "1" to select the break transmission, all bits from start bits to stop bits transfer "0".

■Reception Error

At reception , there are 3 types of error ; overrun error, parity error and framing error. Reception error can be determined by the SCnORE, SCnPEK, SCnFEF flag of the SCnMD3 register. Even one of those errors is detected, the SCnERE flag of the SCnMD3 register is set to "1". The SCnPEK, the SCnFEF flags in recepption error flag are renewed at generation of the reception complete interrupt SCnRIRQ. The SCnORE flag is holded the status unless data of RXBUFn is read out. The judgements of the received error flag should be operated until the next communication is finished. The communication operation does not have any effect on those error flags . Table 11-3-21 shows the list of reception error source.

Table 11-3-21 Reception Error Source of UART Serial Interface

Flag	Error	Error source	
SCnORE	Overrun error	Next data is received before reading the receive buffer.	
SCnPEK	Parity error	at fixed to 0	when parity bit is "1"
		at fixed to 1	when parity bit is "0"
		odd parity	The total of "1" of parity bit and character bit is even.
		even parity	The total of "1" of parity bit and character bit is odd.
SCnFEF	Framing error	Stop bit is not detected.	

■Judgement of Break Status Reception

Reception at break status can be judged. If all received data from start bit to stop bit is "0", the SCnBRKF flag of the SCnMD2 register is set and regard the break status. The SCnBRKF flag is set at generation of the reception complete interrupt SCnRIRQ.

■Sequence Communication

It is possible to transfer continuously. If data is set to the transmission data buffer TXBUFn during communication, the transmission buffer empty flag SCnTEMP is set to continue the communication, automatically. In this case, there is no pause on communication. Data should be set to TXBUFn after data is loaded to the inside shift register before the communication complete interrupt SC0TIRQ is generated.

Also, this LSI has an automatic data transfer function ATC1 that can be one of an activation factor. At activation by ATC1, data can be transfered up to 255 bytes, continuously. In this case, there is a communication blank ; up to 18 machine cycles + 3.5 bit data length. For an activation by ATC1, refer to chapter 15. automatic transfer controller, transfer mode 6 to 9.

■Transmission/reception data polarity switching

In UART communication, polarity of transmission/reception data cannot be switched.
At the same time, setups of the SCnTRN, SCnREN flags of the SCnMD0 register are invalid.

■Clock Setup

At UART communication, the transfer clock is not needed, but the clock setup should be needed to decide the timing of the data transmission / reception in the serial interface.
Select the timer to be used as a baud rate timer, by the SCnCKS register, and set the SCnMST flag of the SCnMD1 register to "1" to select the internal clock (clock master).

At UART communication, set the SCnMST flag of the SCnMD1 register to "1". If that is set to "0", the communication is impossible.

The following items are same to clock synchronous serial.
Reference as follows ;

■First Transfer Bit Setup
Refer to : XI-21

■Transmission Data Buffer
Refer to : XI-21

■Received Data Buffer
Refer to : XI-21

■Transfer Bit Count and First Transfer Bit
Refer to : XI-22

■Receive Bit Count and First Transfer Bit
Refer to : XI-22

■Transmission Buffer Empty Flag
Refer to : XI-25

■Emergency Reset
Refer to : XI-26

■Transmission Timing

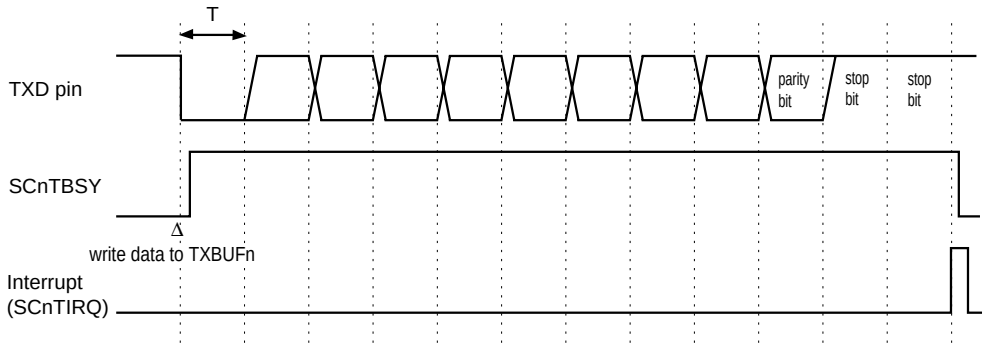


Figure 11-3-16 Transmission Timing (parity bit is enabled)

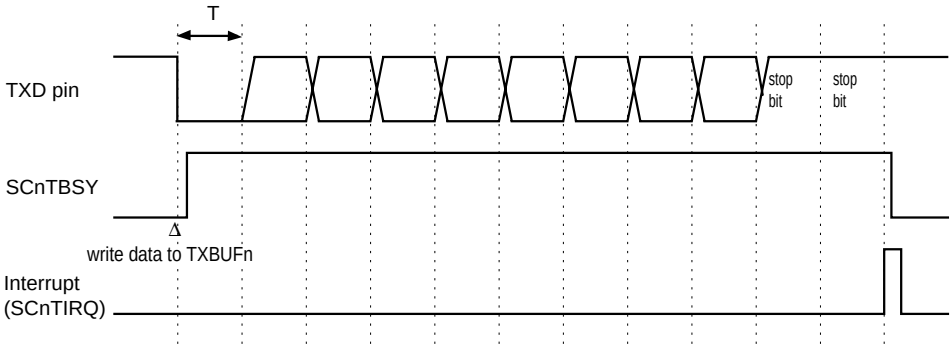


Figure 11-3-17 Transmission Timing (parity bit is disabled)

■Reception Timing

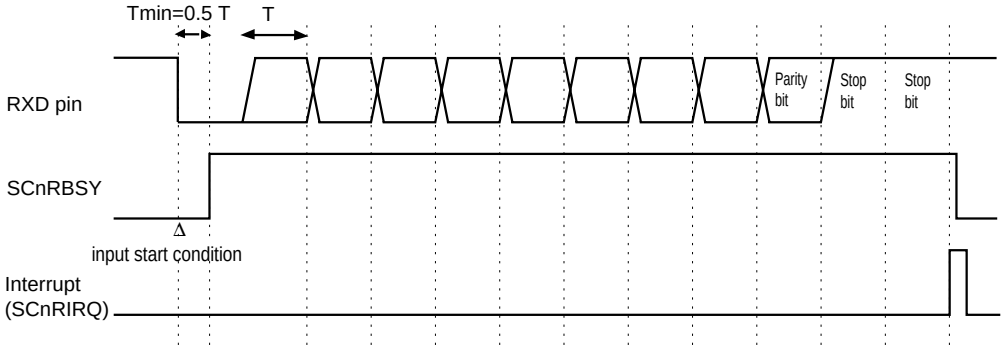


Figure 11-3-18 Reception Timing (parity bit is enabled)

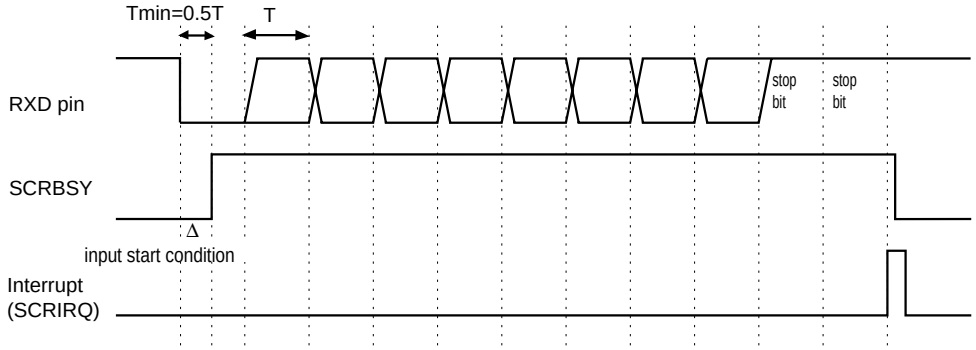


Figure 11-3-19 Reception Timing (parity bit is disabled)

■Transfer Rate

Baud rate timer (timer 2 and timer 4) can set any transfer rate.

Tables 11-3-22, 23 show the setup example of the transfer rate. For detail of the baud rate timer setup, refer to chapter 6. 8-bit Timer.

Table 11-3-22 UART Serial Interface Transfer Rate Setup Register

Setup	Register	Page
Serial 0 clock source (timer output)	SC0CKS	XI - 13
Timer clock source selection	TM5MD	VI - 13
Timer compare register selection	TM5OC	VI - 8

Table 11-3-23 UART Serial Interface Transfer Rate Setup Register

Setup	Register	Page
Serial 1 clock source (timer output)	SC1CKS	XI - 20
Timer clock source selection	TM4MD	VI - 12
Timer compare register selection	TM4OC	VI - 8

Timer 4 compare register is set as follows ;

overflow cycle = (set value of compare register + 1) x timer clock cycle

baud rate = 1 / (overflow cycle x 2 x 8) ("8" means that clock source is divided by 8)

therefore,

set value of compare register = timer clock frequency / (baud rate x 2 x 8) - 1

For example, if baud rate should be 300 bps at timer clock source fs/4 (fosc = 8 MHz, fs = fosc/2), set value should be as follows ;

Set value of comapre register = $(8 \times 10^6 / 2 / 4) / (300 \times 2 \times 8) - 1$

= 207

= x'CF'

Timer clock source and the set values of timer compare register at the standard rate are shown on the following page.

Transfer rate should be selected under 300 kbps.

Table 11-3-24-1 UART Serial Interface Transfer Rate (decimal)

		Transfer rate (bps)									
fosc (MHz)	Clock source (timer)	300		960		1200		2400		4800	
		Set value	Calculated Value	Set value	Calculated Value	Set value	Calculated Value	Set value	Calculated Value	Set value	Calculated Value
4.00	fosc	-	-	-	-	207	1202	103	2404	51	4808
	fosc/4	207	300	64	962	51	1202	25	2404	12	4808
	fosc/16	51	300	-	-	12	1202	-	-	-	-
	fosc/32	25	300	-	-	-	-	-	-	-	-
	fosc/64	12	300	-	-	-	-	-	-	-	-
	fs/2	207	300	64	962	51	1202	25	2404	12	4808
	fs/4	104	297	-	-	25	1202	12	2404	-	-
4.19	fosc	-	-	-	-	217	1201	108	2403	54	4761
	fosc/4	217	300	67	963	-	-	-	-	-	-
	fosc/16	-	-	16	963	-	-	6	2338	-	-
	fosc/32	-	-	-	-	-	-	-	-	-	-
	fosc/64	-	-	-	-	-	-	-	-	-	-
	fs/2	217	300	67	963	-	-	-	-	-	-
	fs/4	108	300	33	963	-	-	13	2338	-	-
8.00	fosc	-	-	-	-	-	-	207	2404	103	4808
	fosc/4	-	-	129	962	103	1202	51	2404	25	4808
	fosc/16	103	300	-	-	25	1202	12	2404	-	-
	fosc/32	51	300	-	-	12	1202	-	-	-	-
	fosc/64	25	300	-	-	-	-	-	-	-	-
	fs/2	-	-	129	962	103	1202	51	2404	25	4808
	fs/4	207	300	64	962	51	1202	25	2404	12	4808
8.38	fosc	-	-	-	-	-	-	217	2403	108	4805
	fosc/4	-	-	135	963	108	1201	-	-	-	-
	fosc/16	108	300	33	963	-	-	13	2338	-	-
	fosc/32	-	-	16	963	-	-	6	2338	-	-
	fosc/64	-	-	-	-	-	-	-	-	-	-
	fs/2	-	-	135	963	108	1201	-	-	-	-
	fs/4	217	300	67	963	-	-	-	-	-	-
12.00	fosc	-	-	-	-	-	-	-	-	155	4808
	fosc/4	-	-	194	962	155	1202	77	2404	38	4808
	fosc/16	155	300	-	-	38	1202	-	-	-	-
	fosc/32	77	300	-	-	-	-	-	-	-	-
	fosc/64	38	300	-	-	-	-	-	-	-	-
	fs/2	-	-	194	962	155	1202	77	2404	38	4808
	fs/4	-	-	-	-	77	1202	38	2404	-	-
16.00	fosc	-	-	-	-	-	-	-	-	207	4808
	fosc/4	-	-	-	-	207	1202	103	2404	51	4808
	fosc/16	207	300	64	962	51	1202	25	2404	12	4808
	fosc/32	103	300	-	-	25	1202	12	2404	-	-
	fosc/64	51	300	-	-	12	1202	-	-	-	-
	fs/2	-	-	-	-	207	1202	103	2404	51	4808
	fs/4	-	-	129	962	103	1202	51	2404	25	4808
16.76	fosc	-	-	-	-	-	-	-	-	-	-
	fosc/4	-	-	-	-	217	1201	108	2403	54	4761
	fosc/16	217	300	67	963	-	-	-	-	-	-
	fosc/32	108	300	33	963	-	-	-	-	-	-
	fosc/64	-	-	16	963	-	-	-	-	-	-
	fs/2	-	-	-	-	217	1201	108	2403	54	4761
	fs/4	-	-	135	963	108	1201	54	2381	-	-
20.00	fosc	-	-	-	-	-	-	-	-	-	-
	fosc/4	-	-	-	-	-	-	129	2404	64	4808
	fosc/16	-	-	-	-	64	1202	-	-	-	-
	fosc/32	129	300	-	-	-	-	-	-	-	-
	fosc/64	64	300	-	-	-	-	-	-	-	-
	fs/2	-	-	-	-	-	-	129	2404	64	4808
	fs/4	-	-	162	959	129	1202	64	2404	-	-

Table 11-3-24-2 UART Serial Interface Transfer Rate (decimal)

		Transfer rate (bps)									
fosc (MHz)	Clock source (timer)	9600		19200		28800		31250		38400	
		Set value	Calculated Value	Set value	Calculated Value	Set value	Calculated Value	Set value	Calculated Value	Set value	Calculated Value
4.00	fosc	25	9615	12	19231	-	-	7	31250	-	-
	fosc/4	-	-	-	-	-	-	1	31250	-	-
	fosc/16	-	-	-	-	-	-	-	-	-	-
	fosc/32	-	-	-	-	-	-	-	-	-	-
	fosc/64	-	-	-	-	-	-	-	-	-	-
	fs/2	-	-	-	-	-	-	1	31250	-	-
	fs/4	-	-	-	-	-	-	-	-	-	-
4.19	fosc	26	9699	-	-	-	-	-	-	-	-
	fosc/4	-	-	-	-	-	-	-	-	-	-
	fosc/16	-	-	-	-	-	-	-	-	-	-
	fosc/32	-	-	-	-	-	-	-	-	-	-
	fosc/64	-	-	-	-	-	-	-	-	-	-
	fs/2	-	-	-	-	-	-	-	-	-	-
	fs/4	-	-	-	-	-	-	-	-	-	-
8.00	fosc	51	9615	25	19231	-	-	15	31250	12	38462
	fosc/4	12	9615	-	-	-	-	3	31250	-	-
	fosc/16	-	-	-	-	-	-	-	-	-	-
	fosc/32	-	-	-	-	-	-	-	-	-	-
	fosc/64	-	-	-	-	-	-	-	-	-	-
	fs/2	12	9615	-	-	-	-	3	31250	-	-
	fs/4	-	-	-	-	-	-	1	31250	-	-
8.38	fosc	54	9523	26	19398	-	-	-	-	-	-
	fosc/4	-	-	-	-	-	-	-	-	-	-
	fosc/16	-	-	-	-	-	-	-	-	-	-
	fosc/32	-	-	-	-	-	-	-	-	-	-
	fosc/64	-	-	-	-	-	-	-	-	-	-
	fs/2	-	-	-	-	-	-	-	-	-	-
	fs/4	-	-	-	-	-	-	-	-	-	-
12.00	fosc	77	9615	38	19231	25	28846	23	31250	-	-
	fosc/4	-	-	-	-	-	-	5	31250	-	-
	fosc/16	-	-	-	-	-	-	-	-	-	-
	fosc/32	-	-	-	-	-	-	-	-	-	-
	fosc/64	-	-	-	-	-	-	-	-	-	-
	fs/2	-	-	-	-	-	-	5	31250	-	-
	fs/4	-	-	-	-	-	-	2	31250	-	-
16.00	fosc	103	9615	51	19231	-	-	31	31250	25	38462
	fosc/4	25	9615	12	19231	-	-	7	31250	-	-
	fosc/16	-	-	-	-	-	-	-	-	-	-
	fosc/32	-	-	-	-	-	-	-	-	-	-
	fosc/64	-	-	-	-	-	-	-	-	-	-
	fs/2	25	9615	-	-	-	-	7	31250	-	-
	fs/4	12	9615	-	-	-	-	3	31250	-	-
16.76	fosc	108	9610	54	19045	-	-	-	-	-	-
	fosc/4	26	9699	-	-	-	-	-	-	-	-
	fosc/16	-	-	-	-	-	-	-	-	-	-
	fosc/32	-	-	-	-	-	-	-	-	-	-
	fosc/64	-	-	-	-	-	-	-	-	-	-
	fs/2	26	9699	-	-	-	-	-	-	-	-
	fs/4	-	-	-	-	-	-	-	-	-	-
20.00	fosc	129	9615	64	19231	-	-	39	31250	-	-
	fosc/4	-	-	-	-	-	-	9	31250	-	-
	fosc/16	-	-	-	-	-	-	-	-	-	-
	fosc/32	-	-	-	-	-	-	-	-	-	-
	fosc/64	-	-	-	-	-	-	-	-	-	-
	fs/2	-	-	-	-	-	-	9	31250	-	-
	fs/4	-	-	-	-	-	-	4	31250	-	-

11-3-6 Serial interface 0 UART Serial Interface Pin Setup

■Serial Interface 0 Pin Setup (1, 2 channels, at transmission)

Table 11-3-25 shows the pins setup at UART serial interface 0 transmission. The pins setup is common to the TXD0 pin, RXD0 pin, regardless of those pins are independent / connected.

Table 11-3-25 UART Serial Interface 0 Pin Setup (1, 2 channels, at transmission)

Setup item	Data output pin	Data input pin
	TXD0A pin/ TXD0B pin	RXD0A pin/ RXD0B pin
Port Pin	P03/P70	P04/P71
Port Pin Setup	Select used pin (A, B)	
	SC0ODC (SC0SEL)	
TXD / RXD pin Setup	TXD0/RXD0 pin independent/connection	
	SC0MD1 (SC0IOM)	
Function	Serial data output	"1" input
	SC0MD1(SC0SBOS)	SC0MD1(SC0SBIS)
Style	Push-pull / Nch open-drain	-
	SC0ODC (SC0ODC0) SC0ODC (SC0ODC2)	
I/O	Output mode	-
	P0DIR (P0DIR3) P7DIR (P7DIR0)	
Pull-up (Pull-down) setup	Add/Not Add	-
	P0PLU (P0PLU3) P7PLUD(P7PLUD0)	

Note) Select pull-up/down resistor with P7RDOWN flag of FLOAT register (x03F2E')
[☞ Chapter4, 4.7.2 Register]

■Serial Interface 0 Pin Setup (2 channels, at reception)

Table 11-3-26 shows the pins setup at UART serial interface 0 reception with 2 channels (TXD0 pin, RXD0 pin).

Table 11-3-26 UART Serial Interface 0 Pin Setup (2 channels, at reception)

Setup item	Data output pin	Data input pin
	TXD0A pin/ TXD0B pin	RXD0A pin/ RXD0B pin
Port Pin	P03/P70	P04/P71
Port Pin Setup	Select used pin (A, B)	
	SC0ODC (SC0SEL)	
TXD / RXD pin Setup	TXD0/RXD0 pin independent/connection	
	SC0MD1 (SC0IOM)	
Function	Port	Serial data input
	SC0MD1(SC0SBOS)	SC0MD1(SC0SBIS)
Style	Push-pull / Nch open-drain	-
	SC0ODC (SC0ODC0) SC0ODC (SC0ODC2)	
I/O	-	input mode
		P0DIR (P0DIR4) P7DIR (P7DIR1)
Pull-up (Pull-down) setup	-	-

■Serial Interface 0 Pin Setup (1 channel, at reception)

Table 11-3-27 shows the pin setup at UART serial interface 0 reception with 1 channel (TXD0 pin). The RXD0 pin is not used, so can be used as a port.

Table 11-3-27 UART Serial Interface 0 Pin Setup (1 channel, at reception)

Setup item	Data output pin	Data input pin
	TXD0A pin/ TXD0B pin	RXD0A pin/ RXD0B pin
Port Pin	P03/P70	P04/P71
Port Pin Setup	Select used pin (A, B)	
	SC0ODC (SC0SEL)	
TXD / RXD pin Setup	TXD0/RXD0 pin independent/connection	
	SC0MD1 (SC0IOM)	
Function	Serial data output	"1" input
	SC0MD1(SC0SBOS)	SC0MD1(SC0SBIS)
Style	-	-
I/O	Input mode	-
	P0DIR (P0DIR3) P7DIR (P7DIR1)	
Pull-up (Pull-down) setup	-	-

■Serial Interface 0 Pin Setup (2 channels, at transmission / reception)

Table 11-3-28 shows the pin setup at UART serial interface 0 transmission / reception with 2 channels (TXD0 pin, RXD0).

Table 11-3-28 UART Serial Interface 0 Pin Setup (2 channels, at transmission / reception)

Setup item	Data output pin	Data input pin
	TXD0A pin/ TXD0B pin	RXD0A pin/ RXD0B pin
Port Pin	P03/P70	P04/P71
Port Pin Setup	Select used pin (A, B)	
	SC0ODC (SC0SEL)	
TXD / RXD pin Setup	TXD0/RXD0 pin independent/connection	
	SC0MD1 (SC0IOM)	
Function	Serial data output	"1" input
	SC0MD1(SC0SBOS)	SC0MD1(SC0SBIS)
Style	Push-pull / Nch open-drain	-
	SC0ODC (SC0ODC0) SC0ODC (SC0ODC2)	
I/O	Output mode	Input mode
	P0DIR (P0DIR3) P7DIR (P7DIR0)	P0DIR (P0DIR4) P7DIR (P7DIR1)
Pull-up (Pull-down) setup	Add/Not Add	-
	P0PLU (P0PLU3) P7PLUD(P7PLUD0)	

Note) Select pull-up/down resistor with P7RDOWN flag of FLOAT register (x'03F2E')
[Chapter4, 4.7.2 Register]

11-3-7 Serial interface 1 UART Serial Interface Pin Setup

■Serial Interface 1 Pin Setup (1, 2 channels, at transmission)

Table 11-3-29 shows the pins setup at UART serial interface 1 transmission. The pins setup is common to the TXD1 pin, RXD1 pin, regardless of those pins are independent / connected.

Table 11-3-29 UART Serial Interface 1 Pin Setup (1, 2 channels, at transmission)

Setup item	Data output pin	Data input pin
	TXD1A pin/ TXD1B pin	RXD1A pin/ RXD1B pin
Port Pin	P00/P73	P01/P74
Port Pin Setup	Select used pin (A, B)	
	SC1ODC (SC1SEL)	
TXD / RXD pin Setup	TXD0/RXD0 pin independent/connection	
	SC0MD1 (SC0IOM)	
Function	Serial data output	"1" input
	SC0MD1(SC0SBOS)	SC0MD1(SC0SBIS)
Style	Push-pull / Nch open-drain	-
	SC1ODC (SC1ODC0) SC1ODC (SC1ODC2)	
I/O	Output mode	-
	P0DIR (P0DIR0) P7DIR (P7DIR3)	
Pull-up (Pull-down) setup	Add/Not Add	-
	P0PLU (P0PLU0) P7PLUD(P7PLUD3)	

Note) Select pull-up/down resistor with P7RDOWN flag of FLOAT register (x'03F2E')
[☞ Chapter4, 4.7.2 Register]

■Serial Interface 1 Pin Setup (2 channels, at reception)

Table 11-3-30 shows the pins setup at UART serial interface 1 reception with 2 channels (TXD1 pin, RXD1 pin).

Table 11-3-30 UART Serial Interface 1 Pin Setup (2 channels, at reception)

Setup item	Data output pin	Data input pin
	TXD1A pin/ TXD1B pin	RXD1A pin/ RXD1B pin
Port Pin	P00/P73	P01/P74
Port Pin Setup	Select used pin (A, B)	
	SC1DC (SC1SEL)	
TXD / RXD pin Setup	TXD0/RXD0 pin independent/connection	
	SC0MD1 (SC0IOM)	
Function	Serial data output	"1" input
	SC0MD1(SC0SBOS)	SC0MD1(SC0SBIS)
Style	-	-
I/O	-	input mode
		P0DIR (P0DIR1) P7DIR (P7DIR4)
Pull-up (Pull-down) setup	-	-

■Serial Interface 1 Pin Setup (1 channel, at reception)

Table 11-3-31 shows the pin setup at UART serial interface reception with 1 channel (TXD1 pin). The RXD1 pin is not used, so can be used as a port.

Table 11-3-31 UART Serial Interface 1 Pin Setup (1 channel, at reception)

Setup item	Data output pin	Data input pin
	TXD1A pin/ TXD1B pin	RXD1A pin/ RXD1B pin
Port Pin	P00/P73	P01/P74
Port Pin Setup	Select used pin (A, B)	
	SC1ODC (SC1SEL)	
TXD / RXD pin Setup	TXD0/RXD0 pin independent/connection	
	SC0MD1 (SC0IOM)	
Function	Serial data output	"1" input
	SC0MD1(SC0SBOS)	SC0MD1(SC0SBIS)
Style	-	-
I/O	Output mode	-
	P0DIR (P0DIR0) P7DIR (P7DIR3)	
Pull-up (Pull-down) setup	-	-

Note) Select pull-up/down resistor with P7RDOWN flag of FLOAT register (x'03F2E')

[Chapter4, 4.7.2 Register]

■Serial Interface 1 Pin Setup (2 channels, at transmission / reception)

Table 11-3-32 shows the pin setup at UART serial interface 1 transmission / reception with 2 channels (TXD1 pin, RXD1).

Table 11-3-32 UART Serial Interface 1 Pin Setup (2 channels, at transmission / reception)

Setup item	Data output pin	Data input pin
	TXD1A pin/ TXD1B pin	RXD1A pin/ RXD1B pin
Port Pin	P00/P73	P01/P74
Port Pin Setup	Select used pin (A, B)	
	SC1DC (SC1SEL)	
TXD / RXD pin Setup	TXD0/RXD0 pin independent/connection	
	SC0MD1 (SC0IOM)	
Function	Serial data output	"1" input
	SC0MD1(SC0SBOS)	SC0MD1(SC0SBIS)
Style	Push-pull / Nch open-drain	-
	SC1ODC (SC1ODC0) SC1ODC (SC1ODC2)	
I/O	Output mode	input mode
	P0DIR (P0DIR0) P7DIR (P7DIR3)	P0DIR (P0DIR1) P7DIR (P7DIR4)
Pull-up (Pull-down) setup	Add/Not Add	-
	P0PLU (P0PLU0) P7PLUD(P7PLUD3)	

11-3-8 Setup Example

■Transmission / Reception Setup

The setup example at UART transmission / reception with serial 0 is shown.

Table 11-3-33 shows the conditions at transmission / reception.

Table 11-3-33 UART Interface Transmision Reception Setup

Setup item	set to
TXD / RXD pin	independent (with 2 channels)
Frame mode specification	8 bits + 2 stop bits
First transfer bit	MSB
Clock source	timer 5
Used pin	A (Port 0)
TXD0A / RX0DA pin type	Nch open-drain
Pull-up resistor of TXD0A pin	added
Parity bit add / check	"0"add / check
Serial interface 0 transmission complete interrupt	Enable.
Serial interface 0 reception complete interrupt	Enable.

An example setup procedure, with a description of each step is shown below.

Setup Procedure	Description
(1) Select prescaler operation. PSCMD (x'3F6F') bp0 : PSCEN = 1	(1) Set the PSCEN flag of the PSCMD register to "1" to select prescaler operation.
(2) Select the clock source. SC0CKS (x'3F97') bp2-0 : SC0PSC2-0 = 110	(2) Set the bp2-0 flag of the SC0CKS register to "110" to select timer 4 output as a clock source.
(3) Select the used pin. SC0ODC(x'3F96') bp7 : SC0SEL = 0	(3) Set the SC0SEL flag of the SC0ODC register to "0" to set I/O used pin to A (port 0).
(4) Control the pin type. SC0ODC(x'3F96') bp0 : SC0ODC0 = 1 P0PLU(x'3F40') bp3 : P0PLU3 = 1	(4) Set the SC0ODC0 flag of the SC0ODC register to "1" to select N-ch open drain for the TXD0A pin. Set the P0PLU3 flag of the P0PLU register to "1" to add pull-up resistor.
(5) Control the pin direction. P0DIR(x'3F30') bp4-3 : P0DIR4-3 = 01	(5) Set the P0DIR4-3 flag of the port 0 pin direction control register (P0DIR) to "01" to set P03 to output mode, and P04 to input mode.

Setup Procedure	Description
(6) Select the start condition. SC0MD0(x'3F92') bp3 : SC0STE = 1	(6) Set the SC0STE flag of the SC0MD0 register to "1" to enable start condition.
(7) Select the first bit to be transfered. SC0MD0(x'3F92') bp4 : SC0DIR = 0	(7) Set the SC0DIR flag of the SC0MD0 register to "0" to select MSB as first transfer bit.
(8) Control the output data. SC0MD2 (x'3F94') bp0 : SC0BRKE = 0	(8) Set the SC0BRKE flag of the SC0MD2 register to "0" to select serial data transmission.
(9) Select the added parity bit. SC0MD2 (x'3F94') bp3 : SC0NPE = 0 bp5-4 : SC0PM1-0 = 00	(9) Set the SC0PM1-0 flag of the SC0MD2 register to "00" to select 0 parity, and set the SC0NPE flag to "0" to add parity bit.
(10) Specify the frame mode. SC0MD2 (x'3F94') bp7-6 : SC0FM1-0 = 11	(10) Set the SC0FM1-0 flag of the SC0MD2 register to "11" to select 8 bits + 2 stop bits at the frame mode.
(11) Set the SC0MD1 register. Select the communication type. SC0MD1 (x'3F93') bp0 : SC0CMD = 1	(11) Set the SC0CMD flag of the SC0MD1 register to "1" to select duplex UART.
(12) Select the clock frequency. SC0MD1 (x'3F93') bp3 : SC0CKM = 1 bp2 : SC0MST = 1	(12) Set the SC0CKM flag of the SC0MD1 register to "1" to select "divided by 8" at source clock. And, the SC0MST flag should be always set to "1" to select colck master.
(13) Control the pin function. SC0MD1 (x'3F93') bp4 : SC0SBOS = 1 bp5 : SC0SBIS = 1 bp7 : SC0IOM = 0	(13) Set the SC0SBOS, SC0SBIS flag of the SC0MD1 register to "1" to set the TXD0A pin to serial data output and the RXD0A pin to serial data input.

Setup Procedure	Description
(14) Enable the interrupt. SC0RICR(x'3FF4') bp1 : SC0RIE = 1 SC0TICR(x'3FF5') bp1 : SC0TIE = 1	(14) Set the SC0RIE flag of the SC0RICR register to "1", and set the SC0TIE flag ot the SC0TICR register to "1" to enable the interrupt request. If any interrupt request flag is already set, clear them. [☞ Chapter 3. 3-1-4 Interrupt Flag Setup]
(15) Set the baud rate timer.	(15) Set the baud rate timer by the TM5MD register, the TM5OC register. Set the TM5EN flag to "1" to start timer 4. [☞ Chapter 6. 6-8 Serial Transfer Clock]
(16) Start serial communication. The transmission data → TXBUF0 (x'3F91') The received data → input to RXD0A	(16) The transmission is started by setting the transmission data to the serial transmission data buffer (TXBUF0). When the transmission has finished, the serial 0 transmission interrupt (SC0TIRQ) is generated. After the serial data is input from the RXD0A pin and the start condition is recognized, the received data is stored. When the reception has finished, the received data is stored to the serial received data buffer RXBUF0 and the serial 0 reception data buffer interrupt SC0RICR is generated.

Note : (6) to (7), (8) to (10), (11) to (13) can be set at once.

When the TXD0 / RXD0 pin are connected for communication with 1 channel, the TXD0 pin inputs / outputs serial data. The port direction control register P0DIR switches I/O. At reception, set SC0SBIOS of the SC0MD1 register to "1" to select serial data input. The RXD0 pin can be used as a general port.

It is possible to shut down the communication. If the communication should be stopped by force, set SC0SBOS and SC0SBIS of the SC0MD1 register to "0".

Each flag should be set as its procedure in order. Activation for communication should be operated after all control registers (except Table 11-2-1 : TXBUF0, RXBUF0) are set.

Chapter 12 Serial Interface 3

12

12-1 Overview

This LSI contains a serial interface 3 can be used for both communication types of clock synchronous and simple IIC (single master).

12-1-1 Functions

Table 12-1-1 shows the functions of serial interface 3.

Table 12-1-1 Serial Interface 3 Functions List

Communication type	Clcok synchronous	IIC (single master)
Interrupt	SC3IRQ	SC3IRQ
Pin	SBO3, SBI3, SBT3	SDA, SCL
3 channels type	√	-
2 channels type	√ (SBO3, SBT3)	√
Start condition	√	√
Transfer bit count	1 to 8 bit	1 to 8 bit
First transfer bit	√	√
Input edge / Output edge	√	-
ACK bit	-	√
ACK bit level	-	√
Continuous operation (with ATC1)	√	-
Clock source	fosc/2 fosc/4 fosc/16 fosc/32 fs/2 fs/4 timer 5 output external clock	fosc/2 fosc/4 fosc/16 fosc/32 fs/2 fs/4 timer 5 output external clock
Maximum transfer rate	2.5 MHz	400 kHz
fosc : machine clock (high speed oscillation) fs : system clock [☞ Chapter 2 2-5. Clock Switching] At IIC communication, the transfer clock is the clock source divided by 3.		

12-1-2 Block Diagram

■Serial Interface 3 Block Diagram

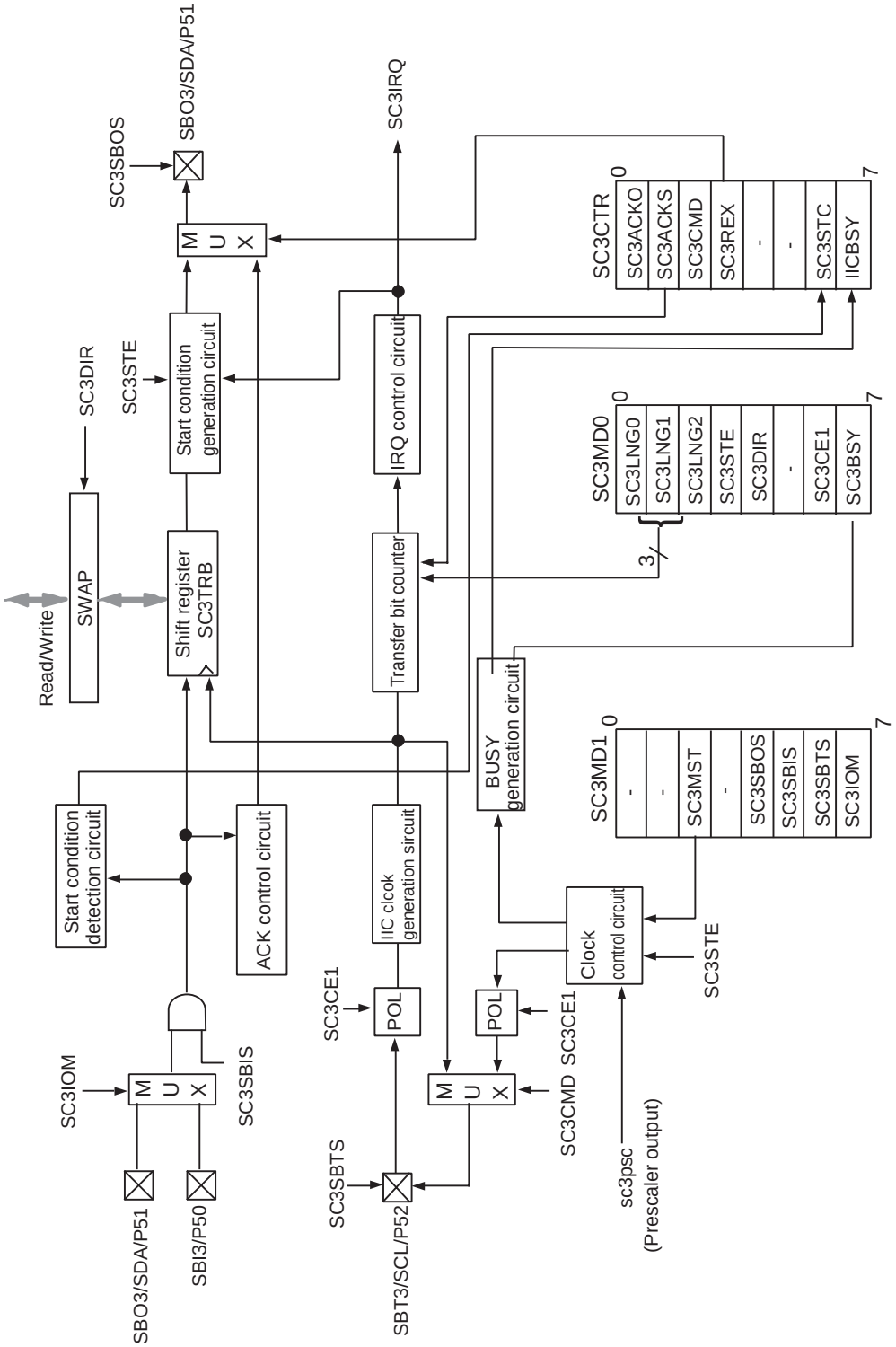


Figure 12-1-1 Serial Interface 3 Block Diagram

12-2 Control Registers

12-2-1 Registers

Table 12-2-1 shows the registers to control serial interface 3.

Table 12-2-1 Serial Interface 3 Control Registers

	Register	Address	R/W	Function	Page
Serial interface 3	SC3MD0	x'03FA8'	R/W	Serial interface 3 mode register 0	XIII - 6
	SC3MD1	x'03FA9'	R/W	Serial interface 3 mode register 1	XIII - 7
	SC3CTR	x'03FAA'	R/W	Serial interface 3 control register	XIII - 8
	SC3TRB	x'03FAB'	R/W	Serial interface 3 transmit/receive shift register	XIII - 5
	SC3ODC	x'03FAE'	R/W	Serial interface 3 port control register	XIII - 9
	SC3CKS	x'03FAF'	R/W	Serial interface 3 transfer clock selection register	XIII - 9
	PSCMD	x'03F6F'	R/W	Prescaler control register	V - 6
	P5DIR	x'03F35'	R/W	Port 5 direction control register	IV - 22
	P5PLU	x'03F45'	R/W	Port 5 pull-up control register	IV - 22
	SC3ICR	x'03FF9'	R/W	Serial interface 3 interrupt control register	III - 34

R / W : Readable / Writable

12-2-2 Data Register

Serial interface 3 has a 8-bit serial data register.

■Serial Interface 3 Transmit / Receive Shift Register (SC3TRB)

	7	6	5	4	3	2	1	0	
SC3TRB	SC3TRB7	SC3TRB6	SC3TRB5	SC3TRB4	SC3TRB3	SC3TRB2	SC3TRB1	SC3TRB0	(At reset: X X X X X X X X)

Figure 12-2-1 Serial Interface 3 Transmit/Receive Shift Register (SC3TRB : x'03FAB', R/W)

12-2-3 Mode Registers

■Serial Interface 3 Mode Register 0 (SC3MD0)

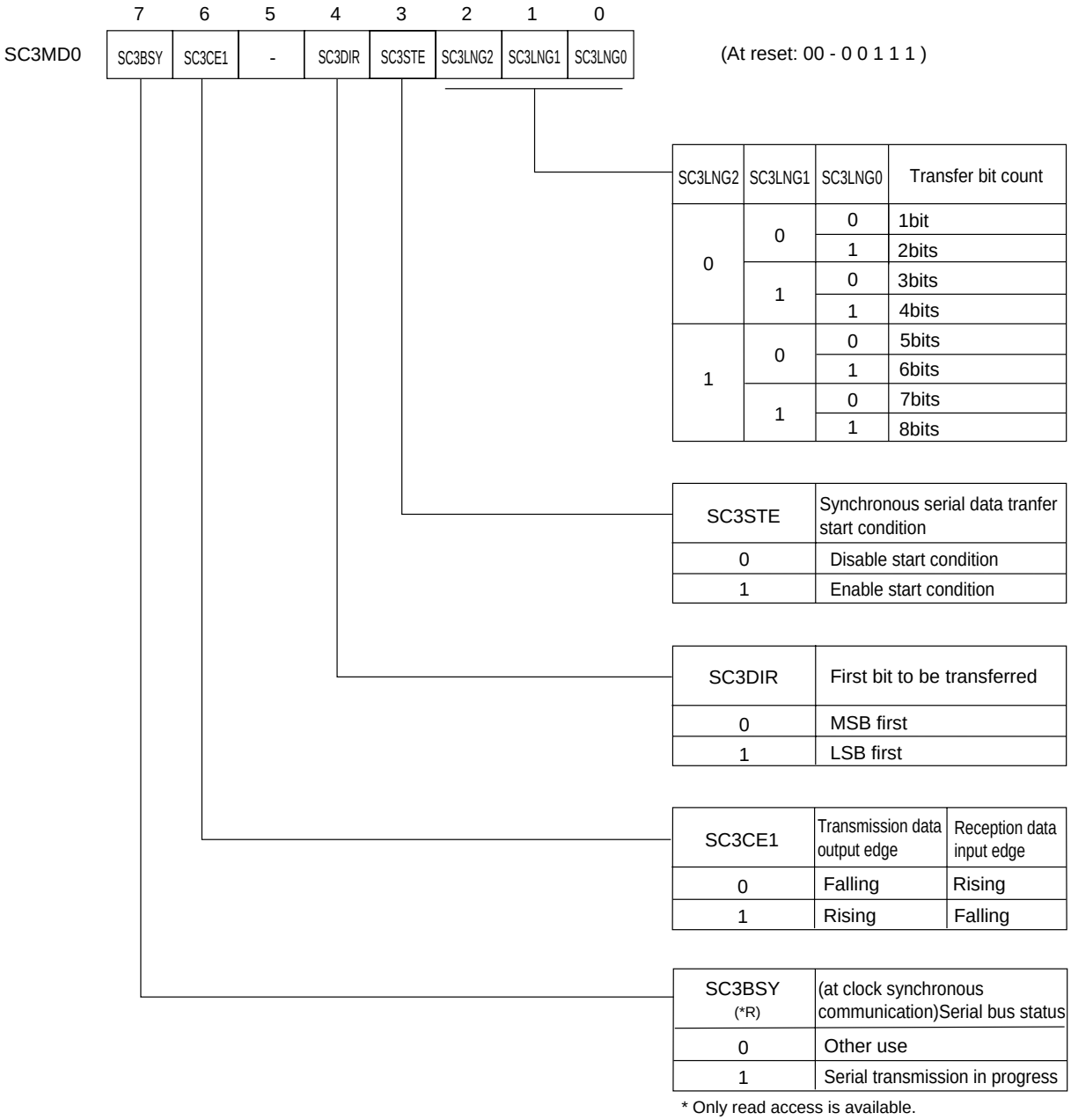


Figure 12-2-2 Serial Interface 3 Mode Register 0 (SC3MD0 : x'03FA8', R/W)

■Serial Interface 3 Mode Register 1 (SC3MD1)

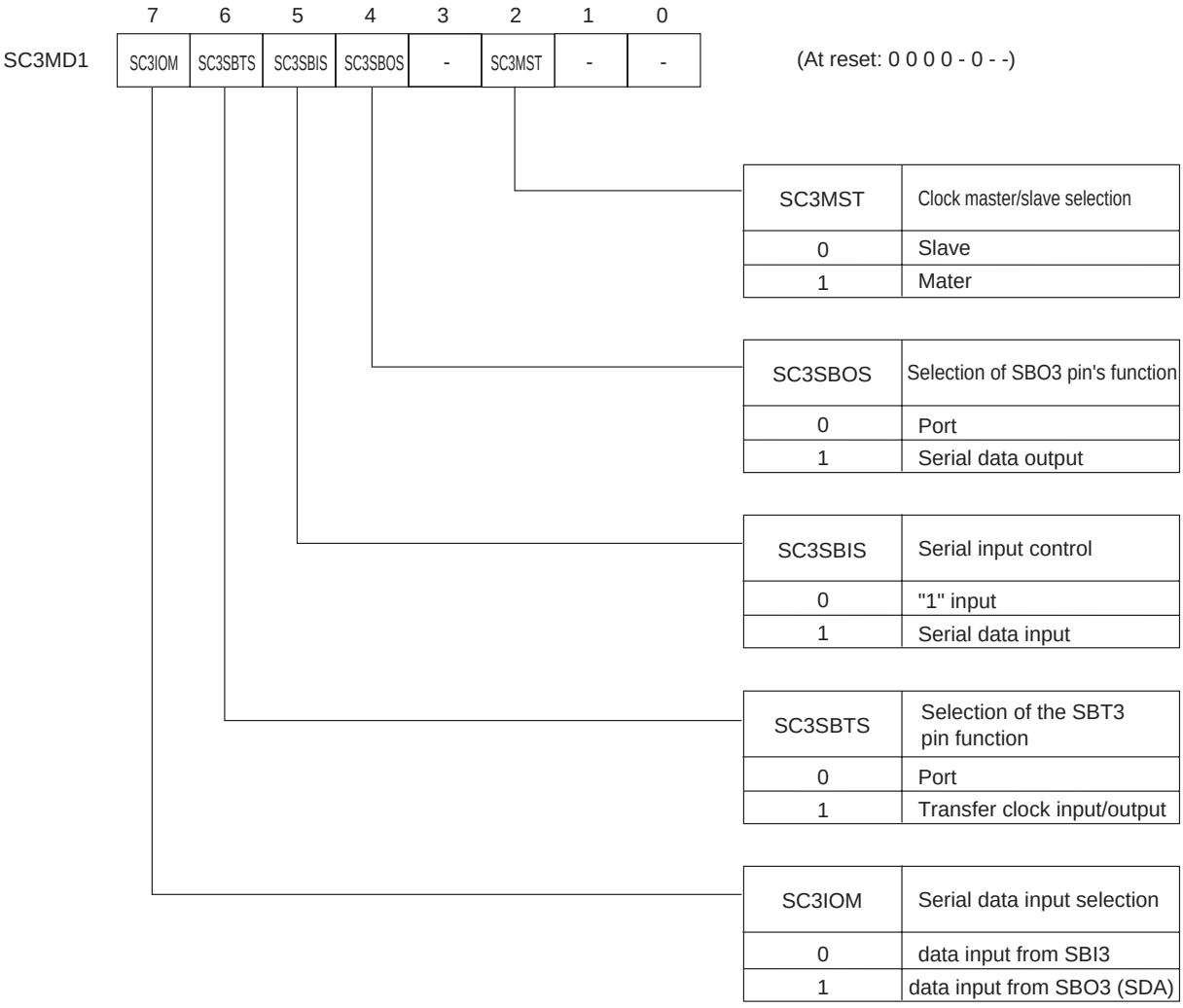


Figure 12-2-3 Serial Interface 3 Mode Register 1 (SC3MD1 : x'03FA9', R/W)

■Serial Interface 3 Control Register (SC3CTR)

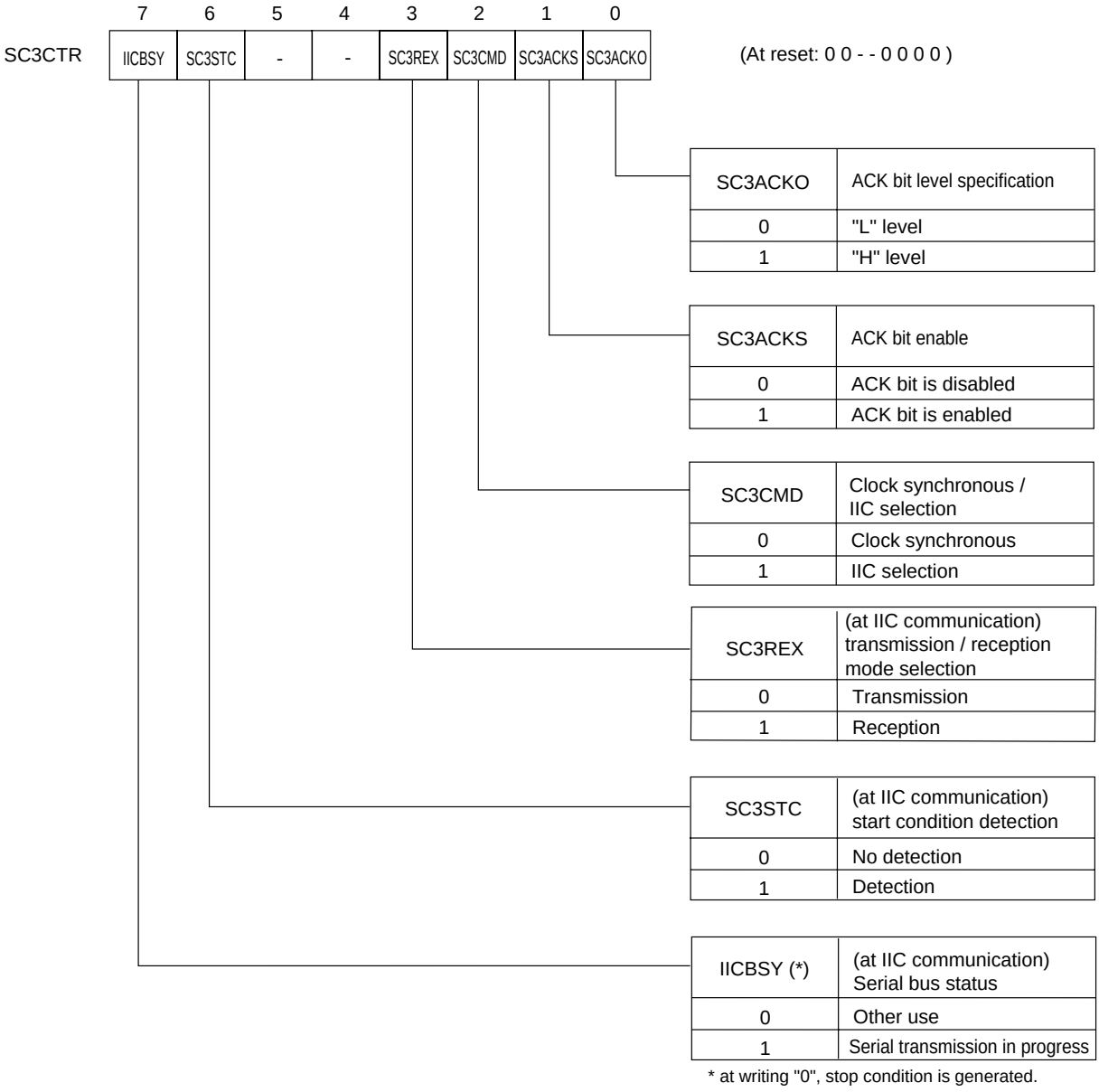


Figure 12-2-4 Serial Interface 3 Control Register (SC3CTR : x'03FAA', R/W)

■Serial Interface 3 Port Control Register (SC3ODC)

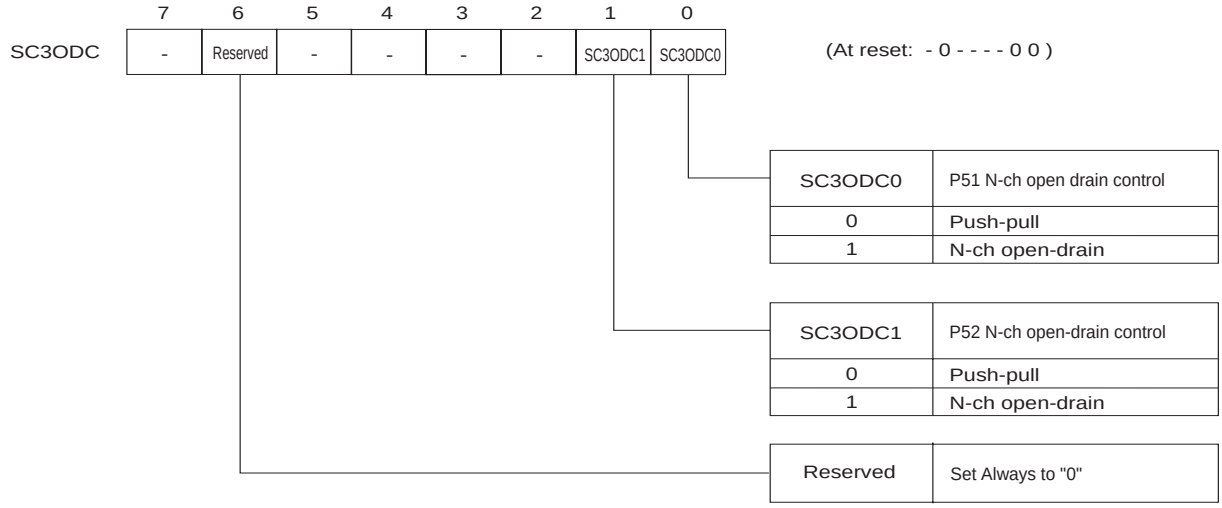


Figure 12-2-5 Serial Interface 3 Port Control Register (SC3ODC : x'03FAE', R/W)

■Serial Interface 3 Transfer Clock Selection Register (SC3CKS)

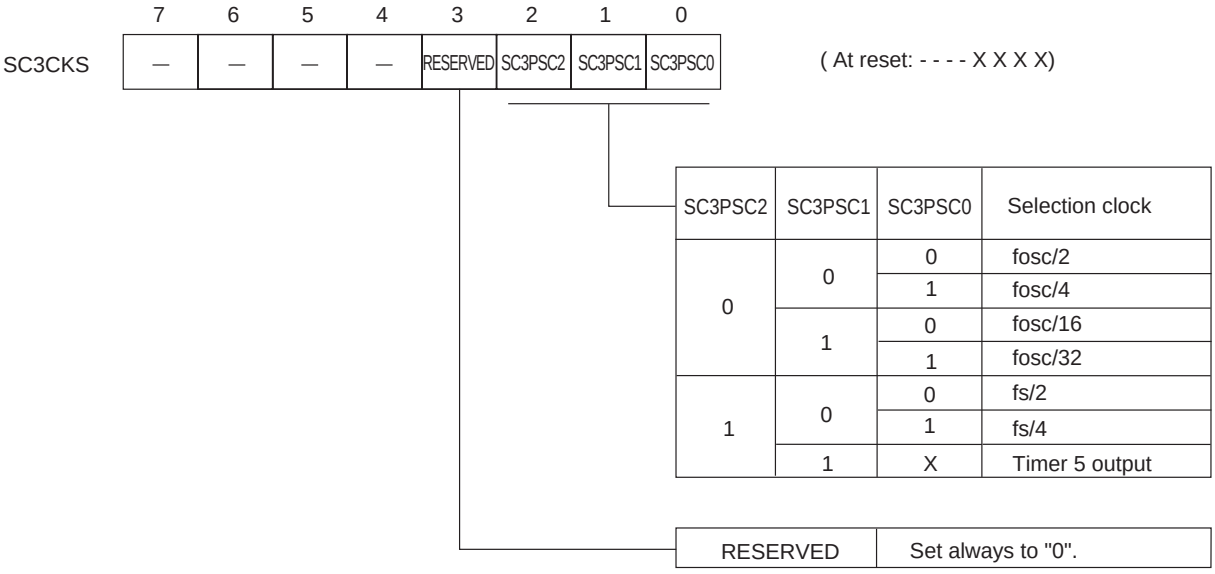


Figure 12-2-6 Serial Interface 3 Transfer Clock Selection Register (SC3CKS : x'03FAF', R/W)

12-3 Operation

This LSI contains a serial interface 3 that can be used for both communication types of clock synchronous and single master IIC.

12-3-1 Clock Synchronous Serial Interface

■Activation Factor for Communication

Table 12-3-1 shows the activation factor for communication. At master communication, the transfer clock is generated by setting data to the transmit/receive shift register SC3TRB, or by receiving start condition. The input signal from the SBT3 pin is masked inside of serial interface to prevent errors by noise except during communication. This mask is automatically released by setting data to SC3TRB (writing data to the SC3TRB register), or by inputting start condition to the data input pin. Therefore, at slave, input the external clock after setting data to SC3TRB, or by inputting start condition.

Table 12-3-1 Activation factor of Synchronous Serial Interface

<table>
<tr><td rowspan="2"></td><td colspan="2">Activation factor</td></tr>
<tr><td>transmission</td><td>reception</td></tr>
<tr><td rowspan="2">at master</td><td rowspan="2">Set transmission data</td><td>Set dummy data</td></tr>
<tr><td>Input start condition</td></tr>
<tr><td rowspan="2">at slave</td><td rowspan="2">Input clock after
transmission data is set</td><td>Input clock
after dummy data is set</td></tr>
<tr><td>Input clock
after start condition is input</td></tr>
</table>

■Transfer Bit Count Setup

The transfer bit count can be selected from 1 bit to 8 bits. Set it by the SC3LNG 2 to 0 flag of the SC3MD0 register (at reset : 111). The SC3LNG2 to 0 flag holds the previous set values till it is set again.

The SBT3 pin is masked inside serial to prevent errors by noise. At slave, input clock to the SBT3 pin after start condition is input or data is set to SC3TRB.

■Start Condition Setup

Start condition can be selected if it is enabled or not. Set by the SC3STE flag of the SC3MD0 register. When start condition is enabled. the transfer bit counter is cleared as start condition is input during communication, and after that, the communication is automatically started again. Start condition is enabled as data line (the SBI3 pin (with 3 channels) or the SBO3 pin (with 2 channels)) is changed from "H" to "L", when clock line (the SBT3 pin) is "H".

■First Transfer Bit Setup

The first bit to be transferred can be set by the SC3DIR flag of the SC3MD0 register. MSB first or LSB first can be selected.

■Transmit /Receive Data Buffer

Data register for transmission/reception is common. That is the transmit/receive shift register SC3TRB. The transmission data should be set to SC3TRB. The transfer clock outputs data by 1 bit in shift. The received data is stored to SC3TRB by 1 bit in shift.

■Transfer Bit Count and First Transfer Bit

At transmission, when the transfer bit count is 1 to 7 bits, data storage way to the transmit/receive shift register SC3TRB depends on the first transfer bit selection. When MSB is the first bit to be transferred, use the upper bits of SC3TRB for storage. In figure 12-3-1-1, if data "A" to "F" are stored to bp2 to bp7 of SC3TRB as the transfer bit count is 6 bits, data is transferred from "F" to "A". When LSB is the first bit to be transferred, use the lower bits of SC3TRB for storage. In figure 12-3-1-2, if data "A" to "F" are stored to bp0 to bp5 of SC3TRB, as the transfer bit count is 6 bits, data is transferred from "A" to "F".

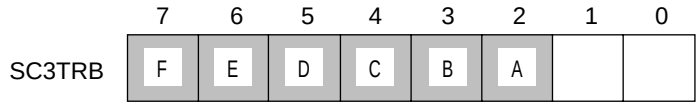


Figure 12-3-1-1 Transfer Bit Count and First Transfer Bit (at MSB first)

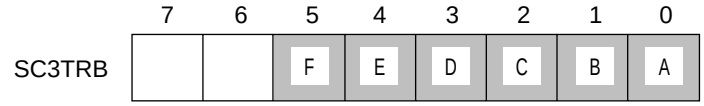


Figure 12-3-1-2 Transfer Bit Count and First Transfer Bit (at LSB first)

■Receive Bit Count and First Transfer Bit

At reception, when the transfer bit count is 1 to 7 bits, data storage way to the transmit/receive shift register SC3TRB depends on the first transfer bit selection. When MSB is the first bit to be transferred, the lower bits of SC3TRB are used for storage. In figure 12-3-1-3, as the transfer bit count is 6 bits, data "A" to "F" are stored to bp0 to bp5 of SC3TRB, and they are transferred from "F" to "A". When LSB is the first bit to be transferred, use the upper bits of SC3TRB for storage. In figure 12-3-1-4, data "A" to "F" are stored to bp2 to bp7 of SC3TRB, as the transfer bit count is 6 bits, and they are transferred from "A" to "F".

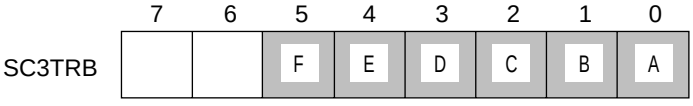


Figure 12-3-1-3 Receive Bit Count and First Transfer Bit (at MSB first)

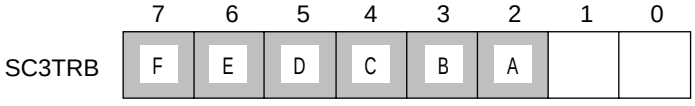


Figure 12-3-1-4 Receive Bit Count and First Transfer Bit (at LSB first)

■Continuous Communication

Serial interface 3 can be started by automatic data transfer function ATC1, built-in this LSI. If ATC1 is used for activation, data can be continuously transferred up to 255 byte. The communication blank, from the generation of the communication complete interrupt SC3IRQ to the generation of the next transfer clock, is up to 18 machine cycles + 2 transfer clocks. For activation by ATC1, refer to chapter 14 Automatic Transfer Controller, Transfer mode 6 to 7.

If start condition is input for activation again, during communication, the transmission data becomes invalid. If the transmission should be operated again, set the transmission data to SC3TRB, again.

■Clock Setup

Clock source is selected from the dedicated prescaler by the SC3CKS register and timer 5 output. The dedicated prescaler is started by selecting "prescaler operation" by the PSCMD (x'03F6F') register. The SC3MST flag of the SC3MD1 register can select the internal clock (clock master), or the external clock (clock slave). Even if the external clock is selected, the internal clock with same frequency to the external clock, should be set by the SC3CKS register, because the internal clock generates the interrupt flag SC3IRQ. Table 12-3-2 shows the internal clock source which can be set by the SC3CKS register.

Table 12-3-2 Synchronous Serial Interface Internal Clock Source

Communication type	Clcok synchronous
Clock source (internal clock)	fosc/2
	fosc/4
	fosc/16
	fosc/32
	fs/2
	fs/4
	timer 5 output

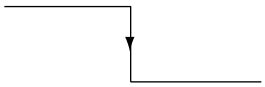
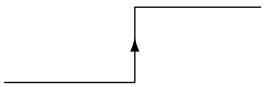
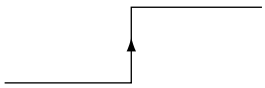
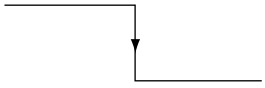
■BUSY Flag

If data is set to the transmit/receive shift register SC3TRB, or start condition is enabled, the busy flag SC3BSY is set. That is cleared by the generation of the communication complete interrupt SC3IRQ.

■Input edge/Output edge Setup

The SC3CE1 flag of the SC3MD0 register can set the output edge of the transmission data, and the input edge of the received data. Data at transmission is output at the falling edge of clock as the SC3CE1 flag = "0", and at the rising edge of clock as the SC3CE1 = "1". Data at reception is input at the rising edge of clock as the SC3CE1 = "0", and at the falling edge of clock as the SC3CE1 flag = "1".

Table 12-3-3 Input Edge/Output Edge of Transmission/Received Data

SC3CE1	Transmission data output edge	Received data input edge
0		
1		

■Data Input Pin Setup

There are 2 communication modes to be selected : 3 channels type (clock pin(SBT3 pin), data output pin (SBO3 pin), data input pin (SBI3 pin)), 2 channels type (clock pin (SBT3 pin), data I/O pin (SBO3 pin)). The SBI3 pin can be used only for serial data input. The SBO3 pin can be used for serial data input or output. The SC3IOM flag of the SC3MD1 register can specify if serial data is input from the SBI3 pin, or the SBO3 pin. When "data input from the SBO3 pin" is selected to communicate with 2 channels, the SBO3 pin's direction control by the P5DIR3 flag of the P5DIR register can switch the transmission / reception. At that time, the SBI3 pin is not used, so that it can be used as a general port.

■Forced Reset at Communication

It is possible to shut down the communication. A forced reset is operated by setting both of the SC3SBOS flag and the SC3SBIS flag of the SC3MD1 register to "0" (the SBO3 pin function : port, input data : input "1"). When a forced reset is operated, the SC3BSY flag of the SC3MD0 register, and the IICBSY flag of the SC3CTR register are cleared, but other control registers hold their set values.

■Last Bit of Transfer Data

Table 12-3-4 shows the data output holding period of the last bit at transmission, and the minimum data input period of the last bit at reception. At slave, setup for the internal clock is needed to keep data holding time at data transmission. After the last bit data output holding period, "H" is output.

Table 12-3-4 Last Bit Data Length of Transmission Data

	at transmission the last bit data holding period	at reception the last bit data input period
at master	1 bit data length	1 bit data length (minimum)
at slave	[1 bit data length of external clock x 1/2] + [internal clock cycle x (1/2 to 3/2)]	

Transfer rate should be up to 2.5 MHz. If the transfer rate is over 2.5 MHz, the transmission data cannot be output correctly.

■Transmission Timing

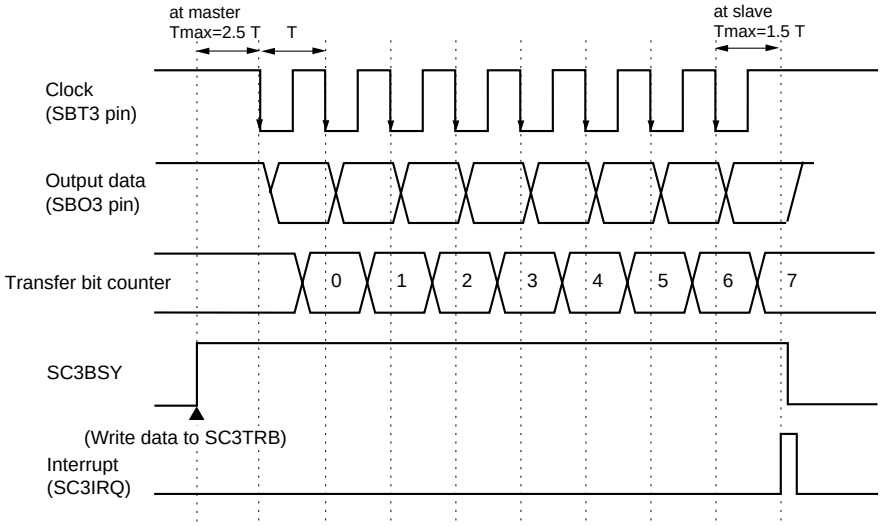


Figure 12-3-2 Transmission Timing (Falling edge, Enable Start Condition)

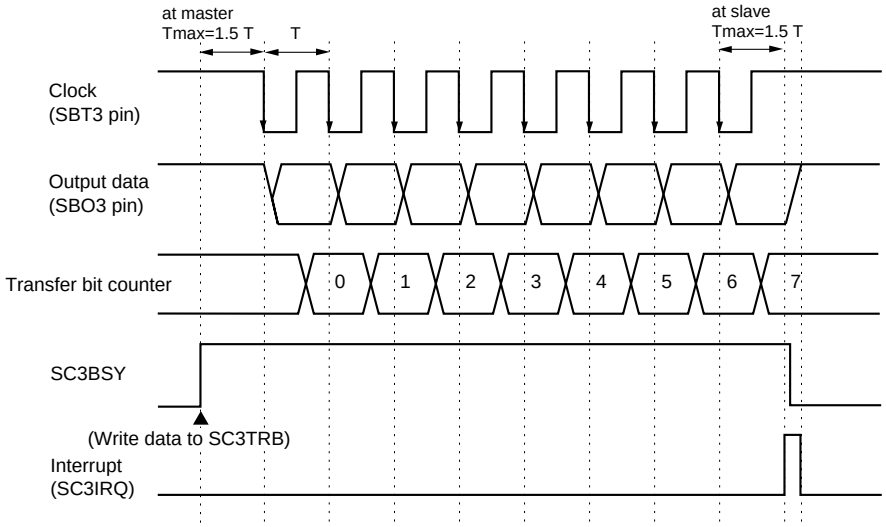


Figure 12-3-3 Transmission Timing (Falling edge, Disable Start Condition)

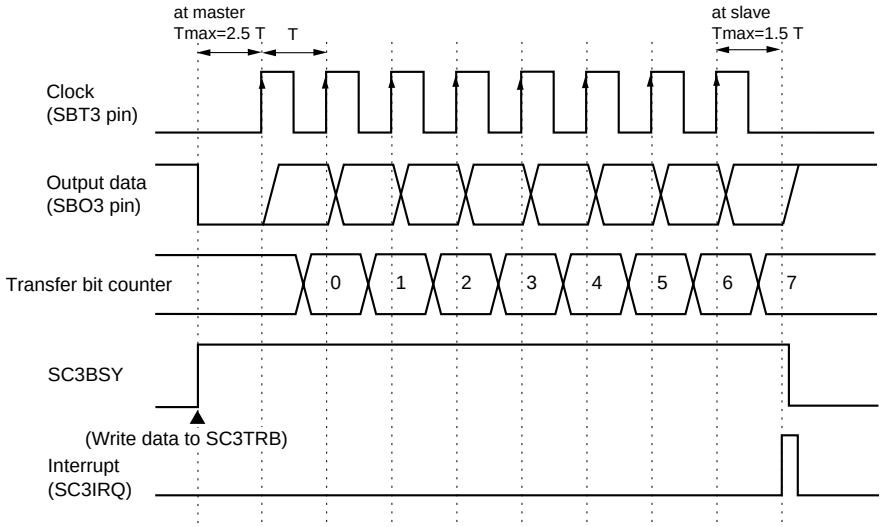


Figure 12-3-4 Transmission Timing (Rising edge, Enable Start Condition)

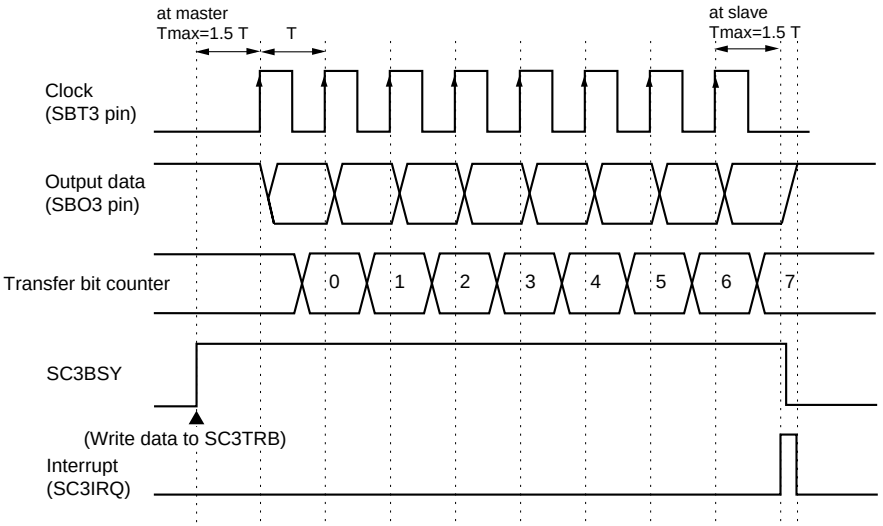


Figure 12-3-5 Transmission Timing (Rising edge, Disable Start Condition)

■Reception Timing

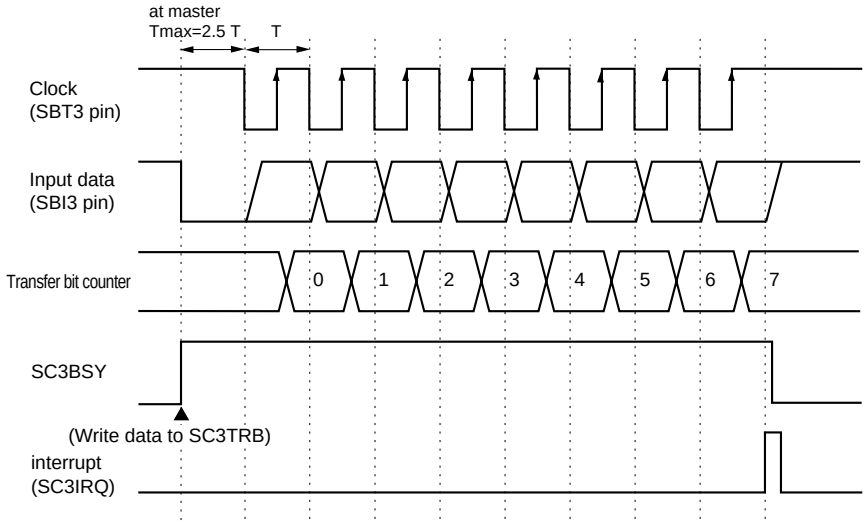


Figure 12-3-6 Reception Timing (Rising edge, Enable Start Condition)

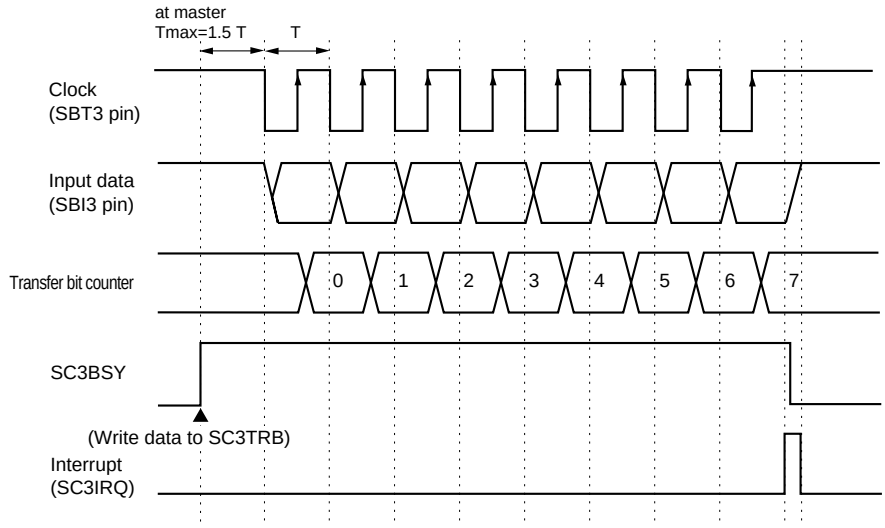


Figure 12-3-7 Reception Timing (Rising edge, Disable Start Condition)

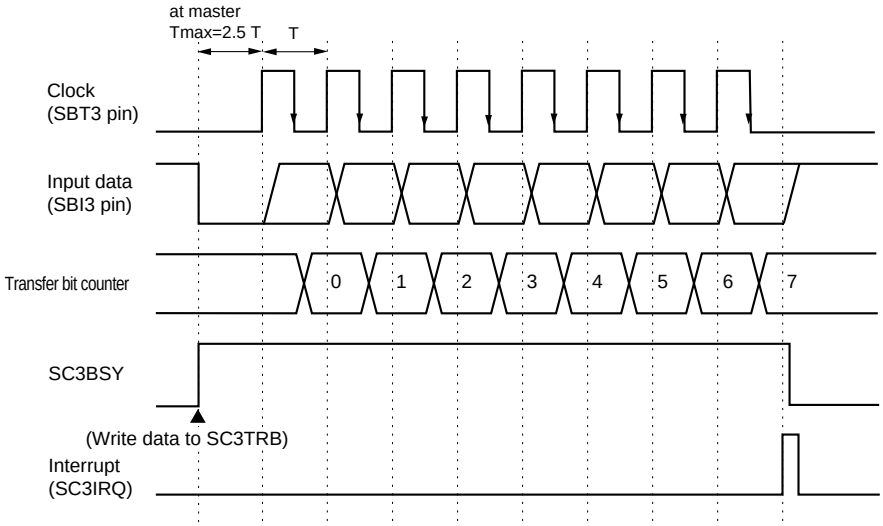


Figure 12-3-8 Reception Timing (Falling edge, Enable Start Condition)

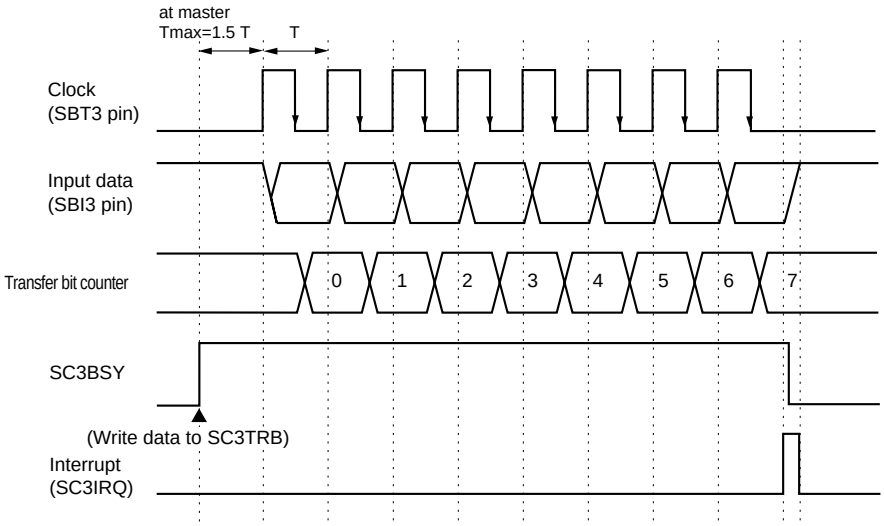


Figure 12-3-9 Reception Timing (Falling edge, Disable Start Condition)

■Transmission/Reception Simultaneous timing

When transmission and reception are operated at the same time, data is recieved at the opposite edge of the transmission clock.

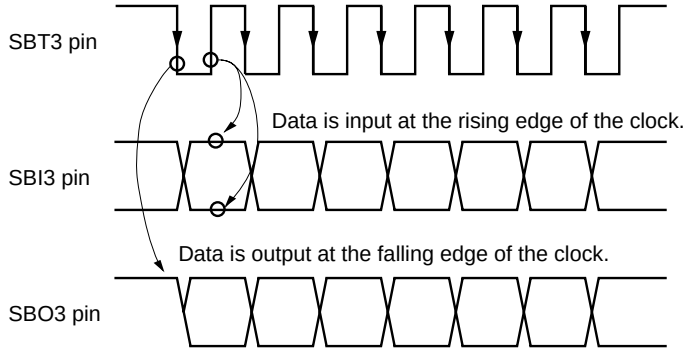


Figure 12-3-10 Transmission/Reception Timing (Reception : Rising edge, Transmission : Falling edge)

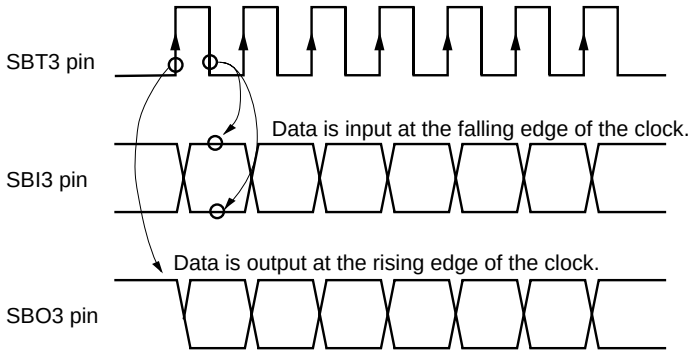


Figure 12-3-11 Transmission/Reception Timing (Reception : Falling edge, Transmission : Rising edge)

■Pin Setup (3 channels, at transmission)

Table 12-3-5 shows the pins setup at synchronous serial interface transmission with 3 channels (SBO3 pin, SBI3 pin, SBT3 pin).

Table 12-3-5 Synchronous Serial Interface Pin Setup (3 channels, at transmission)

Item	Data output pin	Data input pin	Clock I/O pin	
	SBO3 pin	SBI3 pin	SBT3 pin	
			Internal clock	External clock
Pin	P51	P50	P52	
SBI3/SBO3 pin	SBI3/SBO3 independent		-	
	SC3MD1(SC3IOM)			
Function	Serial data output	Input "1"	Serial clock I/O	Serial clock I/O
	SC3MD1(SC3SBOS)	SC3MD1(SC3SBIS)	SC3MD1(SC3SBTS)	
Type	Push-pull/ N-ch open-drain	-	Push-pull/ N-ch open-drain	Push-pull/ N-ch open-drain
	SC3ODC(SC3ODC0)		SC3ODC(SC3ODC1)	
I/O	Output mode	-	Output mode	Input mode
	P5DIR(P5DIR1)		P5DIR(P5DIR2)	
Pull-up	added/not added	-	added/not added	added/not added
	P5PLU(P5PLU1)		P5PLU(P5PLU2)	

■Pin Setup (3 channels, at reception)

Table 12-3-6 shows the pins setup at synchronous serial interface reception with 3 channels (SBO3 pin, SBI3 pin, SBT3 pin).

Table 12-3-6 Synchronous Serial Interface Pin Setup (3 channels, at reception)

Item	Data output pin	Data input pin	Clock I/O pin	
	SBO3 pin	SBI3 pin	SBT3 pin	
			internal clock	external clock
Pin	P51	P50	P52	
SBI3/SBO3 pin	SBI3/SBO3 independent		-	
	SC3MD1(SC3IOM)			
Function	Port	Serial data input	Serial clock I/O	Serial clock I/O
	SC3MD1(SC3SBOS)	SC3MD1(SC3SBIS)	SC3MD1(SC3SBTS)	
Type	-	-	Push-pull/ N-ch open-drain	Push-pull/ N-ch open-drain
			SC3ODC(SC3ODC1)	
I/O	-	Input mode	Output mode	Input mode
		P5DIR(P5DIR0)	P5DIR(P5DIR2)	
Pull-up	-	-	added/not added	added/not added
			P5PLU(P5PLU2)	

■Pin Setup (3 channels, at transmission/reception)

Table 12-3-7 shows the pins setup at synchronous serial interface transmission/reception with 3 channels (SBO3 pin, SBI3 pin, SBT3 pin).

Table 12-3-7 Synchronous Serial Interface Pin Setup (3 channels, at transmission/reception)

Item	Data output pin	Data input pin	Clock I/O pin	
	SBO3 pin	SBI3 pin	SBT3 pin	
			Internal clock	External clock
Pin	P51	P50	P52	
SBI3/SBO3 pin	SBI3/SBO3 independent		-	
	SC3MD1(SC3IOM)			
Function	Serial data output	Input "1"	Serial clock I/O	Serial clock I/O
	SC3MD1(SC3SBOS)	SC3MD1(SC3SBIS)	SC3MD1(SC3SBTS)	
Type	Push-pull/ N-ch open-drain	-	Push-pull/ N-ch open-drain	Push-pull/ N-ch open-drain
	SC3ODC(SC3ODC0)		SC3ODC(SC3ODC1)	
I/O	Output mode	Intput mode	Output mode	Input mode
	P5DIR(P5DIR1)	P5DIR(P5DIR0)	P5DIR(P5DIR2)	
Pull-up	added/not added	-	added/not added	added/not added
	P5PLU(P5PLU1)		P5PLU(P5PLU2)	

■Pin Setup (2 channels, at transmission)

Table 12-3-8 shows the pins setup at synchronous serial interface transmission with 2 channels (SBO3 pin, SBT3 pin). The SBI3 pin is not used, so that it can be used as a general port.

Table 12-3-8 Synchronous Serial Interface Pin Setup (2 channels, at transmission)

Item	Data output pin	Data input pin	Clock I/O pin	
	SBO3 pin	SBI3 pin	SBT3 pin	
			Internal clock	External clock
Pin	P51	P50	P52	
SBI3/SBO3 pin	SBI3/SBO3 independent		-	
	SC3MD1(SC3IOM)			
Function	Serial data output	Input "1"	Serial clock I/O	Serial clock I/O
	SC3MD1(SC3SBOS)	SC3MD1(SC3SBIS)	SC3MD1(SC3SBTS)	
Type	Push-pull/ N-ch open-drain	-	Push-pull/ N-ch open-drain	Push-pull/ N-ch open-drain
	SC3ODC(SC3ODC0)		SC3ODC(SC3ODC1)	
I/O	Output mode	-	Output mode	Input mode
	P5DIR(P5DIR1)		P5DIR(P5DIR2)	
Pull-up	added/not added	-	added/not added	added/not added
	P5PLU(P5PLU1)		P5PLU(P5PLU2)	

■Pin Setup (2 channels, at reception)

Table 12-3-9 shows the pins setup at synchronous serial interface reception with 2 channels (SBO3 pin, SBT3 pin). The SBI3 pin is not used, so that it can be used as a general port.

Table 12-3-9 Synchronous Serial Interface Pin Setup (2 channels, at reception)

Item	Data output pin	Data input pin	Clock I/O pin	
	SBO3 pin	SBI3 pin	SBT3 pin	
			Internal clock	External clock
Pin	P51	P50	P52	
SBI3/SBO3 pin	SBI3/SBO3 independent		-	
	SC3MD1(SC3IOM)			
Function	Port	Serial data input	Serial clock I/O	Serial clock I/O
	SC3MD1(SC3SBOS)	SC3MD1(SC3SBIS)	SC3MD1(SC3SBTS)	
Type	-	-	Push-pull/ N-ch open-drain	Push-pull/ N-ch open-drain
			SC3ODC(SC3ODC1)	
I/O	Input mode	-	Output mode	Input mode
	P5DIR(P5DIR1)		P5DIR(P5DIR2)	
Pull-up	-	-	added/not added	added/not added
			P5PLU(P5PLU2)	

13-3-2 Setup Example

■Transmission/Reception Setup Example

Here is the setup example for transmission/reception with serial interface 3. Table 12-3-10 shows the conditions.

Table 12-3-10 Setup conditions for Synchronous Serial Interface Transmission/Reception

Item	Set to	Item	Set to
SBI3/SBO3 pin	independent (with 3 lines)	Clock	internal clock
Transfer bit count	8 bits	Clock source	fs/2
Start condition	enable	SBT3/SBO3 pin type	N-ch open-drain
First bit to be transfered	MSB	Pull-up resistance of SBT3 pin	added
Input edge	at falling	Pull-up resistance of SBO3 pin	added
Output edge	at rising		

An example setup procedure, with a description of each step is shown below.

Setup Procedure	Description
(1) Select prescaler operation. PSCMD (x'3F6F') bp0 : PSCEN = 1	(1) Set the PSCEN flag of the PSCMD register to "1" to select prescaler operation.
(2) Select the clock source. SC3CKS (x'3FAF') bp2-0 : SC2PSC2-0 = 100 bp3 = 0	(2) Set the SC3PSC2-0 flag of the SC3CKS register to "100" to select fs/2 at clock source. Set bp3 of the SC3CKS register to "0", always.
(3) Control the pin type. SC3ODC (x'3FAE') bp1-0 : SC3ODC1-0 = 11 P5PLU (x'3F45') bp2, 1 : P5PLU2, 1 = 1, 1	(3) Set the SC3ODC1-0 flag of the SC3ODC register to "11" to select N-ch open drain for the SBO3/ SBT3 pin's type. Set the P5PLU2-1 flag of the P5PLU register to "1, 1" to add pull-up resistor.
(4) Control the pin direction. P5DIR (x'3F35') bp2-0 : P5DIR2-0 = 110	(4) Set the P5DIR2-0 flag of P5 pin control direction register (P5DIR) to "110" to set P52, P51, to output mode, to set P50 to input mode.
(5) Select the communication type. SC3CTR (x'3FAA') bp2 : SC3CMD = 0	(5) Set the SC3CMD flag of the serial 3 control register (SC3CTR) to "0" to select synchronous serial.

Setup Procedure	Description
(6) Select the transfer bit count. SC3MD0 (x'3FA8') bp2-0 : SC3LNG2-0 = 111	(6) Set the SC3LNG2-0 flag of the serial 3 mode register (SC3MD0) to "111" to set the transfer bit count to 8 bits.
(7) Select the start condition. SC3MD0 (x'3FA8') bp3 : SC3STE = 1	(7) Set the SC3STE flag of the SC3MD0 register to "1" to enable start condition.
(8) Select the first transfer bit. SC3MD0 (x'3FA8') bp4 : SC3DIR = 0	(8) Set the SC3DIR flag of the SC3MD0 register to "0" to set MSB as the first bit to be transferred.
(9) Select the transfer edge. SC3MD0 (x'3FA8') bp6 : SC3CE1 = 1	(9) Set the SC3CE1 flag of the SC3MD0 register to "1" to set the transmission data output edge to "rising", and the received data input edge to "falling".
(10) Select the transfer clock. SC3MD1 (x'3FA9') bp2 : SC3MST = 1	(10) Set the SC3MST flag of the SC3MD1 register to "1" to select clock master (internal clock).
(11) Control the pin function. SC3MD1 (x'3FA9') bp4 : SC3SBOS = 1 bp5 : SC3SBIS = 1 bp6 : SC3SBTS = 1 bp7 : SC3IOM = 0	(11) Set the SC3SBOS, SC3SBIS, SC3SBTS flags of the SC3MD1 register to "1" to set the SBO3 pin to serial data output, the SBI3 pin to serial data input, and the SBT3 pin to serial clock I/O. Set the SC3IOM flag to "0" to set "serial data input from the SBI3 pin".
(12) Set the other mode register. SC3CTR (x'3FAA') bp7-6, 3, 1-0	(12) At IIC communication, that flag should be set. At synchronous serial communication, no need to be set.
(13) Set the interrupt level. SC3ICR (x'3FF9') bp7-6 : SC3LV1-0 = 10	(13) Set the interrupt level by the SCLV1-0 flag of the serial 3 interrupt control register (SC3ICR).
(14) Enable the interrupt. SC3ICR (x'3FF9') bp1 : SC3IE = 1	(14) Enable the interrupt to the SC3IE flag of the SC3ICR register. If the interrupt request flag (SC3IR of the SC3ICR register) is already set, clear SC3IR before the interrupt is enabled. [☞ Chapter 3 3-1-4. Interrupt Flag Setup]

Setup Procedure	Description
(15) Start serial transmission. Transmission data → SC3TRB (x'3FAB')	(15) Set the transmission data to the serial transmit/receive shift register SC3TRB. The internal clock is generated to start transmission/reception. After the communication is finished, the serial 3 interrupt SC3IRQ is generated.

Note : In the above settings, (6) to (9), (10) to (11),can be set at once.

If the communication is only for transmission, the data that input by setting the SC3SBIS of the SC3MD1 register to "0" should be fixed to "1". The SBI3 pin can be used as a general port.

If the communication is only for reception, set the SC3SBOS of the SC3MD1 register to "0" to select port. The SBO3 pin can be used as a general port.

If the communication is with 2 channels connected the SBO3/SBI3 pins, the SBO3 pin inputs/outputs serial data. The port direction control register P5DIR switches I/O.
At reception, set the SC3SBIS of the SC3MD1 register to "1" to select "input serial data". The SBI3 pin can be used as a general port.

It is possible to shut down the communication. When the communication should be stopped by force, set the SC3SBOS and the SC3SBIS of the SC3MD1 register to "0".

Setup for each flag should be done in order. The activation of communication should be operated after all control registers (table 12-2-1 : except SC3TRB) are set.

The SC3CKS register should set the transfer rate of the transfer clock to "under 2.5 MHz".

12-3-3 Single Master IIC Interface

IIC serial communication in single master is available at serial interface 3. Communication of this IIC interface is based on the data transfer format of Philips, IIC-BUS.

Table 12-3-11 shows the functions of IIC serial interface.

Table 12-3-11 IIC Serial Interface Functions

Communication type	IIC (single master)
Interrupt	SC3IRQ
Pin	SDA, SCL
Transfer bit count	1 to 8 bit
First transfer bit	√
ACK bit	√
ACK bit level	√
Clock source	fosc/2 fosc/4 fosc/16 fosc/32 fs/2 fs/4 timer 5 output
The transfer rate is the clock source divided by 3.	

■Activation factor for Communication

Set data (at transmission) or dummy data (at reception) to the transmit/receive shift register SC3TRB. Start condition and transfer clock are generated to start communication, regardless of transmission/ reception. This serial interface can not be used for slave communication.

■Start Condition Setup

At IIC communication, enable start condition by the SC3STE flag of the SC3MD0 register at the beginning of communication. The SC3STE flag of the SC3MD0 register can select if start condition is enabled or not.

If start condition is detected during data communication when the start condition is enabled, the SC3STC flag of the SC3CTR register is set to "1", and the communication complete interrupt SC3IRQ is generated to finish the transmission. At this case, the communication is not normal so that something should be done by the software, such a counter measure of stop condition, and the communication should be started again.

The SC3STC flag should be cleared by the software.

Start condition is generated as data line (SDA pin) is changed from "H" to "L", when clock line (the SLC pin) is "H".

■Generation of Stop Condition

Stop condition is generated as the SDA line is changed from "L" to "H", when the SCL line is "H". Stop condition can be generated by setting the IICBSY flag of the SC3CTR register to "0" by the software. When the IICBSY flag is "0", use the program with data output function of a general port.

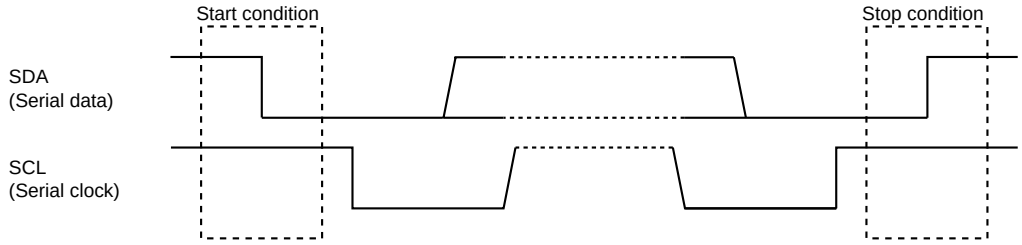


Figure 12-3-12 Start Condition and Stop Condition

■Input Edge/Output Edge Setup

At IIC communication, data is always received at the falling edge of clock. Set the SC3CE1 flag of the SC3MD0 register to "1", and select "falling" at the received data input edge. Even if the SC3CE1 flag is set to "0", the received data is stored at the falling edge of clock, but any error is generated because IIC clock line (SCL) becomes "H" after the communication of the last data.

At IIC communication, set the SC3CE1 flag of the SC3MD0 register to "1" to select "falling" of the received data input edge.

■Data I/O Pin Setup

The SDA pin (for SBO3 pin, too) is used to input/output data. Set the SC3IOM flag of the SC3MD1 register to "1" to input serial data from the SBO3 pin. The SBI3 pin is not used, so it can be used as a general port. But, always set the SC3SBIS flag of the above register to "1" to set "input serial data".

To detect start condition, set the SC3SBIS flag of the SC3MD1 register to "input serial data", regardless of transmission/reception.

■Reception of Acknowledgement (ACK) Bit after Data Transmission

This LSI does not contain the function of receiving the acknowledgement (ACK) bit after data transmission. To receive ACK bit after transmitting data, select sc3acks= "0" (No ACK bit) before data transmisison. By transmitting the 8-bit data, an interrupt generates. Then switch the SBT pin function to "port" in the interrupt routine. With the port function, program a clock for ACK reception and read the ACK data.

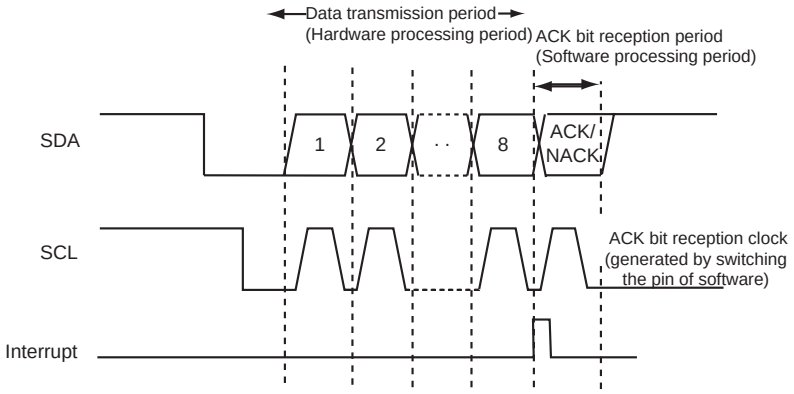


Figure 12-3-13 ACK Bit Reception Timing after Transmission of 8-Bit Data

■Transmission of Acknowledgement (ACK) bit after Data Reception

The way of the selection if ACK bit is enabled or not is the same to the way at the transmission. When ACK bit is enabled, ACK bit and clock are output after data (1 to 8 bits) is received. If the reception is to continue, ACK bit outputs "L". And if the reception is to finish, it outputs "H". The SC3ACK0 of the SC3CTR register sets the output ACK bit level.

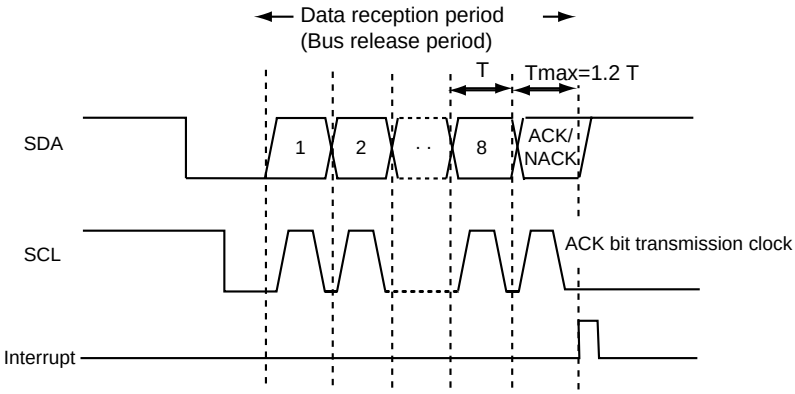


Figure 12-3-14 ACK Bit Transmission Timing after Reception of 8-Bit Data

■Transfer Format

On IIC bus, there are 2 transfer formats : the addressing format that transmits/receives data after 1 byte data (address data) that consists of slave address (7 bits) and R/W bit (1 bit) is transferred after start condition, and the free data format that transmits data after start condition. The serial interface of this LSI supports 2 communication formats for only master transmission and master reception at IIC communication. Sequence of communication is as follows. The shaded part is shown the data, transferred from slave.

[☞ Figure 12-3-16 Master Transmission Timing, Figure 12-3-17 Master Reception Timing]

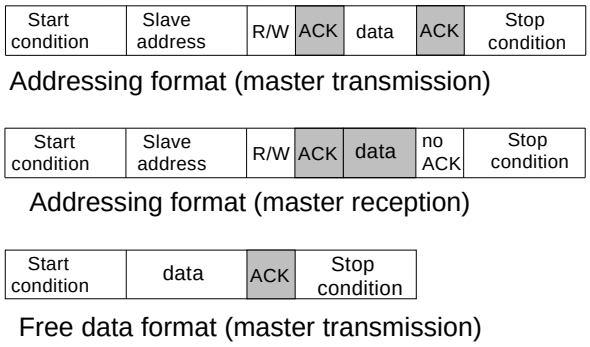


Figure 12-3-15 Communication Sequence on Each Transfer Format

■Clock Setup

The transfer clock of IIC communication is the one that the clock source is divided by 3 inside of this serial. The clock source is selected from the dedicated prescaler and timer 5 output by the SC3CKS register. But clock source should be set so that the transfer rate is not over 400 kHz. The dedicated prescaler starts as the PSCMD (x'03F6F') register selects "prescaler operation". Set the SC3MST flag of the SC3MD1 register to "1" to select the internal clock (clock master), always. This IIC interface can not be used as the external clock (clock slave).

Table 12-3-12 IIC Interface Clock Source

Communication type	Single master IIC
Clcok source (internal clock)	fosc/2
	fosc/4
	fosc/16
	fosc/32
	fs/2
	fs/4
	timer 5 output

The transfer rate at IIC communication should be the one that clock source is divided by 3. The clock source should be set so that the transfer rate is under 400 kHz by the SC3CKS register.

■Transmission/Reception Mode Setup and Operation

The SC3REX flag of the SC3CTR register selects the status of the transmission or the reception. The first data is always added start condition for communication. The start condition is output from the master, this serial.

If the communication is continued (no stop condition is generated), start condition should not be added from the next data. At this case, start condition is set to be disabled in the interrupt service routine after the first data communication is finished. At addressing format, slave address and R/W bit are set to the first data after start condition for transmission.

At master reception, switch to the reception mode at the interrupt transaction after the transmission of the first 1 byte data is finished, after the ACK signal from slave is confirmed. If the communication should be continued to other device without stop, transmit slave address and R/W bit again after start condition is generated again. At reception, the SDA line is automatically released to wait for reception. After the storage of data is finished, confirmation of the reception (ACK bit) is output.

[☞ Figure 12-3-16 Master Transmission Timing, Figure 12-3-17 Master Reception Timing]

■IICBUSY Flag Operation

As data is set to the transmit/receive shift register SC3TRB, the IICBSY flag of the SC3CTR register is set to "1". The IICBSY flag is cleared by software. As the IICBSY flag is cleared, the stop condition is automatically generated to complete the communication.

If start condition is detected during communication, the communication complete interrupt SC3IRQ is generated, then the IICBSY flag is automatically cleared.

■Seaquence Communication

At IIC communication, not the same to the clock synchronous serial communication, the seaquence communication with built-in automatic transfer controller ATC1, is not available.

The following items are the same to the clock synchronous serial. Refer to the following pages.

■First Transfer Bit Setup

Refer to : XII-11

■Transmit, Reception Data Buffer

Refer to : XII-11

■Transfer Bit Count and First Transfer Bit

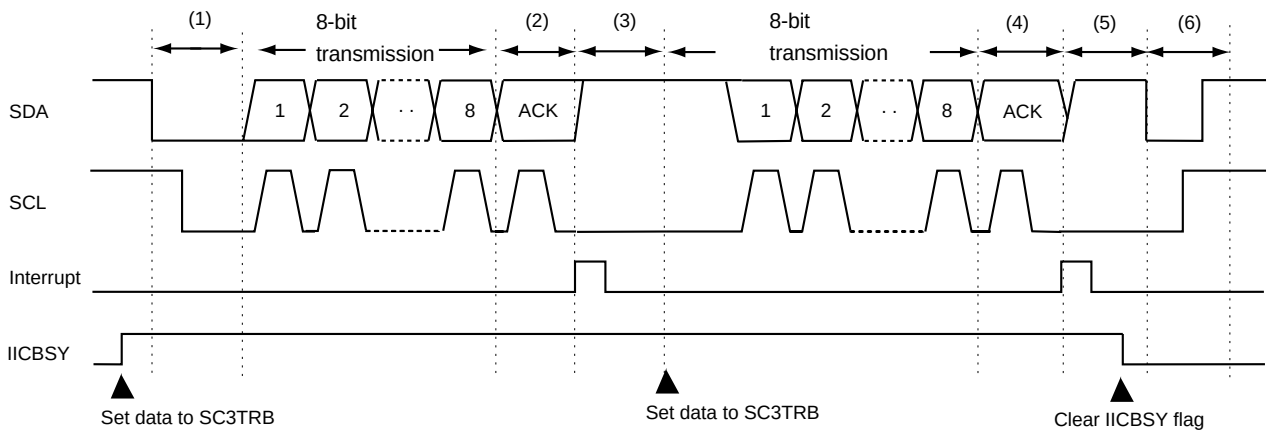
Refer to : XII-11

■Communication Forced Reset

Refer to : XII-13

At communication, set Nch-open drain for pin's type, because the hardware switches if bus is used/released. And even at reception, select the SDA pin (the SBO3 pin) direction control to "output".

■Master Transmission Timing



(1) Output start condition.

(2) Bus released period, ACK bit is received.

(3) Interrupt transaction.
- Disable start condition : SC3STE = 1 →0
- Start communication : set data to SC3TRB

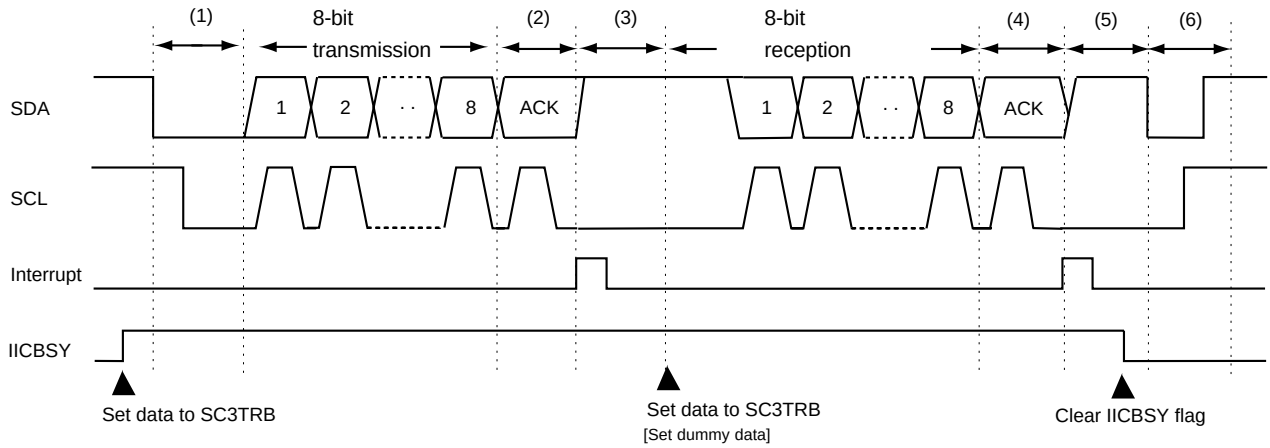
(4) Receive ACK bit.

(5) Interrupt transaction.
- Finish communication : clear the IICBSY flag.

(6) Generates stop condition.

Figure 12-3-16 Master Transmission Timing

■Master Reception Timing



(1) Output start condition.

(2) Bus released period, ACK bit is received.

(3) Interrupt transaction
- Setup for the reception mode : SC3REX = 0 →1
- Disable start condition : SC3STE = 1 →0
- Start communication : set data to SC3TRB.

(4) Output ACK bit.

(5) Bus released period, interrupt transaction
- Complete communication : clear IICBSY flag

(6) Generate stop condition.

Figure 12-3-17 Master Reception Timing

■Pin Setup (2 channels, at transmission)

Table 12-3-13 shows the pins setup at IIC serial interface transmission with 2 channels (SDA pin, SCL pin).

Table 12-3-13 Pin Setup (2 channels, at transmission)

Item	Data output pin	Data input pin
	SDA pin	SCL pin
Pin	P51	P52
SBI3/SBO3 pin	SBI3/SBO3 connection	-
	SC3MD1(SC3IOM)	
Function	Serial data output	Serial clock output
	SC3MD1(SC3SBOS)	SC3MD1(SC3SBIS)
	Serial data input	-
	SC3MD1(SC3SBIS)	
Type	Push-pull/ N-ch open-drain	Push-pull/ N-ch open-drain
	SC3ODC (SC3ODC0)	SC3ODC (SC3ODC1)
I/O	Output mode	Output mode
	P5DIR(P5DIR1)	P5DIR(P5DIR2)
Pull-up	added/not added	added/not added
	P5PLU (P5PLU1)	P5PLU (P5PLU2)

■Pin Setup (2 channels, at reception)

Table 12-3-14 shows the pins setup at IIC serial interface reception with 2 channels (SDA pin, SCL pin).

Table 12-3-14 Pin Setup (2 channels, at reception)

Item	Data output pin	Data input pin
	SDA pin	SCL pin
Pin	P51	P52
SBI3/SBO3 pin	SBI3/SBO3 connection	-
	SC3MD1(SC3IOM)	
Function	Port	Serial clock output
	SC3MD1(SC3SBOS)	SC3MD1(SC3SBIS)
	Serial data input	-
	SC3MD1(SC3SBIS)	
Type	Push-pull/ N-ch open-drain	Push-pull/ N-ch open-drain
	SC3ODC (SC3ODC0)	SC3ODC (SC3ODC1)
I/O	Output mode	Output mode
	P5DIR(P5DIR1)	P5DIR(P5DIR2)
Pull-up	added/not added	added/not added
	P5PLU (P5PLU1)	P5PLU (P5PLU2)

12-3-4 Setup Example

■Master Transmission Setup Example

Here is the setup example for the transmission of the plural data to the all devices on IIC bus with IIC interface function of serial 3. Figure 12-3-15 shows the conditions.

Figure 12-3-15 Conditions Single Master IIC Communication Setup

Item	Set to	Item	Set to
SBI3/SBO3 pins	Connection (with 2 lines)	Clock source	fs/2
Transfer bit count	8 bits	SCL/SDA pin's type	N-ch open-drain
Start condition	enable	Pull-up resistance of SCL pin	added
First transfer bit	MSB	Pull-up resistance of SDA pin	added
ACK bit	enable		

An example setup procedure, with a description of each step is shown below.

Setup Procedure	Description
(1) Select prescaler operation. PSCMD (x'3F6F') bp0 : PSCEN = 1	(1) Set the PSCEN flag of the PSCMD register to "1" to select prescaler operation.
(2) Select the clock source. SC2CKS (x'3FAF') bp2-0 : SC3PSC2-0 = 100 bp3 = 0	(2) Set the SC3PSC2-0 flag of the SC3CKS register to "100" to select fs/2 at clock source. Set bp3 of the SC3CKS register to "0", always.
(3) Control the pin type. SC3ODC (x'3FAE') bp1-0 : SC3ODC1-0 = 11 P5PLU (x'3F45') bp2-1 : P5PLU2-1 = 1, 1	(3) Set the SC3ODC1, 0 flag of the SC3ODC register to "11" to select N-ch open drain for the SDA/SCL pin type. Set the P5PLU2-1 flag of the P5PLU register to "1, 1" to add pull-up resistor.
(4) Control the pin direction. P5DIR (x'3F35') bp2-1 : P5DIR2-1 = 1, 1	(4) Set the P5DIR2-1 flag of P5 pin control direction register (P3DIR) to "1, 1" to set P52, P51, to output mode.

Setup Procedure	Description
(5) Set ACK bit. SC3CTR (x'3FAA') bp0 : SC3ACKO = x bp1 : SC3ACKS = 1	(5) Set the SC3ACKS flag of the serial 3 control register (SC3CTR) to "1" to select "receive ACK bit". At transmission, ACK bit is received, so that the SC3ACKS flag does not need to set the ACK bit level.
(6) Select the communication type. SC3CTR (x'3FAA') bp2 : SC3CMD = 1	(6) Set the SC3CMD flag of the serial 3 control register (SC3CTR) to "1" to select IIC.
<Transmission setup>	
(7) Select the transmission/reception mode. SC3CTR (x'3FAA') bp3 : SC3REX = 0	(7) Set the SC3REX flag of the serial 3 control register (SC3CTR) to "0" to select the transmission mode.
(8) Initialize the monitor flag. SC3CTR (x'3FAA') bp6 : SC3STC = 0 bp7 : IICBSY = 0	(8) Set the SC3STC flag and the IICBSY flag of the serial 3 control register (SC3CTR) to "0, 0" to initialize the start condition detection flag and the BUSY flag.
(9) Set the SC3MD0 register. Select the transfer bit count. SC3MD0 (x'3FA8') bp2-0 : SC3LNG2-0 = 111	(9) Set the SC3LNG2-0 flag of the serial 3 mode register (SC3MD0) to "111" to set the transfer bit count to 9 bits.
(10) Select the start condition. SC3MD0 (x'3FA8') bp3 : SC3STE = 1	(10) Set the SC3STE flag of the SC3MD0 register to "1" to enable start condition.
(11) Select the first bit to be transferred. SC3MD0 (x'3FA8') bp4 : SC3DIR = 0	(11) Set the SC3DIR flag of the SC3MD0 register to "0" to set MSB as the first bit to be transferred.
(12) Select the IIC communication edge. SC3MD0 (x'3FA8') bp6 : SC3CE1 = 1	(12) At IIC communication, set the SC3CE1 flag of the SC3MD0 register to "1", always.

Setup Procedure	Description
(13) Select the transfer clock. SC3MD1 (x'3FA9') bp2 : SC3MST = 1	(13) Set the SC3MST flag of the SC3MD1 register to "1" to select clock master (internal clock). At IIC communication, external clock should not be selected.
(14) Control the pin function. SC3MD1 (x'3FA9') bp4 : SC3SBOS = 1 bp5 : SC3SBIS = 1 bp6 : SC3SBTS = 1 bp7 : SC3IOM = 1	(14) Set the SC3SBOS, SC3SBIS, SC3SBTS flags of the SC3MD1 register to "1" to set the SDA pin (the SBO3 pin) to serial data output, the SBI3 pin to serial data input, and the SCL pin (the SBT3 pin) to serial clock I/O. Set the SC3IOM flag to "1" to set "serial data input from the SDA pin (the SBO3 pin)".
(15) Set the interrupt level. SC3ICR (x'3FF9') bp7-6 : SC3LV1-0 = 10	(15) Set the interrupt level by the SCLV1-0 flag of the serial 3 interrupt control register (SC3ICR).
(16) Enable the interrupt. SC3ICR (x'3FF9') bp1 : SC3IE = 1 <Transmission is started.>	(16) Enable the interrupt to the SC3IE flag of the SC3ICR register. If the interrupt request flag (SC3IR of the SC3ICR register) is already set, clear SC3IR before the interrupt is enabled. [☞ Chapter 3 3-1-4. Interrupt Flag Setup]
(17) Start serial transmission. Confirm that SCL (P52) is "H". Transmission data → SC3TRB (x'3FAB') <Transmission is completed.> <Setup for the next data transmission>	(17) Set the transmission data to the transmit/ receive shift register SC3TRB. Then the transfer clock is generated to start transmission. If the ACK bit is received after data transmission, the communication complete interrupt SC3IRQ is generated.
(18) Judge the monitor flag. SC3CTR (x'3FAA') bp6 : SC3STC	(18) Confirm the SC3STC flag of the serial 3 control register (SC3CTR). When the former transmission is completed in normal, SC3STC = "0". If SC3STC = "1", the communication should be operated again.

Setup Procedure	Description
(19) Judge the ACK bit level. SC3CTR (x'3FAA') bp0 : SC3ACKO	(19) Confirm the level of the ACK bit, received by the SC3ACKS flag of the serial 3 control register (SC3CTR). When SC3ACKO = 0, the transmission is continued. When SC3ACKO = 1, the reception at slave may be impossible, finish the communication.
(20) Select the transfer bit count. SC3MD0 (x'3FA8') bp2-0 : SC3LNG2-0 = 0	(20) If the transfer bit count is changed, set the transfer count bit by the SC3LNG2-0 flag of the serial 3 mode register (SC3MD0).
(21) Select the start condition. SC3MD0 (x'3FA8') bp3 : SC3STE = 0	(21) Set the SC3STE flag of the SC3MD0 register to "0" to disable start condition.
<The next data transmission is started.> (22) Serial transmission is started. [→ (17)]	(22) Set the transmission data to SC3TRB to start the transmission. [→ (17)]
<The transmission is finished.>	
<Transaction after IIC communication> (23) Clear BUSY flag. SC3CTR (x'3FAA') bp7 : IICBSY = 0	(23) Clear the IICBSY flag of the serial 3 control register (SC3CTR) to "0". Then, the stop condition is automatically generated to finish the communication.

Note : In the above (5) to (8), (9) to (12), (13) to (14), (15) to (16), (18) to (19) and (20) to (21), settings can be set at once.

It is possible to shut down the communication. When the communication should be stopped by force, set the SC3SBOS and the SC3SBIS of the SC3MD1 register to "0".

Setup for each flag should be done in order. The activation of communication should be done after all control registers (except table 13-2-1 : SC3TRB) are set.

The SC3CKS register should set the transfer clock so that the transfer rate is "under 400 kHz".

To detect start condition, connect the SBO3/SBI3 pins to be 2 channels. The SDA pin inputs/outputs serial data.

At communication, select Nch-open drain for the pin type, because the bus should be switched to be used/released by the hardware. And even at the reception, select the SDA pin (the SBO3 pin) direction control to "output".

Chapter 13 Serial Interface 4

13

13-1 Overview

This LSI contains a serial interface 4, which is compatible with IIC serial interface (slave) communication.

13-1-1 Functions

Table 13-1-1 shows the functions of serial interface 4.

Table 13-1-1 Serial interface 4 Functions List

Communication type	IIC (slave)
Interrupt	SC4IRQ
Pin	SDA, SCL
Addressing	7 bits / 10 bits
General call	√
Maximum transfer rate	400 kHz (High-speed mode)

13-1-2 Block Diagram

■Serial interface 4 Block Diagram

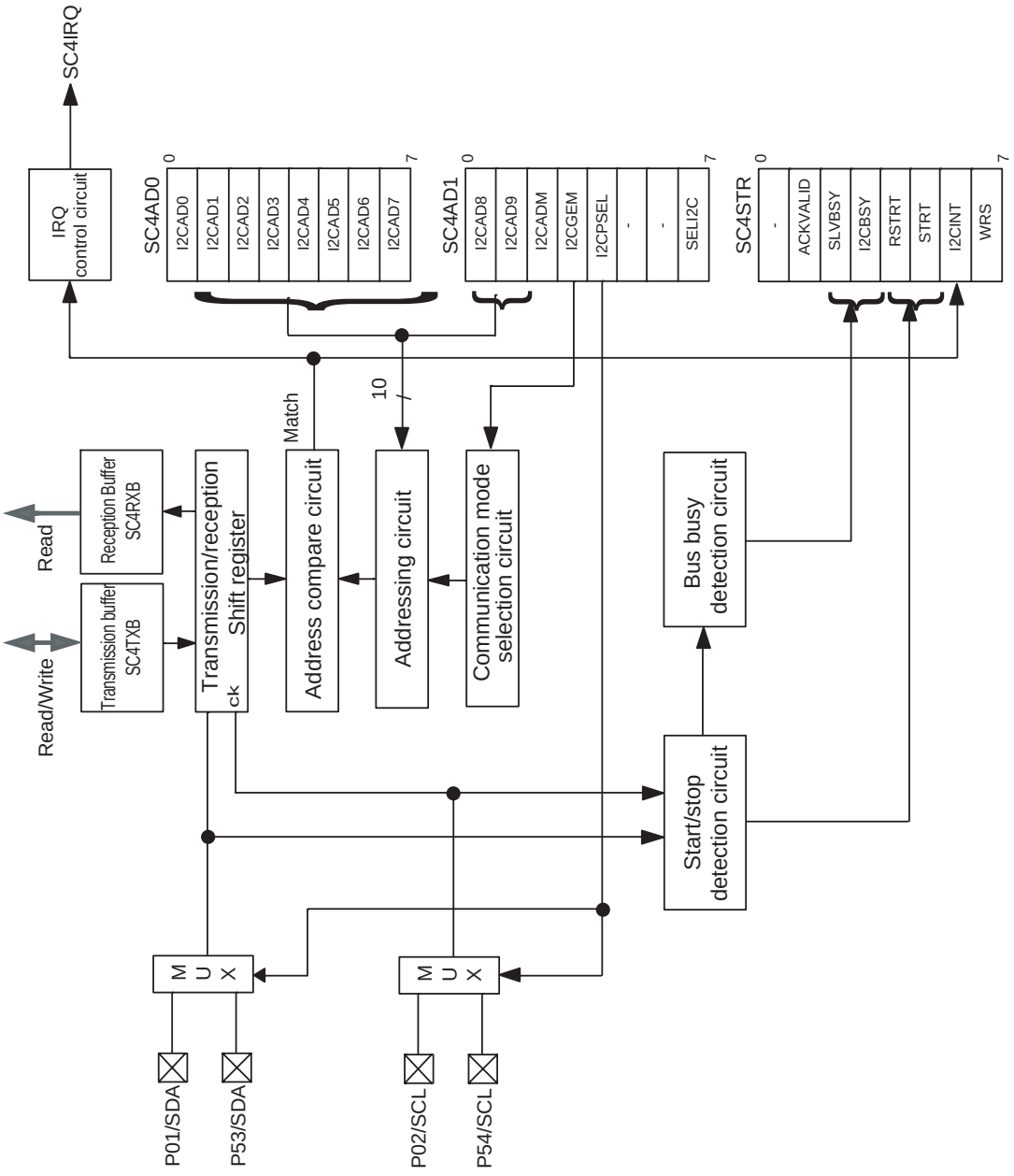


Figure 13-1-1 Serial interface 4 Block Diagram

13-2 Control Registers

13-2-1 Registers

Table 13-2-1 shows the registers to control serial interface 4.

Table 13-2-1 Serial interface 4 Control Registers

	Register	Address	R/W	Function	Page
IIC	SC4AD0	x'03FA3'	R/W	Serial interface 4 addressing register 0	XIII - 6
	SC4AD1	x'03FA4'	R/W	Serial interface 4 addressing register 1	XIII - 6
	SC4TXB	x'03FA5'	R/W	Serial interface 4 transmission data buffer	XIII - 5
	SC4RXB	x'03FAD'	R	Serial interface 4 reception data buffer	XIII - 5
	SC4STR	x'03FAC'	R	Serial interface 4 status register	XIII - 7
	P0DIR	x'03F30'	R/W	Port 0 direction control register	IV - 7
	P0PLU	x'03F40'	R/W	Port 0 pull-up resistor control register	IV - 7
	P0OUT	x'03F10'	R/W	Port 0 output control register	IV - 7
	P5DIR	x'03F35'	R/W	Port 5 direction control register	IV - 22
	P5PLU	x'03F45'	R/W	Port 5 pull-up resistor control register	IV - 22
	P5OUT	x'03F15'	R/W	Port 5 output control register	IV - 22
	SC4ODC0	x'03F3F'	R/W	Serial interface 4 port control register 0	XIII - 8
	SC4ODC1	x'03F3D'	R/W	Serial interface 4 port control register 1	XIII - 8
	SC4ICR	x'03FF3'	R/W	Serial interface 4 interrupt control register	X III - 35

R / W : Readable / Writable

13-2-2 Data Register

Serial interface 4 has a 8-bit buffer registers for transmission/reception.

■Serial interface 4 Reception Data Buffer (SC4RXB)

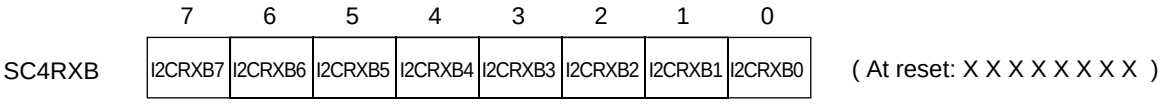


Figure 13-2-1 Serial interface 4 Reception Data Buffer (SC4RXB : x'03FAD', R)

■Serial interface 4 Transmission Data Buffer (SC4TXB)

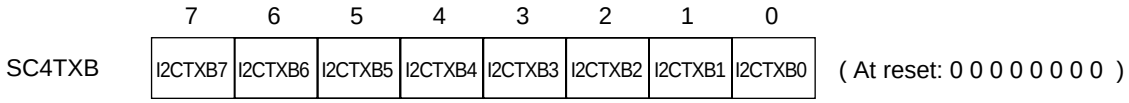


Figure 13-2-2 Serial interface 4 Transmission Data Buffer (SC4TXB : x'03FA5', R/W)

13-2-3 Mode Registers

■Serial interface 4 Addressing Register 0 (SC4AD0)

	7	6	5	4	3	2	1	0	
SC4AD0	I2CAD7	I2CAD6	I2CAD5	I2CAD4	I2CAD3	I2CAD2	I2CAD1	I2CAD0	(At reset: 0 0 0 0 0 0 0 0)

Figure 13-2-3 Serial interface 4 Addressing Register 0 (SC4AD0 : x'03FA3', R/W)

■Serial interface 4 Addressing Register 1 (SC4AD1)

	7	6	5	4	3	2	1	0	
SC4AD1	SELI2C	RESERVED	RESERVED	I2CPSEL	I2CGEM	I2CADM	I2CAD9	I2CAD8	(At reset: 0 0 0 0 0 0 0 0)

I2CADM	Address mode selection
0	7 bits address mode
1	10 bits address mode

I2CGEM	Communication mode selection
0	Normal communication mode
1	General call communication mode

I2CPSEL	Communication port selection
0	P53(SDA), P54(SCL)
1	P01(SDA), P02(SCL)

RESERVED	Set always to "0"

RESERVED	Set always to "0"

SELI2C	Reset control
0	Reset
1	Operational state

Figure 13-2-4 Serial interface 4 Addressing Register 1 (SC4AD1 : x'03FA4', R/W)

■Serial interface 4 Status Register (SC4STR)

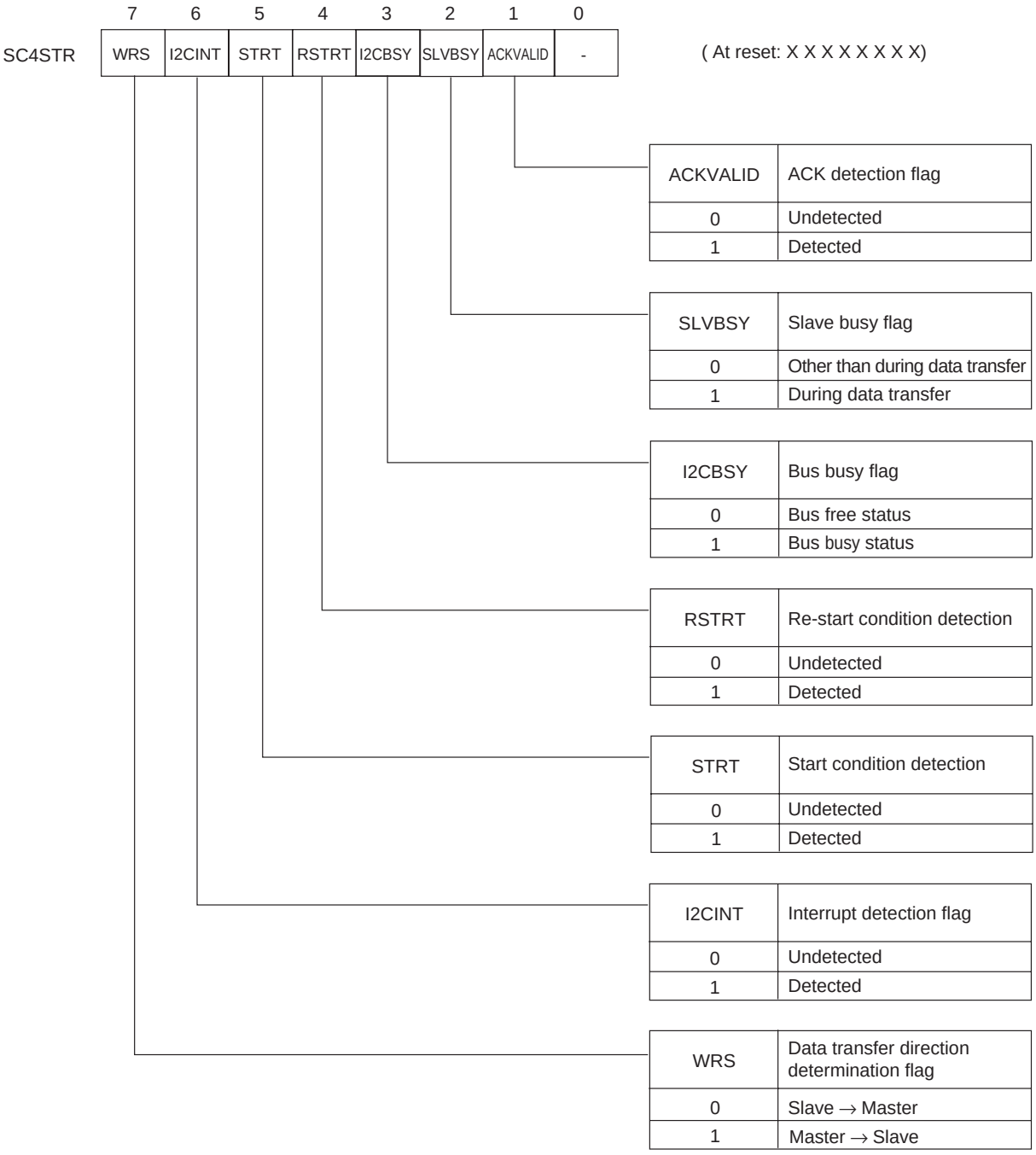
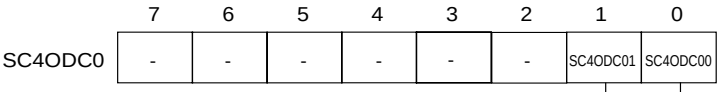


Figure 13-2-5 Serial interface 4 Status Register (SC4STR : x'03FAC', R)

■Serial interface 4 Port Control Register 0 (SC4ODC0)



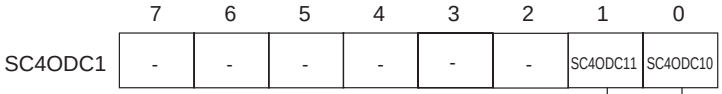
(At reset: - - - - - - 0 0)

SC4ODC00	P01 N-ch open drain control
0	Push-pull
1	N-ch open-drain

SC4ODC01	P02 N-ch open drain control
0	Push-pull
1	N-ch open-drain

Figure 13-2-6 Serial interface 4 Port Control Register 0 (SC4ODC0 : x'03F3F', R/W)

■Serial interface 4 Port Control Register 1 (SC4ODC1)



(At reset: - - - - - - 0 0)

SC4ODC10	P53 N-ch open drain control
0	Push-pull
1	N-ch open-drain

SC4ODC11	P54 N-ch open drain control
0	Push-pull
1	N-ch open-drain

Figure 13-2-7 Serial interface 4 Port Control Register 1 (SC4ODC1 : x'03F3D', R/W)

13-3 Operation

■Activation and Termination Factors

Set the SELI2C flag of the SC4AD1 register to "1" to activate this serial interface. For the termination, set the flag to "0". The ports used for communication can be used as general-purpose port while the serial interface is not in operative state. When the SELI2C register is set to "0", SC4AD0 register, SC4TXB register and SC4RXB register is automatically cleared.

■Slave Address Setup

This serial interface can seletct either 7 bits or 10 bits slave address. To select 7 bits slave address, set the I2CADM flag of the SC4AD1 register to "0" to select 7 bits address mode, and set the slave address to upper 7 bits of the SC4AD0 register (I2CAD7 to I2CAD1). To select 10 bits slave address, set the I2CADM flag of the SC4AD1 register to "1" to select 10 bits address mode, and set the upper 2 bits of the slave address to lower 2 bits of the SC4AD1 register (I2CAD9, I2CAD8) and set the lower 8 bits of the slave address to SC4AD0 register.

■General Call Communitacion

This serial interface is compatible with general call communication mode. Set the I2CGEM flag of the SC4AD1 register to "1" to select general call communication mode. In this mode, slave address set in the SC4AD0 and SC4AD1 registers are invalid.

■Data Transmission/Reception

This serial interface enables automatic address determination after detection of start condition on IIC bus. Serial interface 4 interrupt (SC4IRQ) is generated only when address transmitted from master matches with the set slave address. Data transmission/reception are controlled with the WRS flag of the SC4STR register, and slave transmission is selected when the WRS flag is set to "0", slave reception is selected when the WRS flag is set to "1". In slave transmission, setting the transmission data to SC4TXB register opens the bus line and data transmission is started by the clock transmitted from master. In slave reception, setting the dummy data to SC4RXB register opens the bus line and data reception is started by the clock transmitted from master.

■Start/Re-Start Condition Detection

When data (SDA) pin changes from "H" to "L" while clock (SCL) pin is "H", start condition is detected and the STRT flag of the SC4STR register is set to "1". The STRT flag is cleared to "0" after communication data is set when the interrupt routine right after the slave address reception sets the communication data. If start condition is detected again during data transferring, the RSTRT flag is set. This flag is cleared to "0" after communication data is set when the interrupt routine right after the slave address reception sets the communication data.

If address transmitted from master does not match with the slave address, these flags are automatically cleared at the timing when address miscompare is detected.

■Busy Flag

This serial interface contains 2 busy flags (SLVBSY, I2CBSY).

The SLVBSY flag is set to "1" when address transmitted from master matches with the slave address.

The I2CBSY flag is set to "1" during communication on IIC bus.

In 10 bits addresss mode, if the upper 2 bits address which is first to be transmitted from master matches with the I2CAD9-8 of the SC4AD1 register, the SLVBSY flag is set to "1" and SC4IRQ is not generated. If the lower 8 bits address which is next to be transmitted from master matches with the I2CAD7-0 of the SC4AD0 register, the SLVBSY flag is remained to "1" and SC4IRQ is generated. If these address mismatch, the SLVBSY flag is cleared to "0" and SC4IRQ is not generated.

■Bus Line Monitor

Bus line can be monitored during the general call communicaation.

For monitoring, while the SELI2C flag is set to "1", set the I2CGEM flag of the SC4AD1 register to "1" and set the direction control of the communication pin to input. Though serial 4 interrupt is generated at this time, it does not output signal to the data and clock, and thus, has no effect on the communicaiton.

■Pin Setup

Table 13-3-1 shows pin setup (SDA, SCL pins) for serial interface 4 data transmission.

N-ch open drain setup is always necessary for using this serial interface. Use the pull-up resistor control register (PnPLU) of each port for pull-up resistor setup. Input/output of the transfer data is automatically switched.

Table 13-3-1 Pin Setup

Item	Data I/O pin	Clock I/O pin
Port pin	SDA pin	SCL pin
	P01	P02
Function	P53	P54
Nch open-drain control register	SC4ODC0	
	SC4ODC1	
Pull-up resistor control register	P0PLU	
	P5PLU	

Note that this serial interface does not features the functions which resets the serial interface circuit on determination of reception data or change the slave address. Always use the software for determination of reception data incuding in the general call communication mode.

13-3-1 Setup Example of the Slave IIC Serial Interface

■Setup Example of the Data Transmission

This section describes the setup example of slave transmission using serial interface 4.

Table 13-3-2 shows the conditions for transmission routine.

Table 13-3-2 Pin Setup

Item	Setup
Data pin (SDA)	P01
Clock pin (SCL)	P02
Addressing mode	7 bits
Slave address	110011
Transmission data	x'55'

An example setup procedure, with a description of each step is shown below.

Setup Procedure	Description
(1) Control the pin type. SC4ODC0 (x'3F3F') bp1-0 : SC4ODC01-00 = 11 P0PLU (x'3F40') bp2-1 : P0PLU2-1 = 11	(1) Set the SC4ODC01-0 flag of the SC4ODC0 register to "1" to select N-ch open drain for P01 and P02. Set the P0PLU2-1 flag of the P0PLU register to "1" to add pull-up resistor.
(2) Control the pin direction. P0DIR (x'3F30') bp2-1 : P0PLU2-1 = 11	(2) Set the P0PLU2-1 flag of the port 0 pin direction control register (P0DIR) to "1" to set P01 and P02 to output mode.
(3) Communication pin, Communication mode, address mode selection SC4AD1 (x'3FA4') bp4 : I2CPSEL = 1 bp3 : I2CGEM = 0 bp2 : I2CADM = 0	(3) Set the I2CPSEL flag of the SC4AD1 register to "1" to select P01 and P02 for communication pins. Set the I2CGEM flag to "0" to select normal communication mode, and set the I2CADM flag to "0" to select 7 bits adddress mode.
(4) Serial interface 4 actication SC4AD1 (x'3FA4') : SELI2C = 1	(4) Set the SELI2C flag of the SC4AD1 register to "1" to activate the serial interface.

Setup Procedure	Description
(5) Set the slave address. SC4AD0 (x'3FA3') bp7-1 : I2CAD7-1 = 0110011	(5) Set the slave address to the upper 7 bits of the SC4AD0 register (I2CAD7-1).
(6) IIC communication start	(6) Master on the IIC bus starts communication.
(7) Data transmission/reception confirmation SC4STR (x'3FAC') bp7 : WRS = 0	(7) When the address transmitted from the master and the slave address set in the SC4AD1 register match, serial interface 4 interrupt (SC4IRQ) is generated. In the interrupt routine, make sure the communication is the slave transfer by verifying that the WRS flag of SC4STR register is "0".
(8) Transmission data setup SC4TXB (x'3FA5') bp7-0 : I2CTXB7-0 = x'55'	(8) Set the transmission data to the SC4TXB register.

The transfer rate at IIC communication should be set to under 10 dividing of the system clock.

When master node on the IIC bus issues restart condition at slave transmission, as dummy data, the upper bit should be "1" for transmission data buffer.

Chapter 14 Automatic Transfer Controller

14

14-1 Overview

14-1-1 ATC1

This LSI contains an automatic transfer controller (ATC) that uses direct memory access (DMA) to transfer the contents of the whole memory space (256 KB) using the hardware. This ATC block is called ATC1.

ATC1 is activated by an interrupt or a flag set by the software. Once this occurs, even if it is in the middle of executing an instruction, the microcontroller waits for a time when it can release the bus, stops normal operation, and transfers bus control to ATC1. ATC1 then uses the released bus for the hardware data transfer.

The software sets the activation factor in ATC1 control register 1 (AT1CNT1), then data transfer begins when the AT1ACT flag in ATC1 control register 0 (AT1CNT0) is set to "1". AT1ACT flag is automatically cleared to "0" when ATC1 is activated.

The transfer data counter (AT1TRC) determines the number of transfers that ATC1 makes, up to a maximum of 255 times. There are also 16 transfer modes, set in ATC1 control register 0 (AT1CNT0).

The interrupt enable flag (xxxIE) for interrupt as a trigger factor needs not to be set. This is because the automatic data transfer occurs in the hardware without going through an interrupt service routine. If the interrupt enable flag (xxxIE) is set for the type of interrupt ATC1, a regular interrupt is generated after the automatic transfer ends.

14-1-2 Functions

Table 14-1-1 and 14-1-2 provide a list of the ATC1 trigger factors and transfer modes.

■ATC1 Trigger Factors

Table 14-1-1 ATC1 Trigger Factors

Trigger Factors	External interrupt 0
	External interrupt 1
	External interrupt 2
	External interrupt 3
	Serial interface 4 interrupt
	Timer 1 interrupt
	Timer 7 interrupt
	Timer 7 capture trigger
	Serial interface 0 interrupt
	Serial interface1 interrupt
	Serial interface 3 interrupt
	A/D converter interrupt
	Software activation

■ATC Transfer Modes

Table 14-1-2 Transfer Modes

Transfer Mode	Transfer Direction (*)				Pointer Increment Control		Transfer Operation
	Cycle	Source Address		Destination Address	AT1MAP0	AT1MAP1	
Transfer mode 0		AT1MAP0		AT1MAP1 (I/O area)	-	-	1-byte data transfer
Transfer mode 1		AT1MAP1 (I/O area)		AT1MAP0	-	-	1-byte data transfer
Transfer mode 2		AT1MAP0		AT1MAP1 (I/O area)	AT1MAP0+1	-	1-byte data transfer
Transfer mode 3		AT1MAP1 (I/O area)		AT1MAP0	AT1MAP0+1	-	1-byte data transfer
Transfer mode 4	1st	AT1MAP0		AT1MAP1 (I/O area : even ADR)	AT1MAP0+1	-	1-word data transfer
	2nd	AT1MAP0 [=AT1MAP0+1]		AT1MAP1 (I/O area : odd ADR)	AT1MAP0+1	-	(An even address must be set in AT1MAP1)
Transfer mode 5	1st	AT1MAP1 (I/O area : even ADR)		AT1MAP0	AT1MAP0+1	-	1 word data transfer
	2nd	AT1MAP1 (I/O area : odd ADR)		AT1MAP0 [=AT1MAP0+1]	AT1MAP0+1	-	(An even address must be set in AT1MAP1)
Transfer mode 6	1st	AT1MAP1 (I/O area)		AT1MAP0	AT1MAP0+1	-	Two 1-byte data tranfers
	2nd	AT1MAP0 [=AT1MAP0+1]		AT1MAP1 (I/O area)	AT1MAP0+1	-	
Transfer mode 7	1st	AT1MAP1 (I/O area)		AT1MAP0	AT1MAP0+1	-	Two 1-byte data tranfers
	2nd	AT1MAP0 [=AT1MAP0+1]		AT1MAP1 (I/O area)	-	-	
Transfer mode 8	1st	AT1MAP1 (I/O area : even ADR)		AT1MAP0	AT1MAP0+1	-	Two 1-byte data tranfers
	2nd	AT1MAP0 [=AT1MAP0+1]		AT1MAP1 (I/O area : odd ADR)	AT1MAP0+1	-	(An even address must be set in AT1MAP1)
Transfer mode 9	1st	AT1MAP1 (I/O area : even ADR)		AT1MAP0	AT1MAP0+1	-	Two 1-byte data tranfers
	2nd	AT1MAP0 [=AT1MAP0+1]		AT1MAP1 (I/O area : odd ADR)	-	-	(An even address must be set in AT1MAP1)
Transfer mode A		AT1MAP0		AT1MAP1	-	-	1-byte data transfer (whole memory area)
Transfer mode B		AT1MAP1		AT1MAP0	-	-	1-byte data transfer (whole memory area)
Transfer mode C		AT1MAP0		AT1MAP1	AT1MAP0+1	AT1MAP1+1	1-word data transfer (whole memory area)
Transfer mode D		AT1MAP1		AT1MAP0	AT1MAP0+1	AT1MAP1+1	1-word data transfer (whole memory area)
Transfer mode E		AT1MAP0		AT1MAP1	AT1MAP0+1	AT1MAP1+1	Burst transfer (continues until AT1TCR=0)
Transfer mode F		AT1MAP1		AT1MAP0	AT1MAP0+1	AT1MAP1+1	Burst transfer (continues until AT1TCR=0)

(*) When a memory pointer points to the I/O space, only the lower 8 bits of the pointer are valid.

14-1-3 Block Diagram

■ATC1 Block Diagram

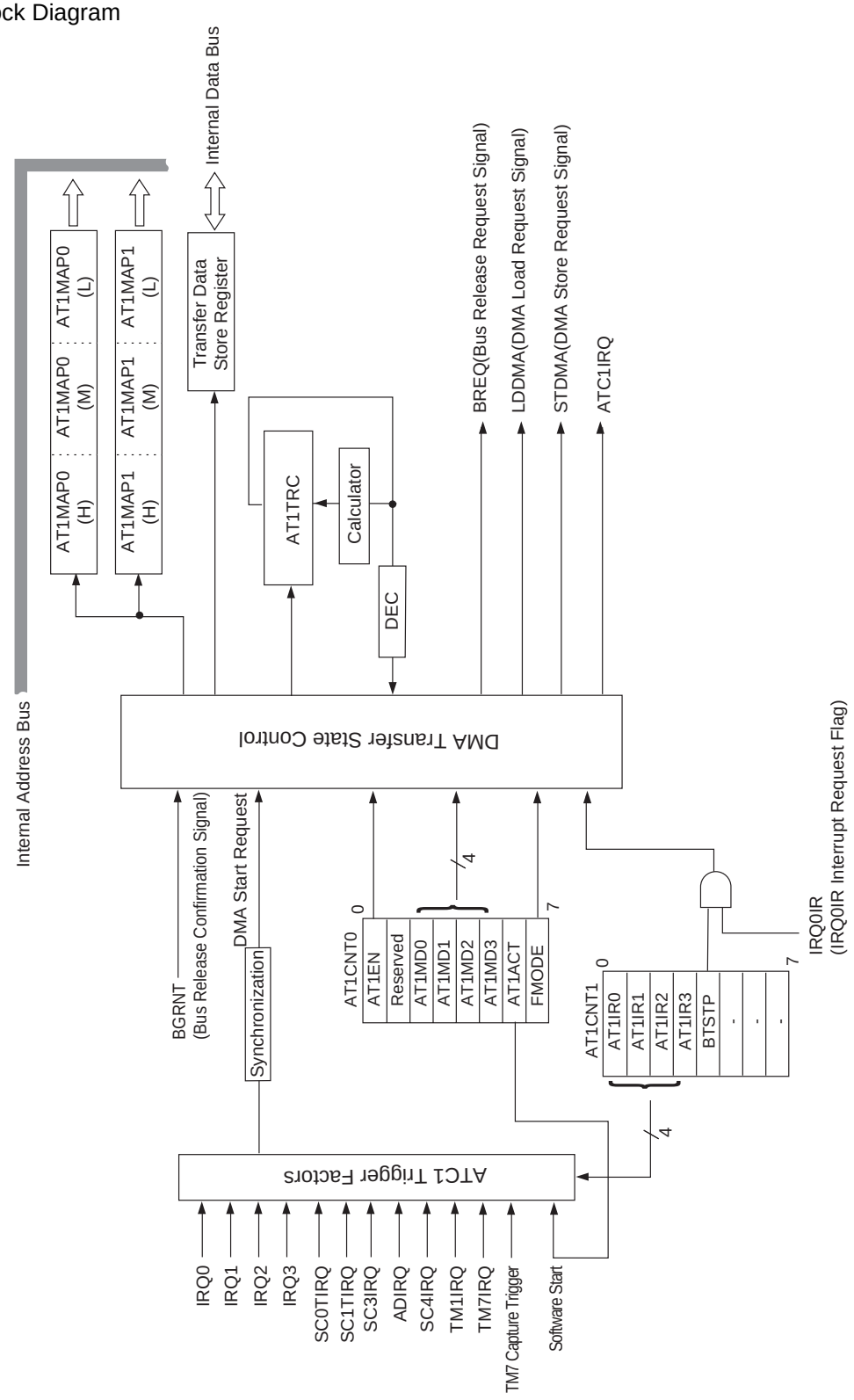


Figure 14-1-1 ATC1 Block Diagram

14-2 Control Registers

14-2-1 Registers

Table 14-2-1 shows the registers used to control ATC1.

Table 14-2-1 ATC1 Control Registers

	Register	Address	R/W	Function	Page
ATC1	AT1CNT0	x'03FD0'	R/W	ATC1 control register 0	XV - 6
	AT1CNT1	x'03FD1'	R/W	ATC1 control register 1	XV - 7
	AT1TRC	x'03FD2'	R/W	ATC1 transfer data counter	XV - 7
	AT1MAP0L	x'03FD3'	R/W	ATC1 memory pointer 0 (lower 8 bits)	XV - 8
	AT1MAP0M	x'03FD4'	R/W	ATC1 memory pointer 0 (middle 8 bits)	XV - 8
	AT1MAP0H	x'03FD5'	R/W	ATC1 memory pointer 0 (upper 2 bits)	XV - 8
	AT1MAP1L	x'03FD6'	R/W	ATC1 memory pointer 1 (lower 8 bits)	XV - 8
	AT1MAP1M	x'03FD7'	R/W	ATC1 memory pointer 1 (middle 8 bits)	XV - 8
	AT1MAP1H	x'03FD8'	R/W	ATC1 memory pointer 1 (upper 2 bits)	XV - 8

R/W : Readable / Writable

■ATC1 Control Register 0 (AT1CNT0)

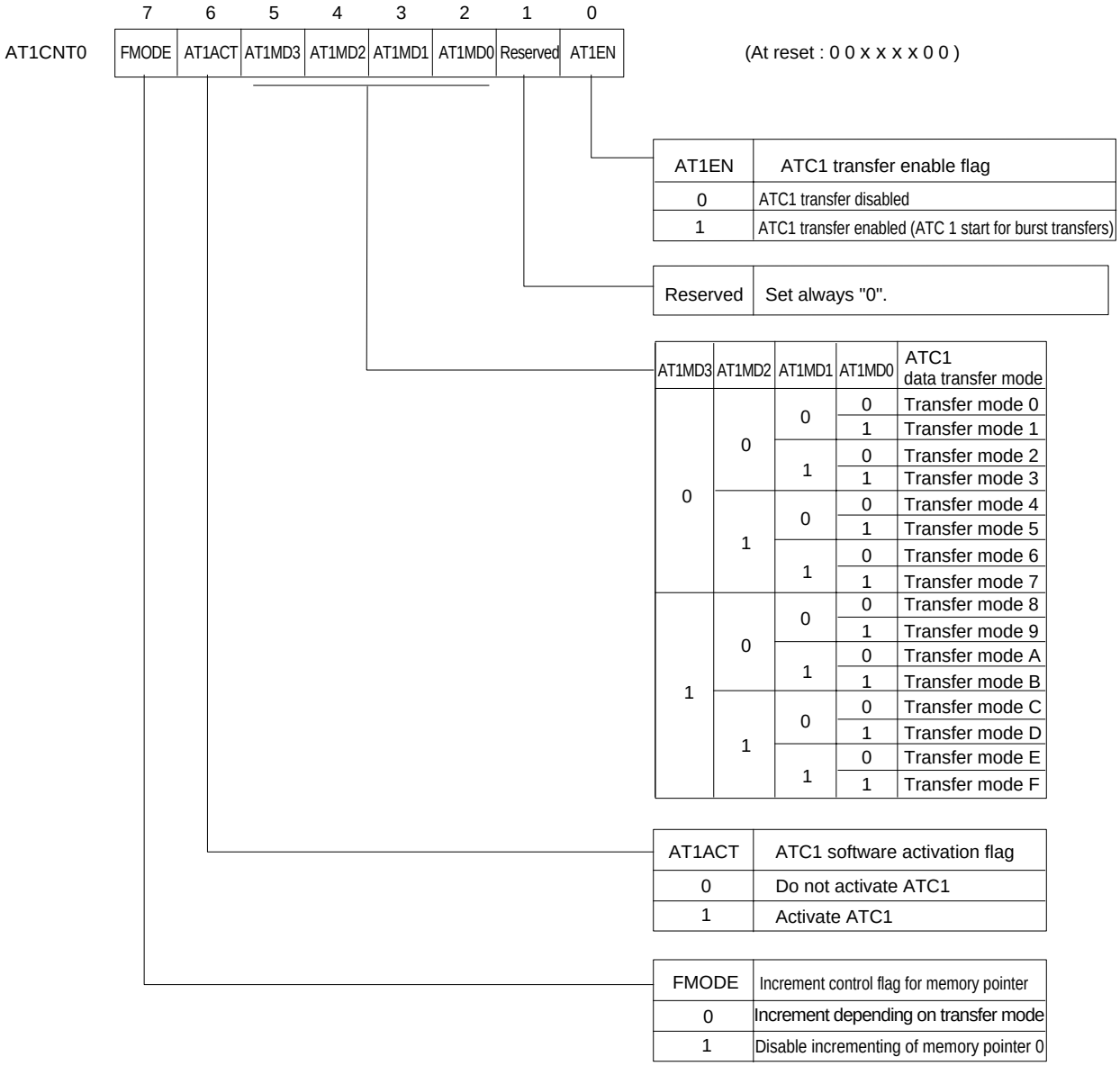


Figure 14-2-1 ATC1 Control Register 0 (AT1CNT0 : x'03FD0', R/W)

■ATC1 Control Register 1 (AT1CNT1)

	7	6	5	4	3	2	1	0
AT1CNT1	-	-	-	BTSTP	AT1IR3	AT1IR2	AT1IR1	AT1IR0

(At reset : - - - x x x x x)

AT1IR3	AT1IR2	AT1IR1	AT1IR0	ATC1 trigger factor settings
0	0	0	0	External interrupt 0
			1	External interrupt 1
		1	0	Serial interface 0 interrupt
			1	Serial interface 1 interrupt
	1	0	0	Timer 7 interrupt
			1	Timer 7 capture trigger
		1	0	A/D interrupt
			1	Software initialization
1	0	0	0	External interrupt 2
			1	External interrupt 3
		1	0	(Disable)
			1	Serial interface 3 interrupt
	1	0	0	Reserved
			1	Reserved
		1	0	Serial interface 4 interrupt
			1	Timer 1 interrupt

BTSTP	Burst transfer stop enable
0	Burst transfer stop disable
1	Burst transfer stop enable (Transfer stops when external interrupt 0 occurs.)

Figure 14-2-2 ATC1 Control Register 1 (AT1CNT1 : x'03FD1', R/W)

■ATC1 Transfer Counter (AT1TRC)

	7	6	5	4	3	2	1	0
AT1TRC	AT1TRC7	AT1TRC6	AT1TRC5	AT1TRC4	AT1TRC3	AT1TRC2	AT1TRC1	AT1TRC0

(At reset : x x x x x x x x)

AT1TRC7 to 0 ATC1 Transfer Data Count Setting

- For transfer modes 0 to D, set this register to the number of ATC activations. The register decrements by 1 after every ATC1 activation. When the count reaches x'00', an ATC1 interrupt occurs and the transfer ends.
- For transfer modes E and F, set this register to number of burst transfers. The register decrements by 1 every time one byte is transfered. When the count reaches x'00', an ATC1 interrupt occurs and the transfer ends.

Figure 14-2-3 ATC1 Transfer Data Counter (AT1TRC : x'03FD2', R/W)

■ATC1 Memory Pointer 0 (AT1MAP0)

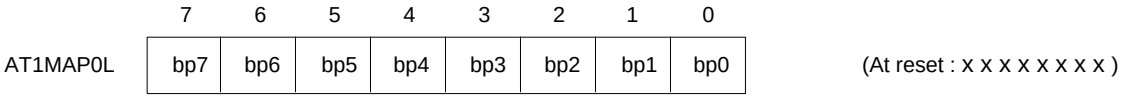


Figure 14-2-4 ATC1 Memory Pointer 0 : Lower 8 bits (AT1MAP0L : x'03FD3', R/W)

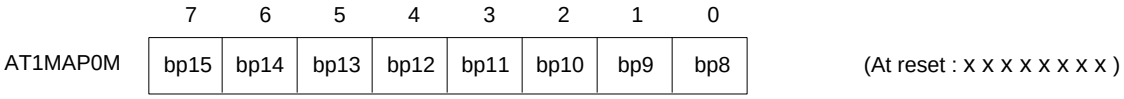


Figure 14-2-5 ATC1 Memory Pointer 0 : Middle 8 bits (AT1MAP0M : x'03FD4', R/W)

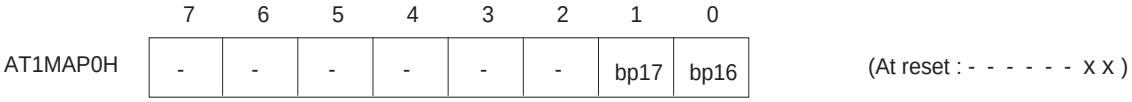


Figure 14-2-6 ATC1 Memory Pointer 0 : Upper 2 bits (AT1MAP0H : x'03FD5', R/W)

■ATC1 Memory Pointer 1 (AT1MAP1)

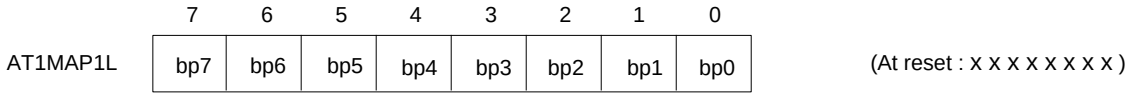


Figure 14-2-7 ATC1 Memory Pointer 1 : Lower 8 bits (AT1MAP1L : x'03FD6', R/W)

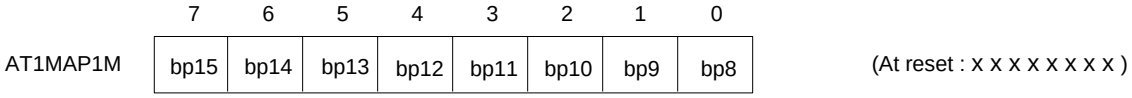


Figure 14-2-8 ATC1 Memory Pointer 1 : Middle 8 bits (AT1MAP1M : x'03FD7', R/W)

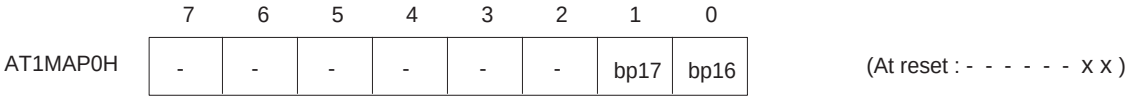


Figure 14-2-9 ATC1 Memory Pointer 1 : Upper 2 bits (AT1MAP1H : x'03FD8', R/W)

14-3 Operation

14-3-1 Basic Operations and Timing

ATC1 is a DMA block that enables the hardware to transfer the whole memory space (256 KB). This section provides a description of and timing for the basic ATC1 operations.

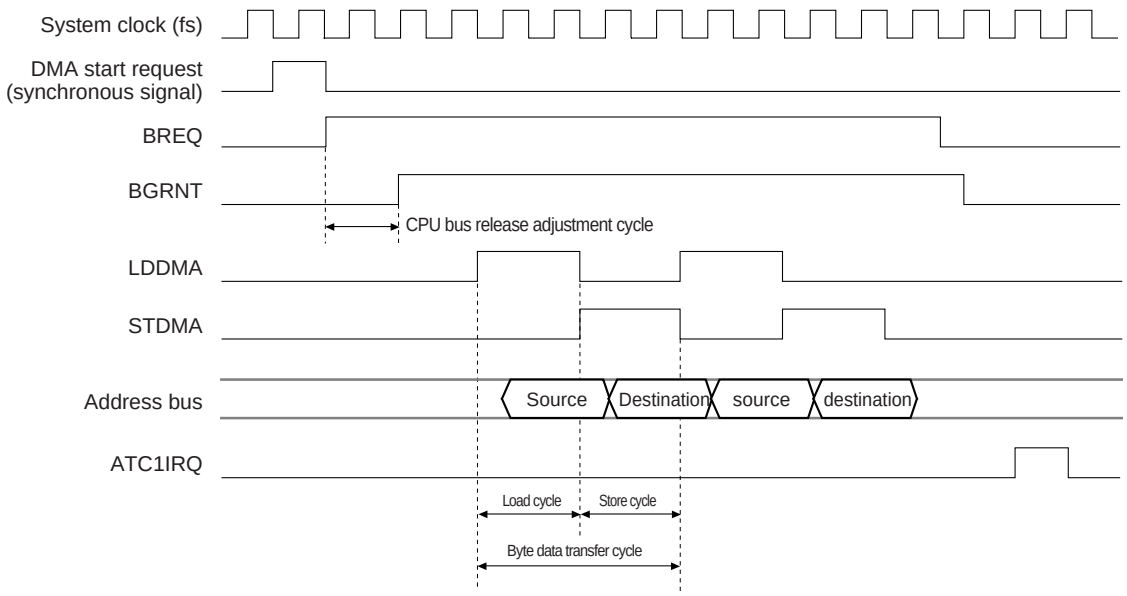


Figure 14-3-1 ATC1 Timing Chart

■ATC1 activation and internal bus acquisition

ATC1 activates either when the selected interrupt factor occurs or when the software sets the activation flag. Set the ATC1 trigger factor in ATC1 control register 1 (AT1CNT1).

When ATC1 starts, the ATC1 controller asserts the BREQ signal, which requests the MCU core to release the bus. When the core receives the BREQ signal, it stops all normal executions, even if it is in the middle of executing an instruction, and releases the bus at the next available timing. The core takes a maximum of four cycles from the time it receives the BREQ signal until it actually releases the bus. After it releases the internal bus, the core returns the bus granted signal, BGRNT, to ATC1. ATC1 can then begin using the bus to transfer data.

When an external interrupt is selected as an ATC1 trigger factor, specify the activation valid edge by the REDGn flag of the external interrupt control register, and the EDGSELn flag of the both edges interrupt control register (EDGDT).
[☞Chapter 3 3-3. External interrupts]

Set the valid edge for external interrupts before ATC1 activates.

■Data transfer

The basic ATC1 operation cycle is the "byte-data transfer cycle", in which ATC1 transfers a single byte of data. This operation consists of two instruction cycles, a load and a store cycle. In the load cycle, ATC1 reads the data from the source address of the source memory, and in the store cycle, ATC1 stores the read data to the destination address of the destination memory.
ATC1 transfers word-length data or a multi-byte stream of data by repeating the byte-data transfer cycle as many times as necessary.

■Transfer end

Once it has transferred all the data, ATC1 generates an interrupt (ATC1IRQ) and stop the automatic transfer. In this way, the ATC1 block bypasses the software and automatically transfers data in a continuous DMA operation.

In both the load and store cycles, the read and write access occurs to the memory exactly as it does in a normal instruction execution. This means that the access timing is different depending on the memory space. Also, the wait settings for I/O and external memory spaces apply. The following is the access timing for each memory space, assuming no-wait situation.

- Internal ROM/RAM space	2 cycles
- External memory space	2 cycles
- I/O space (special registers)	3 cycles + CPU correction cycle (=0.5 cycles)

The MCU core adds the CPU correction cycle (0.5 cycles) for the I/O space to correct the internal clock when it accesses a peripheral for block. It sometimes adds it and sometimes doesn't, depending on the internal state of the core.

In figure 14-3-1. ATC1 Timing Chart, the time, from the rising of DMA activation request signal to the starting of LOAD cycle depends on the state of CPU, but it takes max. 8 cycles.

14-3-2 Setting the Memory Address

■Setting the transfer addresses to the memory pointers

The address of the memory space for an automatically data transfer of ATC1 should be set in the both of memory pointer 0 (AT1MAP0) and memory pointer 1 (AT1MAP1). In each transfer mode, one of those pointer is the source address, and another is the destination address.

■Memory pointer 0 functions

Memory pointer 0 is comprised of three 8-bit registers, AT1MAP0H, AT1MAP0M, and AT1MAP0L. AT1MAP0H holds upper 2bits of the 18-bit address, AT1MAP0M contains the middle 8 bits, and AT1MAP0L contains lower 8 bits. The 18-bit address set in memory pointer 0 points to a specific address in the total memory space of 256 KB.

Memory pointer 0 also contains a computational function that enables it to increment the address based on the transfer state. You can disable this function for all transfer modes by setting the FMODE bit of ATC1 control register 0 to "1".

■Memory pointer 1 functions

Memory pointer 1 is comprised of three 8-bit registers, AT1MAP1H, AT1MAP1M, and AT1MAP1L. AT1MAP1H holds upper 2 bits of the 18-bit address, AT1MAP1M contains the middle 8 bits, and AT1MAP1L contains lower 8 bits. Depending on the transfer mode, either all 18 bits are valid, or only the least significant 8 bits (in AT1MAP1L) are valid. When only the 8 bits in AT1MAP1L are valid, the value x'03F' is assigned to the 10 bits in AT1MAP1H and AT1MAP1M, and the pointer points to the I/O space (special registers).

Memory pointer 1 also contains a computational function that enables it to increment the address based on the transfer state.

14-3-3 Setting the Data Transfer Count

■Transfer data counter (AT1TRC) function

You can preset the data transfer count is preset for ATC1. Set the value in the ATC1 transfer counter (AT1TRC). The counter decrements by one each time ATC1 transfers one byte of data.
The value in the transfer data counter is indeterminate upon reset. The program must initialize the counter before activating ATC1. Note that ATC1 cannot be activated if the transfer data counter is set to x'00'.

■Data transfer operations using the transfer data counter (AT1TRC)

There are two main types of ATC1 data transfers, standard and burst transfers. (See section 14-3-4 " Setting the Data Transfer Modes"). The transfer counter operates differently depending on the transfer type.

1. Standard transfers [transfer modes 0 to D]
In standard transfers, the transfer counter decrements every time ATC1 is activated. When the counter reaches x'00' after a data transfer, ATC1 generates an interrupt (ATC1IRQ). This means that for standard transfers, the program must set the counter to the number of times ATC1 needs to be activated.

2. Burst transfers [transfer modes E to F]
In burst transfers, ATC1 is activated once and continuously transfers multiple bytes of data. In this case, the program must set the counter to the number of data bytes contained in the burst transfer. When the burst transfer starts, the transfer counter decrements every time one byte of data is transferred. When the counter reaches x'00', ATC1 generates an interrupt (ATC1IRQ).
It is also possible to force ATC1 to shut down during a burst transfer using external interrupt 0.
(See 14-3-4 "Setting the Data Transfer Modes").

■The transfer data counter (AT1TRC)

The transfer data counter can be set to a maximum 255 transfers (for standard transfers) or 255 bytes (for burst transfers). Note that setting the counter to x'00' disables transfers.

14-3-4 Setting the Data Transfer Modes

■Data transfer modes

There are two types of ATC1 transfers, standard and burst, and sixteen transfer modes. Set the transfer mode in ATC1 control register 0 (AT1CNT0).

[☞ Table 14-1-2 Transfer Modes]

■Standard and burst transfers

The ATC1 transfer modes are divided into standard transfer modes and burst transfer modes. There are fourteen standard modes, 0 to D, and two burst modes, E and F.

In standard modes, the operation specified for that mode executes each time ATC1 is activated. When the transfer ends, the value set in the transfer counter (AT1TRC) decrements and bus control returns to the MCU core. This operation repeats until the transfer counter reaches x'00'. When this happens, ATC1 completes the final data transfer, then generates an interrupt (ATC1IRQ).

For instance, if the initial transfer counter value is x'05', and the ATC1 activation factor is set to a timer 0 interrupt, ATC1 is activated each time timer 0 overflows and the automatic transfer begins. After fifth data transfers (activated by fifth timer 0 overflow) is complete, the transfer counter value becomes x'00', an ATC1 interrupt occurs, and the operation ends. Timer 0 overflows occurring after this point do not activate ATC1. For standard transfers, the program must set the transfer counter to the number of ATC1 activations required.

In burst modes, once ATC1 is activated, it transfers in one operation the number of bytes set in the transfer counter (AT1TRC). After the burst transfer begins, the transfer counter decrements each time ATC1 transfers one byte of data. When the counter reaches x'00', ATC1 generates an interrupt (ATC1IRQ) and the burst transfer ends. For burst transfers, the program must set the transfer counter to the number of data bytes in the burst transfer.

An external interrupt 0 can also be used to shut down ATC1 during a burst transfer. To enable this function, set the burst transfer stop enable bit (BTSTP) in ATC1 control register 1 (AT1CNT1) to 1.

When BTSTP = 1, ATC1 data transfers stop when the external interrupt 0 interrupt request flag (IRQ0IR flag in the IRQ0ICR register) is set. In an emergency shutdown, the transfer counter and memory pointer save the values they contained prior to the shutdown. When the interrupt service routine ends, a new activation factor restarts ATC1, and the burst transfer begins transferring data from the point at which it stopped.

14-3-5 Transfer Mode 0

In transfer mode 0, ATC1 automatically transfers one byte of data from any memory space to the I/O space (special registers : x'03F00' - x'03FFF') every time an ATC1 activation request occurs.

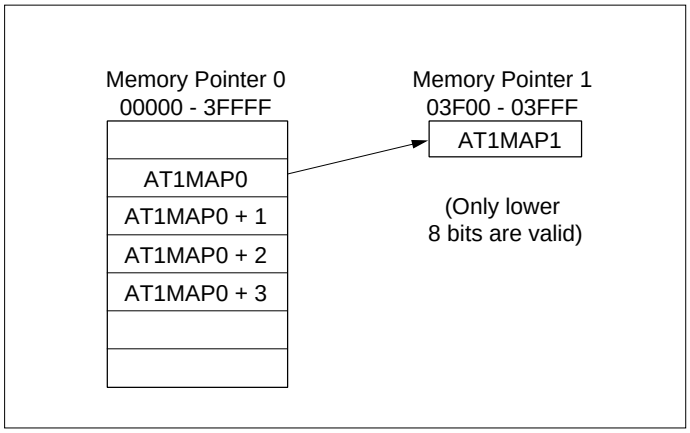


Figure 14-3-2 Transfer Mode 0

Set the source address in 18-bit memory pointer 0 (AT1MAP0H, M, L), and set the destination I/O address in lower 8 bits of memory pointer 1(AT1MAP1L). The upper 10 bits of the I/O space address (x'03F') need not to be set in AT1MAP1H and AT1MAP1M.

Transfer mode 0 does not have an incrementing function for the memory pointers. The data transfer executes for a fixed address.

Set the data transfer count for ATC1 in the transfer data counter (AT1TRC). The counter can be set to a maximum of 255 transfers. The counter decrements each time ATC1 is activated. When it reaches x'00', an interrupt (ATC1IRQ) occurs and the automatic transfer ends.

14-3-6 Transfer Mode 1

In transfer mode 1, ATC1 automatically transfers one byte of data from the I/O space (special registers : x'03F00' - x'03FFF') to any memory space every time an ATC1 activation request occurs.

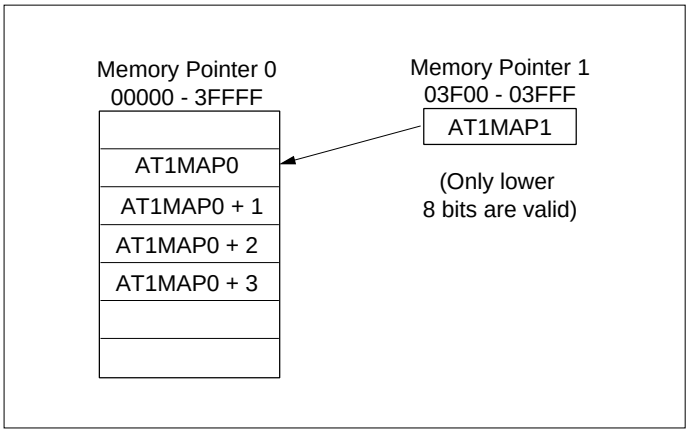


Figure 14-3-3 Transfer Mode 1

Set the source I/O address in lower 8 bits of memory pointer 1 (AT1MAP1L), and set the destination address in 18-bit memory pointer 0 (AT1MAP0H, M, L). The upper 10 bits of the I/O space address (x'03F') need not to be set in AT1MAP1H and AT1MAP1M.

Transfer mode 1 does not have an incrementing function for the memory pointers. The data transfer executes for a fixed address.

Set the data transfer count for ATC1 in the transfer data counter (AT1TRC). The counter can be set to a maximum of 255 transfers. The counter decrements each time ATC1 is activated. When it reaches x'00', an interrupt (ATC1IRQ) occurs and the automatic transfer ends.

14-3-7 Transfer Mode 2

In transfer mode 2, ATC1 automatically transfers one byte of data from any memory space to the I/O space (special registers : x'03F00' - x'03FFF') every time an ATC1 activation request occurs.

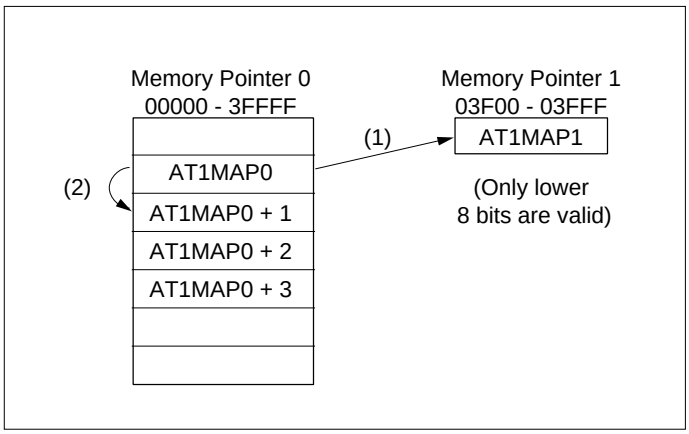


Figure 14-3-4 Transfer Mode 2

Set the source address in 18-bit memory pointer 0 (AT1MAP0H, M, L), and set the destination I/O address in lower 8 bits of memory pointer 1(AT1MAP1L). The upper 10 bits of the I/O space address (x'03F') need not to be set in AT1MAP1H and AT1MAP1M.

In transfer mode 2, the value in memory pointer 0 increments by 1 each time a byte-length data transfer ends. As a result, the source address for the next transfer is one address higher than that for the previous transfer.

Set the data transfer count for ATC1 in the transfer data counter (AT1TRC). The counter can be set to a maximum of 255 transfers. The counter decrements each time ATC1 is activated. When it reaches x'00', an interrupt (ATC1IRQ) occurs and the automatic transfer ends.

14-3-8 Transfer Mode 3

In transfer mode 3, ATC1 automatically transfers one byte of data from the I/O space (special registers : x'03F00' - x'03FFF') to any memory space every time an ATC1 activation request occurs.

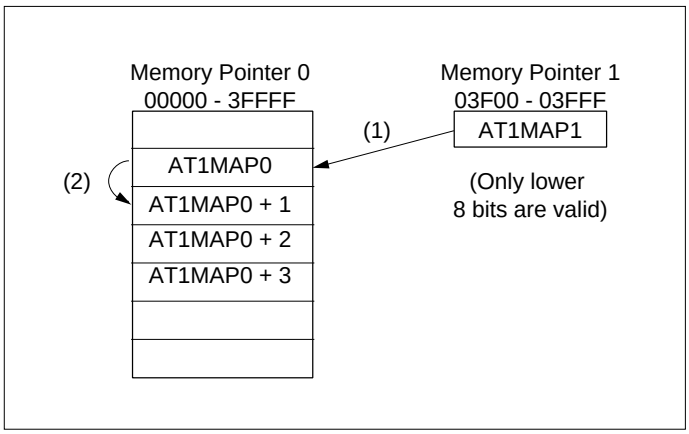


Figure 14-3-5 Transfer Mode 3

Set the source I/O address in lower 8 bits of memory pointer 1 (AT1MAP1L), and set the destination address in 18-bit memory pointer 0 (AT1MAP0H, M, L). The upper 10 bits of the I/O space address (x'03F') need not to be set in AT1MAP1H and AT1MAP1M.

In transfer mode 3, the value in memory pointer 0 increments by 1 each time a byte-length data transfer ends. As a result, the destination address for the next transfer is one address higher than that for the previous transfer.

Set the data transfer count for ATC1 in the transfer data counter (AT1TRC). The counter can be set to a maximum of 255 transfers. The counter decrements each time ATC1 is activated. When it reaches x'00', an interrupt (ATC1IRQ) occurs and the automatic transfer ends.

14-3-9 Transfer Mode 4

In transfer mode 4, ATC1 automatically transfers two bytes (one word) of data from any memory space to the I/O space (special registers : x'03F00' - x'03FFF') every time an ATC1 activation request occurs.

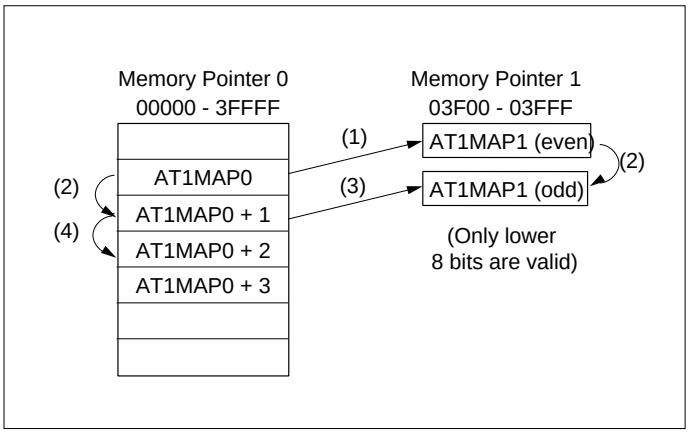


Figure 14-3-6 Transfer Mode 4

Set the source address in 18-bit memory pointer 0 (AT1MAP0H, M, L), and set the destination I/O address in the lower 8 bits of memory pointer 1(AT1MAP1L). The upper 10 bits of the I/O space address (x'03F') need not to be set in AT1MAP1H and AT1MAP1M.

Always set an even address as the destination I/O address in memory pointer 1. When ATC1 transfers one word to the I/O space, ATC1 can transfer the even address set in memory pointer 1 and the odd address that immediately follows it.

In transfer mode 4, ATC1 executes a data byte transfer twice, to send one data word, each time it is activated. The value in memory pointer 0 increments by one each time a byte-length data transfer ends. As a result, the source address for the next ATC1 operation is two addresses higher than that for the previous operation.

In this word-length transfer, ATC1 transfers the first data byte to an even address in the I/O space and the second data byte to an odd address in the I/O space.

Set the data transfer data count for ATC1 in the transfer data counter (AT1TRC). The counter can be set to a maximum of 255 transfers. The counter decrements each time ATC1 is activated (after each *word* transfer). When it reaches x'00', an interrupt (ATC1IRQ) occurs and the automatic transfer ends.

14-3-10 Transfer Mode 5

In transfer mode 5, ATC1 automatically transfers two bytes (one word) of data from the I/O space (special registers : x'03F00' - x'03FFF') to any memory space every time an ATC1 activation request occurs.

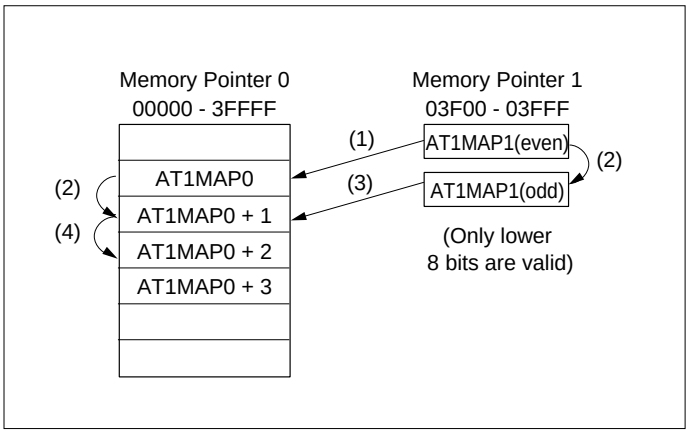


Figure 14-3-7 Transfer Mode 5

Set the source I/O address in lower 8 bits of memory pointer 1 (AT1MAP1L), and set the destination address in 18-bit memory pointer 0 (AT1MAP0H, M, L). The upper 10 bits of the I/O space address (x'03F') need not to be set in AT1MAP1H and AT1MAP1M.

Always set an even address as the source I/O address in memory pointer 1. When ATC1 transfers one word from the I/O space, ATC1 can transfer the even address set in memory pointer 1 and the odd address that immediately follows it.

In transfer mode 5, ATC1 executes a data byte transfer twice, to send one data word, each time it is activated. The value in memory pointer 0 increments by one each time a byte-length data transfer ends. As a result, the destination address for the next ATC1 operation is two addresses higher than that for the previous operation.

In this word-length transfer, ATC1 transfers the first data byte from an even address in the I/O space and the second data byte from an odd address in the I/O space.

Set the data transfer count for ATC1 in the transfer data counter (AT1TRC). The counter can be set to a maximum of 255 transfers. The counter decrements each time ATC1 is activated (after each *word* transfer). When it reaches x'00', an interrupt (ATC1IRQ) occurs and the automatic transfer ends.

14-3-11 Transfer Mode 6

In transfer mode 6, ATC1 automatically transfers one byte of data two times every time an ATC1 activation request occurs.

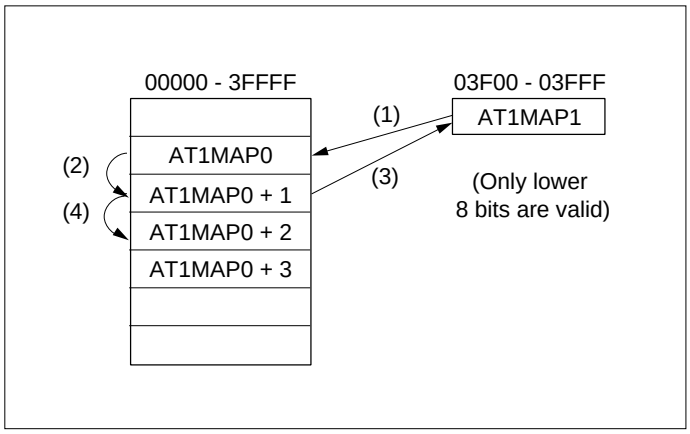


Figure 14-3-8 Transfer Mode 6

In this mode the transfer direction indicated by memory pointers 0 and 1 reverses for the second data byte transfer.

In the first data byte transfer, the I/O space address (x'03F00' - x'03FFF') in memory pointer 1 is the source address, and the address in memory pointer 0, for any memory space, is the destination address. When the first data byte transfer ends, the address in memory pointer 0 increments by one.

In the second data byte transfer, the incremented address in memory pointer 0 becomes the source address, and the I/O space address (x'03F00' - x'03FFF') in memory pointer 1 becomes the destination address. When the second data byte transfer ends, the address in memory pointer 0 increments again.

Set the I/O address in lower 8 bits of memory pointer 1 (AT1MAP1L). The upper 10 bits of the I/O space address (x'03F') need not to be set in AT1MAP1H, AT1MAP1M.

Transfer mode 6 can be used to support continuous transmission/reception for serial interface 3. Set memory pointer 1 to point to the serial transmission/reception shift register (SCnTRB) and select serial interrupts as an ATC1 trigger factor. In this way, each time a serial communication ends the MCU continuously reads the received data (first data byte transfer) then writes the transmission data (second data byte transfer) up to 255 times, entirely through the hardware.

To execute a continuous serial transaction, you must pre-store the serial transmission data in the memory space that memory pointer 0 points, the transmission data must fill every other address in the space. Once the serial transaction ends, the received data is stored empty (skipped) addresses and the transmission and reception data at stored in an alternating pattern.

In transfer mode 6, ATC1 executes a data byte transfer twice each time it is activated. The value in memory pointer 0 increments by one each time a byte-length data transfer ends. As a result, the source address for the next ATC1 operation is two addresses higher than that for the previous operation.

Set the data transfer count for ATC1 in the transfer data counter (AT1TRC). The counter can be set to a maximum of 255 transfers. The counter decrements each time ATC1 is activated (after one byte of data has been transferred twice). When it reaches x'00', an interrupt (ATC1IRQ) occurs and the automatic transfer ends.

14-3-12 Transfer Mode 7

In transfer mode 7, ATC1 automatically transfers one byte of data two times every time an ATC1 activation request occurs.

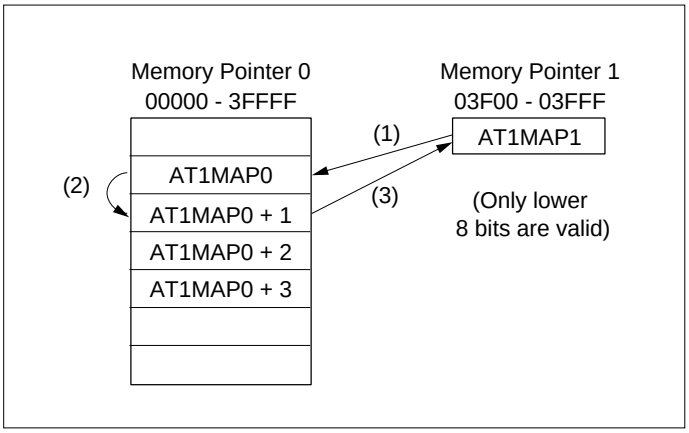


Figure 14-3-9 Transfer Mode 7

In this mode the transfer direction indicated by memory pointers 0 and 1 reverses for the second data byte transfer.

In the first data byte transfer, the I/O space address (x'03F00' - x'03FFF') in memory pointer 1 is the source address, and the address in memory pointer 0, for any memory space, is the destination address. When the first data byte transfer ends, the address in memory pointer 0 increments by one.

In the second data byte transfer, the incremented address in memory pointer 0 becomes the source address, and the I/O space address (x'03F00' - x'03FFF') in memory pointer 1 becomes the destination address. The address in memory pointer 0 remains unchanged after the second data byte transfer ends.

Set the I/O address in lower 8 bits of memory pointer 1 (AT1MAP1L). The upper 10 bits of the I/O space address (x'03F') need not to be set in AT1MAP1H, AT1MAP1M.

Transfer mode 7 can be used to support continuous transmission/reception for serial interface 3. Set memory pointer 1 to point to the serial transmission/reception shift register (SCnTRB) and select serial interrupts as an ATC1 trigger factor. In this way, each time a serial communication ends the MCU continuously reads the reception data (first data byte transfer) then writes the transmission data (second data byte transfer) up to 255 times, entirely through the hardware.

To execute a continuous serial transaction, you must pre-store the serial transmission data in the memory space that memory pointer 0 points, once the serial communication ends, the MCU has written to the reception data over the transmission data, so that only reception data remains in the memory.

In transfer mode 7, ATC1 executes a data byte transfer twice each time it is activated. However, the value in memory pointer 0 increments by one only after the first transfer ends. As a result, the source address for the next ATC1 operation is one address higher than that for the previous operation.

Set the data transfer count for ATC1 in the transfer data counter (AT1TRC). The counter can be set to a maximum of 255 transfers. The counter decrements each time ATC1 is activated (after one byte of data has been transferred twice). When it reaches x'00', an interrupt (ATC1IRQ) occurs and the automatic transfer ends.

14-3-13 Transfer Mode 8

In transfer mode 8, ATC1 automatically transfers one byte of data two times every time an ATC1 activation request occurs.

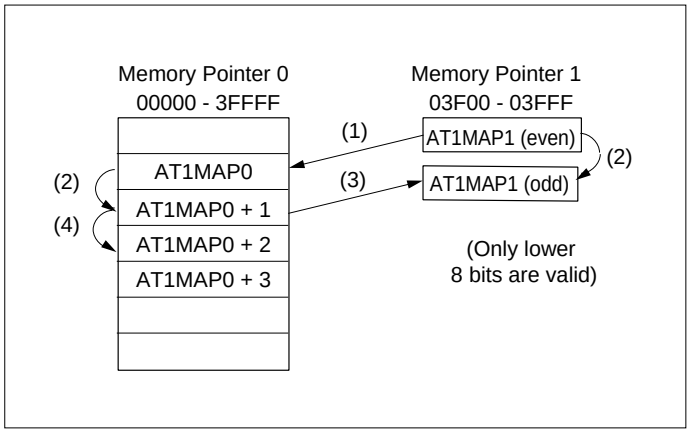


Figure 14-3-10 Transfer Mode 8

In this mode the transfer direction indicated by memory pointers 0 and 1 reverses for the second data byte transfer.

In the first data byte transfer, the I/O space address (x'03F00' - x'03FFF') in memory pointer 1 is the source address, and the address in memory pointer 0, for any memory space, is the destination address. When the first data byte transfer ends, the address in memory pointer 0 increments by one.

In the second data byte transfer, the incremented address in memory pointer 0 becomes the source address, and the I/O space address (x'03F00' - x'03FFF') in memory pointer 1 becomes the destination address. When the second data byte transfer ends, the address in memory pointer 0 increments again.

Set an even I/O address in the lower 8 bits of memory pointer 1 (AT1MAP1L). The upper 10 bits of the I/O space address (x'03F') need not to be set in AT1MAP1H, AT1MAP1M.

Always set an even I/O address in memory pointer 1. In this double transfer of a data byte from and to the I/O space, ATC1 targets the even I/O address set in memory pointer 1 and the odd address that immediately follows it. In this mode, the first data byte transfer accesses an even I/O address and the second data byte transfer accesses an odd I/O address.

Transfer mode 8 can be used to support continuous transmission/ reception for serial interface 0 and 1. Set the memory pointer 1 to point to the serial reception buffer (RXBUF0, RXBUF1) and select serial interrupts as the ATC1 trigger factor. In this way, each the serial communication ends, the MCU continuously reads the reception data (first data byte transfer), then writes the transmission data to the transmission buffer (TXBUF0, TXBUF1) (second data byte transfer) up to 255 times, entirely through the hardware.

Before execute a continuous serial transaction, store the serial transmission data in the memory space that memory pointer 0 points, the transmission data must fill every other address in the space. Once the serial transaction ends, the received data is stored empty (skipped) addresses and the transmission and reception data at stored in an alternating pattern.

In transfer mode 8, ATC1 executes a data byte transfer twice each time it is activated. The value in memory pointer 0 increments by one each time a byte-length data transfer ends. As a result, the source address for the next ATC1 operation is two addresses higher than that for the previous operation.

Set the data transfer count for ATC1 in the transfer data counter (AT1TRC). You can set the counter to a maximum of 255 transfers. The counter decrements each time ATC1 is activated (after one byte of data has been transferred twice). When it reaches x'00', an interrupt (ATC1IRQ) occurs and the automatic transfer ends.

14-3-14 Transfer Mode 9

In transfer mode 9, ATC1 automatically transfers one byte of data two times every time an ATC1 activation request occurs.

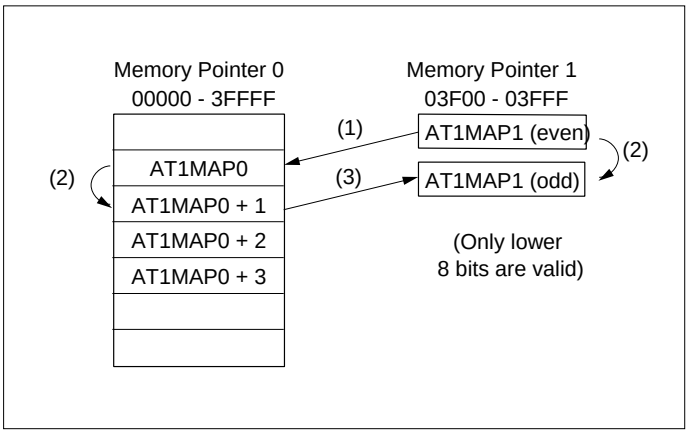


Figure 14-3-11 Transfer Mode 9

In this mode the transfer direction indicated by memory pointers 0 and 1 reverses for the second data byte transfer.

In the first data byte transfer, the I/O space address (x'03F00' - x'03FFF') in memory pointer 1 is the source address, and the address in memory pointer 0, for any memory space, is the destination address. When the first data byte transfer ends, the address in memory pointer 0 increments by one.

In the second data byte transfer, the incremented address in memory pointer 0 becomes the source address, and the I/O space address (x'03F00' - x'03FFF') in memory pointer 1 becomes the destination address. The address in memory pointer 0 remains unchanged after the second data byte transfer ends.

Set an even I/O address in lower 8 bits of memory pointer 1 (AT1MAP1L). The upper 10 bits of the I/O space address (x'03F') need not to be set in AT1MAP1H, AT1MAP1M.

Always set an even I/O address in memory pointer 1. In this double transfer of a data byte from and to the I/O space, ATC1 targets the even I/O address set in memory pointer 1 and the odd address that immediately follows it. In this mode, the first data byte transfer accesses an even I/O address and the second data byte transfer accesses an odd I/O address.

Transfer mode 9 can be used to support continuous transmission/ reception for serial interface 0 and 1. Set the memory pointer 1 to point to the serial reception buffer (RXBUF0, RXBUF1) and select serial interrupts as the ATC1 trigger factor. In this way, each the serial communication ends, the MCU continuously reads the reception data (first data byte transfer), then writes the transmission data to the transmission buffer (TXBUF0, TXBUF1) (second data byte transfer) up to 255 times, entirely through the hardware.

Before execute a continuous serial transaction, store the serial transmission data in the memory space that memory pointer 0 points, once the serial communication ends, the MCU has written to the reception data over the transmission data, so that only reception data remains in the memory.

In transfer mode 9, ATC1 executes a data byte transfer twice each time it is activated. However, the value in memory pointer 0 increments by one only after the first transfer ends. As a result, the source address for the next ATC1 operation is one address higher than that for the previous operation.

Set the data transfer count for ATC1 in the transfer data counter (AT1TRC). The counter can be set to a maximum of 255 transfers. The counter decrements each time ATC1 is activated (after one byte of data has been transferred twice). When it reaches x'00', an interrupt (ATC1IRQ) occurs and the automatic transfer ends.

14-3-15 Transfer mode A

In transfer mode A, ATC1 automatically transfers one byte of data from any memory space to any other memory space every time an ATC1 activation request occurs.

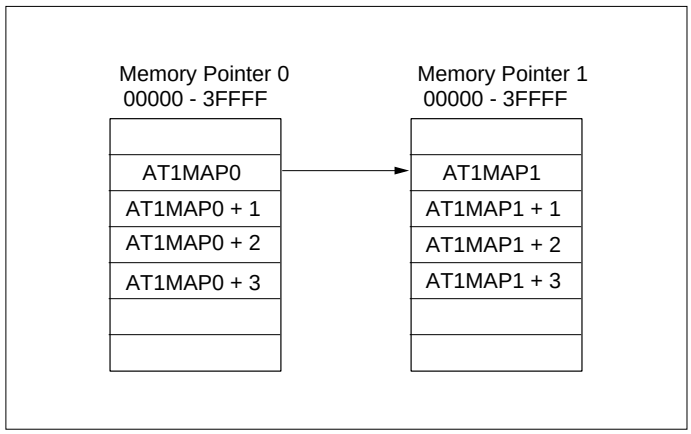


Figure 14-3-12 Transfer Mode A

Set the source address in 18-bit memory pointer 0 (AT1MAP0H, M, L), and set the destination address in 18-bit memory pointer 1 (AT1MAP0H, M, L).

Transfer mode A does not have an incrementing function for the memory pointers. The data transfer executes for a fixed address.

Set the data transfer count for ATC1 in the transfer data counter (AT1TRC). The counter can be set to a maximum of 255 transfers. The counter decrements each time ATC1 is activated. When it reaches x'00', an interrupt (ATC1IRQ) occurs and the automatic transfer ends.

14-3-16 Transfer Mode B

In transfer mode B, ATC1 automatically transfers one byte of data from any memory space to any other memory space every time an ATC1 activation request occurs.

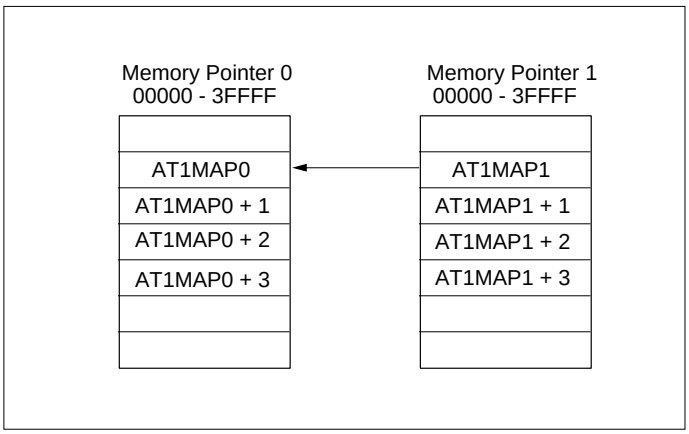


Figure 14-3-13 Transfer Mode B

Set the source address in 18-bit memory pointer 1 (AT1MAP1H, M, L), and set the destination address in 18-bit memory pointer 0 (AT1MAP0H, M, L).

Transfer mode B does not have an incrementing function for the memory pointers. The data transfer executes for a fixed address.

Set the data transfer count for ATC1 in the transfer data counter (AT1TRC). The counter can be set to a maximum of 255 transfers. The counter decrements each time ATC1 is activated. When it reaches x'00', an interrupt (ATC1IRQ) occurs and the automatic transfer ends.

14-3-17 Transfer Mode C

In transfer mode C, ATC1 automatically transfers one byte of data from any memory space to any other memory space every time an ATC1 activation request occurs.

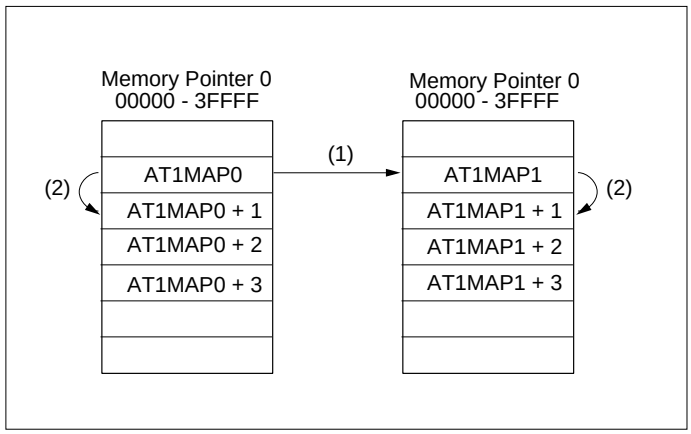


Figure 14-3-14 Transfer Mode C

Set the source address in 18-bit memory pointer 0 (AT1MAP0H, M, L), and set the destination address in 18-bit memory pointer 1 (AT1MAP1H, M, L).

In transfer mode C, the values in memory pointers 0 and 1 increment by 1 each time a byte-length data transfer ends. As a result, the source and destination addresses for the next transfer are one address higher than those for the original transfer.

Set the data transfer count for ATC1 in the transfer data counter (AT1TRC). The counter can be set to a maximum of 255 transfers. The counter decrements each time ATC1 is activated. When it reaches x'00', an interrupt (ATC1IRQ) occurs and the automatic transfer ends.

14-3-18 Transfer Mode D

In transfer mode D, ATC1 automatically transfers one byte of data from any memory space to any other memory space every time an ATC1 activation request occurs.

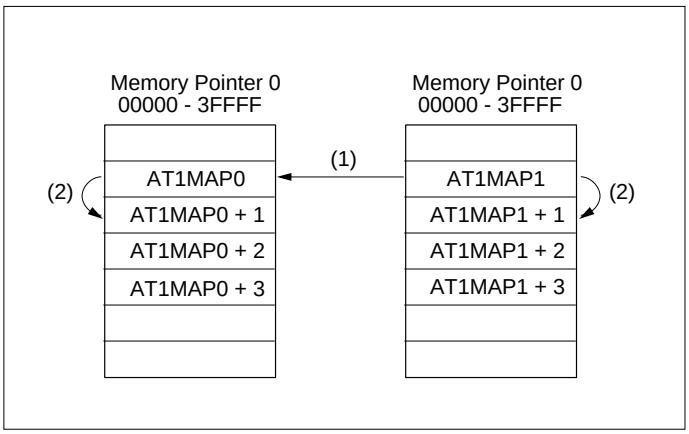


Figure 14-3-15 Transfer Mode D

Set the source address in 18-bit memory pointer 1 (AT1MAP1H, M, L), and set the destination address in 18-bit memory pointer 0 (AT1MAP0H, M, L).

In transfer mode D, the values in memory pointers 0 and 1 increment by 1 each time a byte-length data transfer ends. As a result, the source and destination addresses for the next transfer are one address higher than those for the original transfer.

Set the data transfer count for ATC1 in the transfer data counter (AT1TRC). The counter can be set to a maximum of 255 transfers. The counter decrements each time ATC1 is activated. When it reaches x'00', an interrupt (ATC1IRQ) occurs and the automatic transfer ends.

14-3-19 Transfer Mode E

Transfer mode E is a burst mode. In this mode, when ATC1 is activated, it automatically transfers the number of data bytes set in the transfer data counter (AT1TRC) in one continuous operation.

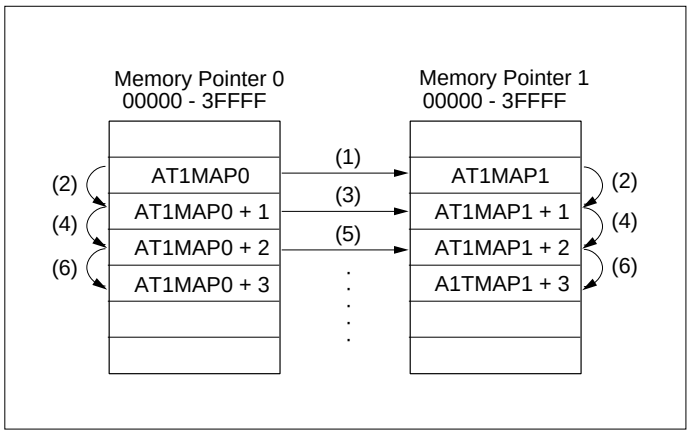


Figure 14-3-16 Transfer Mode E

Set the source address in 18-bit memory pointer 0 (AT1MAP0H, M, L), and set the destination address in 18-bit memory pointer 1 (AT1MAP1H, M, L). Once ATC1 is activated, memory pointers 0 and 1 increment by one each a byte-length data transfer ends.

For burst transfers, set the number of data bytes to be transferred in the transfer data counter (AT1TRC). The counter can be set to a maximum of 255 bytes. Once the burst transfer starts, the counter decrements each time ATC1 transfers one byte of data. When it reaches x'00', an interrupt (ATC1IRQ) occurs and the burst transfer ends.

It is possible to shut down ATC1 during burst transfers using external interrupt 0. You can enable or disable ATC1 shutdown with the burst transfer stop enable flag (BSTP) of ATC1 control register 1 (AT1CNT1). When BTSTP=1 and the interrupt request flag for external interrupt 0 (the IRQ0IR flag in the IRQ0ICR register) is set, the ATC1 data transfer shuts down immediately. During this shutdown, the transfer counter and the memory pointers save the values they contained prior to the shutdown. When the interrupt service routine ends and a new ATC1 trigger factor occurs, the burst transfer restarts from the point at which it stopped.

14-3-20 Transfer Mode F

Transfer mode F is a burst mode. In this mode, when ATC1 is activated, it automatically transfers the number of data bytes set in the transfer data counter (AT1TRC) in one continuous operation.

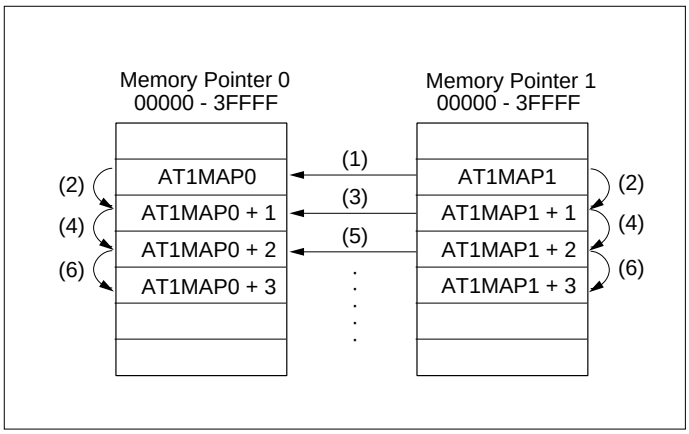


Figure 14-3-17 Transfer Mode F

Set the source address in 18-bit memory pointer 1 (AT1MAP1H, M, L), and set the destination address in 18-bit memory pointer 0 (AT1MAP0H, M, L). Once ATC1 is activated, memory pointers 0 and 1 increment by one each a byte-length data transfer ends.

For burst transfers, set the number of data bytes to be transferred in the transfer data counter (AT1TRC). The counter can be set to a maximum of 255 bytes. Once the burst transfer starts, the counter decrements each time ATC1 transfers one byte of data. When it reaches x'00', an interrupt (ATC1IRQ) occurs and the burst transfer ends.

It is possible to shut down ATC1 during burst transfers using external interrupt 0. You can enable or disable ATC1 shutdown with the burst transfer stop enable flag (BSTP) of ATC1 control register 1 (AT1CNT1). When BTSTP=1 and the interrupt request flag for external interrupt 0 (the IRQ0IR flag in the IRQ0ICR register) is set, the ATC1 data transfer shuts down immediately. During this shutdown, the transfer counter and the memory pointers save the values they contained prior to the shutdown. When the interrupt service routine ends and a new ATC1 trigger factor occurs, the burst transfer restarts from the point at which it stopped.

14-4 Setup Example

An example setup procedure, with a description of each step is as follows ;

Setup Procedure	Description
(1) Set the data transfer mode. AT1CNT0 (x'3FD0') bp7 :FMODE bp6 :AT1ACT = 0 bp5-2 :AT1MD3-0 bp0 :AT1EN = 0	(1) Select the data transfer mode with the AT1MD flag in the AT1CNT0 register. No matter which mode you select, setting the FMODE flag disables the incrementing function in memory pointer 0. Normally set this flag to 0. Note that you must set the ATC1 enable flag, AT1EN, to 0 at this step. Only enable ATC1 after setting all the other registers.
(2) Set memory pointer 0. AT1MAP0L (x'3FD3') AT1MAP0M (x'3FD4') AT1MAP0H (x'3FD5')	(2) Depending on the transfer mode you selected, set the source or destination address in the AT1MAP0 registers.
(3) Set memory pointer 1. AT1MAP1L (x'3FD6') AT1MAP1M (x'3FD7') AT1MAP1H (x'3FD8')	(3) Depending on the transfer mode you selected, set the source or destination address in the AT1MAP1 registers.
(4) Set the transfer data counter. AT1TRC (x'3FD2')	(4) Set the ATC1 data transfer count in the AT1TRC register.
(5) Select the ATC1 activation factor. AT1CNT1 (x'3FD1') bp4 :BTSTP bp3-0 :AT1IR3-0	(5) Select the ATC1 activation factor with the AT1IR flag in the AT1CNT1 register. If you select a burst-type transfer mode, then you must also enable or disable ATC1 shutdown at this step, by setting the BTSTP.
(6) Enable ATC operation. AT1CNT0 (x'3FD0') bp0 :AT1EN = 1	(6) Enable ATC1 data transfers with the AT1EN flag in the AT1CNT0 register.

To activate ATC1 in the software, first complete steps (1) to (6), then set the AT1ACT flag in the AT1CNT0 register. After the AT1ACT flag is set, ATC1 is started and data transfer is started. The hardware automatically clears AT1ACT flag when ATC1 is activated. On the standard transfer mode, set a program that sets flags as much as the data transfer needs.

Chapter 15 A/D Converter

15

15-1 Overview

This LSI has an A/D converter with 10 bits resolution. That has a built-in sample hold circuit, and software can switch channel 0 to 6 (AN0 to AN6) to analog input. As A/D converter is stopped, the power consumption can be reduced by a built-in ladder resistance. A/D converter is activated by 2 factors : a register setup or an external interrupt.

15-1-1 Functions

Table 15-1-1 shows the A/D converter functions.

Table 15-1-1 A/D Converter Functions

A/D Input Pins	7 pins
Pins	AN6 to AN0
Interrupt	ADIRQ
Resolution	10 bits
Conversion Time (Min.)	9.6 μs (T_{AD}=as 800 ns)
Input range	V_{REF-} to V_{REF+}
Power Consumption	Built-in Ladder Resistance (ON/OFF)

15-1-2 Block Diagram

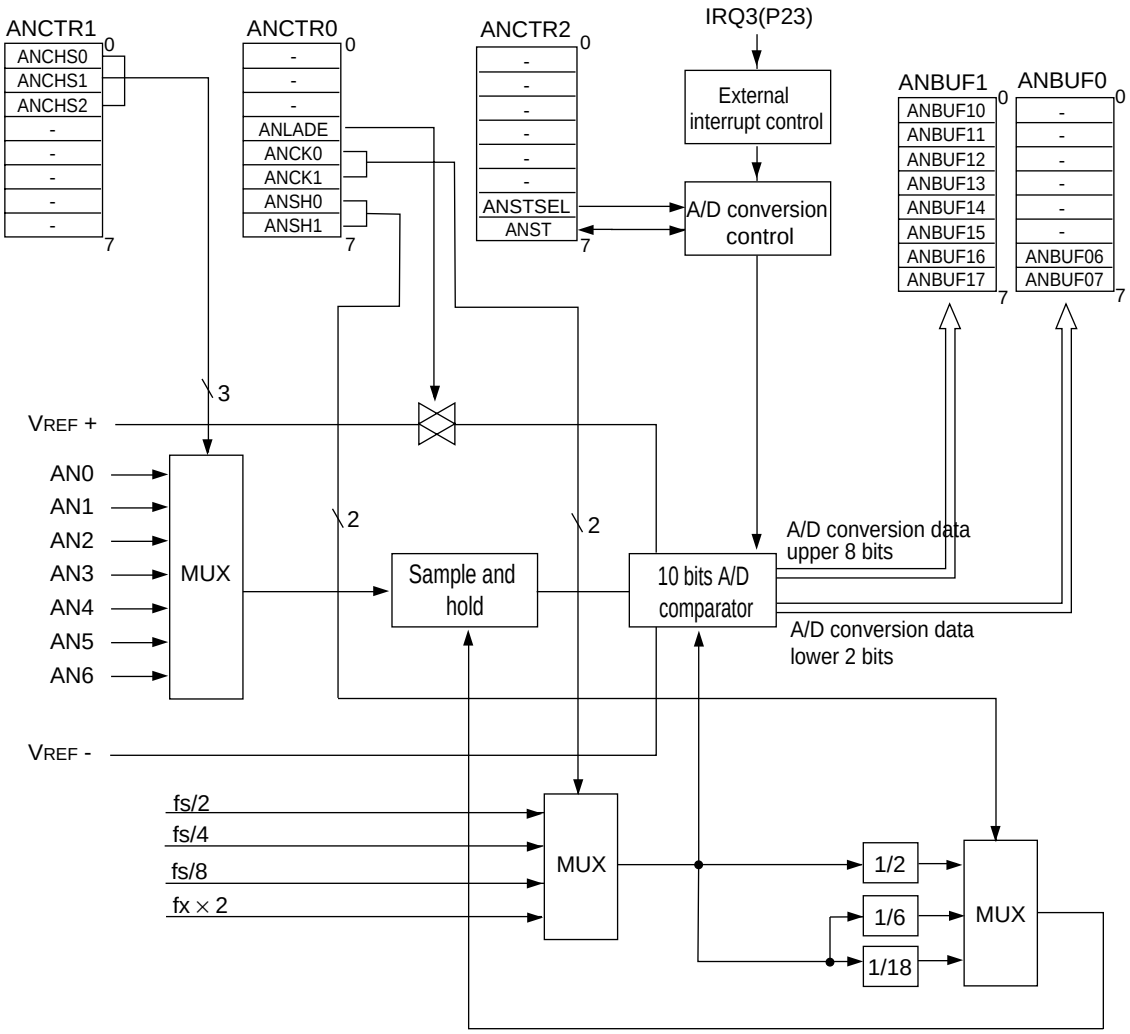


Figure 15-1-1 A/D Converter Block Diagram

15-2 Control Registers

A/D converter consists of the control register (ANCTRn) and the data storage buffer (ANBUFn).

15-2-1 Registers

Table 15-2-1 shows the registers used to control A/D converter.

Table 15-2-1 A/D Converter Control Registers

Register	Address	R/W	Function	Page
ANCTR0	x'03FB0'	R/W	A/D converter control register 0	XV - 5
ANCTR1	x'03FB1'	R/W	A/D converter control register 1	XV - 6
ANCTR2	x'03FB2'	R/W	A/D converter control register 2	XV - 6
ANBUF0	x'03FB3'	R	A/D converter data storage buffer 0	XV - 7
ANBUF1	x'03FB4'	R	A/D converter data storage buffer 1	XV - 7
ADICR	x'03FFA'	R/W	A/D +converter interrupt control register	III - 36
IRQ3ICR	x'03FE5'	R/W	External interrupt 3 control register	III - 20
EDGDT	x'03F8F'	R/W	Both edges interrupt control register	III - 45
PAIMD	x'03F3A'	R/W	Port A input mode register	IV - 43
PAPLUD	x'03F4A'	R/W	Port A pull-up/pull-down resistance control register	IV - 42
PADIR	x'03F3A'	R/W	Port A direction control register	IV - 42

R/W : Readable/Writable
R : Readable only

15-2-2 Control Registers

■A/D Converter Control Register 0 (ANCTR0)

	7	6	5	4	3	2	1	0
ANCTR0	ANSH1	ANSH0	ANCK1	ANCK0	ANLADE	-	-	-

(At reset : 0 0 0 0 - - -)

ANLADE	A/D ladder resistance control
0	A/D ladder resistance OFF
1	A/D ladder resistance ON

ANCK1	ANCK0	A/D conversion clock (ftad=1/TAD)
0	0	fs/2
	1	fs/4
1	0	fs/8
	1	fx × 2

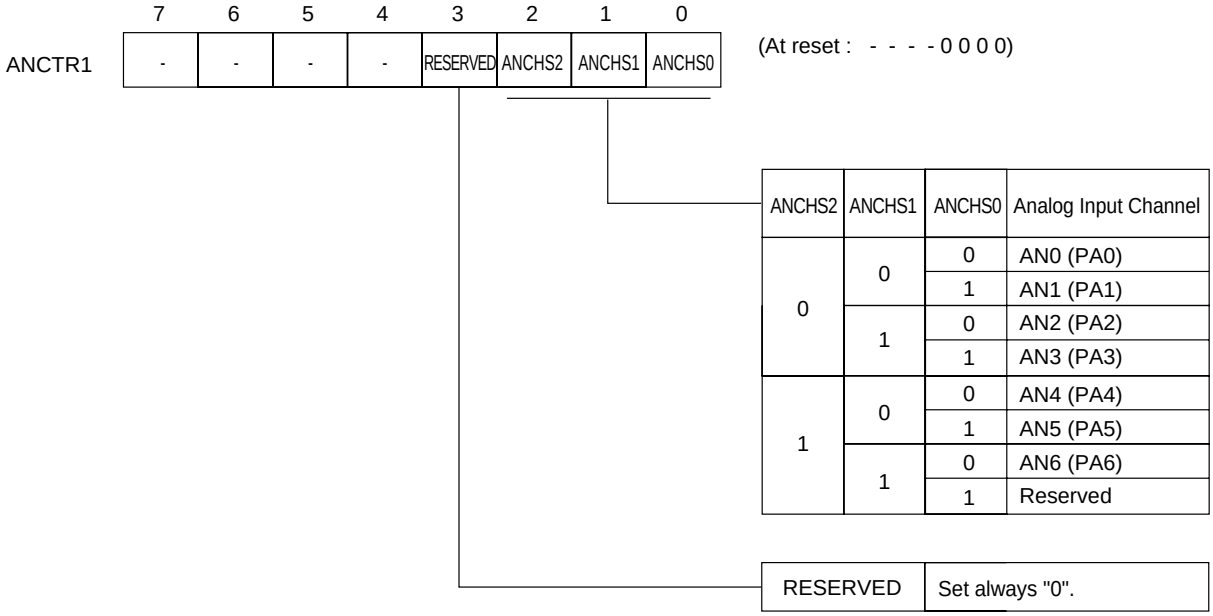
∗as 800 ns < TAD ≤ 15.26 µs

ANSH1	ANSH0	Sample and hold time
0	0	TAD × 2
	1	TAD × 6
1	0	TAD × 18
	1	Reserved

∗ Sampling and holding time is decided by the input impedance at analog input.
TAD means the cycle for A/D conversion clock.

Figure 15-2-1 A/D Converter Control Register 0 (ANCTR0 : x'03FB0', R/W)

■A/D Converter Control Register 1 (ANCTR1)

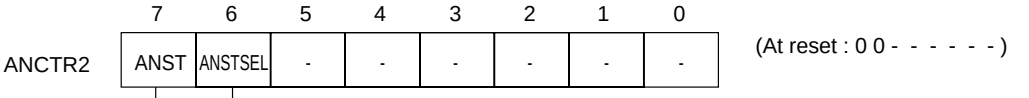


ANCHS2	ANCHS1	ANCHS0	Analog Input Channel
0	0	0	AN0 (PA0)
		1	AN1 (PA1)
	1	0	AN2 (PA2)
		1	AN3 (PA3)
1	0	0	AN4 (PA4)
		1	AN5 (PA5)
	1	0	AN6 (PA6)
		1	Reserved

RESERVED	Set always "0".

Figure 15-2-2 A/D Converter Control Register 1 (ANCTR1 : x'03FB1', R/W)

■A/D Converter Control Register 2 (ANCTR2)



ANSTSEL	A/D conversion activation factor selection
0	Set the ANST flag to "1".
1	Set the ANST flag, or the external interrupt 3 to "1".

ANST	A/D conversion status
0	A/D conversion is completed, stopped
1	A/D conversion is started, in progress

Figure 15-2-3 A/D Converter Control Register 2 (ANCTR2 : x'03FB2', R/W)

15-2-3 Data Buffers

■A/D Conversion Data Storage Buffer 0 (ANBUF0)

The lower 2 bits from the result of A/D conversion are stored to this register.

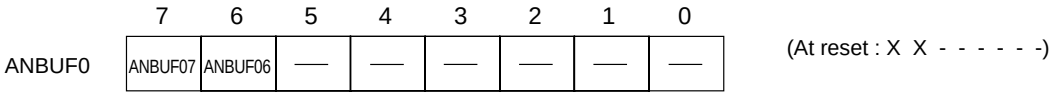


Figure 15-2-4 A/D Conversion Data Buffer 0 (ANBUF0 : x'03FB3', R)

■A/D Conversion Data Storage Buffer 1 (ANBUF1)

The upper 8 bits from the result of A/D conversion are stored to this register.

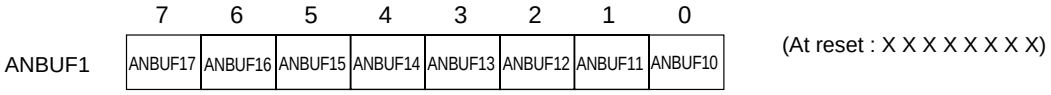


Figure 15-2-5 A/D Conversion Data Buffer 1 (ANBUF1 : x'03FB4', R)

15-3 Operation

Here is a description of A/D converter circuit setup procedure.

(1) Set the analog pins.
Set the analog input pin, set in (2), to "special function pin" by the port A input mode register (PAIMD).
* Setup for the port A input mode register should be done before analog voltage is put to pins.

(2) Select the analog input pin.
Select the analog input pin from AN6 to AN0 (PA6 to PA0) by the ANCHS2 to ANCHS0 flag of the A/D converter control register 1 (ANCTR1).

(3) Select the A/D converter clock.
Select the A/D converter clock by the ANCK1, ANCK0 flag of the A/D converter control register 0 (ANCTR0).
Setup should be such a way that converter clock (TAD) does not drop under 800 ns with any oscillator.

(4) Set the sample hold time.
Set the sample hold time by the ANSH1, ANSH0 flag of the A/D converter control register 0 (ANCTR0). The sample hold time should be based on analog input impedance.

(5) Set the A/D ladder resistance.
Set the ANLADE flag of the A/D converter control register 0 (ANCTR0) to "1", and a current flow through the ladder resistance and A/D converter goes into the waiting.
* (2) to (5) are not in order. (3), (4) and (5) can be operated simultaneously.

(6) Select the A/D converter activation factor, then start A/D conversion.
Set the ANST flag of the A/D converter control register 2 (ANCTR2) to "1" to start A/D converter, or set the ANSTSEL flag of the A/D converter control register 2 (ANCTR2) to "1" to start A/D conversion by the external interrupt IRQ3.
* Specify the valid edge by the EDGSEL3 flag of the both edges interrupt control register (EDGDT) and the REDG3 flag of the external interrupt 3 control register (IRQ3ICR).

(7) A/D conversion
Each bit of the A/D buffer 0,1 is generated after sampling with the sample and hold time set in (3). Each bit is generated in sequence from MSB to LSB.

(8) Complete the A/D conversion.
When A/D conversion is finished, the ANST flag is cleared to "0", and the result of the conversion is stored to the A/D buffer (ANBUF0, 1). At the same time, the A/D complete interrupt request (ADIRQ) is generated.

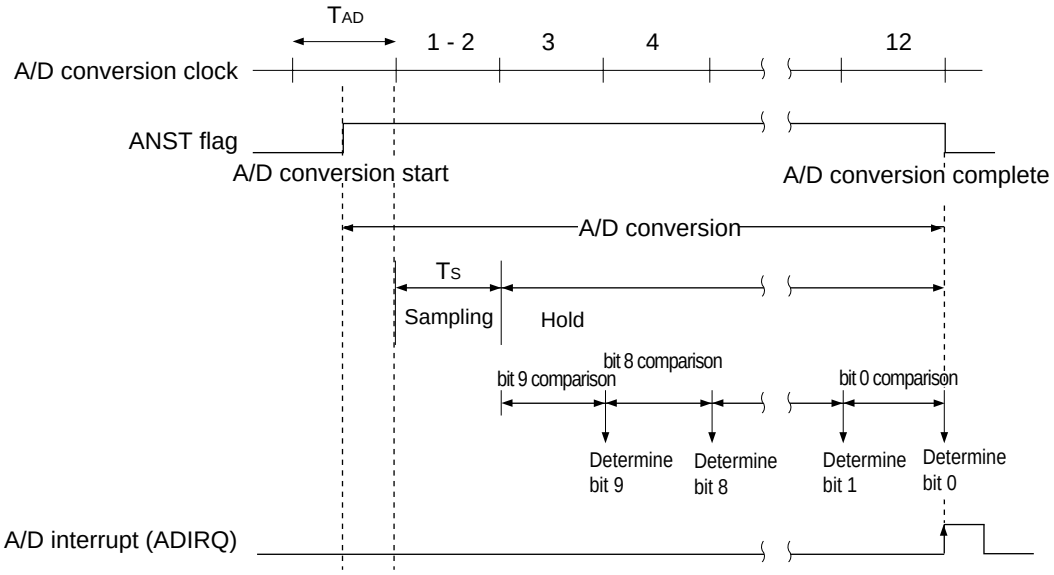


Figure 15-3-1 Operation of A/D Conversion

To read the value of the A/D conversion, A/D conversion should be done several times to prevent noise error by confirming the match of level by program, or by using the average value.

15-3-1 Setup

■Input Pins of A/D Converter Setup

Input pins for A/D converter is selected by the ANCH2 to 0 flag of the ANCTR1 register.

Table 15-3-1 Input Pins of A/D Converter Setup

ANCHS2	ANCHS1	ANCHS0	A/D pin
0	0	0	AN0 pin
		1	AN1 pin
	1	0	AN2 pin
		1	AN3 pin
1	0	0	AN4 pin
		1	AN5 pin
	1	0	AN6 pin
		1	Reserved

■Clock of A/D Converter Setup

The A/D converter clock is set by the ANCK1 to 0 flag of the ANCTR0 register. Set the A/D converter clock (T_{AD}) more than 800 ns and less than 15.26 µs. Table 15-3-2 shows the machine clock (fosc, fx, fs) and the A/D converter clock (T_{AD}). (calculated as fs = fosc/2, fx/4)

Table 15-3-2 A/D Conversion Clock and A/D Conversion Cycle

ANCK1	ANCK0	A/D conversion clock	A/D conversion cycle (TAD)		
			at oscillation for high speed		at oscillation for low speed
			at fosc=20 MHz	at fosc=8.38 MHz	at fx=32.768 kHz
0	0	fs/2	200.00 ns (no usable)	477.33 ns (no usable)	244.14 µs (no usable)
	1	fs/4	400.00 ns (no usable)	954.65 ns	488.28 µs (no usable)
1	0	fs/8	800.00 ns	1.91 µs	976.56 µs (no usable)
	1	fx x 2	15.26 µs	15.26 µs	15.26 µs

For the system clock (fs), refer to Chapter 2. 2-5 Clock Switching.

■Sampling Time (Ts) of A/D Converter Setup

The sampling time of A/D converter is set by the ANSH1 to 0 flag of the ANCTR0 register. The sampling time of A/D converter depends on external circuit, so set the right value by analog input impedance.

Table 15-3-3 Sampling Time of A/D Conversion and A/D Conversion Time

ANSH1	ANSH0	Sampling time (Ts)	A/D conversion time			
			at T_{AD}=800 ns	at T_{AD}=954.65 ns	at T_{AD}=1.91 µs	at T_{AD}=15.26 µs
0	0	T_{AD} x 2	9.60 µs	11.46 µs	22.92 µs	183.12 µs
	1	T_{AD} x 6	12.80 µs	15.27 µs	30.56 µs	244.16 µs
1	0	T_{AD} x 18	22.40 µs	26.73 µs	53.48 µs	427.28 µs
	1	Reserved	-	-	-	-

■Built-in Ladder Resistor Control

The ANLADE flag of the ANCTR0 register is set to "1" to send a current to the ladder resistance for A/D conversion. As A/D converter is stopped, the ANLADE flag of the ANCTR0 register is set to "0" to save the power consumption.

Table 15-3-4 A/D Ladder Resistor Control

ANLADE	A/D ladder resistance control
0	A/D ladder resistance OFF (A/D conversion stopped)
1	A/D ladder resistance ON (A/D conversion operated)

■A/D Conversion Activation Factor Selection Setup

The A/D conversion activation factor is set by the ANSTSEL flag of the ANCTR2 register. The ANSTSEL flag of the ANCTR2 register is set to "1" to start A/D conversion by the external interrupt 3. And if the ANST flag of the ANCTR2 register is set to "1", A/D conversion can be started.

Table 15-3-5 A/D Conversion Activation Factor Selection

ANSTSEL	A/D conversion activation factor
1	The external interrupt 3, or set the ANST flag to "1".
0	Set the ANST flag to "1".

If the external interrupt 3 is selected as the A/D conversion activation factor, specify the valid edge by the REDG3 flag of the external interrupt 3 control register (IRQ3ICR), and the EDGSEL3 flag of the both edges interrupt control register (EDGDT).

[☞Chapter 3. 3-3 External Interrupts]

Specify the interrupt valid edge before the external interrupt 3 is selected as the A/D conversion activation factor.

■A/D Conversion Starting Setup

A/D conversion starting is set by the ANST flag of the ANCTR2 register. The ANST flag of the ANCTR2 register is set to "1" to start A/D conversion. When the external interrupt 3 is selected as the A/D conversion activation factor, the ANST flag of the ANCTR2 register is set to "1" to start A/D conversion, as the external interrupt 3 is generated. Also, the ANST flag of the ANCTR2 register is set to "1" during A/D conversion, then cleared to "0" as the A/D conversion complete interrupt is generated.

Table 15-3-6 A/D Conversion Starting

ANST	A/D conversion status
1	A/D conversion started or in progress.
0	A/D conversion completed or stopped.

15-3-2 Setup Example

■A/D Converter Setup Example by Registers

A/D conversion is started by setting registers. The analog input pins are set to AN0, the converter clock is set to fs/4, and the sampling hold time is set to TAD x 6. Then, A/D conversion complete interrupt is generated.

An example setup procedure, with a description of each step is shown below.

Setup Procedure	Description
(1) Set the analog input pin. PAIMD (x'3F3C') bp0 : PAIMD0 = 1 PAPLUD (x'3F4A') bp0 : PAPLUD0 = 0 PADIR (x'3F3A') bp0 : PADIR0 = 0	(1) Set the analog input pin (set at the procedure 2) to the special function pin by the port A input mode register (PAIMD). Also, set to no pull-up/ pull-down resistance by the port A pull-up/pull-down resistance control register (PAPLUD), and to input mode by port A direction control register (PADIR).
(2) Select the analog input pin. ANCTR1(x'3FB1') bp2-0 : ANCHS2-0 = 000	(2) Select the analog input pin from AN7-0 (PA7-0) by the ANCHS2-0 flag of the A/D converter control register 1 (ANCTR1).
(3) Select the A/D converter clock. ANCTR0 (x'3FB0') bp5-4 : ANCK1-0 = 01	(3) Select the A/D converter clock by the ANCK1, ANCK0 flag of the A/D converter control register 0 (ANCTR0).
(4) Set the sample and hold time. ANCTR0 (x'3FB0') bp7-6 : ANSH1-0 = 01	(4) Set the sample and hold time by the ANSH1, ANSH0 flag of the A/D converter control register 0 (ANCTR0).
(5) Set the interrupt level. ADICR (x'3FFA') bp7-6 : ADLV1-0 = 00	(5) Set the interrupt level by the ADLV1-0 flag of the A/D conversion complete interrupt control register (ADICR). If any interrupt request flag is already set, clear them. [☞ Chapter 3. 3-1-4 Interrupt Flag Setting]
(6) Enable the interrupt. ADICR (x'3FFA') bp1 : ADIE = 1	(6) Enable the interrupt by setting the ADIE flag the ADICR register to "1".

Setup Procedure	Description
(7) Set the A/D ladder resistance. ANCTR0(x'3FB0') bp3 : ANLADE = 1	(7) Set the ANLADE flag of the A/D converter control register 0 (ANCTR0) to "1" to send a current to the ladder resistance for the A/D conversion.
(8) Start the A/D conversion. ANCTR2(x'3FB2') bp6 : ANSTSEL = 0	(8) Set the ANSTSEL flag of the A/D converter control register 2 (ANCTR2) to "0", and select "writing to the ANST flag of the A/D converter control register 2 (ANCTR2)"as the A/D converter activation factor.
(9) Start the A/D conversion operation. ANCTR2 (x'3FB2') bp7 : ANST = 1	(9) Set the ANST flag of the A/D converter control register 2 (ANCTR2) to "1" to start the A/D conversion.
(10) Complete the A/D conversion. ANBUF0 (x'3FB3') ANBUF1 (x'3FB4')	(10) When the A/D conversion is finished, the A/D conversion complete interrupt is generated and the ANST flag of the A/D converter control register 2 (ANCTR2) is cleared to "0". The result of the conversion is stored to the A/D converter buffer (ANBUF0, 1).

Note : The above (3) to (4) can be set at once.

Start the A/D conversion after the current flowing through the ladder resistors stabilizes. The wait time should be decided by the caluculated times from the ladder resistance (max. 80 kΩ), and the external bypass capacitor connected between $V_{REF}+$ and $V_{REF}-$.

■A/D Conversion Setup Example by External Interrupt 3

The A/D conversion is started by the external interrupt 3. The analog input pin is set to AN0, the converter clock is set to fs/4, and the sample hold time is set to TAD x 6. Then, the A/D conversion complete interrupt is generated.

An example setup procedure, with a description of each step is shown below.

Setup Procedure	Description
(1) Set the analog input pin. PAIMD (x'3F3C') bp0 : PAIMD0 = 1 PAPLUD (x'3F4A') bp0 : PAPLUD0 = 0 PADIR (x'3F3A') bp0 : PADIR0 = 0	(1) Set the analog input pin that set in (2), to the special function pin by the port A input mode register (PAIMD). Also, set no pull-up/pull-down resistance by the port A pull-up/pull-down resistance control register (PAPLUD). Set the analog I/O pin, set in (2), to input mode by port A direction control register (PADIR).
(2) Select the analog input pin. ANCTR1 (x'3FB1') bp2-0 : ANCH2-0 = 000	(2) Select the analog input pin from AN6-0 (PA6-0) by the ANCHS2-0 flag of the A/D converter control register 1 (ANCTR1).
(3) Select the A/D converter clock. ANCTR0 (x'3FB0') bp5-4 : ANCK1-0 = 01	(3) Select the A/D converter clock by the ANCK1, ANCK0 flag of the A/D converter control register 0 (ANCTR0).
(4) Set the sample hold time. ANCTR0 (x'3FB0') bp7-6 : ANSH1-0 = 01	(4) Set the sample hold time by the ANSH1, ANSH0 flag of the A/D converter control register 0 (ANCTR0).
(5) Specify the external interrupt 3 valid edge. IRQ3ICR (x'3FE5') bp5 : REDG3 = 1 EDGDT (x'3F8F') bp3 : EDGSEL3 = 0	(5) Specify the valid edge by the REDG3 flag of the external interrupt 3 control register (IRQ3ICR), the EDGSEL3 flag of the both edges interrupt control register (EDGDT). [☞ Chapter 3. 3-1-4 Interrupt Flag Setup]
(6) Set the interrupt level. ADICR (x'3FFA') bp7-6 : ADLV1-0 = 10	(6) Set the interrupt level by the ADLV1-0 flag of the A/D conversion complete interrupt control register (ADICR). If any interrupt request flag is already set, clear them.

Setup Procedure	Description
(7) Enable the interrupt. ADICR (x'3FFA') bp1 : ADIE = 1	(7) Enable the interrupt by setting the ADIE flag of the ADICR register to "1".
(8) Set the A/D ladder resistance. ANCTR0(x'3FB0') bp3 : ANLADE = 1	(8) Set the ANLADE flag of the A/D converter control register 0 (ANCTR0) to "1" to send a current to the ladder resistance for the A/D conversion.
(9) Select the A/D converter activation factor. ANCTR2 (x'3FB2') bp6 : ANSTSEL = 1	(9) Set the ANSTSEL flag of the A/D converter control register 2 (ANCTR2) to "1", and select "writing to the ANST flag of the A/D converter control register 3 (ANCTR3), the external interrupt 3"as the A/D converter activation factor.
(10) Start the A/D conversion. ANCTR2 (x'3FB2') bp7 : ANST = 1	(10) When the external interrupt 3, set in (5) is generated, the ANST flag of the A/D converter control register 2 (ANCTR2) is set to "1" to start the A/D conversion. And even if the external interrupt 3 is not generated, the A/D conversion is started by setting the ANST flag of the A/D converter control register 2 (ANCTR2) to "1".
(11) Complete the A/D conversion.	(11) When the A/D conversion is finished, the A/D conversion complete interrupt is generated, and the ANST flag of the A/D converter control register 2 (ANCTR2) is cleared to "0". The result of the conversion is stored to the A/D converter buffer (ANBUF0, 1).

Note : The above (3) to (4) can be set at once.

Even if the external interrupt 3 is generated during A/D conversion, the A/D converter is operated in normal. Also, once the A/D conversion is finished, it is never started again.

15-3-3 Cautions

A/D conversion can be damaged by noise easily, therefore, anti-noise measures should be taken adequately .

■Anti-noise measures

To A/D input (analog input pin), add condenser near the V_{SS} pins of micro controller.

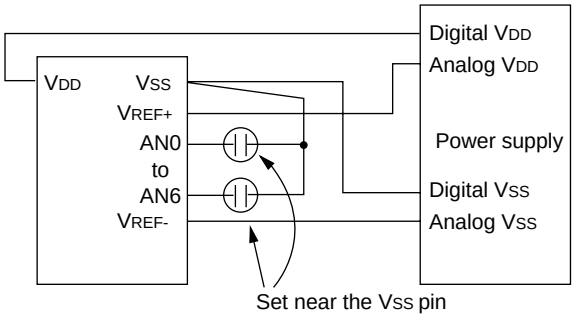


Figure 15-3-2 A/D Converter Recommended Example 1

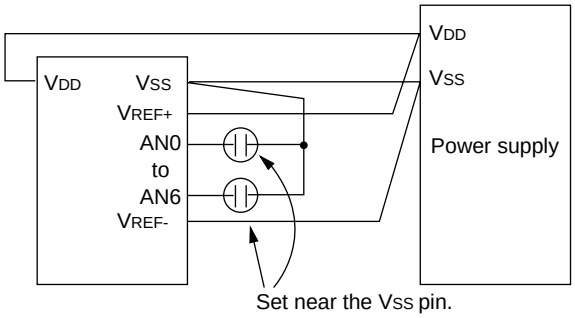
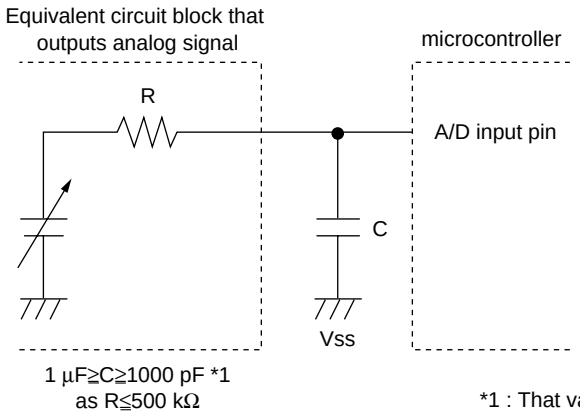


Figure 15-3-3 A/D Converter Recommended Example 2

To maintain high precision of A/D conversion, following instructions on use of A/D converter should be strictly kept.

1. Input impedance R of A/D input pin should be under 500 kΩ[*1]. And connect the external capacitor C (over 1000 pF, under 1 µF)[*1] between Vss and the A/D input pin.
2. Set the A/D conversion frequency depending on the time constant of R and C.
3. Changing the output level of the microcontroller or switching ON/OFF of the peripheral added circuit while the A/D conversion is in progress may lower the precision of A/D conversion, for these may fluctuate the values of the analog input pin and the power pin. Check the waveform of the analog input pin before the system evaluation.



Recommended Connection with A/D Converter

Chapter 16 D/A Converter

16

16-1 Overview

This LSI has a built-in D/A converter with 8 bits solution. There are 2 output channels and 8-bit data registers for each channel. When the D/A converter is not used, the built-in ladder resistance can be set to OFF to save the power consumption.

16-1-1 Functions

Table 16-1-1 shows the D/A converter functions.

Table 16-1-1 D/A Converter Functions

Resolution	8-bit
Pin	DA0/DA1 pin
Power consumption saving	Built-in ladder resistance ON/OFF

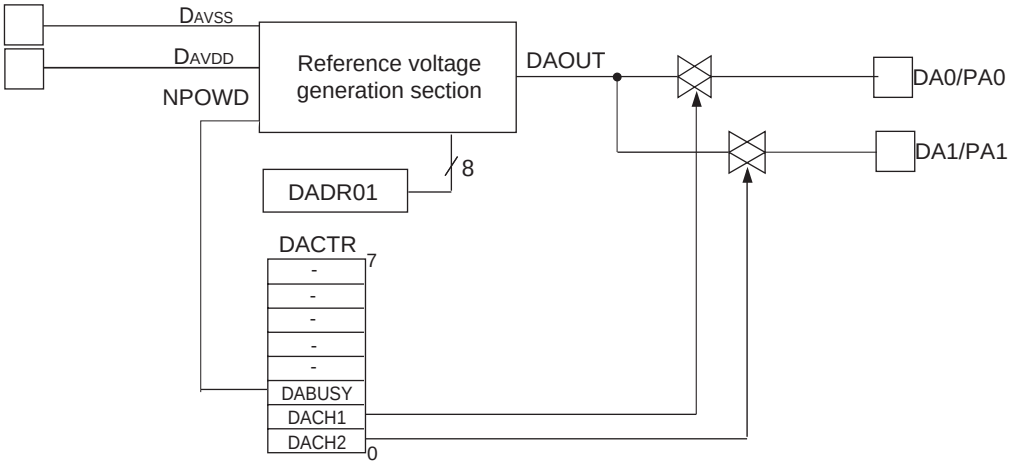


Figure 16-1-1 D/A Converter Block Diagram

16-2 Operation

The D/A converter circuit setup procedure is as follows:

(1) Set the analog pins.
Set the analog input pin, set in (2), to "special function pin" by the port A input mode register (PAIMD).
* Setup for the port A input mode register should be done before analog voltage is put to pins.

(2) Select the analog output pin.
Select the analog output pin from DA1 to DA0 (PA1 to PA0) by the DACH1 to DACH0 flag of the D/A converter control register (DACTR).

(3) Start D/A conversion
Set the DABUSY flag of the D/A converter control register (DACTR) to "1" to apply the ladder resistance current. D/A conversion starts.

(4) DA output.
D/A conversion is done for the data which is set to DADR01 register, and the result of D/A conversion is output to DA0 and DA1.

16-3 Control Registers

16-3-1 Overview

Table 16-3-1 shows the registers to control the D/A converter in MN101C77C.

Table 16-3-1 D/A Converter Control Registers

Register	Address	R/W	Function	Page
DACTR	x'03FBE'	R/W	D/A converter control register	XVII-5
DADR01	x'03FBF'	R/W	D/A converter input data register 01	XVII-6
PADIR	x'03F3A'	R/W	Port A direction control register	IV-42
PAPLUD	x'03F4A'	R/W	Port A pull-up/pull-down resistance control register	IV-42
PAIMD	x'03F3C'	R/W	Port A input control register	IV-43

R/W : Readable/Writable

16-3-2 Control Register (DACTR)

This is the 8-bit readable/writable register that controls the D/A conversion.

■D/A Converter Control Register (DACTR)

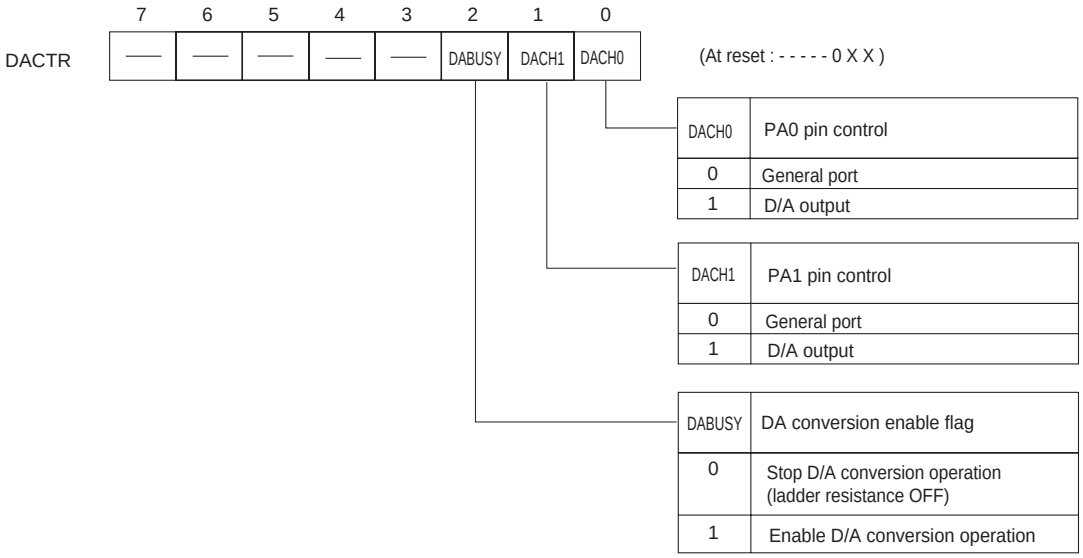


Figure 16-3-1 D/A Converter Control Register (DACTR : x'03FBE' R/W)

16-3-3 Input Data Registers

These readable/writable registers store the A/D converter data.

■D/A Converter Input Data Register 01 (DADR01)
This register stores the D/A conversion data (for DA01 channel).

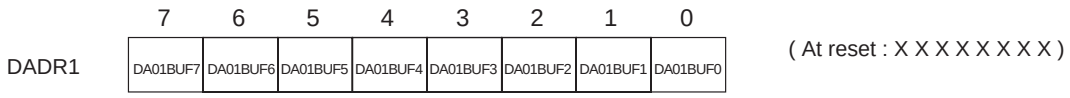


Figure 16-3-2 D/A Converter Input Data Register 01 (DADR01 : x'03FBF' R/W)

16-4 Setup Example

■Channel fixed D/A Converter Setup Example

Conversion channel should be set to DA0.

An example setup procedure, with a description of each step is shown below.

Setup Procedure	Description
(1) Set the port A pin. PAIMD (x'3F3C') bp0 : PAIMD0 = 1 PADIR (x'3F3A') bp0 : PADIR0 = 0 PAPLUD (x'3F4A') bp0 : PAPLUD0 = 0	(1) Set the analog output pin (set at the procedure 2), as the specfical function pin by the port A input mode register (PAIMD). Also, set to "input mode" by the port A I/O direction control register (PADIR), and to "no pull-up resistance" by the port A pull-up resistance control register (PAPLUD).
(2) Set the D/A conversion pin. DACTR (x'3FBE') bp1-0 : DACH1-0 = 01	(2) Set PA0 to D/A output pin by the DACH1-0 flag of the D/A converter control register (DACTR).
(3) Set the D/A converter input data. DADR01 (x'3FBF')	(3) Set the D/A conversion data by the D/A converter input register01 (DADR01).
(4) Start thte D/A conversion. DACTR (x'3FBE') bp2 : DABUSY = 1	(4) Set the DABUSY flag of the D/A converter control register (DACTR) to"1" to start the D/A conversion. The result is output to the DA3-DA0.

Note : The above (1) to (2) can be set at once.

Chapter 17 Appendices

17

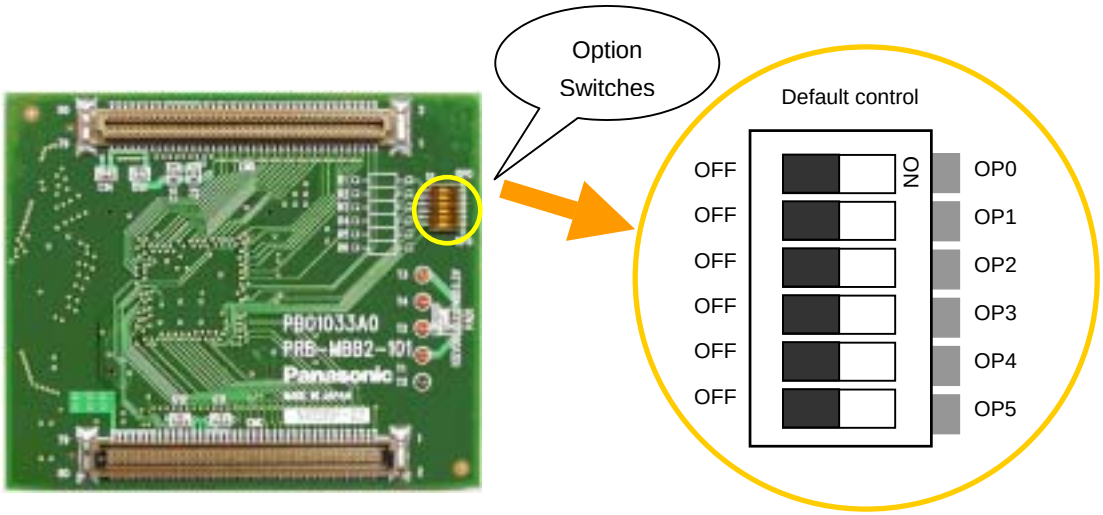
17-1 Probe Switches

17-1-1 PRB-MBB101C77-M

- This probe must be used with the following boards.

  - Connector board: PX-CN101-M
  - MBB board: PRB-MBB101C77-M
  - Adapter board: PRB-ADP101-64-M
  - Dummy target: PRB-DMY101C77-M
    The dummy target should be connected when ICE is operated independently, the adapter board should be connected at connection to the target.
    The power supply voltage of ICE is between 3.0 V to 3.6 V.

  - This probe is mounted the switches for mask option.
  - The option switches are not available.



Top view of MBB board

Figure1: Layout of option switches

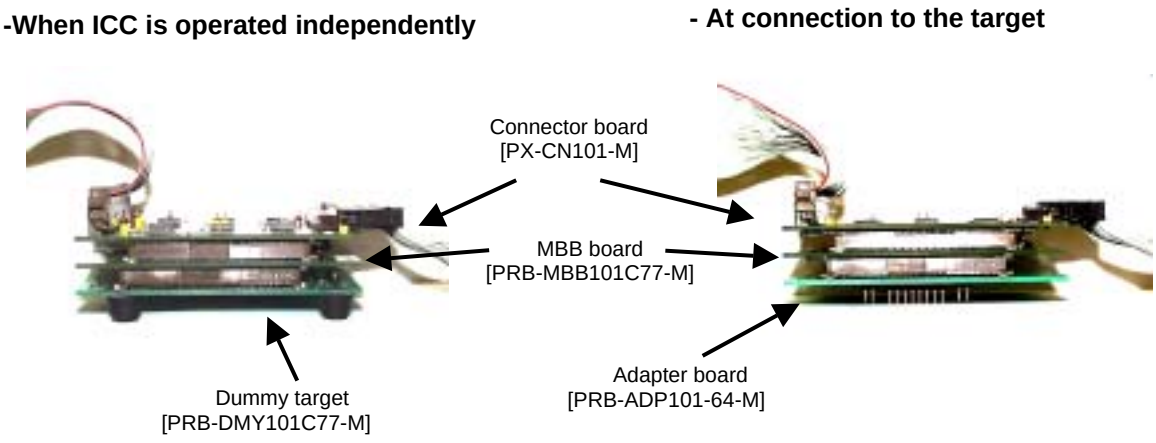


Figure2: Composition with PRB-MBB101C77-M

17-1-2 PX-CN101-M

This board can be used for any MBB models (product No. PRB-MBB101∗∗∗-M) of MN101 series.
(Please visit our website for the latest information on the product.)

Figure1: PX-CN101-M Layout

< How to connect >

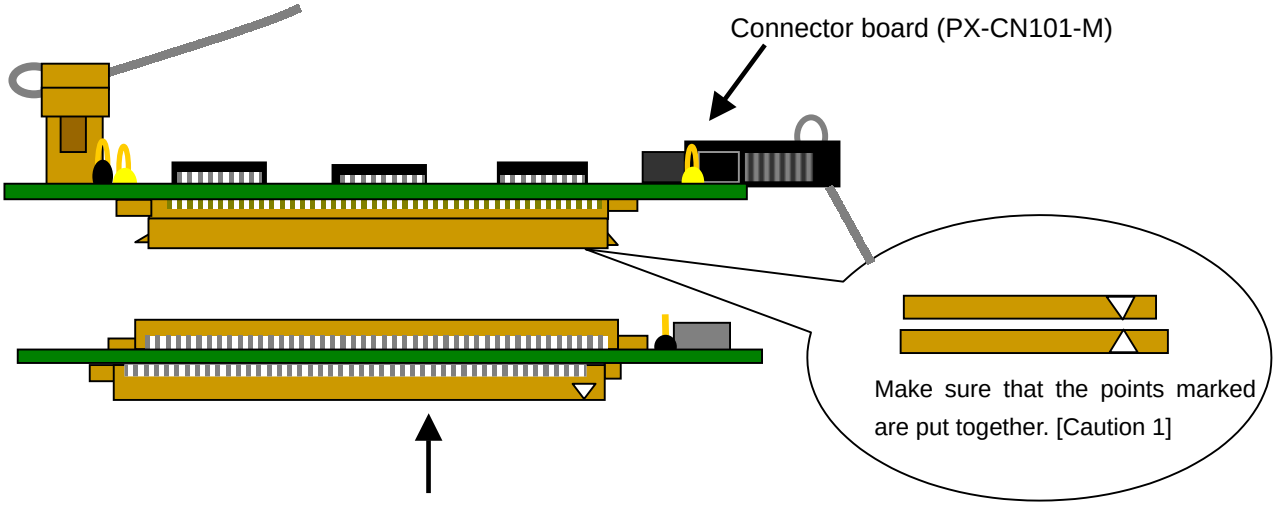


Figure2: PX-CN101-M connection

[Caution1]
Connect CNC of PX-CN101-M to CNC of PRB-MBB101∗∗∗-M, and CND of PX-CN101-M to CND of PRB-MBB101∗∗∗-M.
When connecting the boards, make sure that they are connected without tilt.
If you put pressure on one side of the board, that may cause any damage to the pins.

17-1-3 PRB-ADP101-64-M

When connected to the target, use this board with MBB board.
This board can be used with the following boards.
(The product type is subject to change without prior notice. The latest information should be confirmed on our web site.)

- PRB-MBB101C52-M
- PRB-MBB101C58-M

Improper matching may cause any damage to the ICE.

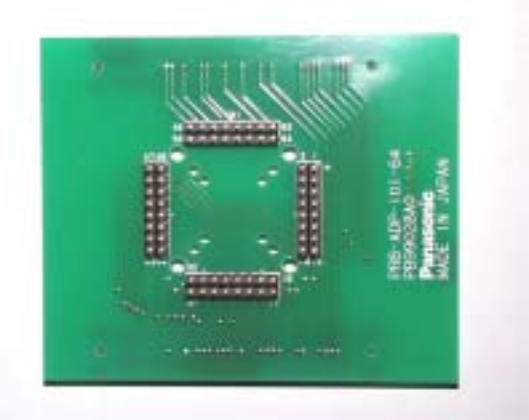
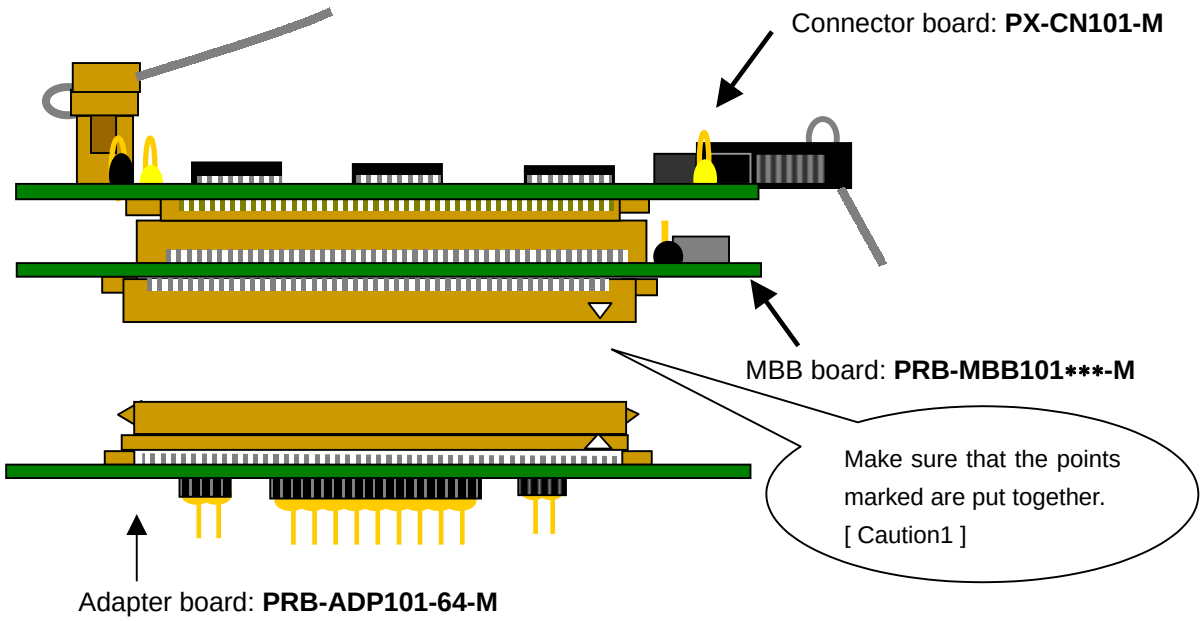


Figure1: PRB-ADP101-64-M Layout

< How to connect >



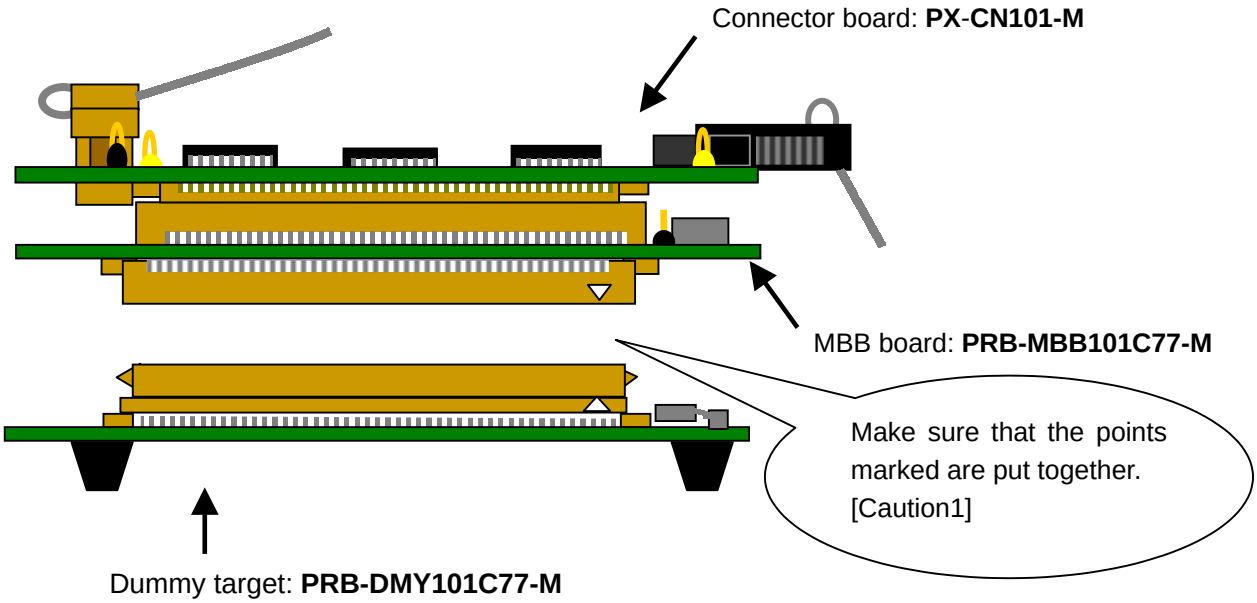
[Caution1] Connect CNE of PRB-MBB101∗∗∗-M to CNE of PRB-ADP101-64-M, and CNF of PRB-MBB101∗∗∗-M to CNF of PRB-ADP101-64-M.
When connecting the boards, make sure that they are connected without tilt.
If you put pressure on one side of the board, that may cause any damage to the pins.

17-1-4 PRB-DMY101C77-M

Dummy target boards differ depending upon the models. This board can be used for only 101C77 64PIN.
When unconnected to the target, use this board with the **PRB-MBB101C77-M**.
Improper matching may cause any damage to the ICE.

Figure1: PRB-DMY101C77-M Layout

< How to connect >



[Caution1]
Connect CNE of PRB-MBB101C77-M to CNE of PRB-DMY101C77-M, and CNF of PRB-MBB101C77-M to CNF of PRB-DMY101C77-M.
When connecting the boards, make sure that they are connected without tilt.
If you put pressure on one side the board, that may cause any damage to the pins.

17-2 Special Function Registers List

Address	Register	Bit Symbol / Initial Value / Description								Page
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
X'3F00'	CPUM	SOSCDBL	OSCSEL1	OSCSEL0	OSCDBL	STOP	HALT	OSC1	OSC0	II - 21 II - 25
		Clock Switching				STOP mode Setup	HALT Mode Setup	Oscillation Control		
X'3F01'	MEMCTR	IOW1	IOW0	IVBM	EXMEM	EXWH	IRWE	EXW1	EXW0	II - 16
		I/O Wait Setup		Interrupt Vector Address	Switch Memory	Switch Wait	Software Writes Setup	Fixed Wait Setup		
X'3F02'	WDCTR	-	-	WDTC2	WDTC1	WDTC0	WDTS1	WDTS0	WDEN	IX - 3
				The lowest value for clear Setup			Watchdog Time-out Period Setup		WDT Activation	
X'3F03'	AREACTR	CS8EXT	CS7EXT	CS6EXT	CS5EXT	CS4EXT	CS3EXT	CS2EXT	CS1EXT	II - 17
		Internal ROM/External Memory Switching								
X'3F05'	CSMD01	CS1MD	CS1W2	CS1W1	CS1W0	-	CS0W2	CS0W1	CS0W0	II - 18
		Bus mode selection	Wait mode selection				Wait mode selection			
X'3F06'	CSMD23	CS3MD	CS3W2	CS3W1	CS3W0	CS2MD	CS2W2	CS2W1	CS2W0	II - 18
		Bus mode selection	Wait mode selection			Bus mode selection	Wait mode selection			
X'3F07'	CSMD45	CS5MD	CS5W2	CS5W1	CS5W0	CS4MD	CS4W2	CS4W1	CS4W0	II -18
		Bus mode selection	Wait mode selection			Bus mode selection	Wait mode selection			
X'3F08'	CSMD67	CS7MD	CS7W2	CS7W1	CS7W0	CS6MD	CS6W2	CS6W1	CS6W0	II - 18
		Bus mode selection	Wait mode selection			Bus mode selection	Wait mode selection			
X'3F09'	CSMD89	Reserved	CS9W2	CS9W1	CS9W0	CS8MD	CS8W2	CS8W1	CS8W0	II - 18
		Set always to "1"	Wait mode selection			Bus mode selection	Wait mode selection			
X'3F0A'	SBNKR	-	-	-	-	-	-	SBA1	SBA0	II - 28
								Bank for Source Address Setup		
X'3F0B'	DBNKR	-	-	-	-	-	-	DBA1	DBA0	II - 28
								Bank for Destination Address Setup		
X'3F0E'	RCCTR	-	-	-	-	-	RC2EN	RC1EN	RC0EN	II - 32
							ROM Correction Control			
X'3F10'	P0OUT	-	P0OUT6	P0OUT5	P0OUT4	P0OUT3	P0OUT2	P0OUT1	P0OUT0	IV - 7
		Port 0 Output Data								
X'3F11'	P1OUT	-	-	-	P1OUT4	P1OUT3	P1OUT2	P1OUT1	P1OUT0	IV - 13
					Port 1 Output Data					
X'3F12'	P2OUT	P2OUT7	-	-	P2OUT4	P2OUT3	P2OUT2	P2OUT1	P2OUT0	IV - 18
		Port 2 Output Data			Port 2 Output Data					
X'3F15'	P5OUT				P5OUT4	P5OUT3	P5OUT2	P5OUT1	P5OUT0	IV - 22
		-	-	-	Port 5 Output Data					
X'3F16'	P6OUT	P6OUT7	P6OUT6	P6OUT5	P6OUT4	P6OUT3	P6OUT2	P6OUT1	P6OUT0	IV - 27
		Port 6 Output Data								
X'3F17	P7OUT	P7OUT7	P7OUT6	P7OUT5	P7OUT4	P7OUT3	P7OUT2	P7OUT1	P7OUT0	IV - 31
		Port 7 Output Data								
X'3F18	P8OUT	P8OUT7	P8OUT6	P8OUT5	P8OUT4	P8OUT3	P8OUT2	P8OUT1	P8OUT0	IV - 38
		Port 8 Output Data								

Address	Register	Bit Symbol /Initial Value /Description								Page
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
X'3F1A'	PAOUT	-	PAOUT6	PAOUT5	P8OUT4	P8OUT3	P8OUT2	P8OUT1	P8OUT0	IV - 42
		Port A Output Data								
X'3F1D'	P8LED	P8LED7	P8LED6	P8LED5	P8LED4	P8LED3	P8LED2	P8LEDT1	P8LED0	IV - 39
		Port 8 Transistor Selection								
X'3F1E'	P6SYO	P6SYO7	P6SYO6	P6SYO5	P6SYO4	P6SYO3	P6SYO2	P6SYO1	P6SYO0	IV - 28
		Port 6 Synchronous Output Selection								
X'3F20'	P0IN	-	P0IN6	P0IN5	P0IN4	P0IN3	P0IN2	P0IN1	P0IN0	IV - 7
			Port 0 Input Data							
X'3F21'	P1IN	-	-	-	P1IN4	P1IN3	P1IN2	P1IN1	P1IN0	IV - 13
					Port 1 Input Data					
X'3F22'	P2IN	P2IN7	-	-	P2IN4	P2IN3	P2IN2	P2IN1	P2IN0	IV - 18
		Port 2 Input Data								
X'3F25'	P5IN	-	-	-	P5IN4	P5IN3	P5IN2	P5IN1	P5IN0	IV - 22
					Port 5 Input Data					
X'3F26'	P6IN	P6IN7	P6IN6	P6IN5	P6IN4	P6IN3	P6IN2	P6IN1	P6IN0	IV - 27
		Port 6 Input Data								
X'3F27'	P7IN	P7IN7	P7IN6	P7IN5	P7IN4	P7IN3	P7IN2	P7IN1	P7IN0	IV - 31
		Port 7 Input Data								
X'3F28'	P8IN	P8IN7	P8IN6	P8IN5	P8IN4	P8IN3	P8IN2	P8IN1	P8IN0	IV - 38
		Port 8 Input Data								
X'3F2A'	PAIN	-	PAIN6	PAIN5	PAIN4	PAIN3	PAIN2	PAIN1	PAIN0	IV - 42
			Port A Input Data							
X'3F2B'	KEYCNT	-	-	-	-	-	-	-	LOCKEN	II - 42
									Register Data Protection Function	
X'3F2D'	OSCMD	-	-	-	-	-	-	SOSC2DS	Reserved	II - 25
								Low Frequency Divided by 2	Set always to "0"	
X'3F2E'	FLOAT	-	PARDWN	-	P7RDWN	-	-	SYOEVS1	SYOEVS0	IV - 32, 43
			PA Pull-up/down Selection		P7 Pull-up/down Selection			P6 Synchronous Output Event Selection		
X'3F2F'	P1OMD	-	P1OMD6	P1OMD5	P1OMD4	P1OMD3	P1OMD2	P1OMD1	P1OMD0	IV - 14
			P77 Output mode Selection	P76 Output mode Selection	P14 Output mode Selection	P13 Output mode Selection	P12 Output mode Selection	P11 Output mode Selection	P10 Output mode Selection	
X'3F30'	P0DIR	-	P0DIR6	P0DIR5	P0DIR4	P0DIR3	P0DIR2	P0DIR1	P0DIR0	IV - 7
		Port 0 I/O Direction Control								
X'3F31'	P1DIR	-	-	-	P1DIR4	P1DIR3	P1DIR2	P1DIR1	P1DIR0	IV - 13
					Port 1 I/O Direction Control					
X'3F32'	P2DIR	-	-	-	P2DIR4	P2DIR3	P2DIR2	P2DIR1	P2DIR0	IV - 18
					Port 2 I/O Direction Control					
X'3F35'	P5DIR	-	-	-	P5DIR4	P5DIR3	P5DIR2	P5DIR1	P5DIR0	IV - 22
					Port 5 I/O Direction Control					

Address	Register	Bit Symbol /Initial Value /Description								Page
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
X'3F36'	P6DIR	P6DIR7	P6DIR6	P6DIR5	P6DIR4	P6DIR3	P6DIR2	P6DIR1	P6DIR0	IV - 27
		Port 6 I/O Direction Control								
X'3F37'	P7DIR	P7DIR7	P7DIR6	P7DIR5	P7DIR4	P7DIR3	P7DIR2	P7DIR1	P7DIR0	IV - 31
		Port 7 I/O Direction Control								
X'3F38'	P8DIR	P8DIR7	P8DIR6	P8DIR5	P8DIR4	P8DIR3	P8DIR2	P8DIR1	P8DIR0	IV - 38
		Port 8 I/O Direction Control								
X'3F3A'	PADIR	-	PADIR6	PADIR5	PADIR4	PADIR3	PADIR2	PADIR1	PADIR0	IV - 42
		Port A I/O Direction Control								
X'3F3C'	PAIMD	-	PAIMD6	PAIMD5	PAIMD4	PAIMD3	PAIMD2	PAIMD1	PAIMD0	IV - 43
				Port A Analog Input Selection						
X'3F3E'	P6IMD	IRQ4SEL	-	-	-	P6KYEN4	P6KYEN3	P6KYEN2	P6KYEN1	III - 46
		IRQ4 Interrupt Source Selection				Port 6 Key Input Interrupt Pin Setup				
X'3F40'	P0PLU	-	P0PLU6	P0PLU5	P0PLU4	P0PLU3	P0PLU2	P0PLU1	P0PLU0	IV - 7
		Port 0 Pull-up Control								
X'3F41'	P1PLU	-	-	-	P1PLU4	P1PLU3	P1PLU2	P1PLU1	P1PLU0	IV - 13
					Port 1 Pull-up Control					
X'3F42'	P2PLU	-	-	-	P2PLU4	P2PLU3	P2PLU2	P2PLU1	P2PLU0	IV - 18
					Port 2 Pull-up Control					
X'3F45'	P5PLU	-	-	-	P5PLU4	P5PLU3	P5PLU2	P5PLU1	P5PLU0	IV - 22
					Port 5 Pull-up Control					
X'3F46'	P6PLU	P6PLU7	P6PLU6	P6PLU5	P6PLU4	P6PLU3	P6PLU2	P6PLU1	P6PLU0	IV - 27
		Port 6 Pull-up Control								
X'3F47'	P7PLUD	P7PLUD7	P7PLUD6	P7PLUD5	P7PLUD4	P7PLUD3	P7PLUD2	P7PLUD1	P7PLUD0	IV - 31
		Port 7 Pull-up/Pull-down Control								
X'3F48'	P8PLU	P8PLU7	P8PLU6	P8PLU5	P8PLU4	P8PLU3	P8PLU2	P8PLU1	P8PLU0	IV - 38
			Port 8 Pull-up Control							
X'3F4A'	PAPLUD	-	PAPLUD6	PAPLUD5	PAPLUD4	PAPLUD3	PAPLUD2	PAPLUD1	PAPLUD0	IV - 42
			Port A Pull-up/Pull-down Control							
X'3F4D'	DLYCTR	BUZOE	BUZS2	BUZS1	BUZS0	DLYS2	DLYS1	DLYS0	-	II - 41 X - 3
		Buzzer Output Enable	Buzzer Output Frequency Selection			Osscillation Stabilization Wait Time Selection				
X'3F50'	TM0BC	TM0BC7	TM0BC6	TM0BC5	TM0BC4	TM0BC3	TM0BC2	TM0BC1	TM0BC0	VI - 9
		Timer 0 Binary Counter								
X'3F51'	TM1BC	TM1BC7	TM1BC6	TM1BC5	TM1BC4	TM1BC3	TM1BC2	TM1BC1	TM1BC0	VI - 9
		Timer 1 Binary Counter								
X'3F52'	TM0OC	TM0OC7	TM0OC6	TM0OC5	TM0OC4	TM0OC3	TM0OC2	TM0OC1	TM0OC0	VI - 8
		Timer 0 Output Compare Register								

Address	Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Page
X'3F53'	TM1OC	TM1OC7	TM1OC6	TM1OC5	TM1OC4	TM1OC3	TM1OC2	TM1OC1	TM1OC0	VI - 8
		Timer 1 Output Compare Register								
X'3F54'	TM0MD	-	-	TM0MOD	TM0PWM	TM0EN	TM0CK2	TM0CK1	TM0CK0	VI - 10
				Timer 0 Pulse Width Measurement	PWM Operation Selection	Timer 0 Count Control	Timer 0 Clock Source Selection			
X'3F55'	TM1MD	-	-	-	TM1CAS	TM1EN	TM1CK2	TM1CK1	TM1CK0	VI - 11
					Cascade Selection	Timer 1 Count Control	Timer 1 Clock Source Selection			
X'3F56'	CK0MD	-	-	-	-	-	TM0PSC1	TM0PSC0	TM0BAS	V - 7
							Timer 0 Count Clock Setup (Prescaler Output)			
X'3F57'	CK1MD	-	-	-	-	-	TM1PSC1	TM1PSC0	TM1BAS	V - 7
							Timer 1 Count Clock Setup (Prescaler Output)			
X'3F60'	TM4BC	TM4BC7	TM4BC6	TM4BC5	TM4BC4	TM4BC3	TM4BC2	TM4BC1	TM4BC0	VI - 9
		Timer 4 Binary Counter								
X'3F61'	TM5BC	TM5BC7	TM5BC6	TM5BC5	TM5BC4	TM5BC3	TM5BC2	TM5BC1	TM5BC0	VI - 9
		Timer 5 Binary Counter								
X'3F62'	TM4OC	TM4OC7	TM4OC6	TM4OC5	TM4OC4	TM4OC3	TM4OC2	TM4OC1	TM4OC0	VI - 8
		Timer 4 Output Compare Register								
X'3F63'	TM5OC	TM5OC7	TM5OC6	TM5OC5	TM5OC4	TM5OC3	TM5OC2	TM5OC1	TM5OC0	VI - 8
		Timer 5 Output Compare Register								
X'3F64'	TM4MD			TM4MOD	TM4PWM	TM4EN	TM4CK2	TM4CK1	TM4CK0	VI - 12
				Timer 4 Pulse Width Measurement	PWM Operation Selection	Timer 4 Count Control	Timer 4 Clock Source Selection			
X'3F65'	TM5MD	-	-	TM5MOD	TM5PWM	TM5EN	TM5CK2	TM5CK1	TM5CK0	VI - 13
				Timer 5 Pulse Width Measurement	PWM Operation Selection	Timer 5 Count Control	Timer 5 Clock Source Selection			
X'3F66'	CK4MD	-	-	-	-	-	TM4PSC1	TM4PSC0	TM4BAS	V - 8
							Timer 4 Count Clock Setup (Prescaler Output)			
X'3F67'	CK5MD	-	-	-	-	-	TM5PSC1	TM5PSC0	TM5BAS	V - 8
							Timer 5 Count Clock Setup (Prescaler Output)			
X'3F68'	TM6BC	TM6BC7	TM6BC6	TM6BC5	TM6BC4	TM6BC3	TM6BC2	TM6BC1	TM6BC0	VIII - 5
		Timer 6 Binary Counter								
X'3F69'	TM6OC	TM6OC7	TM6OC6	TM6OC5	TM6OC4	TM6OC3	TM6OC2	TM6OC1	TM6OC0	VIII - 5
		Timer 6 Output Compare Register								
X'3F6A'	TM6MD	-	-	TM0MOD	TM0PWM	TM0EN	TM0CK2	TM0CK1	TM0CK0	VIII - 6
		Counter Clear Selection	Time Base Timer Interrupt Cycle Selection			Timer 6 Clock Source Selection			Time Base Timer Clock Source Selection	
X'3F6B'	TBCLR	-	-	-	TM1CAS	TM1EN	TM1CK2	TM1CK1	TM1CK0	VIII - 5
		Timer Base Timer Clear Control Register (For Writing Only)								
X'3F6E'	RMCTR	-	-	-	TM0RM	RM0EN	-	RMDTY0	RMBTMS	VI - 14
					P10 Special Function Output Selection	Enable Remote Control Output		Remote Control Duty Selection	Remote Control Base Timer Selection	
X'3F6F'	PSCMD	-	-	-	-	-	-	-	PSCEN	V - 6
									Prescaler Count Control	

Address	Register	Bit Symbol /Initial Value /Description								Page
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 7	
X'3F70'	TM7BCL	TM7BCL7	TM7BCL6	TM7BCL5	TM7BCL4	TM7BCL3	TM7BCL2	TM7BCL1	TM7BCL0	VII - 7
		Timer 7 Binary Counter Lower 8 Bits								
X'3F71'	TM7BCH	TM7BCH7	TM7BCH6	TM7BCH5	TM7BCH4	TM7BCH3	TM7BCH2	TM7BCH1	TM7BCH0	VII - 7
		Timer 7 Binary Counter Upper 8 Bits								
X'3F72'	TM7OC1L	TM7OC1L7	TM7OC1L6	TM7OC1L5	TM7OC1L4	TM7OC1L3	TM7OC1L2	TM7OC1L1	TM7OC1L0	VII - 5
		Timer 7 Output Compare Register 1 Lower 8 Bits								
X'3F73'	TM7OC1H	TM7OC1H7	TM7OC1H6	TM7OC1H5	TM7OC1H4	TM7OC1H3	TM7OC1H2	TM7OC1H1	TM7OC1H0	VII - 5
		Timer 7 Output Compare Register 1 Upper 8 Bits								
X'3F74'	TM7PR1L	TM7PR1L7	TM7PR1L6	TM7PR1L5	TM7PR1L4	TM7PR1L3	TM7PR1L2	TM7PR1L1	TM7PR1L0	VII - 6
		Timer 7 Preset Register 1 Lower 8 Bits								
X'3F75'	TM7PR1H	TM7PR1H7	TM7PR1H6	TM7PR1H5	TM7PR1H4	TM7PR1H3	TM7PR1H2	TM7PR1H1	TM7PR1H0	VII - 6
		Timer 7 Preset Register 1 Upper 8 Bits								
X'3F76'	TM7ICL	TM7ICL7	TM7ICL6	TM7ICL5	TM7ICL4	TM7ICL3	TM7ICL2	TM7ICL1	TM7ICL0	VII - 7
		Timer 7 Input Capture Register Lower 8 Bits								
X'3F77'	TM7ICH	TM7ICH7	TM7ICH6	TM7ICH5	TM7ICH4	TM7ICH3	TM7ICH2	TM7ICH1	TM7ICH0	VII - 7
		Timer 7 Input Capture Register Upper 8 Bits								
X'3F78'	TM7MD1	Reserved	Reserved	TM7CL	TM7EN	TM7PS1	TM7PS0	TM7CK1	TM7CK0	VII - 8
		Set Always to "0"	Set Always to "0"	Timer 7 Output Reset Control	Timer 7 Count Control	Timer 7 Count Clock Selection		Timer 7 Clock Source Selection		
X'3F79'	TM7MD2	T7ICEDG	T7PWMSL	TM7BCR	TM7PWM	TM7IRS1	T7ICEN	T7ICT1	T7ICT0	VII - 9
		Capture Trigger Edge Selection	PWM Mode Selection	Clear Factor Selection	Timer 7 Output Selection	Timer 7 Interrupt Factor Selection	Enable Capture Operation	Timer 7 Capture Trigger Selection		
X'3F7A'	TM7OC2L	TM7OC2L7	TM7OC2L6	TM7OC2L5	TM7OC2L4	TM7OC2L3	TM7OC2L2	TM7OC2L1	TM7OC2L0	VII - 5
		Timer 7 Output Compare Register 2 Lower 8 Bits								
X'3F7B'	TM7OC2H	TM7OC2H7	TM7OC2H6	TM7OC2H5	TM7OC2H4	TM7OC2H3	TM7OC2H2	TM7OC2H1	TM7OC2H0	VII - 5
		Timer 7 Output Compare Register 2 Upper 8 Bits								
X'3F7C'	TM7PR2L	TM7PR2L7	TM7PR2L6	TM7PR2L5	TM7PR2L4	TM7PR2L3	TM7PR2L2	TM7PR2L1	TM7PR2L0	VII - 6
		Timer 7 Preset Register 2 Lower 8 Bits								
X'3F7D'	TM7PR2H	TM7PR2H7	TM7PR2H6	TM7PR2H5	TM7PR2H4	TM7PR2H3	TM7PR2H2	TM7PR2H1	TM7PR2H0	VII - 6
		Timer 7 Preset Register 2 Upper 8 Bits								
X'3F7E'	P1TCNT	-	-	P1CNT5	P1CNT4	P1CNT3	P1CNT2	P1CNT1	P1CNT0	IV - 15
				P14 Output Data Control		P12 Output Data Control		P10 Output Data Control		
X'3F8D'	NFCTR1	-	-	-	-	-	NF4EN	NF3EN	NF2EN	III - 44
							IRQ4 Noise Filter Enable	IRQ3 Noise Filter Enable	IRQ2 Noise Filter Enable	
X'3F8E'	NFCTR0	P21IM	NF1SCK1	NF1SCK0	NF1EN	-	NF0SCK1	NF0SCK0	NF0EN	III - 43
		ACZ Input Enable Flag	IRQ1 Noise Filter Sampling Period Selection		IRQ1 Noise Filter Enable		IRQ0 Noise Filter Sampling Period Selection		IRQ0 Noise Filter Enable	
X'3F8F'	EDGDT	-	-	Reserved	EDGSEL4	EDGSEL3	EDGSEL2	EDGSEL1	EDGSEL0	III - 45
				Set Always to "0"	IRQ4 Both Edge Specification	IRQ3 Both Edge Specification	IRQ2 Both Edge Specification	IRQ1 Both Edge Specification	IRQ0 Both Edge Specification	
X'3F90'	RXBUF0	RXBUF07	RXBUF06	RXBUF05	RXBUF04	RXBUF03	RXBUF02	RXBUF01	RXBUF00	XI - 7
		Serial Interface 0 Data Reception Buffer								

Address	Register	Bit Symbol /Initial Value /Description								Page
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
X'3F91'	TXBUF0	TXBUF07	TXBUF06	TXBUF05	TXBUF04	TXBUF03	TXBUF02	TXBUF01	TXBUF00	XI - 7
		Serial Interface 0 Data Transfer Buffer								
X'3F92'	SC0MD0	SC0CE1	SC0REN	SC0TRN	SC0DIR	SC0STE	SC0LNG2	SC0LNG1	SC0LNG0	XI - 8
		Transmission/ Reception Data Edge Selection	Reception data Polarity Change	Transmission data Polarity Change	Specify First Bit to be Transfered	Start Condition Selection	Synchronous Serial Transfer Bit Count Selection			
X'3F93'	SC0MD1	SC0IOM	SC0SBTS	SC0SBIS	SC0SBOS	SC0CKM	SC0MST	-	SC0CMD	XI - 9
		Data Input Pin Selection	SBT Pin Function Selection	Serial Input Control	SBO Pin Function Selection	Clock Divided By 8 Selection	Master/Slave Selection		Synchronous/ UART Selection	
X'3F94'	SC0MD2	SC0FM1	SC0FM0	SC0PM1	SC0PM0	SC0NPE	-	SC0BRKF	SC0BRKE	XI - 10
		Specify Flame Mode		Specify Added Bit		Parity Enable		Break Status Receive Monitor	Break Status Transmit Control	
X'3F95'	SC0MD3	SC0TBSY	SC0RBSY	SC0TEMP	SC0REMP	SC0FEF	SC0PEK	SC0ORE	SC0ERE	XI - 11
		Transmission Flag	Reception Flag	Transfer Buffer Empty Flag	Receive Buffer Empty Flag	Framing Error Detection	Parity Error Detection	Overrun Error Detection	Error Monitor Flag	
X'3F96'	SC0ODC	SC0SEL	Reserved	-	-	SC0ODC3	SC0ODC2	SC0ODC1	SC0ODC0	XI - 12
		I/O Type Selection	Set Always to "0"			P72 Output Type Selection	P70 Output Type Selection	P05 Output Type Selection	P03 Output Type Selection	
X'3F97'	SC0CKS	-	-	-	-	-	SC0PSC2	SC0PSC1	SC0PSC0	V - 9 XI - 13
							Serial 0 Transfer Clock Selection (Prescaler Output)			
X'3F98'	RXBUF1	RXBUF17	RXBUF16	RXBUF15	RXBUF14	RXBUF13	RXBUF12	RXBUF11	RXBUF10	XI - 14
		Serial Interface 1 Reception Data Buffer								
X'3F99'	TXBUF1	TXBUF17	TXBUF16	TXBUF15	TXBUF14	TXBUF13	TXBUF12	TXBUF11	TXBUF10	XI - 14
		Serial Interface 1 Transmission Data Buffer								
X'3F9A'	SC1MD0	SC1CE1	SC1REN	SC1TRN	SC1DIR	SC1STE	SC1LNG2	SC1LNG1	SC1LNG0	XI - 15
		Transmission/ Reception Data Edge Selection	Reception data Polarity Change	Transmission data Polarity Change	Specify First Bit to be Transfered	Start Condition Selection	Synchronous Serial Transfer Bit Count Selection			
X'3F9B'	SC1MD1	SC1IOM	SC1SBTS	SC1SBIS	SC1SBOS	SC1CKM	SC1MST	-	SC1CMD	XI - 16
		Data Input Pin Selection	SBT Pin Function Selection	Serial Input Control	SBO Pin Function Selection	Clock Divided By 8 Selection	Master/Slave Selection		Synchronous/ UART Selection	
X'3F9C'	SC1MD2	SC1FM1	SC1FM0	SC1PM1	SC1PM0	SC1NPE	-	SC1BRKF	SC1BRKE	XI - 17
		Specify Flame Mode		Specify Added Bit		Parity Enable		Break Status Receive Monitor	Break Status Transmit Control	
X'3F9D'	SC1MD3	SC1TBSY	SC1RBSY	SC1TEMP	SC1REMP	SC1FEF	SC1PEK	SC1ORE	SC1ERE	XI - 18
		Transmission Flag	Reception Flag	Transfer Buffer Empty Flag	Receive Buffer Empty Flag	Framing Error Detection	Parity Error Detection	Overrun Error Detection	Error Monitor Flag	
X'3F9E'	SC1ODC	SC1SEL	Reserved	-	-	SC1ODC3	SC1ODC2	SC1ODC1	SC1ODC0	XI - 19
		I/O Type Selection	Set Always to "0"			P75 Output Type Selection	P73 Output Type Selection	P02 Output Type Selection	P00 Output Type Selection	
X'3F9F'	SC1CKS	-	-	-	-	-	SC1PSC2	SC1PSC1	SC1PSC0	V - 9 XI - 20
							Serial 1 Transfer Clock Selection (Prescaler Output)			
X'3FA8'	SC3MD0	SC3BSY	SC3CE1	-	SC3DIR	SC3STE	SC3LNG2	SC3LNG1	SC3LNG0	XII - 6
		Transmission Flag	Transfer Edge Selection		Specify First Bit to be Transfered	Start Condition Selection	Synchronous Serial Transfer Bit Count Selection			
X'3FA9'	SC3MD1	SC3IOM	SC3SBTS	SC3SBIS	SC3SBOS	-	SC3MST	-	-	XII - 7
		Data Input Pin Selection	SBT Pin Function Selection	Serial Input Control	SBO Pin Function Selection		Master/Slave Selection			
X'3FAA'	SC3CTR	IICBSY	SC3STC	-	-	SC3REX	SC3CMD	SC3ACKS	SC3ACK0	XII - 8
		IIC in Use Transfer Flag	Start Condition Detection Flag			IIC Transmission /Reception Status	Synchronous/ IIC Selection	ACK bit Enable	ACK bit Level	
X'3FAB'	SC3TRB	SC3TRB7	SC3TRB6	SC3TRB5	SC3TRB4	SC3TRB3	SC3TRB2	SC3TRB1	SC3TRB0	XII - 5
		Serial Interface 3 Transmission/Reception Shift Register								

Address	Register	Bit Symbol /Initial Value /Description								Page
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
X'3FAE'	SC3ODC	-	Reserved	-	-	-	-	SC3ODC1	SC3ODC0	XII - 9
			Set Always to "0"					P52 Output Type Selection	P51 Output Type Selection	
X'3FAF'	SC3CKS	-	-	-	-	-	SC3PSC2	SC3PSC1	SC3PSC0	V - 10 XII - 9
							Serial 3 Transfer Clock Selection (Prescaler Output)			
X'3FB0'	ANCTR0	ANSH1	ANSH0	ANCK1	ANCK0	ANLADE	-	-	-	XV - 5
		A/D Sample Hold Timer Setup		A/D Conversion Clock Selection		A/D Rudder Resistance Control				
X'3FB1'	ANCTR1	-	-	-	-	Reserved	ANCHS2	ANCHS1	ANCHS0	XV - 6
						Set Always to "0"	Analog Input Channel Selection			
X'3FB2'	ANCTR2	ANST	ANSTSEL	-	-	-	-	-	-	XV - 6
		A/D Conversion Status	A/D Conversion Start Factor Selection							
X'3FB3'	ANBUF0	ANBUF07	ANBUF06	-	-	-	-	-	-	XV - 7
		A/D Conversion Data Storage Register (Lower 2 bits)								
X'3FB4'	ANBUF1	ANBUF17	ANBUF16	ANBUF15	ANBUF14	ANBUF13	ANBUF12	ANBUF11	ANBUF10	XV - 7
		A/D Conversion Data Storage Register (Upper 8 bits)								
X'3FBE'	DACTR	-	-	-	-	-	DABUSY	DACH1	DACH0	XVI - 5
							D/A Conversion Enable Flag	PA1 Output Type Selection	PA0 Output Type Selection	
X'3FBF'	DADR01	DA01BUF7	DA01BUF6	DA01BUF5	DA01BUF4	DA01BUF3	DA01BUF2	DA01BUF1	DA01BUF0	XVI - 6
		D/A Conversion Data Storage Register								
X'3FC7'	RC0APL	RC0APL7	RC0APL6	RC0APL5	RC0APL4	RC0APL3	RC0APL2	RC0APL1	RC0APL0	II - 33
		ROM Correction Address 0 Setting Register Lower 8 bits								
X'3FC8'	RC0APM	RC0APM7	RC0APM6	RC0APM5	RC0APM4	RC0APM3	RC0APM2	RC0APM1	RC0APM0	II - 33
		ROM Correction Address 0 Setting Register Middle 8 bits								
X'3FC9'	RC0APH	-	-	-	-	-	-	RC0APH1	RC0APH0	II - 33
		ROM Correction Addreess 0 Setting Register Upper 2 bits								
X'3FCA'	RC1APL	RC1APL7	RC1APL6	RC1APL5	RC1APL4	RC1APL3	RC1APL2	RC1APL1	RC1APL0	II - 33
		ROM Correction Address 1 Setting Register Lower 8 bits								
X'3FCB'	RC1APM	RC1APM7	RC1APM6	RC1APM5	RC1APM4	RC1APM3	RC1APM2	RC1APM1	RC1APM0	II - 33
		ROM Correction Address 1 Setting Register Middle 8 bits								
X'3FCC'	RC1APH	-	-	-	-	-	-	RC1APH1	RC1APH0	II - 33
		ROM Correction Addreess 1 Setting Register Upper 2 bits								
X'3FCD'	RC2APL	RC2APL7	RC2APL6	RC2APL5	RC2APL4	RC2APL3	RC2APL2	RC2APL1	RC2APL0	II - 34
		ROM Correction Address 2 Setting Register Lower 8 bits								
X'3FCE'	RC2APM	RC2APM7	RC2APM6	RC2APM5	RC2APM4	RC2APM3	RC2APM2	RC2APM1	RC2APM0	II - 34
		ROM Correction Address 2 Setting Register Middle 8 bits								
X'3FCF'	RC2APH	-	-	-	-	-	-	RC2APH1	RC2APH0	II - 34
		ROM Correction Addreess 2 Setting Register Upper 2 bits								
X'3FD0'	ATCNT0	FMODE	AT1ACT	ATMD3	ATMD2	ATMD1	ATMD0	Reserved	AT1EN	XIV - 6
		Pointer 0 Increment Control	ATC1 Program Activation Flag	ATC1 Data Transfer Mode Selection				Set Always to "0"	ATC1 Transfer Enable	

Address	Register	Bit Symbol /Initial Value /Description								Page
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
X'3FD1'	ATCNT1	-	-	-	BTSTP	AT1IR3	AT1IR2	AT1IR1	AT1IR0	XIV - 7
					Burst Transfer Enable flag	ATC1 Activation Factor Selection				
X'3FD2'	AT1TRC	AT1TRC7	AT1TRC6	AT1TRC5	AT1TRC4	AT1TRC3	AT1TRC2	AT1TRC1	AT1TRC0	XIV - 7
		ATC1 Transfer Count Setting								
X'3FD3'	AT1MAP0L	AT1MAP0L7	AT1MAP0L6	AT1MAP0L5	AT1MAP0L4	AT1MAP0L3	AT1MAP0L2	AT1MAP0L1	AT1MAP0L0	XIV - 8
		ATC1 Memory Pointer 0 Lower 8 bits								
X'3FD4'	AT1MAP0M	AT1MAP0M15	AT1MAP0M14	AT1MAP0M13	AT1MAP0M12	AT1MAP0M11	AT1MAP0M10	AT1MAP0M9	AT1MAP0M8	XIV - 8
		ATC1 Memory Pointer 0 Middle 8 bits								
X'3FD5'	AT1MAP0H	-	-	-	-	-	-	AT1MAP0H17	AT1MAP0H16	XIV - 8
								ATC1 Memory Pointer 0 Upper 2 bits		
X'3FD6'	AT1MAP1L	AT1MAP1L7	AT1MAP1L6	AT1MAP1L5	AT1MAP1L4	AT1MAP1L3	AT1MAP1L2	AT1MAP1L1	AT1MAP1L0	XIV - 8
		ATC1 Memory Pointer 1 Lower 8 bits								
X'3FD7'	AT1MAP1M	AT1MAP1L15	AT1MAP1L14	AT1MAP1M13	AT1MAP1M12	AT1MAP1M11	AT1MAP1M10	AT1MAP1M9	AT1MAP1M8	XIV - 8
		ATC1 Memory Pointer 1 Middle 8 bits								
X'3FD8'	AT1MAP1H	-	-	-	-	-	-	AT1MAP1H17	AT1MAP1H16	XIV - 8
								ATC1 Memory Pointer 1 Upper 2 bits		
X'3FE1'	NMICR	-	-	-	-	-	PIR	WDIR	RESERVED	III - 16
							Program Interrupt Request	Watchdog Timer Interrupt Request	Set Always to "0"	
X'3FE2'	IRQ0ICR	IRQ0LV1	IRQ0LV0	REDG0	-	-	-	IRQ0IE	IRQ0IR	III - 17
		Specify IRQ0 Interrupt Level		IRQ0 Interrupt Valid Edge				Enable IRQ0 Interrupt	Request IRQ0 Interrupt	
X'3FE3'	IRQ1ICR	IRQ1LV1	IRQ1LV0	REDG1	-	-	-	IRQ1IE	IRQ1IR	III - 18
		Specify IRQ1 Interrupt Level		IRQ1 Interrupt Valid Edge				Enable IRQ1 Interrupt	Request IRQ1 Interrupt	
X'3FE4'	IRQ2ICR	IRQ2LV1	IRQ2LV0	REDG2	-	-	-	IRQ2IE	IRQ2IR	III - 19
		Specify IRQ2 Interrupt Level		IRQ2 Interrupt Valid Edge				Enable IRQ2 Interrupt	Request IRQ2 Interrupt	
X'3FE5'	IRQ3ICR	IRQ3LV1	IRQ3LV0	REDG3	-	-	-	IRQ3IE	IRQ3IR	III - 20
		Specify IRQ3 Interrupt Level		IRQ3 Interrupt Valid Edge				Enable IRQ3 Interrupt	Request IRQ3 Interrupt	
X'3FE6'	IRQ4ICR	IRQ4LV1	IRQ4LV0	REDG4	-	-	-	IRQ4IE	IRQ4IR	III - 21
		Specify IRQ4 Interrupt Level		IRQ4 Interrupt Valid Edge				Enable IRQ4 Interrupt	Request IRQ4 Interrupt	
X'3FE9'	TM0ICR	TM0LV1	TM0LV0	-	-	-	-	TM0IE	TM0IR	III - 22
		Specify TM0 Interrupt Level						Enable TM0 Interrupt	Request TM0 Interrupt	
X'3FEA'	TM1ICR	TM1LV1	TM1LV0	-	-	-	-	TM1IE	TM1IR	III - 23
		Specify TM1 Interrupt Level						Enable TM1 Interrupt	Request TM1 Interrupt	
X'3FED'	TM4ICR	TM4LV1	TM4LV0	-	-	-	-	TM4IE	TM4IR	III - 24
		Specify TM4 Interrupt Level						Enable TM4 Interrupt	Request TM4 Interrupt	
X'3FEE'	TM5ICR	TM5LV1	TM5LV0	-	-	-	-	TM5IE	TM5IR	III - 25
		Specify TM5 Interrupt Level						Enable TM5 Interrupt	Request TM5 Interrupt	
X'3FEF'	TM6ICR	TM6LV1	TM6LV0	-	-	-	-	TM6IE	TM6IR	III - 26
		Specify TM6 Interrupt Level						Enable TM6 Interrupt	Request TM6 Interrupt	

Address	Register	Bit Symbol /Initial Value /Description								Page
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
X'3FF0'	TBICR	TBLV1	TBLV0	-	-	-	-	TBIE	TBIR	III - 27
		Specify TB Interrupt Level						Enable TB Interrupt	Request TB Interrupt	
X'3FF1'	TM7ICR	TM7LV1	TM7LV0	-	-	-	-	TM7IE	TM7IR	III - 28
		Specify TM7 Interrupt Level						Enable TM7 Interrupt	Request TM7 Interrupt	
X'3FF2'	T7OC2ICR	T7OC2LV1	T7OC2LV0	-	-	-	-	T7OC2IE	T7OC2IR	III - 29
		Specify T7OC2 Interrupt Level						Enable T7OC2 Interrupt	Request T7OC2 Interrupt	
X'3FF4'	SC0RICR	SC0RLV1	SC0RLV0	-	-	-	-	SC0RIE	SC0RIR	III - 30
		Specify SC0 Reception Interrupt Level						Enable SC0 Reception Interrupt	Request SC0 Reception Interrupt	
X'3FF5'	SC0TICR	SC0TLV1	SC0TLV0	-	-	-	-	SC0TIE	SC0TIR	III - 31
		Specify SC0 Transmission Interrupt Level						Enable SC0 Transmission Interrupt	Request SC0 Transmission Interrupt	
X'3FF6'	SC1RICR	SC1RLV1	SC1RLV0	-	-	-	-	SC1RIE	SC1RIR	III - 32
		Specify SC1 Reception Interrupt Level						Enable SC1 Reception Interrupt	Request SC1 Reception Interrupt	
X'3FF7'	SC1TICR	SC1TLV1	SC1TLV0	-	-	-	-	SC1TIE	SC1TIR	III - 33
		Specify SC1 Transmission Interrupt Level						Enable SC1 Transmission Interrupt	Request SC1 Transmission Interrupt	
X'3FF9'	SC3ICR	SC3LV1	SC3LV0	-	-	-	-	SC3IE	SC3IR	III - 34
		Specify SC3 Interrupt Level						Enable SC3 Interrupt	Request SC3 Interrupt	
X'3FFA'	ADICR	ADLV1	ADLV0	-	-	-	-	ADIE	ADIR	III - 36
		Specify AD Interrupt Level						Enable AD Interrupt	Request AD Interrupt	
X'3FFC'	ATC1ICR	ATC1LV1	ATC1LV0	-	-	-	-	ATC1IE	ATC1IR	III - 37
		Specify ATC1 Interrupt Level						Enable ATC1 Interrupt	Request ATC1 Interrupt	
X'3FA3'	SC4AD0	I2CAD7	I2CAD6	I2CAD5	I2CAD4	I2CAD3	I2CAD2	I2CAD1	I2CAD0	XIII - 6
		Address Setting Register								
X'3FA4'	SC4AD1	SELI2C	Reserved	Reserved	I2CPSEL	I2CGEM	I2CADM	I2CAD9	I2CAD8	XIII - 6
		Enable Communication Operation	Set Always to "0"	Set Always to "0"	Serial Pin Selection	Comunication Mode Selection	Address Setting Selection	Address Setting Register		
X'3FA5'	SC4TXB	I2CTXB7	I2CTXB6	I2CTXB5	I2CTXB4	I2CTXB3	I2CTXB2	I2CTXB1	I2CTXB0	XIII - 5
		Data Transmission Buffer								
X'3FAD'	SC4RXB	I2CRXB7	I2CRXB6	I2CRXB5	I2CRXB4	I2CRXB3	I2CRXB2	I2CRXB1	I2CRXBS0	XIII - 5
		Data Reception Buffer								
X'3FAC'	SC4STR	WRS	I2CINT	STRT	RSTRT	I2CBSY	SLVBSY	ACKVALID	-	XIII - 7
		Transfer Direction Determination	Interrupt Detection	Start Detection	Restart Detection	Bus Busy Detection	Slave Busy Detection	ACK Signal Detection		
X'3F3F'	SC4ODC0	-	-	-	-	-	-	SC4ODC01	SC4ODC00	XIII - 8
								P02 Output Type Selection	P01 Output Type Selection	
X'3F3D'	SC4ODC1	-	-	-	-	-	-	SC4ODC11	SC4ODC10	XIII - 8
								P54 Otput Type Selection	P53 Output Type Selection	
X'3FF3'	SC4ICR	SC4LV1	SC4LV0	-	-	-	-	SC4IE	SC4IR	III - 35
		SC4 Interrupt Level Setting						Enable SC4 Interrupt	Enable SC4 Interrupt	

Address	Register	Bit Symbol / Initial Value / Description								Page
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
X'3FA3'	SC4AD0	I2CAD7	I2CAD6	I2CAD5	I2CAD4	I2CAD3	I2CAD2	I2CAD1	I2CAD0	XIV - 6
		Addressing Register								
X'3FA4'	SC4AD1	SELI2C	Reserved	Reserved	I2CPSEL	I2CGEM	I2CADM	I2CAD9	I2CAD8	XIV - 6
		Communication Enable			Serial Interface Pin Selection	Communication Mode Selection	Address Selection	Addressing Register		
X'3FA5'	SC4TXB	I2CTXB7	I2CTXB6	I2CTXB5	I2CTXB4	I2CTXB3	I2CTXB2	I2CTXB1	I2CTXB0	XIV - 5
		Data Transmission Buffer								
X'3FAD'	SC4RXB	I2CRXB7	I2CRXB6	I2CRXB5	I2CRXB4	I2CRXB3	I2CRXB2	I2CRXB1	I2CRXBS0	XIV - 5
		Data Reception Buffer								
X'3FAC'	SC4STR	WRS	I2CINT	STRT	RSTRT	I2CBSY	SLVBSY	ACKVALID	-	XIV - 7
		Transfer Direction Determination	Interrupt Detection	Start Detection	Re-Start Detection	Bus Busy Detection	Slave Busy Detection	ACK Signal Detection		
X'3F3F'	SC4ODC0	-	-	-	-	-	-	SC4ODC01	SC4ODC00	XIV - 8
								P05 Output Type Selection	P03 Output Type Selection	
X'3F3D'	SC4ODC1	-	-	-	-	-	-	SC4ODC11	SC4ODC10	XIV - 8
								P05 Output Type Selection	P03 Output Type Selection	
X'3FF3'	SC4ICR	SC4LV1	SC4LV0	-	-	-	-	SC4IE	SC4IR	III - 39
		SC4 Interrupt Level Setup						SC4 Interrupt Enable	SC4 Interrupt Request	

17-3 Instruction Set

MN101C SERIES INSTRUCTION SET

Group	Mnemonic	Operation	Flag VF	Flag NF	Flag CF	Flag ZF	Code Size	Cycle	Re-peat	Machine Code Ext.	1	2	3	4	5	6	7	8	9	10	11	Notes
Data Move Instructions																						
MOV	MOV Dn,Dm	Dn Dm	--	--	--	--	2	1		1010	DnDm											
	MOV imm8,Dm	imm8 Dm	--	--	--	--	4	2		1010	DmDm	<#8.	...>									
	MOV Dn,PSW	Dn PSW	●	●	●	●	3	3		0010	1001	01Dn										
	MOV PSW,Dm	PSW Dm	--	--	--	--	3	2		0010	0001	01Dm										
	MOV (An),Dm	mem8(An) Dm	--	--	--	--	2	2		0100	1ADm											
	MOV (d8,An),Dm	mem8(d8+An) Dm	--	--	--	--	4	2		0110	1ADm	<d8.	...>									*1
	MOV (d16,An),Dm	mem8(d16+An) Dm	--	--	--	--	7	4		0010	0110	1ADm	<d16	....	....	...>						
	MOV (d4,SP),Dm	mem8(d4+SP) Dm	--	--	--	--	3	2		0110	01Dm	<d4>										*2
	MOV (d8,SP),Dm	mem8(d8+SP) Dm	--	--	--	--	5	3		0010	0110	01Dm	<d8.	...>								*3
	MOV (d16,SP),Dm	mem8(d16+SP) Dm	--	--	--	--	7	4		0010	0110	00Dm	<d16	....	....	...>						
	MOV (io8),Dm	mem8(IOTOP+io8) Dm	--	--	--	--	4	2		0110	00Dm	<io8	...>									
	MOV (abs8),Dm	mem8(abs8) Dm	--	--	--	--	4	2		0100	01Dm	<abs	8..>									
	MOV (abs12),Dm	mem8(abs12) Dm	--	--	--	--	5	2		0100	00Dm	<abs	12..	...>								
	MOV (abs16),Dm	mem8(abs16) Dm	--	--	--	--	7	4		0010	1100	00Dm	<abs	16..	....	...>						
	MOV Dn,(Am)	Dn mem8(Am)	--	--	--	--	2	2		0101	1aDn											
	MOV Dn,(d8,Am)	Dn mem8(d8+Am)	--	--	--	--	4	2		0111	1aDn	<d8.	...>									*1
	MOV Dn,(d16,Am)	Dn mem8(d16+Am)	--	--	--	--	7	4		0010	0111	1aDn	<d16	....	....	...>						
	MOV Dn,(d4,SP)	Dn mem8(d4+SP)	--	--	--	--	3	2		0111	01Dn	<d4>										*2
	MOV Dn,(d8,SP)	Dn mem8(d8+SP)	--	--	--	--	5	3		0010	0111	01Dn	<d8.	...>								*3
	MOV Dn,(d16,SP)	Dn mem8(d16+SP)	--	--	--	--	7	4		0010	0111	00Dn	<d16	....	....	...>						
	MOV Dn,(io8)	Dn mem8(IOTOP+io8)	--	--	--	--	4	2		0111	00Dn	<io8	...>									
	MOV Dn,(abs8)	Dn mem8(abs8)	--	--	--	--	4	2		0101	01Dn	<abs	8..>									
	MOV Dn,(abs12)	Dn mem8(abs12)	--	--	--	--	5	2		0101	00Dn	<abs	12..	...>								
	MOV Dn,(abs16)	Dn mem8(abs16)	--	--	--	--	7	4		0010	1101	00Dn	<abs	16..	....	...>						
	MOV imm8,(io8)	imm8 mem8(IOTOP+io8)	--	--	--	--	6	3		0000	0010	<io8	...>	<#8.	...>							
	MOV imm8,(abs8)	imm8 mem8(abs8)	--	--	--	--	6	3		0001	0100	<abs	8..>	<#8.	...>							
	MOV imm8,(abs12)	imm8 mem8(abs12)	--	--	--	--	7	3		0001	0101	<abs	12..	...>	<#8.	...>						
	MOV imm8,(abs16)	imm8 mem8(abs16)	--	--	--	--	9	5		0011	1101	1001	<abs	16..	....	...>	<#8.	...>				
	MOV Dn,(HA)	Dn mem8(HA)	--	--	--	--	2	2		1101	00Dn											
MOVW	MOVW (An),DWm	mem16(An) DWm	--	--	--	--	2	3		1110	00Ad											
	MOVW (An),Am	mem16(An) Am	--	--	--	--	3	4		0010	1110	10Aa										*4
	MOVW (d4,SP),DWm	mem16(d4+SP) DWm	--	--	--	--	3	3		1110	011d	<d4>										*2
	MOVW (d4,SP),Am	mem16(d4+SP) Am	--	--	--	--	3	3		1110	010a	<d4>										*2
	MOVW (d8,SP),DWm	mem16(d8+SP) DWm	--	--	--	--	5	4		0010	1110	011d	<d8.	...>								*3
	MOVW (d8,SP),Am	mem16(d8+SP) Am	--	--	--	--	5	4		0010	1110	010a	<d8.	...>								*3
	MOVW (d16,SP),DWm	mem16(d16+SP) DWm	--	--	--	--	7	5		0010	1110	001d	<d16	....	....	...>						
	MOVW (d16,SP),Am	mem16(d16+SP) Am	--	--	--	--	7	5		0010	1110	000a	<d16	....	....	...>						
	MOVW (abs8),DWm	mem16(abs8) DWm	--	--	--	--	4	3		1100	011d	<abs	8..>									
	MOVW (abs8),Am	mem16(abs8) Am	--	--	--	--	4	3		1100	010a	<abs	8..>									
	MOVW (abs16),DWm	mem16(abs16) DWm	--	--	--	--	7	5		0010	1100	011d	<abs	16..	....	...>						
	MOVW (abs16),Am	mem16(abs16) Am	--	--	--	--	7	5		0010	1100	010a	<abs	16..	....	...>						
	MOVW DWn,(Am)	DWn mem16(Am)	--	--	--	--	2	3		1111	00aD											
	MOVW An,(Am)	An mem16(Am)	--	--	--	--	3	4		0010	1111	10aA										*4
	MOVW DWn,(d4,SP)	DWn mem16(d4+SP)	--	--	--	--	3	3		1111	011D	<d4>										*2
	MOVW An,(d4,SP)	An mem16(d4+SP)	--	--	--	--	3	3		1111	010A	<d4>										*2
	MOVW DWn,(d8,SP)	DWn mem16(d8+SP)	--	--	--	--	5	4		0010	1111	011D	<d8.	...>								*3
	MOVW An,(d8,SP)	An mem16(d8+SP)	--	--	--	--	5	4		0010	1111	010A	<d8.	...>								*3
	MOVW DWn,(d16,SP)	DWn mem16(d16+SP)	--	--	--	--	7	5		0010	1111	001D	<d16	....	....	...>						
	MOVW An,(d16,SP)	An mem16(d16+SP)	--	--	--	--	7	5		0010	1111	000A	<d16	....	....	...>						
	MOVW DWn,(abs8)	DWn mem16(abs8)	--	--	--	--	4	3		1101	011D	<abs	8..>									
	MOVW An,(abs8)	An mem16(abs8)	--	--	--	--	4	3		1101	010A	<abs	8..>									
	MOVW DWn,(abs16)	DWn mem16(abs16)	--	--	--	--	7	5		0010	1101	011D	<abs	16..	....	...>						
	MOVW An,(abs16)	An mem16(abs16)	--	--	--	--	7	5		0010	1101	010A	<abs	16..	....	...>						
	MOVW DWn,(HA)	DWn mem16(HA)	--	--	--	--	2	3		1001	010D											
	MOVW An,(HA)	An mem16(HA)	--	--	--	--	2	3		1001	011A											
	MOVW imm8,DWm	sign(imm8) DWm	--	--	--	--	4	2		0000	110d	<#8.	...>									*5
	MOVW imm8,Am	zero(imm8) Am	--	--	--	--	4	2		0000	111a	<#8.	...>									*6
	MOVW imm16,DWm	imm16 DWm	--	--	--	--	6	3		1100	111d	<#16	....	....	...>							

*1 d8 sign-extension
*2 d4 zero-extension
*3 d8 zero-extension
*4 A=An, a=Am
*5 #8 sign-extension
*6 #8 zero-extension

MN101C SERIES INSTRUCTION SET

Group	Mnemonic	Operation	Flag VF	NF	CF	ZF	Code Size	Cycle	Re-peat	extension	Machine Code 1 2 3 4 5 6 7 8 9 10 11	Notes
	MOVW imm16,Am	imm16 Am	--	--	--	--	6	3			1101 111a <#16 ....>	
	MOVW SP,Am	SP Am	--	--	--	--	3	3			0010 0000 100a	
	MOVW An,SP	An SP	--	--	--	--	3	3			0010 0000 101A	
	MOVW DWn,DWm	DWn DWm	--	--	--	--	3	3			0010 1000 00Dd	*1
	MOVW DWn,Am	DWn Am	--	--	--	--	3	3			0010 0100 11Da	
	MOVW An,DWm	An DWm	--	--	--	--	3	3			0010 1100 11Ad	
	MOVW An,Am	An Am	--	--	--	--	3	3			0010 0000 00Aa	*2
PUSH	PUSH Dn	SP-1 SP,Dn mem8(SP)	--	--	--	--	2	3			1111 10Dn	
	PUSH An	SP-2 SP,An mem16(SP)	--	--	--	--	2	5			0001 011A	
POP	POP Dn	mem8(SP) Dn,SP+1 SP	--	--	--	--	2	3			1110 10Dn	
	POP An	mem16(SP) An,SP+2 SP	--	--	--	--	2	4			0000 011A	
EXT	EXT Dn,DWm	sign(Dn) DWm	--	--	--	--	3	3			0010 1001 000d	*3
Arithmetic manupulation instructions												
ADD	ADD Dn,Dm	Dm+Dn Dm	●	●	●	●	3	2			0011 0011 DnDm	
	ADD imm4,Dm	Dm+sign(imm4) Dm	●	●	●	●	3	2			1000 00Dm <#4>	*6
	ADD imm8,Dm	Dm+imm8 Dm	●	●	●	●	4	2			0000 10Dm <#8. ...>	
ADDC	ADDC Dn,Dm	Dm+Dn+CF Dm	●	●	●	●	3	2	O		0011 1011 DnDm	
ADDW	ADDW DWn,DWm	DWm+DWn DWm	●	●	●	●	3	3	O		0010 0101 00Dd	*1
	ADDW DWn,Am	Am+DWn Am	●	●	●	●	3	3	O		0010 0101 10Da	
	ADDW imm4,Am	Am+sign(imm4) Am	●	●	●	●	3	2			1110 110a <#4>	*6
	ADDW imm8,Am	Am+sign(imm8) Am	●	●	●	●	5	3			0010 1110 110a <#8. ...>	*7
	ADDW imm16,Am	Am+imm16 Am	●	●	●	●	7	4			0010 0101 011a <#16 ....>	
	ADDW imm4,SP	SP+sign(imm4) SP	--	--	--	--	3	2			1111 1101 <#4>	*6
	ADDW imm8,SP	SP+sign(imm8) SP	--	--	--	--	4	2			1111 1100 <#8. ...>	*7
	ADDW imm16,SP	SP+imm16 SP	--	--	--	--	7	4			0010 1111 1100 <#16 ....>	
	ADDW imm16,DWm	DWm+imm16 DWm	●	●	●	●	7	4			0010 0101 010d <#16 ....>	
ADDUW	ADDUW Dn,Am	Am+zero(Dn) Am	●	●	●	●	3	3	O		0010 1000 1aDn	*8
ADDSW	ADDSW Dn,Am	Am+sign(Dn) Am	●	●	●	●	3	3	O		0010 1001 1aDn	
SUB	SUB Dn,Dm(when Dn Dm)	Dm-Dn Dm	●	●	●	●	3	2	O		0010 1010 DnDm	
	SUB Dn,Dn	Dn-Dn Dn	0	0	0	1	2	1			1000 01Dn	
	SUB imm8,Dm	Dm-imm8 Dm	●	●	●	●	5	3			0010 1010 DmDm <#8. ...>	
SUBC	SUBC Dn,Dm	Dm-Dn-CF Dm	●	●	●	●	3	2	O		0010 1011 DnDm	
SUBW	SUBW DWn,DWm	DWm-DWn DWm	●	●	●	●	3	3			0010 0100 00Dd	*1
	SUBW DWn,Am	Am-DWn Am	●	●	●	●	3	3			0010 0100 10Da	
	SUBW imm16,DWm	DWm-imm16 DWm	●	●	●	●	7	4			0010 0100 010d <#16 ....>	
	SUBW imm16,Am	Am-imm16 Am	●	●	●	●	7	4			0010 0100 011a <#16 ....>	
MULU	MULU Dn,Dm	Dm*Dn DWk	0	●	●	●	3	8			0010 1111 111D	*4
DIVU	DIVU Dn,DWm	DWm/Dn DWm-l...DWm-h	●	●	●	●	3	9			0010 1110 111d	*5
CMP	CMP Dn,Dm	Dm-Dn...PSW	●	●	●	●	3	2			0011 0010 DnDm	
	CMP imm8,Dm	Dm-imm8...PSW	●	●	●	●	4	2			1100 00Dm <#8. ...>	
	CMP imm8,(abs8)	mem8(abs8)-imm8...PSW	●	●	●	●	6	3			0000 0100 <abs 8..> <#8. ...>	
	CMP imm8,(abs12)	mem8(abs12)-imm8...PSW	●	●	●	●	7	3			0000 0101 <abs 12.. ...> <#8. ...>	
	CMP imm8,(abs16)	mem8(abs16)-imm8...PSW	●	●	●	●	9	5			0011 1101 1000 <abs 16.. ....> <#8. ...>	
CMPW	CMPW DWn,DWm	DWm-DWn...PSW	●	●	●	●	3	3			0010 1000 01Dd	*1
	CMPW DWn,Am	Am-DWn...PSW	●	●	●	●	3	3			0010 0101 11Da	
	CMPW An,Am	Am-An...PSW	●	●	●	●	3	3			0010 0000 01Aa	*2
	CMPW imm16,DWm	DWm-imm16...PSW	●	●	●	●	6	3			1100 110d <#16 ....>	
	CMPW imm16,Am	Am-imm16...PSW	●	●	●	●	6	3			1101 110a <#16 ....>	
Logical manipulation instructions												
AND	AND Dn,Dm	Dm&Dn Dm	0	●	0	●	3	2			0011 0111 DnDm	
	AND imm8,Dm	Dm&imm8 Dm	0	●	0	●	4	2			0001 11Dm <#8. ...>	
	AND imm8,PSW	PSW&imm8 PSW	●	●	●	●	5	3			0010 1001 0010 <#8. ...>	
OR	OR Dn,Dm	DmlDn Dm	0	●	0	●	3	2			0011 0110 DnDm	
	OR imm8,Dm	Dmlimm8 Dm	0	●	0	●	4	2			0001 10Dm <#8. ...>	
	OR imm8,PSW	PSWlimm8 PSW	●	●	●	●	5	3			0010 1001 0011 <#8. ...>	
XOR	XOR Dn,Dm	Dm^Dn Dm	0	●	0	●	3	2			0011 1010 DnDm	*9
	XOR imm8,Dm	Dm^imm8 Dm	0	●	0	●	5	3			0011 1010 DmDm <#8. ...>	

*1 D=DWn, d=DWm
*2 A=An, a=Am
*3 d=DWm
*4 D=DWk
*5 D=DWm
*6 #4 sign-extension
*7 #8 sign-extension
*8 Dn zero extension
*9 m≠n

MN101C SERIES INSTRUCTION SET

Group	Mnemonic	Operation	Flag VF	Flag NF	Flag CF	Flag ZF	Code Size	Cycle	Re-peat	Extension	Machine Code 1	2	3	4	5	6	7	8	9	10	11	Notes
NOT	NOT Dn	¯Dn Dn=	0	●	0	●	3	2			0010	0010	10Dn									
ASR	ASR Dn	Dn.msb temp,Dn.lsb CF Dn>>1 Dn,temp Dn.msb	0	--	●	●	3	2	○		0010	0011	10Dn									
LSR	LSR Dn	Dn.lsb CF,Dn>>1 Dn 0 Dn.msb	0	0	●	●	3	2	○		0010	0011	11Dn									
ROR	ROR Dn	Dn.lsb temp,Dn>>1 Dn CF Dn.msb,temp CF	0	●	●	●	3	2	○		0010	0010	11Dn									
Bit manipulation instructions																						
BSET	BSET (io8)bp	mem8(IOTOP+io8)&bpdata...PSW 1 mem8(IOTOP+io8)bp	0	●	0	●	5	5			0011	1000	0bp.	<io8	...>							
	BSET (abs8)bp	mem8(abs8)&bpdata...PSW 1 mem8(abs8)bp	0	●	0	●	4	4			1011	0bp.	<abs	8..>								
	BSET (abs16)bp	mem8(abs16)&bpdata...PSW 1 mem8(abs16)bp	0	●	0	●	7	6			0011	1100	0bp.	<abs	16..	....	...>					
BCLR	BCLR (io8)bp	mem8(IOTOP+io8)&bpdata...PSW 0 mem8(IOTOP+io8)bp	0	●	0	●	5	5			0011	1000	1bp.	<io8	...>							
	BCLR (abs8)bp	mem8(abs8)&bpdata...PSW 0 mem8(abs8)bp	0	●	0	●	4	4			1011	1bp.	<abs	8..>								
	BCLR (abs16)bp	mem8(abs16)&bpdata...PSW 0 mem8(abs16)bp	0	●	0	●	7	6			0011	1100	1bp.	<abs	16..	....	...>					
BTST	BTST imm8,Dm	Dm&imm8...PSW	0	●	0	●	5	3			0010	0000	11Dm	<#8.	...>							
	BTST (abs16)bp	mem8(abs16)&bpdata...PSW	0	●	0	●	7	5			0011	1101	0bp.	<abs	16..	....	...>					
Branch instructions																						
Bcc	BEQ label	if(ZF=1), PC+3+d4(label)+H PC if(ZF=0), PC+3 PC	--	--	--	--	3	2/3			1001	000H	<d4>									*1
	BEQ label	if(ZF=1), PC+4+d7(label)+H PC if(ZF=0), PC+4 PC	--	--	--	--	4	2/3			1000	1010	<d7.	...H								*2
	BEQ label	if(ZF=1), PC+5+d11(label)+H PC if(ZF=0), PC+5 PC	--	--	--	--	5	2/3			1001	1010	<d11	....	...H							*3
	BNE label	if(ZF=0), PC+3+d4(label)+H PC if(ZF=1), PC+3 PC	--	--	--	--	3	2/3			1001	001H	<d4>									1
	BNE label	if(ZF=0), PC+4+d7(label)+H PC if(ZF=1), PC+4 PC	--	--	--	--	4	2/3			1000	1011	<d7.	...H								*2
	BNE label	if(ZF=0), PC+5+d11(label)+H PC if(ZF=1), PC+5 PC	--	--	--	--	5	2/3			1001	1011	<d11	....	...H							*3
	BGE label	if((VF^NF)=0),PC+4+d7(label)+H PC if((VF^NF)=1),PC+4 PC	--	--	--	--	4	2/3			1000	1000	<d7.	...H								*2
	BGE label	if((VF^NF)=0),PC+5+d11(label)+H PC if((VF^NF)=1),PC+5 PC	--	--	--	--	5	2/3			1001	1000	<d11	....	...H							*3
	BCC label	if(CF=0),PC+4+d7(label)+H PC if(CF=1), PC+4 PC	--	--	--	--	4	2/3			1000	1100	<d7.	...H								*2
	BCC label	if(CF=0), PC+5+d11(label)+H PC if(CF=1), PC+5 PC	--	--	--	--	5	2/3			1001	1100	<d11	....	...H							*3
	BCS label	if(CF=1),PC+4+d7(label)+H PC if(CF=0), PC+4 PC	--	--	--	--	4	2/3			1000	1101	<d7.	...H								*2
	BCS label	if(CF=1), PC+5+d11(label)+H PC if(CF=0), PC+5 PC	--	--	--	--	5	2/3			1001	1101	<d11	....	...H							*3
	BLT label	if((VF^NF)=1),PC+4+d7(label)+H PC if((VF^NF)=0),PC+4 PC	--	--	--	--	4	2/3			1000	1110	<d7.	...H								*2
	BLT label	if((VF^NF)=1),PC+5+d11(label)+H PC if((VF^NF)=0),PC+5 PC	--	--	--	--	5	2/3			1001	1110	<d11	....	...H							*3
	BLE label	if((VF^NF)|ZF=1),PC+4+d7(label)+H PC if((VF^NF)|ZF=0),PC+4 PC	--	--	--	--	4	2/3			1000	1111	<d7.	...H								*2
	BLE label	if((VF^NF)|ZF=1),PC+5+d11(label)+H PC if((VF^NF)|ZF=0),PC+5 PC	--	--	--	--	5	2/3			1001	1111	<d11	....	...H							*3
	BGT label	if((VF^NF)|ZF=0),PC+5+d7(label)+H PC if((VF^NF)|ZF=1),PC+5 PC	--	--	--	--	5	3/4			0010	0010	0001	<d7.	...H							*2

*1 d4 sign-extension
*2 d7 sign-extension
*3 d11 sign-extension

MN101C SERIES INSTRUCTION SET

Group	Mnemonic	Operation	Flag VF	Flag NF	Flag CF	Flag ZF	Code Size	Cycle	Re-peat	Exten-sion	Machine Code 1	2	3	4	5	6	7	8	9	10	11	Notes
Bcc	BGT label	if((VF^NF)|ZF=0),PC+6+d11(label)+H PC if((VF^NF)|ZF=1),PC+6 PC	--	--	--	--	6	3/4			0010	0011	0001	<d11	....	...H						*3
	BHI label	if(CFIZF=0),PC+5+d7(label)+H PC if(CFIZF=1), PC+5 PC	--	--	--	--	5	3/4			0010	0010	0010	<d7.	...H							*2
	BHI label	if(CFIZF=0),PC+6+d11(label)+H PC if(CFIZF=1), PC+6 PC	--	--	--	--	6	3/4			0010	0011	0010	<d11	....	...H						*3
	BLS label	if(CFIZF=1),PC+5+d7(label)+H PC if(CFIZF=0), PC+5 PC	--	--	--	--	5	3/4			0010	0010	0011	<d7.	...H							*2
	BLS label	if(CFIZF=1),PC+6+d11(label)+H PC if(CFIZF=0), PC+6 PC	--	--	--	--	6	3/4			0010	0011	0011	<d11	....	...H						*3
	BNC label	if(NF=0),PC+5+d7(label)+H PC if(NF=1),PC+5 PC	--	--	--	--	5	3/4			0010	0010	0100	<d7.	...H							*2
	BNC label	if(NF=0),PC+6+d11(label)+H PC if(NF=1),PC+6 PC	--	--	--	--	6	3/4			0010	0011	0100	<d11	....	...H						*3
	BNS label	if(NF=1),PC+5+d7(label)+H PC if(NF=0),PC+5 PC	--	--	--	--	5	3/4			0010	0010	0101	<d7.	...H							*2
	BNS label	if(NF=1),PC+6+d11(label)+H PC if(NF=0),PC+6 PC	--	--	--	--	6	3/4			0010	0011	0101	<d11	....	...H						*3
	BVC label	if(VF=0),PC+5+d7(label)+H PC if(VF=1),PC+5 PC	--	--	--	--	5	3/4			0010	0010	0110	<d7.	...H							*2
	BVC label	if(VF=0),PC+6+d11(label)+H PC if(VF=1),PC+6 PC	--	--	--	--	6	3/4			0010	0011	0110	<d11	....	...H						*3
	BVS label	if(VF=1),PC+5+d7(label)+H PC if(VF=0),PC+5 PC	--	--	--	--	5	3/4			0010	0010	0111	<d7.	...H							*2
	BVS label	if(VF=1),PC+6+d11(label)+H PC if(VF=0),PC+6 PC	--	--	--	--	6	3/4			0010	0011	0111	<d11	....	...H						*3
	BRA label	PC+3+d4(label)+H PC	--	--	--	--	3	3			1110	111H	<d4>									*1
	BRA label	PC+4+d7(label)+H PC	--	--	--	--	4	3			1000	1001	<d7.	...H								*2
	BRA label	PC+5+d11(label)+H PC	--	--	--	--	5	3			1001	1001	<d11	....	...H							*3
CBEQ	CBEQ imm8,Dm,label	if(Dm=imm8),PC+6+d7(label)+H PC if(Dm≠imm8),PC+6 PC	●	●	●	●	6	3/4			1100	10Dm	<#8.	...>	<d7.	...H						*2
	CBEQ imm8,Dm,label	if(Dm=imm8),PC+8+d11(label)+H PC if(Dm≠imm8),PC+8 PC	●	●	●	●	8	4/5			0010	1100	10Dm	<#8.	...>	<d11	....	...H				*3
	CBEQ imm8,(abs8),label	if(mem8(abs8)=imm8),PC+9+d7(label)+H PC if(mem8(abs8)≠imm8),PC+9 PC	●	●	●	●	9	6/7			0010	1101	1100	<abs	8..>	<#8.	...>	<d7.	...H			*2
	CBEQ imm8,(abs8),label	if(mem8(abs8)=imm8),PC+10+d11(label)+H PC if(mem8(abs8)≠imm8),PC+10 PC	●	●	●	●	10	6/7			0010	1101	1101	<abs	8..>	<#8.	...>	<d11	....	...H		*3
	CBEQ imm8,(abs16),label	if(mem8(abs16)=imm8),PC+11+d7(label)+H PC if(mem8(abs16)≠imm8),PC+11 PC	●	●	●	●	11	7/8			0011	1101	1100	<abs	16..	....	...>	<#8.	...>	<d7.	...H	*2
	CBEQ imm8,(abs16),label	if(mem8(abs16)=imm8),PC+12+d11(label)+H PC if(mem8(abs16)≠imm8),PC+12 PC	●	●	●	●	12	7/8			0011	1101	1101	<abs	16..	....	...>	<#8.	...>	<d11	....	...H *3
CBNE	CBNE imm8,Dm,label	if(Dm≠imm8),PC+6+d7(label)+H PC if(Dm=imm8),PC+6 PC	●	●	●	●	6	3/4			1101	10Dm	<#8.	...>	<d7.	..H>						*2
	CBNE imm8,Dm,label	if(Dm≠imm8),PC+8+d11(label)+H PC if(Dm=imm8),PC+8 PC	●	●	●	●	8	4/5			0010	1101	10Dm	<#8.	...>	<d11	....	...H				*3
	CBNE imm8,(abs8),label	if(mem8(abs8)≠imm8),PC+9+d7(label)+H PC if(mem8(abs8)=imm8),PC+9 PC	●	●	●	●	9	6/7			0010	1101	1110	<abs	8..>	<#8.	...>	<d7.	...H			*2
	CBNE imm8,(abs8),label	if(mem8(abs8)≠imm8),PC+10+d11(label)+H PC if(mem8(abs8)=imm8),PC+10 PC	●	●	●	●	10	6/7			0010	1101	1111	<abs	8..>	<#8.	...>	<d11	....	...H		*3
	CBNE imm8,(abs16),label	if(mem8(abs16)≠imm8),PC+11+d7(label)+H PC if(mem8(abs16)=imm8),PC+11 PC	●	●	●	●	11	7/8			0011	1101	1110	<abs	16..	....	...>	<#8.	...>	<d7.	...H	*2
	CBNE imm8,(abs16),label	if(mem8(abs16)≠imm8),PC+12+d11(label)+H PC if(mem8(abs16)=imm8),PC+12 PC	●	●	●	●	12	7/8			0011	1101	1111	<abs	16..	....	...>	<#8.	...>	<d11	....	...H *3
TBZ	TBZ (abs8)bp,label	if(mem8(abs8)bp=0),PC+7+d7(label)+H PC if(mem8(abs8)bp=1),PC+7 PC	0	●	0	●	7	6/7			0011	0000	0bp.	<abs	8..>	<d7.	...H					*2
	TBZ (abs8)bp,label	if(mem8(abs8)bp=0),PC+8+d11(label)+H PC if(mem8(abs8)bp=1),PC+8 PC	0	●	0	●	8	6/7			0011	0000	1bp.	<abs	8..>	<d11	....	...H				*3

*1 d4 sign-extension
*2 d7 sign-extension
*3 d11 sign-extension

MN101C SERIES INSTRUCTION SET

Group	Mnemonic	Operation	Flag VF	Flag NF	Flag CF	Flag ZF	Code Size	Cycle	Re-peat	Extension	Machine Code 1	2	3	4	5	6	7	8	9	10	11	Notes
TBZ	TBZ (io8)bp,label	if(mem8(IOTOP+io8)bp=0),PC+7+d7(label)+H PC if(mem8(IOTOP+io8)bp=1),PC+7 PC	0	●	0	●	7	6/7			0011	0100	0bp.	<io8 ...>	<d7. ...H							*1
	TBZ (io8)bp,label	if(mem8(IOTOP+io8)bp=0),PC+8+d11(label)+H PC if(mem8(IOTOP+io8)bp=1),PC+8 PC	0	●	0	●	8	6/7			0011	0100	1bp.	<io8 ...>	<d11	...H						*2
	TBZ (abs16)bp,label	if(mem8(abs16)bp=0),PC+9+d7(label)+H PC if(mem8(abs16)bp=1),PC+9 PC	0	●	0	●	9	7/8			0011	1110	0bp.	<abs 16.. ....>	<d7. ...H							*1
	TBZ (abs16)bp,label	if(mem8(abs16)bp=0),PC+10+d11(label)+H PC if(mem8(abs16)bp=1),PC+10 PC	0	●	0	●	10	7/8			0011	1110	1bp.	<abs 16.. ....>	<d11	...H						*2
TBNZ	TBNZ (abs8)bp,label	if(mem8(abs8)bp=1),PC+7+d7(label)+H PC if(mem8(abs8)bp=0),PC+7 PC	0	●	0	●	7	6/7			0011	0001	0bp.	<abs 8..>	<d7. ...H							*1
	TBNZ (abs8)bp,label	if(mem8(abs8)bp=1),PC+8+d11(label)+H PC if(mem8(abs8)bp=0),PC+8 PC	0	●	0	●	8	6/7			0011	0001	1bp.	<abs 8..>	<d11	...H						*2
	TBNZ (io8)bp,label	if(mem8(io)bp=1),PC+7+d7(label)+H PC if(mem8(io)bp=0),PC+7 PC	0	●	0	●	7	6/7			0011	0101	0bp.	<io8 ...>	<d7. ...H							*1
	TBNZ (io8)bp,label	if(mem8(io)bp=1),PC+8+d11(label)+H PC if(mem8(io)bp=0),PC+8 PC	0	●	0	●	8	6/7			0011	0101	1bp.	<io8 ...>	<d11	...H						*2
	TBNZ (abs16)bp,label	if(mem8(abs16)bp=1),PC+9+d7(label)+H PC if(mem8(abs16)bp=0),PC+9 PC	0	●	0	●	9	7/8			0011	1111	0bp.	<abs 16.. ....>	<d7. ...H							*1
	TBNZ (abs16)bp,label	if(mem8(abs16)bp=1),PC+10+d11(label)+H PC if(mem8(abs16)bp=0),PC+10 PC	0	●	0	●	10	7/8			0011	1111	1bp.	<abs 16.. ....>	<d11	...H						*2
JMP	JMP (An)	0 PC.17-16,An PC.15-0,0 PC.H	---	---	---	---	3	4			0010	0001	00A0									
	JMP label	abs18(label)+H PC	---	---	---	---	7	5			0011	1001	0aaH	<abs 18.b	p15~ 0..>							*5
JSR	JSR (An)	SP-3 SP,(PC+3).bp7-0 mem8(SP) (PC+3).bp15-8 mem8(SP+1) (PC+3).H mem8(SP+2).bp7, 0 mem8(SP+2).bp6-2, (PC+3).bp17-16 mem8(SP+2).bp1-0 0 PC.bp17-16 An PC.bp15-0,0 PC.H	---	---	---	---	3	7			0010	0001	00A1									
	JSR label	SP-3 SP,(PC+5).bp7-0 mem8(SP) (PC+5).bp15-8 mem8(SP+1) (PC+5).H mem8(SP+2).bp7, 0 mem8(SP+2).bp6-2, (PC+5).bp17-16 mem8(SP+2).bp1-0 PC+5+d12(label)+H PC	---	---	---	---	5	6			0001	000H	<d12	...>								*3
	JSR label	SP-3 SP,(PC+6).bp7-0 mem8(SP) (PC+6).bp15-8 mem8(SP+1) (PC+6).H mem8(SP+2).bp7, 0 mem8(SP+2).bp6-2, (PC+6).bp17-16 mem8(SP+2).bp1-0 PC+6+d16(label)+H PC	---	---	---	---	6	7			0001	001H	<d16	....	...>							*4
	JSR label	SP-3 SP,(PC+7).bp7-0 mem8(SP) (PC+7).bp15-8 mem8(SP+1) (PC+7).H mem8(SP+2).bp7, 0 mem8(SP+2).bp6-2, (PC+7).bp17-16 mem8(SP+2).bp1-0 abs18(label)+H PC	---	---	---	---	7	8			0011	1001	1aaH	<abs 18.b	p15~ 0..>							*5
	JSRV (tbl4)	SP-3 SP,(PC+3).bp7-0 mem8(SP) (PC+3).bp15-8 mem8(SP+1) (PC+3).H mem8(SP+2).bp7 0 mem8(SP+2).bp6-2, (PC+3).bp17-16 mem8(SP+2).bp1-0 mem8(x'004080+tbl4<<2) PC.bp7-0 mem8(x'004080+tbl4<<2+1) PC.bp15-8 mem8(x'004080+tbl4<<2+2).bp7 PC.H mem8(x'004080+tbl4<<2+2).bp1-0 PC.bp17-16	---	---	---	---	3	9			1111	1110	<t4>									
NOP	NOP	PC+2 PC	---	---	---	---	2	1	○		0000	0000										

*1 d7 sign-extension
*2 d11 sign-extension
*3 d12 sign-extension
*4 d16 sign-extension
*5 aa=abs18.17 - 16

MN101C SERIES INSTRUCTION SET

Group	Mnemonic	Operation	Flag VF	Flag NF	Flag CF	Flag ZF	Code Size	Cycle	Re-peat	Extension	Machine Code 1	2	3	4	5	6	7	8	9	10	11	Notes
RTS	RTS	mem8(SP) (PC).bp7-0 mem8(SP+1) (PC).bp15-8 mem8(SP+2).bp7 (PC).H mem8(SP+2).bp1-0 (PC).bp17-16 SP+3 SP	---	---	---	---	2	7			0000 0001											
RTI	RTI	mem8(SP) PSW mem8(SP+1) (PC).bp7-0 mem8(SP+2) (PC).bp15-8 mem8(SP+3).bp7 (PC).H mem8(SP+3).bp1-0 (PC).bp17-16 mem8(SP+4) HA-l mem8(SP+5) HA-h SP+6 SP	●	●	●	●	2	11			0000 0011											
Contorl instructions																						
REP	REP imm3	imm3-1 RPC	---	---	---	---	3	2			0010 0001 1rep											*1

*1 no repeat whn imm3=0, (rep: imm3-1)

Other than the instruction of MN101C Series,the assembler of this Series has the following instructions as macro instructions.
The assembler will interpret the macro instructions below as the assembler instructions.

macro instructions		replaced instructions		remarks
INC	Dn	ADD	1,Dn	
DEC	Dn	ADD	-1,Dn	
INC	An	ADDW	1,An	
DEC	An	ADDW	-1,An	
INC2	An	ADDW	2,An	
DEC2	An	ADDW	-2,An	
CLR	Dn	SUB	Dn,Dm	n=m
ASL	Dn	ADD	Dn,Dm	n=m
LSL	Dn	ADD	Dn,Dm	n=m
ROL	Dn	ADDC	Dn,Dm	n=m
NEG	Dn	NOT ADD	Dn 1,Dn	
NOPL		MOVW	DWn,DWm	n=m
MOV	(SP),Dn	MOV	(0,SP),Dn	
MOV	Dn,(SP)	MOV	Dn,(0,SP)	
MOVW	(SP),DWn	MOVW	(0,SP),DWn	
MOVW	DWn,(SP)	MOVW	DWn,(0,SP)	
MOVW	(SP),An	MOVW	(0,SP),An	
MOVW	An,(SP)	MOVW	An,(0,SP)	

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17-4 Instruction Map

MN101C SERIES INSTRUCTION MAP

1st nibble\2nd nibble

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	NOP	RTS	MOV #8,(io8)	RTI	CMP #8,(abs8)/(abs12)		POP An		ADD #8,Dm				MOVW #8,DWm		MOVW #8,Am	
1	JSR d12(label)		JSR d16(label)		MOV #8,(abs8)/(abs12)		PUSH An		OR #8,Dm				AND #8,Dm			
2	When the exension code is b'oo10'															
3	When the extension code is b'0011'															
4	MOV (abs12),Dm				MOV (abs8),Dm				MOV (An),Dm							
5	MOV Dn,(abs12)				MOV Dn,(abs8)				MOV Dn,(Am)							
6	MOV (io8),Dm				MOV (d4,SP),Dm				MOV (d8,An),Dm							
7	MOV Dn,(io8)				MOV Dn,(d4,SP)				MOV Dn,(d8,Am)							
8	ADD #4,Dm				SUB Dn,Dn				BGE d7	BRA d7	BEQ d7	BNE d7	BCC d7	BCS d7	BLT d7	BLE d7
9	BEQ d4		BNE d4		MOVW DWn,(HA)		MOVW An,(HA)		BGE d11	BRA d11	BEQ d11	BNE d11	BCC d11	BCS d11	BLT d11	BLE d11
A	MOV Dn,Dm / MOV #8,Dm															
B	BSET (abs8)bp								BCLR (abs8)bp							
C	CMP #8,Dm				MOVW (abs8),Am		MOVW (abs8),DWm		CBEQ #8,Dm,d7				CMPW #16,DWm		MOVW #16,DWm	
D	MOV Dn,(HA)				MOVW An,(abs8)		MOVW DWn,(abs8)		CBNE #8,Dm,d7				CMPW #16,Am		MOVW #16,Am	
E	MOVW (An),DWm				MOVW (d4,SP),Am		MOVW (d4,SP),DWm		POP Dn				ADDW #4,Am		BRA d4	
F	MOVW DWn,(Am)				MOVW An,(d4,SP)		MOVW DWn,(d4,SP)		PUSH Dn				ADDW #8,SP	ADDW #4,SP	JSRV (tbl4)	

Extension code: b'0010'

2nd nible\3rd nibble

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	MOVW An,Am				CMPW An,Am				MOVW SP,Am		MOVW An,SP		BTST #8,Dm			
1	JMP (A0)	JSR (A0)	JMP (A1)	JSR (A1)	MOV PSW,Dm				REP #3							
2		BGT d7	BHI d7	BLS d7	BNC d7	BNS d7	BVC d7	BVS d7	NOT Dn				ROR Dn			
3		BGT d11	BHI d11	BLS d11	BNC d11	BNS d11	BVC d11	BVS d11	ASR Dn				LSR Dn			
4	SUBW DWn,DWm				SUBW #16,DWm		SUBW #16,Am		SUBW DWn,Am				MOVW DWn,Am			
5	ADDW DWn,DWm				ADDW #16,DWm		ADDW #16,Am		ADDW DWn,Am				CMPW DWn,Am			
6	MOV (d16,SP),Dm				MOV (d8,SP),Dm				MOV (d16,An),Dm							
7	MOV Dn,(d16,SP)				MOV Dn,(d8,SP)				MOV Dn,(d16,Am)							
8	MOVW DWn,DWm (NOPL @n=m)				CMPW DWn,DWm				ADDUW Dn,Am							
9	EXT Dn,DWm		AND #8,PSW	OR #8,PSW	MOV Dn,PSW				ADDSW Dn,Am							
A	SUB Dn,Dm / SUB #8,Dm															
B	SUBC Dn,Dm															
C	MOV (abs16),Dm				MOVW (abs16),Am		MOVW (abs16),DWm		CBEQ #8,Dm,d12				MOVW An,DWm			
D	MOV Dn,(abs16)				MOVW An,(abs16)		MOVW DWn,(abs16)		CBNE #8,Dm,d12				CBEQ #8,(abs8),d7/d11		CBNE #8,(abs8),d7/d11	
E	MOVW (d16,SP),Am		MOVW (d16,SP),DWm		MOVW (d8,SP),Am		MOVW (d8,SP),DWm		MOVW (An),Am				ADDW #8,Am		DIVU	
F	MOVW An,(d16,SP)		MOVW DWn,(d16,SP)		MOVW An,(d8,SP)		MOVW DWn,(d8,SP)		MOVW An,(Am)				ADDW #16,SP		MULU	

Extension code: b'0011'

2nd nibble\ 3rd nibble	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	TBZ (abs8)bp,d7								TBZ (abs8)bp,d11							
1	TBNZ (abs8)bp,d7								TBNZ (abs8)bp,d11							
2	CMP Dn,Dm															
3	ADD Dn,Dm															
4	TBZ (io8)bp,d7								TBZ (io8)bp,d11							
5	TBNZ (io8)bp,d7								TBNZ (io8)bp,d11							
6	OR Dn,Dm															
7	AND Dn,Dm															
8	BSET (io8)bp								BCLR (io8)bp							
9	JMP abs18(label)								JSR abs18(label)							
A	XOR Dn,Dm / XOR #8,Dm															
B	ADDC Dn,Dm															
C	BSET (abs16)bp								BCLR (abs16)bp							
D	BTST (abs16)bp								cmp #8,(abs16)	mov #8,(abs16)			CBEQ #8,(abs16),d7/11		CBNE #8,(abs16),d7/11	
E	TBZ (abs16)bp,d7								TBZ (abs16)bp,d11							
F	TBNZ (abs16)bp,d7								TBNZ (abs16)bp,d11							

Ver2.1(2001.03.26)

Chapter 18 Flash EEPROM

18-1 Overview

18-1-1 Overview

The MN101CF77G is equivalent to MN101C77C except its Mask ROM is substituted with 128 KB of flash EEPROM.
Operating voltage of MN101CF77G is as follows.

MN101CF77G Operating voltage: V_{DD}=2.7 V to 3.6 V

Normal operation is guaranteed with up to ten programmings. *1

The MN101CF77G is programmed in one of two modes;
PROM writer mode, which uses a dedicated PROM writer for a microcontroller's stand-alone programming. Onboard programming mode, which the CPU controls programming of a microcontroller on a target board.

The 128 KB flash EEPROM is divided into two main areas.

❒ Load program area (8 KB : X'04000' to X'05FFF')
This area stores a load program for onboard programming mode. This area is overwritten only in PROM writer mode. This area is write/erase-protected in the hardware during onboard programming mode.

❒ User program area (120 KB : X'06000' to X'23FFF')
This area stores an user program. It is overwritten in both programming modes.

***1** 1 cycle of "erase-write" process is counted as 1 programming in every block.
That is, when several blocks are programmed one-time separately, programming count is added by just the number of programming cycle. (For instance, when block 1, 2 and 3 are programmed separately, 3 program count is added.)
Therefore, program several blocks together to reduce the programming count.

If serial interface communication pins (P53, P54, P05 and P03) are in floating state, this Flash EEPROM version may enter the onboard programming mode even when the serial writer is not connected to it (on-board programming mode is not selected).
To avoid this, set the pull-up resistors on the target board, or design the circuit in such a way that the pins are "H" or "L" level even at reset.
If load program is not written to the Flash EEPROM, it does not happen.

Figure 18-1-1 shows a memory map in Internal flash EEPROM.

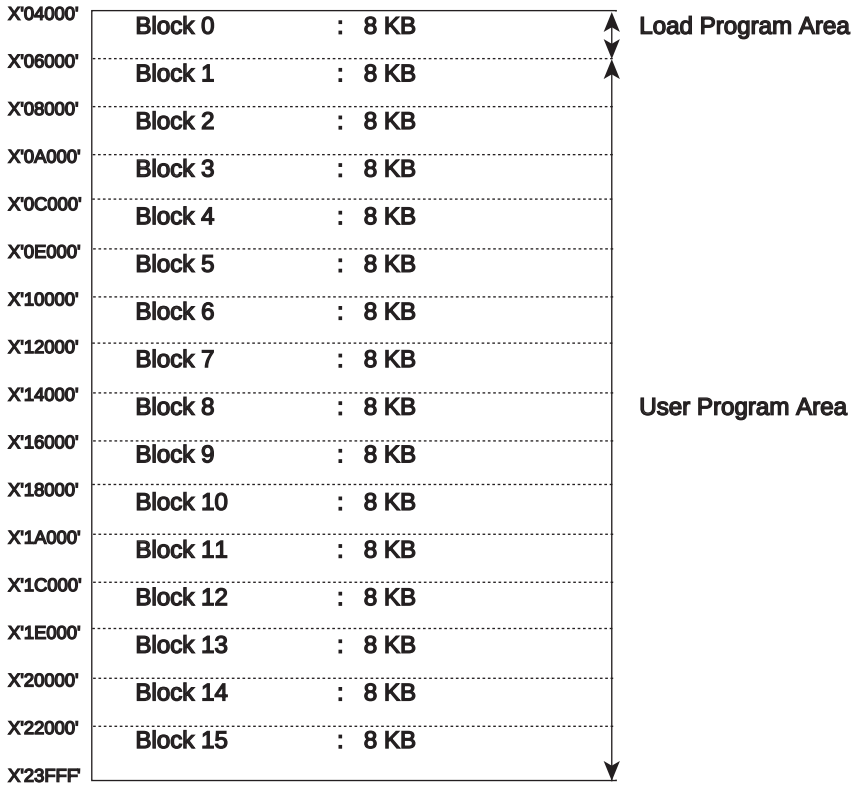

Figure 18-1-1 Memory Map in Internal Flash EEPROM

18-1-2 Differences between Mask ROM version and EPROM version

Table 18-1-1 shows differences between 8-bit microcontroller MN101C77C (Mask ROM version), MN101CF77G (EPROM version).

Table 18-1-1 Differences between Mask ROM version and EPROM version

	MN101C77C (Mask ROM Version)	MN101CF77G (Flash EEPROM Version)
Operating temperature	- 40 °C to +85°C	- 40 °C to +85 °C
Operating Voltage	2.5 V to 3.6 V (100ns / 20MHz) 2.1 V to 3.6 V (200ns / 10MHz) 1.8 V to 3.6 V (500ns / 4MHz)	2.7 V to 3.6 V (100ns / 20MHz)
Pin	Pin No. 5: NC	Pin No. 5: VPP *1
Current consumption	Current consumption of Flash EEPROM versions are larger than that of the Mask ROM versions, as it features voltage boosting. The difference is larger in SLOW and HALT mode.	
Oscillation characteristics	Matching evaluation of each version is necessary when these versions are rotated for mass production.	
Noise characteristics	Noise evaluation of each version is necessary when these versions are rotated for mass production.	

*1 Apply +5 V during Flash EEPROM programming, and apply the same (V_{DD}) potential during other operations.

18-2 Pin Descriptions

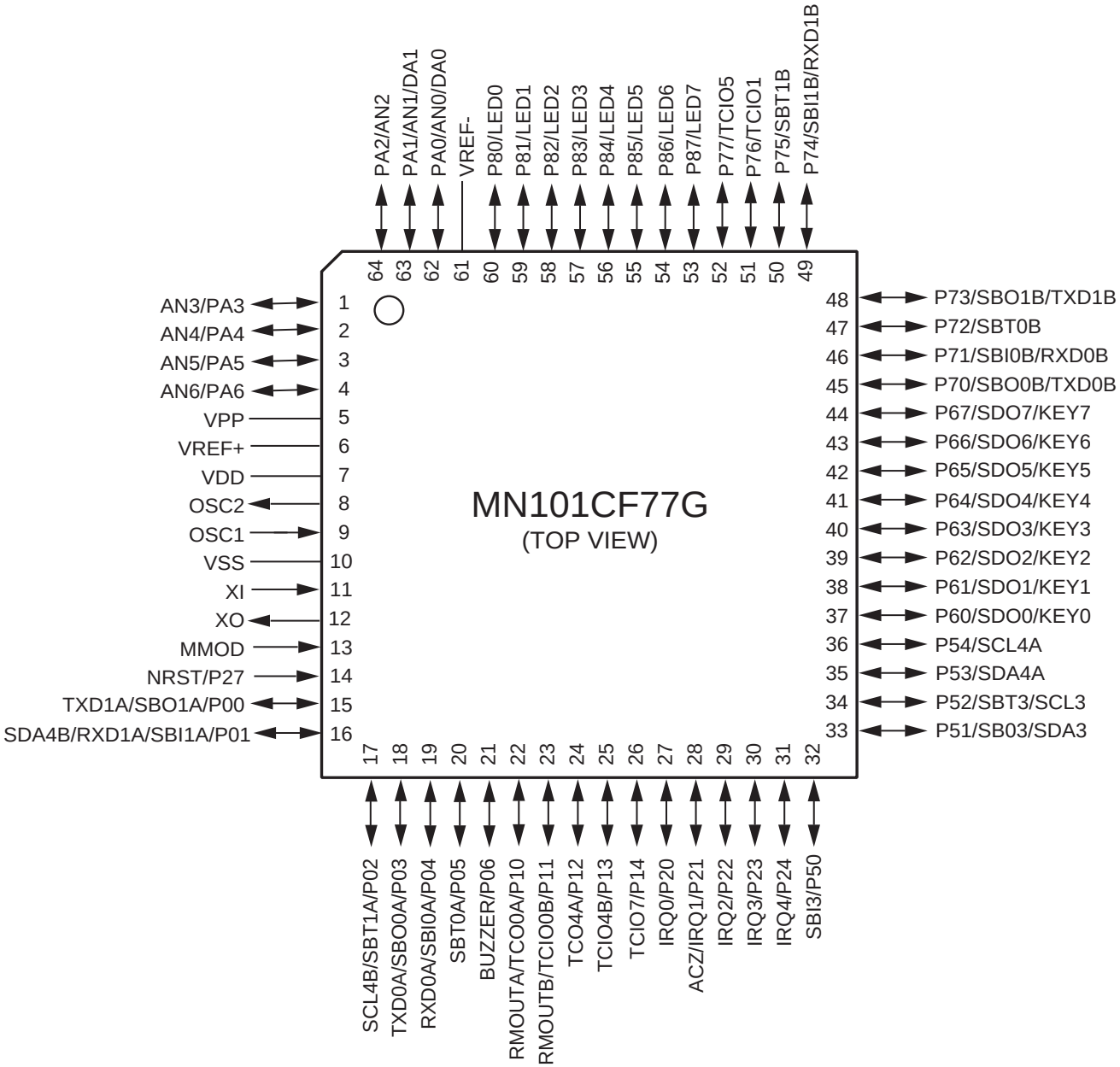

Figure18-2-1 Pin Configuration (LQFP064-P-1414)

18-3 Electrical Characteristics

This LSI user's manual describes the standard specification. Please ask our sales offices for its own product specifications.

Contents \ Model	MN101CF77G
Structure	CMOS integrated circuit
Application	General purpose
Function	CMOS 8-bit single-chip microcontroller

18-3-1 Absolute Maximum Ratings*2,*3

	Parameter		Symbol	Rating	Unit
1	Power supply voltage		V_{DD}	– 0.3 to + 4.6	V
2	Input clamp current (SENS)		IC	– 500 to + 500	µA
3	Input pin voltage		V_I	– 0.3 to V_{DD} +0.3	v
4	Output pin voltage		V_O	– 0.3 to V_{DD} +0.3	
5	I/O pin voltage		V_{IO}	– 0.3 to V_{DD} +0.3	
6	Peak output current	Port 8 *4	I_{OL1} (peak)	30	mA
7		Other than port8	I_{OL2} (peak)	10	
8			I_{OH} (peak)	– 10	
9	Average output current *1	Port 8 *4	I_{OL1} (avg)	20	
10		Other than port8	I_{OL2} (avg)	5	
11			I_{OH} (avg)	– 5	
12	Power dissipation		P_T	300	mW
13	Operating temperature		T_{opr}	– 40 to + 85	°C
14	Storage temperature		T_{stg}	– 40 to + 98	

*1 Applied to any 100 ms period.

*2 Connect at least one bypass capacitor of 0.1 µF or larger between the power supply pin and the ground for latch-up prevention.

*3 The absolute maximum ratings are the limit values beyond which the LSI may be damaged and proper operation is not assured.

*4 Applied when LED is output from P8LED register.

18-3-2 Operating Conditions

[NORMAL mode : fs=fosc/2, SLOW mode : fs=fx/2]

Ta = – 40 °C to + 85 °C V_{DD} = 2.7 V to 3.6 V

Parameter		Symbol	Conditions	Rating			Unit
				MIN	TYP	MAX	
Power supply voltage *1							
1	Power supply voltage	V_{DD1}	fosc=≤20.0 MHz, fs=focs/2 $V_{PP}=V_{DD}$	2.7	-	3.6	V
2		V_{DD2}	fx=≤32.0 kHz, fs=fx/2 $V_{PP}=V_{DD}$	2.7	-	3.6	
3		V_{PP}		-	V_{DD}	-	
4	Voltage to maintain RAM data	V_{DD3}	At STOP mode	2.7	-	3.6	
Operation speed *1							
5	Minimum instruction execution time	t_{c1}	V_{DD}= 2.7 V to 3.6 V, fs=focs/2	0.100	-	125	µs

Ta = – 0 °C to + 50 °C V_{DD} = 2.7 V to 3.6 V

Parameter		Symbol	Conditions	Rating			Unit
				MIN	TYP	MAX	
Programming voltage *2							
6	Flash EEPROM program/erase voltage	V_{DDEW}	During Flash programming	2.7	-	3.6	V
7		V_{PPEW}	During Flash programming	4.8	5	5.2	

*1 $V_{PP}=V_{DD}$ exept during Flash EEPROM program/erase.

*2 Operating tempreture during programming should be within 0 °C to +50 °C .

18-3-3 DC Characteristics

Ta = – 40 °C to + 85 °C V_{DD} = 3.3 V V_{SS} = 0 V

Parameter		Symbol	Conditions	Rating			Unit
				MIN	TYP	MAX	
Power supply current (no load at output pin) *1							
1	Power supply current	I_{DD1}	fosc=20.0 MHz, fs=focs/2 $V_{PP}=V_{DD}$=3.3 V	-	11	24	mA
2		I_{DD2}	fosc=8.39 MHz, fs=focs/2 $V_{PP}=V_{DD}$=3.3 V	-	5.5	11	
3		I_{DD3}	fx=32 kHz, fs=fx/2 $V_{PP}=V_{DD}$=3.3 V	-	100	160	μA
4	Supplu current during HALT1 mode	I_{DD4}	fx=32 kHz, $V_{PP}=V_{DD}$=3.3 V	-	80	160	
5	Supply current during STOP mode	I_{DD5}	$V_{PP}=V_{DD}$=3.3 V Ta= +25 °C	-	0	2	
6		I_{DD6}	$V_{PP}=V_{DD}$=3.3V Ta= -40 °C to +25 °C	-	-	40	

*1 - Measured under conditions of no load, or power down on analog blocks. (Pull-up resistance should be unconnected.)

- The supply current during operation, I_{DD1} (I_{DD2}) are measured under the following conditions :
  After all I/O pins are set to input mode and the oscillation is set to <NORMAL mode>, the MMOD pin is at V_{SS} level, the input pins are at V_{DD} level, and a 20 MHz(8.39 MHz) square wave of V_{DD} and V_{SS} amplitudes is input to the OSC1 pin.
- The supply current during operation, I_{DD3}, is measured under the following conditions :
  After all I/O pins are set to input mode and the oscillation is set to <SLOW mode>, the MMOD pin is at V_{SS} level, the input pins are at V_{DD} level, and a 32 kHz square wave of V_{DD} and V_{SS} amplitudes is input to the XI pin.
- The supply current during HALT mode, I_{DD4}, are measured under the following conditions :
  After all I/O pins are set to input mode and the oscillation is set to <HALT mode>, the MMOD pin is at V_{SS} level, the input pins are at V_{DD} level, and an 32 kHz square wave of V_{DD} and V_{SS} amplitudes is input to the XI pin.
- The supply current during STOP mode, I_{DD5} (I_{DD6}) are measured under the following conditions :
  After the oscillation is set to <STOP mode>, the MMOD pin is at V_{SS} level, the input pins are at V_{DD} level, and the OSC1 and XI pins are unconnected.

18-4 Reprogramming Flow

Figure 18-4-1 shows the flow for reprogramming (erasing and programming) the flash EEPROM. As the figure shows, the User Data Program starts after the memory is erased.

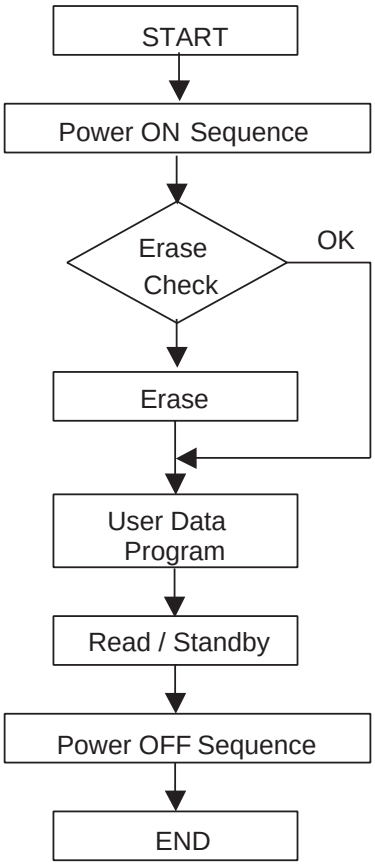

Figure 18-4-1 Reprogramming Flow of Internal Flash EEPROM

Start write routine (User Data Program) only after erase routine is completely finished. However, you can program our product which is already erased without this process. For other products, the erase rouine is necessary, because the erase level may be incompleted even though the test result of "blank check" is "Pass". In such case, reliability of the written data may be damaged even when the write is finished normaly. Also additional write to the address which is already written is forbidden.

18-5 PROM writer mode

In PROM writer mode, the CPU is halted for Internal flash EEPROM to be programed. The microcontroller is inserted into a dedicated adaptor socket, which connects to a PROM writer. When the microcontroller connects to the adaptor socket, it automatically enters PROM writer mode.
For programming using our PanaX Flash writer, you need dedicated adapter socket and gender changer. The P/N are as follows.

Adaptor socket: FLS64LF14-101CF77-3

Matching information of the dedicated writer is posted on our semiconductor website, which is listed on the last page of this manual.

■Fixing a device in the adapter socket and the position of the No.1 pin.

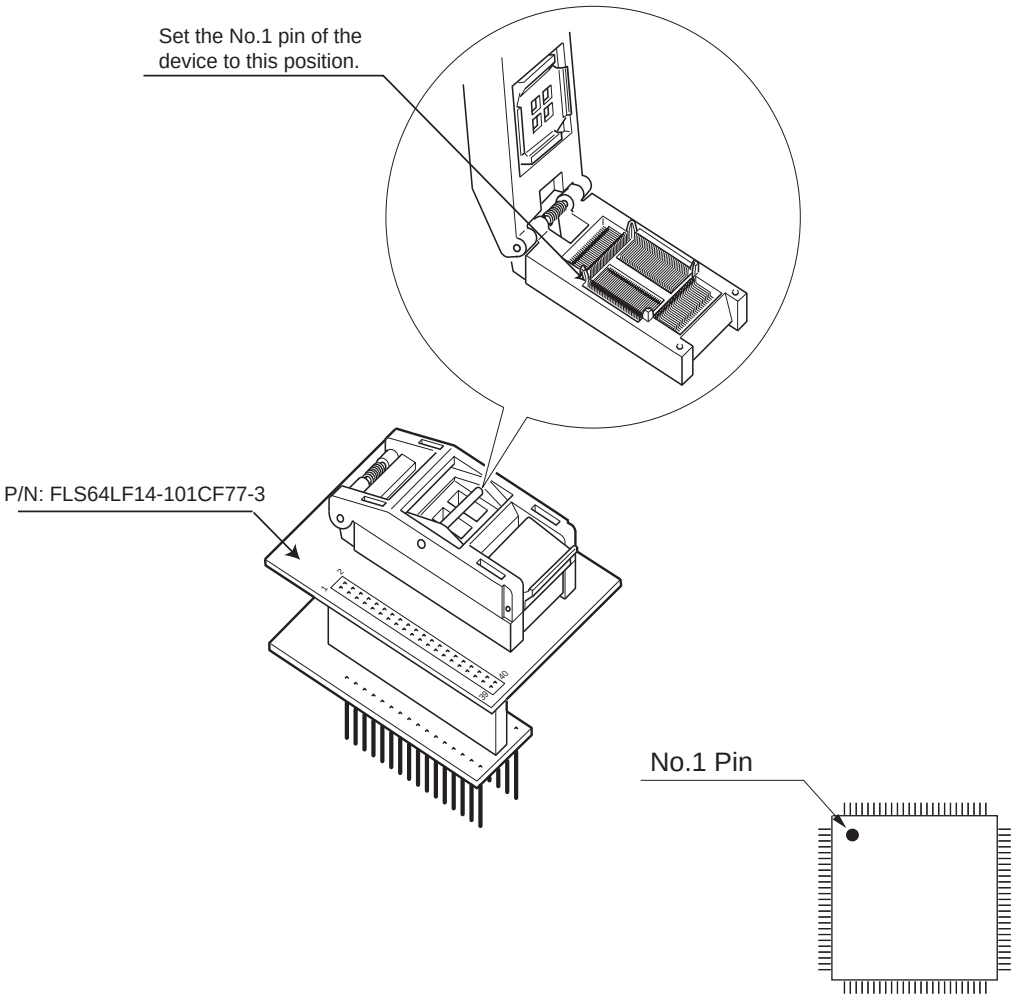

Figure 18-5-1 Fixing a Device on the Adapter Socket and the Position of No.1 Pin

■Pin Configuration for Socket Adaptor

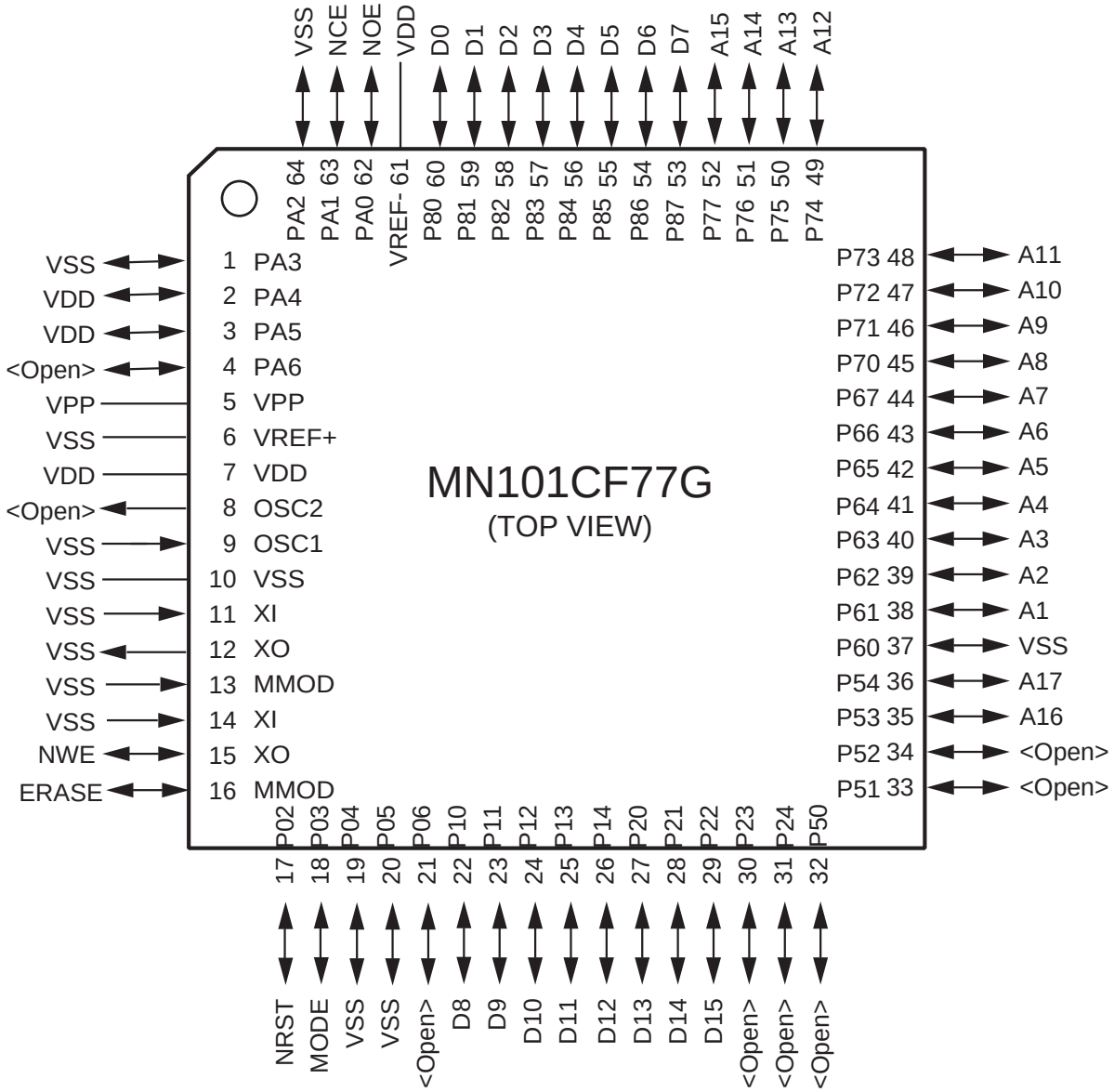

Figure 18-5-2 Pin Configuration for Socket Adaptor

18-6 Onboard Serial Programming Mode

18-6-1 Overview

The onboard serial programming mode is primarily used to program the flash EEPROM in devices that are already installed on a PCB board with internal serial interface.

■Hardware and software requirements
Hardware and software products required for onboard serial programming are as follows.

Hardware requirements
·Onboard serial writer (YDC MODEL: AF200)
·Flash programming connectors or pins for target board.

Software requirements
·Load program installed in the internal flash EEPROM
·Programming algorithm for operating onboard serial writer

■Cautions on onboard serial programming
·Power supply voltage during programming should be within 2.7 V to 3.6 V. If you program outside this limit, reliability of the written data may be damaged.
·Always set the pull-up resistors on the target board so that serial interface communication pins does not become floating state. The pull-up resistors are necessary for the Flash EEPROM not to enter the programming mode when the serial writer is not connected.
·Serial interface I/O pins used for onboard serial programming should be reserved as dedicated pins to prevent other user circuits from communicating with the device. Altenatively, design your target board to be capable of normal communication with serial writer.
· **Install the switch that controlls V_{pp} pin which supplies +5 V during Flash EEPROM programming and supplies same potential (V_{DD}) during other operations.**

18-6-2 Circuit Requirements for the Target Board (in Clock Synchronous Communication using the YDC Serial Writer)

This section describes the circuit requirements for the target board for onboard serial programming with the serial interface 0 using YDC serial writer.

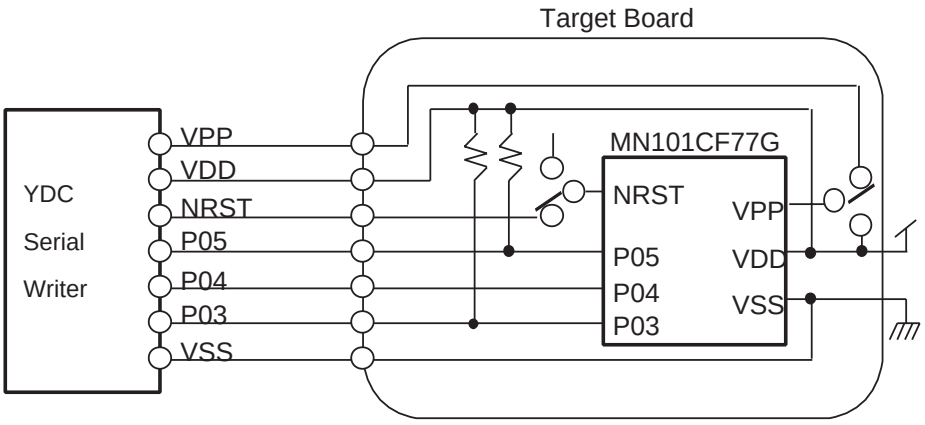

Figure 18-6-1 Target Board for programming using the YDC Serial Writer

Pins

- V_{PP} : 5.0 V power supply (for Flash EEPROM)
- V_{DD} : MN101CF77G: 2.7 V to 3.6 V power supply (for Flash EEPROM and internal circuits)
- NRST : Reset
- P03 : Serial interface 0 data I/O pin (used as SBO0 pin as well)
- P05 : Serial interface 0 clock pin (used as SBT0 pin as well)
- P04 : Busy signal output pin (used as SBI0 as well)
- V_{SS} : Ground

This section describes each memory space of Flash EEPROM.

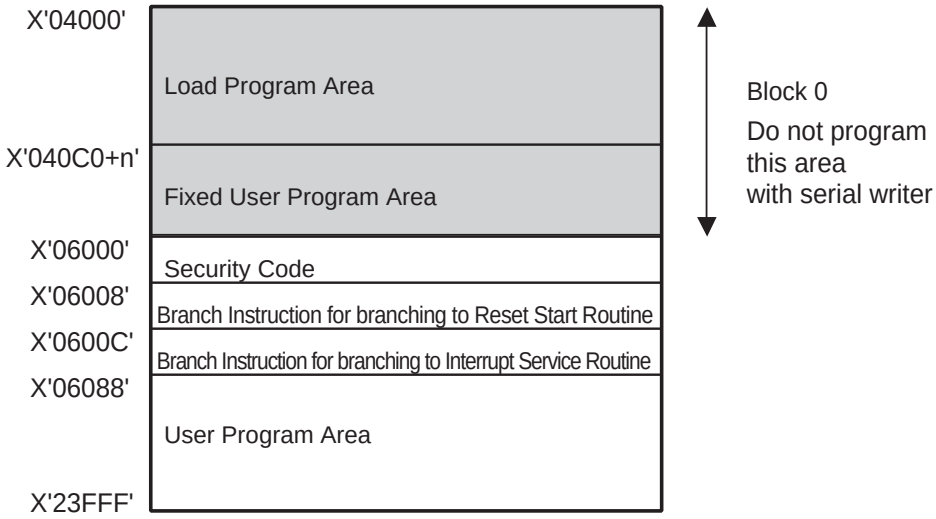

Figure 18-6-2 Flash EEPROM Memory map

*1 Security code can be set to any 8-bit area between x'06000' to x'07FFF'.

・Serial writer load program area (x'04000 to X'040C0+n')

This KB of ROM at address x'04000' to n KB holds the load program for the serial writer.
You need a PROM writer to write/erase this space.

・Fixed user program area (x'040C0+n' to X'05FFF')

This KB of ROM at address x'040C0+n' to X'05FFF' holds the fixed user program.
You need a PROM writer to write/erase this space.

・Security code (x'06000 to X'07FFF')

These bytes holds the password for the serial writer.
The code can be set to any 8-bit area between x'06000' to x'07FFF'.

・Branch instruction to reset service routine (x'06008')

Normally, reset servicing starts at address x'04000', but the soft branch instruction in the serial writer load program branches to x'06008'. This address must hold a JMP instruction pointing to the real start address for the reset service routine.

・Branch instruction to interrupt service routine (x'0600C' to X'06087')

Normally, interrupt servicing starts at address x'04004', but the soft branch instruction in the serial writer load program branches to x'0600C'. This address must hold a JMP instruction pointing to the real start address for the interrupt service routine

x'04004' ⇒ x'0600C', x'04008' ⇒ x'06010', ... x'04078' ⇒ x'06080'

・User program area (x'06088' to X'23FFF')

This area stores the user program.

Use of YDC serial writer

- ·You must write the load program to this LSI before installed in the target board. The load program usually comes with onboard serial writer.
- ·Erase block 0 (load program) is write/erase-protected in the hardware during onboard programming mode.
- ·VPP pin pin must supply 5.0 V from external source.
- ·P05, P03 and P04 pins should be reserved as dedicated pin for serial writer to prevent other user circuits on the target board from communicating with the device. Alternatively, design your target board on which the serial writer can program the device correctly.
- ·Connect pull-up resistors on the target board to P05, P03 and P04 pins, which are connected to the power supply.
- ·NRST and P05 pins are output from the serial writer throgh an open connection.
- ·Install a switch on the target board to toggle between NRST for serial programming and NRST for normal opeation. Alternatively, install a wired-OR connection. (For a wired-OR connection, disable NRST for normal operation during serial programming)

For further information of the onboard serial writer, contact :

YDC Corporation Instrument Business Division Support Center
Phone : 042-333-6245
http://www.ydc.co.jp/micom

18-6-3 Circuit Requirements for the Target Board (in Clock Synchronous Communication using the PanaX Serial Writer)

In programming Flash EEPROM using the PanaX serial writer, you need not to write load program in advance and also be able to use all space of the Flash EEPROM as user program area.
Use P53, P54 for communication with serial writer.
This section describes the circuit requirements for the target board for onboard serial programming in clock synchronous communication using the PanaX Serial Writer.

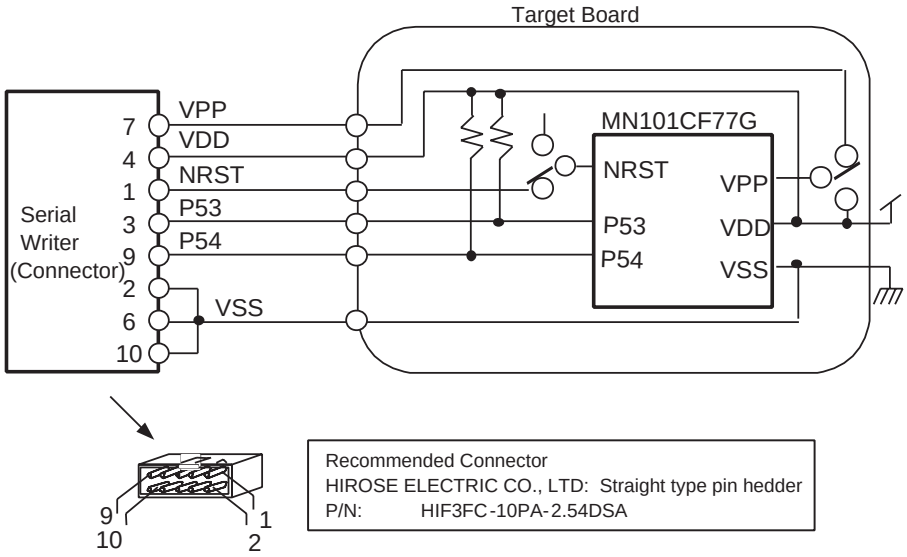

Figure 18-6-3 Target Board for programming using the PanaX Serial Writer

Pins

- V_{PP} : 5.0 V power supply (for Flash EEPROM)
- V_{DD} : MN101CF77G: 2.7 V to 3.6 V power supply (for Flash EEPROM and internal circuits)
- NRST: Reset
- P53 : Data I/O pin for communication
- P54 : Clock input pin for communication
- V_{SS} : Ground

Use of PanaX serial writer (DWIRE programming)

- ·You need not to write load program in advance and also be able to use all space of the Flash EEPROM as user program area.
- ·V_{PP} pin must supply 5.0 V from external power source.
- ·P53 and P54 pins should be reserved as dedicated pins for serial writer to prevent other user circuits on the target board from communicating with the device. Alternatively, design your target board on which the serial writer can program the device correctly.
- ·Connect pull-up resistors on the target board to P53 and P54 pins, which are connected to the power supply.
- ·NRST and SBT2 pins are output from the serial writer through an open connection.
- ·Install a switch on the target board to toggle between NRST for serial programming and NRST for normal opeation. Alternatively, install a wired-OR connection. (For a wired-OR connection, disable NRST for normal operation during serial programming)
- ·You can connect a serial writer easily by setting a 10-wire flat cable on the target board. If a 10-wire flat cable cannot be mounted to the target board, you can solder it directly.
- ·The signal wire lenghth from the serial writer connector to the microcontroller (NRST, P53 and P54) must be shorter than 15 cm.

Selection of circuit device on the target board.

- ·Load capacity of reset signal (NRST)

  Use the oscillation stabilization wait time right after reset in DWIRE programming. That is, rising time from reset must be shorter than 1/3 of the oscillation stabilization wait time.

  Set as:

  Maximun load capacity of reset signal ≤ the value derived from following formula and 100 µF

$$C_{RST} = \frac{\text{Oscillation stabilization wait time}}{3 \times \text{Pull-up resistor value}}$$

- ·Pull-up resistor value (P53, P54)

  Caluculate the resistor value using following formula. When operating voltage is 3.3 V, appropriate value is over 1.65 kΩ.

$$R_{upMin} = \frac{\text{Operating voltage } (V_{DD})}{\text{Maximum output current of pin } (I_{OL})}$$

·To connect resistors in series with communication pins (NRST, P53, P54)

When resistors are connected in series with communication pins, signal spectrum speed drops affected by the load capacity. To ensure effecting reliable communication, the required time in which the operating voltage reaches to 63% of the time constant must be shorter than 1/8 of communication cycle. For example, the maximum resistor value, R_{sMax}, derived from following formula is 208 Ω (at load capacity is 50 pF, communication cycle is12 MHz).

$$R_{sMax} = \frac{1}{8 \times \text{Communication frequency} \times \text{Load capacity}}$$

Large resistors can be connected in series with communication pins by lowering the communication speed. The resistor value should be smaller than 1/10 of the pull-up resistors.

·Open-drain output through writer's communication pin (P53, P54)

During open-drain output through writer's communication pin, signal spectrum speed drops affected by the pull-up resistors and the load capacity. To ensure effecting reliable communication, the required time in which the operating voltage reaches to 63% of the time constant must be shorter than 1/8 of communication cycle. The maximum communication cycle derived from following formula is 1.38 MHz (at load capacity is 50 pF, pull-up resistor is 1.8 kΩ).

$$f_{Max} = \frac{1}{8 \times \text{Pull-up resistor (RupMin)} \times \text{Load capacity}}$$

The communication frequency needs to be lowered for open-drain output, therefore, select push-pull output, if possible.

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