DATA SHEET

UDA1325
Universal Serial Bus (USB) CODEC

Preliminary specification
File under Integrated Circuits, IC01

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Philips
Semiconductors

PHILIPS

Universal Serial Bus (USB) CODEC UDA1325

FEATURES

General

- High Quality USB-compliant Audio/HID device
- Supports 12 Mbits/s serial data transmission
- Fully USB Plug and Play operation
- Supports ‘Bus-powered’ and ‘Self-powered’ operation
- 3.3 V power supply
- Low power consumption with optional efficient power control
- On-chip clock oscillator, only an external crystal is required.

Audio playback channel

- One isochronous output endpoint
- Supports multiple audio data formats (8, 16 and 24 bits)
- Adaptive sample frequency support from 5 to 55 kHz
- One master 20-bit I^2S digital stereo playback output, I^2S and LSB justified serial formats
- One slave 20-bit I^2S digital stereo playback input, I^2S and LSB justified serial formats
- Selectable volume control for left and right channel
- Soft mute control
- Digital bass and treble tone control
- Selectable on-chip digital de-emphasis
- Low total harmonic distortion (typical 90 dB)
- High signal-to-noise ratio (typical 95 dB)
- One stereo Line output.

Audio recording channel

- One isochronous input endpoint
- Supports multiple audio data formats (8, 16 and 24 bits)
- Twelve selectable sample rates (4, 8, 16 or 32 kHz; 5.5125, 11.025, 22.05 or 44.1 kHz; 6, 12, 24 or 48 kHz) via analog PLL (APLL).
- Selectable sample rate between 5 to 55 kHz via a second oscillator (optional)
- One slave 20-bit I^2S digital stereo recording input, I^2S and LSB justified serial formats
- Programmable Gain Amplifier for left and right channel
- Low total harmonic distortion (typical 85 dB)
- High signal-to-noise ratio (typical 90 dB)
- One stereo Line/Microphone input.

USB endpoints

- 2 control endpoints
- 2 interrupt endpoints
- 1 isochronous data sink endpoint
- 1 isochronous data source endpoint.

Document references

- *“USB Specification”*
- *“USB Device Class Definition for Audio Devices”*
- *“Device Class Definition for Human Interface Devices (HID)”*
- *“USB HID Usage Table”*.
- *“USB Common Class Specification”*.

APPLICATIONS

- USB monitors
- USB speakers
- USB microphones
- USB headsets
- USB telephone/answering machines
- USB links in consumer audio devices.

GENERAL DESCRIPTION

The UDA1325 is a single chip stereo USB codec incorporating bitstream converters designed for implementation in USB-compliant audio peripherals and multimedia audio applications. It contains a USB interface, an embedded microcontroller, an Analog-to-Digital Interface (ADIF) and an Asynchronous Digital-to-Analog Converter (ADAC).

The USB interface consists of an analog front-end and a USB processor. The analog front-end transforms the differential USB data into a digital data stream. The USB processor buffers the incoming and outgoing data from the analog front-end and handles all low-level USB protocols. The USB processor selects the relevant data from the universal serial bus, performs an extensive error detection and separates control information and audio information. The control information is made accessible to the microcontroller. At playback, the audio information becomes available at the digital I^2S output of the digital I/O module or is fed directly to the ADAC. At recording, the audio information is delivered by the ADIF or by the digital I^2S input of the I^2S-bus interface.

All I^2S inputs and I^2S outputs support standard I^2S-bus format and the LSB justified serial data format with word lengths of 16, 18 and 20 bits.

Via the digital I/O module with its I^2S input and output, an external DSP can be used for adding extra sound processing features for the audio playback channel.

The microcontroller is responsible for handling the high-level USB protocols, translating the incoming control requests and managing the user interface via general purpose pins and an I^2C-bus.

The ADAC enables the wide and continuous range of playback sampling frequencies. By means of a Sample Frequency Generator (SFG), the ADAC is able to reconstruct the average sample frequency from the incoming audio samples. The ADAC also performs the playback sound processing. The ADAC consists of a FIFO, an unique audio feature processing DSP, the SFG, digital filters, a variable hold register, a Noise Shaper (NS) and a Filter Stream DAC (FSDAC) with line output drivers. The audio information is applied to the ADAC via the USB processor or via the digital I^2S input of the digital I/O module.

The ADIF consists of an Programmable Gain Amplifier (PGA), an Analog-to-Digital Converter (ADC) and a Decimator Filter (DF). An Analog Phase Lock Loop (APLL) or oscillator is used for creating the clock signal of the ADIF. The clock frequency for the ADIF can be controlled via the microcontroller. Several clock frequencies are possible for sampling the analog input signal at different sampling rates.

The wide dynamic range of the bitstream conversion technique used in the UDA1325 for both the playback and recording channel guarantees a high audio sound quality.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
UDA1325PS	SDIP42	plastic shrink dual in-line package; 42 leads (600 mil)	SOT270-1
UDA1325H	QFP64	plastic quad flat package; 64 leads (lead length 1.95 mm); body $14 \times 20 \times 2.8$ mm	SOT319-2

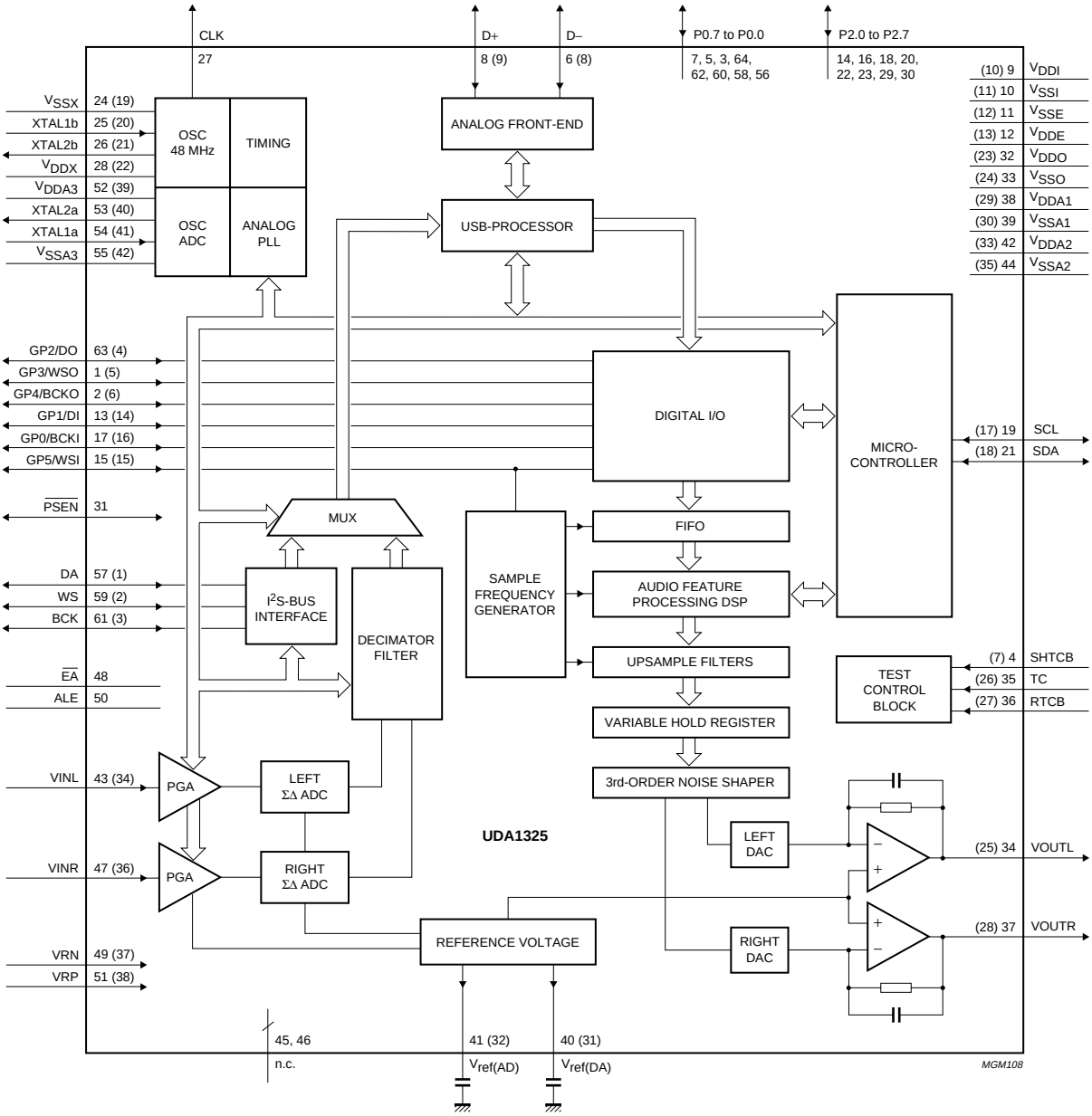
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{DDE}	supply voltage periphery		4.75	5.0	5.25	V
V_{DDI}	supply voltage core		3.0	3.3	3.6	V
$I_{DD(tot)}$	total supply current		–	60	tbf	mA
$I_{DD(tot)(ps)}$	total supply current in power-saving mode	note 1	–	360	–	µA
Dynamic performance DAC						
(THD + N)/S	total harmonic distortion plus noise-to-signal ratio	f_s = 44.1 kHz; R_L = 5 kΩ				
		f_i = 1 kHz (0 dB)	–	–90	–80	dB
			–	0.0032	0.01	%
		f_i = 1 kHz (–60 dB)	–	–30	–20	dB
			–	3.2	10	%
S/N	signal-to-noise ratio at bipolar zero	A-weighted at code 0000H	90	95	–	dBA
$V_{o(FS)(rms)}$	full-scale output voltage (RMS value)	V_{DD} = 3.3 V	–	0.66	–	V
Dynamic performance PGA and ADC						
(THD + N)/S	total harmonic distortion plus noise-to-signal ratio	f_s = 44.1 kHz; PGA gain = 0 dB				
		f_i = 1 kHz; (0 dB); V_i = 1.0 V (RMS)	–	–85	–80	dB
			–	0.0056	0.01	%
		f_i = 1 kHz (–60 dB)	–	–30	–20	dB
			–	3.2	10.0	%
S/N	signal-to-noise ratio	V_i = 0.0 V	90	95	–	dBA
General characteristics						
$f_{i(s)}$	audio input sample frequency		5	–	55	kHz
T_{amb}	operating ambient temperature		0	25	70	°C

Note

1. Exclusive the IDDE current which depends on the components connected to the I/O pins.

BLOCK DIAGRAM



The pin numbers given in parenthesis refer to the SDIP42 version.

Fig.1 Block diagram (QFP64 package).

PINNING

SYMBOL	PIN QFP64	PIN SDIP42	I/O	DESCRIPTION
GP3/WSO	1	5	I/O	general purpose pin 3 or word select output
GP4/BCKO	2	6	I/O	general purpose pin 4 or bit clock output
P0.5	3	–	I/O	Port 0.5 of the microcontroller
SHTCB	4	7	I	shift clock of the test control block (active HIGH)
P0.6	5	–	I/O	Port 0.6 of the microcontroller
D–	6	8	I/O	negative data line of the differential data bus, conforms to the USB standard
P0.7	7	–	I/O	Port 0.7 of the microcontroller
D+	8	9	I/O	positive data line of the differential data bus, conforms to the USB standard
V_{DDI}	9	10	–	digital supply voltage for core
V_{SSI}	10	11	–	digital ground for core
V_{SSE}	11	12	–	digital ground for I/O pads
V_{DDE}	12	13	–	digital supply voltage for I/O pads
GP1/DI	13	14	I/O	general purpose pin 1 or data input
P2.0	14	–	I/O	Port 2.0 of the microcontroller
GP5/WSI	15	15	I/O	general purpose pin 5 or word select input
P2.1	16	–	I/O	Port 2.1 of the microcontroller
GP0/BCKI	17	16	I/O	general purpose pin 0 or bit clock input
P2.2	18	–	I/O	Port 2.2 of the microcontroller
SCL	19	17	I/O	serial clock line I^2C-bus
P2.3	20	–	I/O	Port 2.3 of the microcontroller
SDA	21	18	I/O	serial data line I^2C-bus
P2.4	22	–	I/O	Port 2.4 of the microcontroller
P2.5	23	–	I/O	Port 2.5 of the microcontroller
V_{SSX}	24	19	–	crystal oscillator ground (48 MHz)
XTAL1b	25	20	I	crystal input (analog; 48 MHz)
XTAL2b	26	21	O	crystal output (analog; 48 MHz)
CLK	27	–	O	48 MHz clock output signal
V_{DDX}	28	22	–	supply crystal oscillator (48 MHz)
P2.6	29	–	I/O	Port 2.6 of the microcontroller
P2.7	30	–	I/O	Port 2.7 of the microcontroller
$\overline{PSEN}$	31	–	I/O	program store enable (active LOW)
V_{DDO}	32	23	–	supply voltage for operational amplifier
V_{SSO}	33	24	–	operational amplifier ground
VOUTL	34	25	O	voltage output left channel
TC	35	26	I	test control input (active HIGH)
RTCB	36	27	I	asynchronous reset input of the test control block (active HIGH)
VOUTR	37	28	O	voltage output right channel

SYMBOL	PIN QFP64	PIN SDIP42	I/O	DESCRIPTION
V_{DDA1}	38	29	–	analog supply voltage 1
V_{SSA1}	39	30	–	analog ground 1
$V_{ref(DA)}$	40	31	O	reference voltage output DAC
$V_{ref(AD)}$	41	32	O	reference voltage output ADC
V_{DDA2}	42	33	–	analog supply voltage 2
VINL	43	34	I	input signal left channel PGA
V_{SSA2}	44	35	–	analog ground 2
n.c.	45	–	–	not connected
n.c.	46	–	–	not connected
VINR	47	36	I	input signal right channel PGA
$\overline{EA}$	48	–	–	external access (active LOW)
VRN	49	37	I	negative reference input voltage ADC
ALE	50	–	–	address latch enable (active HIGH)
VRP	51	38	I	positive reference input voltage ADC
V_{DDA3}	52	39	–	supply voltage for crystal oscillator and analog PLL
XTAL2a	53	40	O	crystal output (analog; ADC)
XTAL1a	54	41	I	crystal input (analog; ADC)
V_{SSA3}	55	42	–	crystal oscillator and analog PLL ground
P0.0	56	–	I/O	Port 0.0 of the microcontroller
DA	57	1	I	data Input (digital)
P0.1	58	–	I/O	Port 0.1 of the microcontroller
WS	59	2	I	word select Input (digital)
P0.2	60	–	I/O	Port 0.2 of the microcontroller
BCK	61	3	I	bit clock Input (digital)
P0.3	62	–	I/O	Port 0.3 of the microcontroller
GP2/DO	63	4	I/O	general purpose pin 2 or data output
P0.4	64	–	I/O	Port 0.4 of the microcontroller

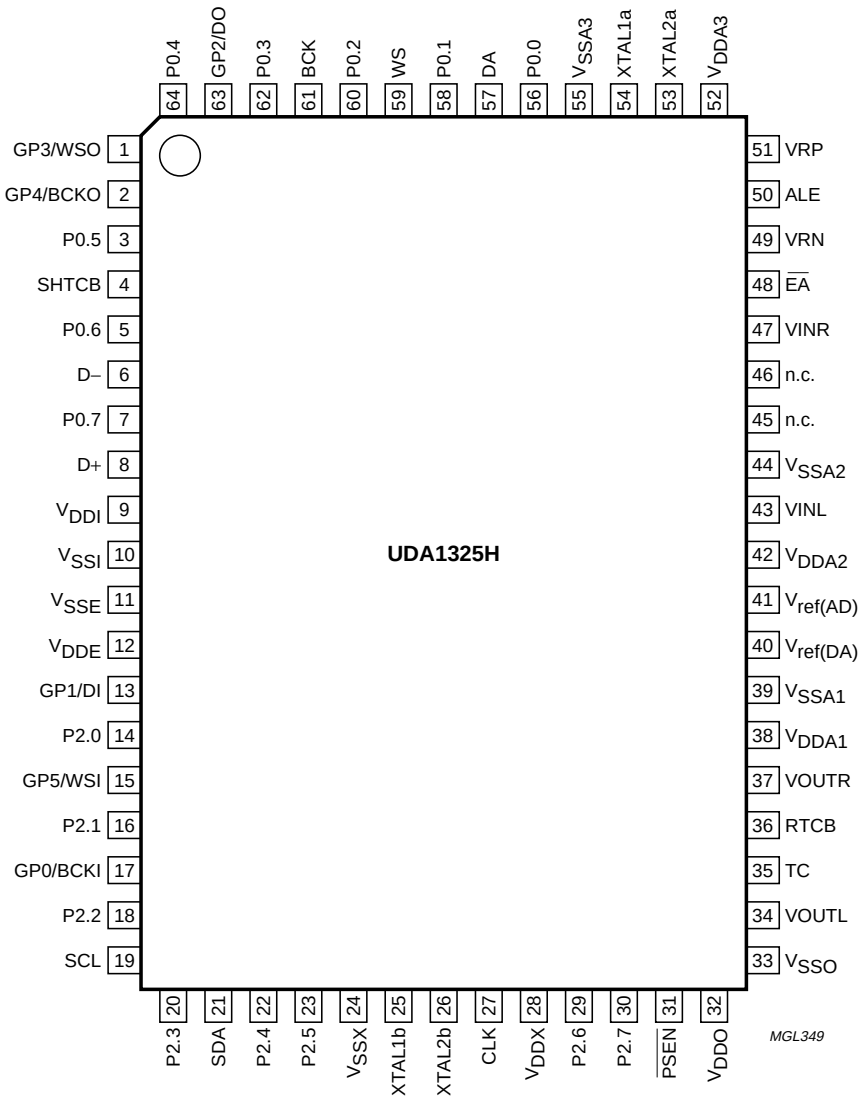


Fig.2 Pin configuration (QFP64 package).

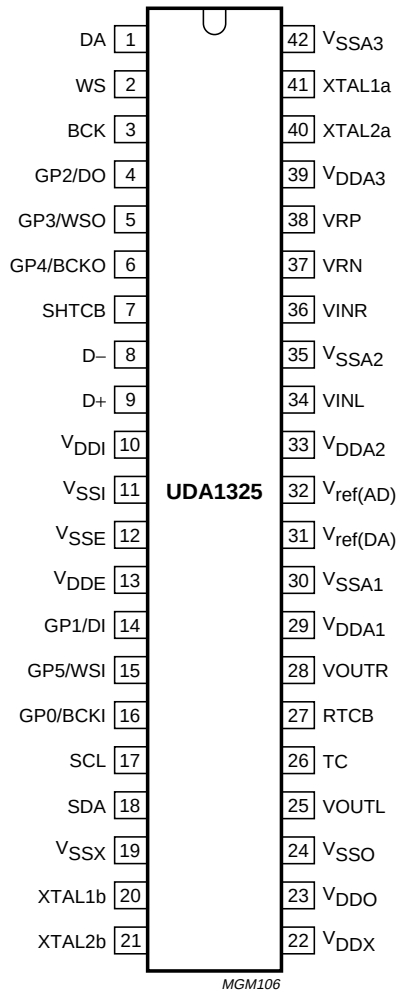


Fig.3 Pin configuration (SDIP42 package).

FUNCTIONAL DESCRIPTION

The Universal Serial Bus (USB)

Data and power is transferred via the USB over a 4-wire cable. The signalling occurs over two wires and point-to-point segments. The signals on each segment are differentially driven into a cable of 90 Ω intrinsic impedance. The differential receiver features input sensitivity of at least 200 mV and sufficient common mode rejection.

The analog front-end

The analog front-end is an on-chip generic USB transceiver. It is designed to allow voltage levels up to V_{DD} from standard or programmable logic to interface with the physical layer of the USB. It is capable of receiving and transmitting serial data at full speed (12 Mbits/s).

The USB processor

The USB processor forms the interface between the analog front-end, the ADIF, the ADAC and the microcontroller. The USB processor consists of:

- A bit clock recovery circuit
- The Philips Serial Interface Engine (PSIE)
- The Memory Management Unit (MMU)
- The Audio Sample Redistribution (ASR) module.

Bit clock recovery

The bit clock recovery circuit recovers the clock from the incoming USB data stream using four times over-sampling principle. It is able to track jitter and frequency drift specified by the USB specification.

Philips Serial Interface Engine (PSIE)

The Philips SIE implements the full USB protocol layer. It translates the electrical USB signals into data bytes and control signals. Depending upon the USB device address and the USB endpoint address, the USB data is directed to the correct endpoint buffer. The data transfer could be of bulk, isochronous, control or interrupt type.

The functions of the PSIE include: synchronization pattern recognition, parallel/serial conversion, bit stuffing/de-stuffing, CRC checking/generation, PID verification/generation, address recognition and handshake evaluation/generation.

The amount of bytes/packet on all endpoints is limited by the PSIE hardware to 8 bytes/packet, except for both isochronous endpoints (336 bytes/packet).

Memory Management Unit (MMU) and integrated RAM

The MMU and integrated RAM handle the temporary data storage of all USB packets that are received or sent over the bus.

The MMU and integrated RAM handle the differences between data rate of the USB and the application allowing the microcontroller to read and write USB packets at its own speed.

The audio data is transferred via an isochronous data sink endpoint or source endpoint and is stored directly into the RAM. Consequently, no handshaking mechanism is used.

Audio Sample Redistribution (ASR)

The ASR reads the audio samples from the MMU and integrated RAM and distributes these samples equidistant over a 1 ms frame period. The distributed audio samples are translated by the digital I/O module to standard I^2S-bus format or 16, 18 or 20 bits LSB-justified I^2S-bus format. The ASR generates the bit clock output (BCKO) and the Word Select Output signal (WSO) of the I^2S output.

The 80C51 microcontroller

The microcontroller receives the control information selected from the USB by the USB processor. It can be used for handling the high-level USB protocols and the user interfaces. The microcontroller does not handle the audio stream.

The major task of the software process that is mapped upon the microcontroller, is to control the different modules of the UDA1325 in such a way that it behaves as a USB device.

The embedded 80C51 microcontroller is compatible with the 80C51 family of microcontrollers described in the 80C51 family single-chip 8-bit microcontrollers of “Data Handbook IC20”, which should be read in conjunction with this data sheet.

The internal ROM size is 12 kbyte. The internal RAM size is 256 byte. A Watchdog Timer is not integrated.

The Analog-to-Digital Interface (ADIF)

The ADIF is used for sampling an analog input signal from a microphone or line input and sending the audio samples to the USB interface. The ADIF consists of a stereo Programmable Gain Amplifier (PGA), a stereo Analog-to-Digital Converter (ADC) and Decimation Filters (DFs). The sample frequency of the ADC is determined by the ADC clock (see Section “The clock source of the analog-to-digital interface”). The user can also select a digital serial input instead of an analog input. In this event the sample frequency is determined by the continuous WS clock with a range between 5 to 55 kHz. Digital serial input is possible with four formats (I^2S-bus, 16, 18 or 20 bits LSB-justified).

Programmable Gain Amplifier circuit (PGA)

This circuit can be used for a microphone or line input. The input audio signals can be amplified by seven different gains (–3 dB, 0 dB, 3 dB, 9 dB, 15 dB, 21 dB and 27 dB).

The gain settings are given in Table 17.

The Analog-to-Digital Converter (ADC)

The stereo ADC of the UDA1325 consists of two 3rd-order Sigma-Delta modulators. They have a modified Ritchie-coder architecture in a differential switched capacitor implementation. The oversampling ratio is 128. Both ADCs can be switched off in power saving mode (left and right separate). The ADC clock is generated by the analog PLL or the ADC oscillator.

The Decimation Filter (DF)

The decimator filter converts the audio data from $128f_s$ down to $1f_s$ with a word width of 8, 16 or 24 bits. This data can be transmitted over the USB as mono or stereo in 1, 2 or 3 bytes/sample. The decimator filters are clocked by the ADC clock.

The clock source of the analog-to-digital interface

The clock source of the ADIF is the analog PLL or the ADC oscillator. The preferred clock source can be selected. The ADC clock used for the ADC and decimation filters is obtained by dividing the clock signal coming from the analog PLL or from the ADC oscillator by a factor Q.

Using the analog PLL the user can select 3 basic APLL clock frequencies (see Table 1).

By connecting the appropriate crystal the user can choose any clock signal between 8.192 and 14.08 MHz via the ADC oscillator.

Table 1 The analog PLL clock output frequencies

FCODE (1 AND 0)	APLL CLOCK FREQUENCY (MHz)
00	11.2896
01	8.1920
10	12.2880
11	11.2896

The dividing factor Q can be selected via the microcontroller. With this dividing factor Q the user can select a range of ADC clock signals allowing several different sample frequencies (see Table 2).

Table 2 ADC clock frequencies and sample frequencies based upon using the APLL as a clock source

APLL CLOCK FREQUENCY (MHz)	DIVIDE FACTOR Q	ADC CLOCK FREQUENCY (MHz)	SAMPLE FREQUENCY (kHz)
8.1920	1	4.096	32
	2	2.048	16
	4	1.024	8
	8	0.512 (not supported)	4 (not supported)
11.2896	1	5.6448	44.1
	2	2.8224	22.05
	4	1.4112	11.025
	8	0.7056	5.5125
12.2880	1	6.144	48
	2	3.072	24
	4	1.536	12
	8	0.768	6

Table 3 ADC clock frequencies and sample frequencies based upon using the OSCAD as a clock source

OSCAD CLOCK FREQUENCY (MHz)	DIVIDE FACTOR Q	ADC CLOCK FREQUENCY (MHz)	SAMPLE FREQUENCY (kHz)
f_{osc}[1]	Q[2]	$f_{osc}/(2Q)$	$f_{osc}/(256Q)$[3]

Notes

1. The oscillator frequency (and therefore the crystal) of OSCAD must be between 8.192 and 14.08 MHz.
2. The Q factor can be 1, 2, 4 or 8.
3. Sample frequencies below 5 kHz and above 55 kHz are not supported.

The Asynchronous Digital-to-Analog Converter (ADAC)

The ADAC receives audio data from the USB processor or from the digital I/O-bus. The ADAC is able to reconstruct the sample clock from the rate at which the audio samples arrive and handles the audio sound processing. After the processing, the audio signal is upsampled, noise-shaped and converted to analog output voltages capable of driving a line output.

The ADAC consists of:

- A Sample Frequency Generator (SFG)
- FIFO registers
- An audio feature processing DSP
- Two digital upsampling filters and a variable hold register
- A digital Noise Shaper (NS)
- A Filter Stream DAC (FSDAC) with integrated filter and line output drivers.

The Sample Frequency Generator (SFG)

The SFG controls the timing signals for the asynchronous digital-to-analog conversion. By means of a digital PLL, the SFG automatically recovers the applied sampling frequency and generates the accurate timing signals for the audio feature processing DSP and the upsampling filters.

The lock time of the digital PLL can be chosen (see Table 8). While the digital PLL is not in lock, the ADAC is muted. As soon as the digital PLL is in lock, the mute is released as described in Section “Soft mute control”.

First-In First-Out (FIFO) registers

The FIFO registers are used to store the audio samples temporarily coming from the USB processor or from the digital I/O input. The use of a FIFO (in conjunction with the SFG) is necessary to remove all jitter present on the incoming audio signal.

The sound processing DSP

A DSP processes the sound features. The control and mapping of the sound features is explained in Section “Controlling the playback features of the ADAC”. Depending on the sampling rate (f_s) the DSP knows four frequency domains in which the treble and bass are regulated. The domain is chosen automatically.

Table 4 Frequency domains for audio processing by the DSP

DOMAIN	SAMPLE FREQUENCY (kHz)
1	5 to 12
2	12 to 25
3	25 to 40
4	40 to 55

The upsampling filters and variable hold function

After the audio feature processing DSP two upsampling filters and a variable hold function increase the oversampling rate to $128f_s$.

The noise shaper

A 3rd-order noise shaper converts the oversampled data to a noise-shaped bitstream for the FSDAC. The in-band quantization noise is shifted to frequencies well above the audio band.

The Filter Stream DAC (FSDAC)

The FSDAC is a semi-digital reconstruction filter that converts the 1-bit data stream of the noise shaper to an analog output voltage. The filter coefficients are implemented as current sources and are summed at virtual ground of the output operational amplifier. In this way very high signal-to-noise performance and low clock jitter sensitivity is achieved. A post filter is not needed because of the inherent filter function of the DAC. On-board amplifiers convert the FSDAC output current to an output voltage signal capable of driving a line output.

USB ENDPOINT DESCRIPTION

The UDA1325 has following six endpoints:

- USB control endpoint 0
- USB control endpoint 1
- USB status interrupt endpoint 1
- USB status interrupt endpoint 2
- Isochronous data sink endpoint
- Isochronous data source endpoint.

Table 5 Endpoint description

ENDPOINT NUMBER	ENDPOINT INDEX	ENDPOINT TYPE	DIRECTION	MAX. PACKET SIZE (BYTES)
0	0	control (default)	out	8
	1		in	8
1	2	control	out	8
	3		in	8
2	4	interrupt	in	8
3	5	interrupt	in	8
4	6	isochronous out	out	336
5	7	isochronous in	in	336

CONTROLLING THE PLAYBACK FEATURES

Controlling the playback features of the ADAC

The exchange of control information between the microcontroller and the ADAC is accomplished through a serial hardware interface comprising the following pins:

L3_DATA: microcontroller interface data line

L3_MODE: microcontroller interface mode line

L3_CLK: microcontroller interface clock line.

See also the description of Port 3 of the 80C51 microcontroller.

Information transfer through the microcontroller bus is organized in accordance with the so-called ‘L3’ format, in which two different modes of operation can be distinguished; address mode and data transfer mode.

The address mode is required to select a device communicating via the L3-bus and to define the destination registers for the data transfer mode. Data transfer for the UDA1325 can only be in one direction, from microcontroller to ADAC to program its sound processing features and other functional features.

ADDRESS MODE

The address mode is used to select a device (in this case the ADAC) for subsequent data transfer and to define the destination registers. The address mode is characterized by L3_MODE being LOW and a burst of 8 pulses on L3_CLK, accompanied by 8 data bits on L3_DATA. Data bits 0 and 1 indicate the type of the subsequent data transfer as shown in Table 6.

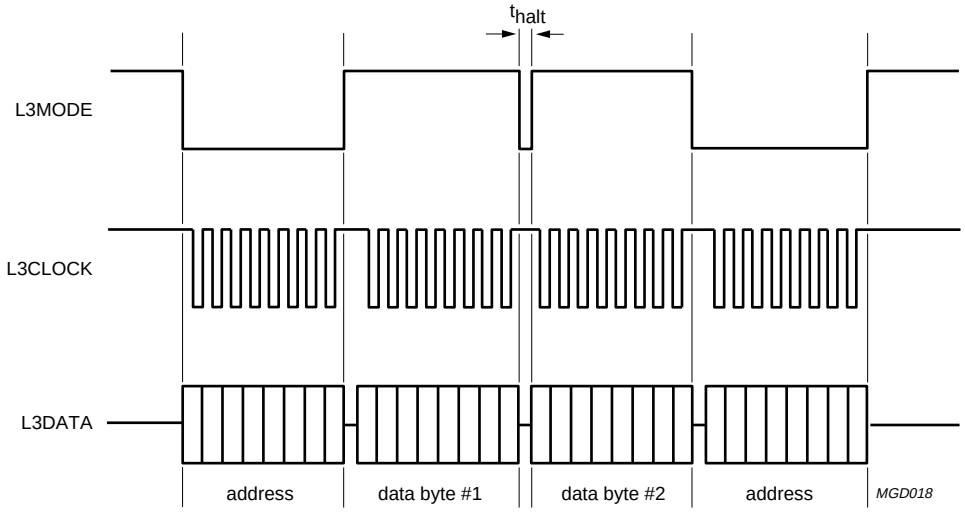
Table 6 Selection of data transfer type

BIT1	BIT0	DATA TRANSFER TYPE
0	0	audio feature registers (volume left, volume right, bass and treble)
0	1	not used
1	0	control registers
1	1	not used

Data bits 7 to 2 represent a 6-bit device address, with bit 7 being the MSB and bit 2 the LSB. The address of the ADAC is 000101 (bits 7 to 2). In the event that the ADAC receives a different address, it will deselect its microcontroller interface logic.

DATA TRANSFER MODE

The selection preformed in the address mode remains active during subsequent data transfers, until the ADAC receives a new address command. The data transfer mode is characterized by L3_MODE being HIGH and a burst of 8 pulses on L3_CLK, accompanied by 8 data bits. All transfers are bitwise, i.e. they are based on groups of 8 bits. Data will be stored in the ADAC after the eight bit of a byte has been received. The principle of a multibyte transfer is illustrated in the figure below.



PROGRAMMING THE SOUND PROCESSING AND OTHER FEATURES

The sound processing and other feature values are stored in independent registers. The first selection of the registers is achieved by the choice of data transfer type. This is performed in the address mode, bits 1 and 0 (see Table 6).
The second selection is performed by bit 7 and/or bit 6 of the data byte depending of the selected data transfer type.

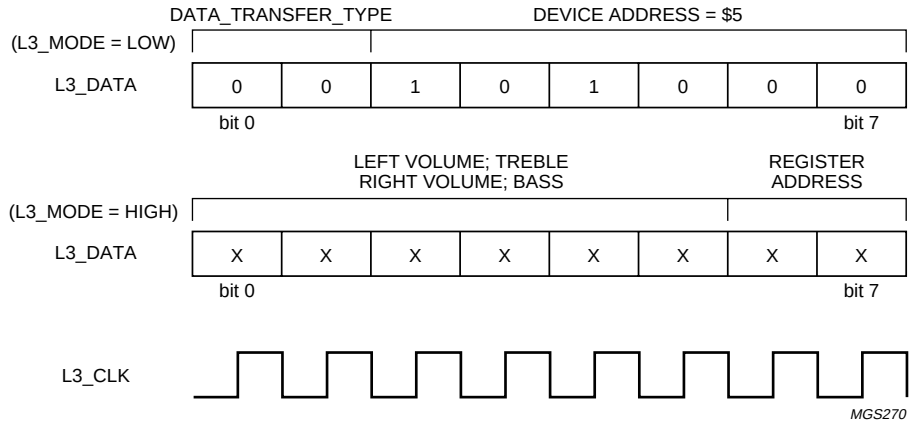
Data transfer type 'audio feature registers'

When the data transfer type 'audio feature registers' is selected 4 audio feature registers can be selected depending on bits 7 and 6 of the data byte (see Table 7).

Table 7 ADAC audio feature registers

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0	REGISTER
0	0	VR5	VR4	VR3	VR2	VR1	VR0	volume right
0	1	VL5	VL4	VL3	VL2	VL1	VL0	volume left
1	0	X	BB4	BB3	BB2	BB1	BB0	bass
1	1	X	TR4	TR3	TR2	TR1	TR0	treble

The sequence for controlling the ADAC audio feature registers via the L3-bus is given in the figure below.



Data transfer type 'control registers'

When the data transfer type 'control registers' is selected 2 general control registers can be selected depending on bit 7 of the data byte (see Table 7).

The sequence for controlling the ADAC control registers via the L3-bus is given in the figure below.

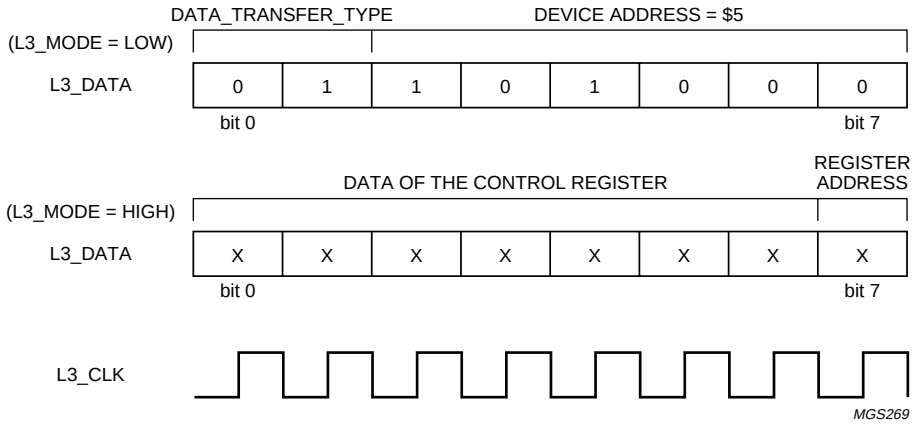


Table 8 ADAC general control registers

REGISTER	BIT	DESCRIPTION	VALUE	COMMENT
Control register 0	0	reset ADAC	0 = not reset 1 = reset	
	1	soft mute control	0 = not muted 1 = mutes	
	2	synchronous/asynchronous	0 = asynchronous 1 = synchronous	select 0
	3	channel manipulation	0 = L -> L, R -> R 1 = L -> R, R -> L	
	4	de-emphasis	0 = de-emphasis off 1 = de-emphasis on	
	6 and 5	audio mode	00 = flat mode 01 = min. mode 10 = min. mode 11 = max. mode	
	7	selecting bit	0	
Control register 1	1 and 0	serial I^2S-bus input format	00 = I^2S-bus 01 = 16-bit LSB justified 10 = 18-bit LSB justified 11 = 20-bit LSB justified	
	3 and 2	digital PLL mode	00 = adaptive 01 = fix state 1 10 = fix state 2 11 = fix state 3	select 00
	4	digital PLL lock mode	0 = adaptive 1 = fixed	select 1
	6 and 5	digital PLL lock speed	00 = lock after 512 samples 01 = lock after 2048 samples 10 = lock after 4096 samples 11 = lock after 16348 samples	select 00
	7	selecting bit	1	

Soft mute control

When the mute (bit 1 of control register 0) is active for the playback channel, the value of the sample is decreased smoothly to zero following a raised cosine curve. There are 32 coefficients used to step down the value of the data, each one being used 32 times before stepping to the next. This amounts to a mute transition of 23 ms at f_s = 44.1 kHz. When the mute is released, the samples are returned to the full level again following a raised cosine curve with the same coefficients being used in reversed order.

The mute, on the master channel is synchronized to the sample clock, so that operation always takes place on complete samples.

Volume control

The volume of the UDA1325 can be controlled from 0 dB down to –60 dB (in steps of 1 dB). Below –60 dB the audio signal is muted (–∞ dB). The setting of 0 dB is always referenced to the maximum available volume setting. Independant volume control of the left and right channel is possible (balance control).

Table 9 Volume settings right playback channel

VR5	VR4	VR3	VR2	VR1	VR0	VOLUME (dB)
0	0	0	0	0	0	0
0	0	0	0	0	1	0
0	0	0	0	1	0	–1
0	0	0	0	1	1	–2
0	0	0	1	0	0	–3
...	...	...	...	...	...	...
1	1	1	1	0	0	–59
1	1	1	1	0	1	–60
1	1	1	1	1	0	–∞
1	1	1	1	1	1	–∞

Table 10 Volume settings left playback channel

VL5	VL4	VL3	VL2	VL1	VL0	VOLUME (dB)
0	0	0	0	0	0	0
0	0	0	0	0	1	0
0	0	0	0	1	0	–1
0	0	0	0	1	1	–2
0	0	0	1	0	0	–3
...	...	...	...	...	...	...
1	1	1	1	0	0	–59
1	1	1	1	0	1	–60
1	1	1	1	1	0	–∞
1	1	1	1	1	1	–∞

Treble control

For the playback channel, treble can be regulated in three audio modes: minimum, flat and maximum mode. In flat mode the audio is not influenced. In minimum and maximum mode, the treble range is from 0 to 6 dB in steps of 2 dB. The programmable treble filter is implemented digitally and has a fixed corner frequency of 3000 Hz for the minimum mode and 1500 Hz for the maximum mode. Because of the exceptional amount of programmable gain, treble should be used with adequate prior attenuation, using volume control.

Table 11 Treble settings

TR4	TR3	TR2	TR1	TR0	TREBLE (dB)		
					FLAT SET	MIN. SET	MAX. SET
0	0	0	0	0	0	0	0
0	0	0	0	1	0	0	0
0	0	0	1	0	0	0	0
0	0	0	1	1	0	0	0
0	0	1	0	0	0	2	2
0	0	1	0	1	0	2	2
0	0	1	1	0	0	2	2
0	0	1	1	1	0	2	2
0	1	0	0	0	0	4	4
0	1	0	0	1	0	4	4
0	1	0	1	0	0	4	4
0	1	0	1	1	0	4	4
0	1	1	0	0	0	6	6
0	1	1	0	1	0	6	6
0	1	1	1	0	0	6	6
0	1	1	1	1	0	6	6
...	...	...	...	...	0	6	6
1	1	1	1	1	0	6	6

Bass control

For the playback channel, bass can be regulated in three audio modes: minimum, flat and maximum mode. In flat mode the audio is not influenced. In minimum mode the bass range is from 0 to approximately 14 dB in steps of 1.5 dB. In maximum mode, the bass range is from 0 to approximately 24 dB in steps of 2 dB. The programmable bass filters are implemented digitally and have a fixed corner frequency of 100 Hz for the minimum mode and 75 Hz for the maximum mode. Because of the exceptional amount of programmable gain, bass should be used with adequate prior attenuation, using volume control.

Table 12 Bass boost settings

BB4	BB3	BB2	BB1	BB0	BASS (dB)		
					FLAT SET	MIN. SET	MAX. SET
0	0	0	0	0	0	0	0
0	0	0	0	1	0	0	0
0	0	0	1	0	0	0	0
0	0	0	1	1	0	0	0
0	0	1	0	0	0	1.1	1.7
0	0	1	0	1	0	1.1	1.7
0	0	1	1	0	0	2.4	3.6
0	0	1	1	1	0	2.4	3.6
0	1	0	0	0	0	3.7	5.4
0	1	0	0	1	0	3.7	5.4
0	1	0	1	0	0	5.2	7.4
0	1	0	1	1	0	5.2	7.4
0	1	1	0	0	0	6.8	9.4
0	1	1	0	1	0	6.8	9.4
0	1	1	1	0	0	8.4	11.3
0	1	1	1	1	0	8.4	11.3
1	0	0	0	0	0	10.2	13.3
1	0	0	0	1	0	10.2	13.3
1	0	0	1	0	0	11.9	15.2
1	0	0	1	1	0	11.9	15.2
1	0	1	0	0	0	13.7	17.3
1	0	1	0	1	0	13.7	17.3
1	0	1	1	0	0	13.7	19.2
1	0	1	1	1	0	13.7	19.2
1	1	0	0	0	0	13.7	21.2
1	1	0	0	1	0	13.7	21.2
1	1	0	1	0	0	13.7	23.2
1	1	0	1	1	0	13.7	23.2
...	...	...	...	...	0	13.7	23.2
1	1	1	1	1	0	13.7	23.2

De-emphasis

De-emphasis is controlled by bit 4 of control register 0. The de-emphasis filter can be switched on or off. The digital de-emphasis filter is dimensioned to produce the de-emphasis frequency characteristics for the sample rate 44.1 kHz. De-emphasis is synchronized to the sample clock, so that operation always takes place on complete samples.

Filter characteristics playback channel

The overall filter characteristic of the UDA1325 in flat mode is given in Fig.4 (de-emphasis off). The overall filter characteristic of the UDA1325 includes the filter characteristics of the DSP in flat mode plus the filter characteristic of the FSDAC (f_s = 44.1 kHz)

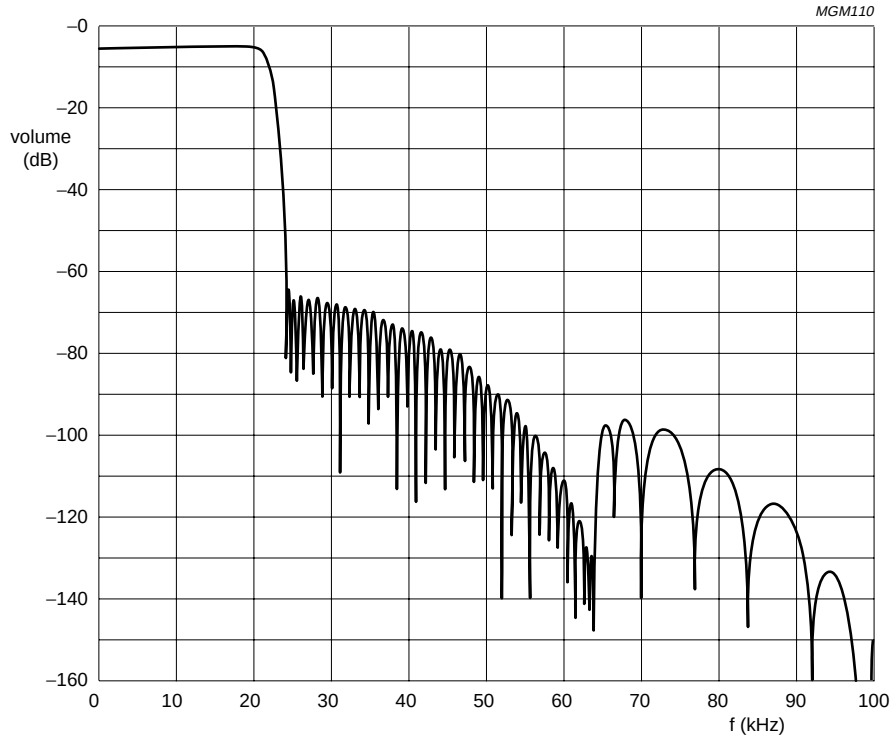


Fig.4 Overall filter characteristics of the UDA1325.

DSP extension port for enhanced playback audio processing

An external DSP can be used for adding extra sound processing features via the I²S inputs and outputs of the digital I/O module. The UDA1325 supports the standard I²S-bus data protocol and the LSB-justified serial data input format with word lengths of 16, 18 and 20 bits. Using the 4-pin digital I/O option the UDA1325 device acts as a master, controlling the BCKO and WSO signals. Using the 6-pin digital I/O option GP2, GP3 and GP4 are output pins (master) and GP0, GP1 and GP5 are input pins (slave).

The period of the WSO signal is determined by the number of samples in the 1 ms frame of the USB. This implies that the WSO signal does not have a constant time period, but is jittery.

The characteristic timing of the I²S-bus signals is illustrated in Figs 5 and 6.

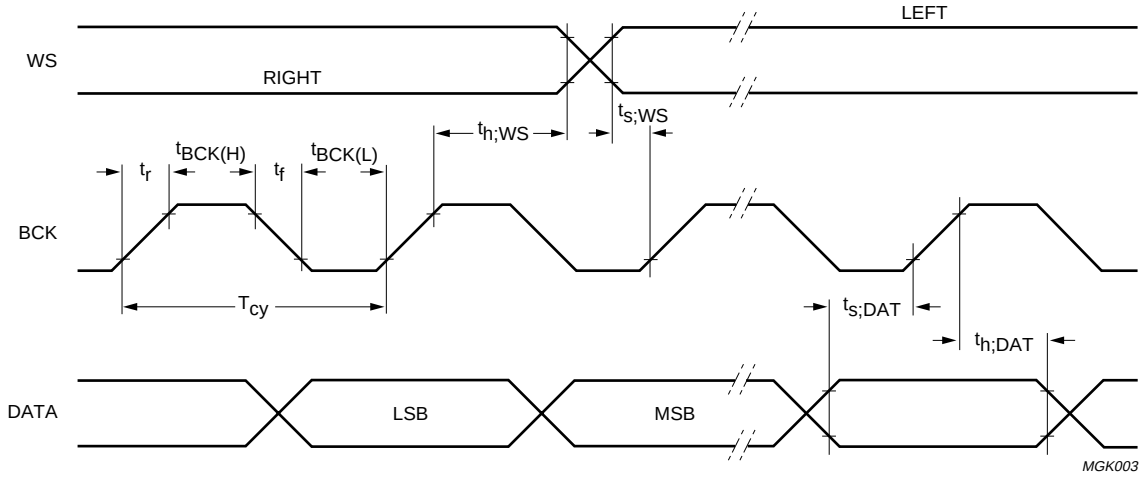


Fig.5 Timing of digital I/O input signals.

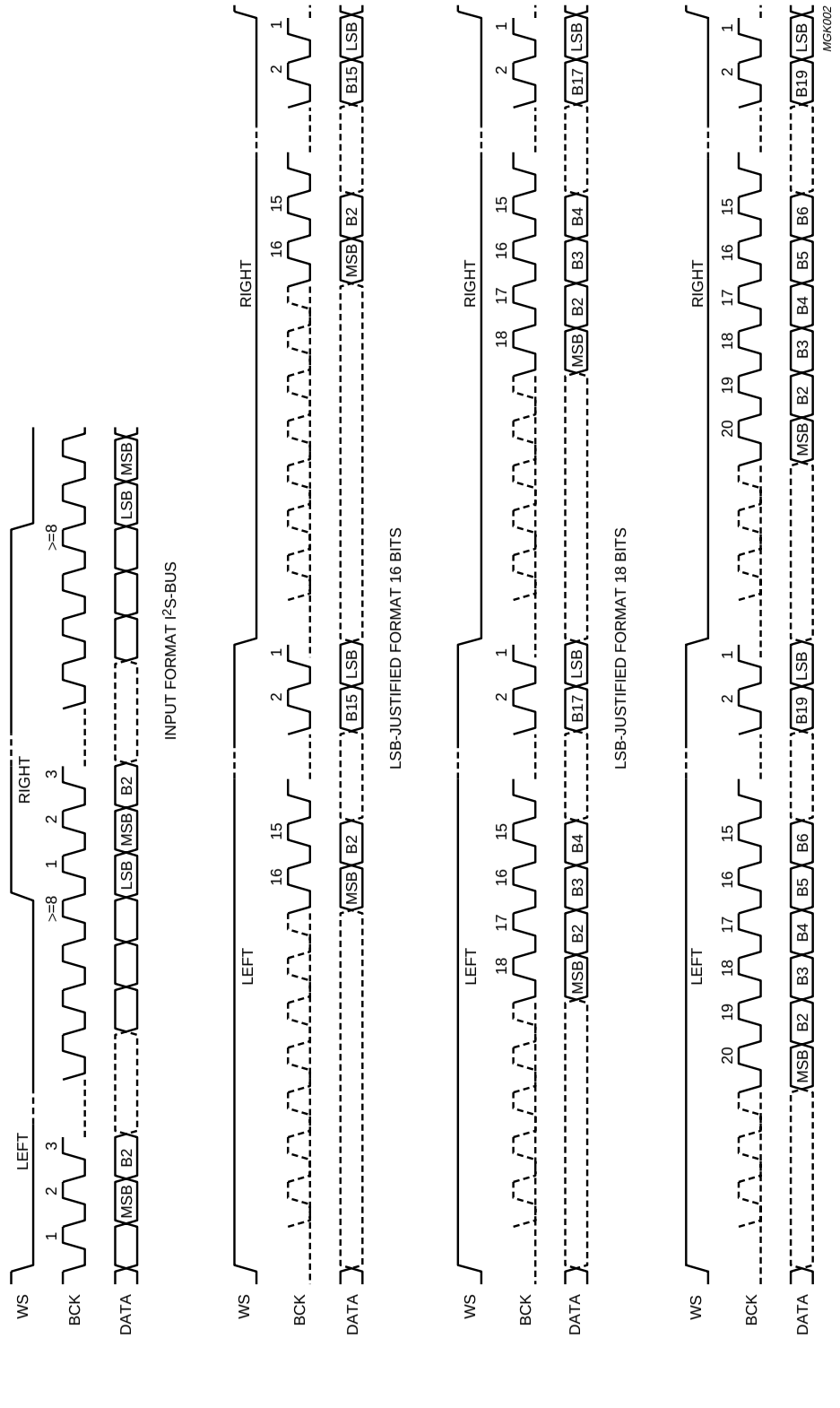


Fig.6 Input formats.

PORT DEFINITION 80C51

Port 1

Table 13 Port 1 of the 80C51 microcontroller

8 BIT PORT 1				
BIT	**FUNCTION**	**LOW**	**HIGH**	**COMMENT**
1.0	ADAC_error	no error	error	
1.1	GP1			general purpose pins
1.2	GP2			
1.3	GP3			
1.4	GP4			
1.5	GP5			
1.6	SCL			I^2C-bus
1.7	SDA			

Port 3

Table 14 Port 3 of the 80C51 microcontroller

8 BIT PORT 3				
BIT	**FUNCTION**	**LOW**	**HIGH**	**COMMENT**
3.0	ASR_error	no error	error	
3.1	PSIE_MMU_SUSPEND	no suspend	suspend	suspend input from USB interface during normal operation or input from restart circuit
3.2	GP0 (INT0_N)			general purpose pin
3.3	PSIE_MMU_INT (INT1_N)			interrupt input from USB interface during normal operation or input from restart circuit
3.4	PSIE_MMU_READY			
3.5	L3_MODE			
3.6	L3_CLK			
3.7	L3_DATA			

MEMORY AND REGISTER SPACE 80C51

Overview registers

Table 15 Register location and recommended values after Power-on reset

ADDRESS	REGISTER	RESET VALUE
0800h	PGA gain	09
0801h	ADIF control	5C
1000h	clock shop settings	00
1001h	reset control and APLL settings	00
1002h	IO selection register	01
1003h	power control	00
2000h	ASR settings	8B
4000h	data register PSIE	
4001h	command register PSIE	

Table 16 Special function register location

ADDRESS	REGISTER	RESET VALUE
CPU registers		
81h	SP	
82h	DPL	
83h	DPH	
D0h	PSW	
E0h	ACC	
F0h	B	
Interrupt registers		
A8h	IE	00h
B8h	IP	00h
Timer 0 and Timer 1 registers		
88h	T01CON	00h
89h	T01MOD	00h
8Ah	T0L	00h
8Bh	T1L	00h
8Ch	T0h	00h
8Dh	T1h	00h
PCON registers		
87h	PCON	00h
Port registers		
80h	P0	FFh
90h	P1	FFh
A0h	P2	FFh
B0h	P3	FFh
I^2C registers (SIO1 registers)		
D8h	S1CON	00h
D9h	S1STA	
DAh	S1DAT	
DBh	S1ADR	

Interrupts

The UDA1325 supports up to five (of maximal 7) interrupt sources. Each interrupt source corresponds to an interrupt vector in the CPU program memory address space:

Source 0: vector 0003h external interrupt 0 (INT0_N)

Source 1: vector 000Bh Timer 0 interrupt

Source 2: vector 0013h external interrupt 1 (INT1_N)

Source 3: vector 001Bh Timer 1 interrupt

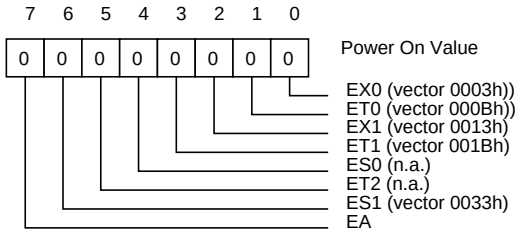
Source 4: vector 0023h UART interrupt (not present)

Source 5: vector 002Bh Timer 2 interrupt (not present)

Source 6: vector 0033h I^2C interrupt.

INTERRUPT ENABLE REGISTER (IE)

Each interrupt source can be individually enabled or disabled by setting or clearing a bit in IE. This register also contains a global interrupt enable bit (EA) which can be cleared to disable all interrupts at once.



Internal registers

Table 17 PGA gain registers

ADDRESS	REGISTER	COMMENTS	BIT	VALUE
0800h	PGA gain register	reserved	7	X
		PGA input selection	6	0 (do not change it)
		PGA gain right channel	5, 4 and 3	000 = –3 dB 001 = 0 dB 010 = 3 dB 011 = 9 dB 100 = 15 dB 101 = 21 dB 110 = 27 dB 111 = 27 dB
		PGA gain left channel	2, 1 and 0	000 = –3 dB 001 = 0 dB 010 = 3 dB 011 = 9 dB 100 = 15 dB 101 = 21 dB 110 = 27 dB 111 = 27 dB

Table 18 ADIF control registers

ADDRESS	REGISTER	COMMENTS	BIT	VALUE
0801h	ADIF control register	reserved	7	X
		number of bits per audio sample to be transmitted to the host	6 and 5	00 = reserved
				01 = 8 bits audio samples
				10 = 16 bits audio samples
				11 = 24 bits audio samples
		mono/stereo selection	4	0 = mono
				1 = stereo
		selection audio input recording channel	3	0 = digital serial audio input
				1 = analog input
		selection high-pass filter of ADIF (DC-filter)	2	0 = high-pass filter off
				1 = high-pass filter on
		I^2S-bus input serial input format recording channel	1 and 0	00 = I^2S-bus
				01 = 16-bit LSB justified
				10 = 18-bit LSB justified
				11 = 20-bit LSB justified

Table 19 Clock shop register

ADDRESS	REGISTER	COMMENTS	BIT	VALUE
1000h	clock shop settings	selection ADC clock source	7	0 = ADC clock from APLL
				1 = ADC clock from OSCAD
		divide factor Q	6 and 5	00 = ADC clock divided-by-1
				01 = ADC clock divided-by-2
				10 = ADC clock divided-by-4
				11 = ADC clock divided-by-8
		clock ADAC	4	0 = enable 1 = disable
		clock 48 MHz internal	3	0 = enable 1 = disable
		clock recovered by PSIE	2	0 = enable 1 = disable
		ADC clock	1	0 = enable 1 = disable
		OSCAD oscillator	0	0 = power on 1 = power off

Table 20 Reset control and APLL register

ADDRESS	REGISTER	COMMENTS	BIT	VALUE
1001h	reset control and APLL settings	fcode (1 and 0) clock frequency selection APLL	7 and 6	00 = 256 × 44.1 kHz 01 = 256 × 32 kHz 10 = 256 × 48 kHz 11 = 256 × 44.1 kHz
		reserved	5	X
		reset ADAC	4	0 = reset off 1 = reset on
		reset MMU	3	0 = reset off 1 = reset on
		reset digital I/O-interface	2	0 = reset off 1 = reset on
		reset ADIF	1	0 = reset off 1 = reset on
		reserved	0	X

Table 21 I/O selection register

ADDRESS	REGISTER	COMMENTS	BIT	VALUE
1002h	I/O selection register	microcontroller control on 48 MHz oscillator	7	0 = UPC control disabled (48 MHz oscillator is enabled)
				1 = UPC control enabled
		audio format	6 and 5	00 = 4-pins I^2S 01 = 6-pins I^2S 10 = 3-pins I^2S (only input) 11 = 3-pins I^2S (only input)
		GP4 I/O if BIT0 = 1	4	0 = output 1 = input
		GP3 I/O if BIT0 = 1	3	0 = output 1 = input
		GP2 I/O if BIT0 = 1	2	0 = output 1 = input
		GP1 I/O if BIT0 = 1	1	0 = output 1 = input
		GP4 to GP1 function	0	0 = I^2S usage 1 = general purpose usage

Table 22 Power control register

ADDRESS	REGISTER	COMMENTS	BIT	VALUE
1003h	power control register analog modules	suspend input selection for P3.1 of the microcontroller	7	0 = suspend from USB interface connected to P3.1 during normal operation 1 = suspend from restart circuit connected to P3.1 (e.g. after power-down)
		interrupt input selection for P3.3 (INT1_N) of the microcontroller	6	0 = interrupt from USB interface connected to P3.3 during normal operation 1 = interrupt from restart circuit connected to P3.3 (e.g. after power-down)
		power APLL	5	0 = power on 1 = power off
		power FSDAC	4	0 = power on 1 = power off
		power ADC left	3	0 = power on 1 = power off
		power ADC right	2	0 = power on 1 = power off
		power PGA left	1	0 = power on 1 = power off
		power PGA right	0	0 = power on 1 = power off

Table 23 ASR control register

ADDRESS	REGISTER	COMMENTS	BIT	VALUE
2000h	ASR control register	robust word clock	7	0 = off (not recommended) 1 = on (recommended)
		serial I^2S-bus output format digital I/O interface	6 and 5	00 = I^2S-bus
				01 = 16-bit LSB justified
				10 = 18-bit LSB justified
				11 = 20-bit LSB justified
		phase inversion (on right mono output)	4	0 = mono phase inversal off
				1 = mono phase inversal on
		bits per sample modi	3 and 2	00 = reserved
				01 = 8-bit audio
				10 = 16-bit audio
				11 = 24-bit audio
		mono or stereo operation	1	0 = mono
				1 = stereo
		ASR register start-up mode	0	0 = stop (e.g. at alternate setting with bandwidth equal to zero) 1 = go

START-UP BEHAVIOUR AND POWER MANAGEMENT

Start-up of the UDA1325

After power-on (of V_{DDA1}), an internal Power-on reset signal becomes HIGH after a certain RC time. This RC time is created by using the internal resistor (2×50 kΩ) divider for creating the reference voltage for the FSDAC in combination with the capacitor connected externally to the V_{REFDA} pin. The FSDAC and the internal resistor divider are supplied by V_{DDA1} and V_{SSA1}. The RC time can be calculated using R = 25000 Ω and C = C_{ref}.

During 20 ms after Power-on reset becomes HIGH the UDA1325 has to initiate the internal registers. During this initialisation, the user should prevent indicating the ‘connected’ status to the USB-host. This can be done by forcing the DP-line LOW (i.e. via one of the GP pins).

Power Management

The total current drawn from the USB supply (for i.e. bus-powered operation of the UDA1325 application) must be less than 500 μA in suspend mode. In order to reach that low current target, the total power dissipation of the UDA1325 can be reduced by disabling all internal clocks and switching off all internal analog modules.

Important note: In order to make use of power reduction (Power-down mode) and be able to restart after power-down, a number of precautions must be taken!

AT INITIALISATION TIME

- Bit 7of the power control register (mux_ctrl_suspend) must be set to ‘1’, in order to connect the CLK_ON of the USB processor with P3.1 of the microcontroller
- Bit 6 of the power control register (mux_ctrl_int1) must be set to ‘0’, in order to connect the PSIE_MMU_INT output pin of the USB processor with P3.3 (INT1_N) of the microcontroller
- Bit 7of the I/O selection register must be set to ‘1’, in order to enable the power-on control of the 48 MHz crystal oscillator automatically by the microcontroller.

IN NORMAL OPERATION MODE

In normal operation working mode, a suspend can be initiated by the falling edge of the CLK_ON output signal of the USB processor. This falling edge comes about 2 ms after the rising edge of the PSIE_MMU_SUSPEND output signal of the USB processor. At this moment, several actions should be taken by the microcontroller:

- All analog modules of the UDA1325 must be switched off; this can be done by setting bits 5 to 0 of the power control register to ‘1’ and bit 0 of the clock shop register to ‘1’
- Bit 6 of the power control register (mux_ctrl_int1) must be set to ‘1’, in order to awake from power-down by the CLK_ON signal of the USB processor
- Put all GP pins in the high or low state (depending of how they are used in the UDA1325 application)
- Put the microcontroller in Power-down mode. This can be done via the PCON register of the microcontroller. This results in an automatically switching off the 48 MHz crystal oscillator and with that all internal clocks (if they are enabled).

On the rising edge of the CLK_ON output signal, the 48 MHz crystal oscillator will be switched on automatically and with that all internal clocks (if they are enabled). At the same time, a counter starts counting for 2048 clock cycles (170 μs). This time is necessary for stabilising the 48 MHz clock of the 48 MHz crystal oscillator.

When the counter reaches its end value (after 2048 cycles), a rising edge will be detected on the P3.3 (INT1_N) of the microcontroller. At this moment, following actions should be taken by the microcontroller:

- The Power-down mode of the microcontroller must be switched off
- Re-initialise all GP pins
- All analog modules of the UDA1325 must be switched on; this can be done by setting bits 5 to 0 of the power control register to ‘0’ and bit 0 of the clock shop register to ‘0’
- Bit 6 of the power control register (mux_ctrl_int1) must be set to ‘0’, in order to connect the PSIE_MMU_INT output pin of the USB processor again with P3.3 (INT1_N) of the microcontroller.

The UDA1325 is now back in its normal operation mode and can be put back in power reduction mode by the falling edge of the CLK_ON signal of the USB processor.

COMMAND SUMMARY

COMMAND NAME	RECIPIENT	CODING	DATA PHASE
Initialization commands			
Set address/enable	device	D0h	write 1 byte
Read address/enable	device	D0h	read 1 byte
Set endpoint enable	device	D8h	write 1 byte
Read endpoint enable	device	D8h	read 1 byte
Set mode	device	F3h	write 1 byte
Data flow commands			
Read interrupt register	device	F4h	read 1 byte
Select endpoint	control OUT	00h	read 1 byte (optional)
	control IN	01h	read 1 byte (optional)
	other endpoints	00h + endpoint index	read 1 byte (optional)
Get endpoint status	control OUT	40h	read 1 byte
	control IN	41h	read 1 byte
	other endpoints	40h + endpoint index	read 1 byte
Set endpoint status	control OUT	40h	write 1 byte
	control IN	41h	write 1 byte
	other endpoints	40h + endpoint index	write 1 byte
Read buffer	selected endpoint	F0h	read n bytes
Write buffer	selected endpoint	F0h	write n bytes
Acknowledge setup	selected endpoint	F1h	none
Clear buffer	selected endpoint	F2h	none
Validate buffer	selected endpoint	FAh	none
General commands			
Read current frame number		F5h	read 1 or 2 bytes

COMMAND DESCRIPTIONS

Command procedure

This chapter describes the commands that can be used by the microcontroller to control the USB processor. There are three basic types of commands:

- Initialization commands
- Data flow commands
- General commands.

A command is represented by an 8 bit code. It can be followed by one or more data write cycles or one or more read cycles or a combination. The PSIE_MMU_READY output connected to Port 3.4 of the microcontroller indicates that the previous action (command write, data read or data write) has completed. A new action can only be initiated if PSIE_MMU_READY is TRUE. The data is valid from the moment PSIE_MMU_READY becomes TRUE.

The PSIE contains a number of interrupt registers, one for each endpoint. Every time a transition occurs, the interrupt flag for the involved endpoint is set. The PSIE_MMU_INT connected to Port 3.3 is an OR function of all interrupt registers.

Initialization commands

Initialization commands are used during the enumeration process of the USB network. They are used to set the USB assigned address, enable endpoints and select the configuration of the device.

SET ADDRESS/ENABLE

Command: D0h.

Data: write 1 byte.

The set address/enable command is used to set the USB assigned address and enable the function. The device always powers up disabled and should be enabled after a bus reset.

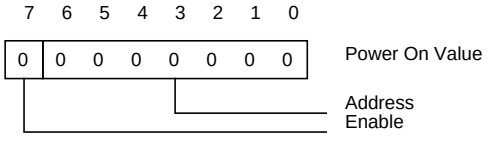


Table 24

BIT	DESCRIPTION
Address	the value written becomes the device address
Enable	a ‘1’ enables this function

READ ADDRESS/ENABLE

Command: D0h.

Data: read 1 byte.

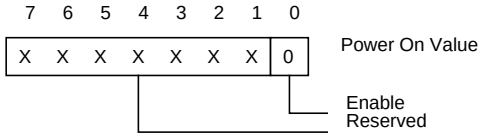
The read address/enable command is used to read the USB assigned address and the enable bit of the device. The format of the data phase is the same as for the set address/enable command.

SET ENDPOINT ENABLE

Command: D8h.

Data: write 1 byte.

The set endpoint enable command is used to set the enable bits for the non default endpoints.



If the enable bit is ‘1’, the non default endpoints are enabled, if ‘0’, the non default endpoints are disabled. The function then only responds to the default control endpoint.

After bus reset, the enable bit is set to ‘0’.

READ ENDPOINT ENABLE

Command: D8h.

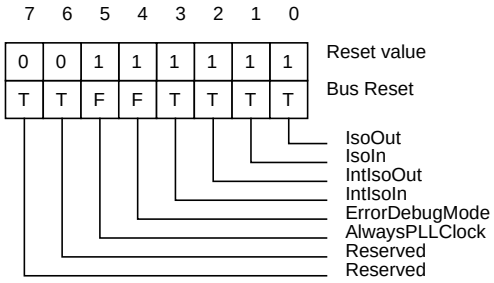
Data: read 1 byte.

The read endpoint enable command is used to read the enable bit for the non default endpoints of the function. The format of the data phase is the same as for the set endpoint enable command.

SET MODE

Command: F3h.

Data: write 1 byte.



Reset value: gives the value of the bits after Power-on reset. Bus reset: a 'F' indicates that the value of the bit is not changed during a bus reset. a 'T' indicates that during a bus reset, the bit is reset to its reset value.

Table 25

BIT	DESCRIPTION
IsoOut	ISO out endpoint can be used
IsoIn	ISO in endpoint can be used
IntIsoOut	allow interrupt from ISO out endpoint
IntIsoIn	allow interrupt from ISO in endpoint
ErrorDebugMode	Setting chip in debug mode
AlwaysPLLClock	the PLL clock must keep on running

Data flow commands

Data flow commands are used to manage the data transmission between the USB endpoints and the host. Much of the data flow is initiated via the interrupt to the microcontroller. The microcontroller uses these commands to access the endpoint buffers and determine whether the endpoint buffers have valid data.

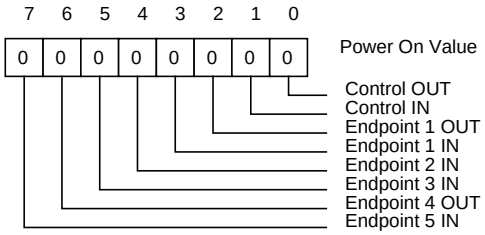
READ INTERRUPT REGISTER

Command: F4h.

Data: read 1 byte.

The read interrupt register command returns the value of the interrupt register. Every time a packet is received or transmitted, an interrupt will be generated and a flag specific to the physical endpoint will be set in the interrupt register. Reading the status of the endpoint will clear the flag.

An interrupt is also generated after a bus reset. When the interrupt register consists of all zeros, and an interrupt was generated, there was a bus reset. The interrupt is cleared when the interrupt register is read.

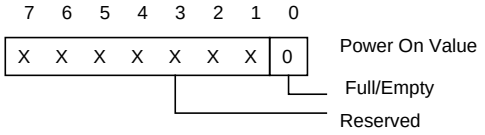


SELECT ENDPOINT

Command: 00h + endpoint index.

Data: optional read 1 byte.

The select endpoint command initializes an internal pointer to the start of the selected buffer. Optionally, this command can be followed by a data read. Bit 0 is low if the buffer is empty and high if the buffer is full. There is one command for every endpoint.



GET ENDPOINT STATUS

Command: 40h + endpoint index.

Data: read 1 byte.

The get endpoint status command is followed by one data read that returns the status of the last transaction of the selected endpoint. This command also resets the corresponding interrupt flag in the interrupt register, and clears the status, indicating that it was read. There is one command for every endpoint.

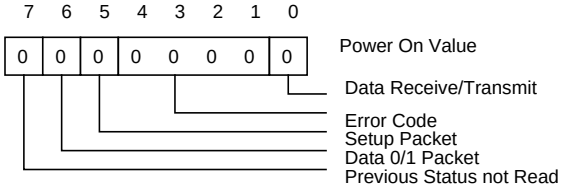


Table 26 Error codes

ERROR CODE	RESULT
0000	no error
0001	PID encoding error; bits 7 to 4 in the PID token are not the inversion of bits 3 to 0
0010	PID unknown; PID encoding is valid, but PID does not exist
0011	unexpected packet; packet is not of the type expected (token, data or acknowledge), or SETUP token received on non-control endpoint
0100	token CRC error
0101	data CRC error
0110	time out error
0111	babble error
1000	unexpected end-of-packet
1001	sent or received NAK
1010	sent stall, a token was received, but the endpoint was stalled
1011	overflow error, the received data packet was larger then the buffer size of the selected endpoint
1100	sent empty packet (ISO only)
1101	bitstuff error
1110	error in sync
1111	wrong data PID

Table 27

BIT	DESCRIPTION
Data receive/transmit	a ‘1’ indicates data has been received or transmitted successfully
Error code	see Table 26
Setup packet	a ‘1’ indicates the last received packet had a SETUP token (this will always read ‘0’ for IN buffers)
Data 0/1 packet	a ‘1’ indicates the last received packet had a DATA 1 PID
Previous status not read	a ‘1’ indicates a second event occurred before the previous status was read

SET ENDPOINT STATUS

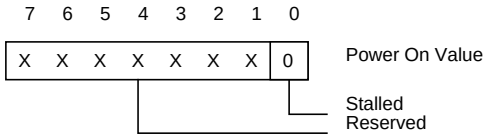
Command: 40h + endpoint index.

Data: write 1 byte.

This command is used to stall or unstall an endpoint. Only the least significant bit has a meaning. When the stalled bit is equal to 1, the endpoint is stalled, when equal to 0, the endpoint is unstalled. There is one command for every endpoint.

A stalled control endpoint is automatically unstalled when it receives a SETUP token, regardless of the contents of the packet. If the endpoint should stay in stalled state, the microcontroller should restall it.

When a stalled endpoint is unstalled, it is also re-initialized. This means that its buffer is flushed and the next DATA PID that will be sent or expected (depending on the direction of the endpoint) is DATA0.



READ BUFFER

Command: F0h.

Data: read n bytes (max. 10).

The read buffer command is followed by a number of data reads, which returns the contents of the selected endpoint data buffer. After each read, the internal buffer pointer is incremented by 1.

The buffer pointer is not reset to the buffer start by the read buffer command. This means that reading a buffer can be interrupted by any other command (except for select endpoint).

The data in the buffer are organized as follows:

Byte 0: transfer successful, number of data bytes (MSB)

Byte 1: number of data bytes (LSB)

Byte 2: data byte 0

Byte 3: data byte 1

Byte 4: data byte 2

Byte 5: data byte 3

Byte 6: data byte 4

Byte 7: data byte 5

Byte 8: data byte 6

Byte 9: data byte 7.

Bytes 0 and 1 indicate the number of bytes in the buffer. Byte 0 is the Most Significant Byte (MSB). Byte 1 is the Least Significant Byte (LSB). Only bits 1 and 0 of byte 0 are used in the number of bytes indication.

Bit 7 of byte 0 indicates if the transaction was successful (bit 7 is '1' if the transaction was successful). Bits 6 to 2 of byte 0 are reserved.

WRITE BUFFER

Command: F0h.

Data: write n bytes (max. 10).

The write buffer command is followed by a number of data writes, which load the endpoint buffer. After each write, the internal buffer pointer is incremented by 1.

The buffer pointer is not reset to the buffer start by the write buffer command. This means that writing a buffer can be interrupted by any other command (except for select endpoint).

The data must be organized in the same way as described in the read buffer command. Bits 7 to 2 of byte 0 are reserved and must be filled with zeros.

ACKNOWLEDGE SETUP

Command: F1h.

Data: none.

The arrival of a SETUP packet flushes the IN buffer and disables the validate buffer and clear buffer commands for both IN and OUT endpoints.

The microcontroller needs to re-enable these commands by the acknowledge setup command. This ensures that the last SETUP packet stays in the buffer and no packet can be sent back to the host until the microcontroller has acknowledged explicitly that it has seen the SETUP packet.

If the microcontroller is reading the data from a SETUP packet, and a new SETUP packet arrives, the device must accept this new SETUP packet. So the data, currently being read by the microcontroller, is overwritten with the new packet. On the arrival of the new packet, the commands validate buffer and clear buffer are disabled. If the microcontroller has finished reading the data from the buffer, it will try to clear the buffer. The device will ignore this command, so the new SETUP packet in the buffer is not cleared. The microcontroller will now detect the interrupt of the new SETUP packet and will start reading the new data in the buffer.

A SETUP token can be followed by an IN token. After the SETUP token, the microcontroller will start filling the IN buffer. A SETUP token will clear the IN buffer. This avoids the following problem: after a SETUP token, the microcontroller fills the IN buffer. If the SETUP token is followed by a SETUP token and shortly followed by an IN token, the device will send the contents of the IN buffer to the host. The IN buffer was filled after the first SETUP token. That is why after a SETUP token the IN buffer is cleared.

If the microcontroller is still filling the buffer when the second SETUP token arrives, the SETUP token will clear the IN buffer. If the microcontroller has filled the IN buffer, it will validate the buffer. So clearing the IN buffer on receiving a SETUP token is not enough.

If a SETUP token is received, the device will also disable the validate buffer command for the IN buffer. If the microcontroller needs to fill the buffer after a SETUP token, the command acknowledge setup command must be sent to enable the validate buffer command.

CLEAR BUFFER

Command: F2h.

Data: none.

When a packet is received completely, an internal endpoint buffer full flag is set. All subsequent packets will be refused by returning a NACK to the host. When the microcontroller has read the data, it should free the buffer by the clear buffer command. When the buffer is cleared, new packets will be accepted.

VALIDATE BUFFER

Command: FAh.

Data: none.

When the microcontroller has written data into an IN buffer, it should set the buffer full flag by the validate buffer command. This indicates that the data in the buffer are valid and can be sent to the host when the next IN token is received.

General commands

READ CURRENT FRAME NUMBER

Command: F5h.

Data: read 1 or 2 bytes.

This command is followed by one or two data reads and returns the frame number of the last successfully received SOF. The frame number is eleven bits wide. The frame number is returned least significant byte first. In case the user is only interested in the lower 8 bits of the frame number only the first byte needs to be read.

I²C MASTER/SLAVE INTERFACE

The I²C module implements a master/slave I²C-bus interface with integrated shift register, shift timing generation and slave address recognition. It is compliant to the I²C-bus specification IC20/Jan92. I²C standard mode (100 kHz SCL) and fast mode (400 kHz) are supported. Low speed mode and extended 10 bit addressing are unsupported.

Characteristics of the I²C-bus

The I²C-bus is for 2-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a Serial Clock Line (SCL). Both lines must be connected to V_{DDE} via a pull-up resistor.

The timing definition of the I²C-bus is given in Fig.7.

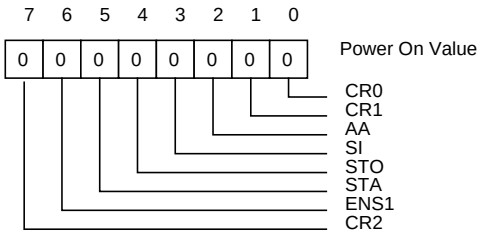
Programmer's view

For a detailed description of the I²C-bus protocol refer to Philips Integrated Circuits Data Handbook IC20, 8XC552.

The programmer's view of the I²C library function is -with one exception- identical to that of the 8XC552 microcontroller. Only the bit rate frequency selection in S1CON and the handling of the Timer 1 overflow information deviates to accommodate 400 kHz operation.

S1CON register

The CPU can read from and write to this 8-bit SFR. Two bits are effected by the SIO1 hardware: the SI bit is set when a serial interrupt is requested, and the STO bit is cleared when a STOP condition is present on the I²C-bus. The STO bit is also cleared when ENS1 = '0'. Reset initializes S1CON to 00h.



CR2, 1 AND 0 - THE CLOCK RATE BITS

These three bits determine the serial clock frequency when SIO1 is in a master mode.

The various serial rates are shown in Table 28.

Table 28 Serial clock rates (SCL line)

CR2	CR1	CR0	I²C BIT FREQUENCY (kHz)
0	0	0	1200
0	0	1	600
0	1	0	400
0	1	1	300
1	0	0	150
1	0	1	100
1	1	0	75
1	1	1	3.9 ... 501

When the CR bits are '111', the maximum bit rate for the data transfer will be derived from the Timer 1 overflow rate divided by 2 (i.e. every time the Timer 1 overflows, the SCL signal will toggle).

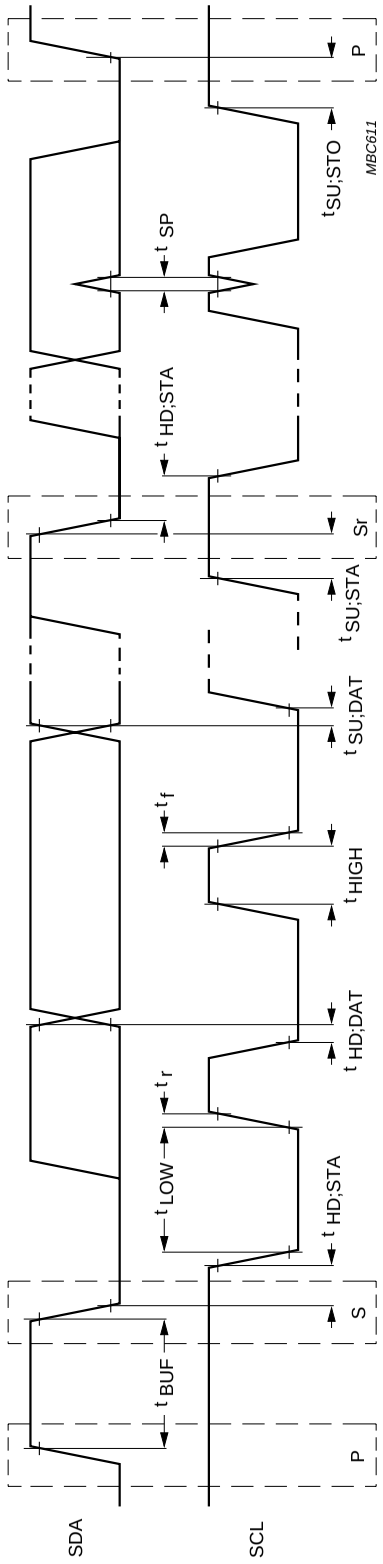


Fig.7 Definition of timing of the I²C-bus.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
All digital I/Os						
$V_{I/O}$	DC input/output voltage range		–0.5	–	V_{DDE}	V
I_O	output current	V_{DDE} = 5.0 V	–	–	4	mA
Temperature values						
T_j	junction temperature		0	–	125	°C
T_{stg}	storage temperature		–55	–	+150	°C
T_{amb}	operating ambient temperature		0	25	70	°C
Electrostatic handling						
V_{es}	electrostatic handling	note 1	–3000	–	+3000	V
		note 2	–300	–	+300	V

Notes

1. Equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.
2. Equivalent to discharging a 200 pF capacitor through a 2.5 μH series conductor.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(j-a)}$	thermal resistance from junction to ambient			
	UDA1325PS	in free air	48	K/W
	UDA1325H	in free air	48	K/W

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DDE}	supply voltage periphery (I/O)	4.75	5.0	5.25	V
V_{DD}	supply voltage (core)	3.0	3.3	3.6	V
V_I	DC input voltage range				
	for D+ and D–	0.0	–	V_{DD}	V
	for VINL and VINR	–	$0.5V_{DD}$	–	V
	for digital I/Os	0.0	–	V_{DDE}	V

DC CHARACTERISTICS

V_{DDE} = 5.0 V; V_{DD} = 3.3 V; T_{amb} = 25 °C; f_{osc} = 48 MHz; f_s = 44.1 kHz; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{DDE}	digital supply voltage periphery		4.75	5.0	5.25	V
V_{DDI}	digital supply voltage core		3.0	3.3	3.6	V
V_{DDA1}	analog supply voltage 1		3.0	3.3	3.6	V
V_{DDA2}	analog supply voltage 2		3.0	3.3	3.6	V
V_{DDA3}	analog supply voltage 3		3.0	3.3	3.6	V
V_{DDO}	operational amplifier supply voltage		3.0	3.3	3.6	V
V_{DDX}	crystal oscillator supply voltage		3.0	3.3	3.6	V
I_{DDE}	digital supply current periphery	note 1	–	3.7	–	mA
I_{DDI}	digital supply current core		–	39.0	–	mA
I_{DDA1}	analog supply current 1		–	3.6	–	mA
I_{DDA2}	analog supply current 2		–	8.0	–	mA
I_{DDA3}	analog supply current 3		–	0.9	9.0[2]	mA
I_{DDO}	operational amplifier supply current		–	3.0	–	mA
I_{DDX}	crystal oscillator supply current		–	1.2	13.0[3]	mA
P_{tot}	total power dissipation		–	200	–	mW
P_{ps}	total power dissipation in power saving mode	note 4	–	1.2	–	mW
Inputs/outputs D+ and D–						
V_I	static DC input voltage		–0.5	–	V_{DDI}	V
$V_{O(H)}$	static DC output voltage HIGH	R_L = 15 kΩ connected to GND	2.8	–	3.6	V
$V_{O(L)}$	static DC output voltage LOW	R_L = 1.5 kΩ connected to V_{DD}	–	–	0.3	V
$\lvert I_{LO} \rvert$	high impedance data line output leakage current		–	–	10	μA
$V_{I(diff)}$	differential input sensitivity		0.2	–	–	V
$V_{CM(diff)}$	differential common mode range		0.8	–	2.5	V
$V_{SE(R)(th)}$	single-ended receiver threshold voltage		0.8	–	2.0	V
C_{IN}	transceiver input capacitance	pin to GND	–	–	20	pF
Digital input pins						
V_{IL}	LOW-level input voltage		–	–	$0.3V_{DDE}$	V
V_{IH}	HIGH-level input voltage		$0.7V_{DDE}$	–	V_{DDE}	V
$\lvert I_{LI} \rvert$	input leakage current		–	–	1	μA
C_I	input capacitance		–	–	5	pF

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
PGA and ADC						
$V_{ref(AD)}$	reference voltage PGA and ADC		–	$0.5V_{DDA2}$	–	V
$V_{ref(ADC)(pos)}$	positive reference voltage of the ADC		–	V_{DDA2}	–	V
$V_{ref(ADC)(neg)}$	negative reference voltage of the ADC		–	0.0	–	V
$V_{I(PGA)}$	DC input voltage VINL and VINR of the PGA		–	$0.5V_{DDA2}$	–	V
$R_{I(PGA)}$	DC input resistance at VINL and VINR of the PGA		–	12.5	–	kΩ
Filter stream DAC						
$V_{ref(DA)}$	reference voltage DAC		–	$0.5V_{DDA1}$	–	V
$V_{O(CM)}$	common mode output voltage		–	$0.5V_{DDA1}$	–	V
$R_{O(VOUT)}$	output resistance at VOUTL and VOUTR		–	11	–	Ω
$R_{O(L)}$	output load resistance		2.0	–	–	kΩ
$C_{O(L)}$	output load capacitance		–	–	50	pF

Notes

1. This value depends strongly on the application. The specified value is the typical value obtained using the application diagram as illustrated in Fig.8.
2. At start-up of the OSCAD oscillator.
3. At start-up of the OSC48 oscillator.
4. Exclusive the IDDE current which depends on the components connected to the I/O pins.

AC CHARACTERISTICS

V_{DDE} = 5.0 V; V_{DDI} = 3.3 V; T_{amb} = 25 °C; f_{osc} = 48 MHz; f_s = 44.1 kHz; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Driver characteristics D+ and D– (full-speed mode)						
$f_{o(s)}$	audio sample output frequency		5	–	55	kHz
t_r	rise time	C_L = 50 pF	4	–	20	ns
t_f	fall time	C_L = 50 pF	4	–	20	ns
$t_{rf(m)}$	rise/fall time matching (t_r/t_f)		90	–	110	%
V_{cr}	output signal crossover voltage		1.3	–	2.0	V
$R_{o(drive)}$	driver output resistance	steady-state drive	28	–	43	Ω
Data source timings D+ and D– (full-speed mode)						
$f_{i(s)}$	audio sample input frequency		5	–	55	kHz
$f_{fs(D)}$	full speed data rate		11.97	12.00	12.03	Mbits/s
$t_{fr(D)}$	frame interval		0.9995	1.0000	1.0005	ms
$t_{J1(diff)}$	source differential jitter to next transition		–3.5	0.0	+3.5	ns
$t_{J2(diff)}$	source differential jitter for paired transitions		–4.0	0.0	+4.0	ns
$t_{W(EOP)}$	source end of packet width		160	–	175	ns
$t_{EOP(diff)}$	differential to end of packet transition skew		–2.0	–	+5.0	ns
t_{JR1}	receiver data jitter tolerance to next transition		–18.5	0.0	+18.5	ns
t_{JR2}	receiver data jitter tolerance for paired transitions		–9.0	0.0	+9.0	ns
t_{EOPR1}	end of packet width at receiver must reject as end of packet		40	–	–	ns
t_{EOPR2}	end of packet width at receiver must accept as end of packet		82	–	–	ns
Serial input/output data timing						
f_s	system clock frequency		–	12	–	MHz
$f_{i(WS)}$	word selection input frequency		5	–	55	kHz
t_r	rise time		–	–	20	ns
t_f	fall time		–	–	20	ns
$t_{BCK(H)}$	bit clock HIGH time		55	–	–	ns
$t_{BCK(L)}$	bit clock LOW time		55	–	–	ns
$t_{s;DAT}$	data set-up time		10	–	–	ns
$t_{h;DAT}$	data hold time		20	–	–	ns
$t_{s;WS}$	word selection set-up time		20	–	–	ns
$t_{h;WS}$	word selection hold time		10	–	–	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
SDA and SCL lines for 100 kHz I^2C devices						
f_{SCL}	SCL clock frequency		0	–	100	kHz
t_{BUF}	bus free time between a STOP and START condition		4.7	–	–	µs
$t_{HD;STA}$	hold time (repeated) START condition		4.0	–	–	µs
t_{LOW}	LOW period of the SCL clock		4.7	–	–	µs
t_{HIGH}	HIGH period of the SCL clock		4.0	–	–	µs
$t_{SU;STA}$	set-up time for a repeated START condition		4.7	–	–	µs
$t_{SU;STO}$	set-up time for STOP condition		4.0	–	–	µs
$t_{HD;DAT}$	data hold time		5.0	–	–	µs
$t_{SU;DAT}$	data set-up time		250	–	–	ns
t_r	rise time of both SDA and SCL signals		–	–	1000	ns
t_f	fall time of both SDA and SCL signals		–	–	300	ns
$C_{L(bus)}$	capacitive load for each bus line		–	–	400	pF
Oscillator 1 (system clock)						
f_{osc}	oscillator frequency		–	48	–	MHz
δ	duty factor		–	50	–	%
g_m	transconductance		12.8	22.1	30.2	mS
R_o	output resistance		0.6	1.1	2.3	kΩ
$C_{i(XTAL1a)}$	parasitic input capacitance XTAL1a		4.5	4.8	5.2	pF
$C_{i(XTAL2a)}$	parasitic input capacitance XTAL2a		4.1	4.6	5.0	pF
I_{start}	start-up current		3.7	7.6	13.0	mA
Oscillator 2 (for ADC clock)						
f_{osc}	oscillator frequency		8.192	–	14.08	MHz
δ	duty cycle		–	50	–	%
g_m	transconductance		8.1	13.6	18.1	mA/V
R_o	output resistance		1.3	2.0	4.0	kΩ
$C_{i(XTAL1b)}$	parasitic input capacitance XTAL1b		5.0	5.4	5.7	pF
$C_{i(XTAL2b)}$	parasitic input capacitance XTAL2b		4.1	4.6	5.0	pF
I_{start}	start-up current		2.4	5.0	8.4	mA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Analog PLL (for ADC clock)						
$f_{clk(PLL)}$	PLL clock frequency		8.1920	11.2896	12.2880	MHz
δ	duty factor		–	50	–	%
$t_{strt(PO)}$	start-up time after power-on		–	–	10	ms
Power-on reset						
$t_{su(PO)}$	power-on set-up-time	note 1	$25C_{ref}$[2]	–	–	ms
PGA and ADC						
$V_{i(FS)(rms)}$	full-scale input voltage (RMS value)	PGA gain = –3 dB	–	1414[3]	–	mV
		PGA gain = 0 dB	–	1000	–	mV
		PGA gain = 3 dB	–	708	–	mV
		PGA gain = 9 dB	–	355	–	mV
		PGA gain = 15 dB	–	178	–	mV
		PGA gain = 21 dB	–	89	–	mV
		PGA gain = 27 dB	–	44	–	mV
$C_{i(PGA)}$	input capacitance of the PGA		–	–	20	pF
(THD + N)/S	total harmonic distortion plus noise-to-signal ratio	f_s = 44.1 kHz at input signal of 1 kHz; PGA gain = 0 dB; note 4				
		V_i (0 dB)	–	–85	–80	dB
		1.0 V (RMS)	–	0.0056	0.01	%
		V_i (–60 dB)	–	–30	–20	dB
			–	3.2	10.0	%
S/N	signal to noise ratio	V_i = 0.0 V	90	95	–	dBA
α_{ct}	crosstalk between channels	PGA gain = 0 dB	–	100	–	dB
f_s	sample frequency ($128f_s$)		0.640	–	7.04	MHz
OL	digital output level	PGA gain = 0 dB, V_i = 1 V (RMS)	–	–2.0	–	dBFS

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Filter stream DAC						
RES	resolution		16	–	–	bits
$V_{o(FS)(rms)}$	full-scale output voltage (RMS value)	V_{DD} = 3.3 V	–	0.66	–	V
SVRR	supply voltage ripple rejection at V_{DDA} and V_{DDO}	f_{ripple} = 1 kHz $V_{ripple(p-p)}$ = 0.1 V	–	60	–	dB
$\lvert\Delta V_o\rvert$	channel unbalance	maximum volume	–	0.03	–	dB
α_{ct}	crosstalk between channels	R_L = 5 kΩ	–	95	–	dB
(THD + N)/S	total harmonic distortion plus noise-to-signal ratio	f_s = 44.1 kHz; R_L = 5 kΩ; note 5				
		at input signal of 1 kHz (0 dB)	–	–90	–80	dB
			–	0.0032	0.01	%
		at input signal of 1 kHz (–60 dB)	–	–30	–20	dB
			–	3.2	10	%
S/N	signal-to-noise ratio at bipolar zero	A-weighting at code 0000H	90	95	–	dB

Notes

1. Strongly depends on the external decoupling capacitor connected to $V_{ref(DA)}$.
2. C_{ref} in μF.
3. Although a level of 1.414 V (RMS) would be required to optimal drive the ADC in this gain setting, this level can not be used. Due to the 3.3 V supply voltage input, signals of 1.17 V (RMS) and higher will result in clipping.
4. Measured with the APLL as ADC clock source.
5. Measured with I^2S-bus input as digital source.

APPLICATION INFORMATION

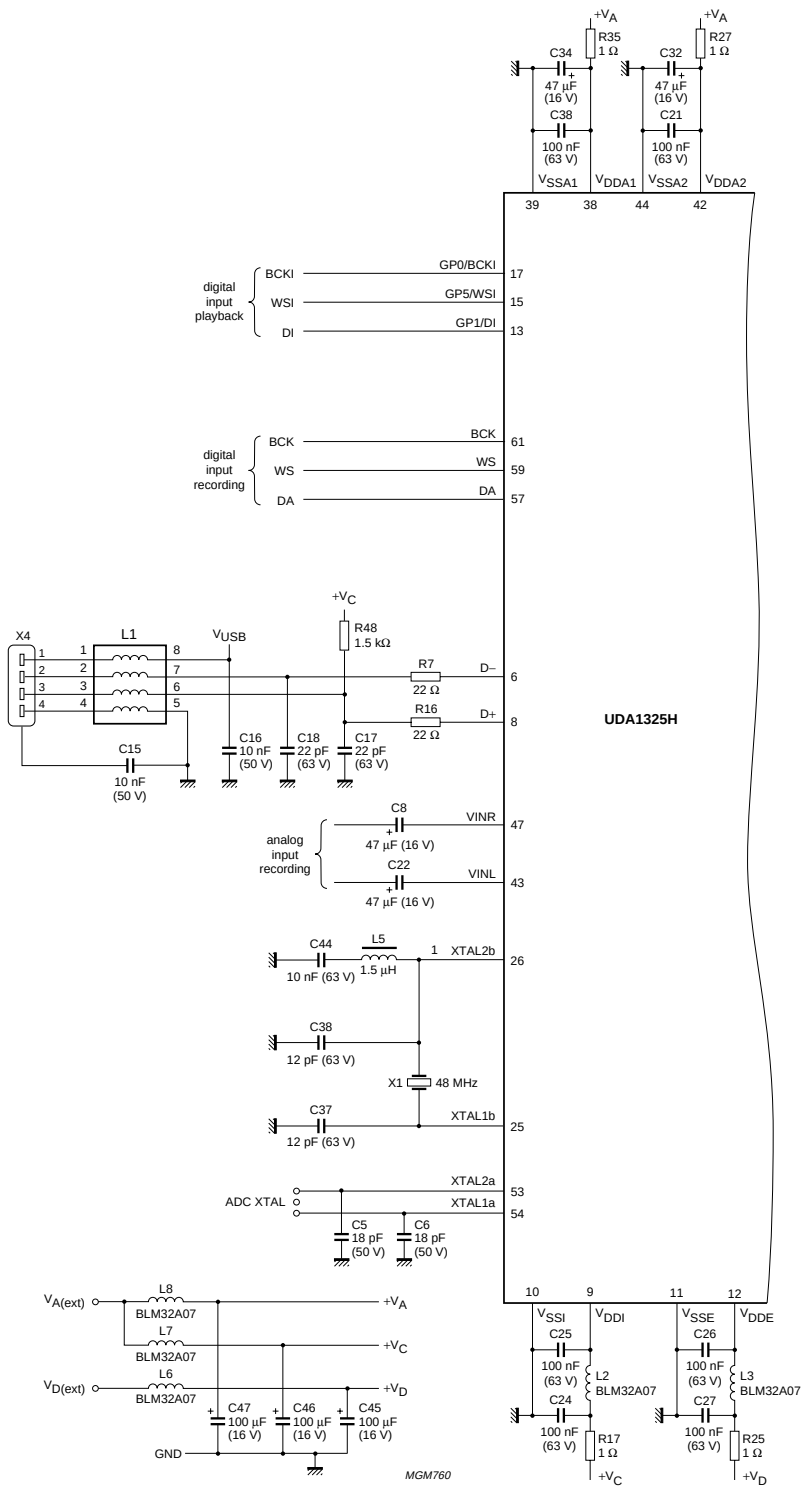


Fig.8 Application diagram UDA1325H (continued in Fig.9).

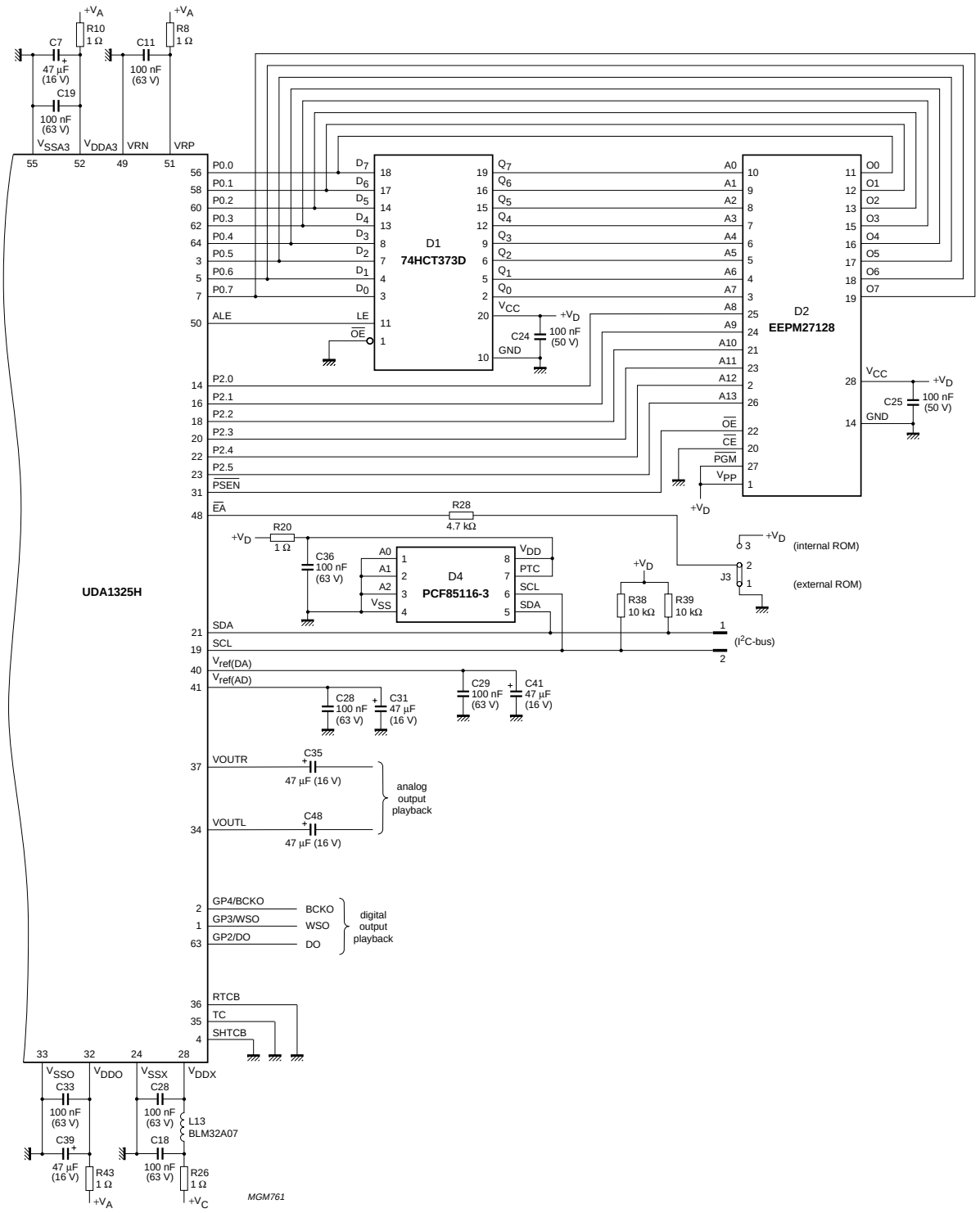


Fig.9 Application diagram UDA1325H (continued from Fig.8).

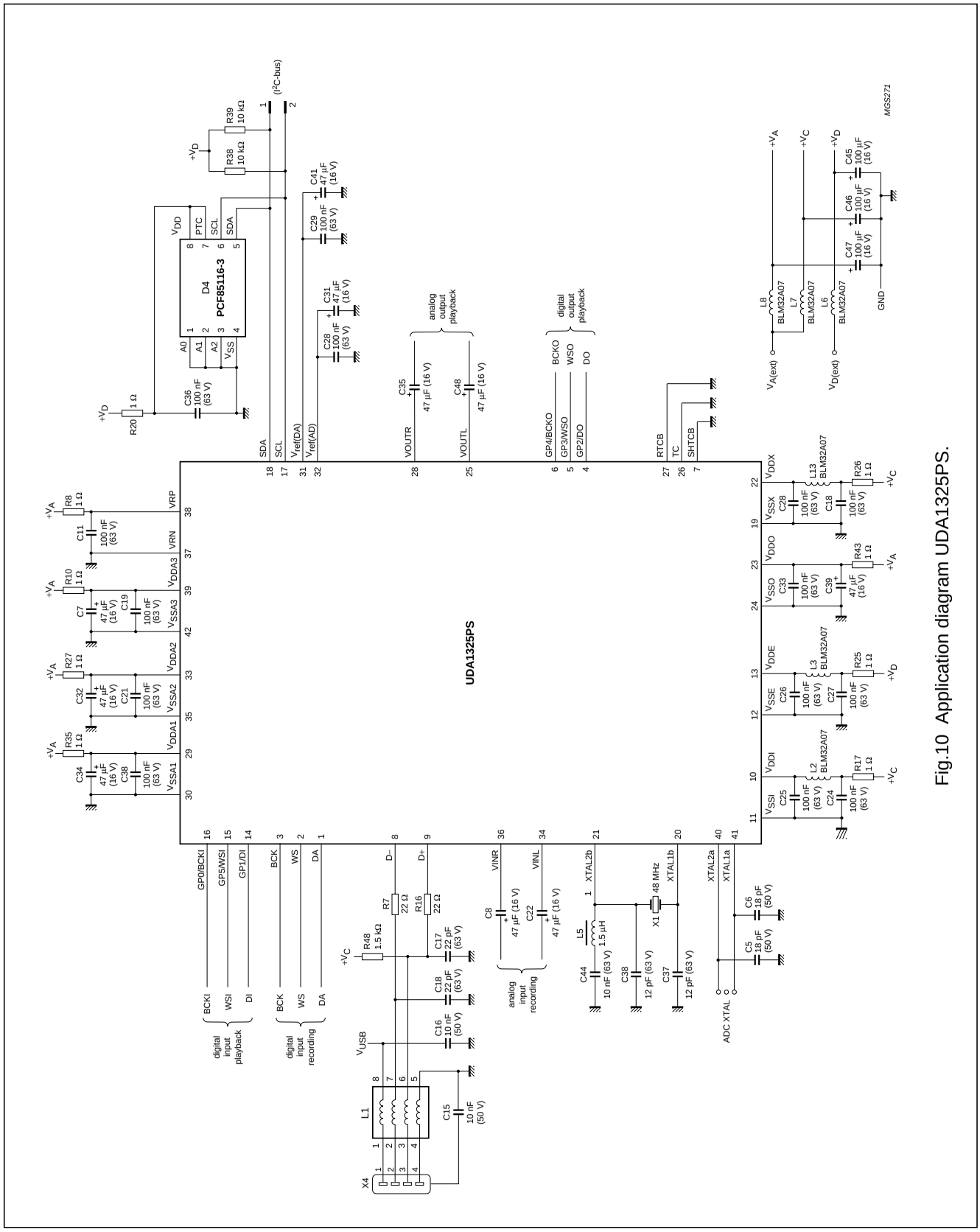
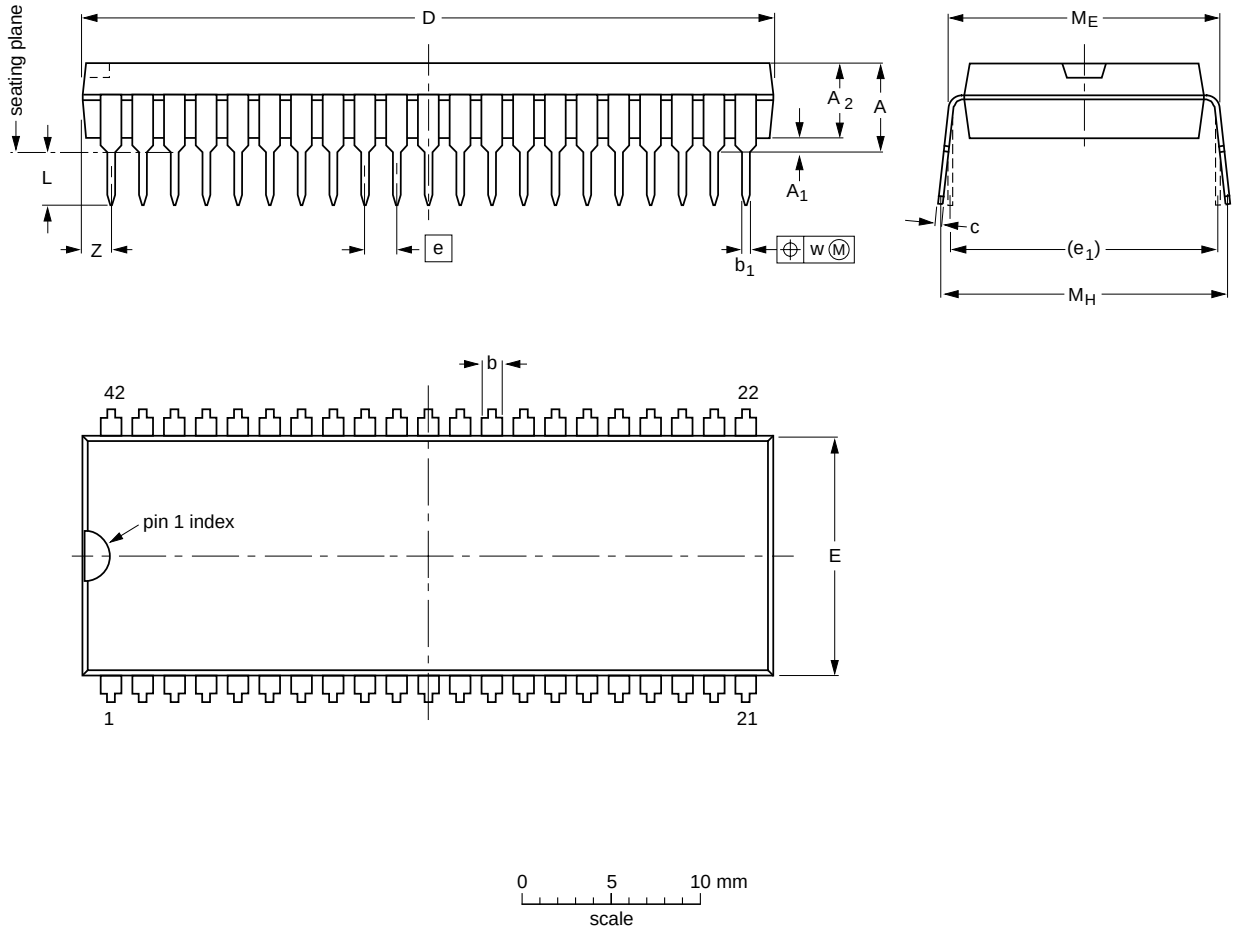


Fig.10 Application diagram UDA1325PS.

PACKAGE OUTLINES

SDIP42: plastic shrink dual in-line package; 42 leads (600 mil) **SOT270-1**



DIMENSIONS (mm are the original dimensions)

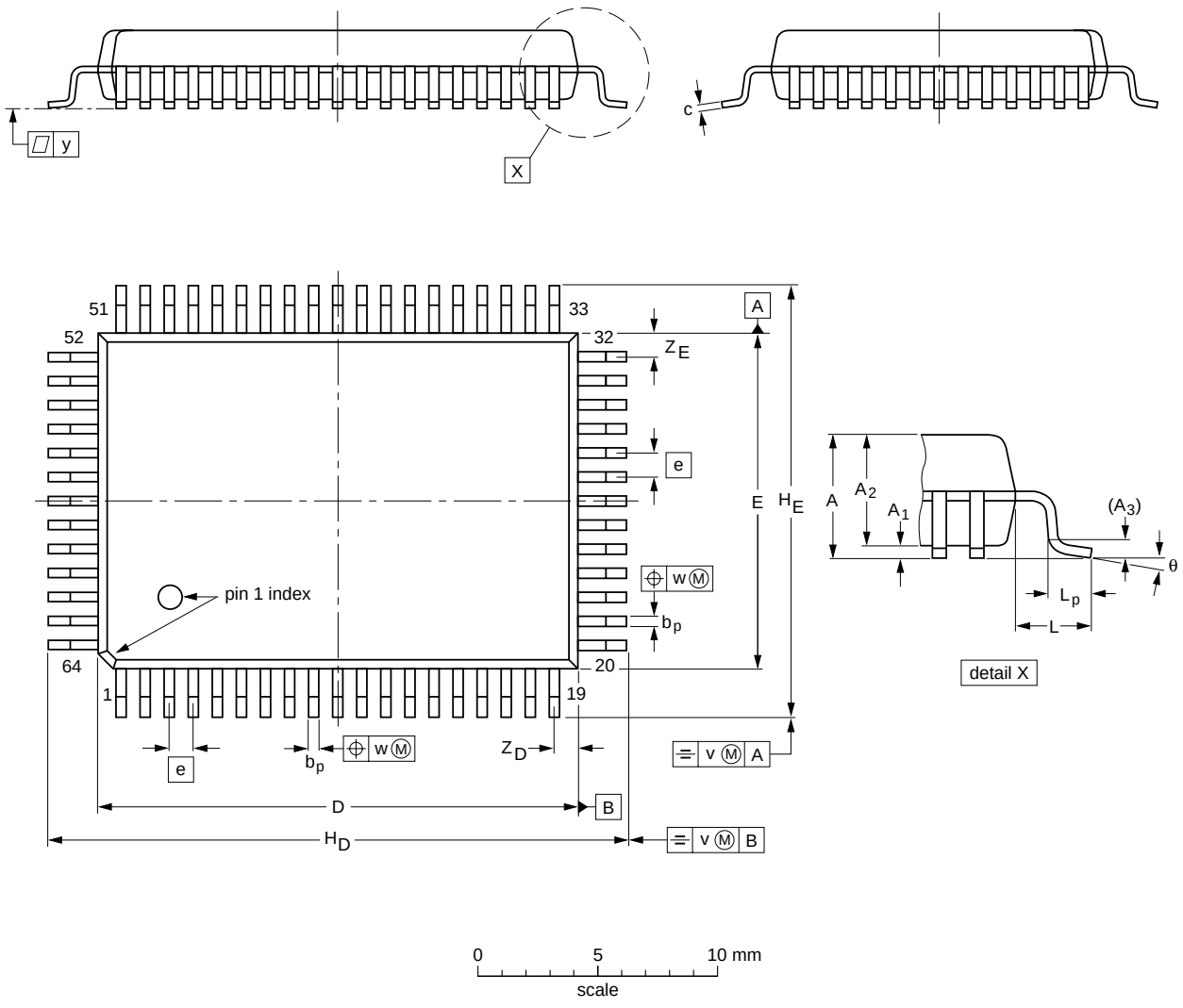
UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	5.08	0.51	4.0	1.3 0.8	0.53 0.40	0.32 0.23	38.9 38.4	14.0 13.7	1.778	15.24	3.2 2.9	15.80 15.24	17.15 15.90	0.18	1.73

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT270-1						~~90-02-13~~ 95-02-04

QFP64: plastic quad flat package; 64 leads (lead length 1.95 mm); body 14 x 20 x 2.8 mm **SOT319-2**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	3.20	0.25 0.05	2.90 2.65	0.25	0.50 0.35	0.25 0.14	20.1 19.9	14.1 13.9	1	24.2 23.6	18.2 17.6	1.95	1.0 0.6	0.2	0.2	0.1	1.2 0.8	1.2 0.8	7^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT319-2						~~95-02-04~~ 97-08-01

SOLDERING

Introduction

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mount components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mount ICs, or for printed-circuit boards with high population densities. In these situations reflow soldering is often used.

Through-hole mount packages

SOLDERING BY DIPPING OR BY SOLDER WAVE

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joints for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg(max)}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

MANUAL SOLDERING

Apply the soldering iron (24 V or less) to the lead(s) of the package, either below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

Surface mount packages

REFLOW SOLDERING

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, infrared/convection heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferable be kept below 230 °C.

WAVE SOLDERING

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.
A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

MANUAL SOLDERING

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

Suitability of IC packages for wave, reflow and dipping soldering methods

MOUNTING	PACKAGE	SOLDERING METHOD		
		WAVE	REFLOW(1)	DIPPING
Through-hole mount	DBS, DIP, HDIP, SDIP, SIL	suitable(2)	–	suitable
Surface mount	BGA, SQFP	not suitable	suitable	–
	HLQFP, HSQFP, HSOP, HTSSOP, SMS	not suitable(3)	suitable	–
	PLCC(4), SO, SOJ	suitable	suitable	–
	LQFP, QFP, TQFP	not recommended(4)(5)	suitable	–
	SSOP, TSSOP, VSO	not recommended(6)	suitable	–

Notes

1. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *"Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods"*.
2. For SDIP packages, the longitudinal axis must be parallel to the transport direction of the printed-circuit board.
3. These packages are not suitable for wave soldering as a solder joint between the printed-circuit board and heatsink (at bottom version) can not be achieved, and as solder may stick to the heatsink (on top version).
4. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
5. Wave soldering is only suitable for LQFP, QFP and TQFP packages with a pitch (e) equal to or larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
6. Wave soldering is only suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
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