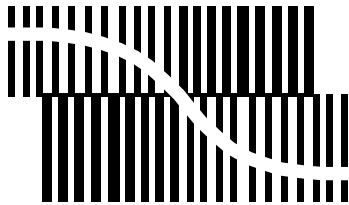


# DATA SHEET



BITSTREAM CONVERSION

## **UDA1334BT** Low power audio DAC

Product specification

2002 May 22

**Low power audio DAC****UDA1334BT**

|                 |   |                           |  |
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# Low power audio DAC

# UDA1334BT

## 1 FEATURES

### 1.1 General

- 1.8 to 3.6 V power supply voltage
- Integrated digital filter plus DAC
- Supports sample frequencies from 8 to 100 kHz
- Automatic system clock versus sample rate detection
- Low power consumption
- No analog post filtering required for DAC
- Slave mode only applications
- Easy application
- SO16 package.

### 1.2 Multiple format data interface

- I<sup>2</sup>S-bus and LSB-justified format compatible
- 1f<sub>s</sub> input data rate.

### 1.3 DAC digital sound processing

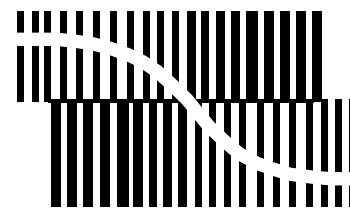
- Digital de-emphasis for 44.1 kHz sampling rate
- Mute function.

### 1.4 Advanced audio configuration

- High linearity, wide dynamic range and low distortion
- Standby or Sleep mode in which the DAC is powered down.

## 4 ORDERING INFORMATION

| TYPE NUMBER | PACKAGE |  |          |
|-------------|---------|--|----------|
|             | NAME    | DESCRIPTION  | VERSION  |
| UDA1334BT   | SO16    | plastic small outline package; 16 leads; body width 3.9 mm | SOT109-1 |



BITSTREAM CONVERSION

## 2 APPLICATIONS

This audio DAC is excellently suitable for digital audio portable application, such as portable MD, MP3 and DVD players.

## 3 GENERAL DESCRIPTION

The UDA1334BT supports the I<sup>2</sup>S-bus data format with word lengths of up to 24 bits and the LSB-justified serial data format with word lengths of 16, 20 and 24 bits.

The UDA1334BT has basic features such as de-emphasis (at 44.1 kHz sampling rate) and mute.

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5 QUICK REFERENCE DATA

| SYMBOL   | PARAMETER  | CONDITIONS                                       | MIN. | TYP. | MAX. | UNIT |
|--|--|--|------|------|------|------|
| <b>Supplies</b>  |  |  |      |      |      |      |
| V <sub>DDA</sub>   | DAC analog supply voltage                            |  | 1.8  | 2.0  | 3.6  | V    |
| V <sub>DDD</sub>   | digital supply voltage                               |  | 1.8  | 2.0  | 3.6  | V    |
| I <sub>DDA</sub>   | DAC analog supply current                            | normal operating mode                            | –    | 2.3  | –    | mA   |
|  |  | Sleep mode                                       | –    | 125  | –    | µA   |
| I <sub>DDD</sub>   | digital supply current                               | normal operating mode                            | –    | 1.4  | –    | mA   |
|  |  | Sleep mode                                       |      |      |      |      |
|  |  | clock running                                    | –    | 250  | –    | µA   |
|  |  | no clock running                                 | –    | 20   | –    | µA   |
| T <sub>amb</sub>   | ambient temperature                                  |  | –40  | –    | +85  | °C   |
| <b>Digital-to-analog converter (V<sub>DDA</sub> = V<sub>DDD</sub> = 2.0 V)</b> |  |  |      |      |      |      |
| V <sub>o(rms)</sub>  | output voltage (RMS value)                           | at 0 dB (FS) digital input; note 1               | –    | 600  | –    | mV   |
| (THD + N)/S  | total harmonic distortion-plus-noise to signal ratio | f <sub>s</sub> = 44.1 kHz; at 0 dB               | –    | –80  | –    | dB   |
|  |  | f <sub>s</sub> = 44.1 kHz; at –60 dB; A-weighted | –    | –37  | –    | dB   |
|  |  | f <sub>s</sub> = 96 kHz; at 0 dB                 | –    | –75  | –    | dB   |
|  |  | f <sub>s</sub> = 96 kHz; at –60 dB; A-weighted   | –    | –35  | –    | dB   |
| S/N  | signal-to-noise ratio                                | f <sub>s</sub> = 44.1 kHz; code = 0; A-weighted  | –    | 97   | –    | dB   |
|  |  | f <sub>s</sub> = 96 kHz; code = 0; A-weighted    | –    | 95   | –    | dB   |
| α <sub>CS</sub>  | channel separation                                   |  | –    | 100  | –    | dB   |
| <b>Digital-to-analog converter (V<sub>DDA</sub> = V<sub>DDD</sub> = 3.0 V)</b> |  |  |      |      |      |      |
| V <sub>o(rms)</sub>  | output voltage (RMS value)                           | at 0 dB (FS) digital input; note 1               | –    | 900  | –    | mV   |
| (THD + N)/S  | total harmonic distortion-plus-noise to signal ratio | f <sub>s</sub> = 44.1 kHz; at 0 dB               | –    | –90  | –    | dB   |
|  |  | f <sub>s</sub> = 44.1 kHz; at –60 dB; A-weighted | –    | –40  | –    | dB   |
|  |  | f <sub>s</sub> = 96 kHz; at 0 dB                 | –    | –85  | –    | dB   |
|  |  | f <sub>s</sub> = 96 kHz; at –60 dB; A-weighted   | –    | –37  | –    | dB   |
| S/N  | signal-to-noise ratio                                | f <sub>s</sub> = 44.1 kHz; code = 0; A-weighted  | –    | 100  | –    | dB   |
|  |  | f <sub>s</sub> = 96 kHz; code = 0; A-weighted    | –    | 98   | –    | dB   |
| α <sub>CS</sub>  | channel separation                                   |  | –    | 100  | –    | dB   |
| <b>Power dissipation (at f<sub>s</sub> = 44.1 kHz)</b>                         |  |  |      |      |      |      |
| P  | power dissipation                                    | playback mode                                    |      |      |      |      |
|  |  | at 2.0 V supply voltage                          | –    | 7.4  | –    | mW   |
|  |  | at 3.0 V supply voltage                          | –    | 17   | –    | mW   |
|  |  | Sleep mode; at 2.0 V supply voltage              |      |      |      |      |
|  |  | clock running                                    | –    | 0.75 | –    | mW   |
|  |  | no clock running                                 | –    | 0.3  | –    | mW   |

Note

1. The DAC output voltage scales proportionally to the power supply voltage.

Low power audio DAC

UDA1334BT

6 BLOCK DIAGRAM

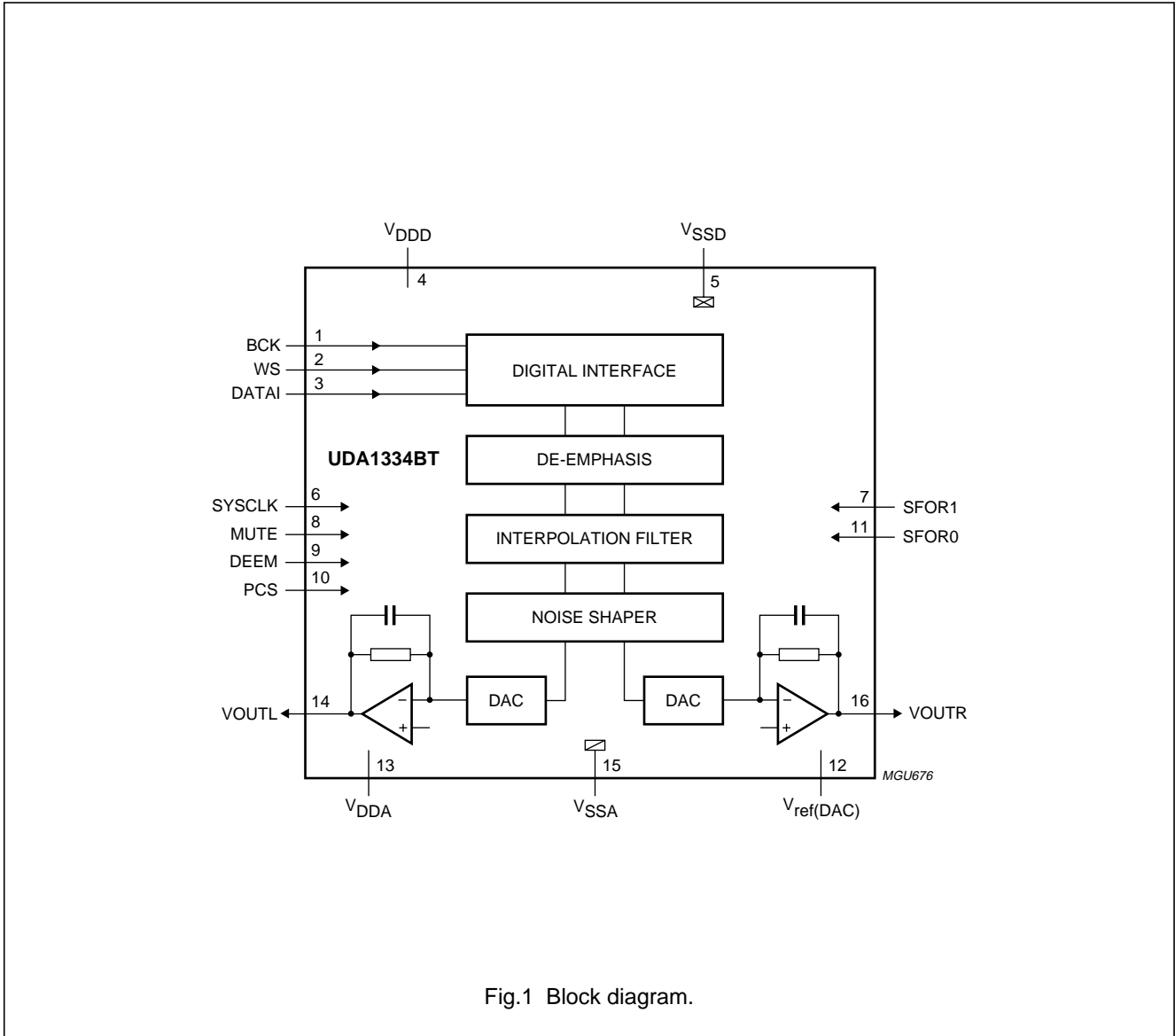


Fig.1 Block diagram.

## Low power audio DAC

## UDA1334BT

## 7 PINNING

| SYMBOL                | PIN | PAD TYPE                               | DESCRIPTION                                 |
|-----------------------|-----|--|---|
| BCK                   | 1   | 5 V tolerant digital input pad; note 1 | bit clock input                             |
| WS                    | 2   | 5 V tolerant digital input pad; note 1 | word select input                           |
| DATAI                 | 3   | 5 V tolerant digital input pad; note 1 | serial data input                           |
| V <sub>DDD</sub>      | 4   | digital supply pad                     | digital supply voltage                      |
| V <sub>SSD</sub>      | 5   | digital ground pad                     | digital ground                              |
| SYSCLK                | 6   | 5 V tolerant digital input pad; note 1 | system clock input                          |
| SFOR1                 | 7   | 5 V tolerant digital input pad; note 1 | serial format select 1                      |
| MUTE                  | 8   | 5 V tolerant digital input pad; note 1 | mute control                                |
| DEEM                  | 9   | 5 V tolerant digital input pad; note 1 | de-emphasis control                         |
| PCS                   | 10  | 3-level input pad; note 2              | power control and sampling frequency select |
| SFOR0                 | 11  | digital input pad; note 2              | serial format select 0                      |
| V <sub>ref(DAC)</sub> | 12  | analog pad                             | DAC reference voltage                       |
| V <sub>DDA</sub>      | 13  | analog supply pad                      | DAC analog supply voltage                   |
| VOUTL                 | 14  | analog output pad                      | DAC output left                             |
| V <sub>SSA</sub>      | 15  | analog ground pad                      | DAC analog ground                           |
| VOUTR                 | 16  | analog output pad                      | DAC output right                            |

## Notes

1. 5 V tolerant is only supported if the power supply voltage is between 2.7 and 3.6 V. For lower power supply voltages this is maximum 3.3 V tolerant.
2. Because of test issues these pads are not 5 V tolerant and they should be at power supply voltage level or at a maximum of 0.5 V above that level.

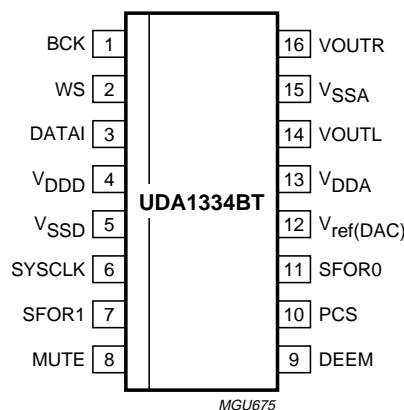


Fig.2 Pin configuration.

## Low power audio DAC

## UDA1334BT

**8 FUNCTIONAL DESCRIPTION****8.1 System clock**

The UDA1334BT operates in slave mode only; this means that in all applications the system must provide the system clock and the digital audio interface signals (BCK and WS).

The system clock must be locked in frequency to the digital interface signals.

The UDA1334BT automatically detects the ratio between the SYSCLK and WS frequencies.

The BCK clock can be up to  $64f_s$ , or in other words the BCK frequency is 64 times the Word Select (WS) frequency or less:  $f_{BCK} \leq 64 \times f_{WS}$ .

**Remarks:**

1. The WS edge MUST fall on the negative edge of the BCK at all times for proper operation of the digital I/O data interface
2. For LSB-justified formats it is important to have a WS signal with a duty factor of 50%.

The modes which are supported are given in Table 1.

**Table 1** Supported sampling ranges

| CLOCK MODE | SAMPLING RANGE                 |
|------------|--------------------------------|
| $768f_s$   | 8 to 55 kHz                    |
| $512f_s$   | 8 to 100 kHz                   |
| $384f_s$   | 8 to 100 kHz                   |
| $256f_s$   | 8 to 100 kHz                   |
| $192f_s$   | 8 to 100 kHz <sup>(1)(2)</sup> |
| $128f_s$   | 8 to 100 kHz <sup>(2)</sup>    |

**Notes**

1. This mode can only be supported for power supply voltages down to 2.4 V. For lower voltages, in  $192f_s$  mode the sampling frequency should be limited to 55 kHz.
2. Not supported in the low sampling frequency mode.

An example is given in Table 2 for a 12.228 MHz system clock input.

**Table 2** Example using a 12.228 MHz system clock

| CLOCK MODE | SAMPLING FREQUENCY    |
|------------|-----------------------|
| $128f_s$   | 96 kHz                |
| $192f_s$   | 64 kHz <sup>(1)</sup> |
| $256f_s$   | 48 kHz                |
| $384f_s$   | 32 kHz                |
| $512f_s$   | 24 kHz                |
| $768f_s$   | 16 kHz                |

**Note**

1. This mode can only be supported for power supply voltages down to 2.4 V. For lower voltages, in  $192f_s$  mode the sampling frequency should be limited to 55 kHz.

**8.2 Interpolation filter**

The interpolation digital filter interpolates from  $1f_s$  to  $64f_s$  by cascading FIR filters (see Table 3).

**Table 3** Interpolation filter characteristics

| ITEM             | CONDITION      | VALUE (dB) |
|------------------|----------------|------------|
| Pass-band ripple | 0 to $0.45f_s$ | $\pm 0.02$ |
| Stop band        | $>0.55f_s$     | -50        |
| Dynamic range    | 0 to $0.45f_s$ | $>114$     |

**8.3 Noise shaper**

The 5th-order noise shaper operates at  $64f_s$ . It shifts in-band quantization noise to frequencies well above the audio band. This noise shaping technique enables high signal-to-noise ratios to be achieved. The noise shaper output is converted into an analog signal using a Filter Stream DAC (FSDAC).

# Low power audio DAC

# UDA1334BT

### 8.4 Filter stream DAC

The FSDAC is a semi-digital reconstruction filter that converts the 1-bit data stream of the noise shaper to an analog output voltage. The filter coefficients are implemented as current sources and are summed at virtual ground of the output operational amplifier. In this way very high signal-to-noise performance and low clock jitter sensitivity is achieved. No post-filter is needed due to the inherent filter function of the DAC. On-board amplifiers convert the FSDAC output current to an output voltage signal capable of driving a line output.

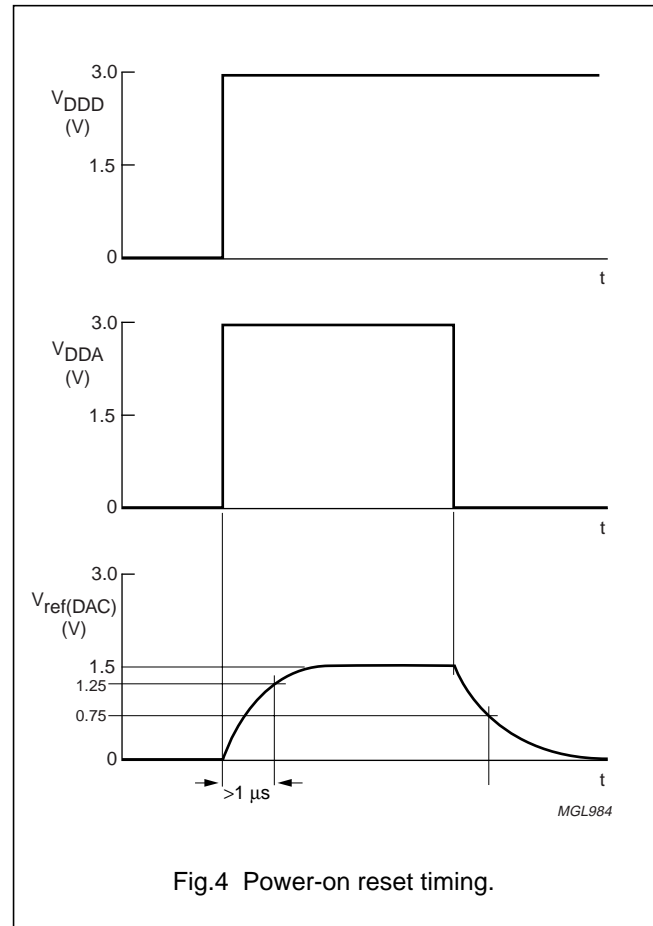
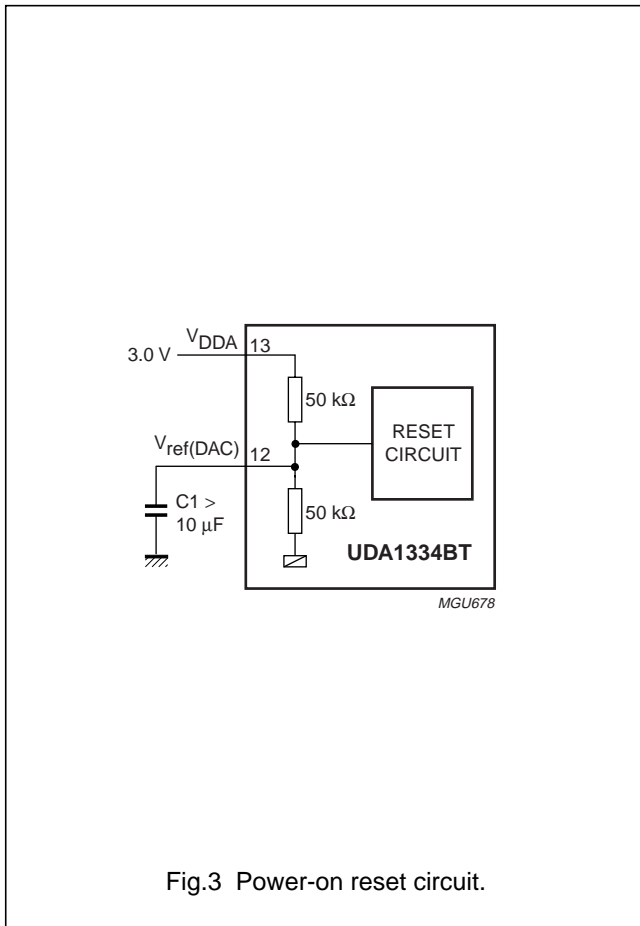
The output voltage of the FSDAC scales proportionally with the power supply voltage.

### 8.5 Power-on reset

The UDA1334BT has an internal Power-on reset circuit (see Fig.3) which resets the test control block.

The reset time (see Fig.4) is determined by an external capacitor which is connected between pin  $V_{ref(DAC)}$  and ground. The reset time should be at least  $1 \mu s$  for  $V_{ref(DAC)} < 1.25 V$ . When  $V_{DDA}$  is switched off, the device will be reset again for  $V_{ref(DAC)} < 0.75 V$ .

During the reset time the system clock should be running.





# Low power audio DAC

# UDA1334BT

## 8.6 Feature settings

The features of the UDA1334BT can be set by control pins SFOR1, SFOR0, MUTE, DEEM and PCS.

### 8.6.1 DIGITAL INTERFACE FORMAT SELECT

The digital audio interface formats (see Fig.5) can be selected via the pins SFOR1 and SFOR0 as shown in Table 4.

**Table 4** Data format selection

| SFOR1 | SFOR0 | INPUT FORMAT                |
|-------|-------|-----------------------------|
| LOW   | LOW   | I <sup>2</sup> S-bus input  |
| LOW   | HIGH  | LSB-justified 16 bits input |
| HIGH  | LOW   | LSB-justified 20 bits input |
| HIGH  | HIGH  | LSB-justified 24 bits input |

### 8.6.2 MUTE CONTROL

The output signal can be soft muted by setting pin MUTE to HIGH level as shown in Table 5.

**Table 5** Mute control

| MUTE | FUNCTION |
|------|----------|
| LOW  | mute off |
| HIGH | mute on  |

### 8.6.3 DE-EMPHASIS CONTROL

De-emphasis can be switched on for  $f_s = 44.1$  kHz by setting pin DEEM at HIGH level. The function description of pin DEEM is given in Table 6.

**Table 6** De-emphasis control

| DEEM | FUNCTION        |
|------|-----------------|
| LOW  | de-emphasis off |
| HIGH | de-emphasis on  |

**Remark:** the de-emphasis function is only supported in the normal operating mode, not in the low sampling frequency mode.

### 8.6.4 POWER CONTROL AND SAMPLING FREQUENCY SELECT

Pin PCS is a 3-level pin and is used to set the mode of the UDA1334BT. The definition is given in Table 7.

**Table 7** PCS function definition

| PCS  | FUNCTION                    |
|------|-----------------------------|
| LOW  | normal operating mode       |
| MID  | low sampling frequency mode |
| HIGH | Power-down or Sleep mode    |

The low sampling frequency mode is required to have a higher oversampling rate in the noise shaper in order to improve the signal-to-noise ratio. In this mode the oversampling ratio of the noise shaper will be  $128f_s$  instead of  $64f_s$ .

# Low power audio DAC

## UDA1334BT

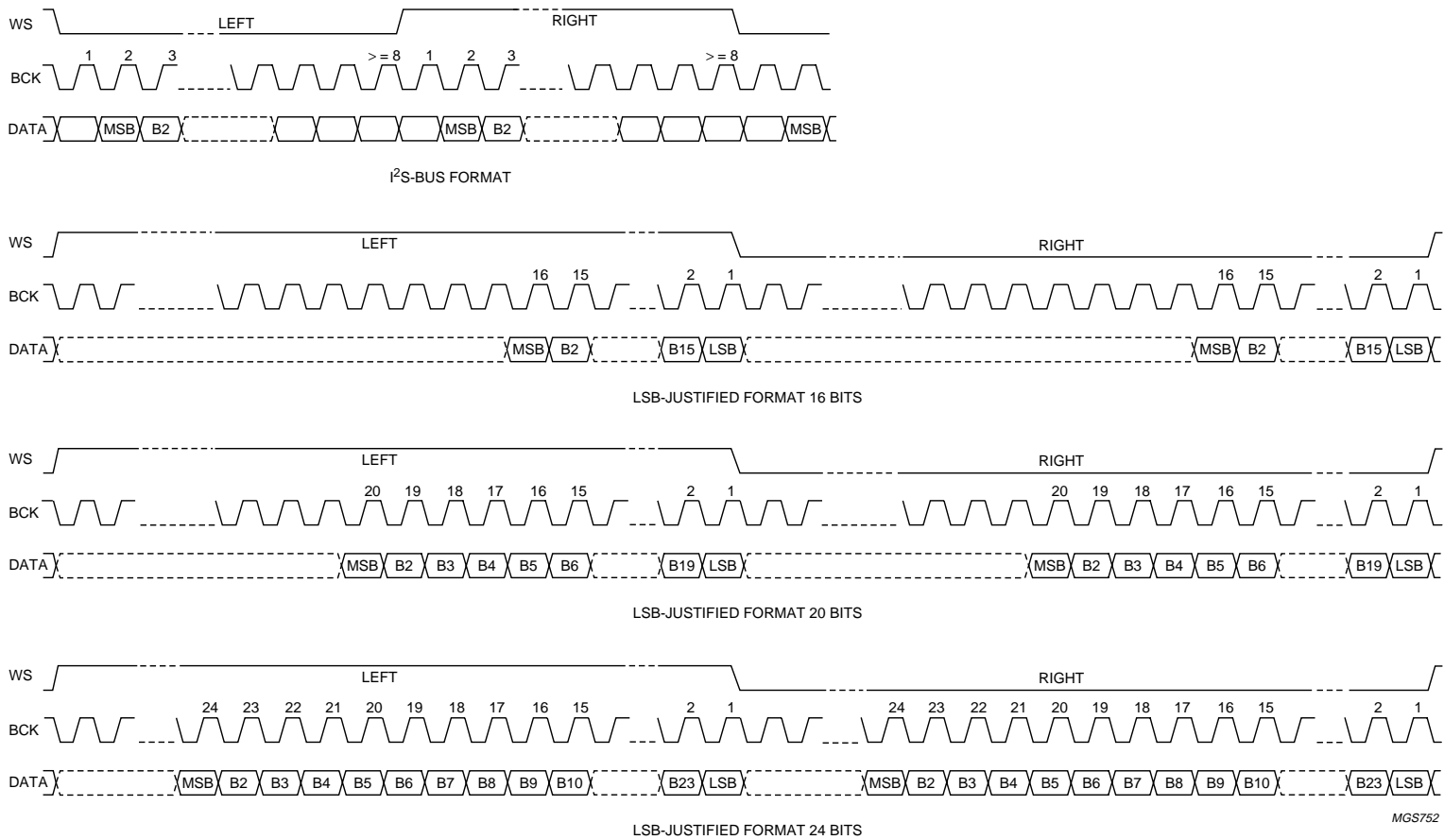


Fig.5 Digital audio formats

## Low power audio DAC

## UDA1334BT

**9 LIMITING VALUES**

In accordance with the Absolute Maximum Rating System (IEC 60134).

| SYMBOL          | PARAMETER                      | CONDITIONS                          | MIN.  | MAX.  | UNIT |
|-----------------|--------------------------------|-------------------------------------|-------|-------|------|
| $V_{DD}$        | supply voltage                 | note 1                              | –     | 4.0   | V    |
| $T_{xtal(max)}$ | maximum crystal temperature    |                                     | –     | 150   | °C   |
| $T_{stg}$       | storage temperature            |                                     | –65   | +125  | °C   |
| $T_{amb}$       | ambient temperature            |                                     | –40   | +85   | °C   |
| $V_{es}$        | electrostatic handling voltage | human body model                    | –2000 | +2000 | V    |
|                 |                                | machine model                       | –200  | +200  | V    |
| $I_{sc(DAC)}$   | short-circuit current of DAC   | note 2                              |       |       |      |
|                 |                                | output short-circuited to $V_{SSA}$ | –     | 450   | mA   |
|                 |                                | output short-circuited to $V_{DDA}$ | –     | 300   | mA   |

**Note**

- All supply connections must be made to the same power supply.
- Short-circuit test at  $T_{amb} = 0\text{ °C}$  and  $V_{DDA} = 3\text{ V}$ . DAC operation after short-circuiting cannot be warranted.

**10 HANDLING**

Inputs and outputs are protected against electrostatic discharge in normal handling. However, it is good practice to take normal precautions appropriate to handling MOS devices.

**11 THERMAL CHARACTERISTICS**

| SYMBOL        | PARAMETER                                   | CONDITIONS  | VALUE | UNIT |
|---------------|---|-------------|-------|------|
| $R_{th(j-a)}$ | thermal resistance from junction to ambient | in free air | 145   | K/W  |

**12 QUALITY SPECIFICATION**

In accordance with “SNW-FQ-611-D”.

**13 DC CHARACTERISTICS**

$V_{DDD} = V_{DDA} = 2.0\text{ V}$ ;  $T_{amb} = 25\text{ °C}$ ;  $R_L = 5\text{ k}\Omega$ ; all voltages with respect to ground (pins  $V_{SSA}$  and  $V_{SSD}$ ); unless otherwise specified.

| SYMBOL          | PARAMETER                 | CONDITIONS              | MIN. | TYP. | MAX. | UNIT          |
|-----------------|---------------------------|-------------------------|------|------|------|---------------|
| <b>Supplies</b> |                           |                         |      |      |      |               |
| $V_{DDA}$       | DAC analog supply voltage | note 1                  | 1.8  | 2.0  | 3.6  | V             |
| $V_{DDD}$       | digital supply voltage    | note 1                  | 1.8  | 2.0  | 3.6  | V             |
| $I_{DDA}$       | DAC analog supply current | normal operating mode   |      |      |      |               |
|                 |                           | at 2.0 V supply voltage | –    | 2.3  | –    | mA            |
|                 |                           | at 3.0 V supply voltage | –    | 3.5  | –    | mA            |
|                 |                           | Sleep mode              |      |      |      |               |
|                 |                           | at 2.0 V supply voltage | –    | 125  | –    | $\mu\text{A}$ |
|                 |                           | at 3.0 V supply voltage | –    | 175  | –    | $\mu\text{A}$ |

## Low power audio DAC

## UDA1334BT

| SYMBOL                            | PARAMETER                                      | CONDITIONS                                    | MIN.                 | TYP.                | MAX.                   | UNIT |  |
|-----------------------------------|--|---|----------------------|---------------------|------------------------|------|--|
| I <sub>DDD</sub>                  | digital supply current                         | normal operating mode                         |                      |                     |                        |      |  |
|                                   |  | at 2.0 V supply voltage                       | –                    | 1.4                 | –                      | mA   |  |
|                                   |  | at 3.0 V supply voltage                       | –                    | 2.1                 | –                      | mA   |  |
|                                   |  | Sleep mode;                                   |                      |                     |                        |      |  |
|                                   |  | at 2.0 V supply voltage                       |                      |                     |                        |      |  |
|                                   |  | clock running                                 | –                    | 250                 | –                      | μA   |  |
| no clock running                  | –  | 20  | –                    | μA                  |                        |      |  |
| Sleep mode;                       | at 3.0 V supply voltage                        | clock running                                 | –                    | 375                 | –                      | μA   |  |
|                                   |  | no clock running                              | –                    | 30                  | –                      | μA   |  |
| <b>Digital input pins; note 2</b> |  |   |                      |                     |                        |      |  |
| V <sub>IH</sub>                   | HIGH-level input voltage                       | at 2.0 V supply voltage                       | 1.3                  | –                   | 3.3                    | V    |  |
|                                   |  | at 3.0 V supply voltage                       | 2.0                  | –                   | 5.0                    | V    |  |
| V <sub>IL</sub>                   | LOW-level input voltage                        | at 2.0 V supply voltage                       | –0.5                 | –                   | +0.5                   | V    |  |
|                                   |  | at 3.0 V supply voltage                       | –0.5                 | –                   | +0.8                   | V    |  |
| I <sub>LI</sub>                   | input leakage current                          |   | –                    | –                   | 1                      | μA   |  |
| C <sub>i</sub>                    | input capacitance                              |   | –                    | –                   | 10                     | pF   |  |
| <b>3-level input: pin PCS</b>     |  |   |                      |                     |                        |      |  |
| V <sub>IH</sub>                   | HIGH-level input voltage                       |   | 0.9V <sub>DDD</sub>  | –                   | V <sub>DDD</sub> + 0.5 | V    |  |
| V <sub>IM</sub>                   | MID-level input voltage                        |   | 0.4V <sub>DDD</sub>  | –                   | 0.6V <sub>DDD</sub>    | V    |  |
| V <sub>IL</sub>                   | LOW-level input voltage                        |   | –0.5                 | –                   | +0.5                   | V    |  |
| <b>DAC</b>                        |  |   |                      |                     |                        |      |  |
| V <sub>ref(DAC)</sub>             | reference voltage                              | with respect to V <sub>SSA</sub>              | 0.45V <sub>DDA</sub> | 0.5V <sub>DDA</sub> | 0.55V <sub>DDA</sub>   | V    |  |
| R <sub>o(ref)</sub>               | output resistance on pin V <sub>ref(DAC)</sub> |   | –                    | 25                  | –                      | kΩ   |  |
| I <sub>o(max)</sub>               | maximum output current                         | (THD + N)/S < 0.1%;<br>R <sub>L</sub> = 800 Ω | –                    | 1.6                 | –                      | mA   |  |
| R <sub>L</sub>                    | load resistance                                |   | 3                    | –                   | –                      | kΩ   |  |
| C <sub>L</sub>                    | load capacitance                               | note 3  | –                    | –                   | 50                     | pF   |  |

**Notes**

1. All supply connections must be made to the same external power supply unit.
2. At 3 V supply voltage, the input pads are TTL compatible. However, at 2.0 V supply voltage no TTL levels can be accepted, but levels from 3.3 V domain can be applied to the pins.
3. When the DAC drives a capacitive load above 50 pF, a series resistance of 100 Ω must be used to prevent oscillations in the output operational amplifier.

## Low power audio DAC

## UDA1334BT

**14 AC CHARACTERISTICS****14.1 2.0 V supply voltage**

$V_{DD} = V_{DDA} = 2.0$  V;  $f_i = 1$  kHz;  $T_{amb} = 25$  °C;  $R_L = 5$  k $\Omega$ .; all voltages with respect to ground (pins  $V_{SSA}$  and  $V_{SSD}$ ); unless otherwise specified.

| SYMBOL        | PARAMETER  | CONDITIONS                                       | MIN. | TYP. | MAX. | UNIT |
|---------------|--|--|------|------|------|------|
| <b>DAC</b>    |  |  |      |      |      |      |
| $V_{o(rms)}$  | output voltage (RMS value)                           | at 0 dB (FS) digital input                       | –    | 600  | –    | mV   |
| $\Delta V_o$  | unbalance between channels                           |  | –    | 0.1  | –    | dB   |
| (THD + N)/S   | total harmonic distortion-plus-noise to signal ratio | $f_s = 44.1$ kHz; at 0 dB                        | –    | –80  | –    | dB   |
|               |  | $f_s = 44.1$ kHz; at –60 dB; A-weighted          | –    | –37  | –    | dB   |
|               |  | $f_s = 96$ kHz; at 0 dB                          | –    | –75  | –    | dB   |
|               |  | $f_s = 96$ kHz; at –60 dB; A-weighted            | –    | –35  | –    | dB   |
| S/N           | signal-to-noise ratio                                | $f_s = 44.1$ kHz; code = 0; A-weighted           | –    | 97   | –    | dB   |
|               |  | $f_s = 96$ kHz; code = 0; A-weighted             | –    | 95   | –    | dB   |
| $\alpha_{cs}$ | channel separation                                   |  | –    | 100  | –    | dB   |
| PSRR          | power supply rejection ratio                         | $f_{ripple} = 1$ kHz; $V_{ripple} = 30$ mV (p-p) | –    | 60   | –    | dB   |

**14.2 3.0 V supply voltage**

$V_{DD} = V_{DDA} = 3.0$  V;  $f_i = 1$  kHz;  $T_{amb} = 25$  °C;  $R_L = 5$  k $\Omega$ .; all voltages with respect to ground (pins  $V_{SSA}$  and  $V_{SSD}$ ); unless otherwise specified.

| SYMBOL        | PARAMETER  | CONDITIONS                                       | MIN. | TYP. | MAX. | UNIT |
|---------------|--|--|------|------|------|------|
| <b>DAC</b>    |  |  |      |      |      |      |
| $V_{o(rms)}$  | output voltage (RMS value)                           | at 0 dB (FS) digital input                       | –    | 900  | –    | mV   |
| $\Delta V_o$  | unbalance between channels                           |  | –    | 0.1  | –    | dB   |
| (THD + N)/S   | total harmonic distortion-plus-noise to signal ratio | $f_s = 44.1$ kHz; at 0 dB                        | –    | –90  | –    | dB   |
|               |  | $f_s = 44.1$ kHz; at –60 dB; A-weighted          | –    | –40  | –    | dB   |
|               |  | $f_s = 96$ kHz; at 0 dB                          | –    | –85  | –    | dB   |
|               |  | $f_s = 96$ kHz; at –60 dB; A-weighted            | –    | –37  | –    | dB   |
| S/N           | signal-to-noise ratio                                | $f_s = 44.1$ kHz; code = 0; A-weighted           | –    | 100  | –    | dB   |
|               |  | $f_s = 96$ kHz; code = 0; A-weighted             | –    | 98   | –    | dB   |
| $\alpha_{cs}$ | channel separation                                   |  | –    | 100  | –    | dB   |
| PSRR          | power supply rejection ratio                         | $f_{ripple} = 1$ kHz; $V_{ripple} = 30$ mV (p-p) | –    | 60   | –    | dB   |

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**14.3 Timing**

$V_{DD} = V_{DDA} = 1.8$  to  $3.6$  V;  $T_{amb} = -20$  to  $+85$  °C;  $R_L = 5$  k $\Omega$ ; all voltages with respect to ground (pins  $V_{SSA}$  and  $V_{SSD}$ ); unless otherwise specified; note 1.

| SYMBOL                                     | PARAMETER               | CONDITIONS              | MIN.         | TYP. | MAX.         | UNIT    |
|--|-------------------------|-------------------------|--------------|------|--------------|---------|
| <b>System clock timing</b> (see Fig.6)     |                         |                         |              |      |              |         |
| $T_{sys}$                                  | system clock cycle time | $f_{sys} = 256f_s$      | 35           | 88   | 780          | ns      |
|  |                         | $f_{sys} = 384f_s$      | 23           | 59   | 520          | ns      |
|  |                         | $f_{sys} = 512f_s$      | 17           | 44   | 390          | ns      |
| $t_{CWH}$                                  | system clock HIGH time  | $f_{sys} < 19.2$ MHz    | $0.3T_{sys}$ | –    | $0.7T_{sys}$ | ns      |
|  |                         | $f_{sys} \geq 19.2$ MHz | $0.4T_{sys}$ | –    | $0.6T_{sys}$ | ns      |
| $t_{CWL}$                                  | system clock LOW time   | $f_{sys} < 19.2$ MHz    | $0.3T_{sys}$ | –    | $0.7T_{sys}$ | ns      |
|  |                         | $f_{sys} \geq 19.2$ MHz | $0.4T_{sys}$ | –    | $0.6T_{sys}$ | ns      |
| <b>Reset timing</b>                        |                         |                         |              |      |              |         |
| $t_{reset}$                                | reset time              |                         | 1            | –    | –            | $\mu$ s |
| <b>Serial interface timing</b> (see Fig.7) |                         |                         |              |      |              |         |
| $f_{BCK}$                                  | bit clock frequency     |                         | –            | –    | $64f_s$      | Hz      |
| $t_{BCKH}$                                 | bit clock HIGH time     |                         | 50           | –    | –            | ns      |
| $t_{BCKL}$                                 | bit clock LOW time      |                         | 50           | –    | –            | ns      |
| $t_r$                                      | rise time               |                         | –            | –    | 20           | ns      |
| $t_f$                                      | fall time               |                         | –            | –    | 20           | ns      |
| $t_{su}(DATAI)$                            | set-up time data input  |                         | 20           | –    | –            | ns      |
| $t_h(DATAI)$                               | hold time data input    |                         | 0            | –    | –            | ns      |
| $t_{su}(WS)$                               | set-up time word select |                         | 20           | –    | –            | ns      |
| $t_h(WS)$                                  | hold time word select   |                         | 10           | –    | –            | ns      |

**Note**

1. The typical value of the timing is specified at  $f_s = 44.1$  kHz (sampling frequency).

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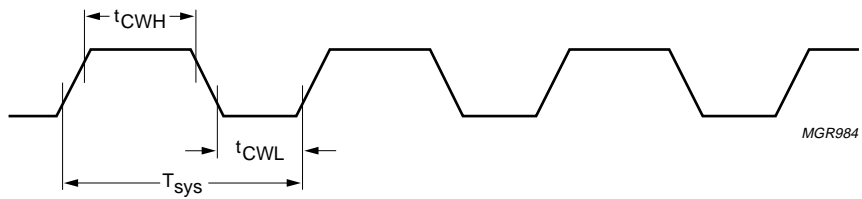


Fig.6 System clock timing.

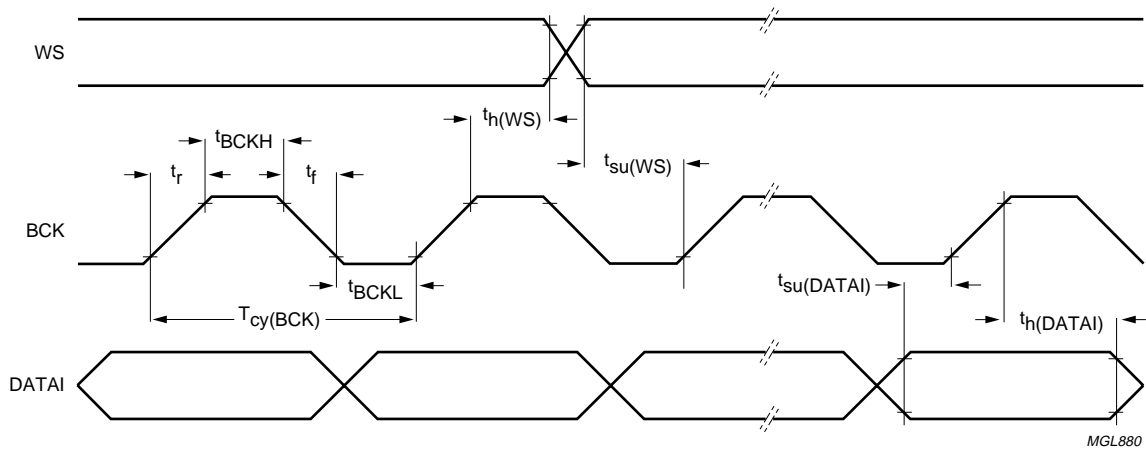


Fig.7 Serial interface timing.

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15 APPLICATION INFORMATION

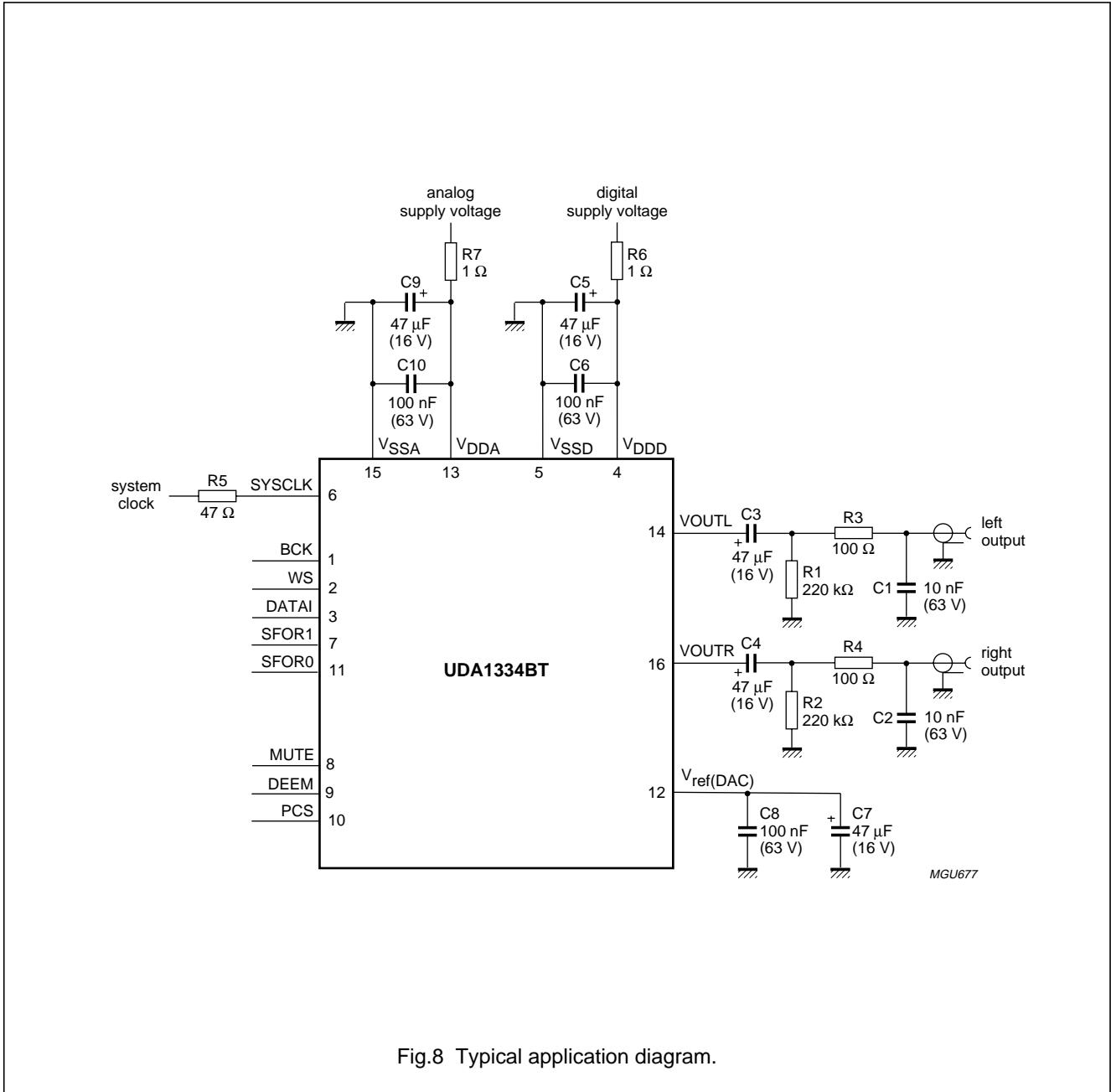


Fig.8 Typical application diagram.



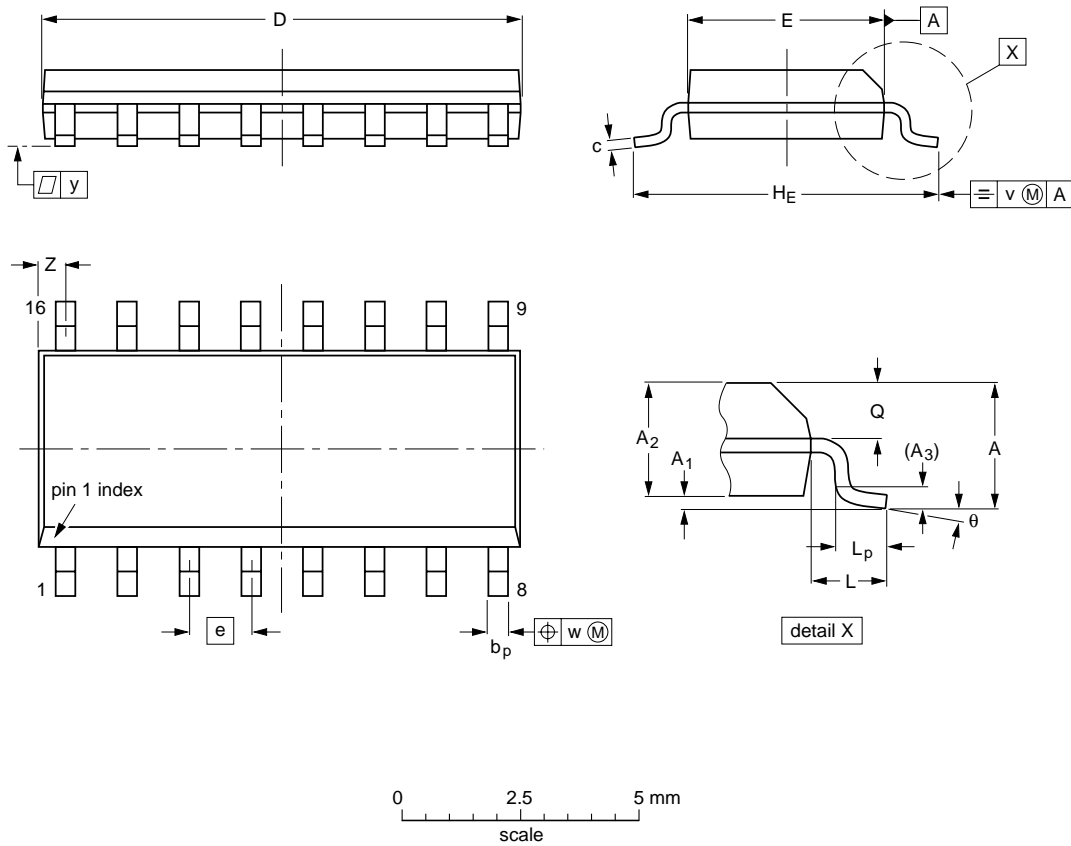
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16 PACKAGE OUTLINE

SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

| UNIT   | A max. | A <sub>1</sub> | A <sub>2</sub> | A <sub>3</sub> | b <sub>p</sub> | c                | D <sup>(1)</sup> | E <sup>(1)</sup> | e     | H <sub>E</sub> | L     | L <sub>p</sub> | Q              | v    | w    | y     | Z <sup>(1)</sup> | θ        |
|--------|--------|----------------|----------------|----------------|----------------|------------------|------------------|------------------|-------|----------------|-------|----------------|----------------|------|------|-------|------------------|----------|
| mm     | 1.75   | 0.25<br>0.10   | 1.45<br>1.25   | 0.25           | 0.49<br>0.36   | 0.25<br>0.19     | 10.0<br>9.8      | 4.0<br>3.8       | 1.27  | 6.2<br>5.8     | 1.05  | 1.0<br>0.4     | 0.7<br>0.6     | 0.25 | 0.25 | 0.1   | 0.7<br>0.3       | 8°<br>0° |
| inches | 0.069  | 0.010<br>0.004 | 0.057<br>0.049 | 0.01           | 0.019<br>0.014 | 0.0100<br>0.0075 | 0.39<br>0.38     | 0.16<br>0.15     | 0.050 | 0.244<br>0.228 | 0.041 | 0.039<br>0.016 | 0.028<br>0.020 | 0.01 | 0.01 | 0.004 | 0.028<br>0.012   |          |

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES |        |      | EUROPEAN PROJECTION | ISSUE DATE            |
|-----------------|------------|--------|------|---------------------|-----------------------|
|                 | IEC        | JEDEC  | EIAJ |                     |                       |
| SOT109-1        | 076E07     | MS-012 |      |                     | 97-05-22-<br>99-12-27 |

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### 17 SOLDERING

#### 17.1 Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

#### 17.2 Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferably be kept below 220 °C for thick/large packages, and below 235 °C for small/thin packages.

#### 17.3 Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

The footprint must incorporate solder thieves at the downstream end.

- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

#### 17.4 Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

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## 17.5 Suitability of surface mount IC packages for wave and reflow soldering methods

| PACKAGE <sup>(1)</sup>   | SOLDERING METHOD                  |                       |
|--|-----------------------------------|-----------------------|
|  | WAVE                              | REFLOW <sup>(2)</sup> |
| BGA, LBGA, LFBGA, SQFP, TFBGA, VFBGA                             | not suitable                      | suitable              |
| HBCC, HBGA, HLQFP, HSQFP, HSOP, HTQFP, HTSSOP, HVQFN, HVSON, SMS | not suitable <sup>(3)</sup>       | suitable              |
| PLCC <sup>(4)</sup> , SO, SOJ                                    | suitable                          | suitable              |
| LQFP, QFP, TQFP  | not recommended <sup>(4)(5)</sup> | suitable              |
| SSOP, TSSOP, VSO   | not recommended <sup>(6)</sup>    | suitable              |

**Notes**

1. For more detailed information on the BGA packages refer to the “(LF)BGA Application Note” (AN01026); order a copy from your Philips Semiconductors sales office.
2. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the “Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods”.
3. These packages are not suitable for wave soldering. On versions with the heatsink on the bottom side, the solder cannot penetrate between the printed-circuit board and the heatsink. On versions with the heatsink on the top side, the solder might be deposited on the heatsink surface.
4. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
5. Wave soldering is suitable for LQFP, TQFP and QFP packages with a pitch (e) larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
6. Wave soldering is suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

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18 DATA SHEET STATUS

| DATA SHEET STATUS <sup>(1)</sup> | PRODUCT STATUS <sup>(2)</sup> | DEFINITIONS  |
|----------------------------------|-------------------------------|--|
| Objective data                   | Development                   | This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.  |
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Notes

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2. The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL <http://www.semiconductors.philips.com>.

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