DATA SHEET

TDA1561Q
2 × 23 W high efficiency car radio power amplifier

Preliminary specification
Supersedes data of 1997 Jun 11
File under Integrated Circuits, IC01

1997 Aug 14

Philips
Semiconductors

PHILIPS

2 × 23 W high efficiency car radio power amplifier

TDA1561Q

FEATURES

- Low dissipation due to switching from Single-Ended (SE) to Bridge-Tied Load (BTL) mode
- High Common Mode Rejection Ratio (CMRR)
- Mute/standby/operating/SE-only (mode select pin)
- Zero crossing mute and standby circuit
- Load dump protection circuit
- Short-circuit safe to ground, to supply voltage and across load
- Loudspeaker protection circuit
- Device switches to single-ended operation at excessive junction temperatures.

GENERAL DESCRIPTION

The TDA1561Q is a monolithic power amplifier in a 13 lead single-in-line (SIL) plastic power package. It contains two identical 23 W amplifiers. The dissipation is minimized by switching from SE to BTL mode, only when a higher output voltage swing is needed. The device is primarily developed for car radio applications.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage	DC biased	6.0	14.4	18	V
		non operating	–	–	30	V
		load dump	–	–	50	V
I_{ORM}	repetitive peak output current		–	–	4	A
$I_{q(tot)}$	total quiescent current	$R_L = \infty$	–	95	150	mA
I_{stb}	standby current		–	1	50	μA
$\|Z_i\|$	input impedance		–	60	–	kΩ
P_o	output power	RL = 4 Ω; EIAJ	–	36	–	W
		THD 10%	21	23	–	W
G_v	voltage gain		31	32	33	dB
CMRR	common mode rejection ratio	f = 1 kHz; $R_s = 0\ \Omega$	–	80	–	dB
SVRR	supply voltage ripple rejection	f = 1 kHz; $R_s = 0\ \Omega$	45	55	–	dB
$\|\Delta V_O\|$	DC output offset voltage		–	–	150	mV
α_{cs}	channel separation	$R_s = 0$ kΩ	40	60	–	dB
$\|\Delta G_v\|$	channel unbalance		–	–	1	dB

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA1561Q	DBS13P	plastic DIL-bent-SIL power package; 13 leads (lead length 12 mm)	SOT141-6

BLOCK DIAGRAM

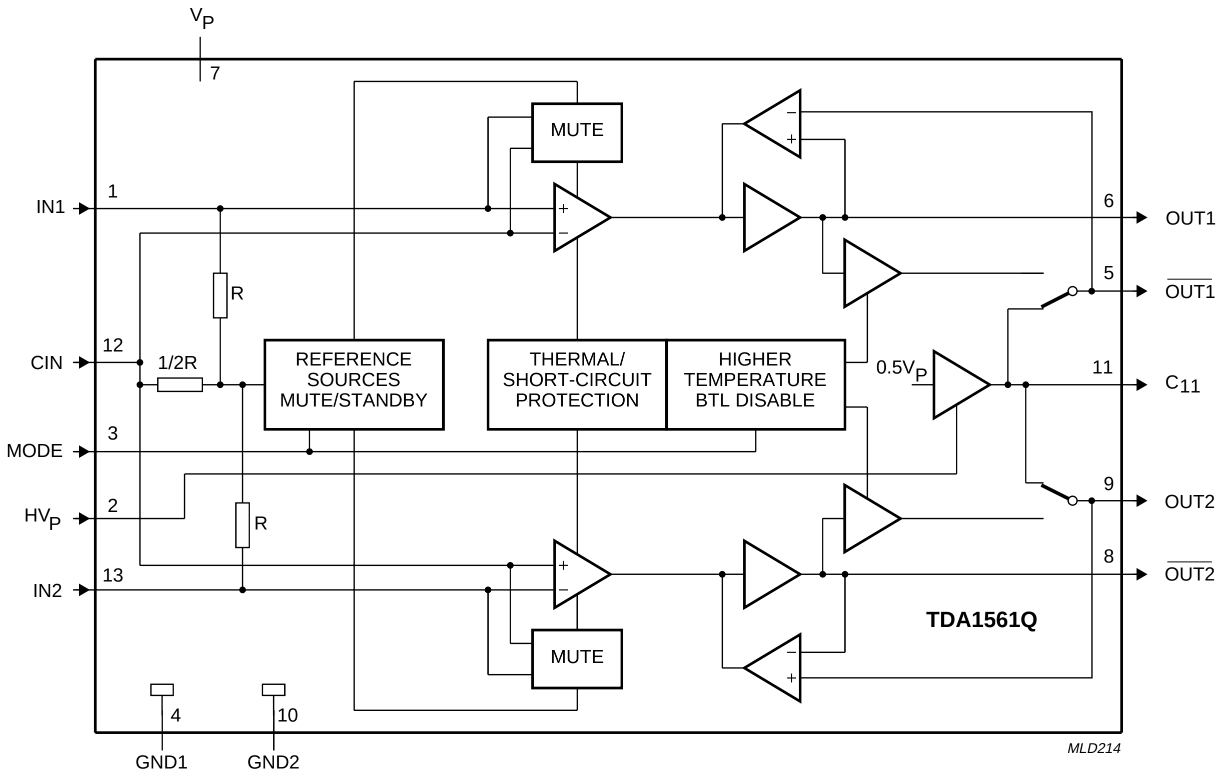


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
IN1	1	input 1
HV_P	2	half supply voltage control input
MODE	3	mute/standby/operating/SE-only
GND1	4	ground 1
$\overline{OUT1}$	5	inverting output 1
OUT1	6	non-inverting output 1
V_P	7	supply voltage
$\overline{OUT2}$	8	inverting output 2
OUT2	9	non-inverting output 2
GND2	10	ground 2
C_{11}	11	electrolytic capacitor for single-ended (SE) mode
CIN	12	common input
IN2	13	input 2

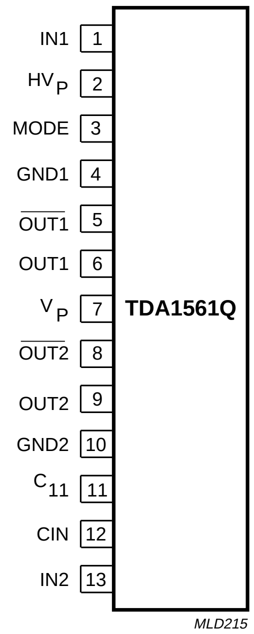


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The TDA1561Q contains two identical amplifiers with differential inputs. At low output power (up to output amplitudes of 3 V (RMS) at V_P = 14.4 V), the device operates as a normal SE amplifier. When a larger output voltage swing is needed, the circuit switches internally to BTL operation.

With a sine wave input signal the dissipation of a conventional BTL amplifier up to 2 W output power is more than twice the dissipation of the TDA1561Q (see Fig.9).

In normal use, when the amplifier is driven with music-like signals, the high (BTL) output power is only needed for a small percentage of time. Under the assumption that a music signal has a normal (Gaussian) amplitude distribution, the dissipation of a conventional BTL amplifier with the same output power is approximately 70% higher (see Fig.10).

The heatsink has to be designed for use with music signals. With such a heatsink, the thermal protection will disable the BTL mode when the junction temperature exceeds 145 °C. In this case the output power is limited to 5 W per amplifier.

The gain of each amplifier is internally fixed at 32 dB. With the MODE pin, the device can be switched to the following modes:

- Standby with low standby current (<50 μA)
- Mute condition, DC adjusted
- On, operation
- SE-only, operation (BTL disabled).

The device is fully protected against short-circuiting of the output pins to ground and to the supply voltage. It is also protected against short-circuiting the loudspeaker and high junction temperatures. In the event of a permanent short-circuit condition to ground or the supply voltage, the output stage will be switched off causing a low dissipation. With permanent short-circuiting of the loudspeaker, the output stage will be repeatedly switched on and off. The duty cycle in the ‘on’ condition is low enough to prevent excessive dissipation.

To avoid plops during switching from ‘mute’ to ‘on’ or from ‘on’ to ‘mute/standby’ while an input signal is present, a built-in zero-crossing detector allows only switching at zero input voltage. However, when the supply voltage drops below 6 V (e.g. engine start), the circuit mutes immediately avoiding clicks coming from electronic circuitry preceding the power amplifier.

The voltage of the SE electrolytic capacitor (pin 11) is always kept at $0.5V_P$ by means of a voltage buffer (see Fig.1). The value of this capacitor has an important influence on the output power in SE mode, especially at low signal frequencies, a high value is recommended to minimize dissipation at low frequencies.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_P	supply voltage	operating	–	18	V
		non operating	–	30	V
		load dump; t_r > 2.5 ms	–	50	V
$V_{P(sc)}$	short-circuit safe voltage		–	18	V
V_{rp}	reverse polarity voltage		–	6	V
I_{OSM}	non-repetitive peak output current		–	6	A
I_{ORM}	repetitive peak output current		–	4	A
P_{tot}	total power dissipation		–	60	W
T_{stg}	storage temperature		–55	+150	°C
T_{vj}	virtual junction temperature		–	150	°C
T_{amb}	operating ambient temperature		–40	–	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(j-c)}$	thermal resistance from junction to case	see note 1	1.3	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient		40	K/W

Note

1. The value of $R_{th(c-h)}$ depends on the application (see Fig.3).

Heatsink design

There are two parameters that determine the size of the heatsink. The first is the rating for the virtual junction temperature and the second is the ambient temperature at which the amplifier must still deliver its full power in the BTL mode.

With a conventional BTL amplifier, the maximum power dissipation with a music-like signal (at each amplifier) will be approximately two times 5 W. At a virtual junction temperature of 150 °C and a maximum ambient temperature of 60 °C, $R_{th(vj\text{-}c)}$ = 1.3 K/W and $R_{th(c\text{-}h)}$ = 0.2 K/W, the thermal resistance of the heatsink should be: $\frac{150-60}{2 \times 5} - 1.3 - 0.2 = 7.5$ K/W

Compared to a conventional BTL amplifier, the TDA1561Q has a higher efficiency. The thermal resistance of the heatsink should be:

$$1.7\left(\frac{150-60}{2 \times 5}\right) - 1.3 - 0.2 = 13.8 \text{ K/W}$$

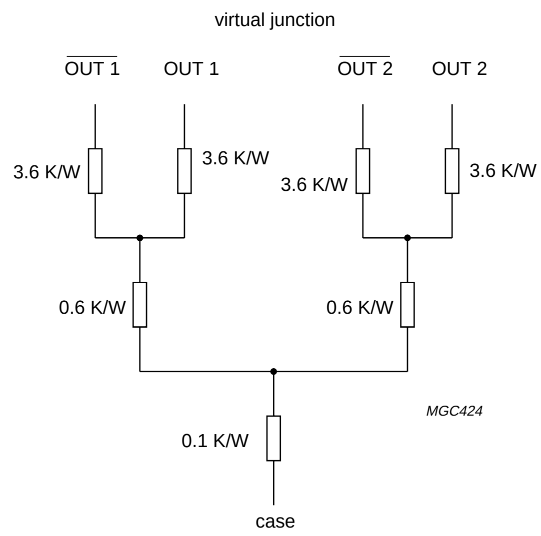


Fig.3 Thermal equivalent resistance network.

DC CHARACTERISTICS

V_P = 14.4 V; T_{amb} = 25 °C; measured in Fig.6; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_P	supply voltage	note 1	6.0	14.4	18.0	V
I_q	quiescent current	$R_L = \infty$	–	95	150	mA
I_{stb}	standby current		–	1	50	μA
V_C	average electrolytic capacitor voltage at pin 11		–	7.1	–	V
$\|\Delta V_O\|$	DC output offset voltage	on state	–	–	150	mV
		mute state	–	–	50	mV
Mode select switch (see Fig.4)						
V_{ms}	voltage at mode select pin (pin 3)	standby condition	0	–	1	V
		mute condition	2	–	3	V
		on condition (SE/BTL mode)	4	–	5.5	V
		on condition (SE mode only)	7.5	–	V_P	V
I_{ms}	switch current through pin 3	V_{ms} = 5 V	–	–	40	μA
Protection						
T_{dis}	BTL disable temperature		–	145	–	°C

Note

1. The circuit is DC biased at V_P = 6 to 18 V and AC operating at V_P = 8 to 18 V.

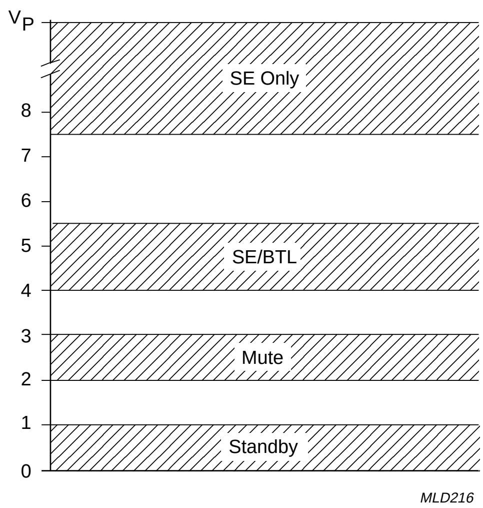


Fig.4 Switching levels of mode select switch.

AC CHARACTERISTICS

V_P = 14.4 V; R_L = 4 Ω; C_{11} = 1000 μF; f = 1 kHz; T_{amb} = 25 °C; measured in Fig.6; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
P_o	output power	THD = 1%	15	18	–	W
		THD = 10%	21	23	–	W
		EIAJ	–	36	–	W
		V_P = 13.2 V; THD = 0.5%	–	14	–	W
		V_P = 13.2 V; THD = 10%	–	20	–	W
THD	total harmonic distortion	P_o = 1 W; f = 1 kHz; note 1	–	0.1	–	%
P_d	dissipated power		see Figs 9 and 10			W
B_p	power bandwidth	THD = 1%; P_o = –1 dB with respect to 15 W	–	20 to 15 000	–	Hz
$f_{ro(l)}$	low frequency roll-off	–1 dB; note 2	–	25	–	Hz
$f_{ro(h)}$	high frequency roll-off	–1 dB	130	–	–	kHz
G_v	closed loop voltage gain		31	32	33	dB
SVRR	supply voltage ripple rejection	R_S = 0 Ω; V_{ripple} = 2 V (p-p)				
		on; f = 1 kHz	45	60	–	dB
		mute; f = 1 kHz	–	90	–	dB
		standby; f = 100 Hz to 10 kHz	80	–	–	dB
CMRR	common mode rejection ratio	R_s = 0 Ω; f = 1 kHz	–	80	–	dB
$\|Z_i\|$	input impedance		45	60	75	kΩ
$\|\Delta Z_i\|$	mismatch in input impedance		–	1	–	%
V_{SE-BTL}	SE to BTL switch voltage level	note 3	–	3	–	V
$\|V_{out}\|$	output voltage-mute (RMS value)	V_i = 1 V (RMS)	–	50	100	μV
$V_{n(o)}$	noise output voltage	on; R_s = 0 Ω; note 4	–	160	300	μV
		on; R_s = 10 kΩ; note 4	–	170	–	μV
		mute; note 5	–	20	–	μV
α_{cs}	channel separation	R_s = 0 Ω	40	60	–	dB
$\|\Delta G_v\|$	channel unbalance		–	–	1	dB

Notes

1. The distortion is measured with a bandwidth of 10 Hz to 30 kHz.
2. Frequency response externally fixed (input capacitors determine low frequency roll-off).
3. The SE to BTL switch voltage level depends on V_P.
4. Noise output voltage measured with a bandwidth of 20 Hz to 20 kHz.
5. Noise output voltage is independent of R_s (see Fig.6)(V_i = 0 V).

TEST AND APPLICATION INFORMATION

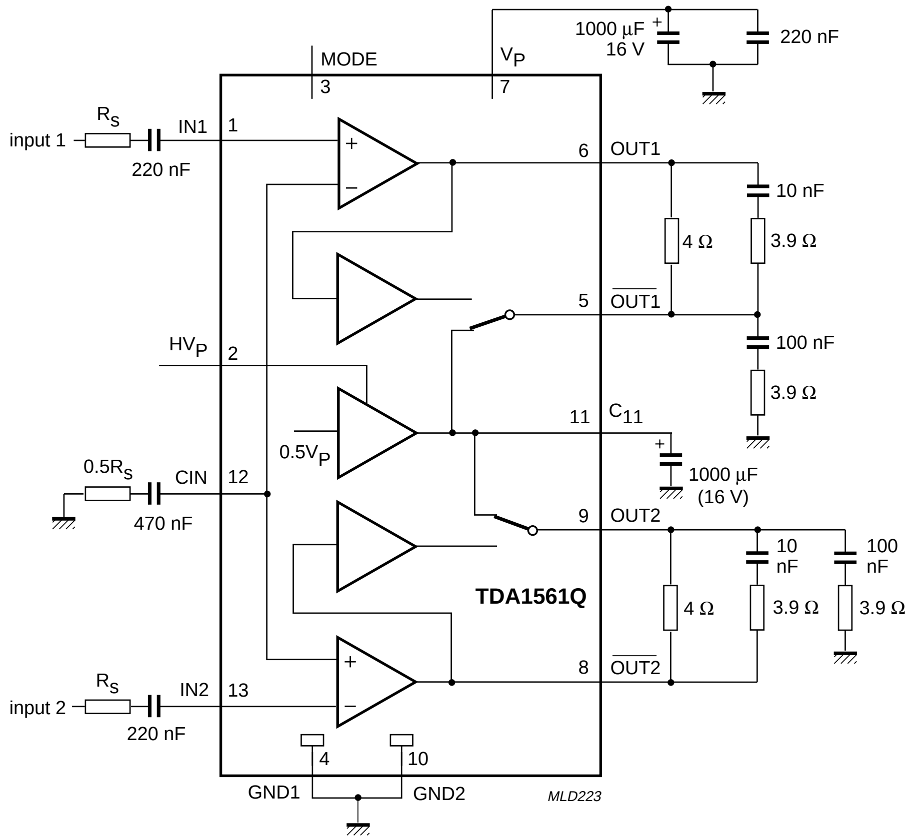
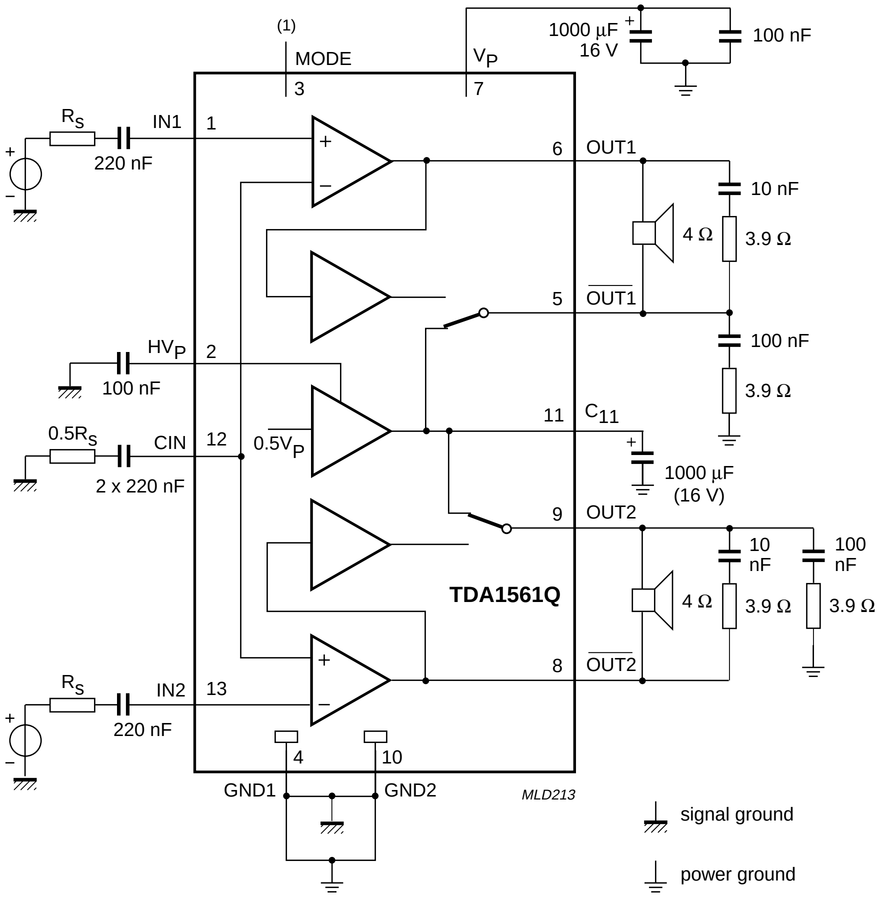
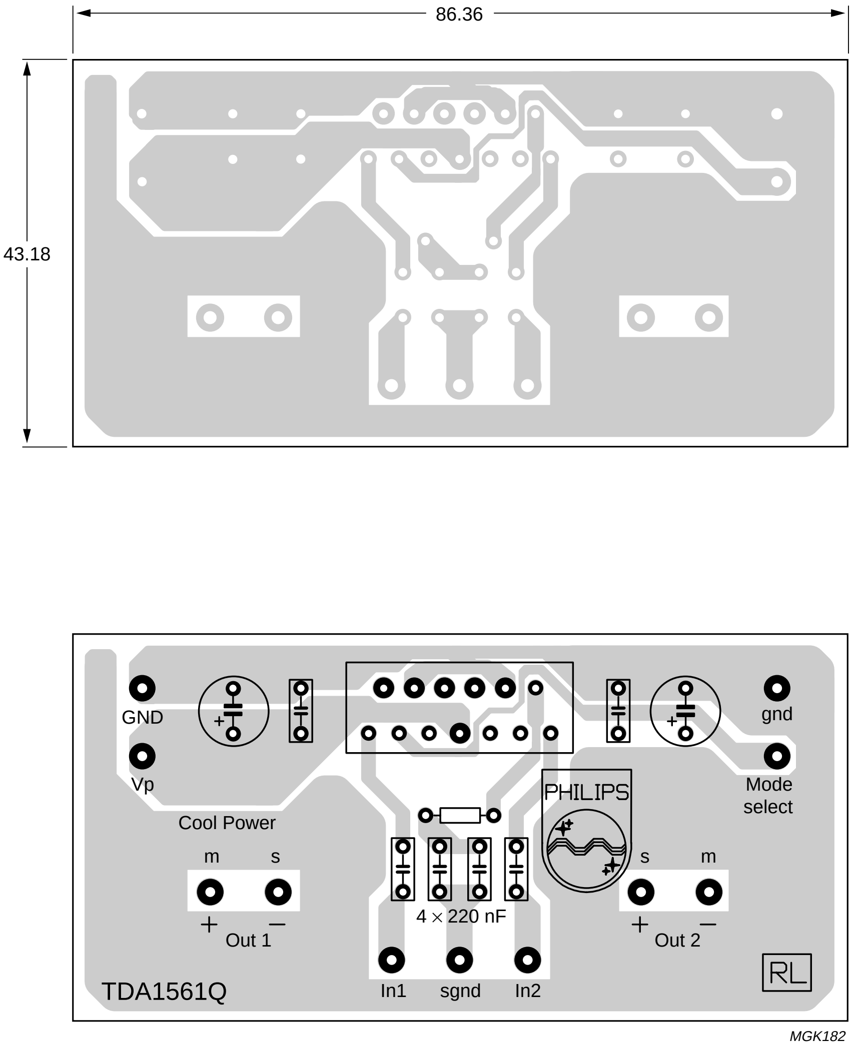


Fig.5 Test diagram.



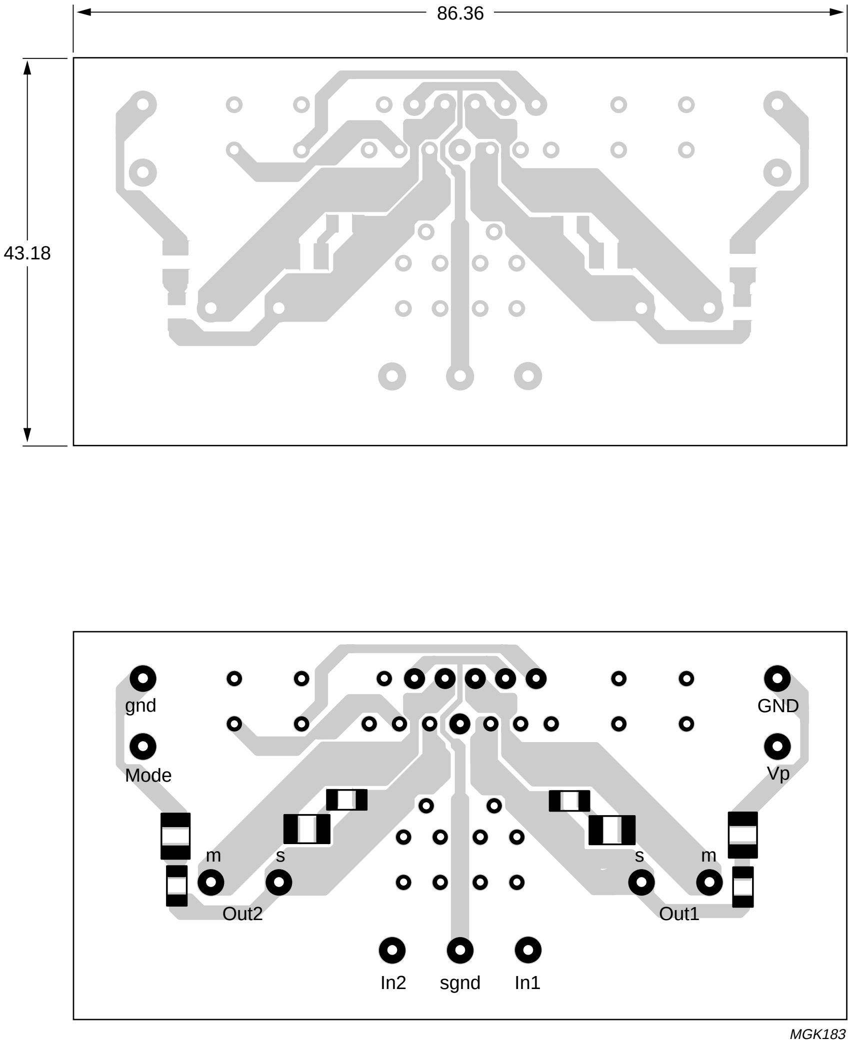
Connect Boucherot filter to pin 4 respectively pin 10 with the shortest possible connection.

Fig.6 Application diagram.



Dimensions in mm.

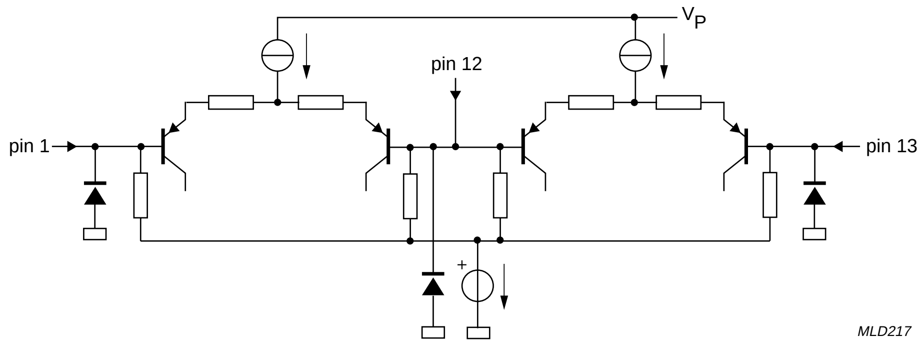
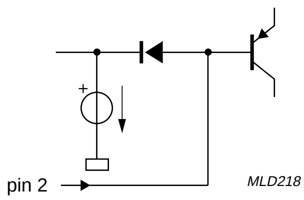
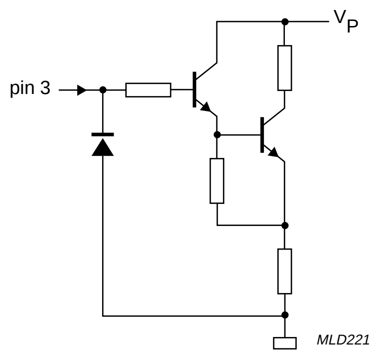
Fig.7 PCB layout (component side) for the application of Fig.6.

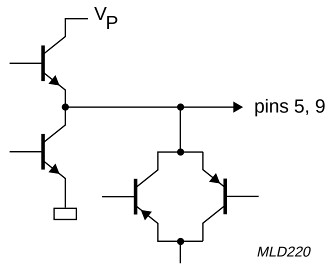
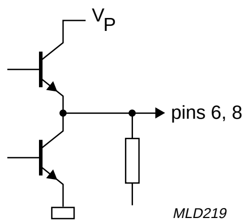
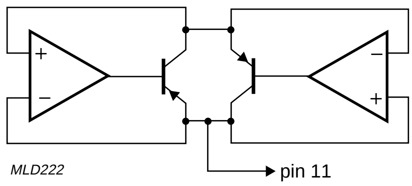


Dimensions in mm.

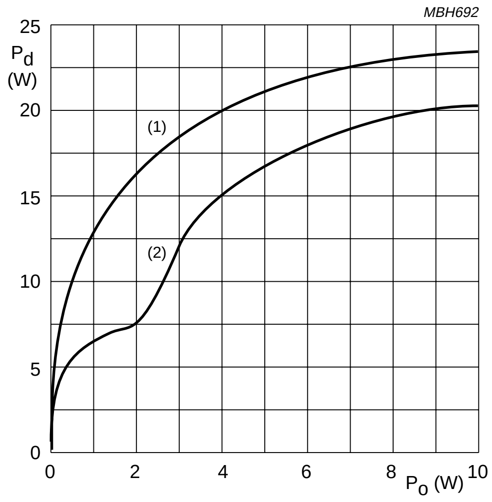
Fig.8 PCB layout (soldering side) for the application of Fig.6.

INTERNAL PIN CONFIGURATIONS

PIN	NAME	EQUIVALENT CIRCUIT
1,12,13	IN1, CIN, IN2	
2	HV_P	
3	MODE	

PIN	NAME	EQUIVALENT CIRCUIT
5, 9	$\overline{OUT1}$, OUT2	
6, 8	OUT1, $\overline{OUT2}$	
11	C_{11}	

ADDITIONAL APPLICATION INFORMATION

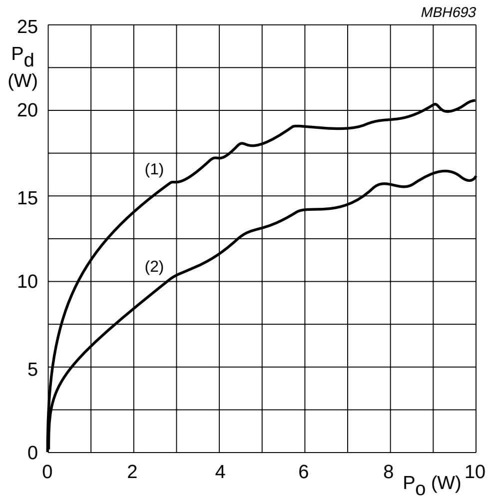


Input signal 1 kHz, sinusoidal; V_P = 14.4 V.

(1) For a conventional BTL amplifier.

(2) For TDA1561Q.

Fig.9 Dissipation; sine wave driven.



(1) For a conventional BTL amplifier.

(2) For TDA1561Q.

Fig.10 Dissipation; pink noise through IEC-268 filter.

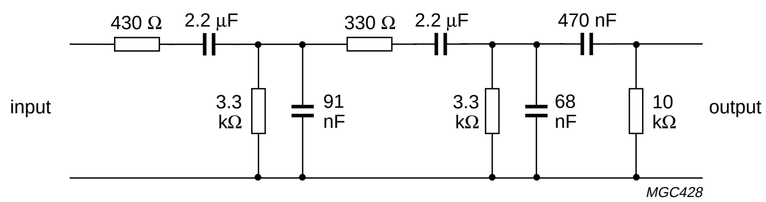


Fig.11 IEC-268 filter.

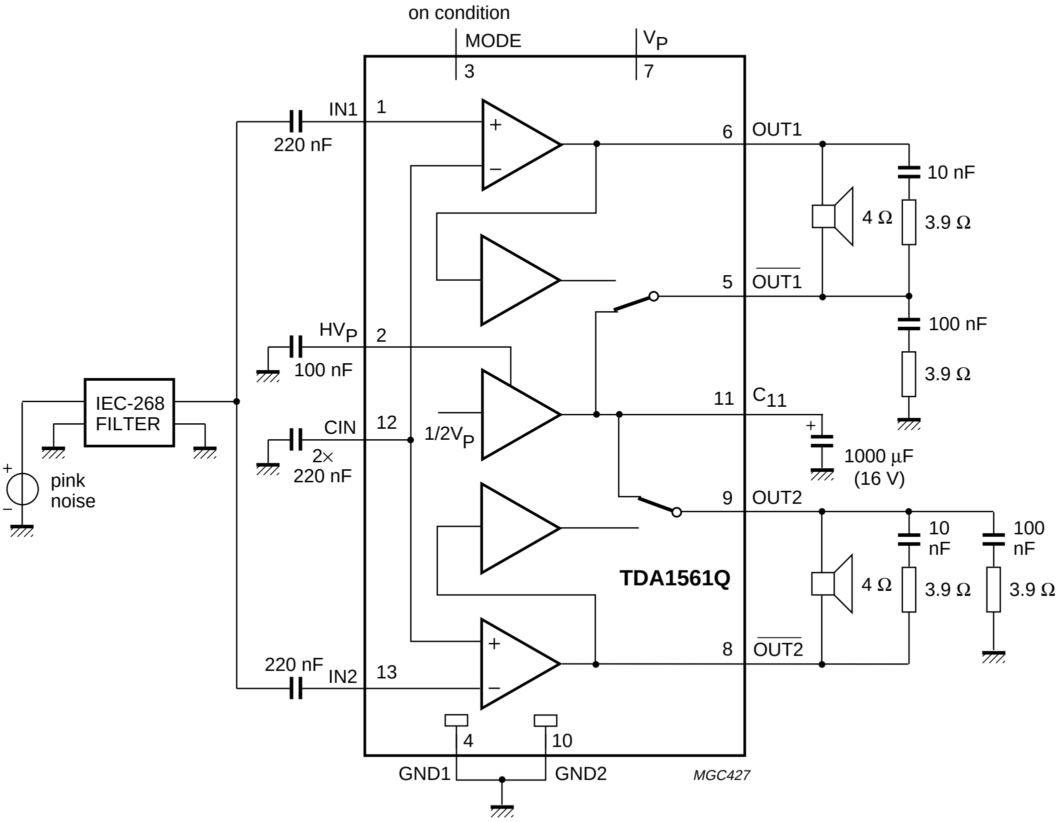
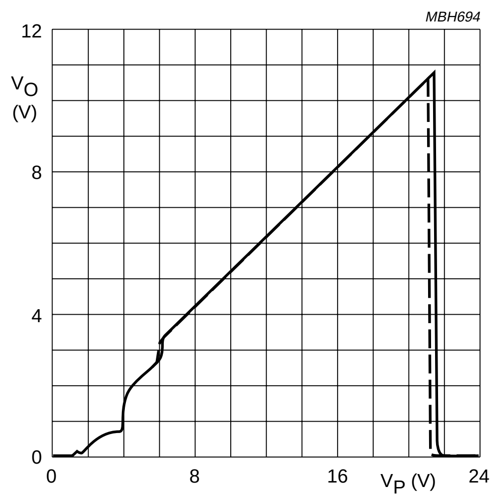
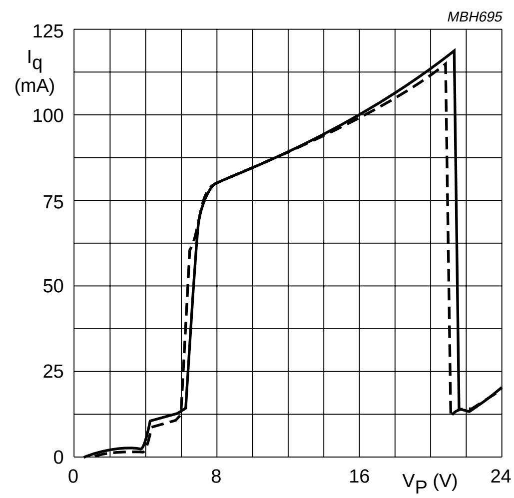


Fig.12 Test and application diagram for dissipation measurements with a music-like signal (pink noise).



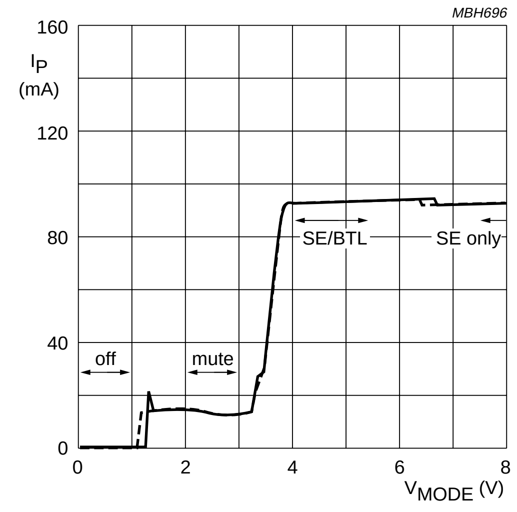
V_{ms} = 5 V.

Fig.13 DC output voltage as a function of V_P.



V_{ms} = 5 V; $R_l = \infty$.

Fig.14 Quiescent current as a function of V_P.



V_P = 14.4 V; V_{in} = 0 mV; $R_l = \infty$.

Fig.15 I_P as a function of V_{ms} (pin 3).

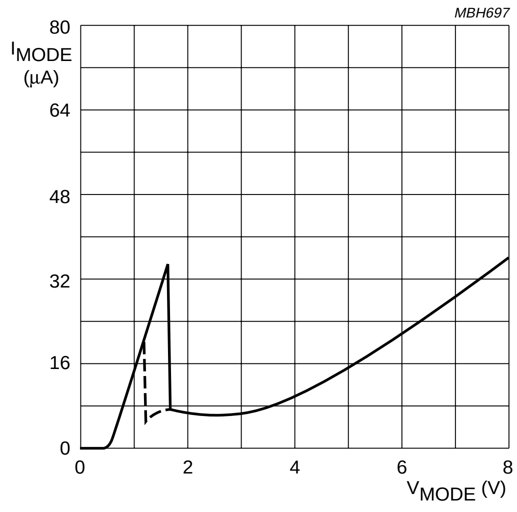
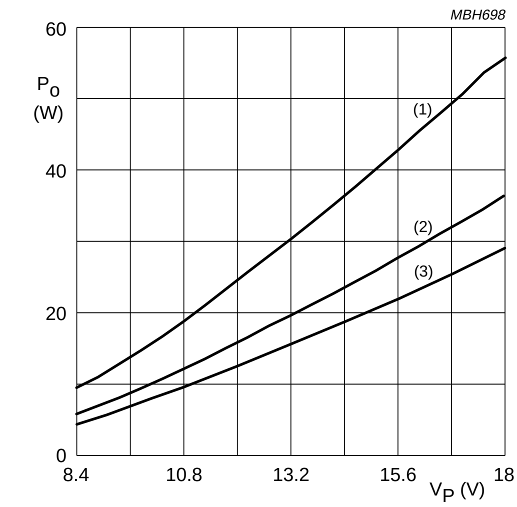


Fig.16 I_{ms} as a function of V_{ms}.



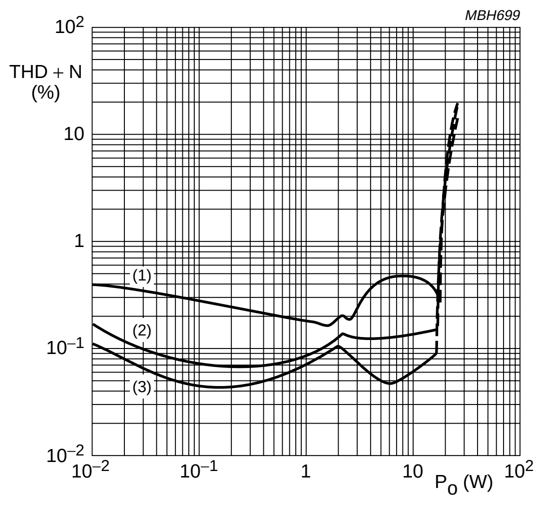
Both channels driven.

(1) EIAJ.

(2) THD = 10%.

(3) THD = 1%.

Fig.17 Output power as a function of V_P.

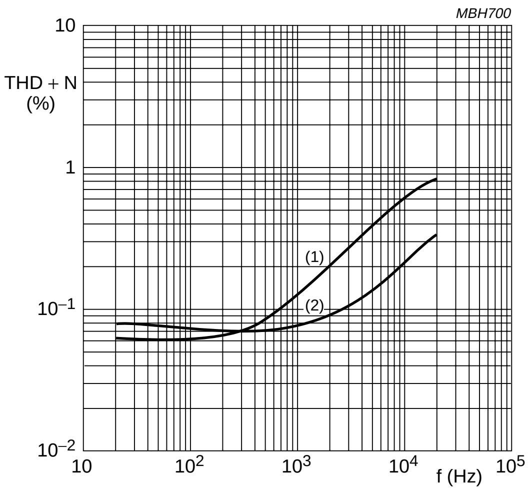


(1) f = 10 kHz.

(2) f = 1 kHz.

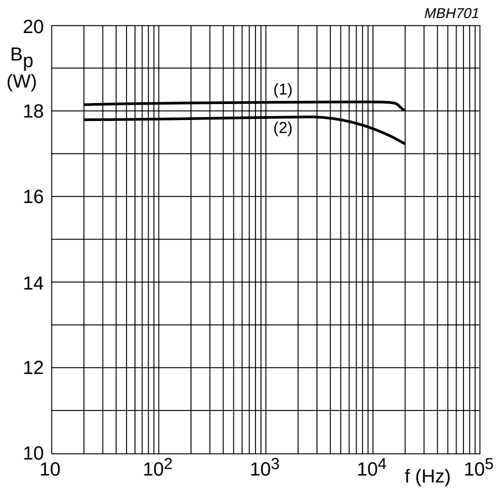
(3) f = 100 Hz.

Fig.18 THD + noise as a function of P_o.



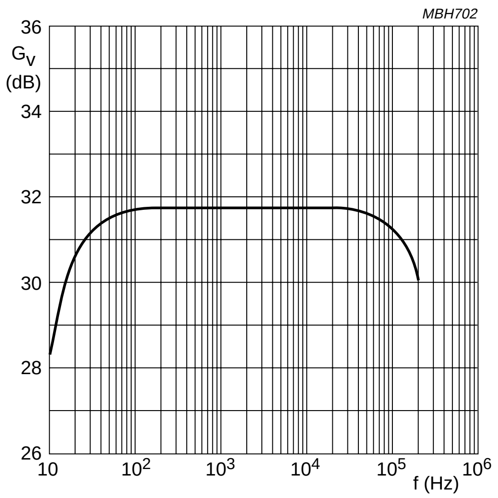
(1) P_o = 10 W.
(2) P_o = 1 W.

Fig.19 THD + noise as a function of frequency.



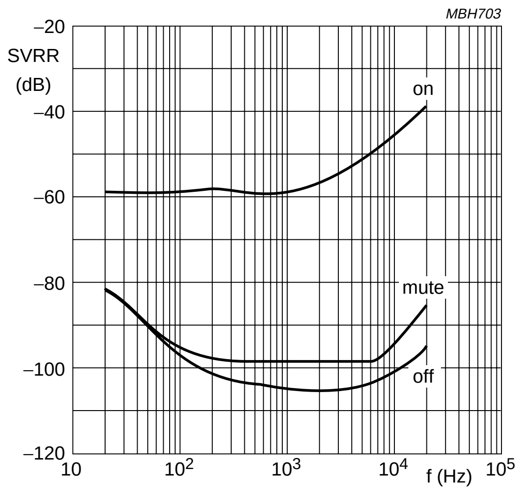
(1) For OUT2.
(2) For OUT1.

Fig.20 Power bandwidth at THD = 1%.



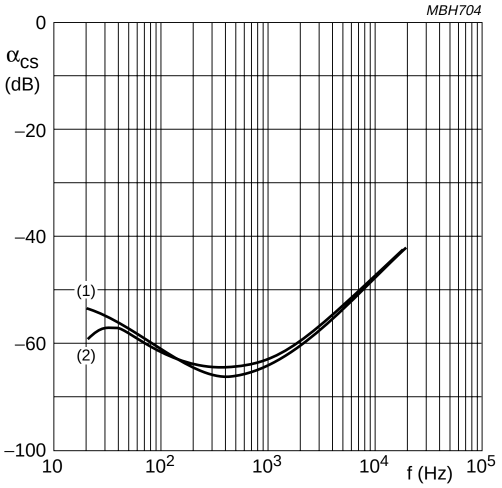
V_{in} = 50 mV.

Fig.21 Gain as a function of frequency.



$V_{ripple(p-p)}$ = 2 V.

Fig.22 SVRR as a function of frequency.



(1) P_o = 1 W.
(2) P_o = 10 W.

Fig.23 Channel separation as a function of frequency.

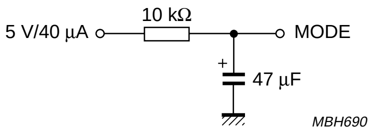
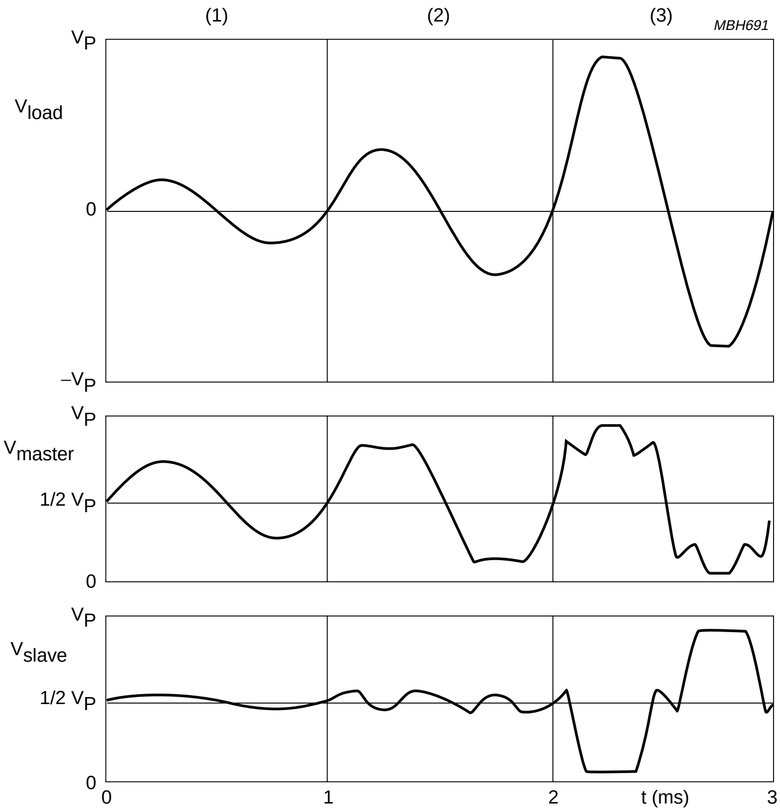


Fig.24 Mode select circuit.

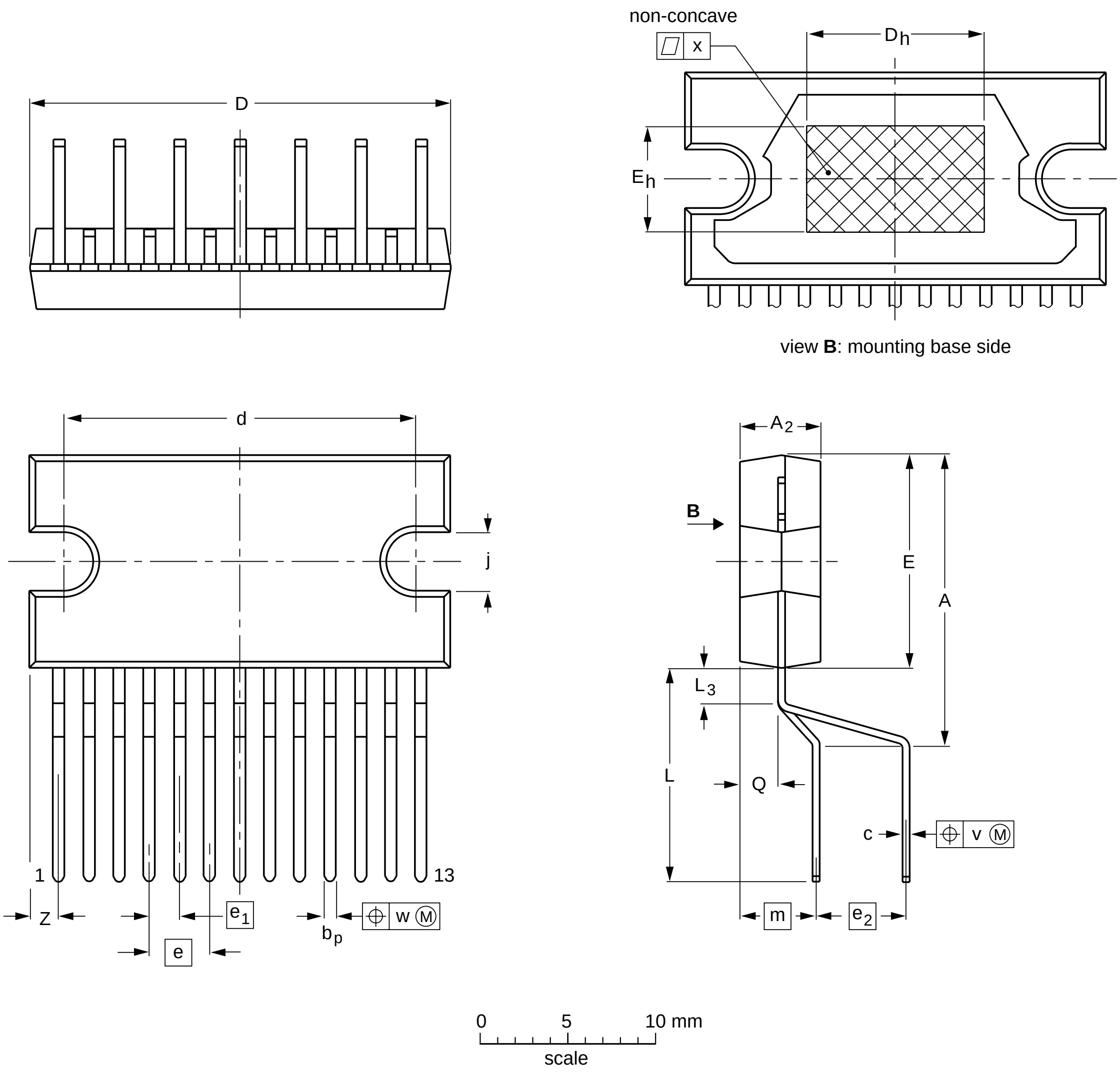


See Fig.5:
$V_{load} = V_6 - V_5$ or $V_8 - V_9$
$V_{master} = V_6$ or V_8
$V_{slave} = V_5$ or V_9

Fig.25 Output waveforms.

PACKAGE OUTLINE

DBS13P: plastic DIL-bent-SIL power package; 13 leads (lead length 12 mm) **SOT141-6**



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_2	b_p	c	$D^{(1)}$	d	D_h	$E^{(1)}$	e	e_1	e_2	E_h	j	L	L_3	m	Q	v	w	x	$Z^{(1)}$
mm	17.0 15.5	4.6 4.2	0.75 0.60	0.48 0.38	24.0 23.6	20.0 19.6	10	12.2 11.8	3.4	1.7	5.08	6	3.4 3.1	12.4 11.0	2.4 1.6	4.3	2.1 1.8	0.8	0.25	0.03	2.00 1.45

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT141-6						~~95-03-11~~ 97-12-16

SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

Soldering by dipping or by wave

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg\ max}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

Repairing soldered joints

Apply a low voltage soldering iron (less than 24 V) to the lead(s) of the package, below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.

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