

 ICOM®

SERVICE MANUAL

VHF FM TRANSCEIVER

IC-V8000

Icom Inc.

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INTRODUCTION

This service manual describes the latest service information for the **IC-V8000 VHF FM TRANSCEIVER** at the time of publication.

VERSION	SYMBOL	SUPPLIED MICROPHONE
Asia	SEA	HM-118N
C.S.America	CSA	HM-118TN
	CSA-1	HM-133V
U.S.A.	USA-2	
	USA-3	HM-118TAN

To upgrade quality, any electrical or mechanical parts and internal circuits are subject to change without notice or obligation.

DANGER

NEVER connect the transceiver to an AC outlet or to a DC power supply that uses more than 16 V. This will ruin the transceiver.

DO NOT expose the transceiver to rain, snow or any liquids.

DO NOT reverse the polarities of the power supply when connecting the transceiver.

DO NOT apply an RF signal of more than 20 dBm (100mW) to the antenna connector. This could damage the transceiver's front end.



ORDERING PARTS

Be sure to include the following four points when ordering replacement parts:

1. 10-digit order numbers
2. Component part number and name
3. Equipment model name and unit name
4. Quantity required

<SAMPLE ORDER>

1110003200 S.I.C TA31136FN IC-V8000 MAIN UNIT 5 pieces
8810006050 Screw Icom screw E7 IC-V8000 Chassis 10 pieces

Addresses are provided on the inside back cover for your convenience.

REPAIR NOTES

1. Make sure a problem is internal before disassembling the transceiver.
2. **DO NOT** open the transceiver until the transceiver is disconnected from its power source.
3. **DO NOT** force any of the variable components. Turn them slowly and smoothly.
4. **DO NOT** short any circuits or electronic parts. An insulated turning tool **MUST** be used for all adjustments.
5. **DO NOT** keep power ON for a long time when the transceiver is defective.
6. **DO NOT** transmit power into a signal generator or a sweep generator.
7. **ALWAYS** connect a 50 dB to 60 dB attenuator between the transceiver and a deviation meter or spectrum analyzer when using such test equipment.
8. **READ** the instructions of test equipment thoroughly before connecting equipment to the transceiver.

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SECTION 1 SPECIFICATIONS

■ GENERAL

- Frequency coverage

Version	Receive	Transmit
[USA]		144.000–148.000 MHz
[SEA]	136.000–174.000 MHz*	140.000–150.000 MHz*
[CSA]		136.000–174.000 MHz*

*Specifications Guaranteed: 144–148 MHz only

- Type of emission
 - Frequency stability
 - Tuning steps
 - Antenna connector
 - Power supply requirement (negative ground)
 - Number of memory channel
 - Call channel
 - Scanning mode
 - Current drain (approx.)
 - Usable temperature range
 - Dimensions (projections not included)
 - Weight
- : FM (F2D / F3E)
: ± 10 ppm (-10°C to $+60^{\circ}\text{C}$; $+14^{\circ}\text{F}$ to $+140^{\circ}\text{F}$)
: 5, 10, 12.5, 15, 20, 25, 30 or 50 kHz
: SO-239 (50Ω)
: 13.8 V DC (Operable voltage range: 11.7 to 15.9 V)
: 207 channels (including 6 scan edges and 1 call channel)
: 1 channel
: Full, Program, Priority, Memory, Channel, Skip, Tone, DTCS, Bank and WX
- | | High (75 W) | 15 A |
|-----------|--------------------|-------|
| Transmit | Middle High (25 W) | 9.0 A |
| | Middle Low (10 W) | 6.0 A |
| | Low (5 W) | 5.0 A |
| Receiving | Max. audio | 1.0 A |
| | Stand-by | 0.8 A |
- : -10°C to $+60^{\circ}\text{C}$; $+14^{\circ}\text{F}$ to $+140^{\circ}\text{F}$
: $150(\text{W}) \times 50(\text{H}) \times 150(\text{D})$ mm; $5\frac{29}{32}(\text{W}) \times 1\frac{31}{32}(\text{H}) \times 5\frac{29}{32}(\text{D})$ in.
: 1.09 kg; 12.3 oz.; 38.4 oz

■ TRANSMITTER

- RF output power (at 13.8 V DC)
- Modulation system
- Maximum frequency deviation
- Spurious emissions
- Microphone connector

- RF output power (at 13.8 V DC)
 - Modulation system
 - Maximum frequency deviation
 - Spurious emissions
 - Microphone connector
- : 75 W / 25 W / 10 W / 5 W (High / Middle High / Middle Low / Low)
: Variable reactance frequency modulation
: Narrow: ± 2.5 kHz*; Wide: ± 5.0 kHz
: Less than -60 dB
: 8-pins modular (600Ω)

■ RECEIVER

- Receive system
- Intermediate frequencies
- Sensitivity
- Squelch sensitivity
- Selectivity
- Spurious and image rejection
- Audio output power (at 7.2 V DC)
- Ext. speaker connector

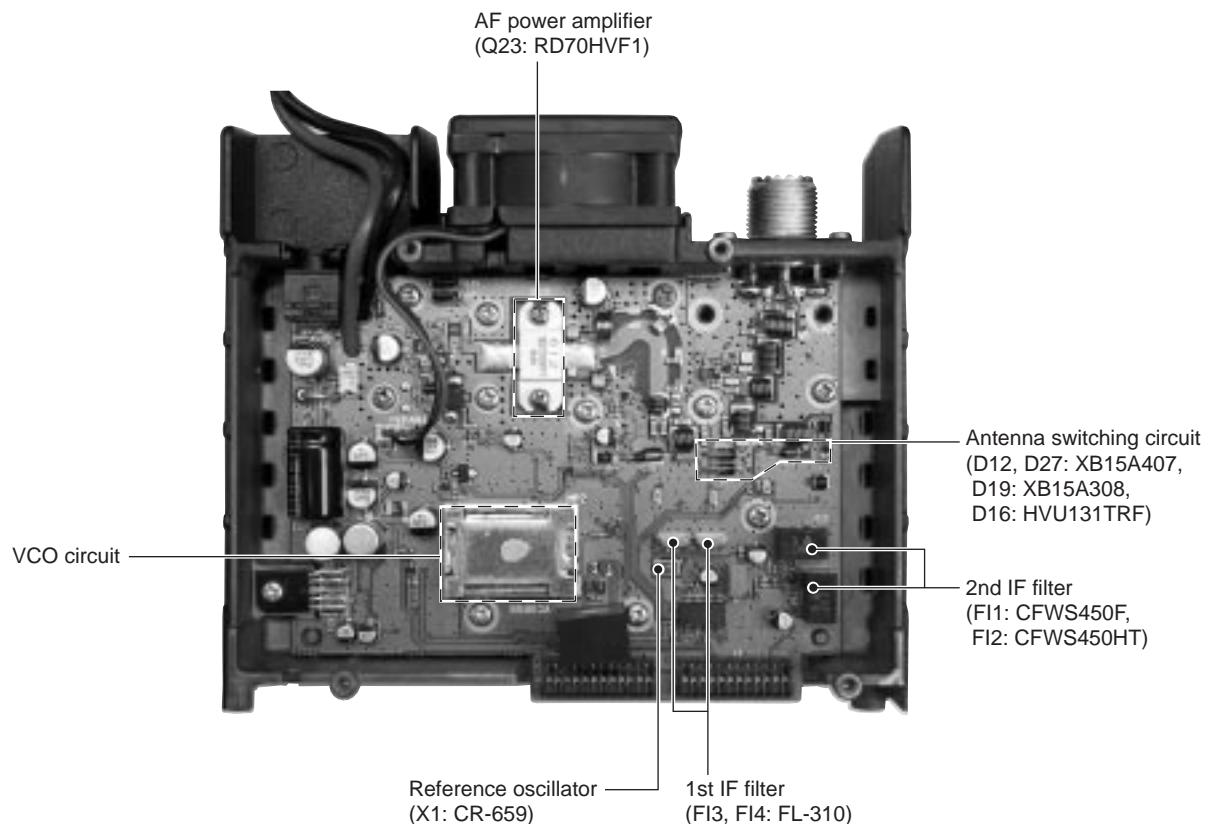
- Receive system
 - Intermediate frequencies
 - Sensitivity
 - Squelch sensitivity
 - Selectivity
 - Spurious and image rejection
 - Audio output power (at 7.2 V DC)
 - Ext. speaker connector
- : Double conversion superheterodyne system
: 1st 21.7 MHz
: 2nd 450 kHz
: $0.15 \mu\text{V}$ at 12 dB SINAD (typical)
: $0.08 \mu\text{V}$ at threshold (typical)
: Narrow; More than ± 3.0 kHz at -6 dB, Less than ± 9.0 kHz at -55 dB*
: Wide; More than ± 6.0 kHz at -6 dB, Less than ± 14.0 kHz at -60 dB
: 60 dB (typical)
: More than 2.0 W at 10% distortion with an 8Ω load
: 3-conductor 3.5(d) mm ($1/8"$)/8 Ω

*[USA] version only

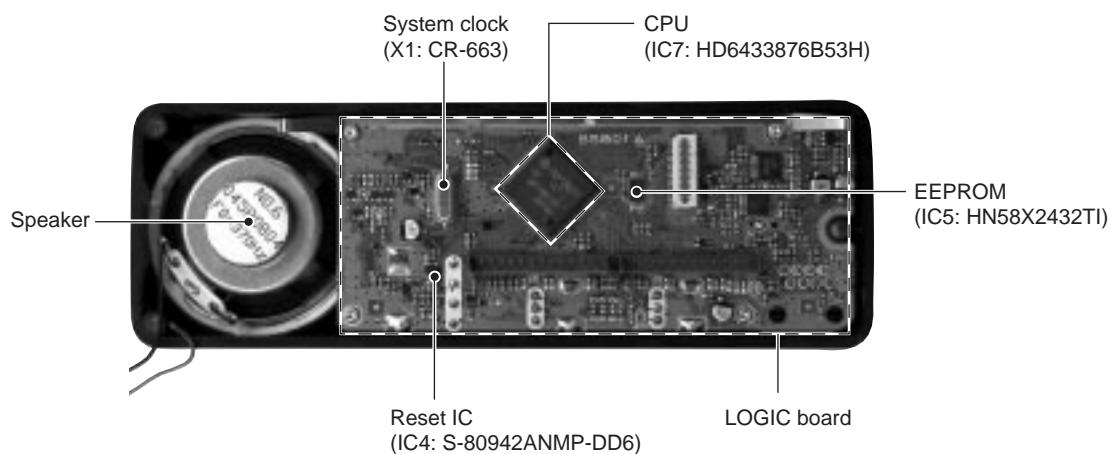
All stated specifications are subject to change without notice or obligation.

SECTION 2 INSIDE VIEWS

• MAIN UNIT



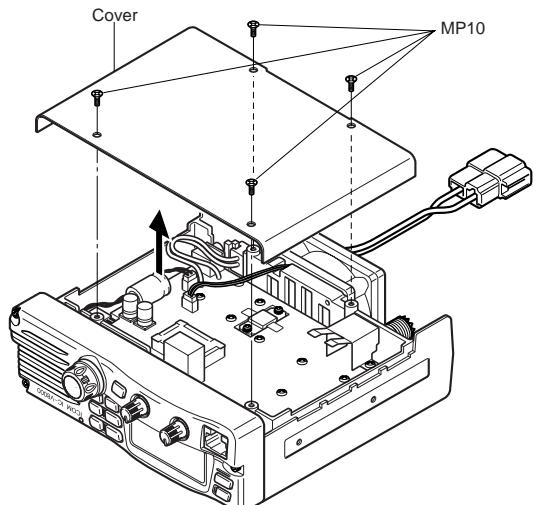
• LOGIC BOARD



SECTION 3 DISASSEMBLY AND OPTION INSTRUCTIONS

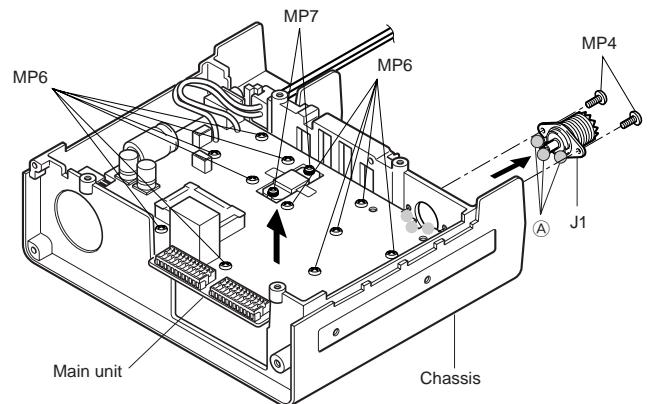
• REMOVING THE COVER

- ① Unscrew 4 screws, MP10.
- ② Remove the cover in the direction of the arrow.



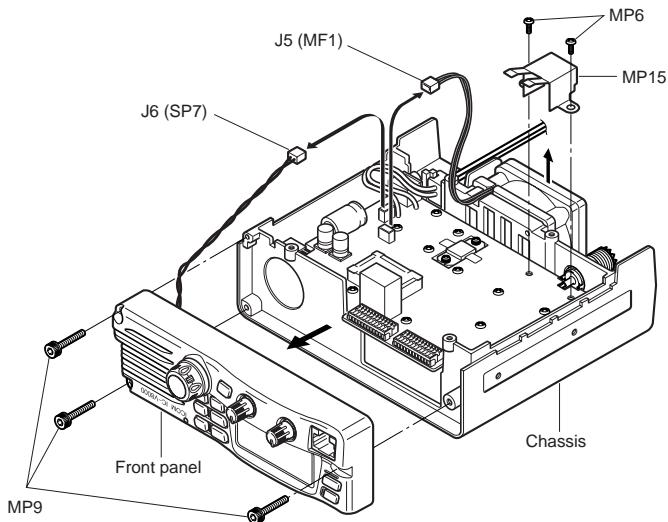
• REMOVING THE MAIN UNIT

- ① Unscrew 11 screws, MP6, and 2 screws, MP7, and 2 screws, MP4.
- ② Unsolder 3 points, Ⓐ, to remove the antenna connector.
- ③ Remove the Main unit in the direction of the arrow.



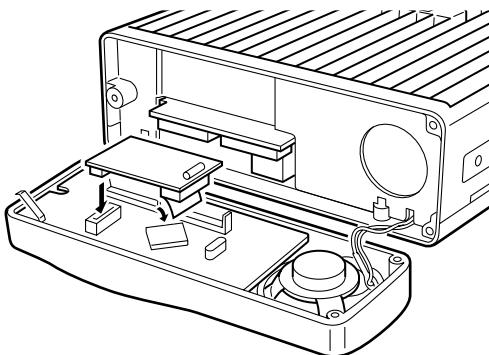
• REMOVING THE FRONT PANEL

- ① Unscrew 3 screws, MP9.
- ② Unplug J6 to separate front panel and chassis.
- ③ Remove the front panel in the direction of the arrow.
- ④ Unplug J5 to separate fan and chassis.
- ⑤ Unscrew 2 screws, MP6, to separate MP15 and chassis.



• OPTIONAL UNIT INSTALLATION

- ① Install the optional unit as illustrated below. Insert it tightly to avoid bad contact.



SECTION 4 CIRCUIT DESCRIPTION

4-1 RECEIVER CIRCUITS

4-1-1 ANTENNA SWITCHING CIRCUIT (MAIN UNIT)

Received signals passed through the low-pass filter (L44, L47, L48, L51, C190, C197, C203, C208, C210, C217, C218). The filtered signals are applied to the $1/4 \lambda$ type antenna switching circuit (D16, D19).

The antenna switching circuit functions as a low-pass filter while transmitting. However, its impedance becomes very high while D16 and D19 are turn ON. Thus transmit signals are blocked from entering the receiver circuits. The antenna switching circuit employs a $1/4 \lambda$ type diode switching system. The passed signals are then applied to the RF amplifier circuit.

4-1-2 RF CIRCUIT (MAIN UNIT)

The RF circuit amplifies signals within the range of frequency coverage and filters out-of-band signals.

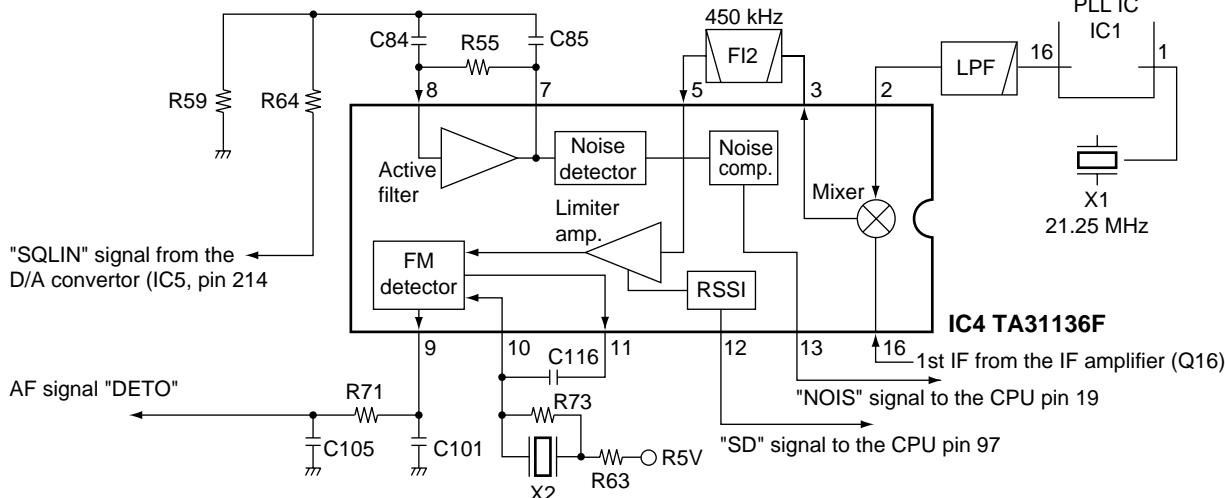
The signals from the antenna switching circuit are applied to the limitter (D15), and are then passed through the bandpass filter (D13, L43, C183, C182). The filtered signals are amplified at the RF amplifier (Q27), then applied to the 1st mixer circuit after out-of-band signals are suppressed at the bandpass filter (D9-D11).

D9-D11, D13 employ varactor diodes that track the bandpass filters and are controlled by the T1-T3 signals from the D/A convertor (IC5, pins 10, 11, 23). These diodes tune the center frequency of an RF passband for wide bandwidth receiving and good image response rejection.

4-1-3 1ST MIXER AND 1ST IF CIRCUITS (MAIN UNIT)

The 1st mixer circuit converts the received signal to a fixed frequency of the 1st IF signal with a PLL output frequency. By changing the PLL frequency, only the desired frequency will pass through two crystal filters at the next stage of the 1st mixer.

• 2ND IF AND DEMODULATOR CIRCUITS



The signals from the RF circuit are mixed at the 1st mixer (Q19) with a 1st LO signal coming from the VCO circuit to produce a 21.70 MHz 1st IF signal.

The 1st IF signal is applied to two crystal filters (FL3 and FL4) to suppress out-of-band signals. The filtered 1st IF signal is applied to the IF amplifier (Q16), then applied to the 2nd mixer circuit (IC4, pin 16).

4-1-4 2ND IF AND DEMODULATOR CIRCUITS (MAIN UNIT)

The 2nd mixer circuit converts the 1st IF signal to a 2nd IF signal. A double conversion superheterodyne system (which converts receive signal twice) improves the image rejection ratio and obtain stable receiver gain.

The 1st IF signal from the IF amplifier is applied to the 2nd mixer section of the FM IF IC (IC4, pin 16), and is mixed with the 2nd LO signal to be converted to a 450 kHz 2nd IF signal.

The FM IF IC contains the 2nd mixer, limiter amplifier, quadrature detector and active filter circuits. A 21.25 MHz 2nd LO signal is produced at the PLL circuit.

The 2nd IF signal from the 2nd mixer (IC4, pin 3) passes through a ceramic filter (FL1; When wide is selected, F2; When Narrow is selected. (Narrow is [USA] version only.)) to remove unwanted heterodyned frequencies. It is then amplified at the limiter amplifier (IC4, pin 5) and applied to the quadrature detector (IC4, pins 10, 11) to demodulate the 2nd IF signal into AF signals.

4-1-5 AF CIRCUIT (MAIN AND LOGIC UNITS)

The AF amplifier circuit amplifies the demodulated AF signals to drive a speaker.

AF signals from the FM IF IC (IC2, pin 9) are applied to the analog switch (LOGIC UNIT; IC6, pin 1) via the high pass filter (IC3c, pins 9, 8). The output signals from pin 11 are applied to the volume adjustment pot (LOGIC UNIT; R31). The signals are applied to the AF power amplifier (IC9, pin 1) after passing through the AFmute switch (Q29).

The AF signals are applied to the AF power amplifier circuit (IC9, pin 1) to obtain the specified audio level. The amplified AF signals, output from pin 4, are applied to the internal speaker (CHASSIS UNIT; SP1) via the speaker jack (J6) when no plug is connected to the external speaker jack (J1).

4-1-6 SQUELCH CIRCUIT (MAIN AND LOGIC UNITS)

A squelch circuit cuts out AF signals when no RF signals are received. By detecting noise components in the AF signals, the squelch switches the analog switch.

A portion of the AF signals from the FM IF IC (IC4, pin 9) are applied to the D/A converter (IC5, pin 13) as the DETO signal. The signals from the D/A converter (IC5, pin 14) are applied to the FM IF IC active filter section (IC4, pin 8) where noise components are amplified and detected with an internal noise detector via the SQLIN line.

The trigger circuit converts the detected signals to a HIGH or LOW signal and applies this (from pin 13) to the CPU (LOGIC UNIT; IC7, pin 19) as the NOIS signal. The CPU controls the analog switch IC (LOGIC UNIT; IC6) via the expander IC (LOGIC UNIT; IC8). When the CPU receives a HIGH level NOIS signal, the CPU controls the RMUT line to cut the AF signals at the analog switch IC (LOGIC UNIT; IC6). At the same time, the AFON line controls the AF mute circuit (Q29) to cut out the VOLOUT signal for the AF power amplifier (IC9).

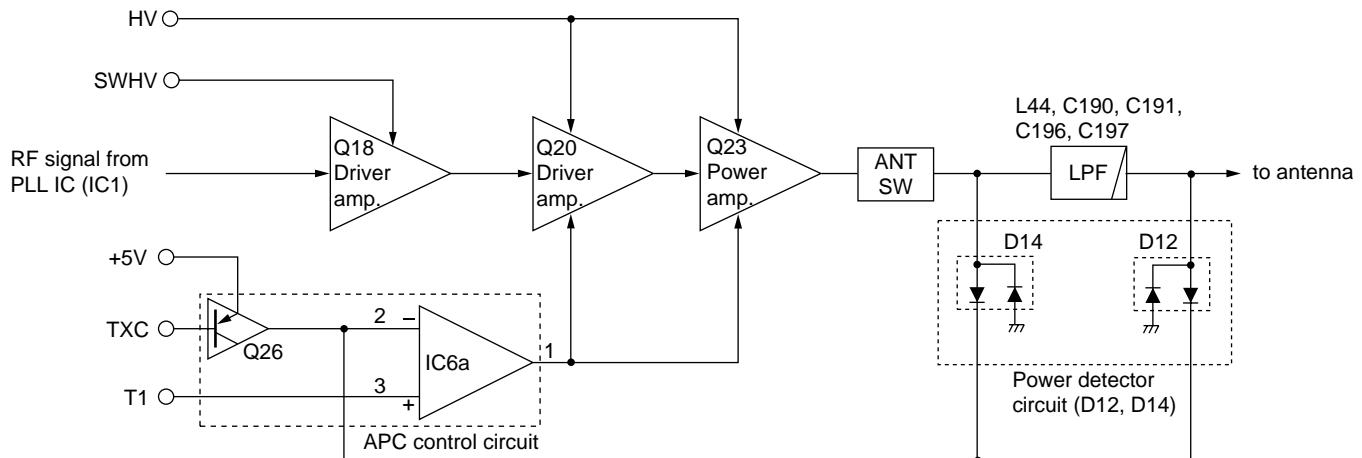
4-2 TRANSMITTER CIRCUITS

4-2-1 MICROPHONE AMPLIFIER CIRCUIT (LOGIC AND MAIN UNITS)

The microphone amplifier circuit amplifies audio signals with +6 dB/octave pre-emphasis from the microphone to a level needed for the modulation circuit.

The AF signals from the microphone pass through the MIC switch (IC2, D4) and high-pass filter (IC3a, pin 2), and are then applied to the microphone amplifier circuit (IC3d, pin 12) via the R39 and C47 for +6 dB/octave pre-emphasis. The amplified AF signals are applied to the analog switch (IC6, pin 4), and are then applied to the D/A converter (MAIN UNIT; IC5, pin 1) via the MODIN signal. The AF signals are applied to the modulator circuit via the MOD signal.

• APC CIRCUIT



4-2-2 MODULATION CIRCUIT (MAIN UNIT)

The modulation circuit modulates the VCO oscillating signal (RF signal) using the microphone audio signals.

The audio signals (SHIFT) change the reactance of D2 to modulate an oscillated signal at the VCO (Q6, D4). The oscillated signal is amplified at the LO (Q9) and buffer (Q11) amplifiers, then applied to the TX/RX switch circuit (D6, D7).

4-2-3 DRIVE/POWER AMPLIFIER CIRCUITS (MAIN UNIT)

The signal from the VCO circuit passes through the TX/RX switching circuit (D6) and is amplified at the pre-drive (Q17), drive (Q18, Q20) and power (Q23) amplifiers to obtain 75 W of RF power (at 13.8 V DC/typical). The amplified signal passes through the low-pass filter (L37, L39, C151, C156, C159, C167, C176, C227–C229), and then applied to the antenna switching circuit (D12). The signal is applied to the antenna connector (CHASSIS UNIT; J1) after being passed through the low-pass filter (L44, L47, L48, L51, C190, C197, C203, C208, C210, C217, C218).

The bias current of the drive (Q18, Q20) and power (Q23) amplifiers is controlled by the APC circuit to stabilize the output power.

4-2-4 APC CIRCUIT (MAIN UNIT)

The APC (Automatic Power Control) circuit (IC6a, Q26) protects drive and power amplifiers from excessive currents and selects HIGH or LOW output power.

The output voltage from the power detector circuit (D14, D17) is applied to the differential amplifier (IC6a, pin 2), and the "T3" signal from the D/A converter (IC5, pin 23) is applied to the other input for reference.

When the driving current increases, the input voltage of the differential amplifier (IC6a, pin 2) will be increased. In such cases, the differential amplifier output voltage (pin 1) is decreased to reduce the drive current.

Q26 is controlled by the TXC signal from the expander IC (IC2, pin 14) to select HIGH or LOW output power.

4-3 PLL CIRCUITS

4-3-1 PLL CIRCUIT (MAIN AND LOGIC UNITS)

A PLL circuit provides stable oscillation of the transmit frequency and receive 1st LO frequency. The PLL output compares the phase of the divided VCO frequency to the reference frequency. The PLL output frequency is controlled by the divided ratio (N-data) of a programmable divider.

An oscillated signal from the TX and RX-VCO circuits passes through the LO and buffer amplifiers (Q9, Q12) is applied to the PLL IC (IC1, pin 6) and is prescaled in the PLL IC based on the divided ratio (N-data). The reference signal is generated at the reference oscillator (X1) and is also applied to the PLL IC. The PLL IC detects the out-of-step phase using the reference frequency and outputs it from pin 15. The output signal is passed through the loop filter(Q2) and is then applied to the TX and RX-VCO circuits as lock voltage.

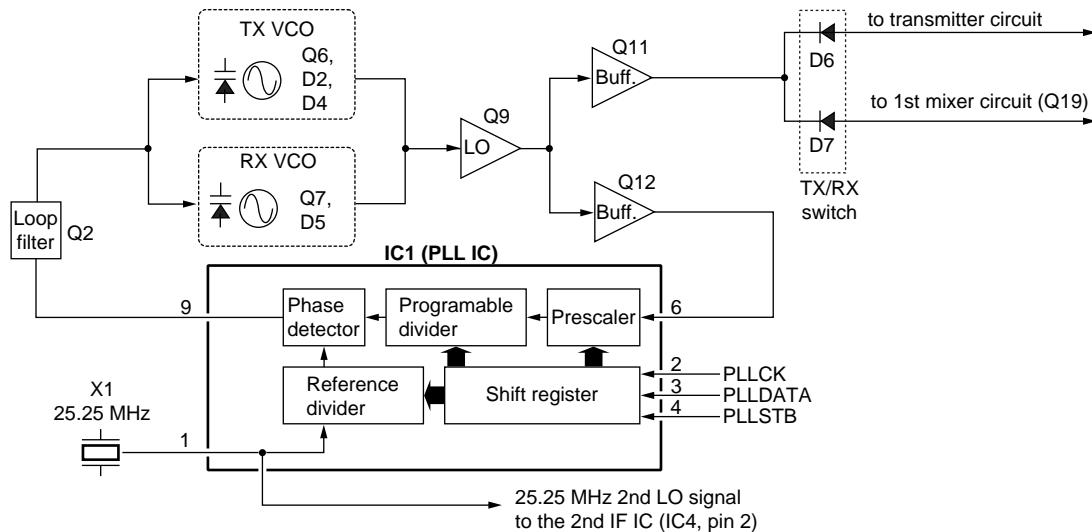
The lock voltage is also used for the receiver tunable bandpass filters to match the filter's center frequency to the desired receive frequency. The lock voltage is passed through the loop filter (Q2), and then applied to the DC amplifier (Q10). The amplified signal is applied to the CPU (LOGIC unit; IC7, pin 98) via the "LVIN" signal. The signal is analyzed at the CPU, and then applied to bandpass filters (D9–D11, D13) as "T1", "T2", "T3" signals via the D/A converter.

4-3-2 VCO CIRCUIT (MAIN UNIT)

The VCO circuit contains a separate TX-VCO (Q6, D2, D4) and RX-VCO (Q7, D5). The oscillated signal is amplified at the LO (Q9) and buffer (Q11) amplifiers, and is then Tx/Rx switching circuit (D6, D7). Then Tx and Rx signals are applied to the pre-driver (Q17) and 1st mixer circuit (Q19) respectively.

A portion of the signal from LO amplifier (Q9) is amplified at the buffer amplifier (Q12) and is then fed back to the PLL IC (IC1, pin 6) as the comparison signal.

• PLL CIRCUIT



4-4 POWER SUPPLY CIRCUITS VOLTAGE LINE

LINE	DESCRIPTION
HV	The voltage from the power supply.
SWHV	The same voltage as HV line which is controlled by the HVSW circuit (Q28, Q30, Q31). When the [POWER] switch is pushed, the CPU outputs the "PWRON" control signal via the expander IC (IC2). The signal is applied to the HVSW circuit to turn the circuit ON. The output voltage is applied to the drive amplifier (Q18), +8V regulator circuit (IC7), etc.
C5V	Common 5 V for the CPU converted from the HV line by the C5V regulator circuit (IC8). The circuit outputs the voltage regardless of the power ON/OFF condition. The output voltage is applied to the EEPROM (LOGIC UNIT; IC5), CPU (LOGIC UNIT; IC7), etc.
+8V	Common 8 V converted from the 13.8 V line by the +8V regulator circuit (IC7). The output voltage is applied to the LO (Q9) and buffer (Q11) amplifiers, etc.
+5V	Common 5 V converted from the +8 V line by the +5V regulator circuit (Q21, Q22).
T8	Transmit 8 V controlled by the T8V regulator circuit (Q14, Q15) using the "TXC" signal from the I/O expander IC (IC2).
R5V	Receive 5 V controlled by the R5V regulator circuit (Q25) using "RXC" signal from the I/O expander IC (IC2). The output voltage is applied to the FM IC IC (IC4), IF (Q16) and RF (Q27) amplifiers, etc.

4-5 PORT ALLOCATIONS

4-5-1 CPU (LOGIC UNIT: IC7)

Pin number	Port name	Description
1	DETO	Input port for the weather alert signal detection.
9	RESET	Input port for reset signal.
11	CSHIFT	Outputs reference oscillator for the CPU control signal.
12	SCK	Outputs serial clock signal to the expander IC (MAIN unit; IC2, pin 3), D/A convertor IC (MAIN unit, IC5, pin 7), etc.
14	SO	Outputs serial signals to the D/A convertor IC (MAIN unit; IC5, pin 8),etc.
15	PTT	Input port for the [PTT] switch. High : While [PTT] switch is pushed.
16	CLIN	Input port for the cloning signal.
17	CLOUT	Outputs the cloning signal.
19	NOIS	Input port for noise signals (pulse type).
20	COLOR	Outputs LCD back light color control signal. Low : While choosing umber color.
21 22	DIM1 DIM0	Outputs LCD contrast control signal.
23	REMO	Input port for the remote signals from a remote microphone (HM-133V) via the [MIC] jack.
26	UNLK	Input port for PLL unlock signal from the PLL IC (MAIN unit; IC1, pin 14).
32–35	COM4–COM1	Outputs LCD common signals.
36–39	KR3–KR0	Input port for initial matrix. Low : While keys are pushing.
40	EXTMIC	Input port for the remote control microphone (HM-133V) connecting detection. Low : While HM-133V is connected.
41	OPV2	Input port for the optional unit detection signal.
44	PLLSTB	Outputs strobe signals to the PLL IC (IC1, pin 4).
45	PLLCK	Outputs PLL IC (IC1, pin 2) clock signal.
47	EXSTB OPV3	<ul style="list-style-type: none"> • Outputs strobe signal to the expander IC (IC2, pin 1). • Input port for the optional unit detection signal.
49–51	OPT1–OPT3	I/O port for optional unit control signal.
53	DUSE	Outputs low-pass filter cut-off frequency control signal when DTCS is activated.

Pin number	Port name	Description
54	ESCK	Outputs EEPROM (LOGIC unit; IC5, pin 6) clock signal.
55	ESDA	I/O port for the data signals from/to the EEPROM (LOGIC unit; IC5, pin 5).
56–88	SEG1–SEG32	Output LCD driver signals.
90	CTCC	Outputs CTCSS and DTCS tone signal.
91	TONE	Outputs DTMF, BEEP and 1750 Hz tone signal.
95	SQLV	Input port for the squelch level detection.
96	MICUD	Input port for the microphone up/down signal while connecting the microphone.
97	SD	Input port for the RSSI detection.
98	LVIN	Input port for the PLL lock voltage.
99	PDET	Input port for the power detector voltage.
100	TEMP	Input port for the transceiver's internal tempareture detection.

4-5-2 D/A CONVERTOR IC (MAIN UNIT: IC5)

Pin number	Port name	Description
2	MOD	Outputs transmit devetion control signal.
3	SQLATT	Outputs attenuator control signal.
10	T1	<ul style="list-style-type: none"> • Outputs tunable bandpass filter control signal while receiving. • Outputs TX power control signal while transmitting.
11, 23	T2, T3	Output tunable bandpass filter control signals.
14	SQLIN	Outputs squelch control signal.
15	DTC	Outputs DTCS's gradient control signal.
22	FC	Outputs reference frequency control signal to X1.

4-5-3 I/O EXPANDER IC (MAIN UNIT: IC2)

Pin number	Port name	Description																
4 7 12	FANC1 FANC FANC2	<p>Outputs cooling fan control signal. The fan speed is depended as shown below.</p> <table border="1"> <thead> <tr> <th>Fan speed</th> <th>FANC</th> <th>FANC1</th> <th>FANC2</th> </tr> </thead> <tbody> <tr> <td>Hi</td> <td>H</td> <td>H</td> <td>H</td> </tr> <tr> <td>Middle</td> <td>H</td> <td>L</td> <td>H</td> </tr> <tr> <td>Low</td> <td>H</td> <td>H</td> <td>L</td> </tr> </tbody> </table>	Fan speed	FANC	FANC1	FANC2	Hi	H	H	H	Middle	H	L	H	Low	H	H	L
Fan speed	FANC	FANC1	FANC2															
Hi	H	H	H															
Middle	H	L	H															
Low	H	H	L															
6	AFMUTE	Outputs AF mute circuit control signal. High : While AF mute is ON.																
11	SHIFT	Outputs TX and RX VCO's regulator control signals. High : While receiving. Low : While transmitting.																
13	RXC	Outputs R5 regulator control signal. Low : While receiving.																
14	TXC	Outputs TX power control signal. High : While transmitting.																

SECTION 6 MECHANICAL PARTS AND DISASSEMBLY

6-1 IC-V8000

[CHASSIS PARTS]

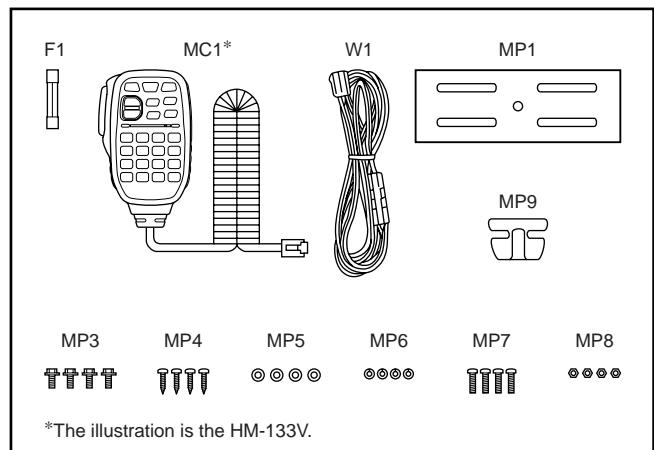
REF. NO.	ORDER NO.	DESCRIPTION	QTY.
J1	6510004880	Connector MR-DSE-01	1
MF1	2710000720	Fan DF125020BH	1
MP1	8010018801	2509 Chassis-1	1
MP2	8030056880	2509 Fan holder	1
MP3	8110007670	2509 Cover	1
MP4	8810008660	Screw BT M3 x 8 NI-ZU (BT)	2
MP5	8810008660	Screw BT M3 x 8 NI-ZU (BT)	1
MP6	8810008660	Screw BT M3 x 8 NI-ZU (BT)	13
MP7	8810008030	Screw H M2.6 x 8	2
MP9	8810005160	Hex socket bolt M3 x 20 ZK	3
MP10	8810009610	Screw M2.6 x 6 ZK	4
MP11	8930039610	Thermally sheet (C)	3
MP14	8810010140	Screw M3 x 30 ZK	4
MP15	8510014500	2509 Shield plate	1
MP16	8930057880	Rubber sheet (BA)	1
MP17	8930048390	Sheet (BZ)	1

[ACCESSORIES]

REF. NO.	ORDER NO.	DESCRIPTION	QTY.
F1	5210000080	Fuse (20A)	1
MC1	0880001060 0800005740 0800005820 0800005720	Microphone HM-133 ACC [CSA-1], [USA-2] Microphone HM-118TN ACC [CSA] Microphone HM-118N ACC [SEA] Microphone HM-118TAN ACC [USA-3]	1 1 1 1
W1	8900010990	Cable OPC-1132 ACC	1
MP1	8010016730	150 Mobil bracket	1
MP2	8930041170	452 Felt	2
MP3	8820000530	Flange bolt M4 x 8	4
MP4	8810000950	Screw A0 M5 x 16	4
MP5	8850000180	Flat washer M5 SUS	4
MP6	8850000500	Spring washer M5 SUS	4
MP7	8810000470	Screw M5 x 12 (+/-)	4
MP8	8830000250	Nut M5 SUS	4
MP9	8930007300	MIC hanger	[USA] only 1

[LOGIC BOARD]

REF. NO.	ORDER NO.	DESCRIPTION	QTY.
DS19	5030002250	L1-0256TAM	1
S9	2250000370	Encoder EVQ-VENF01 24B	1
SP1	2510001150	Speaker 045P0804	1
WS1	8600036880	FX2509 P01L0	1
EP9	8930057360	LCD contact SRCN-2509-SP-N-W	1
MP1	8210018440	2509 Front panel	1
MP2	8930057300	2509 LCD filter	1
MP3	8210018450	2509 Reflectort	1
MP4	8930056850	2509 A-keyboard	1
MP5	8930056860	2509 B-keyboard	1
MP6	8930056870	2509 C-keyboard	1
MP7	8510014340	2509 Front plate	1
MP8	8610010602	Knob N-267-2	2
MP9	8610011140	Knob N-291	1
MP12	8810008760	Screw B0 M2 x 8 NI-ZU (BT)	4

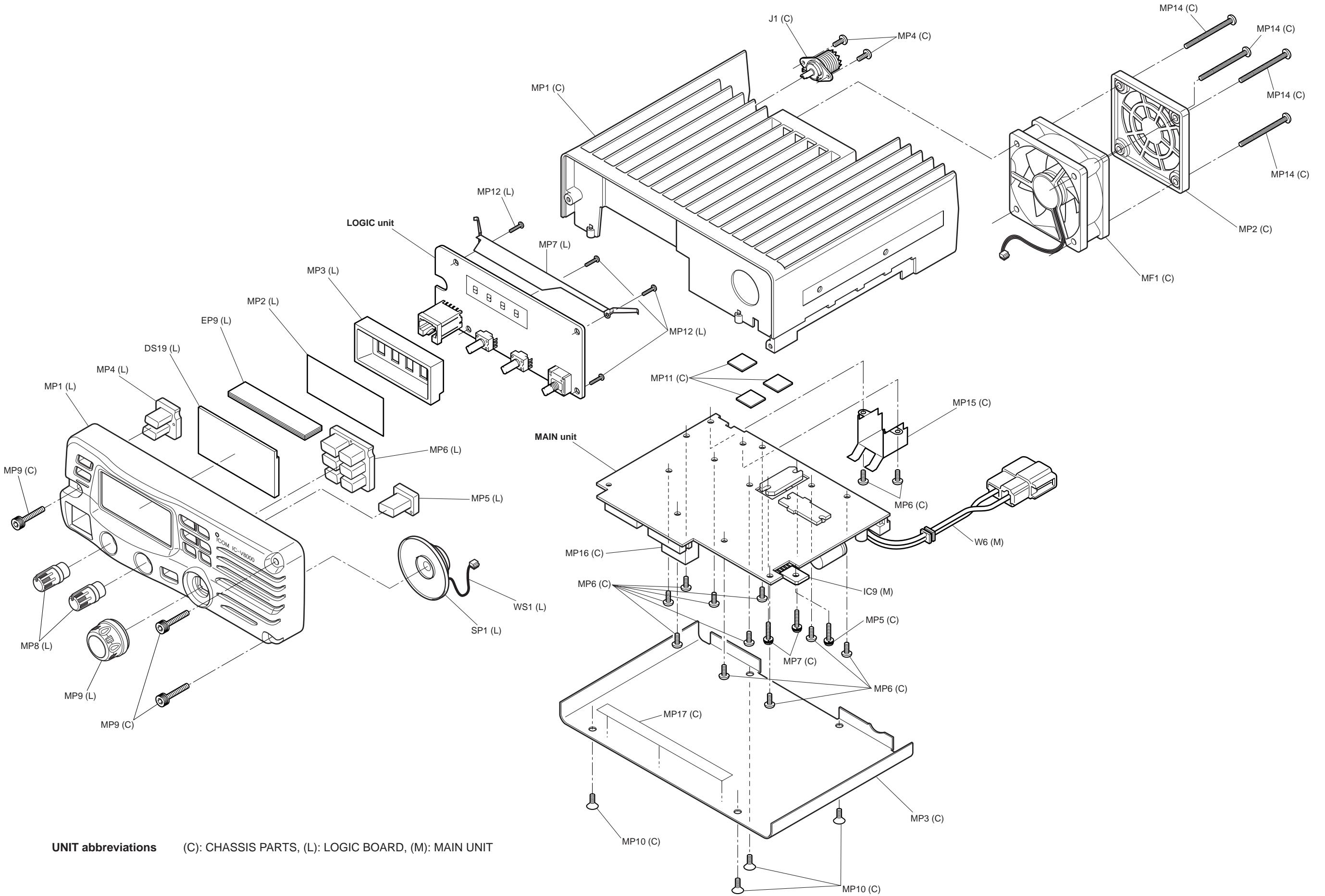


*The illustration is the HM-133V.

Screw abbreviations A0, B0, BT: Self-tapping
NI-ZU: Nickel-Zinc
ZK: Black
SUS: Stainless

[MAIN UNIT]

REF. NO.	ORDER NO.	DESCRIPTION	QTY.
W6	8900010980	Cable OPC-1131	1
MP1	8410002380	2399 Heatsink	1
MP2	8510014470	2509 VCO case	1
MP3	8510014460	2509 VCO cover	1



6-2 HM-133V

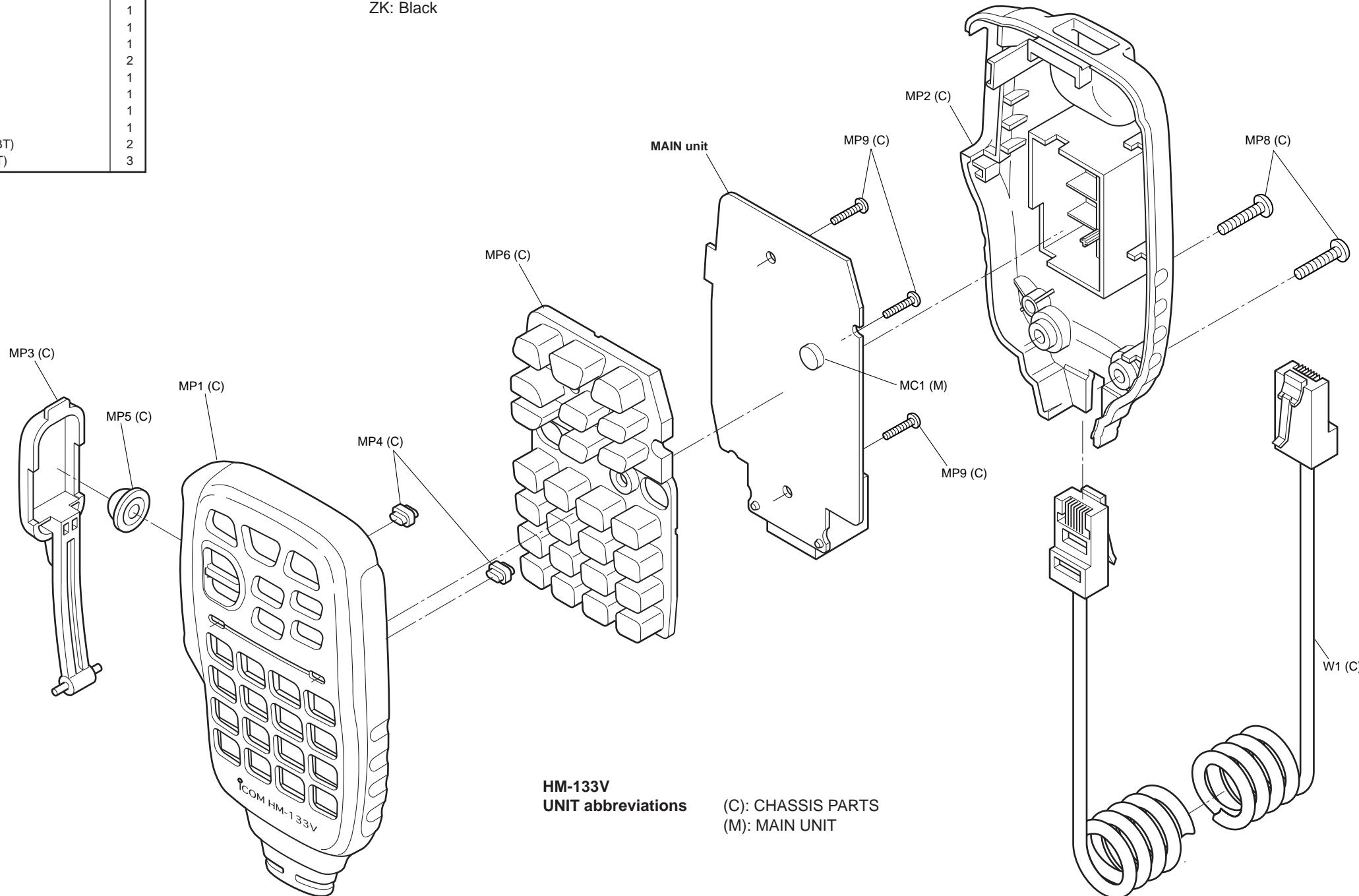
[CHASSIS PARTS]

REF. NO.	ORDER NO.	DESCRIPTION	QTY.
W1	8900010450	Cable OPC-153	1
MP1	8210018830	2539 Front panel	1
	8210018890	2539 Front panel (A)	1
	8210018910	2539 Front panel (B)	1
MP2	8210018840	2539 Rear panel	1
MP3	8930057380	2539 PTT button	1
MP4	8930057390	2539 LED lens	2
MP5	8930057570	SW rubber	1
MP6	8930057520	2539 Keyboard	1
	8930057710	2539 Keyboard (A)	1
	8930057700	2539 Keyboard (B)	1
MP8	8810009370	Screw B0 M3 x 12 ZK (BT)	2
MP9	8810009560	Screw B0 M2 x 6 ZK (BT)	3

[MAIN UNIT]

REF. NO.	ORDER NO.	DESCRIPTION	QTY.
MC1	7700002310	Microphone EM-140	1

Screw abbreviations B0, BT: Self-tapping
ZK: Black



SECTION 7 SEMI-CONDUCTOR INFORMATION

• TRANSISTOR AND FET'S

2SA1576 R (Symbol: FR)	2SA1734 (Symbol: LB)	2SA1586 GR (Symbol: S0)	2SB1132 R (Symbol: BARB)	2SC2712 BL (Symbol: L0)
2SC3356 (Symbol: R22)	2SC4116 BL (Symbol: LL)	2SC4116 GR (Symbol: LG)	2SC4213 B (Symbol: AB)	2SC4226 R25 (Symbol: R25)
2SC4406 4 (Symbol: JT)	2SC4684 (LB) (Symbol: 2-7B2A)	2SK1069 4 (Symbol: FJ)	2SK3074 (Symbol: UW)	2SK3075 (Symbol: UB F)
3SK272 (Symbol: K)	DTA113 ZU (Symbol: 111)	DTA114 EU (Symbol: 16)	DTA143 TUA (Symbol: 93)	DTA144 EU (Symbol: 16)
DTB113 ZK (Symbol: G11)	DTC114 EU (Symbol: 24)	DTC143 ZU (Symbol: 123)	DTC144 EU (Symbol: 26)	DTC144 TU (Symbol: 06)
RD70HVF1 (Symbol: RD70HVF1)	XP4601 (Symbol: 5C)			

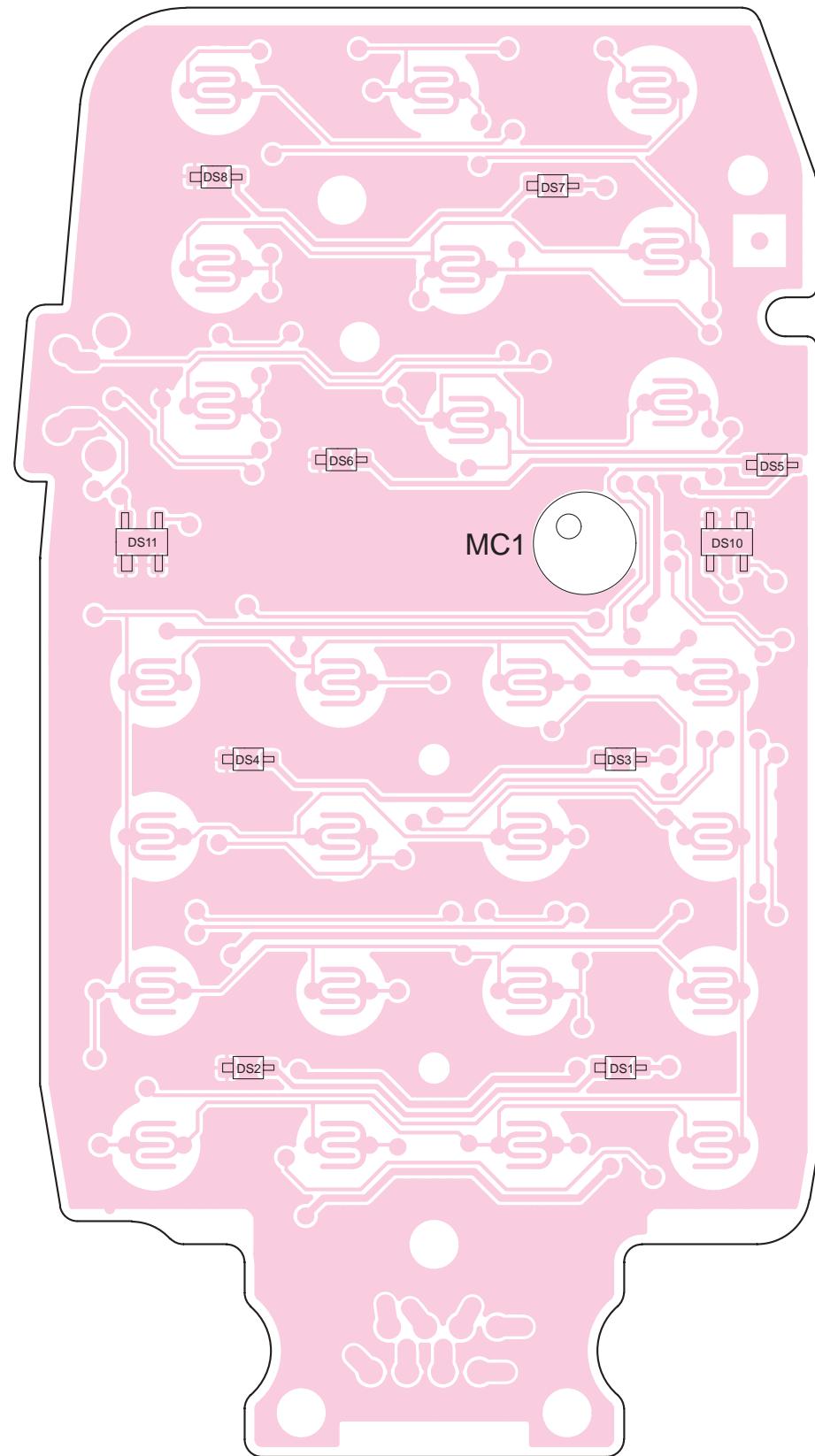
• DIODES

1SS133 (Symbol: Yellow line)	1SS355 (Symbol: A)	DA221 (Symbol: K)	DAN222 (Symbol: N)	DSA3A1 (Symbol:)
HVC350B (Symbol: BO)	HVC375B (Symbol: B8)	HVC376B (Symbol: B9)	HVU131TRF (Symbol: P1)	MA2S111 (Symbol: A)
MA2S728 (Symbol: B)	MA742 (Symbol: M1U)	MA77 (Symbol: 4B)	MA8056M (Symbol: 5-6)	MA8075 L (Symbol: 7-5)
MA8091 M (Symbol: 9-1)	RD20E B2 (Symbol: 202)	XB15A308 (Symbol: T8)	XB15A407 (Symbol: None)	

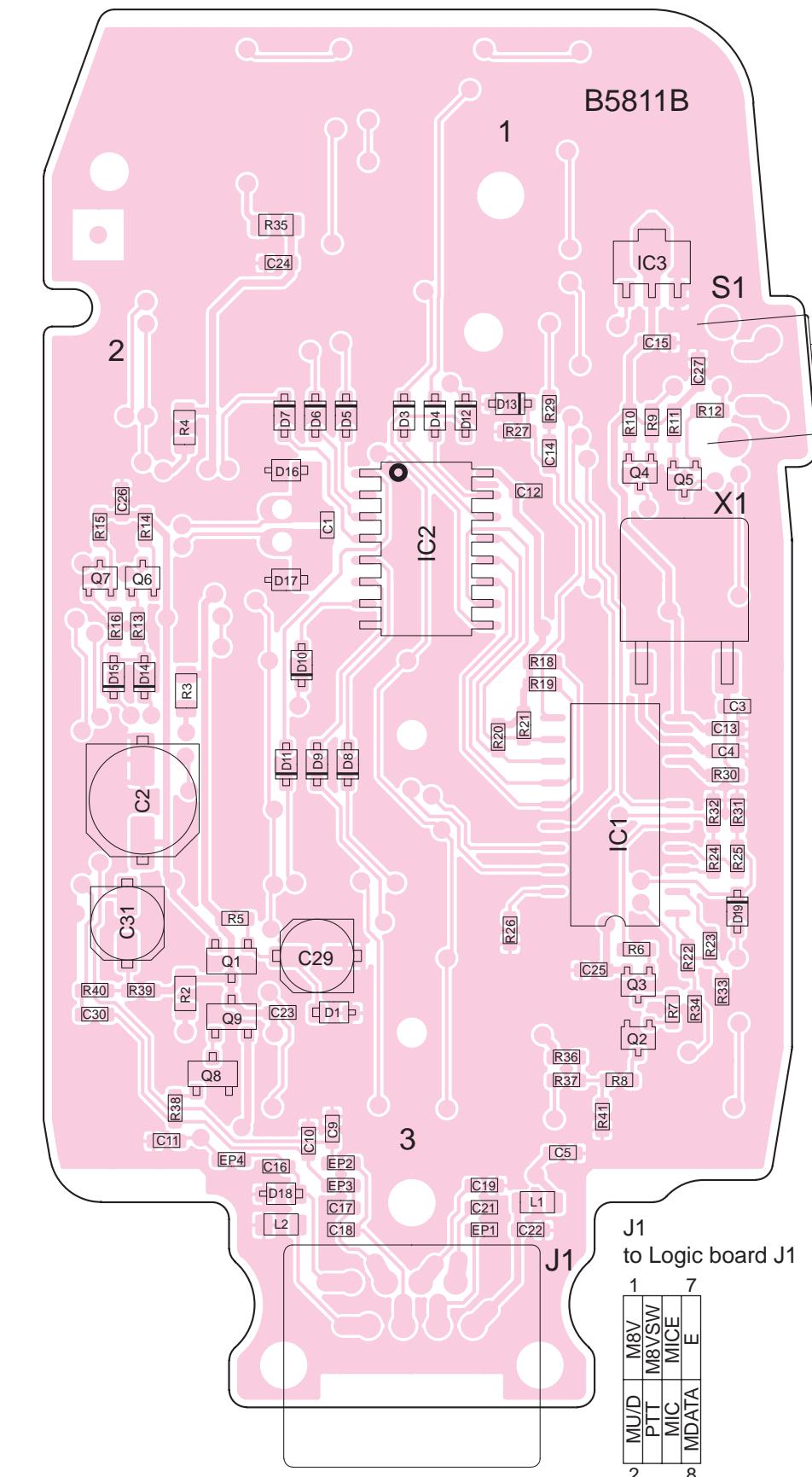
SECTION 8 BOARD LAYOUTS

8-1 HM-133V

• TOP VIEW

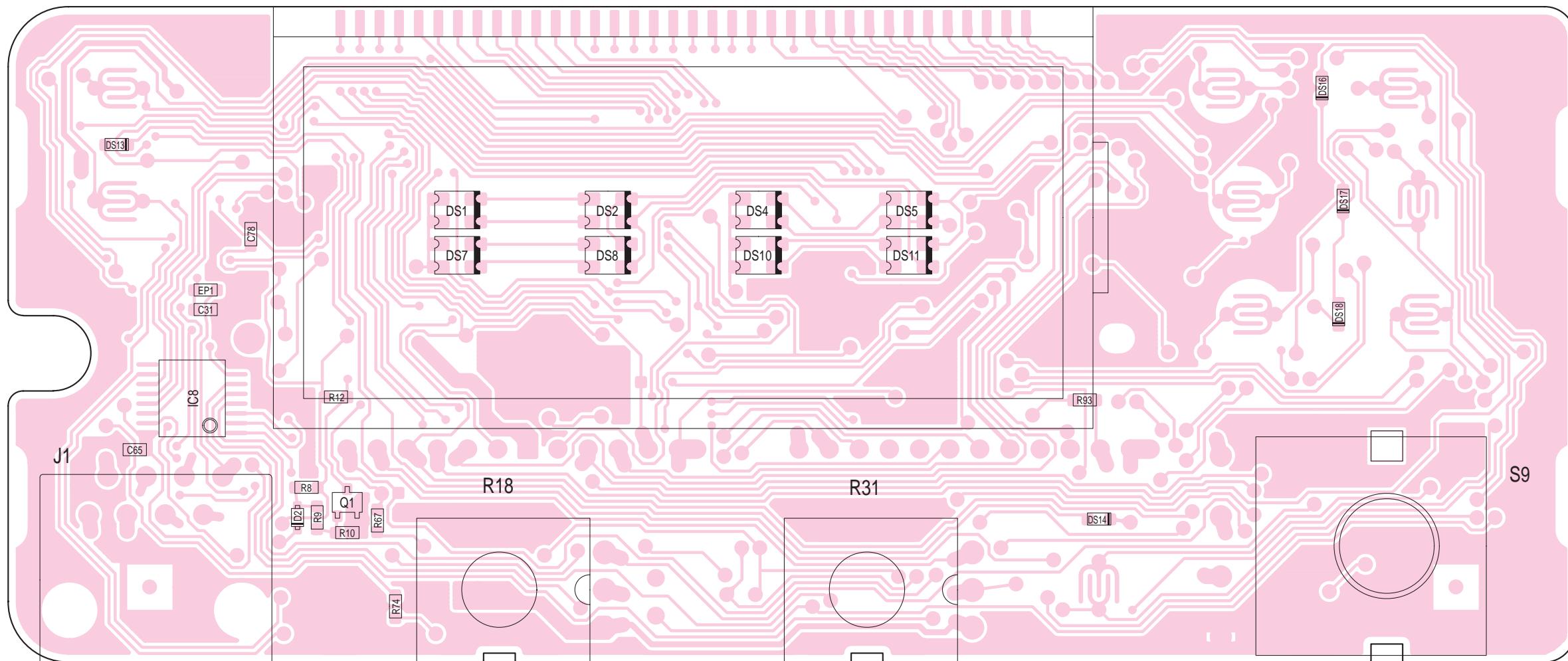


• BOTTOM VIEW



8-2 LOGIC BOARD

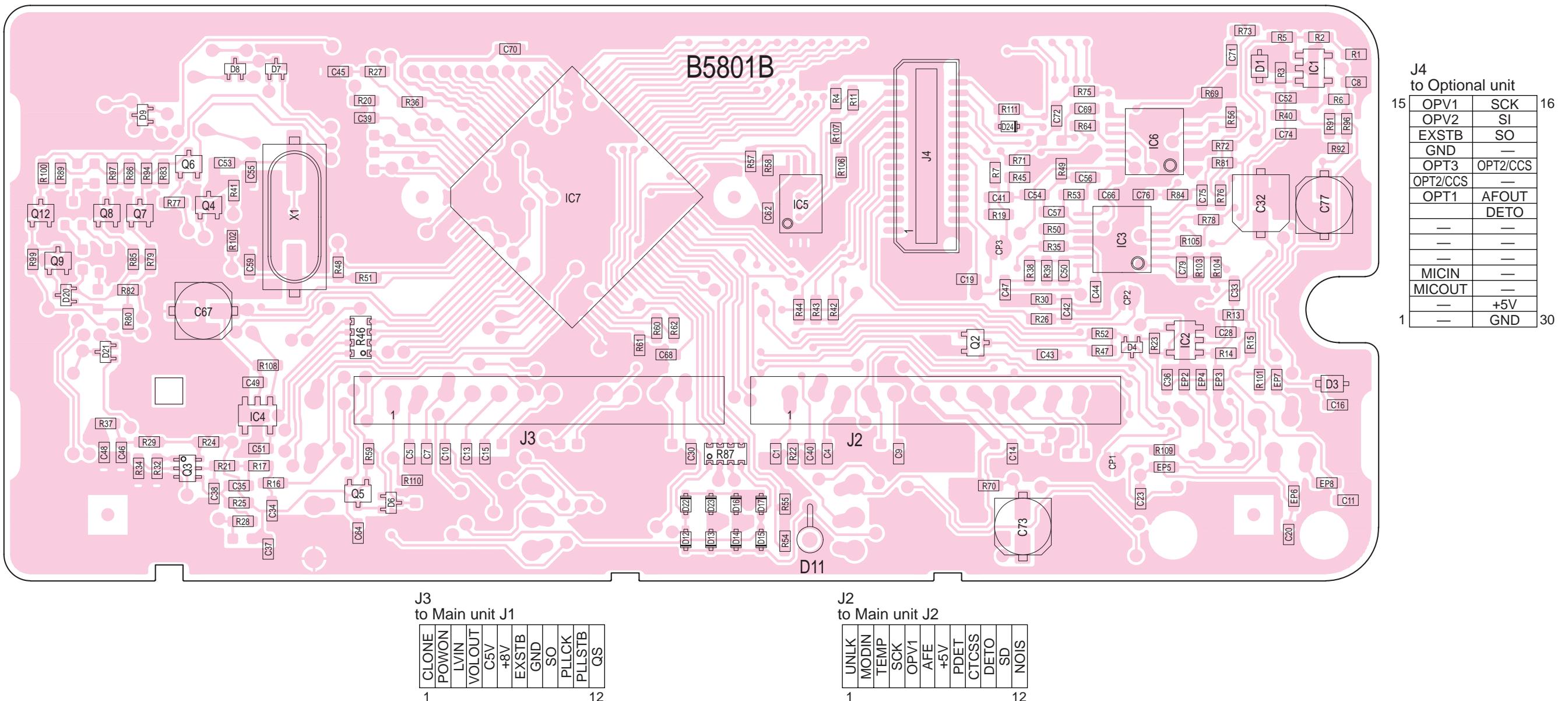
• TOP VIEW



J1
From External Microphone

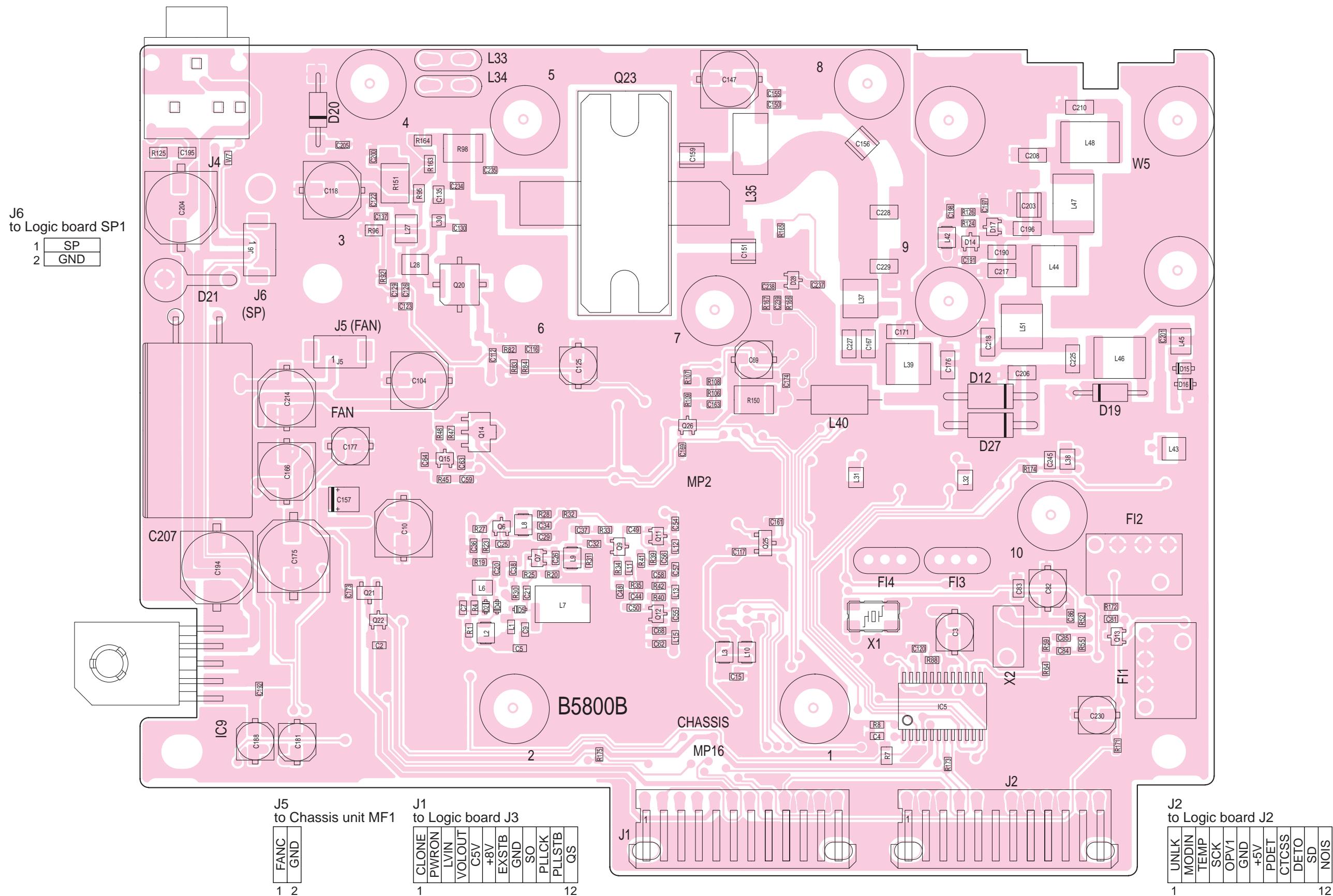
MICIN	GND
MIC	MICE
EXTMIC	PTT
MICUD	8V

• BOTTOM VIEW

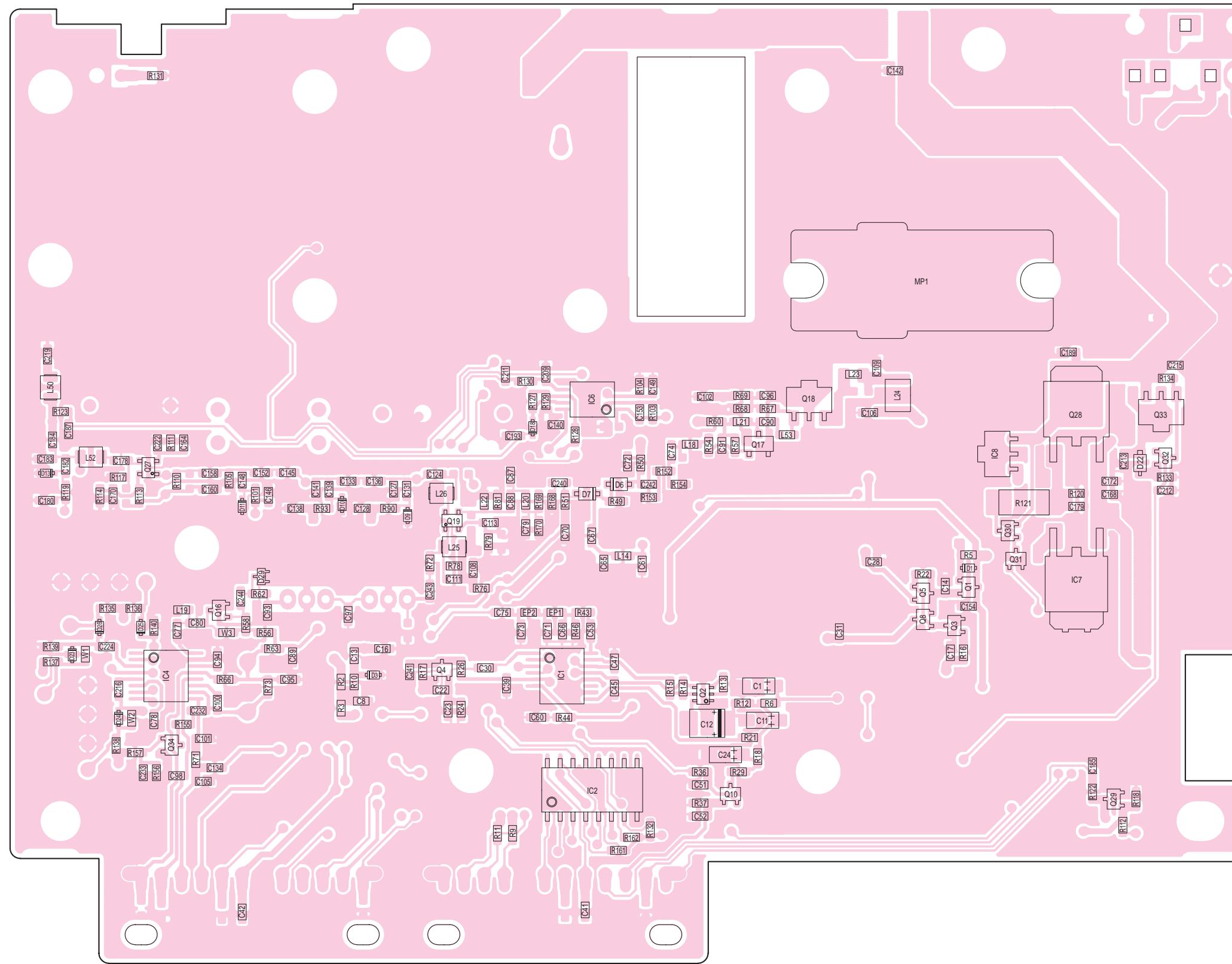


8-3 MAIN UNIT

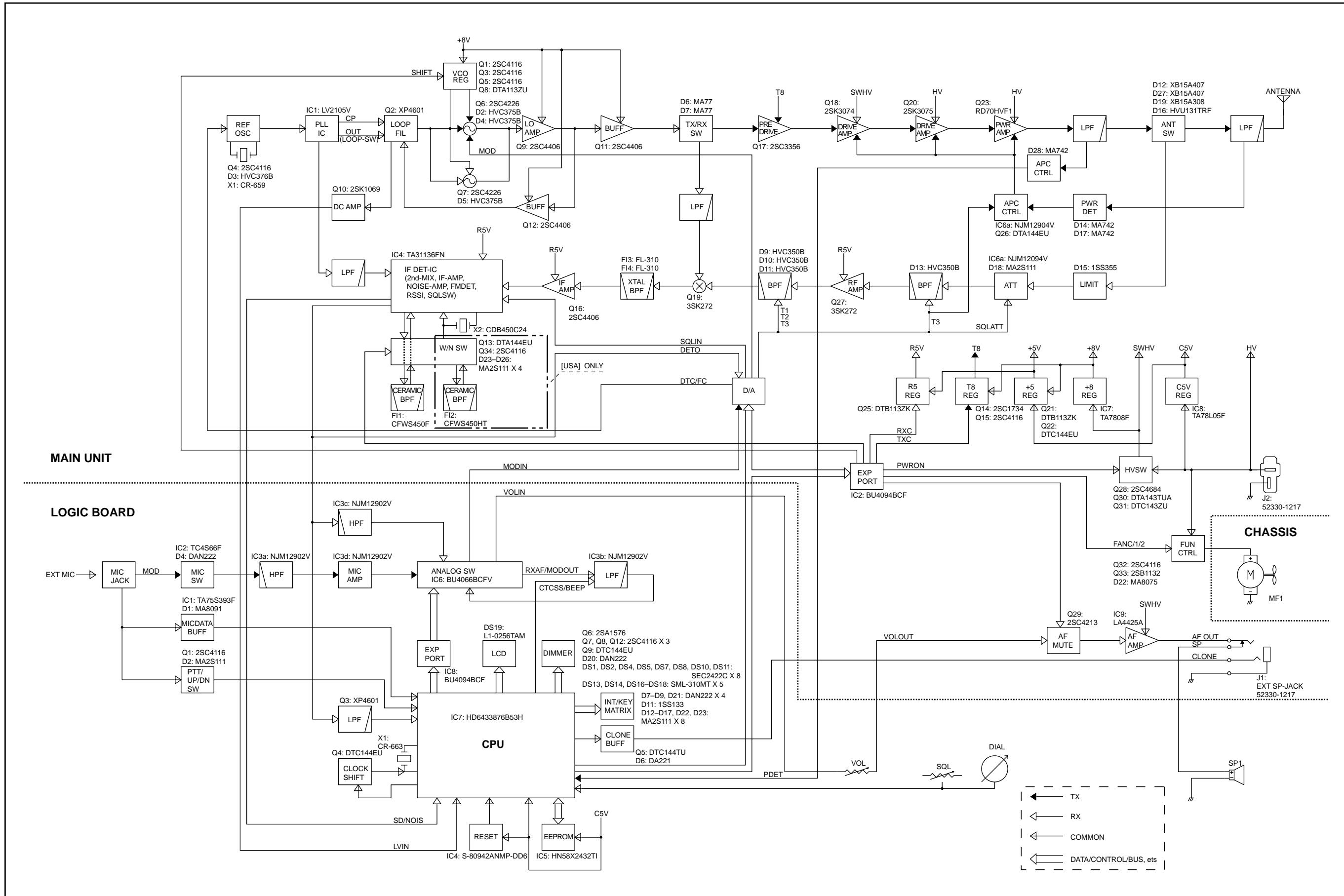
• TOP VIEW



• BOTTOM VIEW

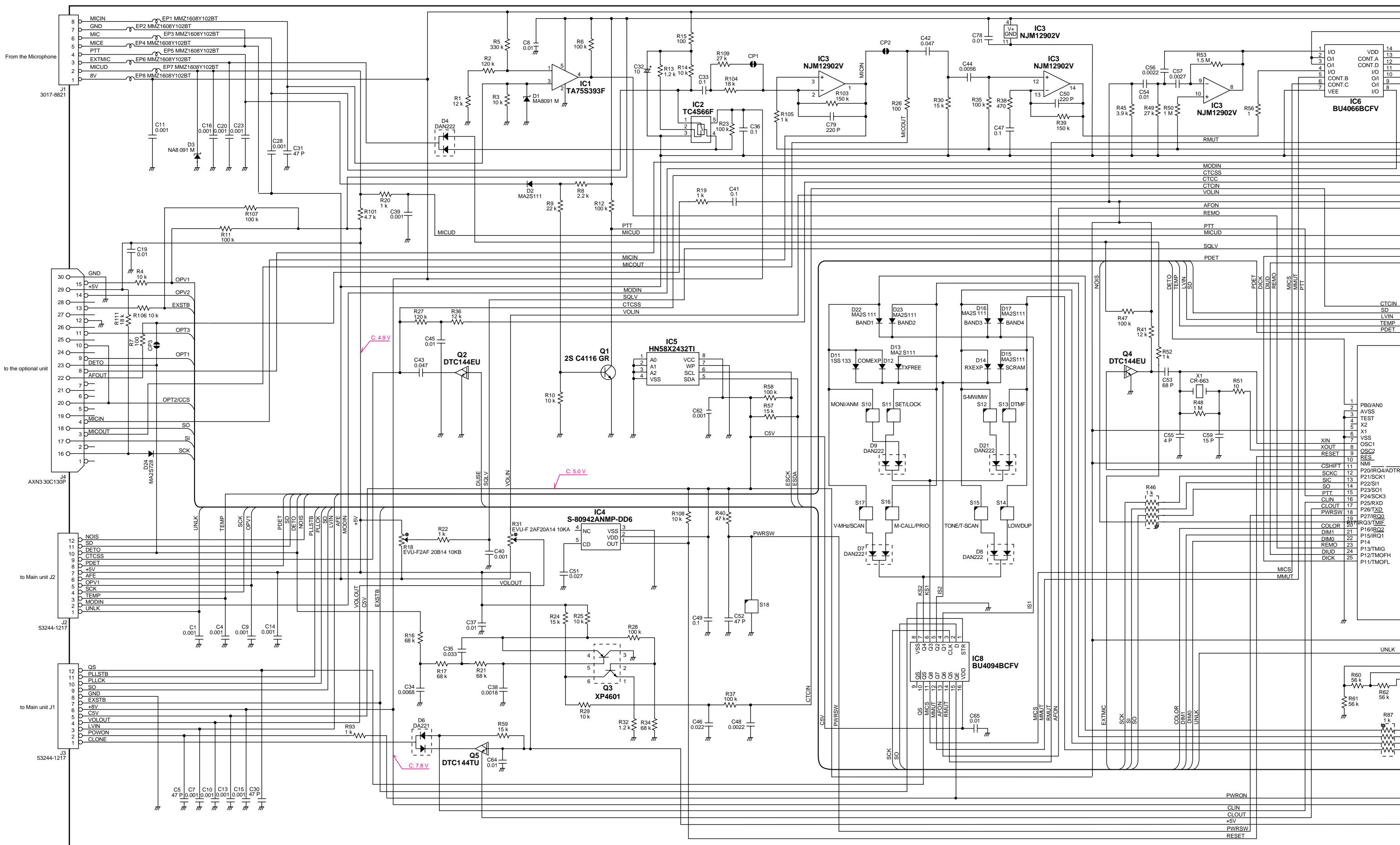


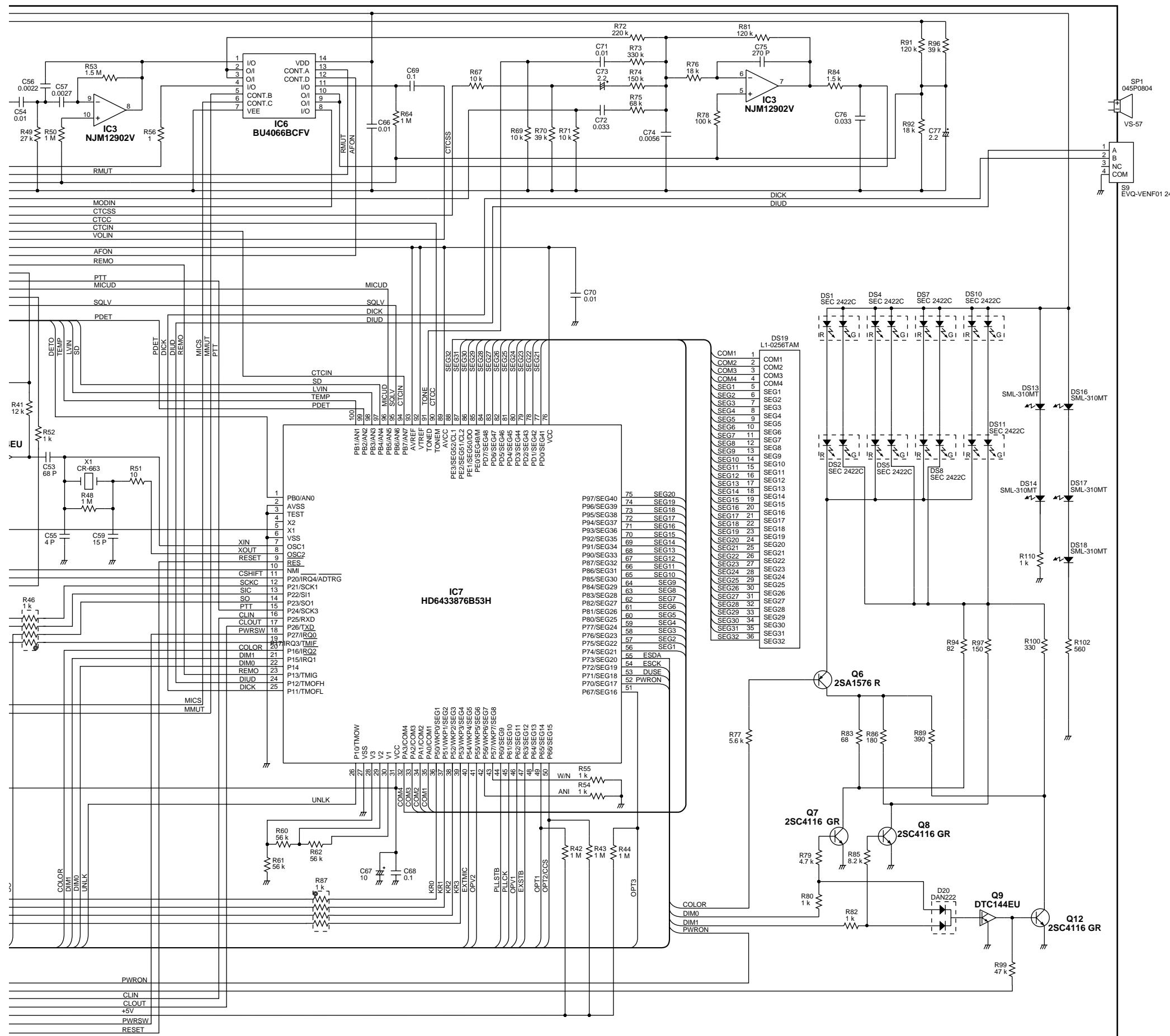
SECTION 9 BLOCK DIAGRAM



SECTION 10 VOLTAGE DIAGRAM

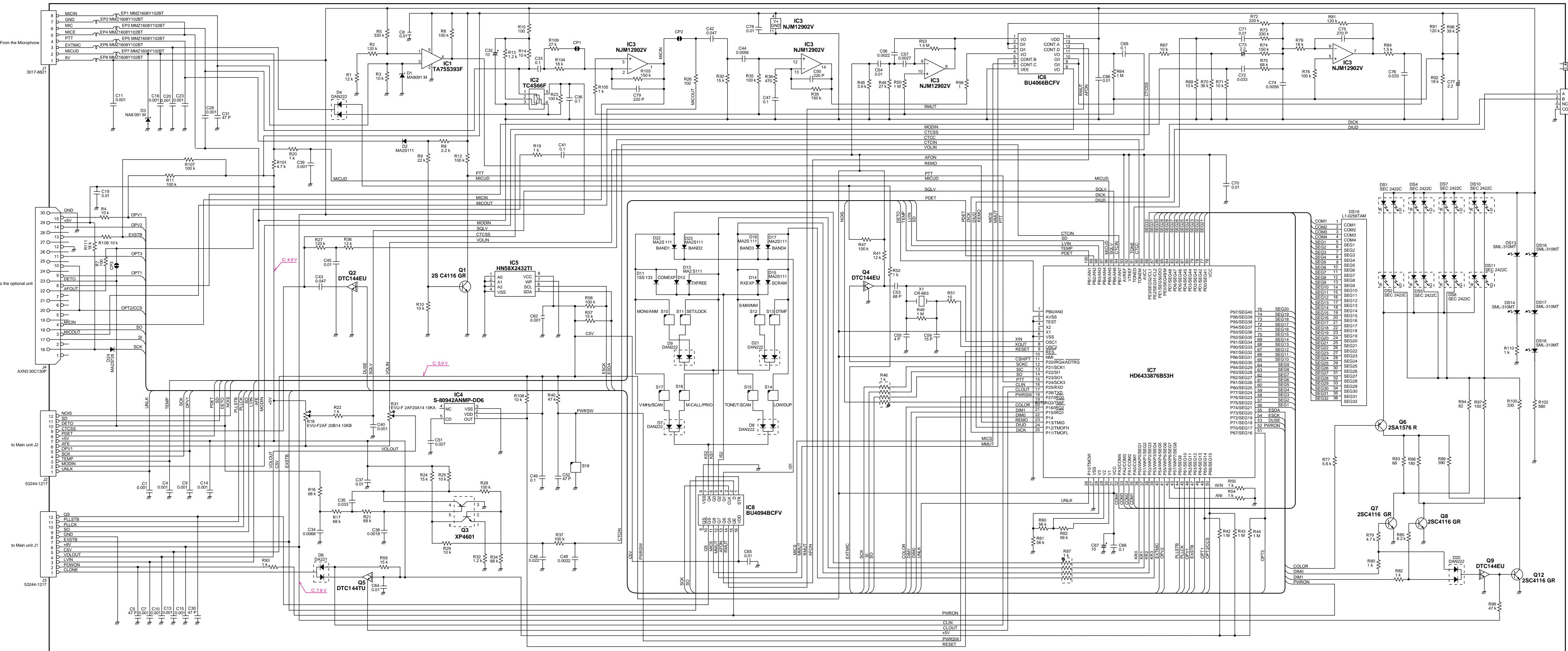
10-1 LOGIC BOARD



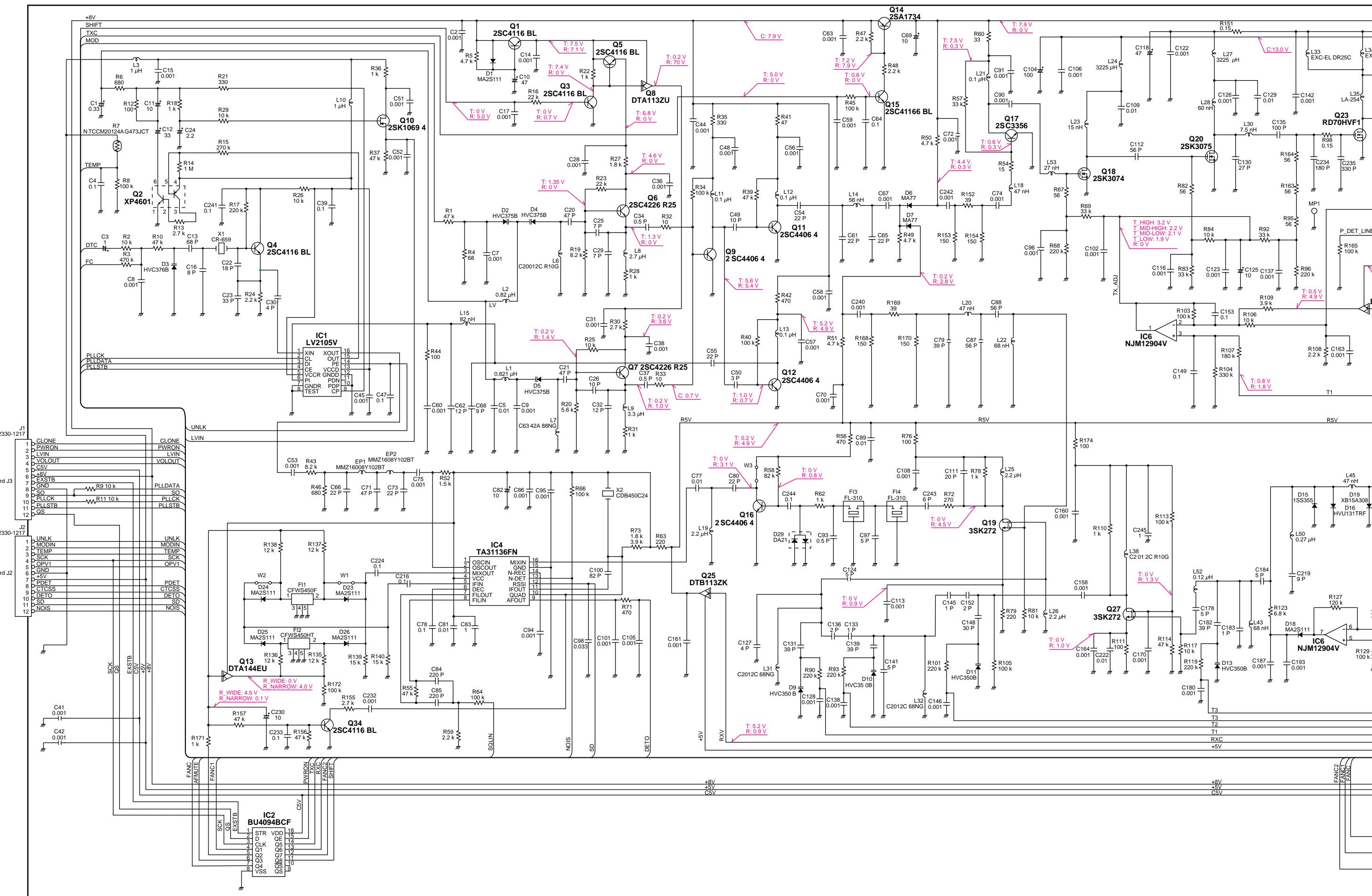


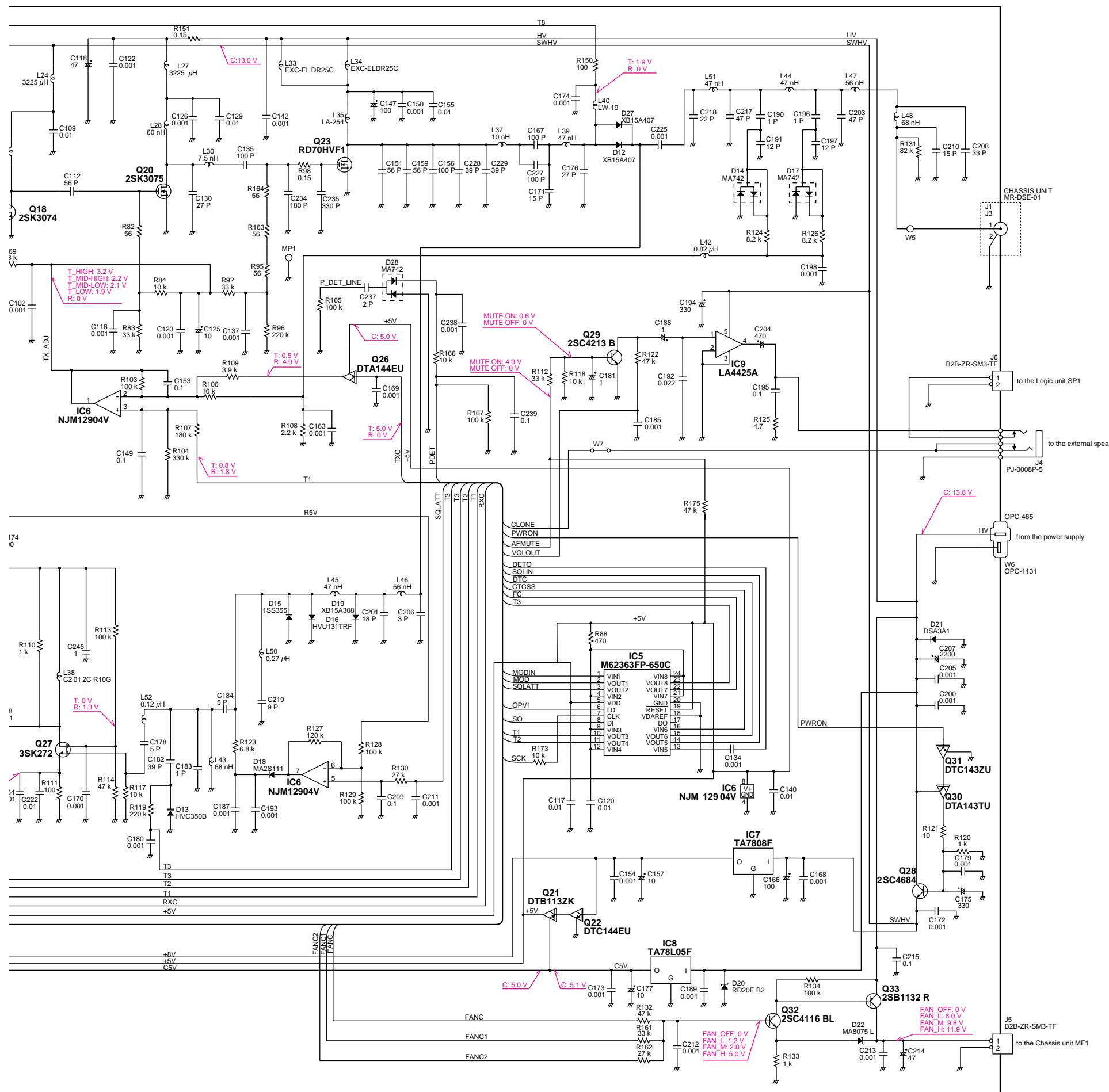
SECTION 10 VOLTAGE DIAGRAM

10-1 LOGIC BOARD

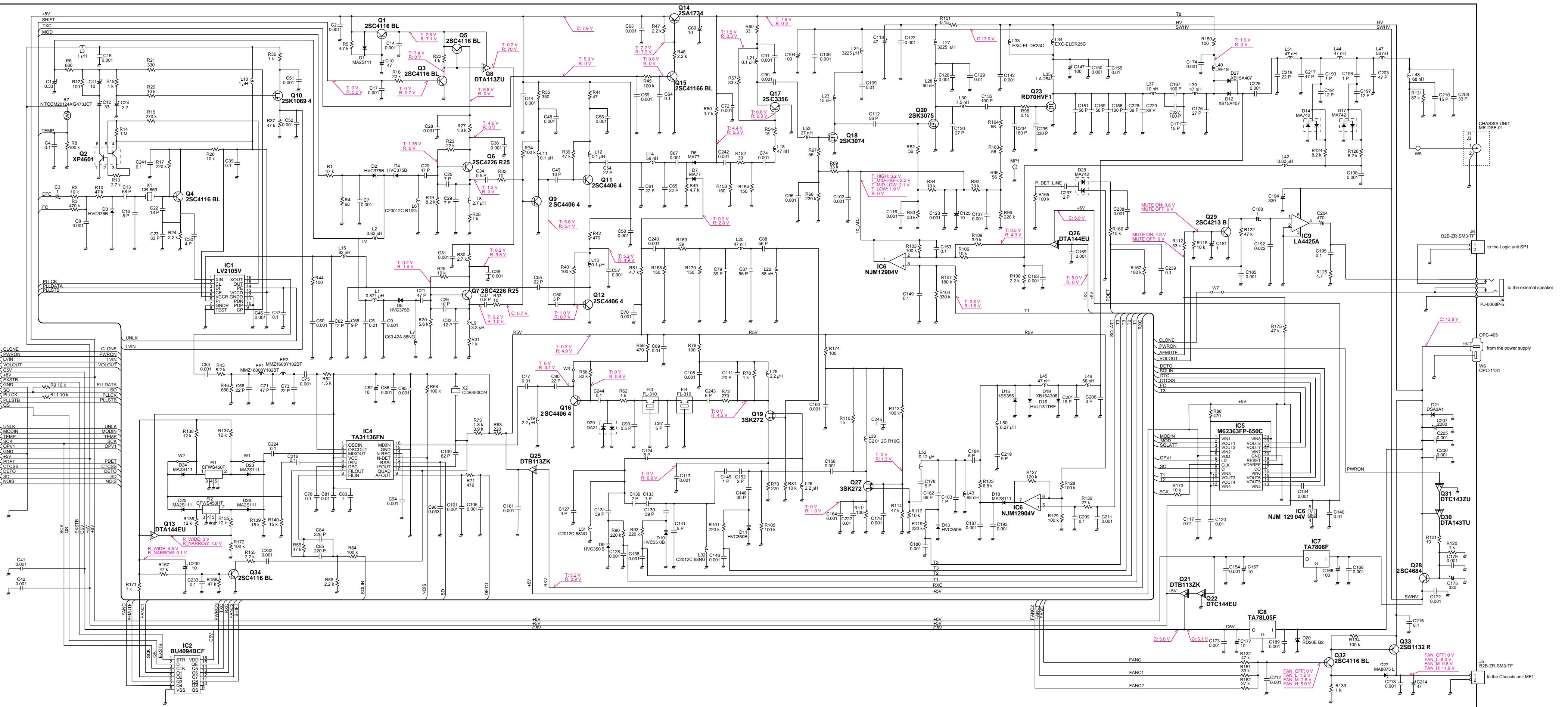


10-2 MAIN UNIT





10-2 MAIN UNIT



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