

HD74AC182

Carry Lookahead Generator

REJ03D0258-0200Z (Previous ADE-205-378 (Z)) Rev.2.00 Jul.16.2004

Description

The HD74AC182 is a high-speed carry lookahead generator. It is generally used with the HD74AC181 or HD74AC381 4-bit arithmetic logic unit to provide high-speed lookahead over word lengths of more than four bits.

Features

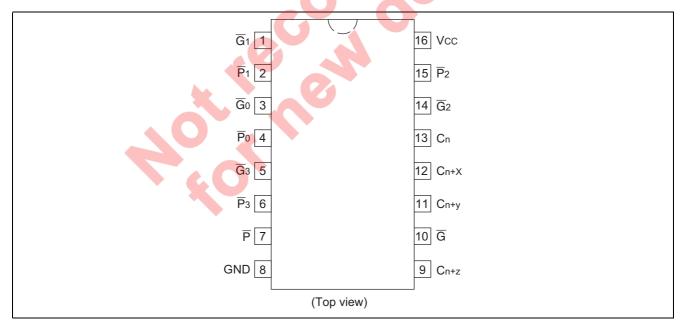
- Outputs Source/Sink 24 mA
- Ordering Information

Part Name	Package Type	Package Code	Package Abbreviation	Taping Abbreviation (Quantity)
HD74AC182FPEL	SOP-16 pin (JEITA)	FP-16DAV	FP	EL (2,000 pcs/reel)
HD74AC182RPEL	SOP-16 pin (JEDEC)	FP-16DNV	RP	EL (2,500 pcs/reel)

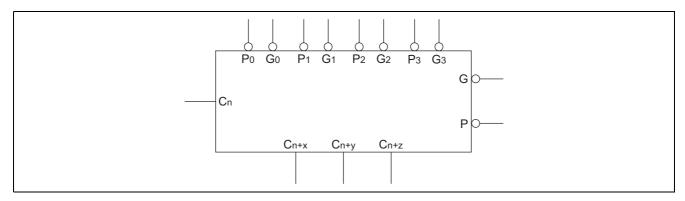
Notes: 1. Please consult the sales office for the above package availability.

2. The packages with lead-free pins are distinguished from the conventional products by adding V at the end of the package code.

Pin Arrangement



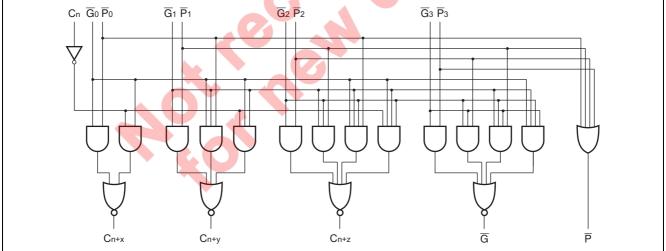
Logic Symbol



Pin Names

Cn	Carry Input
$egin{array}{c} \overline{\mathrm{G}}_0, \overline{\mathrm{G}}_2 \ \overline{\mathrm{G}}_1 \ \overline{\mathrm{G}}_3 \end{array}$	Carry Generate Inputs (Active Low)
$\overline{\mathbf{G}}_{1}$	Carry Generate Input (Active Low)
$\overline{\mathbf{G}}_3$	Carry Generate Input (Active Low)
$\overline{\overline{P}}_{0}^{3}, \overline{\overline{P}}_{1}$ $\overline{\overline{P}}_{2}^{2}$ $\overline{\overline{P}}_{3}^{3}$	Carry Propagate Inputs (Active Low)
$\overline{ extbf{P}}_2$	Carry Propagate Input (Active Low)
$\overline{\overline{P}}_3$	Carry Propagate Input (Active Low)
$\frac{C_{n+x}}{\overline{G}}$ to C_{n+z}	Carry Outputs
$\overline{\mathbf{G}}$	Carry Generate Output (Active Low)
\overline{P}	Carry Propagate Output (Active Low)

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Functional Description

The HD74AC182/HD74ACT182 carry lookahead generator accepts up to four pairs of Active Low Carry Propagate (\overline{P}_0) to \overline{P}_3) and Carry Generate (\overline{G}_0) to \overline{G}_3) signals and an Active High Carry input (Cn) and provides anticipated Active High carries $(C_{n+x}, C_{n+y}, C_{n+z})$ across four groups of binary adders. The HD74AC182/HD74ACT182 also has Active Low Carry Propagate (\overline{P}) and Carry Generate (\overline{G}) outputs which may be used for further level of lookahead. The logic equations provided at the outputs are:

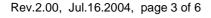
$$\begin{split} &C_{n+x}\!=G_0+P_0C_n\\ &C_{n+y}\!=G_1+P_1G_0+P_1P_0C_n\\ &C_{n+z}\!=\!G_2+P_2G_1+P_2P_1G_0+P_2P_1P_0C_n\\ &\overline{G}=\overline{G_3+P_3G_2+P_3P_2G_1+P_3P_2P_1G_0}\\ &\overline{P}=P_{\overline{3}}\overline{P_2P_1P_0} \end{split}$$

Also, the HD74AC182/HD74ACT182 can be used with binary ALUs in an active Low or active High input operand mode. The connections (Figure a) to and from the ALU to the carry lookahead generator are identical in both cases. Carries are rippled between lookahead blocks. The critical speed path follows the circled numbers. There are several possible arrangements for the carry interconnects, but all achieve about the same speed. A 28-bit ALU is formed by dropping the last HD74AC182/HD74ACT182.

Truth Table

Inputs								Outputs					
C _n	$\overline{G}_{\scriptscriptstyle{0}}$	\overline{P}_{0}	G₁	\overline{P}_1	$\overline{G}_{\scriptscriptstyle{2}}$	$\overline{P}_{\scriptscriptstyle 2}$	$\overline{G}_{\scriptscriptstyle{3}}$	\overline{P}_3	C _{n+x}	C _{n+y}	C _{n+z}	G	P
Χ	Н	Н							L				
L	Н	X							L				
Χ	L	X							Н				
Н	Х	L							Н				
X	Х	X	Н	Н						L			
X	Н	Н	Н	Х						Ĺ			
L	Н	X	Н	X						L			
X	X	X	L	X						H			
X	L	X	X	L						H			
Н	X	L	X	L						I			
X	X	X	X	X	Н	Н			X		L		
X	X	X	Н	Н	Н	X					L		
X	Н	Н	Н	X	Н	X					L		
L	Н	X	Н	X	Н	X					L		
X	X	X	X	X	L	X					Н		
X	X	X	L	X	X	L					Н		
X	L	X	X	L	X	L					Н		
Н	X	L	X	Ļ	X						Н		
	X		X	X	X	X	Н	Н				Н	
	X		X	X	H	Н	Н	X				Н	
	X		Н	Н	Н	X	Н	X				Н	
	Н		H	X	Н	X	Н	X				Н	
	X		X	X	X	X	L	X				L	
	X		X	X	L	X	X	L				L	
	X		L	X	X	L	X	L				L	
	L		X	L	Χ	L	X	L				L	
		Н		X		X		Χ					Н
		Χ		Н		X		Χ					Н
		Χ		X		Н		Χ					Н
		Χ		Χ		Χ		Н					Н
		L		L		L		L					L

H : High Voltage LevelL : Low Voltage LevelX : Immaterial





Absolute Maximum Ratings

Item	Symbol	Ratings	Unit	Condition
Supply voltage	V _{cc}	-0.5 to 7	V	
DC input diode current	I _{IK}	-20	mA	$V_1 = -0.5V$
		20	mA	$V_i = Vcc+0.5V$
DC input voltage	Vı	-0.5 to Vcc+0.5	V	
DC output diode current	I _{OK}	-50	mA	$V_{O} = -0.5V$
		50	mA	$V_O = Vcc+0.5V$
DC output voltage	Vo	-0.5 to Vcc+0.5	V	
DC output source or sink current	Io	±50	mA	
DC V _{CC} or ground current per output pin	I _{CC} , I _{GND}	±50	mA	
Storage temperature	Tstg	-65 to +150	°C	

Recommended Operating Conditions

Item	Symbol	Ratings	Unit	Condition
Supply voltage	V _{CC}	2 to 6	V	
Input and output voltage	V_{I}, V_{O}	0 to V _{cc}	V	
Operating temperature	Та	-40 to +85	°C	
Input rise and fall time	tr, tf	8	ns/V	V _{CC} = 3.0V
(except Schmitt inputs)				$V_{CC} = 4.5 \text{ V}$
V_{IN} 30% to 70% V_{CC}				$V_{CC} = 5.5 \text{ V}$

DC Characteristics

Item	Sym- bol	Vcc (V)	Ta = 25°C			-40 to 5°C	Unit	Condition	
			min.	typ.	max.	min.	max.		
Input Voltage	V _{IH}	3.0	2.1	1.5	- 1	2.1	_	V	$V_{OUT} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$
		4.5	3.15	2.25	-	3.15	—		
		5.5	3.85	2.75	_	3.85	—		
	V_{IL}	3.0	_	1.50	0.9	_	0.9		$V_{OUT} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$
		4.5	_	2.25	1.35	_	1.35		
		5.5	_	2.75	1.65	_	1.65		
Output voltage	V _{OH}	3.0	2.9	2.99	_	2.9	_	٧	$V_{IN} = V_{IL} \text{ or } V_{IH}$
		4.5	4.4	4.49	_	4.4	_		$I_{OUT} = -50 \mu A$
		5.5	5.4	5.49	_	5.4	_		
		3.0	2.58	_	_	2.48	_		$V_{IN} = V_{IL} \text{ or } V_{IH}$ $I_{OH} = -12 \text{ mA}$
		4.5	3.94	_	_	3.80	_		$I_{OH} = -24 \text{ mA}$
		5.5	4.94	_	_	4.80	_		$I_{OH} = -24 \text{ mA}$
	V _{OL}	3.0	_	0.002	0.1	_	0.1		$V_{IN} = V_{IL}$ or V_{IH}
		4.5	_	0.001	0.1	_	0.1		I _{OUT} = 50 μA
		5.5	_	0.001	0.1	_	0.1		
		3.0	_	_	0.32	_	0.37		$V_{IN} = V_{IL} \text{ or } V_{IH}$ $I_{OL} = 12 \text{ mA}$
		4.5	_	_	0.32	_	0.37		$I_{OL} = 24 \text{ mA}$
		5.5	_	_	0.32	_	0.37		$I_{OL} = 24 \text{ mA}$
Input leakage current	I _{IN}	5.5	_	_	±0.1	_	±1.0	μΑ	$V_{IN} = V_{CC}$ or GND
Dynamic output	I _{OLD}	5.5	_	_	_	86	_	mΑ	V _{OLD} = 1.1 V
current*	I _{OHD}	5.5	_	_	_	-75	_	mA	V _{OHD} = 3.85 V
Quiescent supply current	I _{cc}	5.5	_	_	8.0	_	80	μΑ	$V_{IN} = V_{CC}$ or ground

^{*}Maximum test duration 2.0 ms, one output loaded at a time.



AC Characteristics

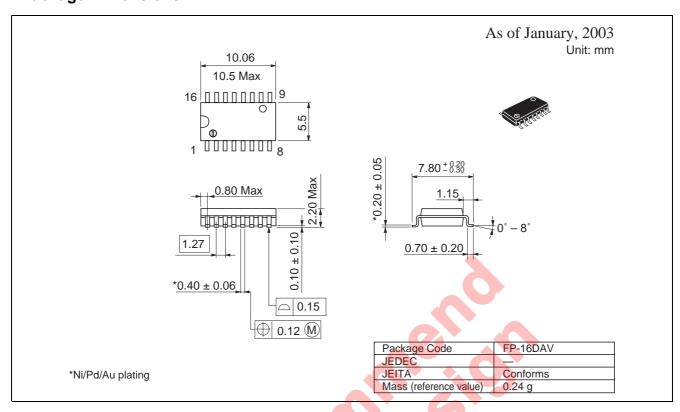
			Ta = +25°C			Ta = -40°	C to +85°C	
			$C_L = 50 pF$			C _L =	50 pF	
Item	Symbol	V _{cc} (V)*1	Min	Тур	Max	Min	Max	Unit
Propagation delay	t _{PLH}	3.3	1.0	8.0	10.5	1.0	11.5	ns
P _n to P		5.0	1.0	5.5	8.0	1.0	9.0	
Propagation delay	t _{PHL}	3.3	1.0	8.0	10.5	1.0	11.5	ns
P _n to P		5.0	1.0	5.5	8.0	1.0	9.0	
Propagation delay	t _{PLH}	3.3	1.0	9.5	12.0	1.0	13.0	ns
C_n to $C_{n+x, y, z}$		5.0	1.0	7.5	10.0	1.0	11.0	
Propagation delay	t _{PHL}	3.3	1.0	9.0	12.0	1.0	13.0	ns
C_n to $C_{n+x, y, z}$		5.0	1.0	7.0	10.0	1.0	11.0	
Propagation delay	t _{PLH}	3.3	1.0	10.5	13.0	1.0	14.0	ns
P_n or G_n to $C_{n+x, y, z}$		5.0	1.0	8.0	10.5	1.0	11.5	
Propagation delay	t _{PHL}	3.3	1.0	11.5	14.0	1.0	15.5	ns
P_n or G_n to $C_{n+x, y, z}$		5.0	1.0	9.0	11.5	1.0	12.5	

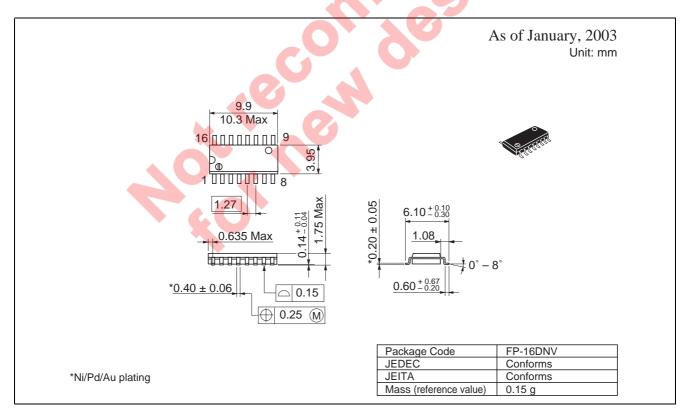
Note: 1. Voltage Range 3.3 is 3.3 V \pm 0.3 V Voltage Range 5.0 is 5.0 V \pm 0.5 V

Capacitance

Item	Symbol	Тур	Unit		Condition
Input capacitance	C _{IN}	4.5	pF	$V_{CC} = 5.5 \text{ V}$	
Power dissipation capacitance	C_{PD}	50.0	pF	$V_{CC} = 5.0 \text{ V}$	
			96,		

Package Dimensions





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