M65881AFP

Digital Amplifier Processor of S-Master* Technology

REJ03F0004-0100Z
Rev.1.00
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DESCRIPTION

The M65881AFP is a S-Master technique processor for digital amplifier enable to convert from multi liner-PCM digital input signal to high precise switching-pulse digital output without analog processing.
The M65881AFP has built-in 24bit sampling rate converter and digital-gain-controller.
The M65881AFP enables to realize high precise (X`tal oscillation accuracy.) full digital amplifier systems combining with power driver IC.

FEATURES

•Built-in 24bit Sampling Rate Converter.
  Input Signal Sampling Rate from 32KHz to 192KHz (24bit Maximum).
  4 kinds of Digital Input Format.
•Built-in L/R Independent Digital Gain Control.
•Built-in Soft Mute Function with Exponential Approximate-Curve.
•Correspondence to Output for Headphone.

OUTLINE : 42P2R
0.8mm pitch 42pin SSOP

MAIN SPECIFICATION

•Master Clock
  Primary Clock: 256Fsi/512Fsi Secondary Clock: 1024Fso/512Fso
•Input Signal Format:
  MSB First Right Justified(16/20/24bit),MSB First Left Justified(24bit)
  LSB First Right Justified(24bit),I²S(24bit)
•Input Signal Sampling Rate from 32kHz to 192kHz.
•Gain Control Function:
  +30dB~-∞dB (0.1dB Step until -96dB, -138dB Minimum)
•Third Order ΔΣ (16Fso:6bit/5bit,32Fso:5bit)

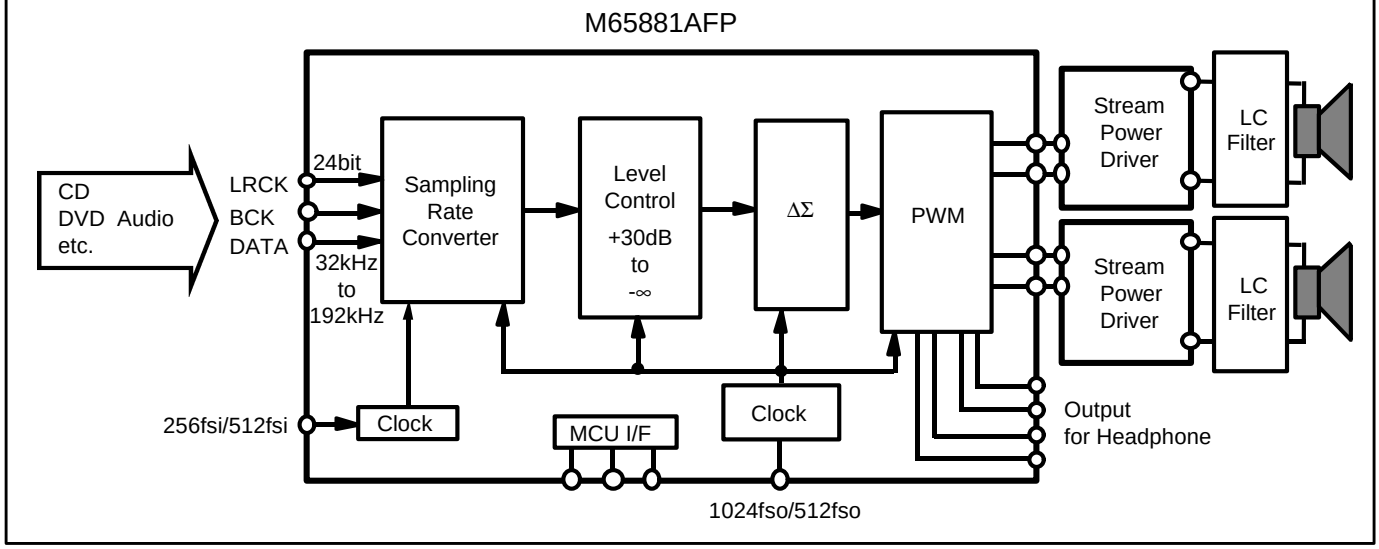
APPLICATION

DVD Receiver, AV Amplifier

RECOMMENDED OPERATING CONDITIONS

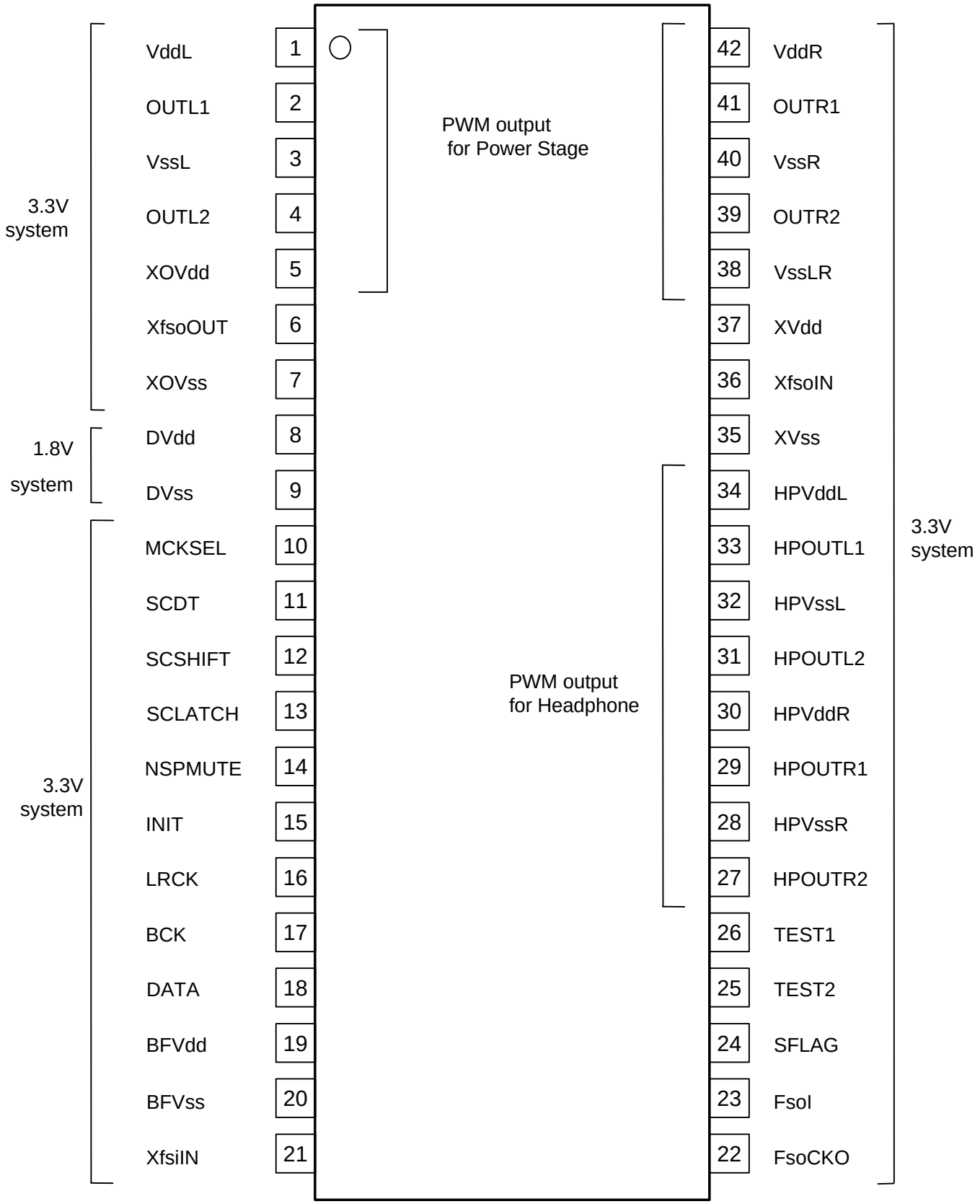
Logic Block:1.8V±10%,PWM Buffer Block :3.3V±10%

SYSTEM BLOCK DIAGRAM)

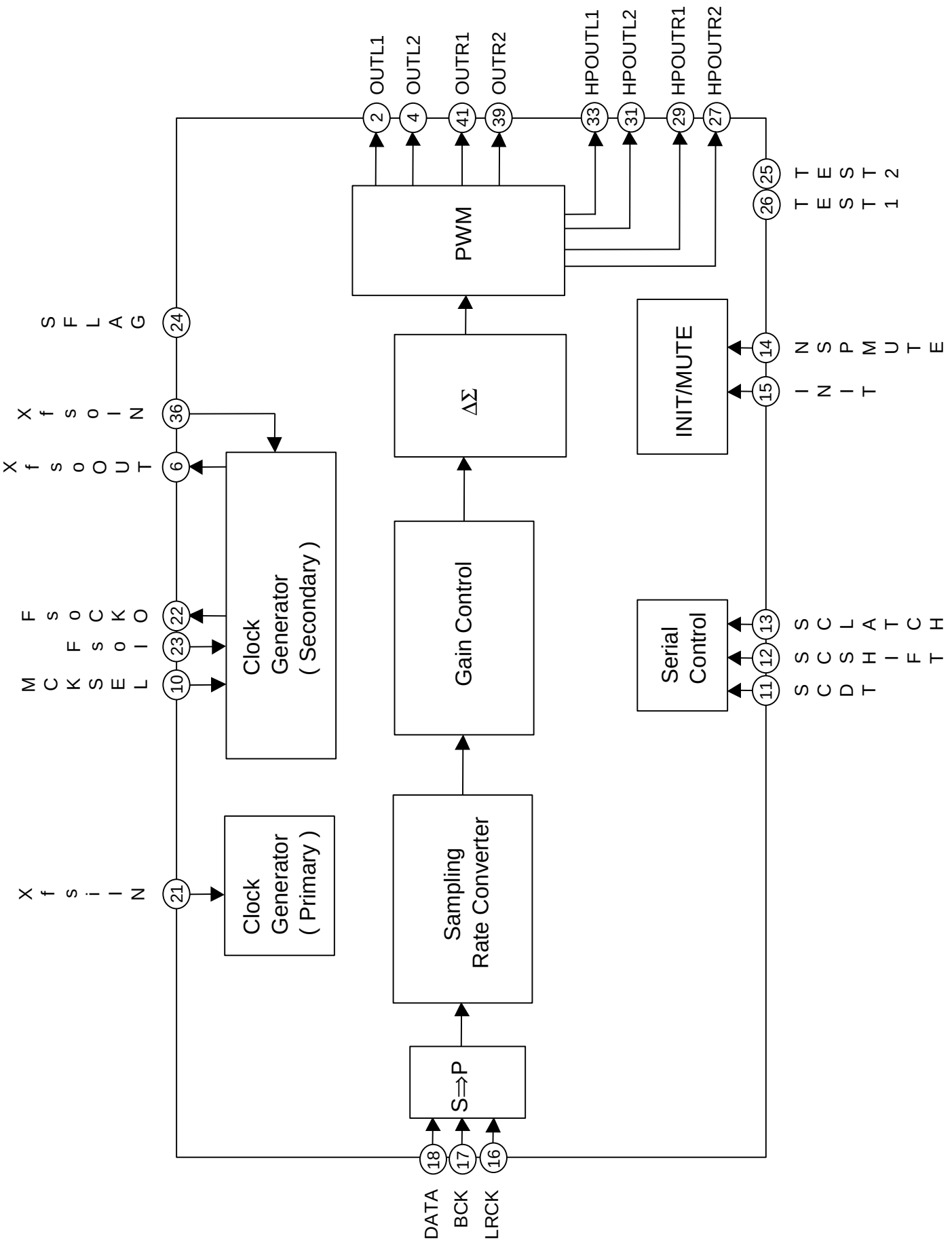


* "S-Master" is the digital amplifier technology developed by Sony Corporation. "S-Master" is a trademark of Sony Corporation.

PIN CONFIGURATION



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Min.	Typ.	Max	Unit
Supply Voltage	PWMVdd	3.3V system (XVdd, XOVdd, PWM Output for Power Stage & Headphone)	-0.3	–	3.8	V
	BFVdd	3.3V system	-0.3	–	3.8	V
	DVdd	1.8V system	-0.3	–	2.5	V
Input Voltage Range	Vi		-0.3	–	Vdd+0.3	V
Power Dissipation	Pd	Ta=75ºC		350		mW
Storage Temperature	Tstg		-40	–	125	ºC

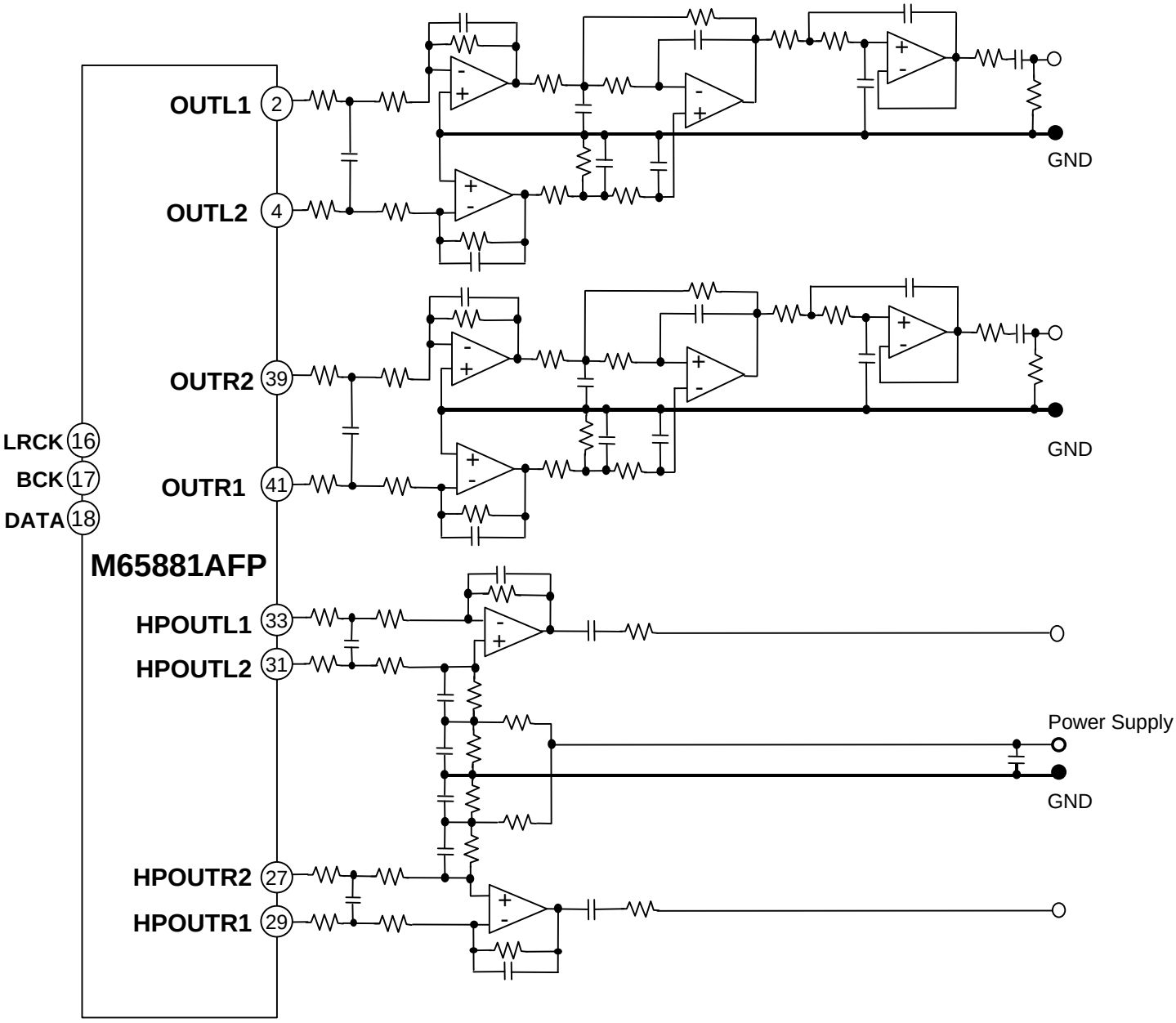
RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Condition	Min.	Typ.	Max	Unit
Supply Voltage	PWMVdd	3.3V system (XVdd, XOVdd, PWM Output for Power Stage & Headphone)	3.0	3.3	3.6	V
	BFVdd	3.3V system	3.0	3.3	3.6	V
	DVdd	1.8V system	1.6	1.8	2.0	V
Operating Temperature	Ta		-20	–	75	ºC
Operating Frequency	XfsoIN		16	–	52.5	MHz
	XfsiIN		8	–	25	MHz

ELECTRICAL CHARACTERISTICS (Ta=25ºC,PWMVdd=3.3V, DVdd=1.8V : Unless otherwise specified.)

Parameter		Symbol	Conditions	Min.	Typ.	M	Unit
"H" Level Input Voltage		VIH3	BFVdd=3.0 to 3.6V	0.75Vdd	–	–	V
"L" Level Input Voltage		VIH3	BFVdd=3.0 to 3.6V	–	–	0.25Vdd	V
Input Leek Current		Ileak		–	–	10	µA
"H" Level Output Voltage	XfsoOUT SFLAG FsoCKO OUTL1,2 OUTR1,2 HPOUTL1,2 HPOUTR1,2	VOH3	BFVdd=3.0 to 3.6V IOH3=-4.0mA (SFLAG,FsoCKO) IOH3=-2.0mA (XfsoOUT,OUTL1,2,OUTR1,2) IOH3=-1.0mA (HPOUTL1,2,HPOUTR1,2)	Vdd-0.5	–	–	V
"L" Level Output Voltage	XfsoOUT SFLAG FsoCKO OUTL1,2 OUTR1,2 HPOUTL1,2 HPOUTR1,2	VOL3	BFVdd=3.0 to 3.6V IOL3=4.0mA (SFLAG, FsoCKO) IOL3=2.0mA (XfsoOUT,OUTL1,2,OUTR1,2) IOL3=1.0mA (HPOUTL1,2,HPOUTR1,2)	–	–	0.5	V
Power Supply Current		Idd2	1.8V system (DVdd)	–	3.5	–	mA
		Idd3	3.3V system (PWMVdd, BFVdd) OUTxx, HPOUTxx="OPEN"	–	2.5	–	mA

CHARACTERISTICS EVALUATION CIRCUIT



Reference characteristic			Conditions
Output for Power Stage	S/N	102dB(typ)	• Input :1kHz 0dB Full scale sine wave • FS :Primary clock 44.1kHz, Secondary clock 48kHz • PWM Output format 1 • AC dithering E • DC dithering : 0.1% • Gain data setting : (Index) 10000b/ (Mantissa) 10000000b • THD+N: Filter 20kHz LPF S/N: Filter 22kHz LPF + JIS-A
	THD+N	0.002%(typ)	
Output for Headphone	S/N	100dB(typ)	
	THD+N	0.006%(typ)	

PIN DESCRIPTION

Pin No.	Name	I/O	Description	Output Current on 3.3V	Signal Level
1	VddL		Power Supply for Lch PWM Power Stage (3.3V)	–	–
2	OUTL1	O	Lch PWM1 Output for Power Stage		3.3V
3	VssL		GND for Lch PWM Power Stage	–	–
4	OUTL2	O	Lch PWM2 Output for Power Stage		3.3V
5	XOVdd		Power Supply for Secondary Master Clock Buffer (3.3V)	–	–
6	XfsoOUT	O	Buffered Output of Secondary Master Clock (1024/512fso)	2mA	3.3V
7	XOVss		GND for Secondary Master Clock Buffer	–	–
8	DVdd		Power Supply for Digital Block (1.8V)	–	–
9	DVss		GND for Digital Block	–	–
10	MCKSEL	I	Secondary Master Clock Selector "L":1024fso, "H":512fso	–	3.3V
11	SCDT	I	Serial Control • Data Input	–	3.3V
12	SCSHIFT	I	Serial Control • Shift Clock Input	–	3.3V
13	SCLATCH	I	Serial Control • Latch Signal Input	–	3.3V
14	NSPMUTE	I	PWM Duty 50% Mute ("L": Active)	–	3.3V
15	INIT	I	Initialize Input (Power Supply Reset) ; "L" : Reset, "H" : Release	–	3.3V
16	LRCK	I	LRCK Input (PCM Signal)	–	3.3V
17	BCK	I	BCK Input (PCM Signal)	–	3.3V
18	DATA	I	DATA Input (PCM Signal)	–	3.3V
19	BFVdd		Power Supply for Input/Output 3.3V Buffer	–	–
20	BFVss		GND for Input/Output 3.3V Buffer	–	–
21	XfsiIN	I	Primary Master Clock Input (256fsi/512fsi)	–	3.3V
22	FsoCKO	O	Secondary Fso Clock Output	4mA	3.3V
23	FsoI	I	Secondary Fso Clock Input	–	3.3V
24	SFLAG	O	Asynchronous Flag (H: Active)	4mA	3.3V
25	TEST2	I	Test2 must be connected to GND	–	3.3V
26	TEST1	I	Test1 must be connected to GND	–	3.3V
27	HPOUTR2	O	Rch PWM2 Output for Headphone		3.3V
28	HPVssR		GND for Rch Headphone	–	–
29	HPOUTR1	O	Rch PWM1 Output for Headphone		3.3V
30	HPVddR		Power Supply for Rch Headphone (3.3V)	–	–
31	HPOUTL2	O	Lch PWM2 Output for Headphone		3.3V
32	HPVssL		GND for Lch Headphone	–	–
33	HPOUTL1	O	Lch PWM1 Output for Headphone		3.3V
34	HPVddL		Power Supply for Lch Headphone (3.3V)	–	–
35	XVss		GND for Secondary Master Clock Input Buffer	–	–
36	XfsoIN	I	Secondary Master Clock Input (1024fso/512fso)	–	3.3V
37	XVdd		Power Supply for Secondary Master Clock Buffer (3.3V)	–	–
38	VssLR		GND for PWM Power Stage	–	–
39	OUTR2	O	Rch PWM 2 Output for Power Stage		3.3V
40	VssR		GND for Rch PWM Power Stage	–	–
41	OUTR1	O	Rch PWM 1 Output for Power Stage		3.3V
42	VddR		Power Supply for Rch PWM Power Stage (3.3V)	–	–

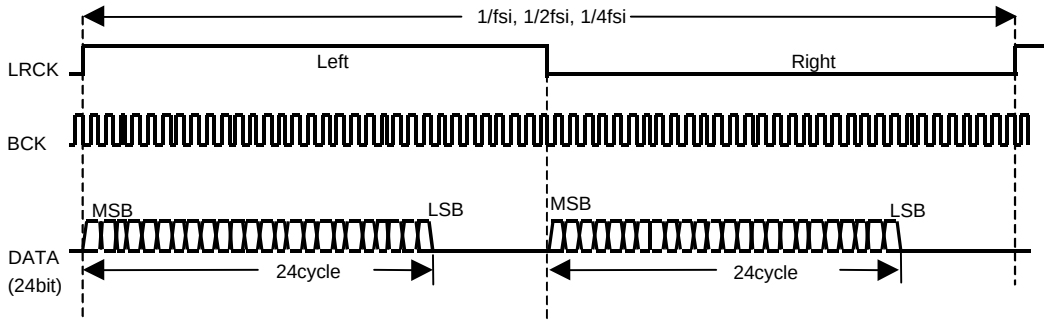
EXPLANATION OF OPERATION

1. DATA,BCK,LRCK

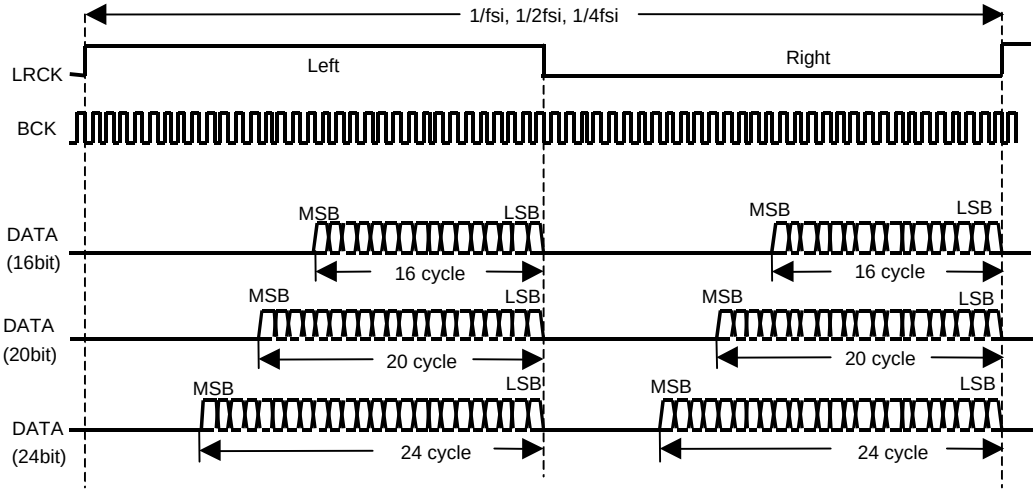
DATA,BCK, and LRCK are input pins for Digital Audio Signal of CD, MD, DVD etc..
Input formats are supported by 4 ways, and are set by Serial Control, "System1 Mode, bit3 and bit4".
Input data length are selectable in a case of "MSB First Right Justified"
(Serial Control "System1 Mode,bit5 and bit6").

•Input formats are shown in following figures.

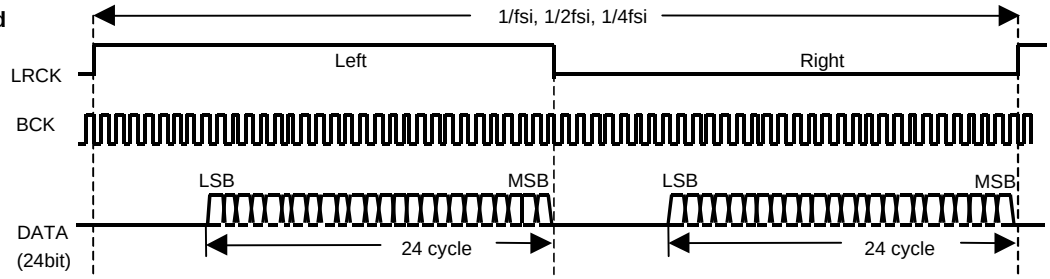
MSB first left justified (24bit)



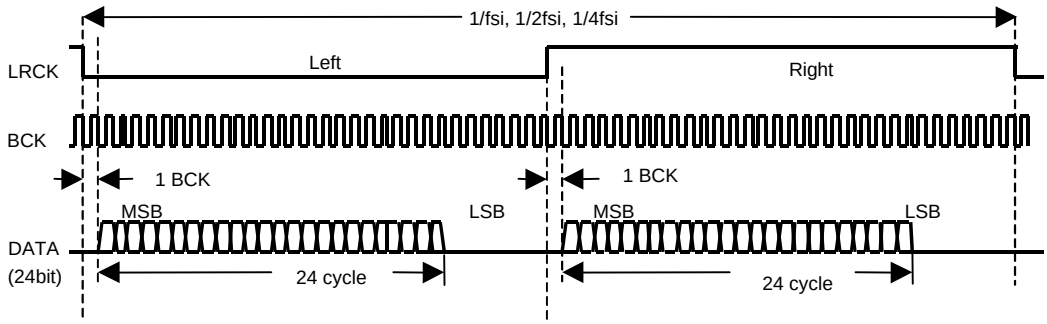
MSB first right justified (16bit, 20bit, 24bit)



LSB first right justified (24bit)



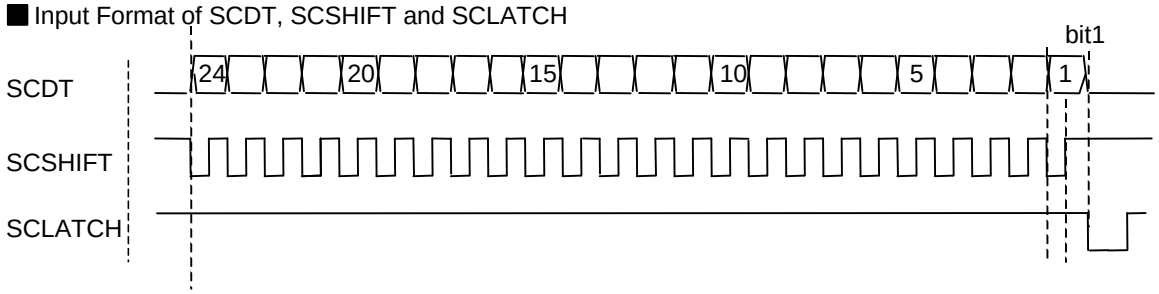
I²S(24bit)



2. SCDT, SCSHIFT, SCLATCH

SCDT, SCSHIFT and SCLATCH are input pins for setting M65881AFP's operation.
Input format of SCDT, SCSHIFT and SCLATCH is shown below.

■ Input Format of SCDT, SCSHIFT and SCLATCH



• Mode Setting

The operating mode are classified in four and assigned by bit1 and bit2. These four functions are shown below.

(bit1 and bit2)= ("L" and "L") Gain control mode: Gain control.
(bit1 and bit2) = ("L "and "H") System1 Mode: Primary block initialization, etc.
(bit1 and bit2)= (H and "L") System2 Mode : Secondary block initialization, etc.
(bit1 and bit2) = ("H" and "H") Test mode (setting prohibition)

Refer to Page13 about these four setting in detail.

3. MCKSEL, XfsoIN, XfsoOUT

XfsoIN pin is secondary master clock input.
The setting of MCKSEL pin selects secondary master clock.
XfsoOUT pin is buffered-output from XfsoIN pin's input clock.

MCKSEL	XfsoIN
"L"	1024fso
"H"	512fso

4. XfsiIN

XfsiIN pin is primary master clock input.
The frequency of primary master clock must be selected by serial control "System2 mode :bit3 (IMCKSEL)"

bit3 (IMCKSEL)	XfsiIN
"H"	512fsi
"L"	256fsi

■ The relations between input signal sampling rate and master clock frequency.

Input sampling rate	Primary clock 512fsi/256fsi[Hz]	Secondary clock 1024fso/512fso[Hz]
1fsi : 32k / 2fsi : 64k / 4fsi : 128k	16.384M/8.192M	32.768M/16.384M
1fsi : 44.1k / 2fsi : 88.2k / 4fsi : 176.4k	22.579M/11.290M	| / |
1fsi :48k / 2fsi : 96k / 4fsi : 192k	24.576M/12.288M	49.152M/24.576M

Input signal and primary clock are related to synchronization. The primary clock frequency are 512 or 256 times as much as the input signal fsi (32k, 44.1k and 48k.)
The primary and secondary clock are related to independence. (asynchronization)
At 1024fso setting, secondary clock= frequency range from 32.768MHz to 49.152MHz.
At 512fso setting, secondary clock = frequency range from 16.384MHz to 24.576MHz.

***Primary clock**

This clock means input side clock system of sampling rate converter.

***Secondary clock**

This clock means output side clock system of sampling rate converter.
This clock makes to operate after sampling rate converter block.
(Gain Control Block and PWM Block, etc.)

*"fsi" and "fso" are defined as following stated in this specification.

fsi : Primary sampling frequency
fso : Secondary sampling frequency

5. FsoCKO

FsoCKO is clock output pin of 1fso frequency. The output is divided-clock of XfsoIN, and frequency is free-running at power on. FsoCKO pin's clock is utilized for a synchronization in case that have used plural M65881AFP, take a synchronization between M65881AFP and other external devices.
Refer to the following Chapter 6. in detail.

6. FsoI, SFLAG

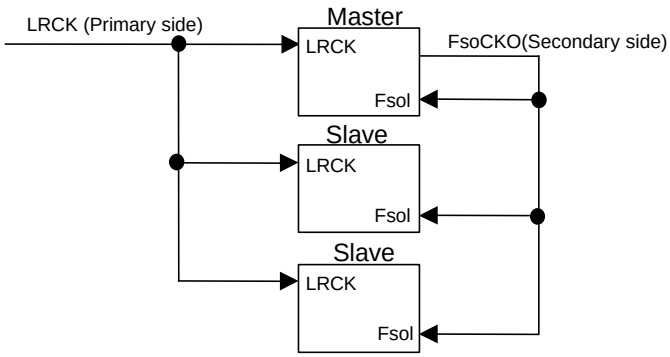
M65881AFP synchronizes in clock input from the external source devices. So it makes synchronized operation between source devices or another M65881AFP (in case of Multi channel Operation).
The primary side operation (input side of sampling rate converter) are synchronized in LRCK, and the secondary side operation (output side of sampling rate converter) are synchronized in FsoI.
M65881AFP detects rise edge of these synchronized clock in normal operation, and the M65881AFP does operation of resynchronization in case that the cycle has changed.
In addition, the M65881AFP re-synchronizes for a synchronized clock, in case that M65881AFP detects SYNC flag (Serial Control, System2 Mode,bit6) rise edge, too.
While re-synchronizing, SFLAG pin outputs "H" and data is muted inside.
In case of using Multiplex (for multi channel application) and Single (for 2ch application), detail explanation is shown below.

■ Multiplex use

Primary side: Synchronize with LRCK. All ICs synchronize with an source device by connecting common LRCK.

Secondary side: Synchronize with FsoCKO of Master IC. One of M65881AFP becomes a master IC, and the synchronization between ICs is carried out by FsoCKO of Master IC. FsoCKO pin outputted from this master IC is entered each FsoI pins of master and slave ICs.

ASYNCEN2=enable



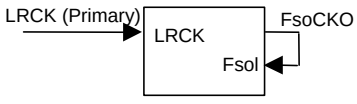
Multiplex use (6ch)

■ Single use

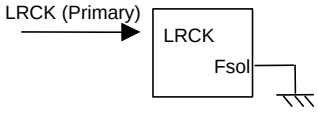
Primary side: Synchronize with LRCK. Therefore M65881AFP synchronizes with source devices.

Secondary side: There is no need for external devices and other ICs to synchronize, therefore FsoCKO is connected to FsoI, In other way, By setting secondary side asynchronous detection to “disable” with “ASYNCEN2” flag (Serial Control, System2 mode,bit8), FsoI can also be considered as fixation.

ASYNCEN2=enable



ASYNCEN2=disable



7. OUTL1, OUTL2, OUTR1, OUTR2

OUTL1, OUTL2, OUTR1 and OUTR2 are pulse output modulated ΔΣ output to PWM signal.
These pins are connected to external Power Driver ICs.The PWM output can be selected PWM Output Format 1, 2, 3 and 4 by serial control data(System1 mode, bit22,23).

PWM Output Form1 : General Modulation
PWM Output Form2 : Symmetrical Modulation
PWM Output Form3 : Modulation returned with time domain.
(The rise and fall edge of Lch and Rch in a term are reverse.)
PWM Output Form4: Modulation returned with time domain.
(The rise and fall edge of Lch and Rch in a term are same timing.)

- In each 4 forms, the rate and bit length of PWM Output can be changed. Moreover, an output mute function and an output pins reverse function can be controlled by the pin setting or serial control. Refer to pin setting of the following page about a phase of the PWM output for Power Stage and Headphone. The PWM output control is shown in the following table.

■ PWM output control

Item	Operation	Setting Operation
Output Form (Common setting for Power Stage and Headphone)	Output Form Selection 1,2,3,4	Set up by the serial control system 1 mode bit 22,23 (PWM MODE 0 and 1). (Refer to system 1 mode(Page16) for details)
Operating Rate and Data Bit Length (Common setting for Power Stage and Headphone)	Select to 16fso/6bit ,16fso/5bit ,32fso/5bit from operating rate and data bit length of ΔΣ. PWM operation are synchronized by this setting.	Set up by the serial control system 2 mode bit16 and bit17. (Refer to system 2 mode(Page 18) for details.)
Output Muting (Common setting for Power Stage and Headphone)	Duty 50% Mute (Selectable common and independent setting for Lch/ Rch.)	< Common setting for Lch / Rch > Set NSPMUTE pin "L" or set up by serial control " System 2 mode bit14 (NSPMUTE) "H". < Independent Setting for Lch / Rch > Set up by serial control Gain Control Mode bit9,10 (NSPMUTEL,NSPMUTER) "H" . (Refer to Page 11,18 and 13 for details)
	Absolute Zero Mute	Set up by serial control system2 mode bit15(PGMUTE) "H". (See system2 mode(Page 18))
Reverse Output Pins Function	Reverse on Lch and Rch of output pins (Common setting for Power Stage and Headphone)	Set up by serial control system2 mode bit9 (CHSEL).
	Reverse for R1 and R2 of output pins. (Only enable for Power Stage.)	Set up by serial control system2 mode bit12 (CHRSEL).

8. HPOUTL1, HPOUTL2, HPOUTR1, HPOUTR2

HPOUTL1, HPOUTL2, HPOUTR1 and HPOUTR2 are output pins for Headphone output.
PWM output modulated ΔΣ output data to pulse width.

■ The Phase of PWM Output for Power Stage and PWM Output for Headphone.

The output for Headphone is reverse phase as output for Power.
Moreover, it is possible to set L1 and R1 output same phase by serial control the system 1 mode, bit24= "H"(PWMHP).

In addition, NSPMUTE, PGMUTE and CHSEL are set in common PWM for Power and PWM for Headphone, and as for CHRSEL flag is set as a function of only PWM for Power.
(Refer to previous page "Table of PWM control" for details).

9. NSPMUTE

NSPMUTE pin sets to PWM Output to Duty 50% Mute.
L: PWM Output 50% Mute
H: Mute release

10. INIT

INIT is the pin for reset to all functions of M65881AFP.
"L" level: (1) Clear of data memory, (2) Initialization of a serial control setting
(3) PWM Output Duty 50% Mute
(" L" period needs more than 5msec.)
"H" level : Usual operation.
*The rise edge from "L" to "H": Re-synchronization are operated, which is same at serial control SYNC function. (system2 mode bit6)

11. TEST1, TEST2

TEST1 and TEST2 pins are test input for factory shipping test of M65881AFP.
TEST1 and TEST2 pins must be tied to "L" level on usual operation.

12. Power supply and GND

Power supply and GND routes have a following 6 isolated lines.

(1) VddL, VssL,VddR, VssR, VssLR
VddL, VssL,VddR, VssR and VssLR pins are Power supply and GND for PWM Output buffer.
Lch and Rch have a independent power supply and GND. Power supply must be fixed at 3.3V.

(2) HPVddL, HPVssL, HPVddR, HPVssR
HPVddL, HPVssL, HPVddR and HPVssR pins are Power supply and GND of PWM Output buffer for Headphone. Lch and Rch have a independent power supply and GND.
Power supply must be fixed at 3.3V.

(3) XVdd, XVss
XVdd and XVss are Power supply and GND for XfsoIN clock input block.
Power supply voltage must be fixed at 3.3V.

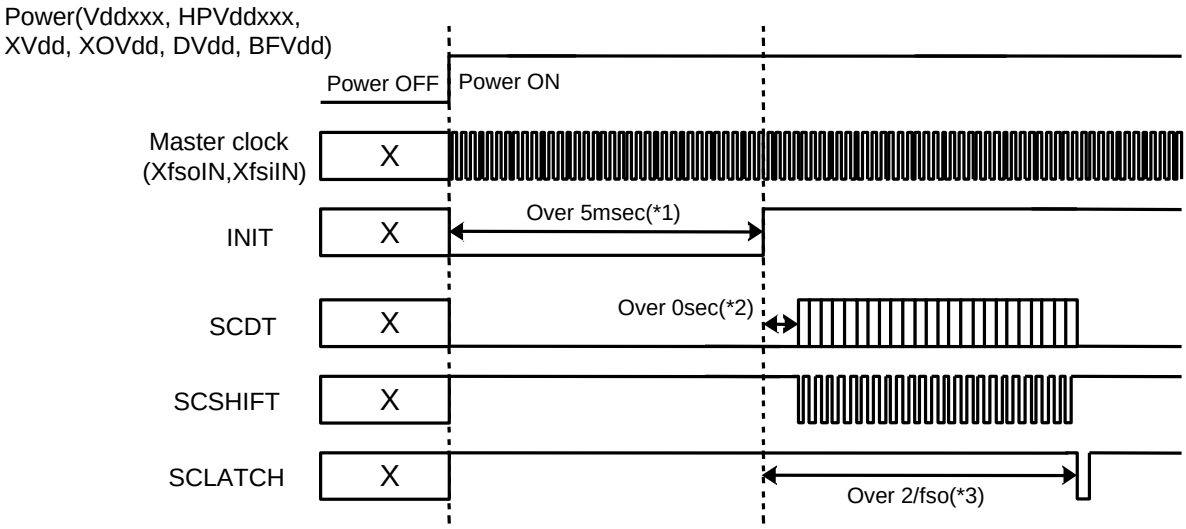
(4) XOVdd, XOVss
XOVdd and XOVss are Power supply and GND for XfsoOUT Clock Output.
Power supply voltage must be fixed at 3.3V

(5) DVdd, DVss
DVdd, DVss are Power supply and GND for internal digital block.
Power supply voltage must be fixed at 1.8V.

(6) BFVdd, BFVss
BFVdd and BFVss are Power and GND for input/output buffer (except for PWM block and clock buffer). Power supply voltage must be fixed at 3.3V.

13. Power sequences

System power-on sequencing * Refer to following figure.



*1 After a power supply and Master clock become to stable, INIT pin must be "L" over 5msec.
*2 Data transfer is possible right after INIT release.
*3 Until SCLATCH is operated, a period over 2/fso (fso=48kHz, over 42µsec) is necessary after INIT release.

SERIAL CONTROL

1. Gain Control Mode

No setting bits means " Don't care".

bit	Flag name	Functional Explanation	H	L	INIT
1	MODE1	Mode setting1		"L" fixed	–
2	MODE2	Mode setting2		"L" fixed	–
3	TEST1	Test Mode 1		"L" fixed	L
4	TEST2	Test Mode 2		"L" fixed	L
5	NSLMT1	Output Limit 1	Refer to Table 1-1.		L
6	NSLMT2	Output Limit 2			L
7	GCONT1	Channel selection for Gain Control Block 1	L/R Independence	L/R Common	L
8	GCONT2	Channel selection for Gain Control Block 2	Lch	Rch	L
9	NSPMUTEL	Lch Duty 50% Mute for PWM Output	active	non-active	L
10	NSPMUTER	Rch Duty 50% Mute for PWM Output	active	non-active	L
11					–
12	GAIN0	Gain Data Index (MSB)			H
13	GAIN1	Gain Data Index			L
14	GAIN2	Gain Data Index			L
15	GAIN3	Gain Data Index			L
16	GAIN4	Gain Data Index (LSB)			L
17	GAIN5	Gain Data Mantissa (MSB)			H
18	GAIN6	Gain Data Mantissa			L
19	GAIN7	Gain Data Mantissa			L
20	GAIN8	Gain Data Mantissa			L
21	GAIN9	Gain Data Mantissa			L
22	GAIN10	Gain Data Mantissa			L
23	GAIN11	Gain Data Mantissa			L
24	GAIN12	Gain Data Mantissa (LSB)			L

•Output Limit (bit5,6: NSLMT1,2)

The M65881AFP has Over Flow Limit function which detects by input signal level and limit gain control.
The limit Value is set by Gain control Mode (bit5,6 "NSLMT1, 2") and System2 Mode(bit17 "NSOBIT").

•Limit value setting of output for gain control and ΔΣ (bit5, 6 : NSLMT1, 2)

Table 1-1a Limit Value [In case of 6bit mode, system2 mode bit 17(NSOBIT)="L".]

NSLMT1,2	Output Limit Value of gain	PWM Output (Limit Value from ΔΣ Block)
(L, L)	±0.9375	63 values (±31)
(H, L)	±0.90625	61 values (±30)
(L, H)	±0.875	59 values (±29)
(H, H)	±0.84375	57 values (±28)

Table 1-1b Limit Value [In case of 5bit mode, system2 mode bit 17(NSOBIT)="H".]

NSLMT1,2	Output Limit Value of gain	PWM Output (Limit Value from ΔΣ Block)
(L, L)	±0.90625	31 value (±15)
(H, L)	±0.875	31 value (±15)
(L, H)	±0.84375	29 value (±14)
(H, H)	±0.8125	29 value (±14)

•Channel selection for Gain Control Block (bit7,bit8: GCONT1, GCONT2)

These bit selection enable to control gain data "L/R common" or "L/R independence".
GCONT1:"L"… L/R common "H"...L/Rch independence.
GCONT2:"L"… Rch only "H"…Lch only
Bit8 is enable only the case of " Bit7="H".

•PWM Duty 50% Mute (bit9,10:NSPMUTEL,R)

*Enable both output for Power and Headphone.

These bit set "Duty 50% fixed Mute" with Lch/Rch independence.
NSPMUTEL : "L"….Mute release, "H"…Lch Mute
NSPMUTER : "L"….Mute release, "H"…Rch Mute

* Duty 50 % Mute Operation are operated by one of the following setting.
  - Gain control bit9,10 (NSPMUTEL,R)
  - NSPMUTE pin
  - Serial control system2 mode ,bit 14 (NSPMUTE)

The index and Mantissa part of Gain Data (bit12-bit24 :GAIN0-GAIN12)

The gain value is set from bit12-bit24.
Index part: bit12(MSB) to bit16(LSB)
Mantissa part: bit17(MSB) to bit24(LSB)
The gain data is assigned 13bits, composed of Index part 5bits and of Mantissa part 8bits.

The range of Index parts is following statements.
Index part: 10100b(16.0) to 10000b(1.0) to 00000b(2^{-16})

The range of Mantissa parts is following statements.
Mantissa part:Index part; 10100b to 00001b: Mantissa part; 11111111b to 10000000b (128 step/ Index).
Index part; 00000b: Mantissa part; 11111111b to 00000000b (256 step).

Initial value: Index part: 10000b Mantissa part: 10000000b

Infinity zero: Index part: 00000b Mantissa part: 00000000b

Notice of GAIN value setting continuously
In case of Gain value setting continuously, for example of setting L/Rch independently, please take the interval time (pulse interval time of SCLATCH signal) more than 1/fso. For example, in the case of fso=48kHz, please take the interval time more than 21µsec.

• The Gain Data and Audio Output Level.

Gain data consists of 13bits (Index part: 5bit, Mantissa part: 8bit).
e.g. 10000b(1.0)/10000000b(0.5) means 0.5(0dB).

Table 1-2 Gain data and output level

Gain Data	Polarity	Output absolute maximum value	Output Level
10100/11111111 (b) ～ 10001/10000000 (b) ～ 10000/10000000 (b)	+	15.9375 ～ 1.0 ～ 0.5	+30.069dB ～ +6.021dB ～ 0dB
01111/11111111 (b) ～ 00000/10000000 (b) ～ 00000/00000001 (b) 00000/00000000 (b)		0.498046875 ～ $0.5 * 2^{-16}$ ～ $0.00390625 * 2^{-16}$ infinity zero	-0.0340dB ～ -96.330dB ～ -138.474dB

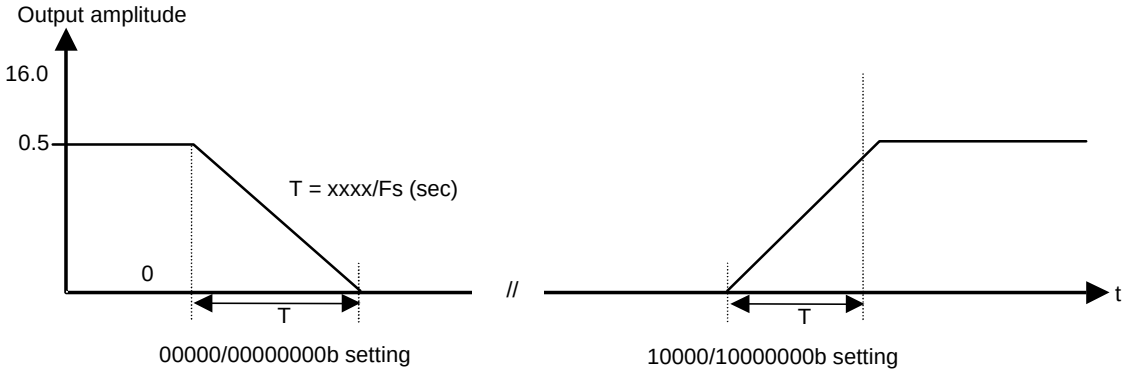
• Calculation method of Gain Value

The way to calculation of Gain value from Gain Data is following equation.

$$\text{Gain value} = 20\log\left[\, 2^{\langle\text{Index data (decimal value)}-16\rangle} \times \frac{\text{Mantissa Data (decimal value)}}{128} \,\right] \text{dB}$$

• Soft Mute

The Soft Mute function is executed by setting of Gain Data as 00000/00000000b
(" / " means dividing point between index part and mantissa part).
The release from Soft Mute Function must be executed by setting the gain data before soft mute.
The Soft mute Function and release from there don't have linear curve but
have characteristics of approximate exponential curve.



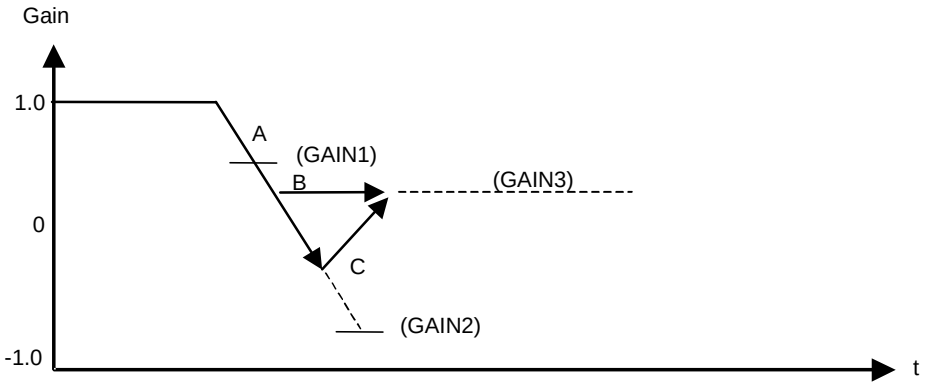
Characteristics of Soft Mute function

• Operating time of Soft Mute

Total steps from Maximum value(10100b/11111111b) to Minimum value(00000b/00000000b)
(128steps/1 index) × (20index (10100b-10000b)) +256steps = 2816steps.
The transition term of up and down depend on 2fso clock.
Therefore, in case of fso=48kHz, T=1/2fso=10.416µsec/step, transition term are following.
From Maximum value (10100b/11111111b) to Minimum value (00000b/00000000b) : 2816T=29.333msec.
From 0dB value (10000b/10000000b) to Minimum value (00000b/0000000b) : 2304T=24msec
6dB transition term (when over 00000b/10000000b (=-96dB) value) : 128T=1.333msec.

• Soft Attenuate

Transition from older Gain Attenuation to newer Gain Attenuation always operates with Soft Mute function.
For example, in case of Gain1 > Gain3 > Gain2, transition process is shown below.
At first, GAIN1 is operated, then second, GAIN2 is operated.
In case that GAIN2 is operated faster than GAIN1 of transition completion (refer to "A" situation in figure)
GAIN1 is ignored and data approaches at GAIN2.
Further, GAIN3 is operated faster than GAIN2 of transition completion(Refer to "B" or "C" situation in figure),
GAIN2 is ignored and data approaches at GAIN3 .



Soft Attenuate

2. System1 Mode

No setting bits means "Don't care".

bit	Flag name	Function Explanation	H	L	INIT
1	MODE1	Mode Setting 1		"L" fixed	–
2	MODE2	Mode Setting 2	"H" fixed		–
3	IFMT0	Input Format Selection	Refer to the Table2-1 below		L
4	IFMT1				L
5	IBIT0	Setting for Input Word Length	Refer to the Table2-2 below		L
6	IBIT1				L
7	ISF0	Input sampling rate selection	Refer to the Table2-3 below		L
8	ISF1				L
9	EMPFS1	Fsi selection for De-emphasis Filter	Refer to the Table2-4 below		L
10	EMPFS2				L
11	DF1IMUTE	Zero Mute at DATA input	active	non-active	L
12	DF2IMUTE	Zero Mute at sampling rate converter input	active	non-active	L
13					–
14					–
15					–
16					–
17					–
18					–
19					–
20	ASYNC1MODE	Asynchronous Detection Flag for Primary Side	Zero Mute	PWM:duty50%	L
21					–
22	PWMMODE0	Selection for PWM Output type	Refer to the Table2-5 below		L
23	PWMMODE1				L
24	PWMHP	Phase of HPOUTL1/R1 based on PWM output for power	Same Phase	Reverse Phase	L

Table 2-1 Selection of input format

bit	Flag Name	MSB First Left Justified	MSB First Right Justified	LSB First Right Justified	I^2S
3	IFMT0	L	H	L	H
4	IFMT1	L	L	H	H

Table 2-2 Setting for Input Data Word Length

bit	Flag Name	16bit	20bit	24bit	Don't use
5	IBIT0	L	L	H	H
6	IBIT1	L	H	L	H

Table 2-3 Selection of Input Sampling Rate (fsi:32k to 48kHz, 2fsi:64k to 96kHz, and 4fsi:128k to 192kHz)

bit	Flag Name	fsi	2fsi	4fsi	Don`t use
7	ISF0	L	H	L	H
8	ISF1	L	L	H	H

Table 2-4 Fs selection for De-emphasis filter (De-emphasis is "ON" except for bit9=L and bit10=L)

bit	Flag Name	32.0k	44.1k	48.0k	OFF
9	EMPFS1	H	L	H	L
10	EMPFS2	H	H	L	L

Table 2-5 Selection PWM Output

bit	Flag name	PWM Output Form1	PWM Output Form2	PWM Output Form3	PWM Output Form4
22	PWMMODE0	L	H	L	H
23	PWMMODE1	L	L	H	H

•PWM Output Form2 enables to operate following conditions.
MCKSEL=L (Secondary master clock 1024fso)
Serial Control System2 Mode; bit16 (NSOBIT) = "H" (5bit)
bit 17 (NSSPEED)="L" (16fso)
In case of the setting and release for PWM Output Form 2,
Refer to "The NOTE1 at setting PWM output Form 2" on next page.

■ Selection of Input format (bit3,4: IFMT0,1)
Refer to Table 2-1.

■ Input word length (bit5,6: IBIT0,1)
Refer to Table 2-2. This setting is enable the case of MSB First Right justified.

■ Selection of Input Sampling Rate (bit7,8 : ISF0,1)
Refer to Table 2-3

■ Fs Selection for De-emphasis filter (De-emphasis is "ON" except for bit9="L" and bit10="L".
(bit9, bit10) : ("L", "L") …De-emphasis Filter off
except ("L", "L") … De-emphasis Filter on (Setting fsi)

■ Zero Mute at DATA input (bit11: DF1IMUTE)
"L" … Mute release
"H" … Mute
The input data from DATA pin is muted in this setting.

■ Zero Mute at Sampling Rate Converter Input (bit12: DF2IMUTE)
"L" … Mute release
"H" … Mute
DF2IMUTE is muting control of sampling rate converter input data.

■ Selection of Muting operation at primary Side Asynchronous Detection (bit20: ASYNC1MODE)
"L" -- Duty 50% Mute of PWM output at primary side asynchronous detection.
"H"… Input Zero Mute of the gain control at primary side asynchronous detection.
(PWM Output 50% Mute doesn't be operated in this setting.)

■ Selection of PWM output form (bit22, 23:PWMMODE 0 and 1) Refer to Table 2-5.
* Enable to PWM for Power and for Headphone.
• The Selection of PWM output form 1, 2, 3, and 4 Refer to Page10 for the details.

● NOTE1 ; At the setting of PWM Output Form2
PWM Output Form2 enable to operate the following conditions.
bit17(NSOBIT)="H“(5bit), bit16(NSSPEED)="L“(16fso)
Only in terminal MCKSEL="L" (secondary side master clock 1024 fso)

■ In case of setting and release for PWM Output Form2,set both flags as follows.
•Serial Control System Mode1 bit 22,23 (PWMMODE0,1)
Mode2 bit 16 (NSSPEED), bit17 (NSOBIT)

< In case of the setting for PWM output form2 >
(1) Set to Serial Control system2 mode ; bit17(NSOBIT)="H"
bit16(NSSPEED)="L".
(To be set as MCKSEL="L" in advance is required.)
(2) Serial control system1 mode bit22, 23(PWMMODE0,1)="H","L"
(When a setup of both (1) and (2) is completed, it changes to Form2. When (2) is set up before (1),
The term until a setup of (1) holds the last PWM Output Form.)

< In case of release for PWM output form2 >
(1) Serial control System 1 mode bit22, bit 23 (PWMMODE 0 , 1) is set as the Form to be used.
(2) Serial Control System2 mode bit17(NSOBIT),bit16(NSSPEED) is set the condition to be used.
When a setup of (1) is completed, PWM Output Form changes. When (2) is set up before (1),
a term until a setup of (1) is worked keeps the Form 2 in the state of
serial control system 2 mode bit17(NSOBIT) =H, bit16(NSSPEED) =L.

● NOTE2; Selection of PWM output form
Pay attention in selection and setting above-mentioned that a noise may occur by internal clock changes when Setting of MCKSEL pin is changed and the serial control system 2 modes
bit17 (NSOBIT) and bit16 (NSSPEED).
Since especially MCKSEL pin sets up an internal master clock, use with a fixed value recommended.
In changing MCKSEL, initialization with INIT pin and a re-setup of all the bits by serial control are needed after changing MCKCEL.

■ Phase of PWM Output pins for Headphone(bit24:PWMHP) *Enable only for PWM output for Headphone.

"L" -- The Output for Headphone L1 and R1 are reverse phase as the PWM output L1 and R1 for Power Stage.
(In this setting, the outputs for Headphone L1, L2, R1and R2 are reverse phase
as output for Power Stage.)
"H" -- The Output for Headphone L1 and R1 are same phase as the PWM output L1 and R1 for Power Stage.
(In this setting, L2 and R2 Output for Headphone are reverse phase as L2 and R2 Output for Power Stage.)

Refer to Page11.

3. System2 Mode

No setting bits means "Don't care".

bit	Flag name	Functional Explanation	H	L	INIT
1	MODE1	Mode settiing1	"H" fixed		-
2	MODE2	Mode setting2		"L" fixed	-
3	IMCKSEL	Input master clock Selection	512fsi	256fsi	L
4					-
5					-
6	SYNC	Re-synchronization	L ->H : Resynchronization		L
7	XFsoOEN	XfsoOUT pin output "enable".	disable	enable	L
8	ASYNCEN2	Asynchronous Detection Flag for secondary Side	enable	disable	L
9	CHSEL	L/R inversion of PWM output pin	active	non-active	L
10	DRPOL	ΔΣ Block : Rch Input Phase	Negative phase	Positive phase	L
11	SRCRST	Sampling Rate Converter Reset	active	non-active	L
12	CHRSEL	L/R inversion of PWM output pin	active	non-active	L
13	GIMUTE	Zero Mute at Gain Control Input Clock	active	non-active	L
14	NSPMUTE	Duty 50% Mute for PWM Output	active	non-active	L
15	PGMUTE	G_MUTE of PWM Output Data	active	non-active	L
16	NSSPEED	ΔΣ Block : Operating Speed	32fso	16fso	L
17	NSOBIT	ΔΣ Block : Setting of Output bit number	5bit (31value)	6bit (63 value)	L
18	DCDRPOL	ΔΣ Block : Rch Phase of AC dithering	Negative phase	Positive phase	L
19	DCDSEL0	ΔΣ Block : DC dithering selection	Refer to Table 3-1		L
20	DCDSEL1				L
21	ACDRPOL	ΔΣ Block : Rch Phase of AC dithering	Negative phase	Positive phase	L
22	ACDSEL0	ΔΣ Block : AC dithering selection	Refer to Table 3-2		L
23	ACDSEL1				L
24	ACDSEL2				L

Table 3-1 DC dithering selection at ΔΣ block

bit	Flag name	Non dithering	DC dithering 0.1%	DC dithering 0.2%	DC dithering 0.4%
19	DCDSEL0	L	H	L	H
20	DCDSEL1	L	L	H	H

Table 3-2 AC dithering selection at ΔΣ block

bit	Flag name	Non dithering	AC dithering A	AC dithering C	AC dithering E
22	ACDSEL0	don't care	L	L	L
23	ACDSEL1	L	H	L	H
24	ACDSEL2	L	L	H	H

Table 3-3 Setting of ΔΣ block operating

bit	Flag / Pin code name	16fso,6bit	16fso,5bit	16fso, 5bit	32fso, 5bit
16	NSSPEED	L	L	X	H
17	NSOBIT	L	H	X	H
Pin	MCKSEL	L (Secondary master clock 1024fso)	L (Secondary master clock 1024fso)	H (Secondary master clock 512fso)	L (Secondary master clock 1024fso)

The selection of primary master clock (bit3: IMCKSEL)

L … 256fsi
H … 512fsi ("512fsi" are divided into half "256fsi" and operate as primary master clock.)

■ Re-synchronization (bit6: SYNC)

Refer to Page9 in details on re-synchronous operation.
Resynchronization process starts by SYNC rise edge, therefore SYNC level must be fixed to "L" just before SYNC operation.

■ "Enable" of a XfsoOUT output (bit7:XfsoOEN)

"L" ... Clock Output (enable)
"H"… "L" fixed (disable)

■ Flag to " Enable " of Asynchronous Detection for secondary block (bit8: ASYNCEN2)
ASYNCEN2 (bit8) controls " Enable" and " Disable" for secondary asynchronous detector.
"L“ … "disable"
"H" … "enable“
Under condition of ASYNCEN2="L", secondary side asynchronous detection is in-effective under asynchronous position, whether Fsol Clock is not inputted, there by M65881AFP does not operate function for instance mute operation.

■ Reverse Lch/Rch for PWM Output pins (bit9: CHSEL)
* Enable to control for both PWM for Power and Headphone.
"L" … As it is aligned
"H" … Reverse to pin alignment of Lch/Rch

■ ΔΣ Rch Input Phase (bit10: DRPOL)
"L"…. Same phase ("Through")
"H"….This setting makes ΔΣ Rch Input in reverse, further makes PWM block input phase reverse, ultimately phase becomes positive phase (Input pin and Output pin's phase is same).

■ Sampling rate converter block reset (Initialize function) (bit11: SRCRST)
"L" …..normal operation
"H" to "L" edge…..Reset (Initialize function)

■ Reverse for R1 and R2 of Output pins. (bit12:CHRSEL).
“L”… As it is aligned
"H".....Reverse to pin alignment of R1/R2.

■ Zero Mute of a gain control input (bit13:GIMUTE)
"L" …Mute release H… Mute

■ Duty 50% Mute of PWM Output (bit14: NSPMUTE)
Fixed PWM duty 50% Mute
"L"…..Mute release
"H"….. Mute
This function exists also in a pin by the same name.
(This Mute function can be set either NSPMUTE flag or NSPMUTE pin.)
Refer to Page13 about a relation with the gain control mode of serial control bit9 and bit 10 (LR independent control).

■ G-Mute for PWM Output Data (bit15: PGMUTE) *Enable to PWM both PWM for Power and Headphone.
At G-MUTE flag = H , PGMUTE pin fixes each PWM Output as followings.
"L"….. Mute release
"H"….. Fixed Mute for PWM Output (Fixed value as follows)
<PWM Output for Power >
L1,L2,R1 and R2 : "L" fixed
< PWM Output for Headphone, Serial control (system1 mode; bit24) PWMHP="L">
L1,L2,R1 and R2 : "H“ fixed
< PWM Output for Headphone, Serial control (system1 mode; bit24) PWMHP="H">
L1, R1 : "L" fixed
L2, R2 : "H" fixed

■ ΔΣ : operating rate (bit16 : NSSPEED) Refer to the Table 3-3
"L" … 16fso
"H" … 32fso *Enable only MCKSEL="L"(1024fso), NSOBIT="H“
(Except for this condition, Operating rate automatically becomes 16fso).

■ ΔΣ : The setting of bit length (bit17 : NSOBIT) Refer to the Table 3-3.
NSOBIT selects bit length for ΔΣ operation. This is set by force as 5bit at MCKSEL="H".
"L" … 6bit (63 value)
"H" … 5bit (31value)

■ ΔΣ : DC dithering Rch Phase (bit18:DCDRPOL)
"L"…Same phase “H"…Reverse phase

■ ΔΣ : DC dithering selection (bit19, 20 : DCDSEL0,1) Refer to the Table 3-1.

■ ΔΣ :AC dithering Rch Phase (bit21 : ACDRPOL)
"L"…Same phase “H"…Reverse phase

■ ΔΣ : AC dithering selection (bit22, 23, 24 : ACDSEL0, 1, 2) Refer to the Table 3-2.

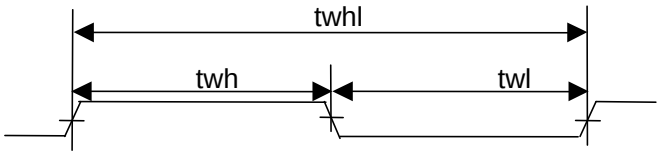
AC CHARACTERISTICS

(Ta=25ºC, PWMVdd=3.3V, DVdd=1.8V)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
XfsoIN Duty Ratio	duty(XfsoIN)		40	50	60	%
XfsiIN Duty Ratio	duty(XfsiIN)	512fsi	30	50	70	%
		256fsi	40	50	60	%
SCSHIFT Pulse time	tw (SCSHIFT)		160			nsec
SCDT Setup time	tsu (SCDT)		80			nsec
SCDT Hold time	th (SCDT)		80			nsec
SCLATCH Pulse Width	tw (SCLATCH)		160			nsec
SCLATCH Setup Time	tsu (SCLATCH)		160			nsec
SCLATCH Hold time	th (SCLATCH)		160			nsec
BCK Pulse Width	tw (BCK)		35			nsec
DATA Setup Time	tsu (DATA)		20			nsec
DATA Hold time	th (DATA)		20			nsec
LRCK Setup time	tsu (LRCK)		20			nsec
LRCK Hold time	th (LRCK)		20			nsec

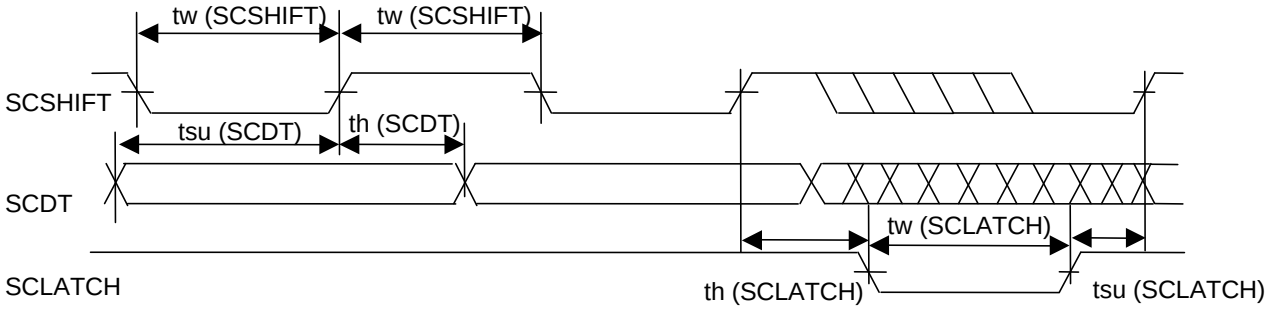
AC CHARACTERISTICS TIMING CHART

(1)XfsoIN, XfsiIN Duty Ratio

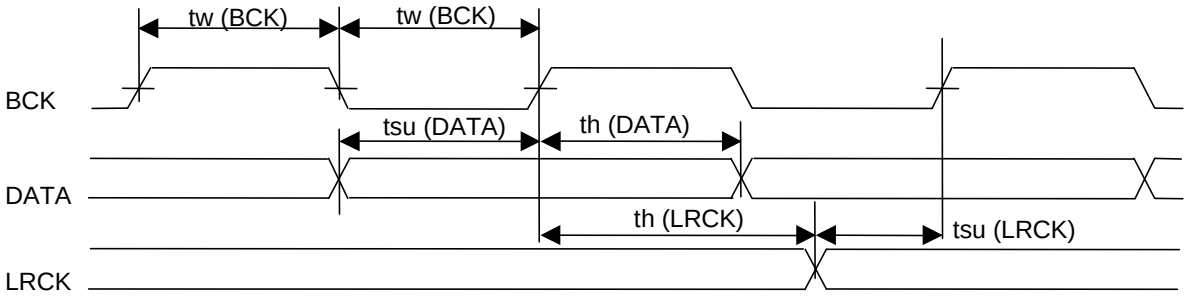


$$\text{duty (XfsoIN, XfiIN)} = \frac{twh}{twhl}$$

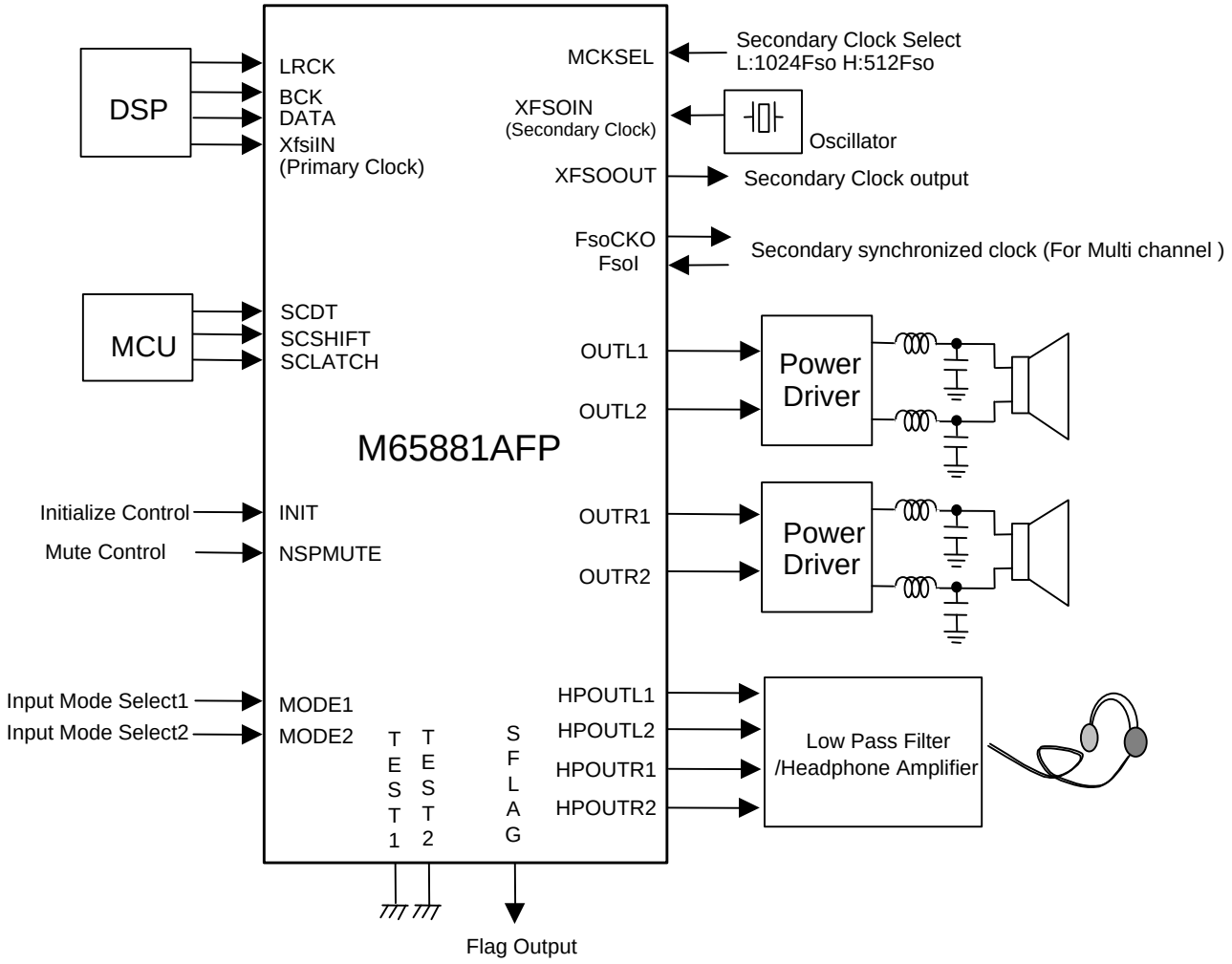
(2)SCSHIFT, SCDT, SCLATCH Input Timing



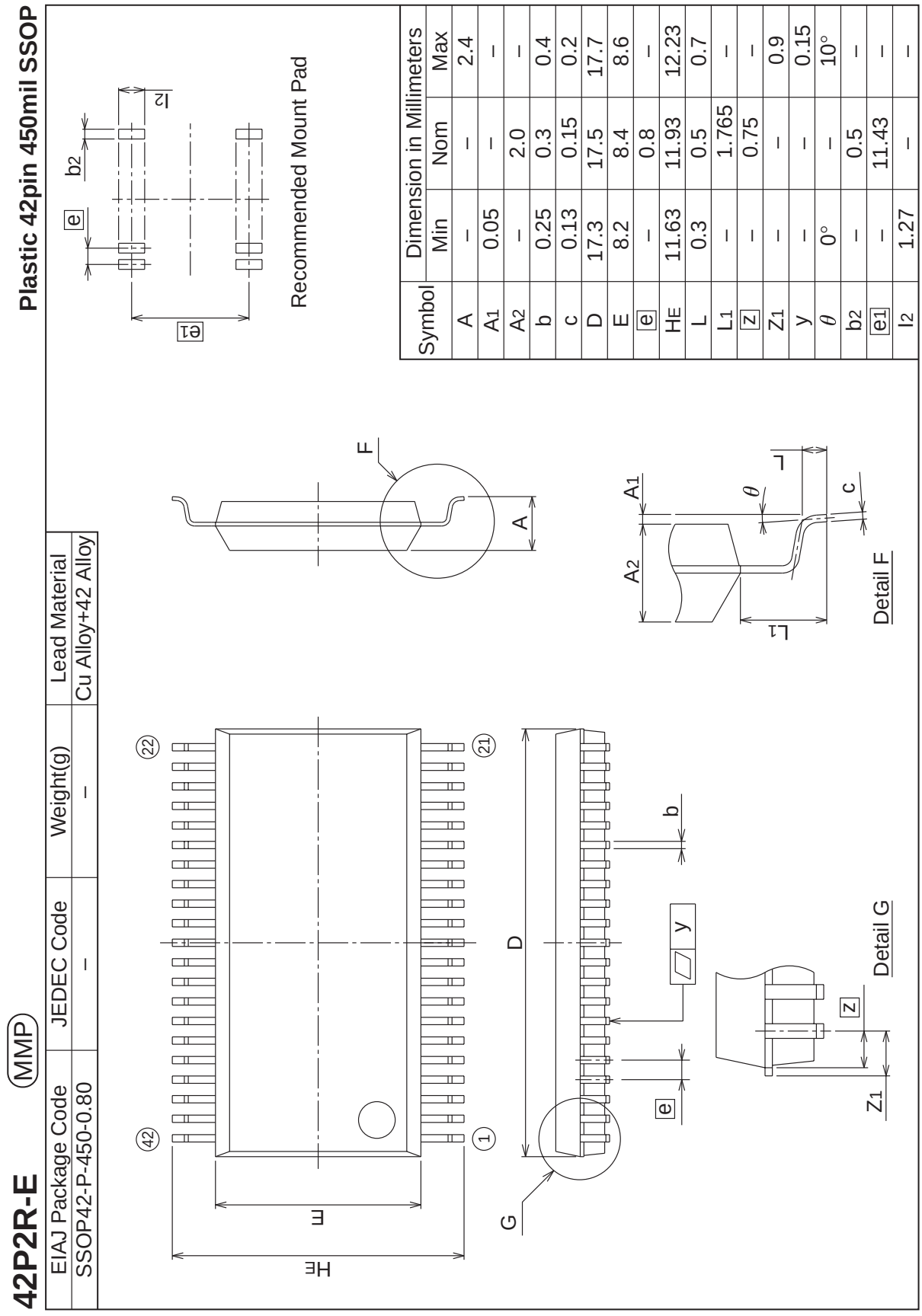
(3)BCK, DATA, LRCK Input Timing



APPLICATION EXAMPLE



DETAILED DIAGRAM OF PACKAGE OUTLINE



Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	–	–	2.4
A_1	0.05	–	–
A_2	–	2.0	–
b	0.25	0.3	0.4
c	0.13	0.15	0.2
D	17.3	17.5	17.7
E	8.2	8.4	8.6
e	–	0.8	–
H_E	11.63	11.93	12.23
L	0.3	0.5	0.7
L_1	–	1.765	–
z	–	0.75	–
Z_1	–	–	0.9
y	–	–	0.15
θ	0°	–	10°
b_2	–	0.5	–
e_1	–	11.43	–
l_2	1.27	–	–

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