Product Manual

3.5” Hard Disk Drives

SAMSUNG ELECTRONICS

SPINPOINT V40

JULY 7, 2001 (Rev 1.0)

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CHAPTER 1 SCOPE

Welcome to the SpinPoint V40 series of Samsung hard disk drives. This series of drives consists of the following models: SV2001H, SV3012H,SV4002H, SV6003H,SV6014H and SV8004H. This chapter provides an overview of the contents of this manual, including the intended user, manual organization, terminology and conventions. In addition, it provides a list of references that might be helpful to the reader.

1.1 User Definition

The SpinPoint V40 product manual is intended for the following readers:

- Original Equipment Manufacturers (OEMs)
- Distributors

1.2 Manual Organization

This manual provides information about installation, principles of operation, and interface command implementation. It is organized into the following chapters:

- Chapter 1 - SCOPE
- Chapter 2 - DESCRIPTION
- Chapter 3 - SPECIFICATIONS
- Chapter 4 - INSTALLATION
- Chapter 5 - DISK DRIVE OPERATION
- Chapter 6 - AT INTERFACE and ATA COMMANDS
- Chapter 7 - MAINTENANCE

In addition, this manual contains a glossary of terms to help you understand important information.

1.3 Terminology and Conventions

The following abbreviations are used in this manual:

µinches	Microinches(10^{-6} inches)
µs	Microseconds
Bpi	Bits per inch
DB	Decibels
Fci	Flux changes per inch
GB	Gigabytes
Hz	Hertz
Kbytes	Kilobytes
Lb	Pounds
M	Meter
MA	Milliampere
MB	Megabytes
Mbit/s	Megabits per second
Mbytes/s	Megabytes per second
MHz	Megahertz
Mil	Millinches
Ms	Milliseconds
MV	Millivolts
Ns	Nanoseconds
Rpm	Rotations per minute
Tpi	Tracks per inch
V	Volts
W	Watts

This manual uses the following conventions:

- **Computer Message**
  Computer message refers to items you type at the computer keyboard. These items are listed in all capitals in Courier New font. For example:

  FORMAT C:/S

- **Commands and Messages**
  Interface commands and messages sent from the drive to the host are listed in all capitals. For example:

  READ SECTORS

  WRITE LONG

- **Parameters**
  Parameters are given as initial capitals when spelled out and as all capitals when abbreviated. For example:
  Prefetch Enable: PE
  Cache Enable: CE

- **Names of Bits and Registers**
  Bit names and register names are presented in initial capitals. For example:
  Host Software Reset
  Sector Count Register

- **Hexadecimal Notation**
  Hexadecimal notation is identified using the small letterform. For example:
  30h

- **Signal Negation**
  An active low signal name is listed with a dash character (-) following the signal name. For example:
  IOR-

- **Notes**
  Notes are used after tables to provide you with supplementary information.

- **Host**
  In general, the system in which the drive resides is referred to as the host.

1.4 Reference

For additional information about the AT interface, refer to:

- ATA-2 (AT Attachment 2), Revision 3, January, 1995
- ATA-3 (Attachment-3 Interface) Revision 7b, 27 January, 1997
- ATA-4 (AT Attachment with Packet Interface Extension) Revision 18, 19 august 1998
- ATA-5 (AT Attachment with Packet Interface Extension) Revision 3, 29 February 2000
- ATA-6 (AT Attachment with Packet Interface Extension)

CHAPTER 2 DESCRIPTION

This chapter summarizes general functions and key features of the Spinpoint V40 drive, as well as the standards and regulations they meet.

2.1 Introduction

The Samsung SpinPoint V40 3.5 inch disk drives are high capacity, high performance random access storage devices, which use non-removable 3.5-inch disks as storage media. Each disk incorporates thin film metallic media technology for enhanced performance and reliability. And for each disk surface there is a corresponding movable head actuator assembly to randomly access the data tracks and write or read the user data. The formatted capacities of the SpinPoint V40 family are 20.0,30.06,40.0,60.0,60.06 and 80.0 gigabytes of storage. Samsung defines a gigabyte (GB) as one billion bytes.

The SpinPoint V40 drives include the AT controller embedded in the disk drive PCB electronics. The drive's electrical interface is compatible with all mandatory, optional and vendor-specific commands within the ATA specification.

Drive size conforms to the industry standard 3.5-inch form factor. The interface connectors are the standard 40-pin for AT Interface and 4-pin for DC power supplies.

The SpinPoint V40 incorporates Advanced GMR (Giant Magneto Resistive) head and Noise Predictive PRML (Partial Response Maximum Likelihood) signal processing technologies. These advanced technologies allow for an areal density of over 29.18 gigabits per square inch and storage capacity of over 40.06 gigabytes per disk.

The heads, disk(s), and actuator housing are environmentally sealed within an aluminum-alloy base and cover. As the disks spin, air circulates within this base and cover, commonly referred to as the head and disk assembly (HDA), through a non-replaceable absolute filter ensuring a contamination free environment for the heads and disks throughout the life of the drive.

2.2 Key Features

Key features of the SpinPoint V40 hard disk drives include:

- Formatted capacities are 20.0,30.06, 40.0, 60.0,60.06 and 80.0 Gbytes
- Low-profile, 1-inch height form factor
- 8.9 msec average seek time
- High accuracy rotary voice coil actuator with embedded sector servo
- Ultra ATA33/66/100 interface
- ATA standard PIO Mode 4/DMA Mode 2/Ultra DMA Mode 4 & 5(UDMA 66/100) support
- Supports both CHS and LBA Addressing modes
- Supports all logical geometries as programmed by the host

- Proprietary 2048KB read look-ahead cache with a segmented buffer and write stacking capability
- Transparent media defect mapping
- Read and write mode auto-reassign
- High performance in-line defective sector skipping
- Automatic error correction and retries
- Optimized 480-bit ECC and 7-byte CRC with 10 way interleave on-the-fly (OTF) correction
- Automatic magnet latch
- Noise predictive PRML read channel
- 2nd generation TA detection and correction
- Dynamic anti-stiction algorithm
- Advanced GMR head
- SMART support
- Cable select ability
- Supported Automatic Acoustic Management (AAM)

2.3 Standards and Regulations

The SpinPoint V40 depends upon its host equipment to provide power and appropriate environmental conditions to achieve optimum performance and compliance with applicable industry and governmental regulations. Special attention has been given in the areas of safety, power distribution, shielding, audible noise control, and temperature regulation.

The SpinPoint V40 hard disk drives satisfy the following standards and regulations:

- Underwriters Laboratory (UL): Standard 1950. Information technology equipment including business equipment.
- Canadian Standards Association (CSA): Standard C22.2 No.3000-201 Information technology equipment including business equipment.
- Technisher Überwachungs Verein (TUV): Standard EN 60 950. Information technology equipment including business equipment.

2.4 Hardware Requirements

SpinPoint V40 hard disk drives are designed for use with host computers and controllers that are PC/AT compatible. They are connected to a PC either by:

- Using an adapter board, or
- Plugging a cable from the drive directly into a PC motherboard with an IDE (Integrated Drive Electronics) interface.

CHAPTER 3 SPECIFICATIONS

This chapter gives a detailed description of the physical, electrical, and environmental characteristics of the SpinPoint V40 hard disk drives.

3.1 Specification Summary

Table 3-1 Specifications

DESCRIPTION	SV2001H	SV3012H	SV4002H	SV6003H	SV6014H	SV8004H
Number of Disks	1	1	1	2	2	2
Number of R/W heads	1	2	2	3	4	4
Maximum recording density (bpi)	504K					
Maximum flux density (fci)	536K					
Track density (tpi)	57,500/55,000/52,000					
Data tracks per surface (maximum)	55,850					
Encoding method	Noise Predictive PRML					
Interface	Ultra ATA / 66/100					
Actuator type	Rotary Voice Coil					
Servo type	Embedded Sector Servo					
Number of Cylinder Reserved	8					
Maximum Writing Frequency (MHz)	235.56					
Spindle speed (rpm)	5,400 ± 0.35%					

3.2 Physical Specifications

Table 3-2 Physical Specifications

DESCRIPTION	SV2001H	SV3012H	SV4002H	SV6003H	SV6014H	SV8004H
Track pitch (µinches)	17.39					
Data head flying height (µinches)	0.5					
Inner most data track radius (inches)	0.8204					
Outer most data track radius (inches)	1.8031					
Physical dimensions:						
Length (inches)	5.75					
Width (inches)	4.00					
Height (inches)	1.00					
Weight (lb)	1.4					

3.3 Logical Configurations

Table 3-3 Logical Configurations

DESCRIPTION	SV2001H	SV3012H	SV4002H	SV6003H	SV6014H	SV8004H
Default logical mode:						
Number of cylinders	38,869	58,246	77,622	116,374	116,375	155,127
Number of heads / cylinders	16	16	16	16	16	16
Number of sectors / heads	63	63	63	63	63	63
Total Number of logical sectors	39,179,952	58,711,968	78,242,976	117,304,992	117,306,000	156,368,016
Capacity	20.06 GB	30.06 GB	40.06 GB	60.06 GB	60.06 GB	80.06 GB

* Maximum number of logical cylinders in CHS mode is 16,383.
Systems that incorporate more than 8.4GB per storage device must access the drive in LBA addressing mode.

3.4 Performance Specifications

Table 3-4 Performance Specifications

DESCRIPTION	SV2001H	SV3012H	SV4002H	SV6003H	SV6014H	SV8004H
Seek Time (Rd/Wt, typical):						
Average seek time	8.9/10.0 msec					
Track to track seek time	0.8/1.0 msec					
Full stroke seek time	16.5/17.5 msec					
Data Transfer Rate: (Maximum)						
buffer to/from media	443 Mbits/s					
host to/from buffer	16.6/33/66/100 Mbytes/s					
Average latency	5.56 msec					
Rotational Speed	5,400 ± 0.35% rpm					
Motor spin up time (Typical)	10 sec					
Motor spin down time (Typical)	7 sec					
Buffer size	2048 Kbytes					

NOTES: ∗ Seek time is defined as the time from the receipt of a read, write or seek command until the actuator has repositioned and settled on the desired track with the drive operating at nominal DC input voltages and nominal operating temperature.

∗ Average seek time is determined by averaging the time to complete 1,000 seeks of random length.

∗ Average latency is the time required for the drive to rotate1/2 of a revolution and on average is incurred after a seek completion prior to reading or writing user data.

∗ Spin up time is the time elapsed between the supply voltages reaching operating range and the drive being ready to accept all commands.

3.5 Power Requirements

Table 3-5 Power Requirements

Mode	Typical Current (mA rms)		Typical Power (Watts)	Maximum Power (Watts)
	+5 Volts	+12 Volts		
Spin-up	750	2070	26	28.71
Normal	(400)	(235)	4.8	
Idle	(415)	(225)	4.8	
Random Seek (1)	(410)	(320)	6.0	
@ OD Read/Write (2)	(425)	(225)	5.0	
Standby	(60)	(15)	0.8	
Sleep	(60)	(15)	0.8	

1) Random seek: 30% Duty cycle seek commands with logical random location.

2) Read/Write @ OD: On track Read/Write operation at OD, 256 sector commands.

3.6 Environmental Specifications

Table 3-6 Environmental Specifications

DESCRIPTION	SV2001F	SV3012F	SV4002F	SV6003F	SV6014F	SV8004F
Ambient Temperature:						
Operating	5 ~ 55°C					
Non-operating	-40 ~ 70°C					
Maximum gradient without Condensation	20°C/15%/hr					
Relative Humidity (non-condensing):						
Operation	5~85 %					
Non-operation	5~95 %					
Maximum wet bulb temperature:						
Operating	30° C					
Non-operating	40° C					
Altitude (relative to sea level):						
Operating	-650 ~ 10,000 feet					
Non-operating	-1,000 ~ 40,000 feet					
Vibration (1/2 oct/min sweep sine):						
Operating						
5-21Hz	0.034" (double amplitude)					
21-300Hz	1.5 G (P-P) *					
300-500Hz	0.5 G (P-P) **					
Non-operating						
5-21Hz	0.195" (double amplitude)					
21-500Hz	8.0 G (p-p)					
* No more than 20% throughput degradation						
** No error during test						

Table 3-6 Environmental Specifications (continued)

DESCRIPTION		SV2001I	SV3012I	SV4002I	SV4002I	SV6014I	SV6003I
Shock (1/2 sine pulse);							
Operating	2.0 ms			63G			
Non-operating	2.0 ms			350G			
	1.0 ms			150G			
	0.5 ms			200G			
Rotational Shock							
Operating	2.0 ms			2K rad/sec ^{2}			
Non-operating	2.0 ms			20K rad/sec ^{2}			
	1.0 ms			20K rad/sec ^{2}			
Acoustic Noise (Typical Sound Power)							
Idle				3.1 bels			
Random Read/Write				3.3 bels			
Quite Seek				3.1 bels			

3.7 Reliability Specifications

Table 3-7 Reliability Specifications

DESCRIPTION	SV2001I	SV3012I	SV4002I	SV4002I	SV6014I	SV8004I
Recoverable Read Error:			<10 in 10^{11} bits			
Non-Recoverable Read Error:			<1 sector in 10^{14} bits			
MTBF (POH):			500,000 hours			
MTTR (typical):			5 minutes			
Start/Stop Cycles:						
Ambient			50,000			
Stressed			30,000			
Component Design Life:			5 years			

CHAPTER 4 INSTALLATION

This chapter describes how to unpack, mount, configure, and connect a SpinPoint V40 hard disk drive. It also describes how to install the drive in systems.

4.1 Space Requirements

Figure 4-1 shows the external dimensions of the drive.

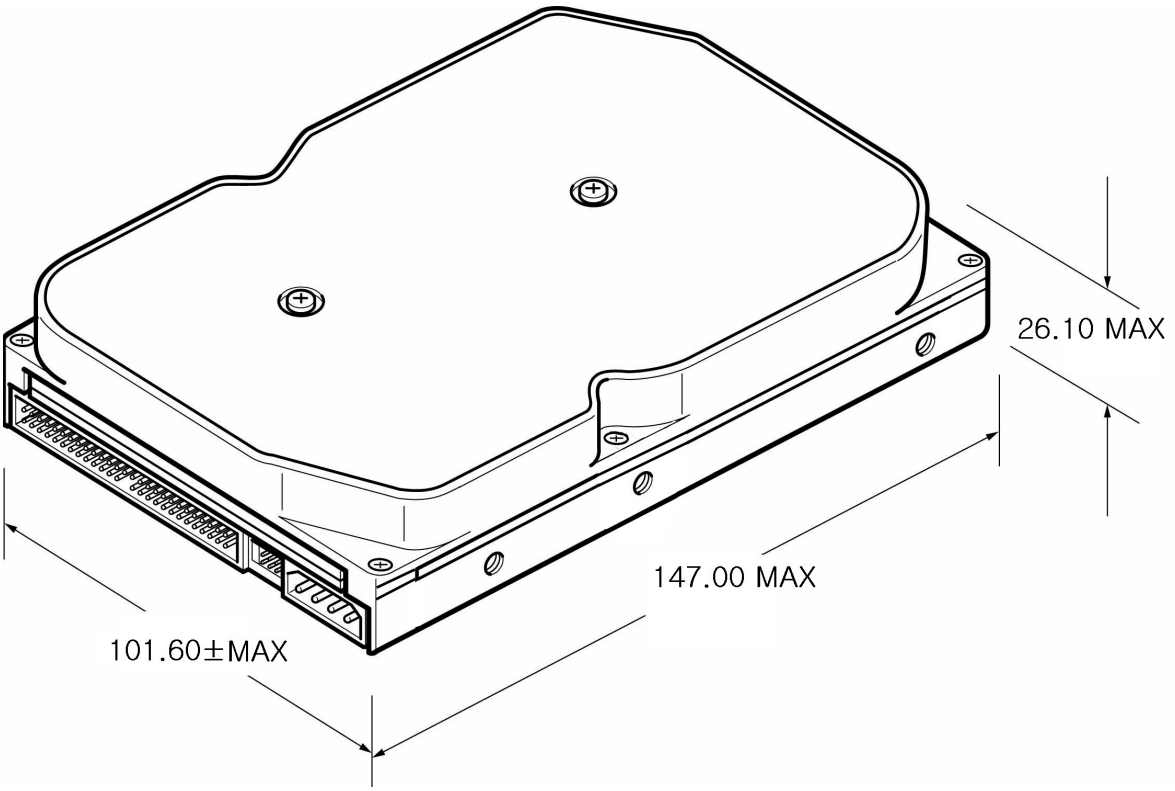


Figure 4-1 Mechanical Dimension

4.2 Unpacking Instructions

(1) Open the shipping container of the SpinPoint V40.

(2) Lift the packing assembly that contains the drive out of the shipping container.

(3) Remove the drive from the packing assembly. When you are ready to install the drive, remove it from the ESD (Electro Static Discharge) protection bag. Take precautions to protect the drive from ESD damage after removing it from the bag.

> **CAUTION: During shipment and handling, the anti-static ESD protection bag prevents electronic component damage due to electrostatic discharge. To avoid accidental damage to the drive, do not use a sharp instrument to open the ESD protection bag.**

(4) Save the packing material for possible future use.

4.3 Mounting

Refer to your system manual for complete mounting details.

(1) Be sure that the system power is off.

(2) For mounting, use four 6-32 UNC screws.

> **CAUTION*:* To avoid stripping the mounting-hole threads, the maximum torque applied to the screws must not exceed 8.0 Kg-cm (6.95 inch-pounds).**

4.3.1 Orientation

Figure 4-2 shows the physical dimensions and mounting holes located on each side of the drive. The mounting holes on SpinPoint V40 hard disk drives allow the drives to be mounted in any direction.

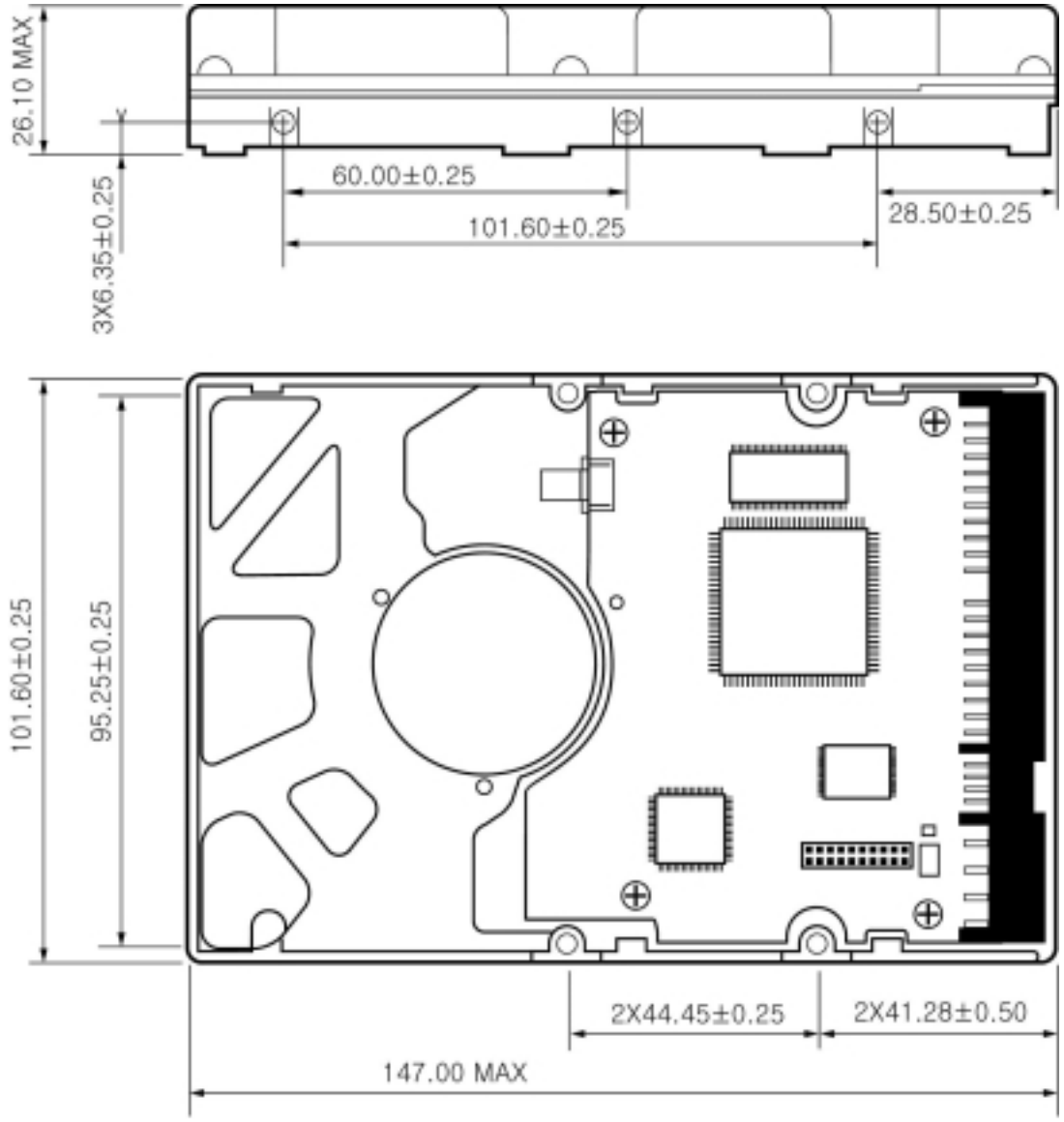


Figure 4-2 Mounting Dimensions (in Millimeters)

4.3.2 Clearance

The printed circuit board (PCB) is designed to be very close to the mounting holes. Do not exceed the specified length for the mounting screw described in Figure 4-3. The specified screw length allows full use of the mounting-hole threads, while avoiding damage or placing unwanted stress on the PCB.

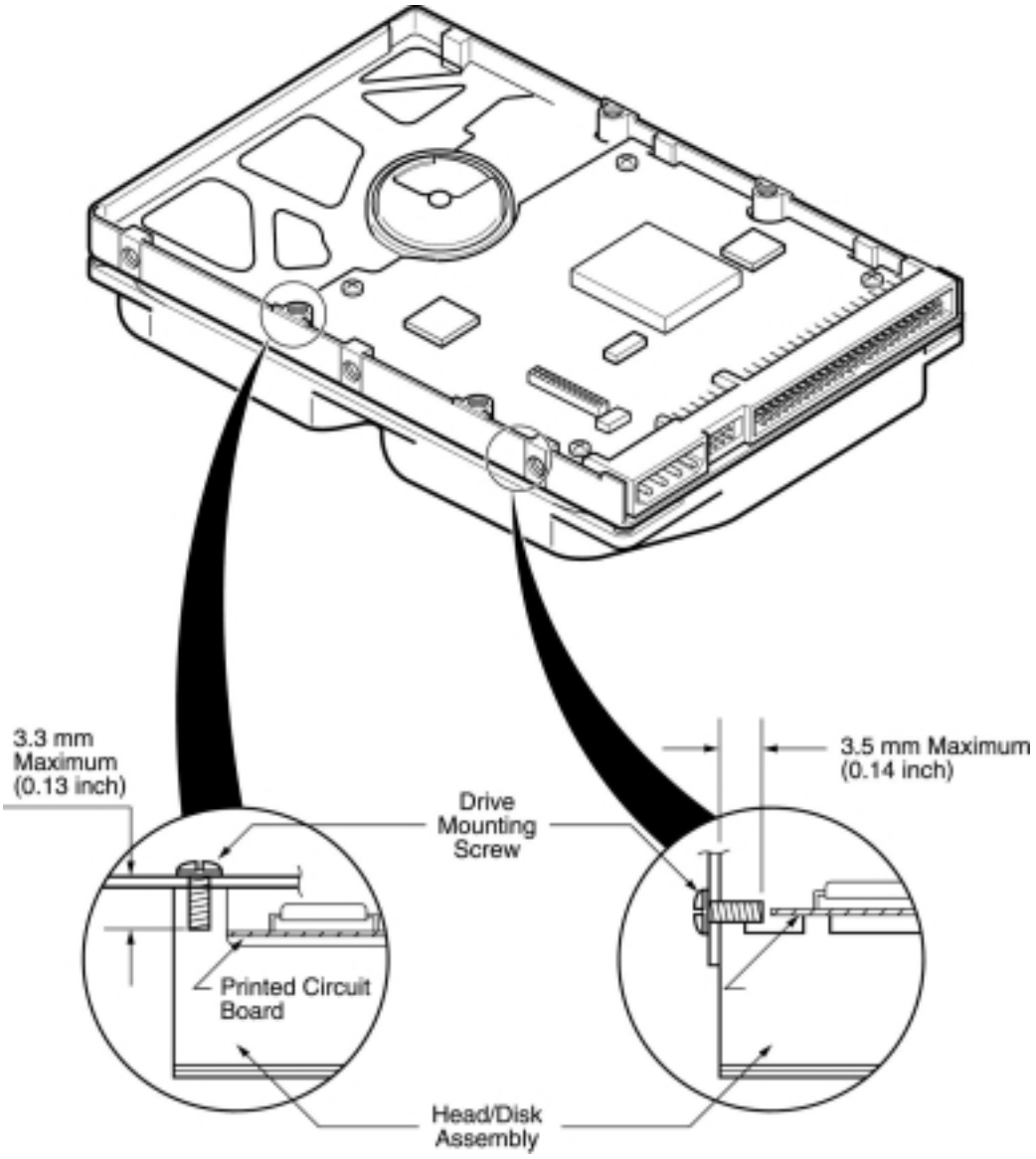


Figure 4-3 Mounting-Screw Clearance

CAUTION: Using mounting screws that are longer than the maximum lengths specified in Figure 4-3 voids the warranty of the drive.

4.3.3 Ventilation

SpinPoint V40 hard disk drives are designed to operate without the need of a cooling fan, provided the ambient air temperature does not exceed 55ºC. Any user-designed cabinet must provide adequate air circulation to prevent exceeding the maximum temperature.

4.4 Cable Connectors

The JHST connector consists of three portions; a DC power connector, a configuration jumper block, and the standard 40 pin AT-Bus Interface connector.

4.4.1 DC Power Connector

The DC power connector is mounted on the back edge of the Printed Circuit Board (PCB) (Figure 4-4). Table 4-1 lists the pin assignments.

Table 4-1 Power Connector Pin Assignment

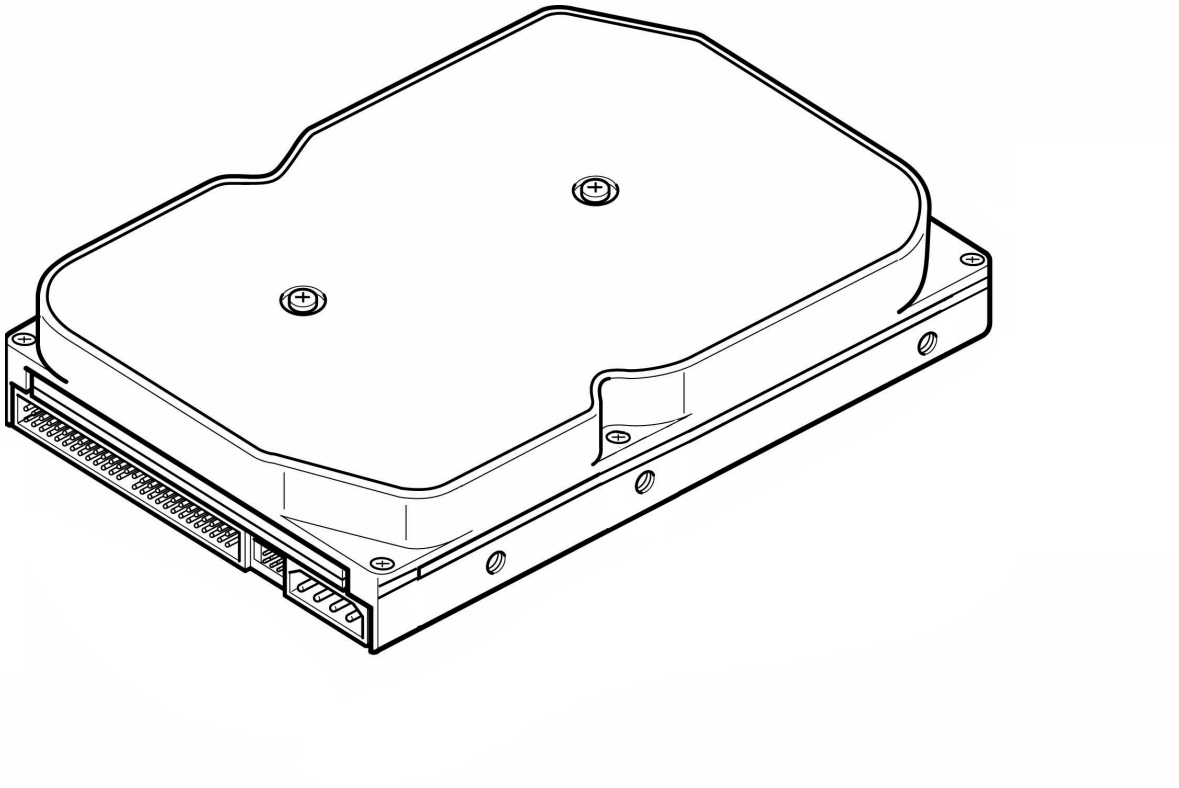
Pin Number	Power Line Designation
1	+12V DC
2	+12V Return (Ground)
3	+5V Return (Ground)
4	+5V DC

4.4.2 AT-Bus Interface Connector

The AT-Bus interface connector on the drive connects the drive to an adapter or an on-board AT adapter in the computer. JHST is a 40-pin Universal Header with two rows of 20 pins on 100-mil centers, as shown in Figure 4-4.

To prevent the incorrect installation of the I/F cable, the connector has been keyed by the removal of Pin #20. The connecting cable is a 40-conductor flat ribbon cable, and the maximum cable length is 0.46m (18 inches).

For pin assignments and signal descriptions, see Chapter 6, AT Interface and ATA Commands.



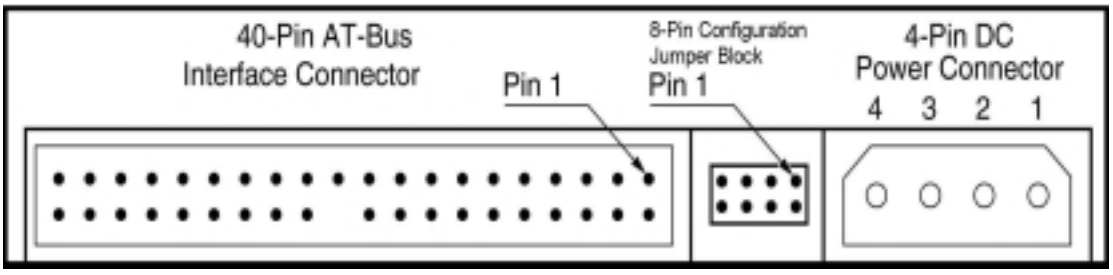
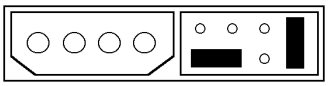


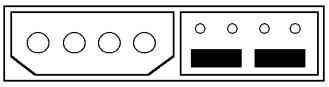
Figure 4-4 DC Power Connector, Configuration Jumper Block & AT-Bus Interface Connector (JHST)

4.5 Jumper Block Configurations



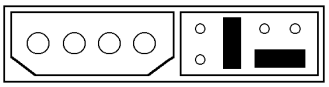
Master Mode

This mode is selected as the factory default. It configures the drive as the Master.



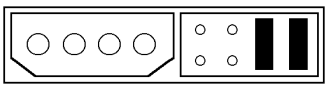
Slave Mode

Select this mode to configure the drive as the Slave.



Cable Select Mode

Select this mode if the Cable Select feature of the AT Bus Interface is to be used for Master / Slave selection.

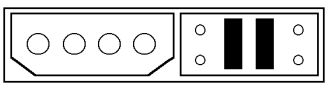


Master Mode with 32GB Clip

Select this mode to limit the capacity of the drive to 32 gigabytes and configure the drive as the Master, or to help install the drive to access the full capacity of the drive as the Master in certain old PC systems.

Slave Mode with 32GB Clip

Select this mode to limit the capacity of the drive to 32 gigabytes and configure the drive as the Slave, or to help install the drive to access the full capacity of the drive as the Slave in certain old PC systems.



Cable Select Mode with 32GB Clip

Select this mode to limit the capacity of the drive to 32 GB and use the Cable Select feature of the AT Bus Interface for Master / Slave selection, or to help install the drive to access the full capacity of the drive using Cable Select feature in certain old PC systems.

NOTES:

- The 32GB Clip may be required for the hard disk drive to be recognized by systems that incorporate specific older BIOS. For the installation instructions, refer to section “4.7.1 Drive Installation to Access the Full Capacity Using 32GB Clip.”

- The ATA standard allows for daisy-chaining up to two drives on the AT-Bus interface. When daisy-chaining two drives, specify one drive as the Master and the other as the Slave. Both drives could also be set to Cable Select Mode if the host is using the Cable Select feature of the AT Bus Interface.

- SpinPoint V40 hard disk drives are shipped from the factory in Master Mode (Drive 0).

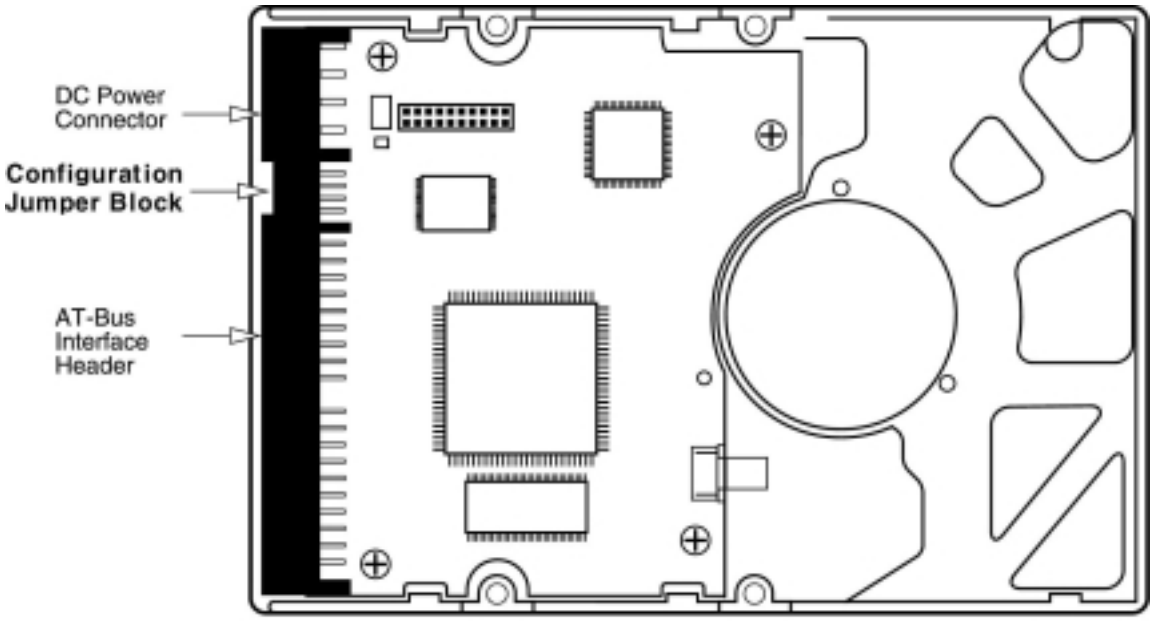


Figure 4-5 Jumper Pin Locations on the Drive PCBA

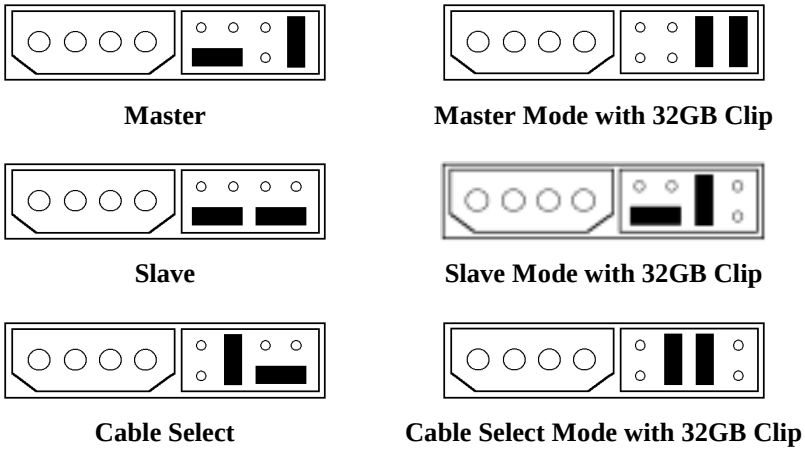


Figure 4-6 Options for Jumper Block Configuration

4.6 Drive Installation

The SpinPoint V40 hard disk drive can be installed in an AT-compatible system in two ways:

- To install the drive with a motherboard that contains a 40-pin AT-bus connector, connect the drive to the motherboard using a 40-pin ribbon cable. Ensure that pin 1 of the drive is connected to pin 1 of the motherboard connector.

- To install the drive in a system without a 40-pin, AT-bus connector on its motherboard, an AT-bus adapter kit is required. The kit includes an adapter board and a ribbon cable to connect the board to the drive.

Figure 4-7 indicates the cable and power cord connections required for proper drive installation.

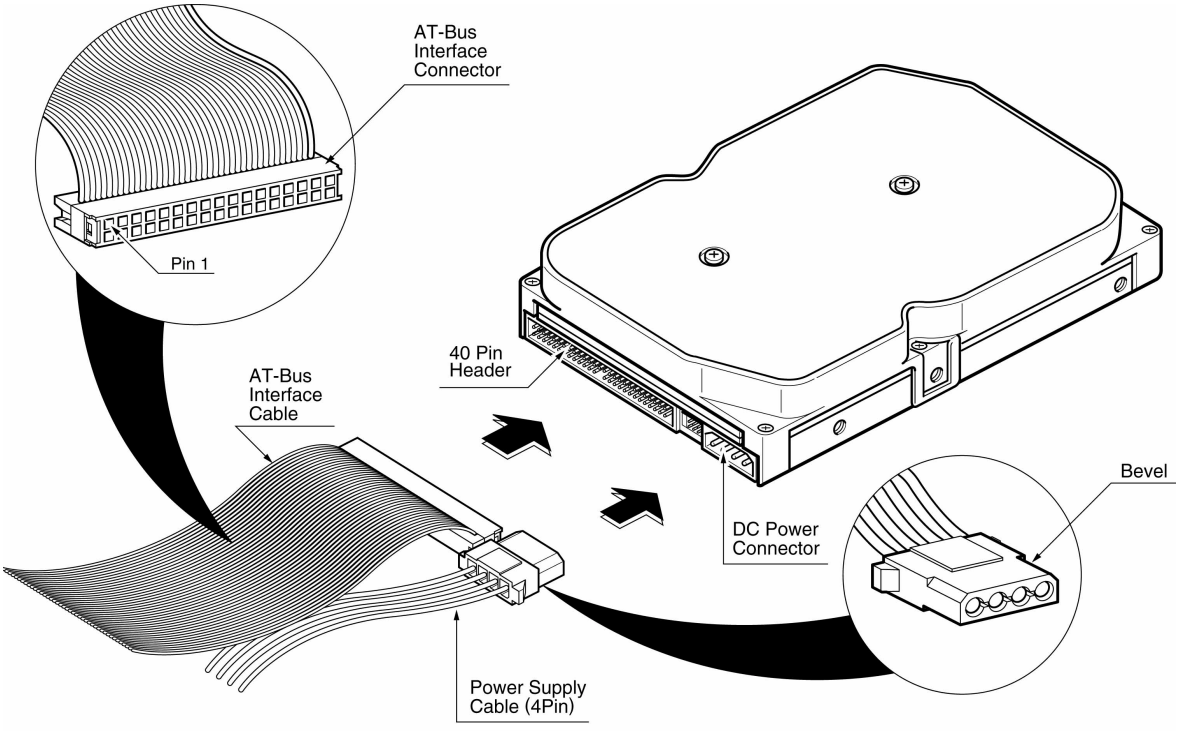


Figure 4-7 DC Power Connector and AT-Bus Interface Cable Connections

4.7 System Startup Procedure

Once the SpinPoint V40 hard disk drive and along with the adapter board (if required) have been installed in your system, the drive can now be partitioned and formatted for operation. To set up the drive correctly, follow these instructions:

1. Power on the system.

2. Typically the system will detect a configuration change automatically. If so, then jump to step 6.

3. If installing 80GB SpinPoint SV8004H model and the system hangs during boot up, follow the instructions in section "4.7.1 Drive Installation to Access the Full Capacity Using 32GB Clip".

4. If the system does not hang but does not automatically detect the drive either during reboot, run the setup program of the system. Setup program is usually on a diagnostics or utility disk, or in the system BIOS. Refer to the manual of your system for this operation. Once you get into setup program then follow step 5.

5. Perform one of the following steps that applies to your system:

   I. Select "Auto Detect" if it is supported.
   II. When using "User Defined" type, enter the appropriate parameters for the installed drive, according to Table 4-2.
   III. When using "Pre-Defined" type, select any drive type that does not exceed the maximum capacity of the drive. Table 4-2 shoes the logical parameters that provide the maximum capacity of SpinPoint V40 family drives.

6. If the system recognizes the drive but experiences problems on properly handling the full capacity of the drive, run Disk Manager utility program provided by Samsung and follow the instructions. The Disk Manager utility program is available from Samsung on a floppy diskette, or downloadable from the Samsung website at www.samsunghdd.com. If, after all these steps are successfully completed, your system will not boot up, then contact technical support.

Table 4-2 Logical Drive Parameters

PARAMETER	SV2001H	SV4002H	SV6003H	SV8004H
Logical Cylinders	20,060	77,622	60,060	155,127
Logical Heads	16	16	16	16
Logical Sectors	63	63	63	63
Total Number of Logical Sectors	39,179,952	78,242,976	117,304,992	156,368,016
Capacity	20.06 GB	40.06 GB	60.06	80.06 GB

NOTES:
- The total numbers of sectors is calculated by (Cylinders x Heads x Sectors) of the selected drive type.
- Maximum number of logical cylinders in CHS mode is 16,383.
- Systems that incorporate more than an 8.4GB per storage device must access the drive in LBA

addressing mode.

- Windows 95 or 98 that use FAT16 file system will limit the drive's logical partition at 2.1GB per logical drive. Windows95 OSR2 or later allow for the FAT32 file system which provides access to greater than 2GBof logical capacity.
- A low-level format is not required, as this was done at the factory before shipment.

4.7.1 Drive Installation to Access the Full Capacity Using 32GB Clip

A system hang condition is identified when the installation of a hard disk drive larger than 32GB is attempted into a PC system that incorporates specific older BIOS'. This issue is caused by the older BIOS' inability to support the full capacity of the hard disk drive, not by the SpinPoint V40 hard disk drive.

One solution to this issue, is to contact the system or motherboard manufacturer and upgrade the BIOS (to enable the system to access the full capacity of the hard disk drive).

As an alternative solution, the drive can be installed by using a 32GB clip jumper on the SpinPoint V40 hard disk drive, along with the Disk Manager utility program. To set up the drive using 32GB clip, follow the instructions provided below:

1. Install a 32 GB clip jumper (see section 4.5).
2. Boot up the system, enter SYSTEM SETUP, change the settings for the drive to "Auto", and exit SYSTEM SETUP.
   NOTE: At this point in the installation, the drive capacity is limited to 32GB. No further steps are needed if the drive is intended to be used as 32 gigabytes.
3. To access the full capacity, reboot the system with the Disk Manager diskette. Disk Manager will install Dynamic Drive Overlay on the drive. The Dynamic Drive Overlay will take control of the drive from the BIOS each time the system is booted, and enable access to the entire capacity of the drive.
4. Select "Easy Disk Installation"
5. Select drive to be installed (master or slave)
6. Select the operating system (Win95 OSR2, 98, 98SE, Me, 2000, or NT)
7. Follow the instruction to format drive

NOTE;
Microsoft identified a 32GB capacity limitation issue with the Windows 95 operating system. The solutions provided above do not overcome the capacity limitation of the Windows 95 operating system. Microsoft recommends that Windows 95 customers who want to use media larger than 32GB, upgrade to Microsoft Windows 98 or Microsoft Windows NT. For more information, please check Microsoft Knowledgebase.

CHAPTER 5 DISK DRIVE OPERATION

This chapter describes the operation of the SpinPoint V40 functional subsystems. It is intended as a guide to the operation of the drive, rather than a detailed theory of operation.

5.1 Head / Disk Assembly (HDA)

A SpinPoint V40 hard disk drive consists of a mechanical sub-assembly and a printed circuit board assembly (PCBA), as shown in Figure 5-1. This section describes the mechanism of the drive.

The head / disk assembly (HDA) contains the mechanical sub-assemblies of the drive, which are sealed between the aluminum-alloy base and cover. The HDA consists of the base casting assembly (which includes the DC spindle motor assembly), the disk stack assembly, the head stack assembly, and the rotary voice coil motor assembly (which includes the actuator latch assembly). The HDA is assembled in a clean room. These subassemblies cannot be adjusted or field repaired.

CAUTION: To avoid contamination in the HDA, never remove or adjust its cover and seals. Disassembling the HDA voids your warranty.

SpinPoint V40 disk drive models and capacities are distinguished by the number of heads and disks. The SV4002H has one (1) disk and two (2) read/write heads. The SV8004H has two (2) disks and four (4) read/write heads.

5.1.1 Base Casting Assembly

A one piece, aluminum-alloy base casting provides a mounting surface for the drive mechanism and PCBA. The base casting also serves as the flange for the DC spindle motor assembly. A gasket provides a seal between the base and cover castings that enclose the drive mechanism.

5.1.2 DC Spindle Motor Assembly

The DC spindle motor assembly consists of the brush-less three-phase motor, spindle bearing assembly, disk mounting hub, and a labyrinth seal. The entire spindle motor assembly is completely enclosed in the HDA and screwed to the base casting. The labyrinth seal prevents bearing lubricant from coming out into the HDA. The motor rotates the spindle shaft at 5400 rpm.

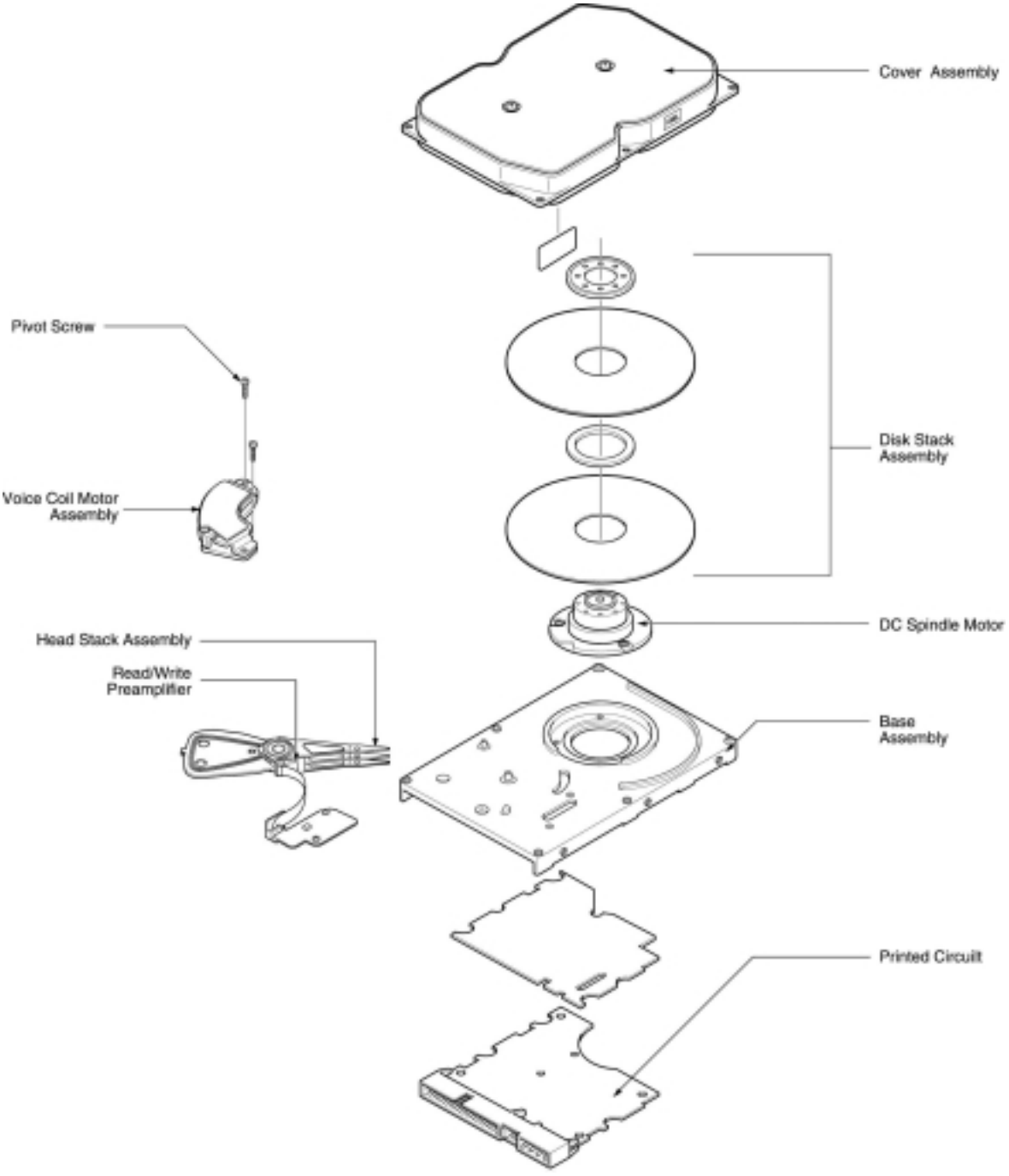


Figure 5-1 Exploded Mechanical View

5.1.3 Disk Stack Assembly

The disk stack assembly in the SpinPoint V40 hard disk drive consists of 1 or 2 disks and disk spacers secured on the hub of the spindle motor assembly by a disk clamp. The aluminum-alloy disks have a sputtered thin-film magnetic coating.

A carbon overcoat lubricates the disk surfaces to prevent heads and media wear due to the repeated head contacts with disk surfaces during head take-offs and landings. Contact between heads and disk surfaces occurs only in the landing zone outside of the data area, when the disks are rotating at slower than normal speed during spin up or down. The landing zone is located at the inner diameter of the disk, far beyond the last cylinder of the data area.

5.1.4 Head Stack Assembly

The head stack assembly consists of an E-block/coil sub-assembly, read/write heads, a flexible circuit, and bearings. The E-block/coil sub-assembly is assembled with an E-block and over-molded coil. Read/write heads are mounted to spring-stainless steel flexures that are then swage mounted onto the E-block arms.

The flexible circuit connects the read/write heads with the PCBA via a connector through the base casting. The flexible circuit contains a read/write Preamplifier IC.

5.1.5 Voice Coil Motor and Actuator Latch Assemblies

The rotary voice coil motor consists of upper and lower permanent magnets and magnetic yokes fixed to the base casting and a rotary over-molded coil on the head stack assembly. Each magnet consists of two alternating poles and is attached to the magnet yoke. Rubber crash stops mounted on the over-molded coil and a magnetic yoke physically prevent the head(s) from moving beyond the designed inner boundary into the spindle or off the disk surface.

Current from the power amplifier induces a magnetic field in the voice coil. Fluctuations in the field around the permanent magnets move the voice coil so that heads can be positioned in the requested cylinder.

5.1.6 Air Filtration System

Heads fly very close to the disk surfaces. Therefore, it is very important that air circulating within the drive be maintained free of particles. Samsung HDAs are assembled in a purified air environment to ensure cleanliness and then sealed with a gasket. To retain this clean air environment, the SpinPoint V40 is equipped with a re-circulating filter, which is located in the path of the airflow close to the rotating disk and is designed to trap any particles that may develop inside HDA.

5.2 Drive Electronics

SpinPoint V40 drives attain their intelligence and performance through the specialized electronic components mounted on the PCBA. The components are mounted on one side of the PCBA.

The Preamplifier IC is the only electrical component that is not on the PCBA. It is mounted on the flexible circuit inside the HDA. Locating the Preamplifier IC as close as possible to the read/write heads via surface mount technology improves the signal to noise ratio.

5.2.1 Digital Signal Process and Interface Controller

The DSP core controller incorporates a true 16-bit digital signal processor (DSP), a bus controller unit(BCU), an interrupt controller unit(ICU), a general purpose timer(GPT), and a 8K word SRAM.

5.2.2 AT Disk Controller

The AT disk controller works in conjunction with the DSP core to perform the ATA interface control, buffer data flow management, disk format/read/write control, and error correction functions of an embedded disk drive controller. The DSP communicates with the disk controller module by reading from and writing to its various internal registers.

To the DSP core, the registers of the disk controller appear as unique memory or I/O locations that are randomly accessed and operated upon. By reading from and writing to the registers, the DSP core initiates operations and examines the status of the different functional blocks. Once an operation is started, successful completion or an error condition may cause the disk controller to interrupt the DSP core, which then examines the status registers of the disk controller and determines an appropriate course of action. The local DSP core may also poll the device to ascertain successful completion or error conditions.

Figure 5-2 illustrates the relationships between the various blocks within the AT disk controller. These blocks will be referred to throughout this document.

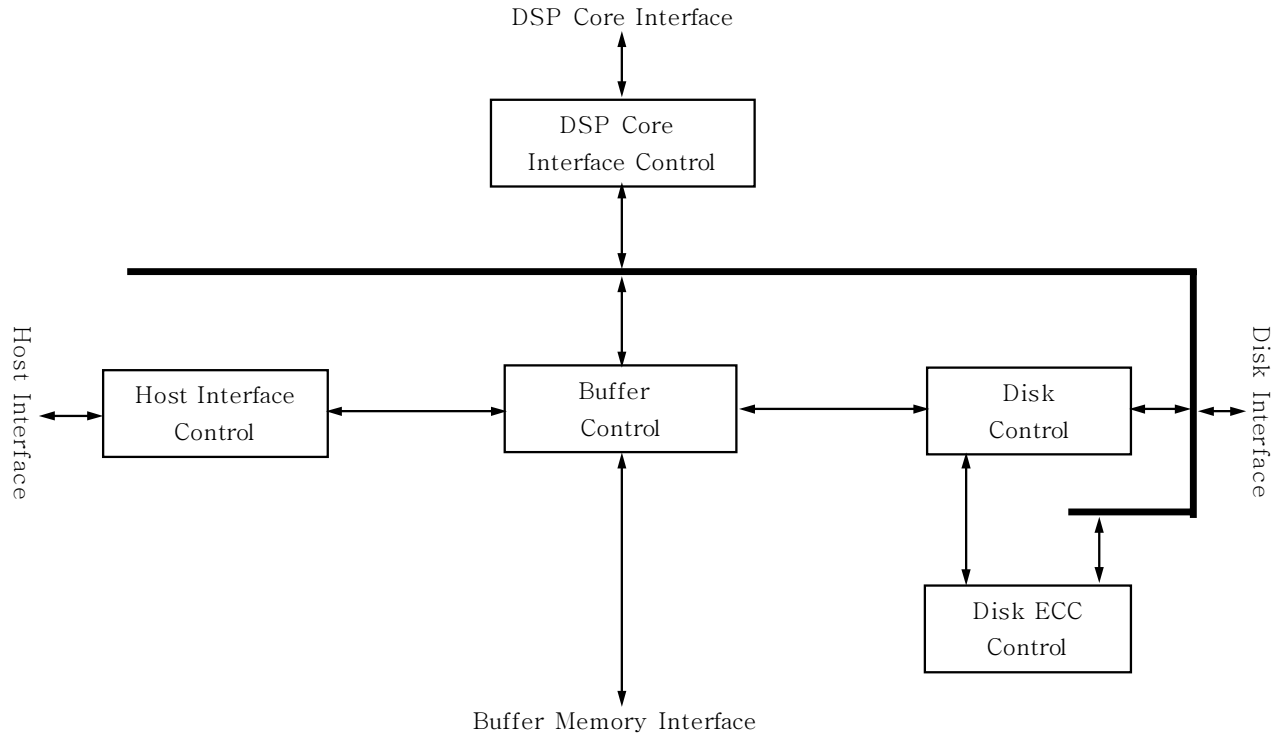


Figure 5-2 SID2001 AT Controller Block Diagram

5.2.2.1 The Host Interface Control Block

The SID2001 AT Controller provides an ATA interface to the host computer and can attach to an ATA-1, 2,3,4 or ATA-5 host. It provides a means for the host to access the Task File registers used to control the transfer of data between host memory and the disk.

The Host Interface Control block can be programmed to execute various host read/write commands either completely automatically without any DSP intervention, semi-automatically with minimal DSP intervention, or manually with the aid of the DSP.

Of particular interest to most designers are the significant advances in ATA automation, which have been incorporated into the AT controller of SID2001. The highlights of ATA automation are:

- Automatic data transfer management for multi-sector Read/Write commands without DSP intervention.
- Automatic data transfer management for Read/Write Multiple commands without DSP intervention.
- Automatic execution of read commands (Auto-Read command execution) for cached data in the buffer by matching the first sector.
- Auto-Write command execution (first sector of a multiple sector write operation is automated, or the transfer of one sector of the selected single sector write operation is automated).
- Automatic Task File registers updates during automatic multi-sector transfers.
- Programmable methods of IRQ assertion allow automation to work with different BIOS implementations and different device drivers.
- Capability to execute multiple consecutive Auto-Write commands without loss of data in the buffer.
- 96-byte host FIFO to allow automation to occur smoothly during discontinuities in transfers on the ATA interface.
- Ability to pause the ATA automatic transfers between the host and buffer on sector and block boundaries.
- Automation of an extensive portion of the ATA command set.

The SID2001 also supports a basic ATAPI reset command.

The SID2001 supports both PIO and DMA type transfers. The supported DMA type transfers include multi-word, and synchronous DMA transfers. DMA transfers and PIO transfers utilize the bus in 8- or 16-bit mode, depending upon the command being executed. The bus is automatically switched between 16- and 8-bit mode while performing Read Long and Write Long commands at the time of ECC byte transfers.

Additional functionality is provided in the Host Interface Control block by the following features:

- Programmable transfer length for automatic ECC byte transfer on the AT bus.
- Automatically inserted wait states are provided to support the IOCHRDY signal pin functions at any ATA interface speed.

- Support for Master/Slave configuration of two embedded disk controller drives.
- Automatic detection of Host status reads.
- Support of both LBA and CHS Task File registers formats.
- Automatic detection of both the software AT reset and hardware AT reset.
- Support for PIO modes 0 through 4.
- Support for multiword DMA modes 0 through 2.
- Support for synchronous DMA (UDMA) transfer mode 0 through 4.

5.2.2.2 The Buffer Control Block

The Buffer Control block manages the flow of data into and out of the buffer. Significant automation allows buffer activity to take place automatically during read/write operations between the host and the disk. This automation works together with automation within the Host Interface Control and Disk Control blocks to provide more bandwidth for the local microprocessor to perform non-data flow functions.

The buffer control circuitry keeps track of buffer full and empty conditions and automatically works with the Disk Control block to stop transfers to or from the disk when necessary. In addition, transfers to or from the host are automatically stopped or started based on buffer full or empty status.

A prioritized five ports architecture is implemented. All ports, except the refresh port, utilize 22-bit buffer address pointers.

The data path to the buffer RAM can be configured as 16-bit path in ATA mode.

SDRAM is fixed at 16 Mbits external. 32-byte Page Mode accesses, along with RAS refresh, are implemented. The full buffer bandwidth of SID2001 is 145 Mbytes/sec.

Additional functionality is provided in the Buffer Control block through the following features:

- Increased automation to support minimal latency read operations with minimal latency.
- Capability to support the execution of multiple consecutive Auto-Write commands without loss of data due to overwriting of data.
- Auto write pointer.
- A disk sector counter that can monitor the transfers between the disk and buffer.
- One VBSC(valid buffer sector counter) register for use with any schedule VBSC value.
- Read/Write cache support.

5.2.2.3 The Disk Control Block

The SID2001 Disk Control block manages the flow of data between the disk and the buffer. It is capable of performing completely automated track read and write operations at a maximum data rate of 443 Mbits/sec in byte wide NRZ mode. Many flexible features and elements of automation have been incorporated to complement the automation contributed by the Host and Buffer blocks.

The Disk Control block consists of the programmable sequencer (Disk Sequencer), CDR/data split logic, disk FIFO, fault tolerant sync detect logic, and other support logic.

The programmable sequencer contains a 31-by-2 byte programmable SRAM and associated control logic, which is programmed by the user to automatically control all single track format, read, and write operations. From within the sequencer micro program, the Disk Control block can automatically deal with such real time functions as defect skipping, servo burst data splitting, branching on critical buffer status and data compare operations. Once the Disk Sequencer is started, it executes each word in logical order. At the completion of the current instruction word, it either continues to the next instruction, continues to execute some other instruction based upon an internal or external condition having been met, or it stops.

During instruction execution or while stopped, registers can be accessed by the DSP to obtain status information reflecting the Disk Sequencer operations taking place.

In addition to the flexible Disk Sequencer, the Disk Control block contains many other features, which are available to satisfy diverse requirements. These include:

- Support for optimized zero latency read operations, with minimal DSP intervention.
- Disk Transfer Length registers monitoring in Disk Sequencer.
- Programmable “Wrap To” registers.
- Ability to specify at which sector to wrap “Wrap To” register, independent of the stopping sector.
- Index counter for power management command support.
- Time-out support when waiting for Sync, Index, Sector, and End of Servo burst to relieve DSP of overhead associated with managing time outs.
- Optional 2-byte fault tolerant byte Sync and external Sync is available.
- Split data support from DSP or buffer.
- A 96-byte FIFO between the buffer and the Disk Control block smoothes out data flow attributed to discontinuities in data or differences in speed.
- Read Gate and Write Gate are directly controlled by the Disk Sequencer micro program.
- Programmable initial condition of NRZ Write data at time of Write Gate assertion.
- Optional manual release of Sector to Host via the Disk Sequencer.
- Optional automatic release of Sector to Host if uncorrectable ECC error.

Features used to support header-less formats include:

- End of Servo (EOS) counter.
- EOS MAX register, which allows the EOS, counter to wrap at a specified value.
- Ability to clear the EOS counter by Index.
- Current Sector counter (Disk Sequencer Physical Position Counter).
- Ability to reset current CDR instruction.
- Defect FIFO optionally supplies defect location information to Disk Sequencer.
- Automatic internal Sector Mark generation (no external Sector Mark needed).
- Automatic Sector/Servo Mark alignment.

5.2.2.4 The Disk ECC Control Block

The SID2001 supports a programmable 10-way interleaved Reed-Solomon ECC. The code is capable of correcting up to ten 3 bytes, one 30 bytes bursts in hardware up to or 60 bytes correction with erasure pointer. The Disk ECC block also supports 32 bits of ESN (Embedded Sector Number) to the ECC generator to allow for greater data integrity in a headerless environment. Error detection and correction is handled in the Disk Control block. Automatic on-the-fly hardware correction will take place for up to three symbols in error per interleave. Correction is guaranteed to complete before the ECC Field of the sector following the sector where the error occurred utilizing standard ATA size sectors. Optional burst limiting can be used to decrease the probability on misdetection and mis-correction. An added feature of the SID2001 ECC block is the ability to log corrected ECC errors.

5.2.2.5 Frequency Synthesizer

The frequency synthesizer is a clock frequency generation circuit used to generate a DSP clock, AT disk controller and servo clock from the External Reference clock input.

5.2.2.6 Power Management

Power management features are incorporated into each block of the SID2001. This allows the designer to tailor the amount of power management to the specified design. Other power management features include:

- Independent power management control for each block.
- DSP block powered down and up when needed.
- Disk Sequencer and associated disk logic powered up when the Disk Sequencer is started.
- Weak pull-up structure on input pins to prevent undesirable power consumption due to floating CMOS inputs.

5.2.3 Read/Write IC

The Read/Write IC, shown in Figure 5-3 provides read/write-processing functions for the drive. The Read/Write IC receives the RD GATE and WR GATE signals, write data, and servo AGC and gates from the Interface Controller. The Read/Write IC sends decoded read data and the read reference clock. It receives write data from the Interface Controller.

The 88C5200 is a sampled-data digital PRML channel designed to work with a disk controller and a read/write preamplifier to provide the signal processing elements required to build a state
of the art high density, high speed disk drive. The 88C5200 implements a noise predictive, PRML Viterbi read channel (supporting) zone-bit recording ,

The read/write channel functions include a time base generator, AGC circuitry, asymmetry correction circuitry (ASC), analog anti-aliasing low-pass filter, analog to digital converter (ADC), digital FIR filter, timing recovery circuits, Viterbi detector, sync mark detection, 32/34 rate block code ENDEC, serializer and de-serializer, and write pre-compensation circuits. Servo functions include servo data detection and PES demodulation. Additionally the 88C5200 contains specialized circuitry to perform various parametric measurements on the processed read signal. This allows for implementation of self-tuning and optimization capability in every drive built using the 88C5200.

A 9-bit NRZ interface is provided to support high speed data transfers to and from the controller. Programming of the 88C5200 is performed through a serial interface. The serial interface is also used to read various channel parameters that are computed on the fly.

5.2.3.1 Time Base Generator

The time base generator provides the write frequency and serves as a reference clock to the synchronizer during non-read mode.

5.2.3.2 Automatic Gain Control

The AGC accepts a differential signal from the pre-amp, and provide a constant output amplitude to the analog filter. It's capable of accepting signal ranges from 40 mV to 400 mVppd.

5.2.3.3 Asymmetry Correction Circuitry (ASC)

The ASC circuit is designed to correct for amplitude asymmetry introduced by MR heads. The compensation range of this circuit is +/-45%. This circuit allows optimal bias current to be used independent of the asymmetry effect.

5.2.3.4 Analog Anti-Aliasing Low Pass Filter

The 7^{th} order equal-ripple analog filter provide filtering of the analog signal from AGC before it's being converted to digital signal with the ADC. It's main function is to avoid aliasing for the ADC circuit.

5.2.3.5 Analog to Digital Converter (ADC) and FIR

The output of the analog filter is quantified using a 6 bit FLASH ADC. The digitized data is then equalized by the FIR to the NPV target response for Viterbi detection. The FIR filter consists of 7 independent programmable taps.

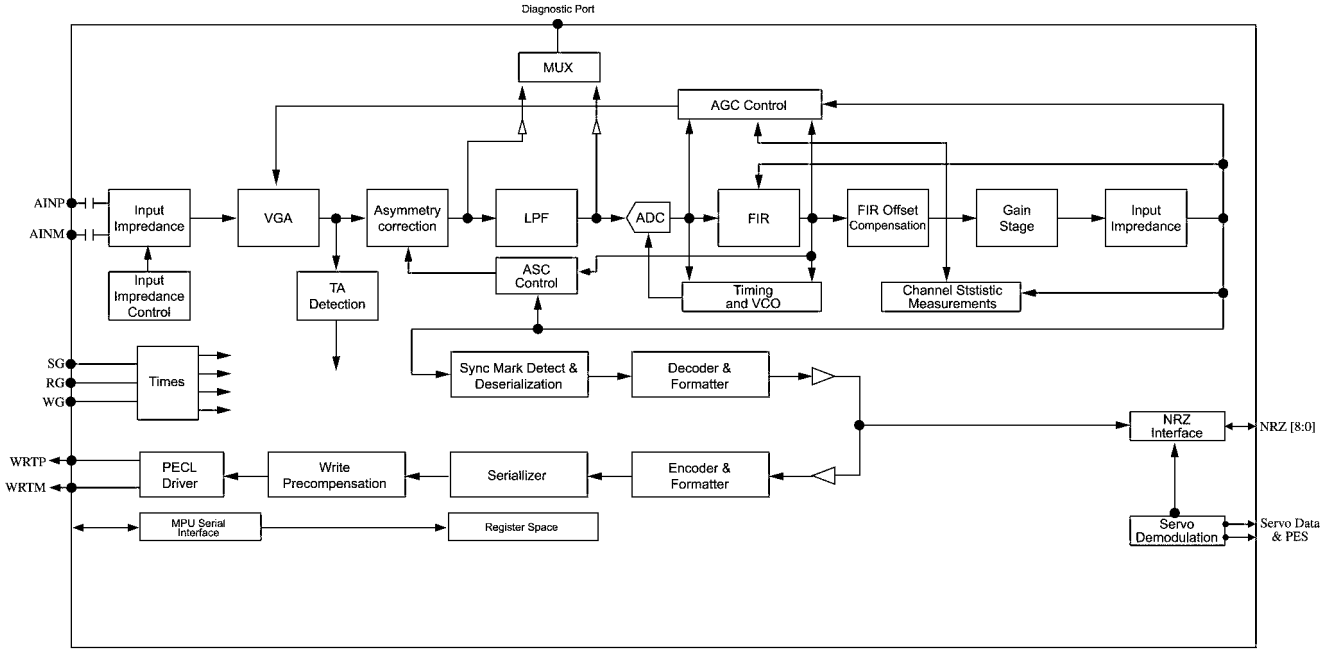


Figure 5-3 Read/Write 88C5200

5.3 Servo System

The Servo System controls the position of the read/write heads and holds them on track during read/write operations. The Servo System also compensates for MR write/read offsets and thermal offsets between heads on different surfaces and for vibration and shock applied to the drive.

The SpinPoint V40 is an Embedded Sector Servo System. Positioning information is radially located in 192 evenly spaced servo sectors on each track.

Radial position information can be provided from these sectors for each data head, 192 times per revolution. Because the drive incorporates multiple data zones and each zone has a different bit density, split data fields are necessary for optimal use of the non-servo area of the disk. The servo area remains phase-coherent across the surface of the disk, even though the disk has various data zones. The main advantage of the Embedded Sector Servo System is that it eliminates the problems of static and dynamic offsets between heads on different surfaces. The SpinPoint V40 Servo System is classified as a digital servo system because track-following and seek control, bias cancellation, and other typical tasks are done in a Digital Signal Processor (DSP).

The Servo system has three modes of operation: track-following mode, settle mode, and velocity control mode.

1. Track-following mode is used when heads are “on-track.” This is a position loop with an integrator in the compensation.
2. Settle mode is used for all accesses; head switches, short-track seeks and long-track seeks. Settle mode is a position loop with velocity damping. Settle mode does not use feed forward.
3. Velocity control mode is used for acceleration and deceleration of the actuator for a seek of two or more tracks. A seek operation of this length is accomplished with a velocity control loop. The drive’s ROM stores the velocity profile in a look-up table.

The feed forward compensation is used while the bandwidth of the control loop is kept low.

5.4 Read and Write Operations

The following two sections describe the read and write channels.

5.4.1 The Read Channel

The drive has one read/write head for each of the data surfaces. The signal path for the Read Channel starts at the read/write heads. When the magnetic flux transitions recorded on a disk pass under the head, they generate low-amplitude, differential output voltages. The read/write head transfers these signals to the flexible circuit’s amplifier, which amplifies the signal.

The flexible circuit transmits the pre-amplified signal from the HDA to the PCBA. The EPRML channel on the PCBA shapes, filters, detects, synchronizes, and decodes the data from the disk. The Read/Write IC then sends the resynchronized data output to the SID2001 DSP & Interface/Disk Controller.

The SID2001 Disk Controller manages the flow of data between the Data Synchronizer on the Read/Write IC and its AT Interface Controller. It also controls data access for the external RAM buffer. The ENDEC of 88C5200 decodes the 32/34 with post-processor format to produce a serial bit stream. This NRZ (Non Return to Zero) serial data is converted to 8-bit bytes.

The Sequencer module identifies the data as belonging to the target sector. After a full sector is read, the SID2001 checks to see if the firmware needs to apply an ECC algorithm to the data.
The Buffer Control section of the SID2001 stores the data in the cache and transmits the data to the AT bus.

5.4.2 The Write Channel

The signal path for the Write Channel follows the reverse order of that for the Read Channel. The host transmits data via the AT bus to the SID2001 Interface Controller. The Buffer Controller section of the SID2001 stores the data in the cache. Because the data is transmitted to the drive at a rate that exceeds the rate at which the drive can write data to the disk, data is stored temporarily in the cache. Thus, the host can present data to the drive at a rate independent of the rate at which the drive can write data to the disk.

Upon correct identification of the target address, the data is shifted to the Sequencer, which generates and appends an error correcting code. The Sequencer then converts the bytes of data to a serial bit stream. The AT controller also generates a preamble field, inserts an address mark, and transmits the data to the ENDEC in the R/W IC where the data is encoded into the 32/34 GCR format and pre-compensates for non-linear transition shift. The amount of write current is set by the SID2001 DSP and Interface/Disk Controller through the serial interface to the preamp.

The SID2001 switches the Preamplifier and Write Driver IC to write mode and selects a head. Once the Preamplifier and Write Driver IC receives a write gate signal, it transmits current reversals to the head, which writes magnetic transitions on the disk

5.5 Firmware Features

This section describes the following firmware features:

- Read Caching
- Write Caching
- Track Skewing
- Defect Management
- Automatic Defect Allocation
- Ten way burst ECC Correction
- SMART (Self-monitoring and reporting technology)
- Dynamic Anti-stiction Algorithm

5.5.1 Read Caching

SpinPoint V40 hard disk drives use a 512KB Read Cache to enhance drive performance and significantly improve system throughput. Use the SET FEATURES command to enable or disable Read Caching. Read caching anticipates host-system requests for data and stores that data for faster future access. When the host requests a certain segment of data, the cache feature utilizes a prefetch strategy to get the data in advance and automatically read and store the following data from the disk into fast RAM. If the host requests this data, the RAM is accessed rather than the disk.

There is a high probability that subsequent data requested will be in the cache, because more than 50 percent of all disk requests are sequential. It takes microseconds rather than milliseconds to retrieve this cached data.

Thus Read Caching can provide substantial time savings during at least half of all disk requests. For example, Read Caching could save most of the disk transaction time by eliminating the seek and rotational latency delays that prominently dominate the typical disk transaction.

Read Caching operates by continuing to fill its cache memory with adjacent data after transferring data requested by the host. Unlike a non-caching controller, The SID2001 Interface Controller continues a read operation after the requested data has been transferred to the host system. This read operation terminates after a programmed amount of subsequent data has been read into the cache memory.

The cache memory consists of a 512KB sync DRAM buffer allocated to hold the data. It can be directly accessed by the host by means of read and write commands. The unit of data stored is the logical block, or a multiple of the 512-byte sector. Therefore, all accesses to cache memory must be in multiples of the sector size. The following commands empty the cache:

- IDENTIFY DRIVE (ECh)
- FORMAT TRACK (50h)
- EXECUTE DRIVE DIAGNOSTIC (90h)
- READ LONG (23h)
- WRITE VERIFY (3Ch)
- INITIALIZE DEVICE PARAMETER (91h)
- SLEEP (99h, E6h)
- STANDBY IMMEDIATELY (94h,E0h)
- READ BUFFER (E4h)
- WRITE BUFFER (E8h)
- WRITE SAME (E9h)

5.5.2 Write Caching

Write caching improves both single and multi-sector write performance by reducing delays introduced by rotational latency. When the drive writes a pattern of multiple sequential data, it stores the data to a cache buffer and immediately sends a COMMAND COMPLETE message to the host before it writes the data to the disk.

The data is then written collectively to the drive thereby minimizing the disk seeking operation. Data is held in cache no longer than the maximum seek time plus rotational latency. Host retries must be enabled for Write Caching to be active.

If the data request is random, the data of the previous command is written to the disk before COMMAND COMPLETE is posted for the current command. Read commands work similarly. The previous write is allowed to finish before the read operation starts.

If a defective sector is found during a write, the sector is automatically relocated before the write occurs. This ensures that cached data that already has been reported as written successfully gets written, even if an error should occur.

If the sector is not automatically relocated, the drive drops out of write caching and reports the error as an ID Not Found. If the write command is still active on the AT interface, the error is reported during that command. Otherwise, it is reported on the next command.

5.5.3 Defect Management

The SpinPoint V40 media is scanned for defects. After defect scanning, the defective sectors are saved in the defect list. A defect encountered in the manufacturing process is slipped to the next physical sector location. All logical sector numbers are pushed down to maintain a sequential order of data. The read/write operation can "slip" over the defective sectors so that the only performance impact is idle time.

5.5.4 Automatic Defect Allocation

The automatic defect allocation feature automatically maps out defective sectors encountered during read sector or write sector operations. These types of defective sectors are typically caused by grown defects. During write operations, if write errors are encountered, all sectors within the target servo frame are mapped out. Original data is transferred and written into designated reserved sector areas determined by the HDD firmware.

5.5.5 Multi-burst ECC Correction

The drive uses a Reed-Solomon code to perform error detection and correction. For each 512 byte block, the software error correction polynomial is capable of correcting:

- One 233-bit burst error
- Ten 3-bytes burst error
- Up to 60 bytes with reassure pointer (off-line correction)

These errors are corrected on the fly with no performance degradation.

5.5.6 SMART

The intent of Self-monitoring, Analysis and Reporting Technology (SMART) is to protect user data and to minimize the likelihood of unscheduled system downtime that may be caused by unpredictable degradation and/or device fault. By monitoring and storing critical performance and calibration parameters, SMART devices attempt to predict the likelihood of near-term degradation or fault condition. Providing the host system knowledge of a negative reliability condition allows the host system to warn the user of the impending risk of a data loss and advise the user of appropriate action.

5.5.7 AAM

The Automatic Acoustic Management (AAM) feature allows the SpinPoint V40 to operate in one of several acoustic noise levels. This provides the user with the option of selecting the desired level of sound noise emanating from the HDD. Low noise operating levels are achieved with some small degree of performance degradation. With this feature disabled, the HDD operates with maximum performance and maximum acoustic noise level. This feature is enabled by the Set Features command.

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CHAPTER 6 AT INTERFACE AND ATA COMMANDS

6.1 Introduction

A Samsung disk drive with an Embedded AT Interface fully supports and enhances PC mass storage requirements. The Samsung AT interface conforms to the ATA/ATAPI-6 standards in Cabling, in Physical Signals, and in Logical Programming schemes. The Samsung Embedded AT controller joins the industry premiere VLSI circuitry with ingenious programming skill that does not compromise performance or reliability. Samsung integrates and delivers the cutting edge in technology. Samsung AT class disk drives are designed to relieve and to enhance the I/O request processing function of system drivers.

6.2 Physical Interface

6.2.1 Signal Conventions

Signal names are shown in all upper case letters. Signals can be asserted (active, true) for either a high (more positive voltage) or low (less positive voltage) state. A dash character (-) at the beginning or end of a signal name indicates that it is asserted at the low level (active low). No dash or a plus character (+) at the beginning or end of a signal name indicates it is asserted high (active high). An asserted signal may be driven high or low by an active circuit, or it may be pulled to the correct state by the bias circuitry.

Control signals that are asserted for one function when high and asserted for another function when low are named with the asserted high function name followed by a slash character (/). The asserted low function name is followed with a dash (-) (e.g., BITENA/BITCLR- enables a bit when high and clears a bit when low). All signals are TTL compatible unless otherwise noted. Negated means that the signal is driven by an active circuit to the state opposite to the asserted state (inactive or false) or may be simply released (in which case the bias circuitry pulls it inactive or false), at the option of the implementer.

6.2.2 Signal Summary

The physical interface consists of single-ended TTL compatible receivers and drivers communicating through a 40/80-conductor flat ribbon non-shielded cable using an asynchronous interface protocol. The pin numbers and signal names are shown in Table 6-1. Reserved signals are left unconnected.

6.2.3 Signal Descriptions

The interface signals and pins are described below and listed in Table 6-1. The signals are listed according to function, rather than in numerical connector pin order.

6.2.3.1 CS1FX- (Drive Chip Select 0)

This is the chip select signal decoded from the host address bus used to select the Command Block registers.

6.2.3.2 CS3FX- (Drive Chip Select 1)

This is the chip select signal decoded from the host address bus used to select the Control Block registers.

6.2.3.3 DA0-2 (Drive Address Bus)

This is the 3-bit binary coded address asserted by the host to access a register or data port in the drive.

6.2.3.4 DASP- (Drive Active/Slave Present)

This is a time-multiplexed signal that indicates that a drive is active, or that Drive 1 is present. This signal is an open collector output, and each drive has a 10K ohm pull-up resistor on this signal.

During power-on initialization or after RESET- is negated, DASP- is asserted by Drive 1 within 400 msec to indicate that Drive 1 is present. Drive 0 allows up to 450 msec for Drive 1 to assert DASP-. If Drive 1 is not present, Drive 0 may assert DASP- to drive an activity LED. DASP- is negated following acceptance of the first valid command by Drive 1 or after 31 seconds, whichever comes first. Any time after negation of DASP-, either drive may assert DASP- to indicate that a drive is active.

6.2.3.5 DD0-DD15 (Drive Data Bus)

This is an 8- or 16-bit bi-directional data bus between the host and the drive. The lower 8 bits are used for 8-bit transfers (e.g., registers, ECC bytes).

6.2.3.6 DIOR- (Drive I/O Read)

This is the Read strobe signal. The falling edge of DIOR- enables data from a register or the data port of the drive onto the host data bus, DD0-DD7 or DD0-DD15. The rising edge of DIOR- latches data at the host.

6.2.3.7 DIOW- (Drive I/O Write)

This is the Write strobe signal. The rising edge of DIOW- clocks data from the host data bus, DD0-DD7 or DD0- DD15, into a register or the data port of the drive.

6.2.3.8 DMACK- (DMA Acknowledge)

This signal shall be used by the host in response to DMARQ to either acknowledge that data has been accepted, or that data is available.

6.2.3.9 DMARQ (DMA Request)

This signal, used for DMA data transfers between host and drive, shall be asserted by the drive when it is ready to transfer data to or from the host. The direction of data transfer is controlled by DIOR- and DIOW-. The signal is used in handshake manner with DMACK- (i.e., the drive shall wait until the host asserts DMACK- before negating DMARQ and re-asserting DMARQ if there is more data to transfer).

When a DMA operation is enabled, IOCS16- and CSIFX- shall not be asserted and transfers shall be 16-bits wide.

6.2.3.10 INTRQ (Drive Interrupt)

This signal is used to interrupt the host system. INTRQ is asserted only when the drive has a pending interrupt, the drive is selected, and the host has cleared nIEN in the Device Control register. If nIEN=1, or the drive is not selected, this output is in a high impedance state, regardless of the presence or absence of a pending interrupt.

INTRQ is negated by:

- Assertion of RESET- or
- The setting of SRST of the Device Control register, or
- The host writing to the Command register, or
- The host reading from the Status register.

On PIO transfers, INTRQ is asserted at the beginning of each data block to be transferred. A data block is typically a single sector, except when declared otherwise by use of the Set Multiple command. An exception occurs on Format Track, Write Sector(s), Write Buffer, and Write Long commands: INTRQ shall not be asserted at the beginning of the first data block to be transferred.

6.2.3.11 IOCS16- (Drive 16-bit I/O)

IOCS16- indicates to the host system that the 16-bit data port has been addressed and that the drive is ready to send or receive a 16-bit word. This is an open collector output.

- When transferring in PIO mode, if IOCS16- is not asserted, DD0-7 is used for 8-bit transfers.
- When transferring in PIO mode, if IOCS16- is asserted, DD0-15 is used for 16-bit data transfers.

6.2.3.12 IORDY (I/O Channel Ready)

This signal is active low to extend the host transfer cycle of any host register access (Read or Write) when the drive is not ready to respond to a data transfer request. When IORDY is not negated, this signal is in the high impedance state.

6.2.3.13 PDIAG- (Passed Diagnostics)

This signal is asserted by Drive 1 to indicate to Drive 0 that it has completed diagnostics. A 10K pull-up resistor is used on this signal by each drive.

Following a power-on reset, software reset, or RESET-, Drive 1 negates PDIAG- within 1 msec (to indicate to Drive 0 that it is busy). Drive 1 then asserts PDIAG- within 30 seconds to indicate that it is no longer busy and is able to provide status. After the assertion of PDIAG-, Drive 1 will be unable to accept commands until it has finished its reset procedure and is Ready (DRDY=1).

Following the receipt of a valid Execute Drive Diagnostics command, Drive 1 negates PDIAG- within 1 msec to indicate to Drive 0 that it is busy and has not yet passed its drive diagnostics. If Drive 1 is present, then Drive 0 waits for up to 5 seconds from the receipt of a valid Execute Drive Diagnostics command for Drive 1 to assert PDIAG-. Drive 1 clears BSY before asserting PDIAG-, as PDIAG- is used to indicate that Drive 1 has passed its diagnostics and is ready to post status.

If DASP- was not asserted by Drive 1 during reset initialization, Drive 0 posts its own status immediately after it completes diagnostics, and clears the Drive 1 Status register to 00h. Drive 0 will be unable to accept commands until it has finished its reset procedure and is Ready (DRDY=1).

6.2.3.14 RESET- (Drive Reset)

This signal is asserted from the host system to reset the drive. It shall be asserted for at least 25 μsec after voltage levels have stabilized during power-on; it is negated thereafter unless some event requires that the drive(s) be reset following power-on.

Table 6-1 shows the correlation between the signals at the ATA interface and the host AT bus.

Table 6-1 AT-Bus Interface Signals

Drive Connector		Direction	AT System BUS
Signal Name	**Pin No.**		
RESET-	1	←—	RESET DRV
Ground	2	——	Ground
DB7	3	←→	SD7
DB8	4	←→	SD8
DB6	5	←→	SD6
DB9	6	←→	SD9
DB5	7	←→	SD5
DB10	8	←→	SD10
DB4	9	←→	SD4
DB11	10	←→	SD11
DB3	11	←→	SD3
DB12	12	←→	SD12
DB2	13	←→	SD2
DB13	14	←→	SD13
DB1	15	←→	SD1
DB14	16	←→	SD14
DB0	17	←→	SD0
DB15	18	←→	SD15
Ground	19	——	Ground
Keypin	20		No Connection

Table 6-1 AT-Bus Interface Signals (continued)

Drive Connector		Direction	AT System BUS
Signal Name	**Pin No.**		
DMARQ	21	⟶	DMARQ
Ground	22	——	Ground
IOW-	23	⟵	IOW-
Ground	23	——	Ground
IOR-	25	⟵	IOR-
Ground	26	——	Ground
IORDY	27	⟶	IORDY
Reserved	28		No Connection
DMACK-	29	⟵	DMACK-
Ground	30	——	Ground
INTRQ	31	⟶	INTRQ
IOCS16-	32	⟶	IOCS16-
ADDR1	33	⟵	SA1
PDIAG- / CBLID-	34	*——*	PDIAG-
ADDR0	35	⟵	SA0
ADDR2	36	⟵	SA2
CS1FX-	37	⟵	CS0-
CS3FX-	38	⟵	CS1-
DASP-	39	*⟶	DASP-
Ground	40	——	Ground

* Drive Intercommunication Signals

Drive 1		Drive 0			Host
34	— PDIAG →	34	34	——	34
39	— DASP- →	39	39	⟶	39

Table 6-2 lists the signal name mnemonic, connector pin number, whether input to (I) or output from (O) the drive, and the full signal name.

Table 6-2 Interface Signals Description

Signal	Pin	DIR	Description
CS1FX-	37	I	Drive chip Select 0
CS3FX-	38	I	Drive chip Select 1
DA0	35	I	Drive Address Bus - Bit 0
DA1	33	I	- Bit 1
DA2	36	I	- Bit 2
DASP-	39	I/O	Drive Active/Slave Present
DD0	17	I/O	Drive Data Bus - Bit 0
DD1	15	I/O	- Bit 1
DD2	13	I/O	- Bit 2
DD3	11	I/O	- Bit 3
DD4	9	I/O	- Bit 4
DD5	7	I/O	- Bit 5
DD6	5	I/O	- Bit 6
DD7	3	I/O	- Bit 7
DD8	4	I/O	- Bit 8
DD9	6	I/O	- Bit 9
DD10	8	I/O	- Bit 10
DD11	10	I/O	- Bit 11
DD12	12	I/O	- Bit 12
DD13	14	I/O	- Bit 13
DD14	16	I/O	- Bit 14
DD15	18	I/O	- Bit 15
DIOR-	25	I	Drive I/O Read
DIOW-	23	I	Drive I/O Write
DMACK-	29	I	DMA Acknowledge
DMARQ	21	O	DMA Request
INTRQ	31	O	Drive Interrupt
IOCS16-	32	O	Drive 16-bit I/O
IORDY	27	O	I/O Channel Ready
PDIAG-	34	I/O	Passed Diagnostics
RESET-	1	I	Drive Reset
Key pin	20	—	Pin used for keying the interface connector

NOTE: A minus sign follows the name of any signal that is asserted as active low.
Direction (DIR) is in reference to the drive:
IN indicates input to the drive.
OUT indicates output from the drive.
I/O indicates that the signal is bi-directional.

6.3 Logical Interface

6.3.1 General

6.3.1.1 Bit Conventions

Bit names are shown in all upper case letters except where a lower case n precedes a bit name. This indicates that when nBIT=0 (bit is zero) the action is true, and when nBIT=1 (bit is one) the action is false. If there is no proceeding n, then when BIT=1 it is true, and when BIT=0 it is false.

A bit can be set to one or cleared to zero, and polarity influences whether it is to be interpreted as true or false:

True	BIT=1	nBIT=0
False	BIT=0	nBIT=1

6.3.1.2 Environment

Data is transferred in parallel (16 bits) either to or from host memory to the device's buffer under the direction of commands previously transferred from the host. The device performs all of the operations necessary to properly write data to, or read data from, the media. Data read from the media is stored in the device's buffer pending transfer to the host memory, and data is transferred from the host memory to the device's buffer to be written to the media.

The devices using this interface shall be programmed by the host computer to perform commands and return status to the host at command completion. When two devices are daisy chained on the interface, commands are written in parallel to both devices, and for all except the Execute Diagnostics command, only the selected device executes the command. On an Execute Diagnostics command addressed to Device 0, both devices shall execute the command, and Device 1 shall post its status to Device 0 via PDIAG-.

Drives are selected by the DEV bit in the Drive/Head register (see 6.3.4.9), and by a jumper or switch on the device designating it as either Device 0 or Device 1. When DEV=0, Device 0 is selected. When DEV=1, Device 1 is selected. When a single device is attached to the interface, it shall be set as Device 0.

Throughout this document, device selection always refers to the state of the DEV bit, the position of the Device 0/Device 1 jumper or switch, or use of the CSEL pin.

A device can operate in either of two addressing modes, CHS or LBA, on a command-by-command basis. A device, which can support LBA mode, is indicated in the register, Sector Number register, Cylinder Low mode in the Device/Head register, Sector Number register, Cylinder Low register, Cylinder High register and HS3-HS0 of the Device/Head register contains the zero based-LBA.

This term defines the addressing mode of the device as being by physical sector address. The physical sector address is made up of three fields: the sector number, the head number and the cylinder number. Sectors are numbered from 1 to a device specific maximum value, which cannot exceed 255. Heads are numbered from 0 to a device specific maximum value, which cannot exceed 15. Cylinders are numbered from 0 to a device specific maximum value, which cannot exceed 65,535. Typically, sequential access to the media is accomplished by treating the sector number as the least significant portion, the head number as the mid portion, and the cylinder number as the most significant portion of the CHS address.

In LBA mode the sectors on the device are assumed to be linearly mapped with an initial definition of: LBA 0 = (Cylinder 0, head 0, sector 1). Irrespective of translate mode geometry set by the host, the LBA address of a given sector does not change:

LBA = [(cylinder * heads_per_cylinder + heads) * sectors_per_track] + sector - 1

6.3.2 I/O Register - Address

Communication to or from the drive is through an I/O register that routes the input or output data to or from registers addressed by a code on signals from the host (CS1FX-, CS3FX-, DA2, DA1, DA0, DIOR- and DIOW-).

The Command Block registers are used for sending commands to the drive or posting status from the drive.

The Control Block registers are used for drive control and to post-alternate status. Table 6-3 lists these registers and the addresses that select them.

Table 6-3 I/O Port Function/Selection Address

Address					Functions	
CS1FX-	**CS3FX-**	**DA2**	**DA1**	**DA0**	**READ(DIOR-)**	**WRITE(DIOW-)**
Control Block Registers						
N	N	X	X	X	High Impedance	Not Used
N	A	0	X	X	High Impedance	Not Used
N	A	1	0	X	High Impedance	Not Used
N	A	1	1	0	Alternate Status	Device Control
N	A	1	1	1	Device Address	Not Used
Command Block Registers						
A	N	0	0	0	Data	Data
A	N	0	0	1	Error Register	Features
A	N	0	1	0	Sector Count	Sector Count
A	N	0	1	1	Sector Number	Sector Number
A	N	0	1	1	* LBA bits 0-7	* LBA bits 0-7
A	N	1	0	0	Cylinder Low	Cylinder Low
A	N	1	0	0	* LBA bits 8-15	* LBA bits 8-15
A	N	1	0	1	Cylinder High	Cylinder High
A	N	1	0	1	* LBA bits 16-23	* LBA bits 16-23
A	N	1	1	0	Drive/Head	Drive/Head
A	N	1	1	0	* LBA bits 24-27	* LBA bits 24-27
A	N	1	1	1	Status	Command
N	N	X	X	X	Invalid Address	Invalid Address

* Mapping of registers in LBA mode.
Logic conventions are:
A = signal asserted
N = signal negated
X = don't care

6.3.3 Control Block Register Descriptions

6.3.3.1 Alternate Status Register (3F6h)

This register contains the same information as the Status register in the Command Block register. The only difference is that reading this register does not imply interrupt acknowledgment nor does it clear a pending interrupt.

7	6	5	4	3	2	1	0
BSY	DRDY	DWF	BSY	DRQ	CORR	IDX	ERR

NOTE: See section 6.3.4.10 for definitions of the bits in this register.

6.3.3.2 Drive Address Register (3F7h)

This register contains the inverted drive select and head select addresses of the currently selected drive. The bits in this register are as follows:

7	6	5	4	3	2	1	0
HiZ	nWTG	nHS3	nHS2	nHS1	nHS0	nDS1	nDS0

- **HiZ** is always in a high impedance state.
- **nWTG** is the Write Gate bit. When writing to the disk drive is in progress, nWTG=0.
- **nHS3 through nHS0** are the one's complement of the binary coded address of the currently selected head. For example, if nHS3 through nHS0 are 1100b, respectively, then head 3 is selected. nHS3 is the most significant bit.
- **nDS1** is the drive select bit for drive 1. When drive 1 is selected and active, nDS1=0.
- **nDS0** is the drive select bit for drive 0. When drive 0 is selected and active, nDS0=0.

NOTE: Caching, translation and master/slave may cause this register to contain invalid data.

6.3.3.3 Device Control Register (3F6h)

The bits in this register are as follows:

7	6	5	4	3	2	1	0
X	X	X	X	1	SRST	nIEN	0

- **SRST** is the host software reset bit. The drive is held reset when this bit is set. If two disk drives are daisy chained on the interface, this bit resets both simultaneously.
- **nIEN** is the enable bit for the drive interrupt to the host. When nIEN=0, and the drive is selected, INTRQ is enabled through a tri-state buffer. When nIEN=1, or the drive is not selected, the INTRQ signal is in a high impedance state.

6.3.4 Command Block Register Descriptions

6.3.4.1 Data Register (1F0h)

This 16-bit register is used to transfer data blocks between the device data buffer and the host. It is also the register through which sector information is transferred on a Format Track command. Data transfers may be either PIO or DMA.

6.3.4.2 Features Register (1F1h)

This register is command specific and used to enable and disable features of the interface (e.g., by the Set Features command to enable and disable caching).

6.3.4.3 Sector Number Register (1F3h)

In **CHS** mode this register contains the starting sector number for any disk data access for the subsequent command. The sector number is from 1 to the maximum number of sectors per track. In **LBA** mode this register contains bits 0-7 of the LBA.
See the command descriptions for the contents of the register at command completion (whether successful or unsuccessful).

6.3.4.4 Error Register (1F1h)

This register contains status from the last command executed by the drive or a Diagnostic Code.
At the completion of any command except Execute Drive Diagnostic, the contents of this register are valid when ERR=1 in the Status register.

Following a power-on, a reset, or completion of an Execute Drive Diagnostic command, this register contains a Diagnostic Code (see Table 6-4).

7	6	5	4	3	2	1	0
ICRCE	UNC	0	IDNF	0	ABRT	TK0NF	AMNF

- **ICRCE (Interface CRC Error)** indicates a CRC error has occurred on the data bus during a Ultra-DMA transfer.
- **UNC (Uncorrectable Data Error)** indicates an uncorrectable data error has been encountered.
- **IDNF (ID Not Found)** indicates the requested sector's ID field could not be found.
- **ABRT (Aborted Command)** indicates the requested command has been aborted due to a drive status error (Not Ready, Write Fault, etc.) or because the command code is invalid.
- **K0NF (Track 0 Not Found)** indicates track 0 has not been found during a Recalibrate command.
- **AMNF (Address Mark Not Found)** indicates the data address mark has not been found after finding the correct ID field.

NOTE: Unused bits are cleared to zero.

6.3.4.5 Sector Count Register (1F2h)

This register contains the number of sectors of data requested to be transferred on a read or write operation between the host and the drive. If the value in this register is zero, a count of 256 sectors is specified.

If this register is zero at command completion, the command was successful. If not successfully completed, the register contains the number of sectors, which need to be transferred in order to complete the request.

The contents of this register may be defined otherwise on some commands (e.g., Initialize Drive Parameters command, Format Track command).

6.3.4.6 Cylinder High Register (1F5h)

In **CHS** mode this register contains the high order bits of the starting cylinder address for any disk access. In **LBA** mode this register contains bits 16-23 of the LBA.

At the end of the command, this register is updated to reflect the current disk address. The most significant bits of the cylinder address are loaded into the Cylinder High register.

6.3.4.7 Cylinder Low Register (1F4h)

In **CHS** mode this register contains the low order 8 bits of the starting cylinder address for any disk access. In **LBA** mode this register contains bits 8-15 of the LBA. At the end of the command, this register is updated to reflect the current disk address.

6.3.4.8 Command Register (1F7h)

This register contains the command code being sent to the drive. Command execution begins immediately after this register is written. The executable commands, the command codes, and the necessary parameters for each command are listed in Table 6-4.

6.3.4.9 Drive/Head Register (1F6h)

This register contains the drive and head numbers. When executing an Initialize Drive Parameters command, the content of this register defines the number of heads minus 1.

7	6	5	4	3	2	1	0
1	LBA	1	DEV	HS3	HS2	HS1	HS0

- **DRV** is the binary encoded drive select number. When DEV=0, Device 0 is selected. When DEV=1, Device 1 is selected.
- **HS3 through HS0** contain the binary coded address of the head to be selected in **CHS** mode (e.g., if HS3 through HS0 are 0011b, respectively, then head 3 will be selected). HS3 is the most significant bit. In **LBA** mode this register contains bits 24-27 of the LBA. At command completion, this register is updated to reflect the currently selected disk address.
- **LBA** is the binary coded address mode select. When L=0, disk addressing is by **CHS** mode. When L=1, disk addressing is by **LBA** mode. This bit was set to zero when the ATA drive didn't support LBA mode

6.3.4.10 Status Register (1F7h)

This register contains the drive status. The contents of this register are updated at the completion of each command. When BSY is cleared, the other bits in this register are valid within 400 nsec. If BSY=1, no other bits in this register are valid. If the host reads this register when an interrupt is pending, it is considered to be the interrupt acknowledge. Any pending interrupt is cleared whenever this register is read.

NOTE: If Drive 1 is not detected as present, Drive 0 clears the Drive 1 Status register to 00h (indicating that the drive is Not Ready).

7	6	5	4	3	2	1	0
BSY	DRDY	DWF	DSC	DRQ	CORR	IDX	ERR

- **BSY (Busy)** is set whenever the drive has access to the Command Block registers. The host should not access the Command Block registers when BSY=1. When BSY=1, a read of any Command Block register returns the contents of the Status register. This bit is set by the drive under the following circumstances:

  a) Within 400 nsec after the negation of RESET- or after SRST has been set in the Device Control register.

  b) Within 400 nsec of a host write of the Command register with a Read, Read Long, Read Buffer, Seek, Recalibrate, Initialize Drive Parameters, Read Verify, Identify Drive, or Execute Drive Diagnostic command.

  c) Within 5 µsec following transfer of 512 bytes of data during execution of a Write, Format Track, or Write Buffer command, or 512 bytes of data and the appropriate number of ECC bytes during the execution of a Write Long command.

- **DRDY (Drive Ready)** indicates that the drive is capable of responding to a command. When there is an error, this bit does not change until the host reads the Status register. Then the bit again indicates the current readiness of the drive. This bit clears at power-on and remains clear until the drive is ready to accept a command.
- **DWF (Drive Write Fault)** indicates the current write fault status. When an error occurs, this bit is not changed until the Status register is read by the host, at which time the bit again indicates the current write fault status.
- **DSC (Drive Seek Complete)** indicates that the drive heads have settled over a track. When an error occurs, this bit is not changed until the Status register is read by the host, at which time the bit again indicates the current Seek Complete status.
- **DRQ (Data Request)** indicates that the drive is ready to transfer a word or byte of data between the host and the drive.
- **CORR (Corrected Data)** indicates that a correctable data error was encountered and the data has been corrected. This condition does not terminate a data transfer.
- **IDX (Index)** is set once per disk revolution.
- **ERR (Error)** indicates that an error occurred during execution of the previous command. The bits in the Error register have additional information regarding the cause of the error.

6.4 At Command Register Descriptions

Commands are issued to the drive by loading the pertinent registers in the command block with the needed parameters, and then writing the command code to the Command register. The manner in which a command is accepted varies. There are three classes of command acceptance (see Table 6-4), all based on the fact that to receive a command, BSY=0:

- Upon receipt of a Class 1 command, the drive sets BSY within 400 nsec.
- Upon receipt of a Class 2 command, the drive sets BSY within 400 nsec, sets up the sector buffer for a write operation, sets DRQ within 700 µsec, and clears BSY within 400 nsec of setting DRQ.
- Upon receipt of a Class 3 command, the drive sets BSY within 400 nsec, sets up the sector buffer for a write operation, sets DRQ within 20 msec, and clears BSY within 400 nsec of setting DRQ.

NOTE: DRQ may be set so quickly on Class 2 and Class 3 that the BSY transition is too short for BSY=1 to be recognized.

If a new command is issued to a drive which has an uncompleted command (subsequently referred to as Old_Command) in progress, the drive immediately responds to the new command (subsequently referred to as New_Command), even if execution of the Old_Command could have been completed.

Table 6-4 Command Codes and Parameters

COMMAND			PARAMETER USED				
Class	DESCRIPTION	CODE	FR	SC	SN	CY	DH
1	Check Power Mode	98h, E5h		y			D
2	Download Micro code	92h					D
1	Execute Device Diagnostic	90h					D*
1	Flush Cache	E7h					D
2	Format Track	50h					d
1	Identify Device	ECh					D
1	Idle	97h, E3h		y			D
1	Idle Immediate	95h, E1h					D
1	Initialize Drive Parameter	91h		y			y
1	Read Buffer	E4h					D
1	Read DMA (w/retry)	C8h		y	y	y	y
1	Read DMA (w/o retry)	C9h		y	y	y	y
1	Read Long (w/retry)	22h		y	y	y	y
1	Read Long (w/o retry)	23h		y	y	y	y
1	Read Multiple	C4h		y	y	y	y
1	Read Native Max Address	F8h					D
1	Read Sector(s) (w/retry)	20h		y	y	y	y
1	Read Sector(s) (w/o retry)	21h		y	y	y	y
1	Read Verify Sector(s) (w/retry)	40h		y	y	y	y
1	Read Verify Sector(s) (w/o retry)	41h		y	y	y	y
1	Recalibrate	1xh					D
1	Seek	7xh			y	y	y
1	Set Features	EFh	y				D
1	Set Max Address	F9h			y	y	y
1	Set Multiple Mode	C6h		y			D
1	Sleep Mode	99h, E6h					D
1	Smart	B0h	y	*1	y	y	D
1	Standby	96h, E2h		y			D
1	Standby Immediate	94h, E0h					D
2	Write Buffer	E8h					D
3	Write DMA (w/retry)	CAh		y	y	y	y
3	Write DMA (w/o retry)	CBh		y	y	y	y
2	Write Long (w/retry)	32h	*2	y	y	y	y
2	Write Long (w/o retry)	33h	*2	y	y	y	y
3	Write Multiple	C5h	*2	y	y	y	y
2	Write Sector(s) (w/retry)	30h	*2	y	y	y	y
2	Write Sector(s) (w/o retry)	31h	*2	y	y	y	y

Legend:

CY = Cylinder register
DH = Device/Head register
FR = Feature register
SC = Sector Count register
SN = Sector Number register

Legend (continued)

y The register contains a valid parameter for this command. For the Device/Head register, y means both the device and head parameters are used.

D Only the drive parameter is valid and not the head parameter.

d The device parametric is valid; the usage of the head parameter is vendor-specific.

D* Address to Device 0, but both devices execute it.

*1 Smart Enable/Disable Auto-save

*2. Maintained for compatibility

6.4.1 Check Power Mode (98h, E5h)

This command checks the power mode.

If the drive is in, going to, or recovering from the Standby Mode, the drive sets BSY, sets the Sector Count register to 00h, clears BSY, and generates an interrupt.

If the drive is in the Idle Mode, the drive sets BSY, sets the Sector Count register to FFh, clears BSY, and generates an interrupt.

6.4.2 Download Micro Code (92h)

This command enables the host to alter the drive's Micro-code. The data transferred using this command is vendor specific.

6.4.3 Execute Device Diagnostics (90h)

This command performs the internal diagnostic tests implemented by the drive. The DRV bit is ignored. Both drives, if present, shall execute this command.

If Drive 1 is present:

- Drive 1 asserts PDIAG- within 5 seconds.
- Drive 0 waits up to 6 seconds for Drive 1 to assert PDIAG-.
- If Drive 1 has not asserted PDIAG-, indicating a failure, Drive 0 appends 80h to its own diagnostic status.
- Both drives execute diagnostics.
- If a Drive 1 diagnostic failure is detected when Drive 0 status is read, then Drive 1 status is obtained by setting the DRV bit, and reading status.

If there is no Drive 1 present:

- Drive 0 posts only its own diagnostic results.
- Drive 0 clears BSY, and generates an interrupt.

The Diagnostic Code written to the Error register is a unique 8-bit code (shown in Table 6-5), not as the single bit flags defined in 6.3.4.4.

If Drive 1 fails diagnostics, Drive 0 "ORs" 80h with its own status and loads that code into the Error register. If Drive 1 passes diagnostics or there is no Drive 1 connected, Drive 0 "ORs" 00h with its own status and loads that code into the Error register.

Table 6-5 Diagnostic Codes

Code	Description
01h	No error detected
02h	Formatter device error
03h	Sector buffer error
04h	ECC circuitry error
05h	Controlling microprocessor error
8xh	Drive 1 failed

6.4.4 Flush Cache (E7h)

This command is used by the host to request the drive to flush the write cache. If write is to be flushed, all data cached will be written to the media. The BSY bit will remain set to one until all data has been successfully written or error occurs.

6.4.5 Format Track (50h)

The track address is specified in the Cylinder High and Cylinder Low registers, and the number of sectors is specified in the Sector Count register. When the command is accepted, the drive sets the DRQ bit and waits for the host to fill the sector buffer. When the sector buffer is filled, the drive clears DRQ, sets BSY, and begins command execution. SpinPoint V40 hard disk drives write zeros to the data fields in the sectors on the specified logical track. The ID fields are not written by this command.
In LBA mode, this command formats a single logical track including the specified LBA.

6.4.6 Identify Device (ECh)

The Identify Device command enables the host to receive parameter information from the device. When the command is issued, the device sets the BSY bit, prepares to transfer the 256 words of device identification data to the host, sets the DRQ bit, clears the BSY bit, and generates an interrupt. The host can then transfer the data by reading the Data register. The parameter words in the buffer have the arrangement and meanings defined in Table 6-6. All reserved bits or words shall be zero.

The F/V column indicates if the word or part of a word had fixed (F) contents that do not change, variable (V) contents that may change depending on the device state or the commands executed by the device, X for words with vendor specific data which may be fixed or variable, and R for reserved words which shall be zero. For removable media devices, the value of fields indicated as fixed (F) may change when media is removed or changed.

Some parameters are defined as a group of bits. A word which is defined as a set of bits is transmitted with the indicated bits on the respective data bus bit (e.g., bit 15 appears on DD15).

Some parameters are defined as a sixteen-bit value. A word which is defined as a sixteen bit value places the most significant bit of the value on bit DD15 and the least significant bit on bit DD0.
Some parameters are defined as a 32-bit value (e.g., words 57 and 58). Such fields are transferred using two word transfers. The device first transfers the least significant bits, bits 15 through 0 of the value, on bits DD15 through DD0 respectively. After the least significant bits have been transferred, the most significant bits, bits 31 through 16 of the value, are transferred on DD15 through DD0 respectively.

Some parameters are defined as a string of ASCII characters. For the string "Copyright," the character 'C' is the first byte, '0' is the 2nd byte, etc. When such fields are transferred, the order of transmission is:

- 1st character ('C') is on bits DD15 through DD8 of the first word
- 2nd character ('o') is on bits DD7 through DD0 of the first word
- 3rd character ('p') is on bits DD15 through DD8 of the second word
- 4th character ('y') is on bits DD7 through DD0 of the second word, etc.

Table 6-6 IDENTIFY DEVICE information

Word	Content	Description
0	045Ah	General configuration bit-significant information: 15 0=ATA device, set to 0 14-8 Retired 7 1=removable media device, set to 0 6 1=not removable controller and/or device, set to 1 5-3 Retired 2 Reserved 1 Retired 0 Reserved
1	XXXXh	Number of logical cylinders
2	0	Reserved
3	00XXh	Number of logical heads
4-5	0	Retired
6	003Fh	Number of logical sectors per logical track
7-9	0	Retired
10-19	XXXX	Serial number (20 ASCII characters, 0 = not specified)
20	0003h	Controller type(0003h): Dual ported, multiple sector buffer with look-ahead cache
21	03B0h	Buffer size in 512-byte increments (3B0h => 944 => 472KB)
22	0004h	Number of ECC bytes (Device Native length is selected via set feature command.)
23-26	XXXX	Firmware revision (8 ASCII characters)
27-46	XXXX	Model number (40 ASCII characters)
47	8010h	15-8 80h 7-0 Maximum number of sectors that shall be transferred per interrupt on READ/WRITE MULTIPLE commands
48	0000h	Reserved

(continued)

Table 6-6 IDENTIFY DEVICE information *(continued)*

Word	Content	Description
49	0B00h	Capabilities 15-14 Reserved 13 1=Standby timer values as specified in this standard are supported 0=Standby timer values shall be managed by the device 12 Reserved 11 1=IORDY supported 0=IORDY may be supported 10 1=IORDY may be disabled 9 Shall be set to one. 8 Shall be set to one. 7-0 Retired
50	0000h	Reserved
51	0200h	PIO data transfer cycle timing mode
52	0200h	DMA data transfer cycle timing mode
53	0007h	15-3 Reserved 2 1=the fields reported in word 88 are valid 1 1=the fields reported in words 64-70 are valid 0 1=the fields reported in words 54-58 are valid
54	XXXXh	Number of current logical cylinders
55	XXXXh	Number of current logical heads
56	XXXXh	Number of current logical sectors per track
57-58	XXXXh	Current capacity in sectors Word 57 specifies the low world of the capacity
59	0XXXh	Current Multiple setting. Bit assignments 15-9 Reserved 8 1=Multiple sector setting is valid 7-0 xxh=Current setting for number of sectors
60-61	XXXXh	Total number of user addressable sectors (LBA mode only) Word 57 specifies the low world of the capacity
62	0000h	Reserved
63	XX07h	Multiword DMA Transfer Capability 15-8 Multiword DMA transfer mode active 7-0 (=7) Multiword DMA transfer modes supported (support mode 0 , 1 and 2)
64	0003h	Flow Control PIO Transfer modes supported 15-8 Reserved 7-0 (=3) Advanced PIO modes supported (‘11b’ = PIO Mode 3 and 4 Supported)
65	0078h	Minimum Multiword DMA transfer cycle time per word 15-0 Cycle time in nanoseconds (120ns, 16.6MB/S)
66	0078h	Manufacturer’s recommended Multiword DMA transfer cycle time 15-0 Cycle time in nanoseconds (120ns, 16.6MB/S)
67	0078h	Minimum PIO transfer cycle time without flow control 15-0 Cycle time in nanoseconds (120ns, 16.6MB/S)
68	0078h	Minimum PIO transfer cycle time with IORDY flow control 15-0 Cycle time in nanoseconds (120ns, 16.6MB/S)
69-79	0000h	Reserved
80	001Eh	Major version number 15-0 (=1Eh) ATA-1, ATA-2, ATA-3 and ATA/ATAPI-4
81	0017h	Minor version number 15-0 (=17h) ATA/ATAPI-4 X3T13 1153D revision 17

Table 6-6 IDENTIFY DEVICE information *(continued)*

Word	Content	Description
82	7469h	Command set supported. 15 (=0) Reserved 14 (=1) NOP command supported 13 (=1) READ BUFFER command supported 12 (=1) WRITE BUFFER command supported 11 (=0) Reserved 10 (=1) Host Protected Area feature set supported 9 (=0) DEVICE RESET command supported 8 (=0) SERVICE interrupt supported 7 (=0) release interrupt supported 6 (=1) look-ahead supported 5 (=1) write cache supported 4 (=0) supports PACKET Command feature set 3 (=1) supports Power Management feature set 2 (=0) supports Removable Media feature set 1 (=0) supports Security Mode feature set 0 (=1) supports SMART feature set
83	4000h	Command sets supported. 15-14 (=01) Word 83 is valid 13-5 (=0) Reserved 4 (=0) Removable Media Status Notification feature set supported 3 (=0) Advanced Power Management feature set supported 2 (=0) CFA feature set supported 1 (=0) READ/WRITE DMA QUEUED supported 0 (=0) DOWNLOAD MICROCODE command supported
84	4000h	Command set/feature supported extension. 15-14 (=01) Word 84 is valid 13-0 (=0) Reserved
85	7468h	Command set/feature enabled. (The default manufacturing setting is as below) 15 (=0) Reserved 14 (=1) NOP command enabled 13 (=1) READ BUFFER command enabled 12 (=1) WRITE BUFFER command enabled 11 (=0) Reserved 10 (=1) Host Protected Area feature set enabled 9 (=0) DEVICE RESET command enabled 8 (=0) SERVICE interrupt enabled 7 (=0) Release interrupt enabled 6 (=1) Look-ahead enabled 5 (=1) Write cache enabled 4 (=0) PACKET Command feature set enabled 3 (=1) Power Management feature set enabled 2 (=0) Removable Media feature set enabled 1 (=0) Security Mode feature set enabled 0 (=0) SMART feature set enabled

(continued)

Table 6-6 IDENTIFY DEVICE information *(continued)*

Word	Content	Description
86	0001h	Command set/feature enabled. . (The default manufacturing setting is as below) 15-5 Reserved 4 (=0) Removable Media Status Notification feature set enabled 3 (=0) Advanced Power Management feature set enabled 2 (=0) CFA feature set enabled 1 (=0) READ/WRITE DMA QUEUED command supported 0 (=0) DOWNLOAD MICROCODE command supported
87	4000h	Command set/feature default. 15-14 Word 87 is valid 13-0 Reserved
88	001Fh	Ultra DMA transfer modes 15-8 (=0Xh) Current active Ultra DMA transfer mode 15-13 Reserved (=0) 12 Ultra DMA mode 4 1= Active 0= Not Active 11 Ultra DMA mode 3 1= Active 0= Not Active 10 Ultra DMA mode 2 1= Active 0= Not Active 9 Ultra DMA mode 1 1= Active 0= Not Active 8 Ultra DMA mode 0 1= Active 0= Not Active 7-0 (1Fh) Ultra DMA transfer mode supported 7-5 Reserved (=0) 4 Ultra DMA mode 4 1= Support 3 Ultra DMA mode 3 1= Support 2 Ultra DMA mode 2 1= Support 1 Ultra DMA mode 1 1= Support 0 Ultra DMA mode 0 1= Support
89-92	0000h	Reserved
93	4101h	Hardware reset result. The contents of bits 12-0 of this word shall change only during the execution of a hardware reset. 15-14 (=01) Word 93 is valid 13 1=device detected CBLID- above $V_{iH,}$ 0=device detected CBLID- below V_{iL} 12-9 (=0) Reserved 8 (=1) Shall be set to one. 7-1 (=0) Reserved 0 (=1) Shall be set to one.
94	8000h	Command automatic acoustic management value. 15-8 (80h) Vendor's recommended acoustic management value. 7-0 (00h) Current automatic acoustic management value.
95-128	0000h	Reserved
129-159	0000h	Vendor specific
160-255	0000h	Reserved

6.4.7 Idle (97h,E3h)

This command causes the drive to set BSY, enter the Idle Mode, clear BSY, and generate an interrupt. The interrupt is generated even though the drive may not have fully transitioned to Idle Mode.

If the drive is already spinning, the spin-up sequence is not executed.

If the Sector Count register is non-zero, then the automatic Idle Mode sequence is enabled, and the timer begins counting down immediately. If the Sector Count register is zero, the automatic power down sequence is disabled.

After the drive enters Idle Mode, it automatically transitions to Standby Mode upon expiration of a prescribed 1 minute spin-down timer.

Table 6-7 Automatic Standby Timer Periods

Sector Count Register Contents	Corresponding Time-out Period
0 (00h)	Timeout Disabled
1-240 (01h-FOh)	(value * 5) seconds
241-251 (F1h-FBh)	(value - 240) * 30 minutes
252 (FCh)	21 minutes
253 (FDh)	8 hours
254 (FEh)	Reserved
255 (FFh)	21 minutes 15 seconds

6.4.8 Idle Immediate (95h,E1h)

This command causes the drive to set BSY, enter Idle Mode, clear BSY, and generate an interrupt. The interrupt is generated even though the drive may not have fully transitioned to Idle Mode.

6.4.9 Initialize Device Parameters (91h)

This command enables the host to set the number of sectors per track and the number of heads minus 1, per cylinder. Upon receipt of the command, the drive sets BSY, saves the parameters, clears BSY, and generates an interrupt.

The only two register values used by this command are the Sector Count register which specifies the number of sectors per track, and the Drive/Head register which specifies the number of heads minus 1. The DRV bit designates these values to Drive 0 or Drive 1, as appropriate.

The sector count and head values are not checked for validity by this command. If they are invalid, no error will be posted until an illegal access is made by some other command.

6.4.10 Read Buffer (E4h)

The Read Buffer command enables the host to read the current contents of the drive's sector buffer. When this command is issued, the drive sets BSY, sets up the sector buffer for a read operation, sets DRQ, clears BSY, and generates an interrupt. The host then reads up to 512 bytes of data from the buffer.

The Read Buffer and Write Buffer commands are synchronized so that sequential Write Buffer (E8h) and Read Buffer commands access the same 512 bytes within the buffer.

6.4.11 Read DMA (C8h:with retry, C9h:without retry)

This command executes in a manner similar to the Read Sector(s) command except for the following:

- The host initializes a slave-DMA channel prior to issuing the command
- Data transfers are qualified by DMARQ and are performed by the slave-DMA channel
- The drive issues only one interrupt per command to indicate that data transfer has stopped and the status is available.

Any unrecoverable error encountered during execution of a Read DMA command results in the termination of data transfer prior to the sector where the error was detected. The drive generates an interrupt to indicate that data transfer has terminated and status is available. The error posting is the same as that for the Read Sector(s) command.

6.4.12 Read Long (22h:with retry, 23h: without retry)

The Read Long command performs similarly to the Read Sectors command except that it returns the data and the ECC bytes appended to the data field of the desired sector. During a Read Long command, the drive does not check the ECC bytes to determine if there has been a data error. Only single sector Read Long operations are supported.

The transfer of the ECC bytes shall be 8 bits wide, and 4 or device native ECC bytes length.

6.4.13 Read Multiple Command (C4h)

The Read Multiple command performs similarly to the Read Sectors command. Interrupts are not generated on every sector, but on the transfer of a block which contains the number of sectors defined by a Set Multiple command.

Command execution is identical to the Read Sectors operation except that the number of sectors defined by a Set Multiple command are transferred without intervening interrupts. DRQ qualification of the transfer is required only at the start of the data block, not on each sector.

The block count of sectors to be transferred without intervening interrupts is programmed by the Set Multiple Mode command, which should be executed prior to the Read Multiple command. When the Read Multiple command is issued, the Sector Count register contains the number of sectors (not the number of blocks or the block count) requested.

If the number of requested sectors is not evenly divisible by the block count, as many full blocks as possible are transferred, followed by a final, partial block transfer. The partial block transfer shall be for n sectors, where

n = Remainder (Sector Count / Block Count)

If the Read Multiple command is attempted before the Set Multiple Mode command has been executed or when Read Multiple commands are disabled, then the Read Multiple operation is rejected with an Aborted Command error.

Disk errors encountered during Read Multiple commands are posted at the beginning of the block or partial block transfer, but DRQ is still set and the data transfer takes place as it normally would, including transfer of corrupted data, if any.

The contents of the Command Block registers, following the transfer of a data block, which had a sector in error, is undefined. The host should retry the transfer as individual requests to obtain valid error information.

Subsequent blocks or partial blocks are transferred only if the error was a correctable data error. All other errors cause the command to stop after transfer of the block, which contained the error. Interrupts are generated when DRQ is set at the beginning of each block or partial block.

6.4.14 Read Native Max Address (F8h)

This command returns the native maximum address. The native maximum address is the highest address accepted by the device in the factory default condition. The native maximum address is the maximum address that is valid when using the SET MAX ADDRESS command.

Normal Output:

Sector Number -
maximum native sector number (IDENTIFY DEVICE word 6) or LBA bits (7:0) for native max address on the device.
Cylinder Low -
maximum native cylinder number low or LBA bits (15:8) for native max address on the device.
Cylinder High -
maximum native cylinder number high or LBA bits (23:16) for native max address on device.
Device/Head -
maximum native head number (IDENTIFY DEVICE word 3 minus one) or LBA bits (27:24) for native max address on the device.
DEV shall indicate the selected device.
Status register -
BSY shall be cleared to zero indicating command completion.
DRDY shall be set to one.
DF (Device Fault) shall be cleared to zero.
DRQ shall be cleared to zero.
ERR shall be cleared to zero.

6.4.15 Read Sector(s) (20h:*with retry*, 21h:*without retry*)

This command reads from 1 to 256 sectors as specified in the Sector Count register. A sector count of 0 requests 256 sectors. The transfer begins at the sector specified in the Sector Number register. See 6.6.1 for the DRQ, IRQ and BSY protocol on data transfers.

If the drive is not already on the desired track, an implied seek is performed. Once at the desired track, the drive searches for the appropriate ID field.

If retries are disabled and two index pulses have occurred without error free reading of the requested ID, an ID Not Found error is posted. If retries are enabled, a vender-specified number of attempts are made to read the requested ID before posting an error.

If the ID is read correctly, the data address mark shall be recognized within a specified number of bytes, or the Address Mark Not Found error is posted. DRQ is always set prior to data transfer, regardless of the presence or absence of an error condition.

At command completion, the Command Block registers contain the cylinder, head, and sector number of the last sector read in CHS mode or of the logical block address in LBA mode.

If an error occurs, the read terminates at the sector where the error occurred. The Command Block registers contain the cylinder, head, and sector number of the sector where the error occurred in CHS mode or of the logical block address in LBA mode. The flawed data is pending in the sector buffer.

6.4.16 Read Verify Sector(s) (40h:*with retry*, 41h:*without retry*)

This command is identical to the Read Sectors command, except that DRQ is never set, and no data is transferred to the host. See 6.6.3 for the protocol. When the command is accepted, the drive sets BSY.

When the requested sectors have been verified, the drive clears BSY and generates an interrupt. Upon command completion, the Command Block registers contain the cylinder, head, and sector number of the last sector verified in CHS mode or of the logical block address in LBA mode. If an error occurs, the Verify terminates at the sector where the error occurred.

The Command Block registers contain the cylinder, head, and sector number in CHS mode, or the logical block address in LBA mode where the error occurred. The Sector Count register contains the number of sectors not yet verified.

6.4.17 Recalibrate (1xh)

This command moves the read/write heads from anywhere on the disk to cylinder 0. Upon receipt of the command, the drive sets BSY and issues a seek to cylinder zero. The drive then waits for the seek to complete before updating status, clearing BSY, and generating an interrupt. If the drive cannot reach cylinder 0, it posts a Track 0 Not Found error.

6.4.18 Seek (7xh)

This command initiates a seek to the track and selects the head specified in the command block. The drive need not be formatted for a seek to execute properly. Refer to section 6.6.3 for the protocol. The drive shall not set DSC=1 until the action of seeking has completed. The drive may return the interrupt before the seek is completed.

If another command is issued to the drive while a seek is being executed, the drive sets BSY=1, waits for the seek to complete, and then begins execution of the command.

6.4.19 Set Features (EFh)

This command is used by the host to establish the following parameters, which affect the execution of certain drive features as shown in Table 6-8.

Table 6-8 Set Feature Register Definitions

Code	Description
02h	Enable Write Cache
03h	Set transfer mode based on value in Sector Count register
33h	Disable Retry
42h	Enable Automatic Acoustic management feature set.
44h	Entire bytes of ECC apply on Read Long/Write Long commands
55h	Disable read look-ahead feature
66h	Disable reverting to power on defaults
77h	Disable ECC
82h	Disable Write Cache
88h	Enable ECC
99h	Enable Retries
AAh	Enable read look-ahead feature
BBh	4 bytes of ECC apply on Read Long/Write Long commands
C2h	Disable Automatic Acoustic management feature set.
CCh	Enable reverting to power on defaults

When the drive receives this command, it sets BSY, checks the contents of the Feature register, clears BSY, and generates an interrupt. If the value in the Feature register is not supported or is invalid, the drive posts an Aborted Command error. Refer to section 6.6.3 for the protocol.

A host can choose the transfer mechanism by Set Transfer Mode and specifying a value in the Sector Count register. The upper 5 bits define the type of transfer, and the low order 3 bits encode the mode value. Refer to Table 6-9.

Table 6-9 Transfer mode values

MODE	Bits(7:3)	Bits(2:0)
PIO default mode	00000	000
PIO default mode, disable IORDY	00000	001
PIO flow control transfer mode	00001	mode
Multiword DMA mode	00100	mode
Ultra DMA mode	01000	mode
mode = transfer mode number		

6.4.20 Set Max Address (F9h)

Host Protected Area feature set.

Inputs

Register	7	6	5	4	3	2	1	0
Features	Na							
Sector Count	Na							VV
Sector Number	Native max address sector number or SET MAX LBA							
Cylinder Low	SET MAX cylinder low or LBA							
Cylinder High	SET MAX cylinder high or LBA							
Device/Head	obs	LBA	obs	DEV	Native max address head number or SET MAX LBA			
Command	F9h							

Sector Count –

VV (Value volatile). If bit 0 is set to one, the device shall preserve the maximum values over power-up or hardware reset. If bit 0 is cleared to zero, the device shall revert to the most recent non-volatile maximum address value setting over power-up or hardware reset.

Sector Number –

Contains the native max address sector number (IDENTIFY DEVICE word 6) or LBA bits (7:0) value to be set.

Cylinder Low –

Contains the maximum cylinder low or LBA bits (15:8) value to be set.

Cylinder High –

Contains the maximum cylinder high or LBA bits (23:16) value to be set.

Device/Head –

If LBA is set to one, the maximum address value is an LBA value.
If LBA is cleared to zero, the maximum address value is a CHS value.
DEV shall indicate the selected device.
Bits (3:0) contain the native max address head number (IDENTIFY DEVICE word 3 minus one) or LBA bits (27:24) value to be set.

Normal outputs

Register	7	6	5	4	3	2	1	0
Error	Na							
Sector Count	Na							
Sector Number	Native max address sector number or LBA							
Cylinder Low	Native max address cylinder low or LBA							
Cylinder High	Native max address cylinder high or LBA							
Device/Head	obs	LBA	obs	LBA	Native max address head or LBA			
Status	BSY	DRDY	DF	na	DRQ	na	na	ERR

Sector Number –

Maximum native sector number or LBA bits (7:0) set on the device.

Cylinder Low –

Maximum cylinder number low or LBA bits (15:8) set on the device.

Cylinder High –

Maximum cylinder number high or LBA bits (23:16) set on device.

Device/Head –

DEV shall indicate the selected device.
maximum native head number or LBA bits (27:24) set on the device.

Status register –

BSY shall be cleared to zero indicating command completion.

DRDY shall be set to one.
DF (Device Fault) shall be cleared to zero.
DRQ shall be cleared to zero.
ERR shall be cleared to zero.

Description
After successful command completion, all read and write access attempts to addresses greater than specified by the successful SET MAX ADDRESS command shall be rejected with an IDNF error. IDENTIFY DEVICE response words 1, 54, 57, 60, and 61 shall reflect the maximum address set with this command.
Hosts should not issue more than one non-volatile SET MAX ADDRESS command after a power-on or hardware reset. Devices should report an IDNF error upon receiving a second non-volatile SET MAX ADDRESS command after a power-on or hardware reset.

The contents of IDENTIFY DEVICE words and the max address shall not be changed if a SET MAX ADDRESS command fails.
After a successful SET MAX ADDRESS command using a new maximum cylinder number value the content of IDENTIFY DEVICE words will abide by the following rules:

1) The content of words 3, 6, 55, and 56 are unchanged
2) The content of word 1 shall equal (the new SET MAX cylinder number + 1) or 16,383, whichever is less
3) The content of words (61:60) shall equal [(the new content of word 1 as determined by the successful SET MAX ADDRESS command) .(the content of word 3) .(the content of word 6)]
4) If the content of words (61:60) as determined by a successful SET MAX ADDRESS command is less than 16,514,064, then the content of word 54 shall be equal to [(the content of words (61:60)) ÷ ((the content of IDENTIFY DEVICE word 55) .(the content of word 56)] or 65,535, whichever is less
5) If the content of word (61:60) as determined by a successful SET MAX ADDRESS command is greater than 16,514,064, then word 54 shall equal the whole number result of [[(16,514,064) ÷ [(the content of word 55) .(the content of word 56)]] or 65,535 whichever is less) The content of words (58:57) shall be equal to [(the new content of word 54 as determined by the successful SET MAX ADDRESS command) .(the content of word 55) .(the content of word 56)]

After a successful SET MAX ADDRESS command using a new maximum LBA address the content of IDENTIFY DEVICE words will abide by the following rules:
.- The content of words (61:60) shall be equal to the new Maximum LBA address + 1.
.- If the content of words (61:60) is greater than 16,514,064 and if the device does not support CHS addressing, then the content of words 1, 3, 6, 54, 55, 56, and (58:57) shall equal zero.

If the device supports CHS addressing:
.- The content of words 3, 6, 55, and 56 are unchanged.
.- If the new content of words (61:60) is less than 16,514,064, then the content of word 1 shall be equal to [(the new content of words (61:60)) ÷ [(the content of word 3) .(the content of word 6)]] or 65,535, whichever is less.
.- If the new content of words (61:60) is greater than or equal to 16,514,064, then the content of word 1 shall be equal to 16,383.
.- If the new content of words (61:60) is less than 16,514,064, then the content of word 54 shall be equal to [(the new content of words (61:60)) ÷ [(the content of word 55) .(the content of word 56)]].
.- If the new content of words (61:60) is greater than or equal to 16,514,064, then the content of word 54 shall be equal to 16,383.
.- Words (58:57) shall be equal to [(the content of word 54) .(the content of word 55) .(the content of word 56)..

6.4.21 Set Multiple Mode (C6h)

This command enables the drive to perform Read and Write Multiple operations and establishes the block count for these commands. Refer to section 6.6.3 for the protocol.

The Sector Count register is loaded with the number of sectors per block. Drives support block sizes of 2, 4, 8, and 16 sectors. Upon receipt of the command, the drive sets BSY=1 and checks the Sector Count register.

If the Sector Count register contains a valid value and the block count is supported, the value is loaded for all subsequent Read Multiple and Write Multiple commands and execution of those commands is enabled. If a block count is not supported, an Aborted Command error is posted, and Read Multiple and Write Multiple commands are disabled.

If the Sector Count register contains 0 when the command is issued, Read and Write Multiple commands are disabled. At power-on, or after a hardware reset, the default mode is Read and Write Multiple disabled. And on software reset, the default mode of Read and Write Multiple will not be changed.

6.4.22 Sleep (99h, E6h)

This command is the only way to cause the drive to enter Sleep Mode. The drive is spun down, and when it is stopped, BSY is cleared, an interrupt is generated, and the interface becomes inactive.

The only way to recover from Sleep mode without a reset or power-on is for the host to issue a software reset.

A drive shall not power-on in Sleep Mode nor remain in Sleep Mode following a reset sequence. If the drive is already spun down, the spin down sequence is not executed.

6.4.23 Standby (96h,E2h)

This command causes the drive to set BSY, enter the Standby Mode, clear BSY, and assert INTRQ. INTRQ is asserted even though the device may not have fully transitioned to Standby Mode.

If the Sector Count register is non-zero, then the Standby Timer is enabled. The value in the Sector Count register shall be used to determine the time programmed into the Standby Mode.

The value in the Sector Count register when the STANDBY command is issued shall determine the time period programmed into the Standby Timer. See Table 6-7.

6.4.24 SMART (B0h)

Individual SMART commands are identified by the value placed in the Feature resister. Table 6-10 shows these Feature register values.

Table 6-10 SMART Feature register values

Value	Command
00h-CFh	Reserved
D0h	SMART READ DATA
D1h	SMART READ ATTRIBUTE THRESHOLDS
D2h	SMART ENABLE/DISABLE ATTRIBUTE AUTOSAVE
D3h	SMART SAVE ATTRIBUTE VALUES
D4h	SMART EXECUTE OFF-LINE IMMEDIATE
D5h	SMART READ LOG SECTOR
D6h	SMART WRITE LOG SECTOR
D7h	Obsolete
D8h	SMART ENABLE OPERATIONS
D9h	SMART DISABLE OPERATIONS
DAh	SMART RETURN STATUS
DBh	SMART ENABLE / DISABLE AUTOMATIC OFF-LINE
DCh-DFh	Reserved
E0h-FFh	Vendor specific

6.4.24.1 Smart disable operation (D9h)

This command disables all SMART capabilities within the device including any and timer and event count functions related exclusively to this feature. After receipt of this command the device shall disable all SMART operations. SMART data shall no longer be monitored or saved by the device. The state of SMART (either enabled or disabled) shall be preserved by the device across power cycles.

After receipt of this command by the device, all other SMART commands (including SMART DISABLE OPERATIONS commands), with the exception of SMART ENABLE OPERATIONS, are disabled and invalid and shall be command aborted by the device.

6.4.24.2 Smart enable/disable attribute autosave (D2h)

This command enables and disables the optional attribute autosave feature of the device. Depending upon the implementation, this command may either allow the device, after some vendor specified event, to automatically save its updated attribute values to non-volatile memory; or this command may cause the autosave feature to be disabled. The state of the attribute autosave feature (either enabled or disabled), shall be preserved by the device across power cycles.

A value of zero written by the host into the device's Sector Count register before issuing this command shall cause this feature to be disabled. Disabling this feature does not preclude the device from saving SMART data to non-volatile memory during some other normal operation such as during a power-on or power-off sequence or during an error recovery sequence.

A value of F1h written by the host into the device's Sector Count register before issuing this command shall cause this feature to be enabled. Any other meaning of this value or any other non-zero value written by the host into this register before issuing this command may differ from device to device. The meaning of any non-zero value written to this register at this time shall be preserved by the device across power cycles.

If this command is not supported by the device, the device shall return command aborted upon receipt from the host

During execution of the autosave routine the device shall not set BSY to one or clear DRDY to zero. If the device receives a command from the host while executing its autosave routine it shall respond to the host within two seconds.

6.4.24.3 Smart enable operations (D8h)

This command enables access to all SMART capabilities within the device. Prior to receipt of this command SMART data are neither monitored nor saved by the device. The state of SMART (either enabled or disabled) shall be preserved by the device across power cycles. Once enabled, the receipt of subsequent SMART ENABLE OPERATIONS commands shall not affect any SMART data or functions.

6.4.24.4 Smart execute off-line immediate (D4h)

This command causes the device to immediately initiate the optional set of activities that collect SMART data in an off-line mode and then save this data to the device's non-volatile memory.

During execution of its off-line activities the device shall not set BSY nor clear DRDY.

If the device is in the process of performing its set of off-line data collection activities (as a result of receiving a SMART EXECUTE OFF-LINE IMMEDIATE command from the host), and is interrupted by any new command from the host except a SMART DISABLE OPERATIONS, SMART EXECUTE OFF-LINE IMMEDIATE, or STANDBY IMMEDIATE command, the device shall suspend or abort its off-line data collection activities and service the host within two seconds after receipt of the new command. After servicing the interrupting command from host the device may immediately re-initiate or resume its off-line data collection activities without any additional commands from host (see the definition for Bit 2 in the Off-line data collection capability byte in 6.4.20.5)

If the device is in the process of performing its off-line data collection activities and is interrupted by a STANDBY IMMEDIATE command from the host, the device shall suspend or abort its off-line data collection activities, and service the host within two seconds after receipt of the command. After receiving a new command that causes the device to exit a power saving mode, the device shall initiate or resume off-line data collection activities without any additional commands from the host unless the device aborted these activities.

If the device is in the process of performing its off-line data collection activities and is interrupted by a SMART DISABLE OPERATIONS command from the host, the device shall suspend or abort its off-line data collection activities and service the host within two seconds after receipt of the command. Upon receipt of the next SMART ENABLE OPERATIONS command the device may, after the next vendor specified event, either re-initiate its off-line data collection activities or resume those activities from where they had been previously suspended.

If the device is in the process of performing its off-line data collection activities and is interrupted by a SMART EXECUTE OFF-LINE IMMEDIATE command from the host, the device shall abort its off-line data collection activities and service the host within two seconds after receipt of the command. The device shall then re-initiate its off-line data collection activities in response to the new EXECUTE OFF-LINE IMMEDIATE command.

6.4.24.5 Smart read data (D0h)

This command returns the Device SMART data structure to the host.

Table 6-11 defines the 512 bytes that make up the device SMART data structure.

Table 6-11 Device SMART data structure

Byte	F/V	Descriptions
0-361	X	Vendor specific
362	V	Off-line data collection status
363	X	Vendor specific
364-365	V	Total time in seconds to complete off-line data collection activity
366	X	Vendor specific
367	F	Off-line data collection capability
368-369	F	SMART capability
370-385	R	Reserved
386-510	X	Vendor specific
511	V	Data structure checksum
Key: F = the content of the byte is fixed and does not change. V = the content of the byte is variable and may change depending on the state of the device or the commands executed by the device. X = the content of the byte is vendor specific and may be fixed or variable. R = the content of the byte is reserved and shall be zero.		

The value of the off-line data collection status byte defines the current status of the off-line activities of the device. Table 6-12 lists the values and their respective definitions.

Table 6-12 Off-line data collection status values

Value	Definition
00h or 80h	Off-line data collection activity was never started.
01h	Reserved
02h or 82h	Off-line data collection activity was completed without error.
03h	Reserved
04h or 84h	Off-line data collection Activity was suspended by an interrupting command from host
05h or 85h	Off-line data collection Activity was aborted by an interrupting command from host
06h or 86h	Off-line data collection Activity was aborted by the device with a fatal error.
07h-3Fh	Reserved
40h-7Fh	Vendor specific
81h	Reserved
83h	Reserved
87h-BFh	Reserved
C0h-FFh	Vendor specific

The total time in seconds to complete off-line data collection activity word specifies how may seconds the device requires to complete its sequence of off-line data collection activity. Valid values for this word are from 0001h to FFFFh.

Off-line data collection capability.

The following describes the definition for the off-line data collection capability bits. If the value of all of these bits is equal to zero, then this device implements no off-line data collection.

- Bit 0 (EXECUTE OFF-LINE IMMEDIATE implemented bit) – If the value of this bit equals one, then the SMART EXECUTE OFF-LINE IMMEDIATE command is implemented by this device. If the value of this bit equals zero, then the SMART EXECUTE OFF-LINE IMMEDIATE command is not implemented by this device.

- Bit 1(vendor specific)

- Bit 2 (abort/restart off-line by host bit) – If the value of this bit equals one, then the device shall abort all off-line data collection activity initiated by an SMART EXECUTE OFF-LINE IMMEDIATE command upon receipt of a new command. Off-line data collection activity must be restarted by a new SMART EXECUTE OFF-LINE IMMEDIATE command from the host. If the value of this bit equals zero, the device shall suspend off-line data collection activity after an interrupting command and resume off-line data collection activity after some vendor-specified event.

- Bits 3-7 (reserved).

SMART capability

The following describes the definition for the SMART capability bits. If the value of all of these bits is equal to zero, then this device does not implement automatic saving of SMART data.

- Bit 0 (power mode SMART data saving capability bit) – If the value of this bit equals one, the device shall save its SMART data prior to going into a power saving mode (Idle, Standby, or Sleep) or immediately upon return to Active or Idle mode from a Standby mode. If the value of this bit equals zero, the device shall not save its SMART date prior to going into a power saving mode (Idle, Standby, or Sleep) or immediately upon return to Active or Idle mode from a Standby mode.

- Bit 1 (SMART data autosave after event capability bit) – The value of this bit shall be equal to one for devices complying with this standard.

- Bits 2-15(reserved).

The data structure checksum is the two's compliment of the result of a simple eight-bit addition of the first 511 bytes in the data structure.

6.4.24.6 SMART read log sector (D5h)

This command returns the indicated log sector to the host.

6.4.24.7 SMART return status (DAh)

This command is used to communicate the reliability status of the device to the host at the host's request. If a threshold exceeded condition is not detected by the device, the device shall set the Cylinder Low register to 4Fh and the Cylinder High register to C2h. If the device detects a threshold-exceeded condition, the device shall set Cylinder Low register to F4h and Cylinder High register to 2Ch

6.4.24.8 SMART save attribution value (D3h)

This command causes the device to immediately save any update attribute values to the device's non-volatile memory regardless of the state of the attribute autosave timer.

6.4.24.9 SMART write log sector (D6h)

This command writes a 512-byte data sector to the indicated log sector.

6.4.25 Standby (96h, E2h)

This command causes the drive to enter Standby Mode. See 6.6.3 for the protocol. The drive may return the interrupt before the transition to Standby Mode is completed.

If the drive is already spun down, the spin down sequence is not executed.

6.4.26 Standby Immediate (94h, E0h)

This command causes the drive to enter Standby Mode. See 6.6.3 for the protocol. The drive may return the interrupt before the transition to Standby Mode is completed.

If the drive is already spun down, the spin down sequence is not executed.

6.4.27 Write Buffer (E8h)

This command enables the host to overwrite the contents of the drive's sector buffer with any data pattern desired. See 6.6.2 for the protocol.

The Read Buffer and Write Buffer commands shall be synchronized within the drive such that sequential Write Buffer and Read Buffer commands access the same 512 bytes within the buffer.

6.4.28 Write Long (32h:with retry, 33h:without retry)

This command is similar to the Write Sectors command, except that it writes the data and the ECC bytes directly from the sector buffer; the drive does not generate the ECC bytes itself. Only single sector Write Long operations are supported.
The transfer of the ECC bytes shall be 8 bits wide, and 4 or device native ECC bytes length.

6.4.29 Write DMA (CAh)

This command executes in a similar manner to Write Sector(s) except for the following:

- The host initializes a slave-DMA channel prior to issuing the command
- Data transfers are qualified by DMARQ and are performed by the slave-DMA channel
- The drive issues only one interrupt per command to indicate that data transfer has terminated and status is available.

Any error encountered during Write DMA execution results in the termination of data transfer. The drive issues an interrupt to indicate that data transfer has terminated and the status is available in the Error register. The error posting is the same as that for the Write Sector(s) command.

6.4.30 Write Multiple Command (C5h)

This command is similar to the Write Sectors command. The drive sets BSY within 400 nsec of accepting the command, and interrupts are not presented on each sector but on the transfer of a block which contains the number of sectors defined by Set Multiple.

Command execution is identical to the Write Sectors operation, except that the number of sectors defined by the Set Multiple command are transferred without intervening interrupts. DRQ qualification of the transfer is required only at the start of the data block, not on each sector.

The block count of sectors to be transferred without intervening interrupts is programmed by the Set Multiple Mode command, which shall be executed prior to the Read Multiple command.

When the Write Multiple command is issued, the Sector Count register contains the number of sectors (not the number of blocks or the block count) requested.

If the number of requested sectors is not evenly divisible by the block count, as many full blocks as possible are transferred, followed by a final, partial block transfer. The partial block transfer is for n sectors, where

n = Remainder (Sector Count / Block Count)

If the Write Multiple command is attempted before the Set Multiple Mode command has been executed, or when Write Multiple commands are disabled, the Write Multiple operation is rejected with an aborted command error.

Disk errors encountered during execution of Write Multiple commands are posted after the attempted disk write of the block or partial block transfer. The Write Multiple command ends with the sector in error, even if it was in the middle of a block. Subsequent blocks are not transferred in the event of an error. Interrupts are generated when DRQ is set at the beginning of each block or partial block.

The contents of the Command Block registers, following the transfer of a data block which had a sector in error, are undefined. The host should retry the transfer as individual requests to obtain valid error information.

6.4.31 Write Sector(s) (30h:*with retry*, 31h:*without retry*)

This command writes from 1 to 256 sectors, as specified in the Sector Count register (a sector count of zero requests 256 sectors), beginning at the specified sector. Refer to Section 6.7 for the DRQ, IRQ and BSY protocol on data transfers.

If the drive is not already on the desired track, an implied seek is performed. Once at the desired track, the drive searches for the appropriate ID field.

If retries are disabled and two index pulses have occurred without error-free reading of the requested ID, an ID Not Found error is posted.

If retries are enabled, up to a predefined number of attempts may be made to read the requested ID before posting an error.

If the ID is read correctly, the data loaded in the buffer is written to the data field of the sector, followed by the ECC bytes. Upon command completion, the Command Block registers contain the cylinder, head, and sector number of the last sector written in CHS mode or the logical block address in LBA mode.

If an error occurs during a write of more than one sector, writing terminates at the sector where the error occurs. The Command Block registers contain the cylinder, head, and sector number of the sector where the error occurred in CHS mode or the logical block address in LBA mode. The host may then read the command block to determine what error has occurred and on which sector it occurred.

6.5 Programming Requirements

6.5.1 Reset Response

A reset is accepted within 400 nsec after the negation of RESET- or within 400 nsec after SRST has been set in the Device Control register.

When the drive is reset by RESET-, Drive 1 indicates it is present by asserting DASP- within 400 msec, and DASP- remains asserted for 30 seconds or until Drive 1 accepts the first command.

When the drive is reset by SRST, the drive sets BSY=1. See also Device Control register (section 6.3.3.3).

When a reset is accepted, and with BSY set:

a) Both drives perform hardware initialization
b) Both drives clear any previously programmed drive parameters
c) Both drives may revert to the default condition
d) Both drives load the Command Block registers with their default values
e) If it was a hardware reset, Drive 0 waits for DASP- to be asserted by Drive 1
f) If operational, Drive 1 asserts DASP-
g) Drive 0 waits for PDIAG- to be asserted, if Drive 1 asserts DASP-
h) If operational, Drive 1 clears BSY
i) If operational, Drive 1 asserts PDIAG-
j) Drive 0 clears BSY

No interrupt is generated when initialization is complete.

The default values for the Command Block registers, if no self-tests are performed or if no errors occurred, are:

Error	=	01h	Cylinder Low	=	00h
Sector Count	=	01h	Cylinder High	=	00h
Sector Number	=	01h	Drive/Head	=	00h

The Error register contains a Diagnostic Code (see Table 6-3).
Following any reset, the host should issue an Initialize Drive Parameters command to ensure the drive is initialized as desired.

6.5.2 Error Posting

The errors that are valid for each command are defined in Table 6-13.
See sections 6.3.4.4 and 6.3.4.10 for the definition of the Error register and Status register bits.

Table 6-13 Command Errors

Command	Error Register						Status Register				
	BBK	UNC	IDNF	ABRT	TK0NF	AMNF	DRDY	DWF	DSC	CORR	ERR
Check Power Mode				V			V	V	V		V
Download Micro Code				V			V	V	V		V
Execute Drive Diags											V
Flush Cache				V			V	V	V		V
Format Track			V	V			V	V	V		V
Identify Drive				V			V	V	V		V
Idle				V			V	V	V		V
Idle Immediate				V			V	V	V		V
Initialize Drive Parms							V	V	V		
Read Buffer				V			V	V	V		V
Read DMA	V	V	V	V		V	V	V	V	V	V
Read Long	V		V	V		V	V	V	V		V
Read Multiple	V	V	V	V		V	V	V	V	V	V
Read Native Max Addr.				V			V		V		V
Read Sector(s)	V	V	V	V		V	V	V	V	V	V
Read Verify Sector(s)	V	V	V	V		V	V	V	V	V	V
Recalibrate				V	V		V	V	V		V
Seek			V	V			V	V	V		V
Set Features				V			V	V	V		V
Set Max Address				V			V		V		V
Set Multiple Mode				V			V	V	V		V
Sleep				V			V	V	V		V
SMART command				V			V	V	V		V
Standby				V			V	V	V		V
Standby Immediate				V			V	V	V		V
Write Buffer				V			V	V	V		V
Write DMA	V		V	V			V	V	V		V
Write Long	V		V	V			V	V	V		V
Write Multiple	V		V	V			V	V	V		V
Write Sector(s)	V		V	V			V	V	V		V
Invalid Command				V			V	V	V		V

Legend:

V	=	Valid on this command	AMNF	=	Data address mark not found
BBK	=	Bad block detected	DRDY	=	Drive not ready detected
UNC	=	Uncorrectable data error	DWF	=	Drive write fault detected
IDNF	=	Requested ID not found	DSC	=	Disk seek complete not detected
ABRT	=	Abort command error	CORR	=	Corrected data error
TK0NF	=	Track zero not found error	ERR	=	Error bit in the Status register

6.5.3 Power Conditions

SpinPoint drives reduce the power required to operate (see Table 6-14), which describes each operating mode and the status of the major components.

Table 6-14 Power Saving Mode

MODE	R/W	Spindle	VCM	Servo	Interface	CPU	ADC	Pre Amp
SLEEP	OFF	OFF	OFF	OFF	Disk OFF Host OFF	OFF	OFF	OFF
STANDBY	OFF	OFF	OFF	OFF	Disk OFF Host OFF	ON	OFF	OFF
IDLE	OFF Partially (Time base generator)	ON	ON	ON	Disk OFF Host OFF	ON	ON	ON
NORMAL	ON	ON	ON	ON	ON	ON	ON	ON

6.5.3.1 Sleep mode

When a Sleep command is received, the drive enters Sleep mode.
The lowest power consumption occurs in Sleep mode. When in Sleep mode, the drive requires a reset to be activated (see 6.4.22).

6.5.3.2 Standby mode

When a Standby command is received, or an Auto-Power Down sequence is enabled and the Auto-Power Down Count is zero, then the drive enters Standby mode.
In Stand-By mode, the drive interface is capable of accepting commands, but the media is not immediately accessible.

6.5.3.3 Idle mode

When an Idle command is received, or an Auto-Power Down sequence is enabled and the Auto-Power Down Count is zero, then the drive enters Idle mode immediately.
After the drive enters Idle Mode, it automatically transitions to Standby Mode upon expiration of a prescribed 1 minute spin-down counter.

In Idle mode, the drive is capable of responding immediately to media access requests. A drive in Idle mode may take longer to complete the execution of a command than in Normal mode, because it may have to activate ENDEC and R/W circuit.

6.5.3.4 Normal mode

In Normal mode, the drive is capable of responding immediately to media access requests, and commands complete execution in the shortest possible time.

See specific power-related commands (0).

The power conditions in each mode are shown in Table 6-15.

Table 6-15 Power Conditions

MODE	SRST	BSY	DRDY	Interface Active	Media
SLEEP	*	x	x	*	0
STANDBY	x	0	1	Yes	0
IDLE	x	0	1	Yes	1
NORMAL	x	x	x	Yes	1

* : See 6.4.22
1 : Active
0 : Inactive
x : Doesn’t care

6.6 Protocol Overview

Commands can be grouped into different classes according to the protocols followed for command execution. The command classes with their associated protocols are defined below.

For all commands, the host first checks if BSY=1, and should proceed no further unless and until BSY=0. For most commands, the host will also wait for DRDY=1 before proceeding. Those commands shown with DRDY=X can be executed when DRDY=0.

6.6.1 PIO Data in Commands

This class includes:

- Identify Drive (ECh)
- Read Buffer (E4h)
- Read Long (22h)
- Read Multiple (C4h)
- Read Sector(s) (20h)
- SMART Read Data
- SMART Read Log Sector

Execution includes the transfer of one or more 512 byte (>512 bytes on Read Long) sectors of data from the drive to the host.

a) The host writes any required parameters to the Features, Sector Count, Sector Number, Cylinder and Drive/Head registers.

b) The host writes the command code to the Command register.

c) The drive sets BSY and prepares for data transfer.

d) When a sector of data is available, the drive sets DRQ and clears BSY prior to asserting INTRQ.

e) After detecting INTRQ, the host reads the Status register, then reads on sector of data via the Data register. In response to the Status register being read, the drive negates INTRQ.

f) The drive clears DRQ. If transfer of another sector is required, the drive also sets BSY and the above sequence is repeated from (d).

6.6.1.1 PIO Read Command

a)	b)		e)			e)		
Setup	Issue Command		Read Status	Transfer Data	=====	Read Status	Transfer Data	
BSY=0	DRDY=1	BSY=1	BSY=0		BSY=1	BSY=0		BSY=1
			DRQ=1 Assert INTRQ	Negate INTRQ	DRQ=0	DRQ=1 Assert INTRQ	Negate INTRQ	DRQ=0

If Error Status is presented, the drive is prepared to transfer data, and it is at the host's discretion that the data is transferred.

6.6.1.2 PIO Read Aborted Command

a)	b)		e)	
Setup	Issue Command		Read Status	
BSY=0	DRDY=1	BSY=1	BSY=0	
			DRQ=1 Assert INTRQ	DRQ=0 Negate INTRQ

Although DRQ=1, there is no data to be transferred under this condition.

6.6.2 PIO Data Out Commands

This class includes:

- Download Microcode (92h)
- Format (50h)
- SMART Write Log Sector
- Write Buffer (E8h)
- Write Long (32h)
- Write Multiple (C5h)
- Write Sector(s) (30h)

Execution includes the transfer of one or more 512 byte (>512 bytes on Write Long) sectors of data from the drive to the host.

a) The host writes any required parameters to the Features, Sector Count, Sector Number, Cylinder and Drive/Head registers.

b) The host writes the command code to the Command register.

c) The drive sets DRQ when it is ready to accept the first sector of data.

d) The host writes one sector of data via the Data register.

e) The drive clears DRQ and sets BSY.

f) When the drive has completed processing of the sector, it clears BSY and asserts INTRQ. If transfer of another sector is required, the drive also sets DRQ.

g) After detecting INTRQ, the host reads the Status registers.

h) The drive clears the interrupt.

i) If transfer of another sector is required, the above sequence is repeated from (d).

6.6.2.1 PIO Write Command

a)	b)				e)			e)	
Setup	Issue Command		Transfer Data		Read Status	Transfer Data	====	Read Status	
BSY=0	DRDY=1	BSY=1	BSY=0 DRQ=1	BSY=1 DRQ=0	BSY=0 DRQ=1 Assert INTRQ	Negate INTRQ	BSY=1 DRQ=0	BSY=0 Assert INTRQ	Negate INTRQ

6.6.2.2 PIO Write Aborted Command

a)	b)		e)	
Setup	Issue Command		Read Status	
BSY=0	DRDY=1	BSY=1	BSY=0 Assert INTRQ	Negate INTRQ

6.6.3 Non-Data Commands

This class includes:

- Check Power Mode (98h,E5h)
- Flush Cache (E7h)
- Execute Drive Diagnostic (DRDY=x) (90h)
- Idle (97h,E3h)
- Idle Immediate (95h,E1h)
- Initialize Drive Parameters (DRDY=x) (91h)
- NOP (00h)
- Read Native Max Address (F8h)
- Read Verify Sector(s) (40h)
- Recalibrate (1Xh)
- Seek (7Xh)
- Set Features (EFh)
- Set Max Address (F9h)
- Set Multiple Mode (C6h)
- Sleep (99h,E6h)
- SMART Disable Operation
- SMART Enable/Disable Autosave
- SMART Enable Operation
- SMART Execute Off-line Immediate
- SMART Return Status
- Standby (96h,E2h)
- Standby Immediate (94h,E0h)

Execution of these commands involves no data transfer.

a) The host writes any required parameters to the Features, Sector Count, Sector Number, Cylinder and Drive/Head registers.

b) The host writes the command code to the Command register.

c) The drive sets BSY.

d) When the drive has completed processing, it clears BSY and asserts INTRQ.

e) The host reads the Status register.

f) The drive negates INTRQ.

6.6.4 DMA Data Transfer Commands

This class comprises:

- Read DMA (C8h)
- Write DMA (C9h)

Data transfers using DMA commands differ in two ways from PIO transfers:

- Data transfers are performed using the slave-DMA channel,
- No intermediate sector interrupts are issued on multi-sector commands.

Initiation of the DMA transfer commands is identical to the Read Sector or Write Sector commands except that the host initializes the slave-DMA channel prior to issuing the command.

The interrupt handler for DMA transfers is different in that:

- No intermediate sector interrupts are issued on multi-sector commands,
- The host resets the DMA channel prior to reading status from the drive.

The DMA protocol allows a high performance, multi-tasking operating system to eliminate processor overhead associated with PIO transfers.

a) Command phase
   1) Host initializes the slave-DMA channel.
   2) Host updates the Command Block registers.
   3) Host writes command code to the Command register.

b) Data phase. The register contents are not valid during a DMA data Phase.
   1) The slave-DMA channel qualifies data transfers to and from the drive with DMARQ.

c) Status phase
   1) Drive generates the interrupt to the host.
   2) Host resets the slave-DMA channel.
   3) Host reads the Status register and Error register.

6.6.4.1 Normal DMA transfer

Initialize DMA	Command	DMA data transfer	Reset DMA	Status
BSY=0	BSY=1	BSY=x DRQ=x	BSY=1 nIEN=0	BSY=0

6.6.4.2 Aborted DMA transfer

Initialize DMA	Command	DMA data	Reset DMA	Status
BSY=0	BSY=1	BSY=x DRQ=1	BSY=1 nIEN=0	BSY=0

6.6.4.3 Aborted DMA Command

Initialize DMA	Command	Reset DMA	Status
BSY=0	BSY=1	BSY=1 nIEN=0	BSY=0

6.7 Timing

The minimum cycle time supported by the device in PIO mode 3, 4 and Multiword DMA mode 1, 2 respectively, shall always be greater than, or equal to the minimum cycle time defined by the associated mode. For example, a device supporting PIO mode 4 timing shall not report a value less than 120ns, the minimum cycle time defined for PIO mode 4 timings.

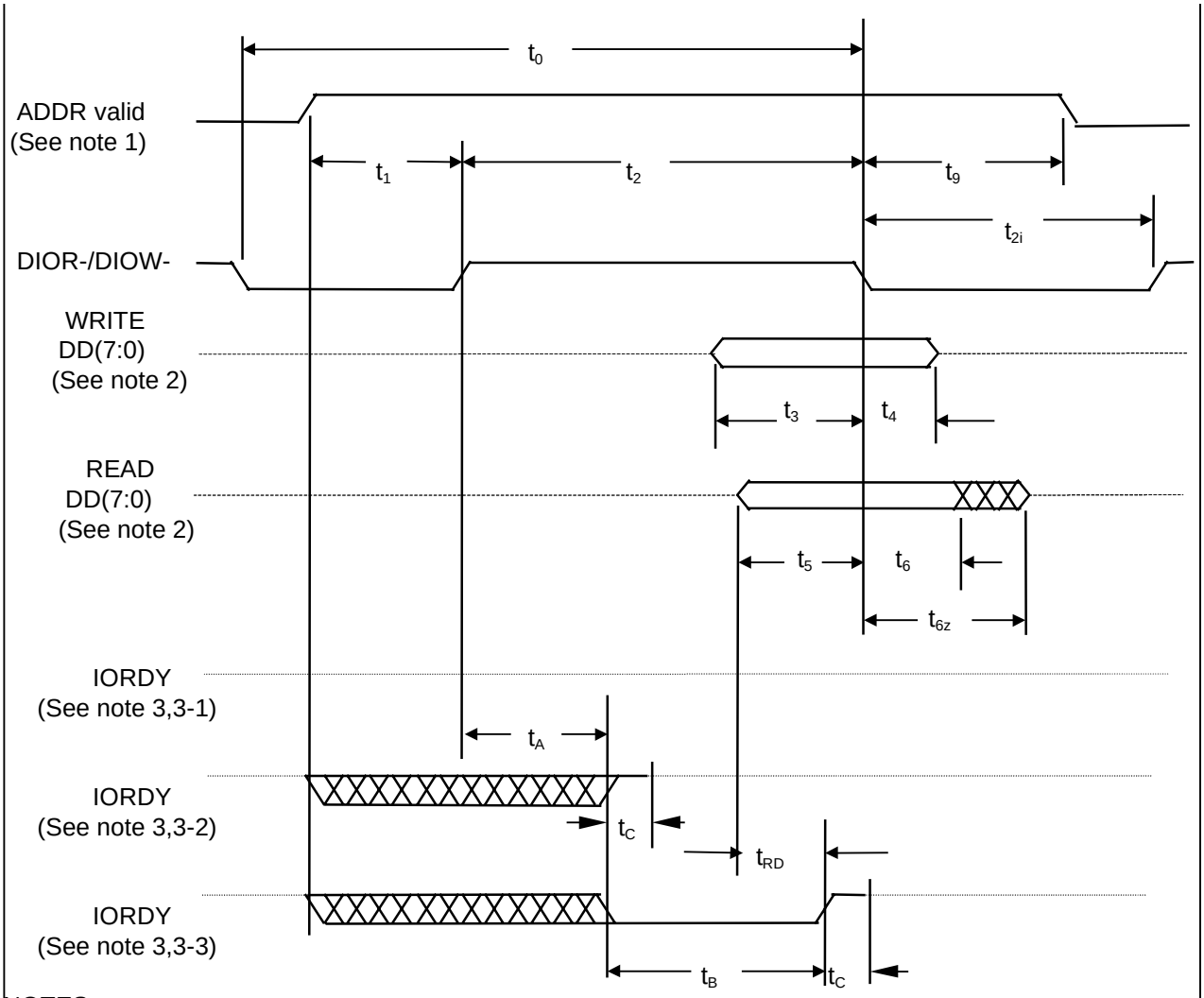
6.7.1 Register transfers

Figure 6-1 defines the relationships between the interface signals for register transfers. Peripherals reporting support for PIO mode 3 or 4 shall power up in a PIO mode 0, 1, or 2.

For PIO modes 3 and above, the minimum value of t_0 is specified by word 68 in the IDENTIFY DEVICE parameter list. Table 6-16 defines the minimum value that shall be placed in word 68.

IORDY will be supported when PIO modes 3 or 4 are the current mode of operation.

> NOTE – Some devices implementing the PACKET Command feature set prior to this standard power up in PIO mode 3 and enable IORDY as the default.



NOTES –

1 Device address consists of signals CS0-, CS1- and DA(2:0)

2 Data consists of DD(7:0).

3 The negation of IORDY by the device is used to extend the PIO cycle. The determination of whether the cycle is to be extended is made by the host after t_A from the assertion of DIOR- or DIOW-. The assertion and negation of IORDY are described in the following three cases:

3-1 Device never negates IORDY, devices keeps IORDY released: no wait is generated.

3-2 Device negates IORDY before t_A, but causes IORDY to be asserted before t_A. IORDY is released prior to negation and may be asserted for no more than 5 ns before release: no wait generated.

3-3 Device negates IORDY before t_A. IORDY is released prior to negation and may be asserted for no more than 5 ns before release: wait generated. The cycle completes after IORDY is reasserted. For cycles where a wait is generated and DIOR- is asserted, the device shall place read data on DD(7:0) for t_{RD} before asserting IORDY.

4 DMACK – Shall remain negated during a register transfer.

Figure 6-1 Register transfer to/from device

Table 6-16 Register transfer to/from device

PIO timing parameters			Mode 0 ns	Mode 1 ns	Mode 2 ns	Mode 3 ns	Mode 4 ns	Note
t_0	Cycle time	(min)	600	383	330	180	120	1,4
t_1	Address valid to DIOR-/DIOW- setup	(min)	70	50	30	30	25	
t_2	DIOR-/DIOW- pulse width 8-bit	(min)	290	290	290	80	70	1
t_{2i}	DIOR-/DIOW- recovery time	(min)	-	-	-	70	25	1
t_3	DIOW- data setup	(min)	60	45	30	30	20	
t_4	DIOW- data hold	(min)	30	20	15	10	10	
t_5	DIOR- data setup	(min)	50	35	20	20	20	
t_6	DIOR- data hold	(min)	5	5	5	5	5	
T_{6Z}	DIOR- data tristate	(max)	30	30	30	30	30	2
t_9	DIOR-/DIOW- to address valid hold	(min)	20	15	10	10	10	
t_{RD}	Read Data Valid to IORDY active (if IORDY initially low after t_A)	(min)	0	0	0	0	0	
t_A	IORDY Setup time		35	35	35	35	35	3
t_B	IORDY Pulse Width	(max)	1250	1250	1250	1250	1250	
t_C	IORDY assertion to release	(max)	5	5	5	5	5	

NOTES –
1 t_0 is the minimum total cycle time, t_2 is the minimum command active time, and t_{2i} is the minimum command recovery time or command inactive time. The actual cycle time equals the sum of the actual command active time and the actual command inactive time. The three timing requirements of t_0, t_2, and t_{2i} shall be met. The minimum total cycle time requirements are greater than the sum of t_2 and t_{2i}. This means a host implementation may lengthen either or both t_2 or t_{2i} to ensure that t_0 is equal to or greater than the value reported in the devices IDENTIFY DEVICE data. A device implementation shall support any legal host implementation.
2 This parameter specifies the time from the negation edge of DIOR- to the time that the data bus is no longer driven by the device (tri-state).
3The delay from the activation of DIOR- or DIOW- until the state of IORDY is first sampled. If IORDY is inactive then the host shall wait until IORDY is active before the PIO cycle is completed. If the device is not driving IORDY negated at the t_A after the activation of DIOR- or DIOW-, then t_5 shall be met and tRD is not applicable. If the device is driving IORDY negated at the time t_A after the activation of DIOR- or DIOW-, then t_{RD} shall be met and t_5 is not applicable.
4 Mode shall be selected no faster than the highest mode supported by the slowest device.

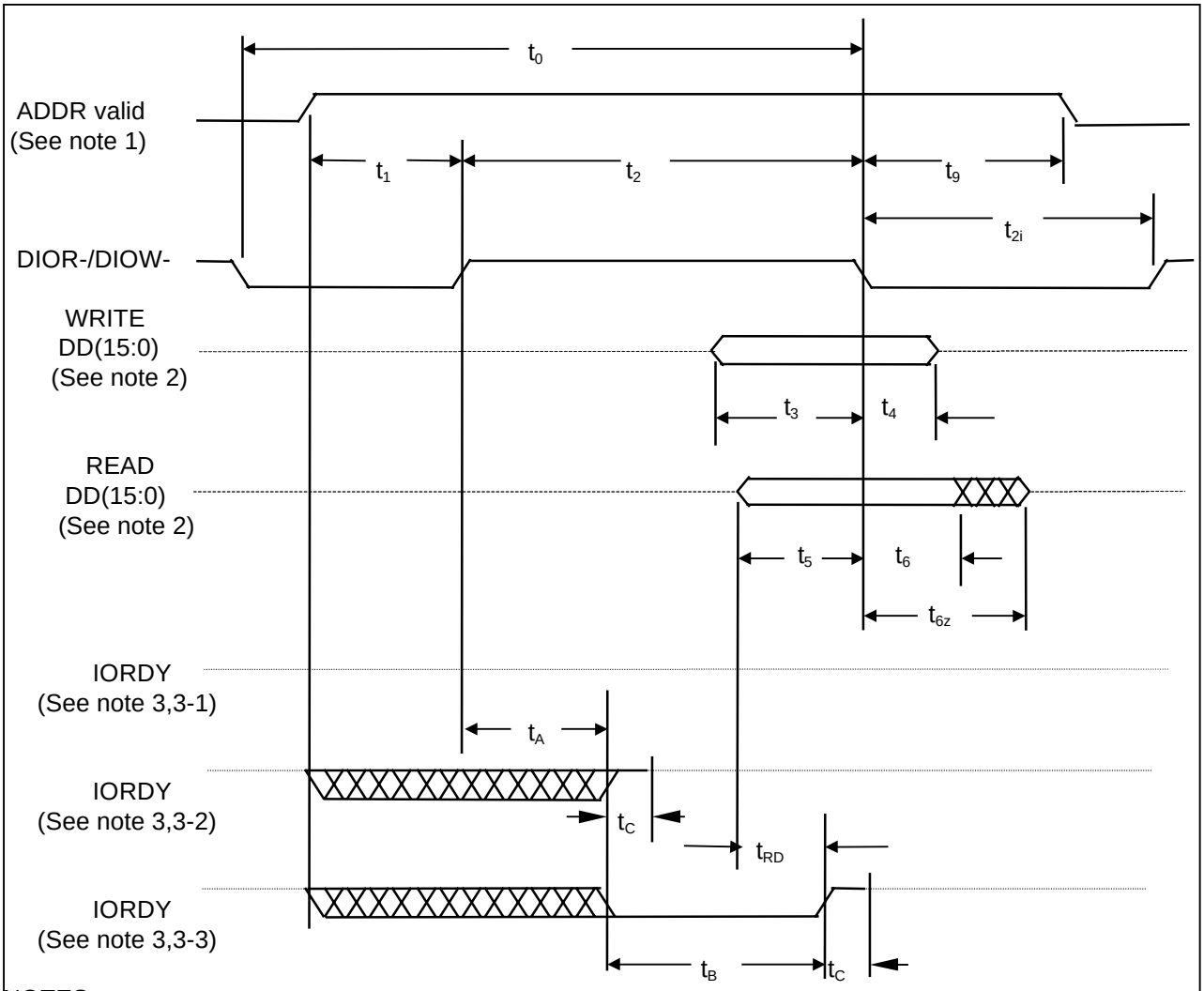
6.7.2 PIO data transfers

Figure 6-2 defines the relationships between the interface signals for PIO data transfers. Peripherals reporting support for PIO mode 3 or 4 shall power up in a PIO mode 0, 1, or 2.

For PIO modes 3 and above, the minimum value of t_0 is specified by word 68 in the IDENTIFY DEVICE parameter list. Table 6-17 defines the minimum value that shall be placed in word 68.

IORDY shall be supported when PIO modes 3 or 4 are the current mode of operation.

> NOTE – Some devices implementing the PACKET Command feature set prior to this standard power up in PIO mode 3 and enable IORDY as the default.



NOTES –

1 Device address consists of signals CS0-, CS1- and DA(2:0)

2 Data consists of DD(15:0).

3 The negation of IORDY by the device is used to extend the PIO cycle. The determination of whether the cycle is to be extended is made by the host after t_A from the assertion of DIOR- or DIOW-. The assertion and negation of IORDY are described in the following three cases:

3-1 Device never negates IORDY, devices keeps IORDY released: no wait is generated.

3-2 Device negates IORDY before t_A, but causes IORDY to be asserted before t_A. IORDY is released prior to negation and may be asserted for no more than 5 ns before release: no wait generated.

3-3 Device negates IORDY before t_A. IORDY is released prior to negation and may be asserted for no more than 5 ns before release: wait generated. The cycle completes after IORDY is reasserted. For cycles where a wait is generated and DIOR- is asserted, the device shall place read data on DD(15:0) for t_{RD} before asserting IORDY.

4 DMACK – shall be negated during a PIO data transfer.

Figure 6-2 PIO data transfer to/from device

Table 6-17 PIO data transfer to/from device

PIO timing parameters			Mode 0 ns	Mode 1 ns	Mode 2 ns	Mode 3 ns	Mode 4 ns	Note
t_0	Cycle time	(min)	600	383	240	180	120	1,4
t_1	Address valid to DIOR-/DIOW- setup	(min)	70	50	30	30	25	
t_2	DIOR-/DIOW- 16-bit	(min)	165	125	100	80	70	1
t_{2i}	DIOR-/DIOW- recovery time	(min)	-	-	-	70	25	1
t_3	DIOW- data setup	(min)	60	45	30	30	20	
t_4	DIOW- data hold	(min)	30	20	15	10	10	
t_5	DIOR- data setup	(min)	50	35	20	20	20	
t_6	DIOR- data hold	(min)	5	5	5	5	5	
t_{6Z}	DIOR- data tri-state	(max)	30	30	30	30	30	2
t_9	DIOR-/DIOW- to address valid hold	(min)	20	15	10	10	10	
t_{RD}	Read Data Valid to IORDY active (if IORDY initially low after t_A)	(min)	0	0	0	0	0	
t_A	IORDY Setup time		35	35	35	35	35	3
t_B	IORDY Pulse Width	(max)	1250	1250	1250	1250	1250	
t_C	IORDY assertion to release	(max)	5	5	5	5	5	

NOTES –

1 t_0 is the minimum total cycle time, t_2 is the minimum command active time, and t_{2i} is the minimum command recovery time or command inactive time. The actual cycle time equals the sum of the actual command active time and the actual command inactive time. The three timing requirements of t_0, t_2, and t_{2i} shall be met. The minimum total cycle time requirements are greater than the sum of t_2 and t_{2i}. This means a host implementation may lengthen either or both t_2 or t_{2i} to ensure that t_0 is equal to or greater than the value reported in the devices IDENTIFY DEVICE data. A device implementation shall support any legal host implementation.

2 This parameter specifies the time from the negation edge of DIOR- to the time that the data bus is no longer driven by the device (tri-state).

3The delay from the activation of DIOR- or DIOW- until the state of IORDY is first sampled. If IORDY is inactive then the host shall wait until IORDY is active before the PIO cycle is completed. If the device is not driving IORDY negated at the t_A after the activation of DIOR- or DIOW-, then t_5 shall be met and t_{RD} is not applicable. If the device is driving IORDY negated at the time t_A after the activation of DIOR- or DIOW-, then t_{RD} shall be met and t_5 is not applicable.

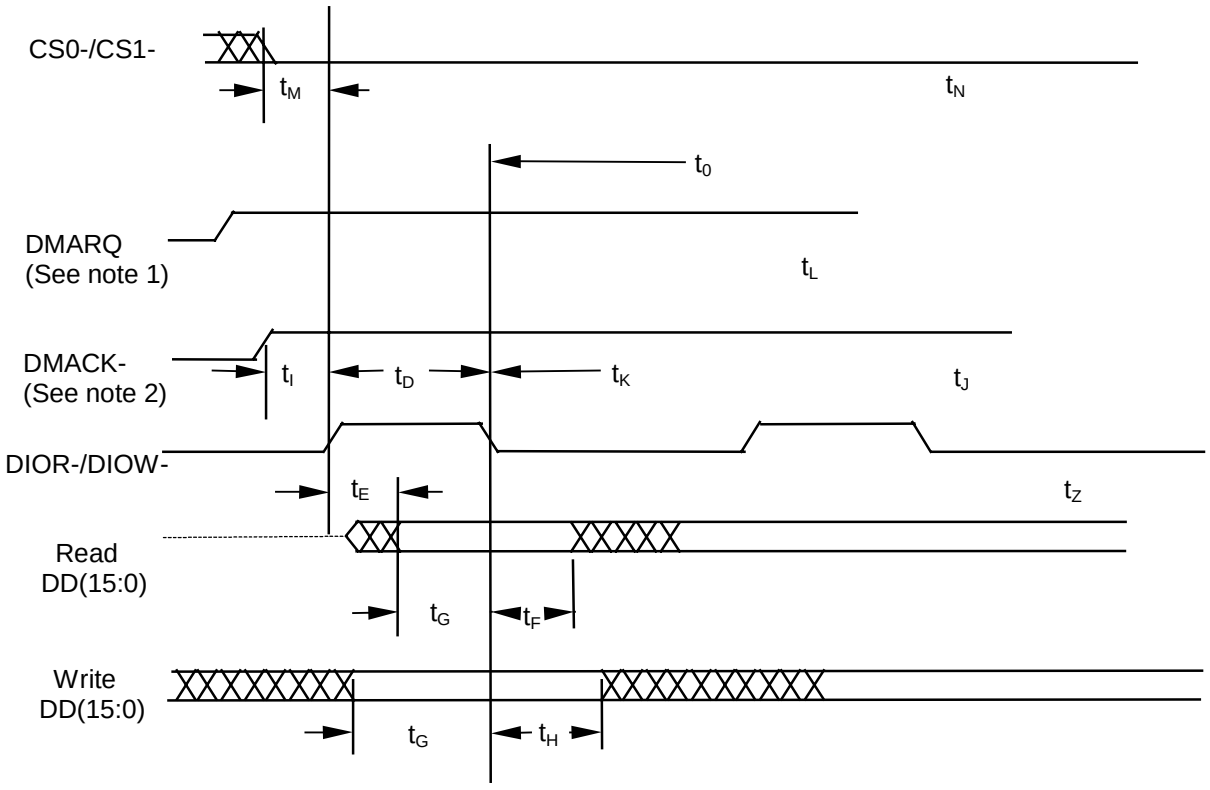
4 Mode may be selected at the highest mode for the device if CS(1:0) and AD(2:0) do not change between read or write cycles or selected at the highest mode supported by the slowest device if CS(1:0) or AD(2:0) do change between read or write cycles.

6.7.3 Multiword DMA data transfer

Figure 6-3 defines the timings associated with Multiword DMA transfers.

For Multiword DMA modes 1 and above, the minimum value of t_0 is specified by word 65 in the IDENTIFY DEVICE parameter list. Table 6-18 defines the minimum value that shall be placed in word 65.

Devices shall power up with mode 0 as the default Multiword DMA mode.



NOTE –
1 To prevent the transmission of another word of data, the Device shall negate DMARQ within the t_L specified time once DMACK- is asserted and reassert it again at a later time to resume the DMA operation. Alternatively, if the device is able to continue the transfer of data, the device may leave DMARQ asserted and wait for the host to reassert DMACK-.
2 This signal may be negated by the Host to suspend the DMA transfer in process.
3 This figure shows the transfer of two words. The actual transfer for a given assertion of DMARQ may be any number of words from one to the remaining number of words to be transferred.

Figure 6-3 Multiword DMA data transfer

Table 6-18 Multiword DMA data transfer

Multiword DMA timing parameters			Mode 0 ns	Mode 1 ns	Mode 2 ns	Note
t_0	Cycle time	(min)	480	150	120	see note
t_D	DIOR-/DIOW-	(min)	215	80	70	see note
t_E	DIOR- data access	(max)	150	60	50	
t_F	DIOR- data hold	(min)	5	5	5	
t_G	DIOR-/DIOW- data setup	(min)	100	30	20	
t_H	DIOW- data hold	(min)	20	15	10	
t_I	DMACK to DIOR-/DIOW- setup	(min)	0	0	0	
t_J	DIOR-/DIOW- to DMACK hold	(min)	20	5	5	
t_{KR}	DIOR- negated pulse width	(min)	50	50	25	see note
t_{KW}	DIOW- negated pulse width	(min)	215	50	25	see note
t_{LR}	DIOR- to DMARQ delay	(max)	120	40	35	
t_{LW}	DIOW- to DMARQ delay	(max)	40	40	35	
t_M	CS(1:0) valid to DIOR-/DIOW-	(min)	50	30	25	
t_N	CS(1:0) hold	(min)	15	10	10	
t_Z	DMACK- to tri-state	(max)	20	25	25	

NOTE – t_0 is the minimum total cycle time, t_D is the minimum command active time, and t_K (t_{KR} or t_{KW}, as appropriate) is the minimum command recovery time or command inactive time. The actual cycle time equals the sum of the actual command active time and the actual command inactive time. The three timing requirements of t_0, t_D, t_K shall be met. The minimum total cycle time requirement, t_0, is greater than the sum of t_D and t_K. This means a host implementation may lengthen either or both t_D or t_K to ensure that t_0 is equal to the value reported in the devices IDENTIFY DEVICE data. A device implementation shall support any legal host implementation.

6.7.4 Ultra DMA data transfer

Figures 6-4 through 6-13 define the timings associated with all phases of Ultra DMA bursts.

Table 6-19 contains the values for the timings for each of the Ultra DMA modes.

6.7.4.1 Initiating an Ultra DMA data in burst

The values for the timings for each of the Ultra DMA modes are contained in 6.7.4.2.

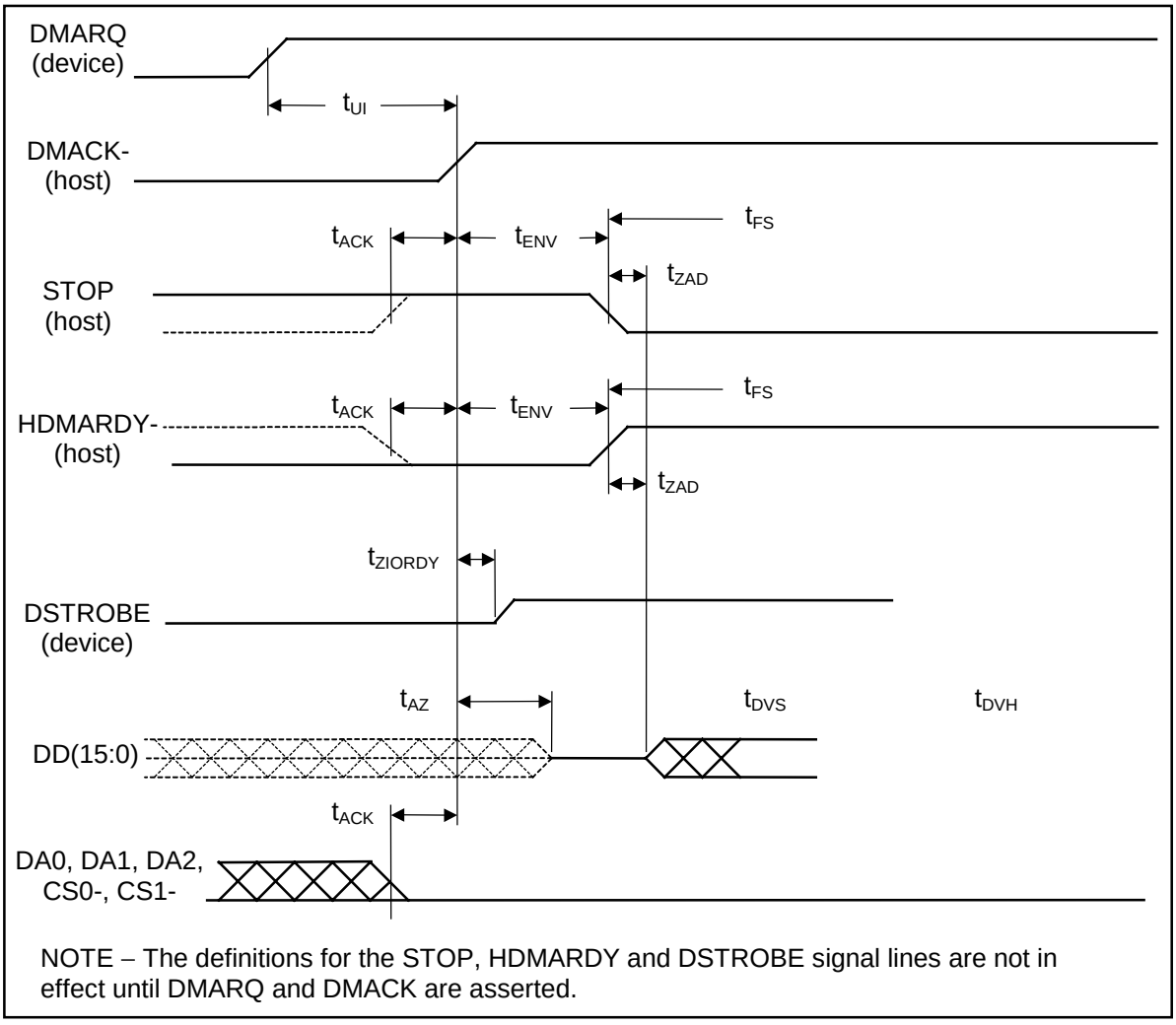


Figure 6-4 Initiating an Ultra DMA data in burst

6.7.4.2 Ultra DMA data burst timing requirements

Table 6-19 Ultra DMA data burst timing requirements

Name	Mode 0 (ns)		Mode 1 (ns)		Mode 2 (ns)		Mode 3 (ns)		Mode 4 (ns)		Mode 5 (ns)		Comment
	min	max	min	max	min	max	min	max	min	max	min	max	(see Notes 1 and 2)
$t_{2CYCTYP}$	240		160		120		90		60		40		Typical sustained average two cycle time
t_{CYC}	112		73		54		39		25		16.8		Cycle time allowing for asymmetry and clock variations (from STROBE edge to STROBE edge)
t_{2CYC}	230		154		115		86		57		38		Two cycle time allowing for clock variations (from rising edge to next rising edge or from falling edge to next falling edge of STROBE)
t_{DS}	15		10		7		7		5		4.0		Data setup time at recipient
t_{DH}	5		5		5		5		5		4.6		Data hold time at recipient
t_{DVS}	70		48		30		20		6		4.8		Data valid setup time at sender (from data valid until STROBE edge) (see Note 4)
t_{DVH}	6		6		6		6		6		4.8		Data valid hold time at sender (from STROBE edge until data may become invalid) (see Note 4)
t_{FS}	0	230	0	200	0	170	0	130	0	120		90	First STROBE time (for device to first negate DSTROBE from STOP during a data in burst)
t_{LI}	0	150	0	150	0	150	0	100	0	100	0	75	Limited interlock time (see Note 3)
t_{MLI}	20		20		20		20		20		20		Interlock time with minimum (see Note 3)
t_{UI}	0		0		0		0		0		0		Unlimited interlock time (see Note 3)
t_{AZ}		10		10		10		10		10		10	Maximum time allowed for output drivers to release (from asserted or negated)
t_{ZAH}	20		20		20		20		20		20		Minimum delay time required for output
t_{ZAD}	0		0		0		0		0				Drivers to assert or negate (from released)
t_{ENV}	20	70	20	70	20	70	20	55	20	55	20	50	Envelope time (from DMACK- to STOP and HDMARDY –during data in burst initiation and from DMACK to STOP during data out burst initiation
t_{SR}		50		30		20		NA		NA		NA	STROBE-to-DMARDY-time (if DMARDY- is negated before this long after STROBE edge, the recipient shall receive no more than one additional data word)
t_{RFS}		75		70		60		60		60		50	Ready-to-final-STROBE time (no STROBE edges shall be sent this long after negation of DMARDY-)
t_{RP}	160		125		100		100		100			85	Ready-to-pause time (that recipient shall wait to pause after negating DMARDY-)
t_{IORDYZ}		20		20		20		20		20		20	Maximum time before releasing IORDY
t_{ZIORDY}	0		0		0		0		0		0		Minimum time before driving STROBE (see note 5)
t_{ACK}	20		20		20		20		20		20		Setup and hold times for DMACK-before assertion or negation).
t_{SS}	50		50		50		50		50		50		Time from STROBE edge to negation of DMARQ or assertion of STOP (when sender terminates a burst)

Table 6-19 Ultra DMA data burst timing requirements (cont).

NOTES –
1 Timing parameters shall be measured at the connector of the sender or receiver to which the parameter applies. For example, the sender shall stop generating STROBE edges t_{RFS} after the negation of DMARDY-. Both STROBE and DMARDY- timing measurements are taken at the connector of the sender.
2 All timing measurement-switching points (low to high and high to low) shall be taken at 1.5V.
3 t_{UI} , t_{MLI} , and t_{LI} indicate sender-to-recipient or recipient-to-sender interlocks, i.e., either sender or recipient is waiting for the other to respond with a signal before proceeding. t_{UI} is an unlimited interlock that has no maximum time value. t_{MLI} is a limited time-out that has a defined minimum. t_{LI} is a limited time-out that has a defined maximum.
4 The test load for t_{DVS} and t_{DVH} shall be a lumped capacitor load with no cable or receivers. Timing for t_{DVS} and t_{DVH} shall be met for all capacitive loads from 15 to 40 pf where all signals have the same capacitive load value.
5 t_{ZIORDY} may be greater than t_{ENV} since the device has a pull up on IORDY- giving it a known state when released.

6.7.4.3 Sustained Ultra DMA data in burst

The values for the timings for each of the Ultra DMA modes are contained in 6.7.4.2.

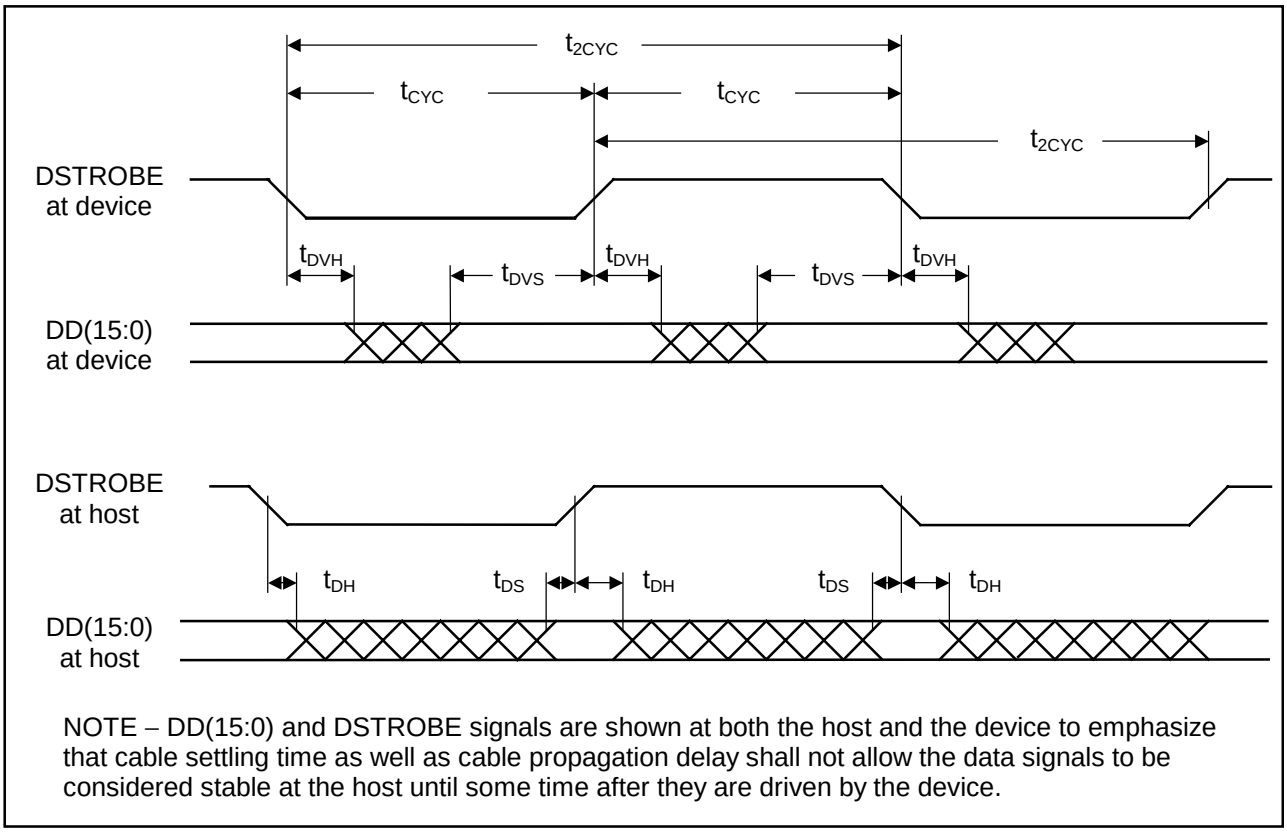


Figure 6-5 Sustained Ultra DMA data in burst

6.7.4.4 Host pausing an Ultra DMA data in burst

The values for the timings for each of the Ultra DMA modes are contained in 6.7.4.2.

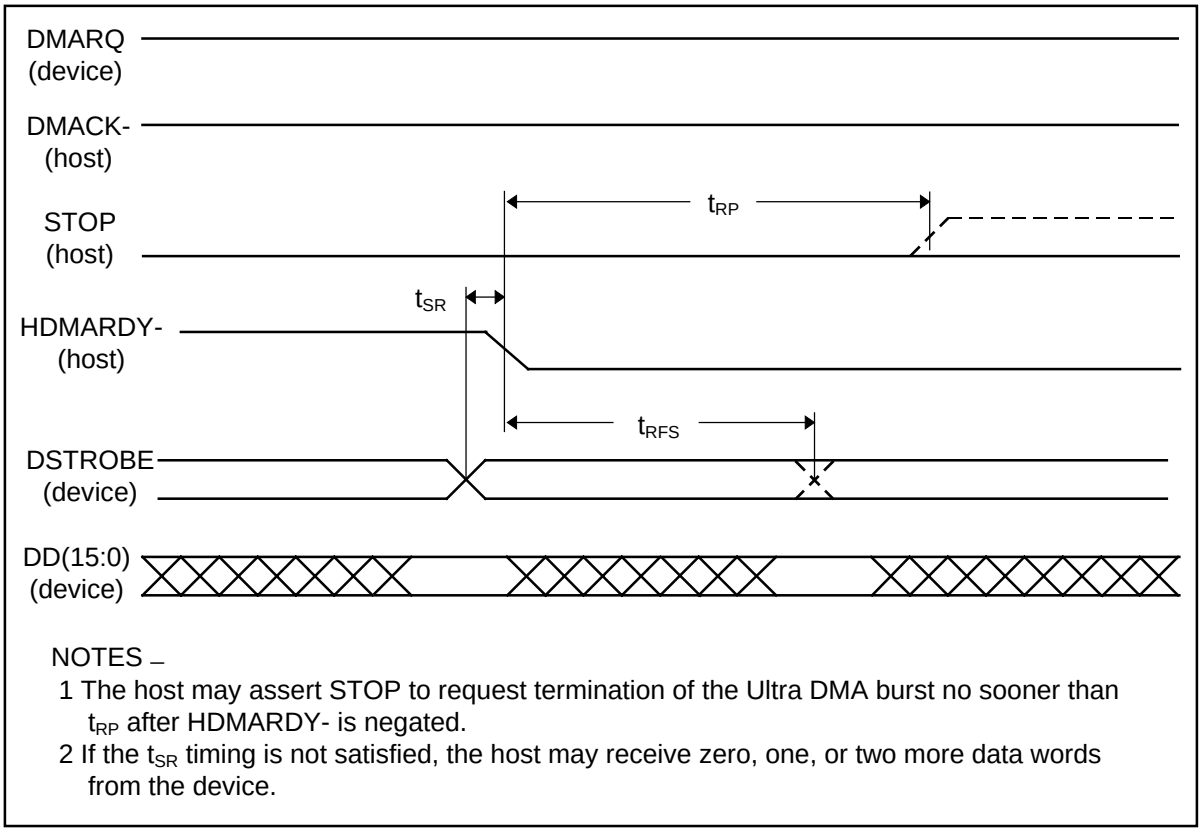


Figure 6-6 Host pausing an Ultra DMA data in burst

6.7.4.5 Device terminating an Ultra DMA data in burst

The values for the timings for each of the Ultra DMA modes are contained in 6.7.4.2.

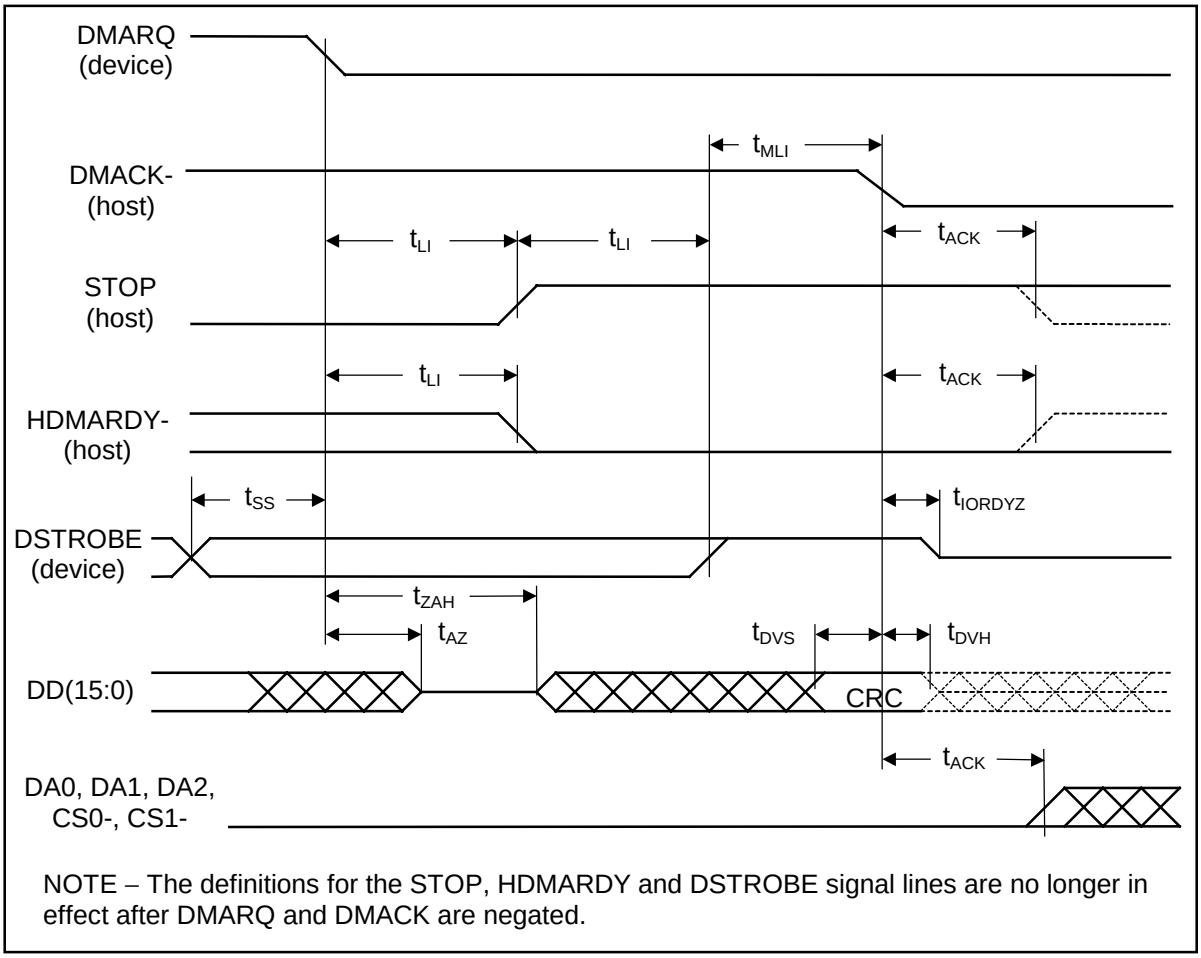


Figure 6-7 Device terminating an Ultra DMA data in burst

6.7.4.6 Host terminating an Ultra DMA data in burst

The values for the timings for each of the Ultra DMA modes are contained in 6.7.4.2.

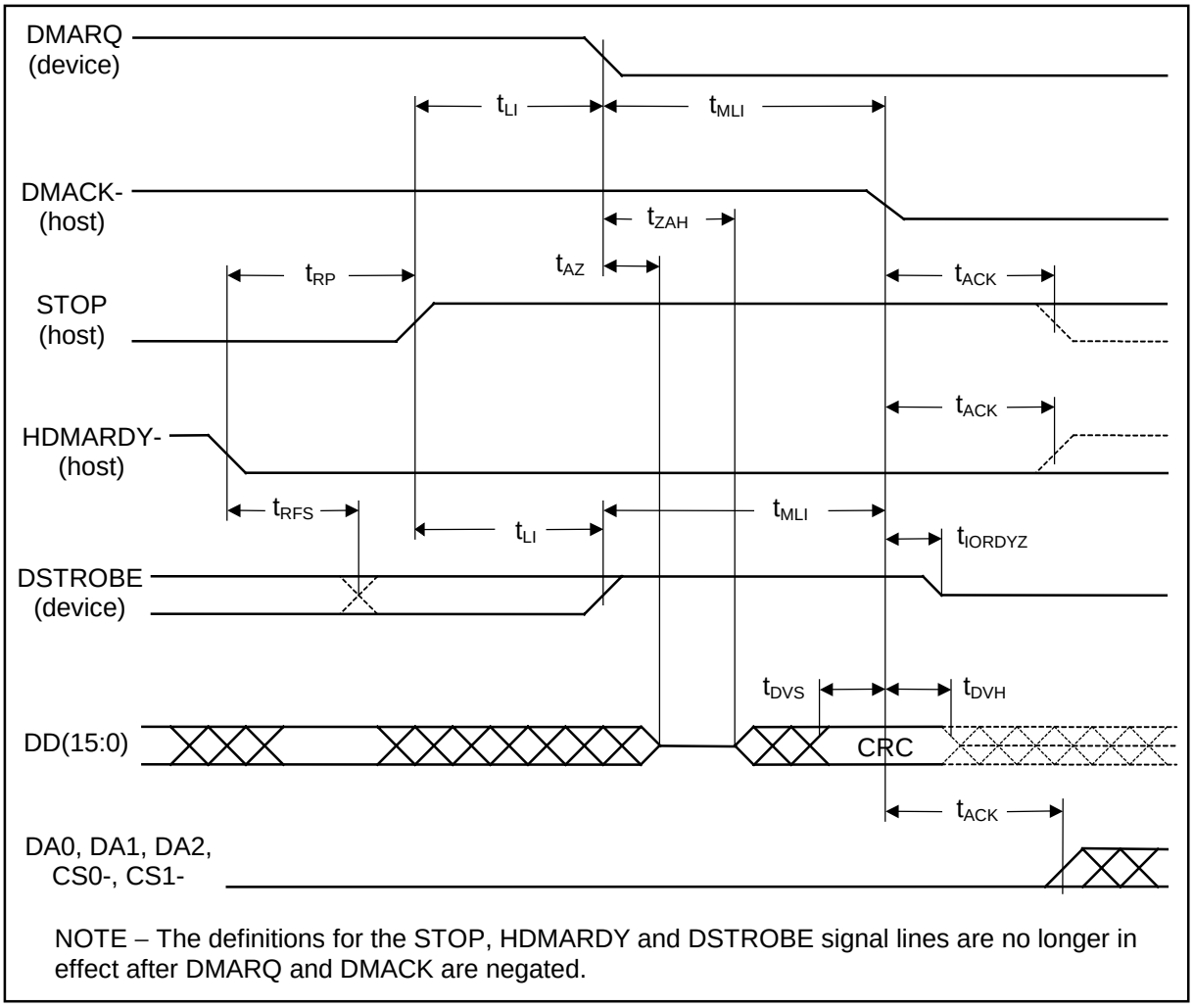


Figure 6-8 Host terminating an Ultra DMA data in burst

6.7.4.7 Initiating an Ultra DMA data out burst

The values for the timings for each of the Ultra DMA modes are contained in 6.7.4.2.

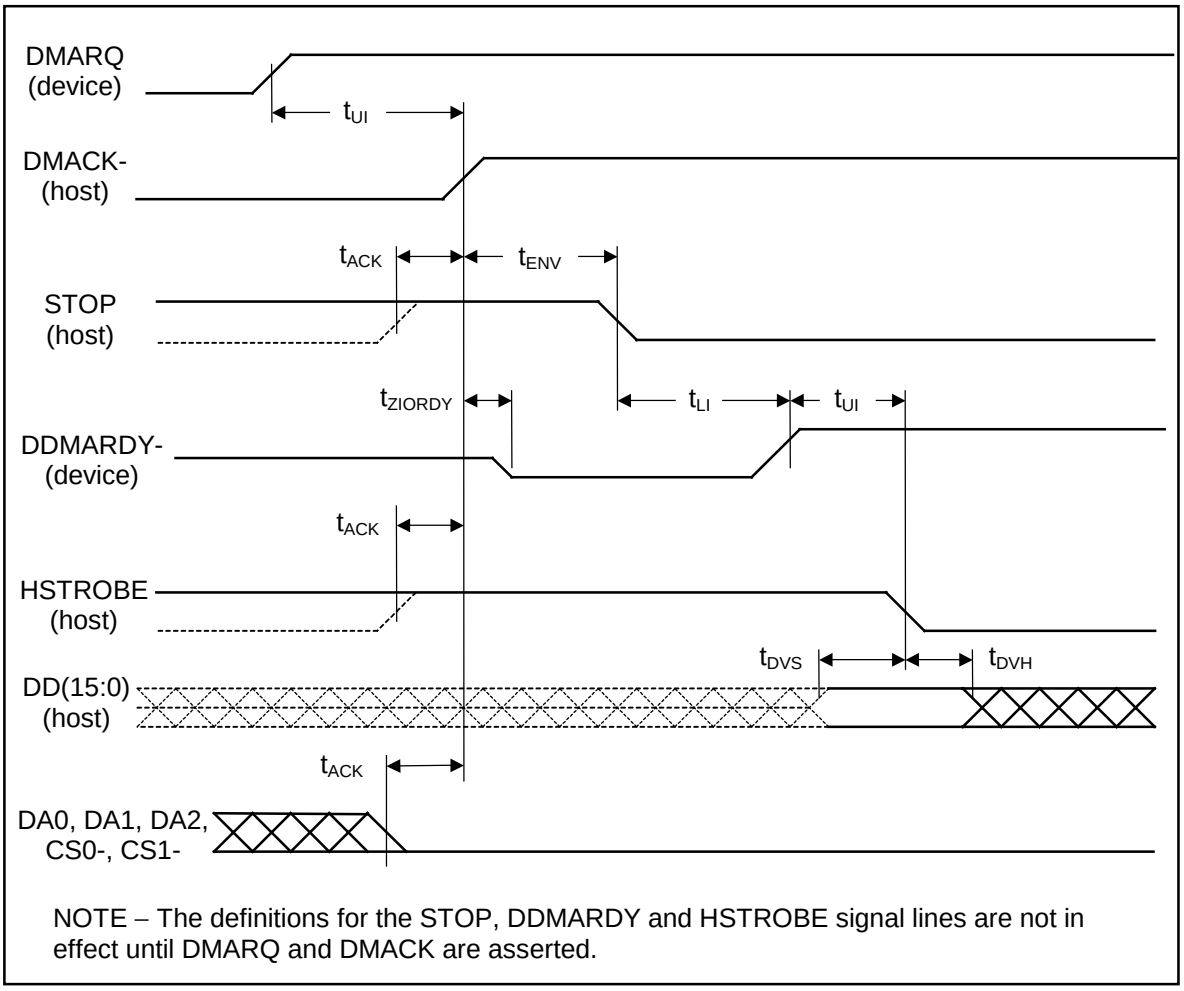


Figure 6-9 Initiating an Ultra DMA data out burst

6.7.4.8 Sustained Ultra DMA data out burst

The values for the timings for each of the Ultra DMA modes are contained in 6.7.4.2.

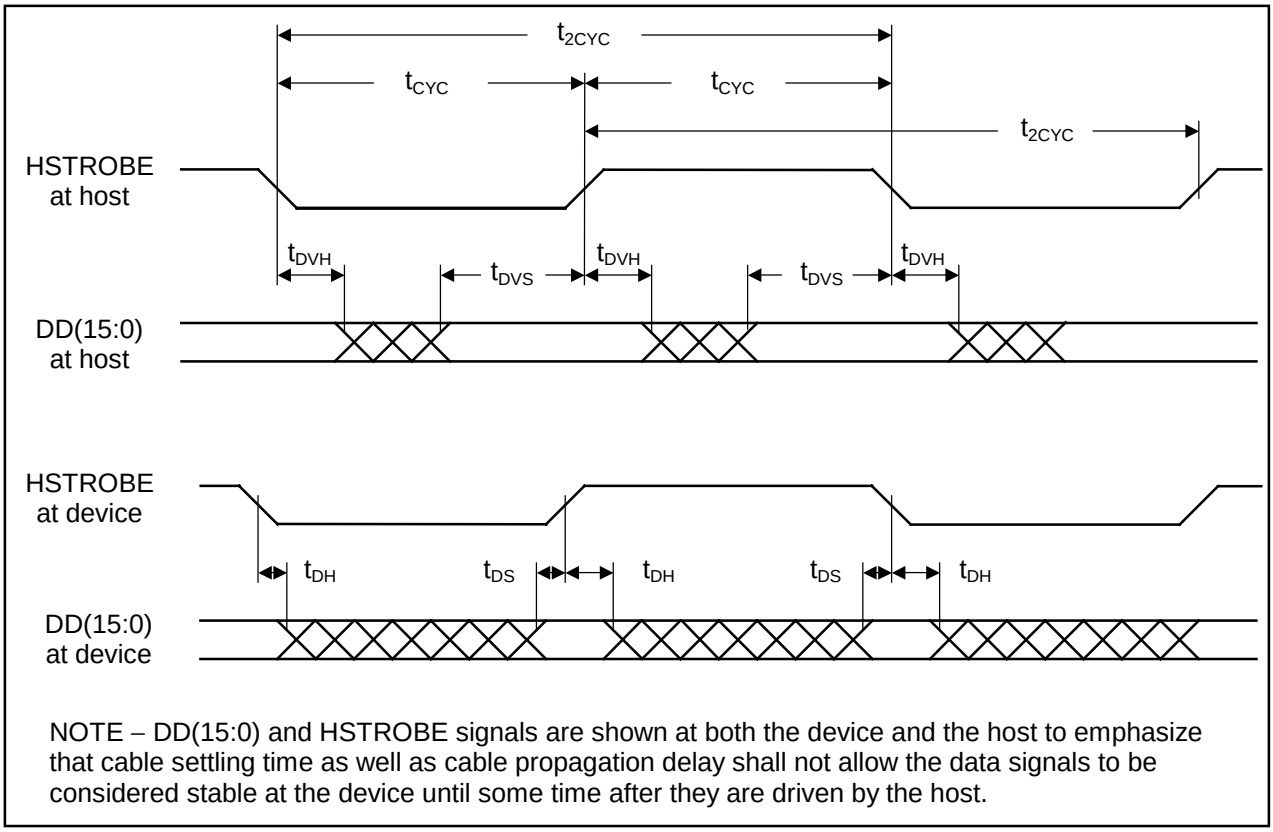


Figure 6-10 Sustained Ultra DMA data out burst

6.7.4.9 Device pausing an Ultra DMA data out burst

The values for the timings for each of the Ultra DMA modes are contained in 6.7.4.2.

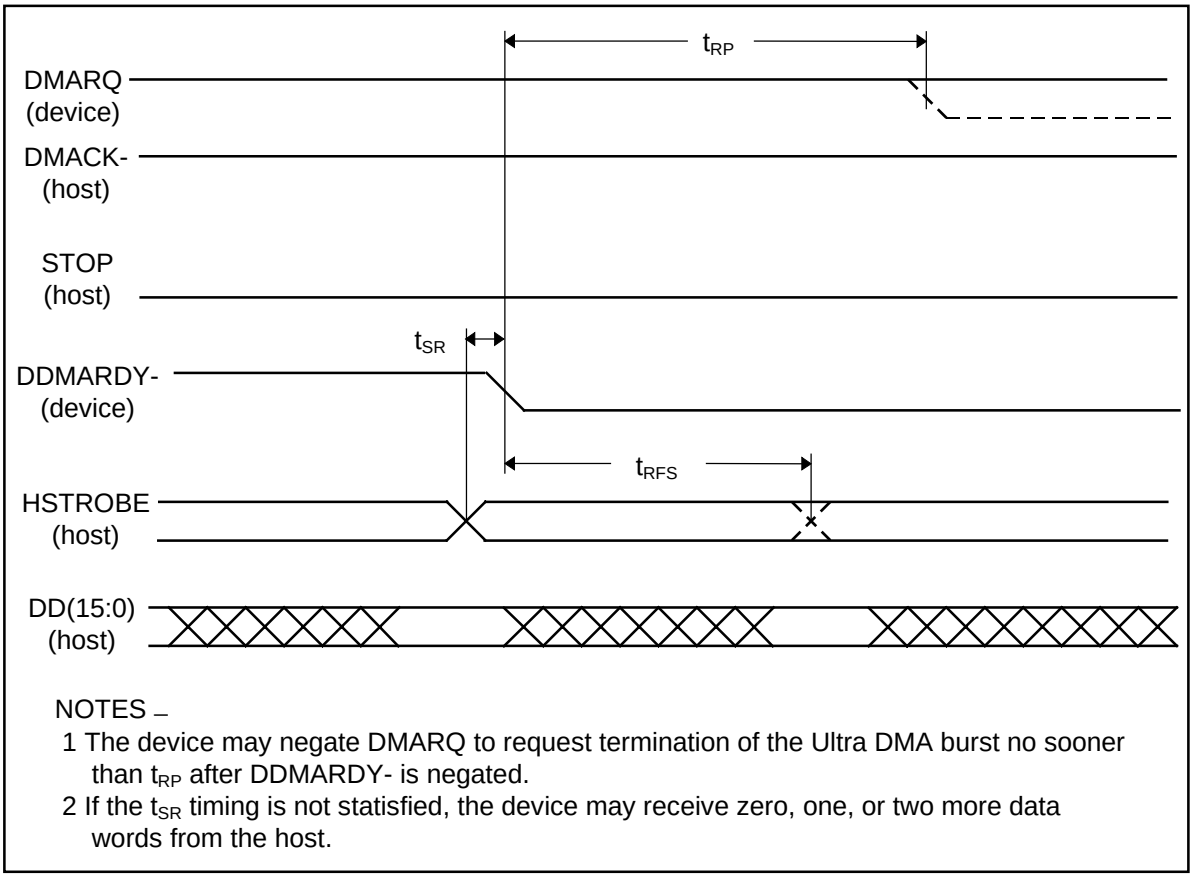


Figure 6-11 Device pausing an Ultra DMA data out burst

6.7.4.10 Host terminating an Ultra DMA data out burst

The values for the timings for each of the Ultra DMA modes are contained in 6.7.4.2.

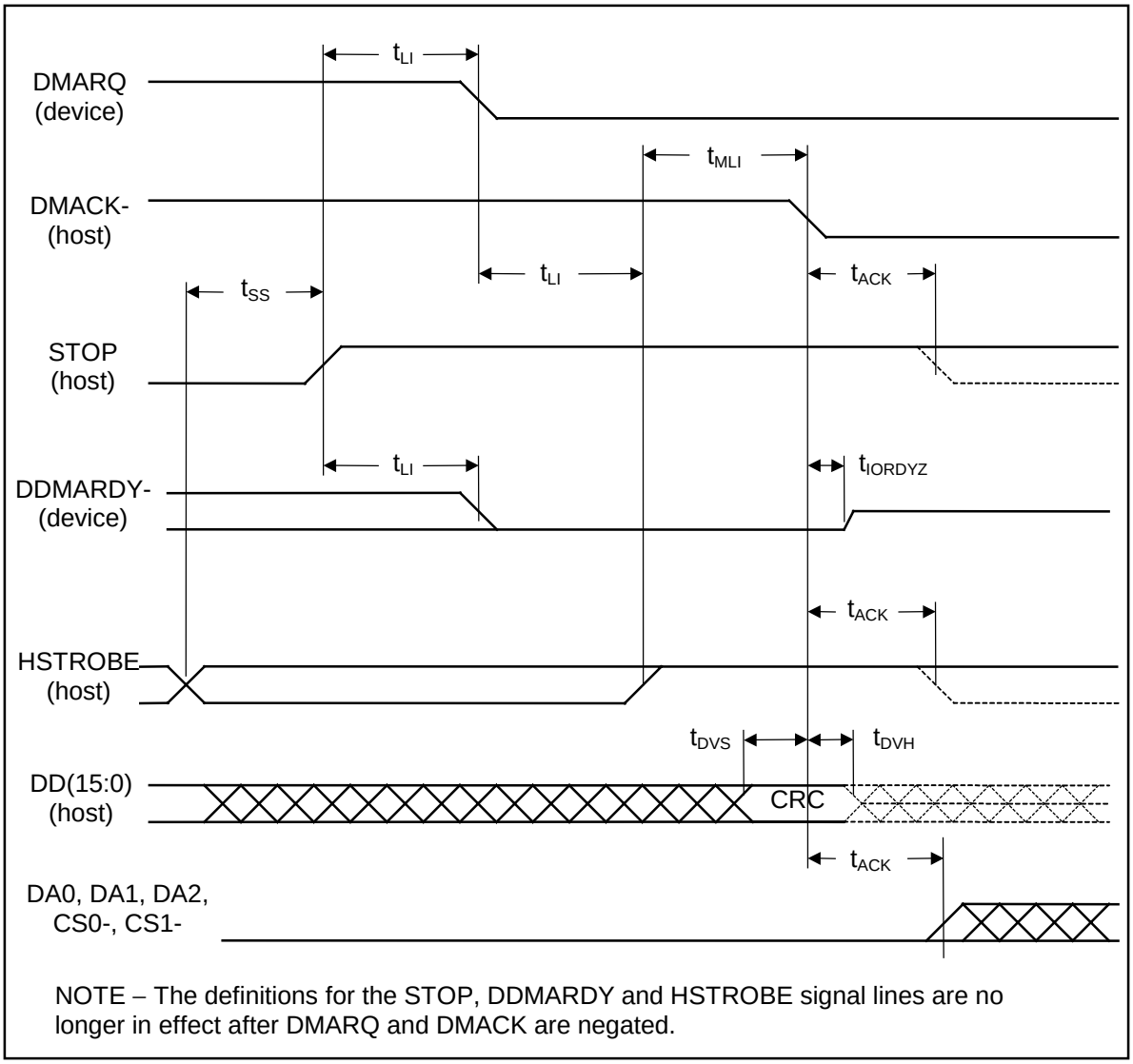


Figure 6-12 Host terminating an Ultra DMA data out burst

6.7.4.11 Device terminating an Ultra DMA data out burst

The values for the timings for each of the Ultra DMA modes are contained in 6.7.4.2.

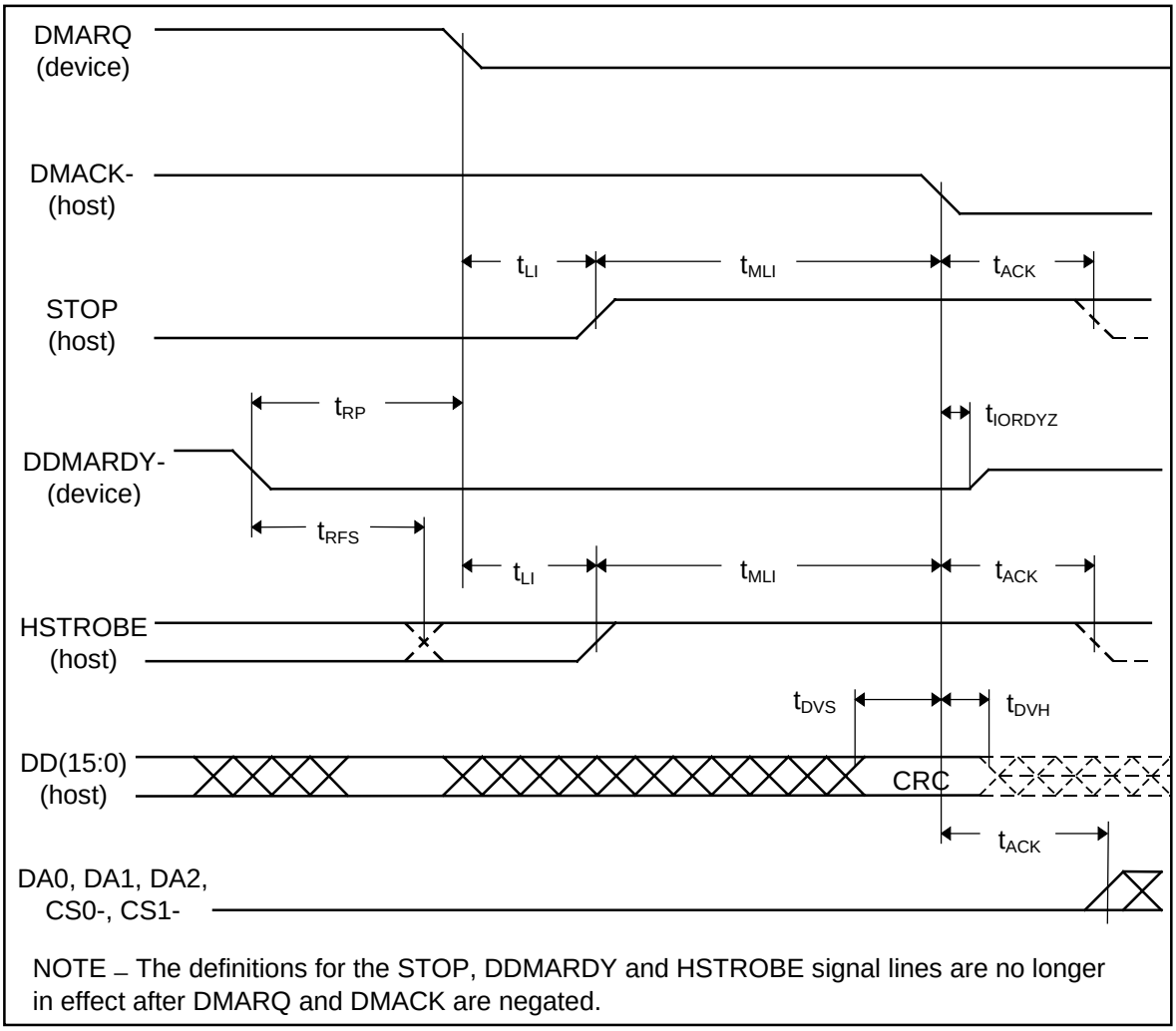


Figure 6-13 Device terminating an Ultra DMA data out burst

CHAPTER 7 MAINTENANCE

7.1 General Information

Samsung's SpinPoint V40 hard disk drives achieve high reliability through their mechanical design and extensive use of microelectronics. Their design allows fast, easy sub-assembly replacement without adjustments, greatly reducing the amount of downtime required for unscheduled repairs.

7.2 Maintenance Precautions

When servicing a drive, the service technician should observe the following precautions to avoid damage to the drive or personal injury.

(1) Do not attempt to open the sealed compartment of the SpinPoint V40, as this will void the warranty and contaminate the media.

(2) Do not lift the SpinPoint V40 by the bezel or by the PCB.

(3) Avoid harsh shocks or vibration to the drive at all times.

(4) Avoid static discharge when handling the SpinPoint V40 drives

(5) Do not touch the components on the PCB.

(6) Observe the environmental limits specified for this product, as listed in section 3.6.

(7) If it becomes necessary to move your computer system, turn off the power to automatically park the heads. Parking the heads moves the heads to a safe, non-data landing zone and locks the heads in place. This helps prevent the media and the heads from accidental damage due to vibration, moving or shipping. Do not move the drive for 20 seconds after removing DC power to ensure that the actuator is completely locked.

Back up your data regularly. Samsung assumes no responsibility for loss of data. For information about back-up and restore procedures, consult your DOS manual. There are also a number of utility programs available that you can use to back up your data.

7.3 Service And Repair

The service and repair of the SpinPoint V40 can be done at a Samsung Service Center. Please contact your representative for warranty information and service/return procedures.