SiI 141B PanelLink® Digital Receiver

May 2001

General Description

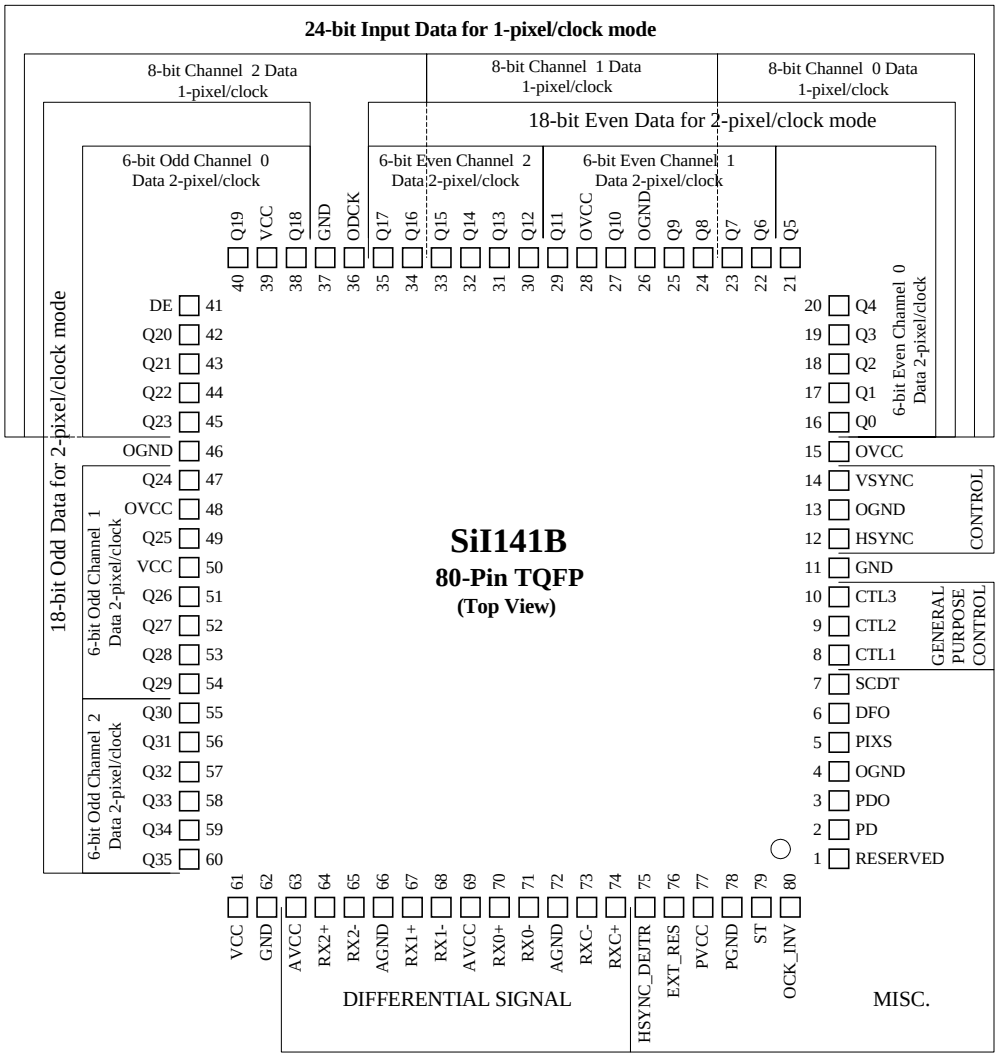
The SiI 141B uses PanelLink Digital technology to support displays ranging from VGA to High Refresh XGA (25-86 MHz), which is ideal for LCD desktop monitor applications. With a flexible single or dual pixel out interface and selectable output drive, the SiI 141B receiver supports up to true color panels (24 bit/pixel, 16.7M colors) in 1 pixel/clock mode (18 bit/pixel in 2 pixel/clock mode). PanelLink also features an inter-pair skew tolerance up to 1 full input clock cycle. The SiI 141B is pin for pin compatible with the SiI 141 but incorporates a number of enhancements. These include an improved jitter tolerant PLL design, new HSYNC filter and power down when the clock is inactive. All PanelLink products are designed on a scaleable CMOS architecture to support future performance requirements while maintaining the same logical interface. System designers can be assured that the interface will be fixed through a number of technology and performance generations.

PanelLink Digital technology simplifies PC design by resolving many of the system level issues associated with high-speed digital design, providing the system designer with a digital interface solution that is quicker to market and lower in cost.

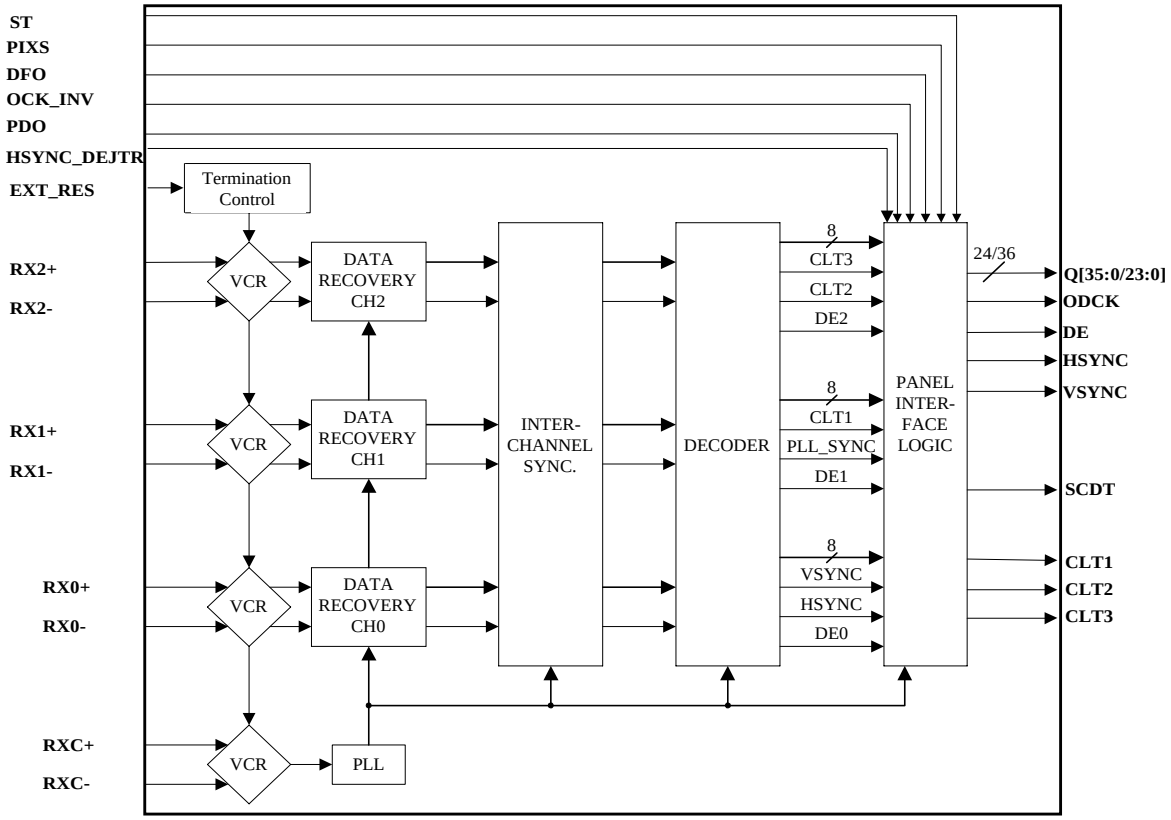
Features

- Scaleable Bandwidth: 25-86 MHz (VGA to High Refresh XGA)
- Low Power: 3.3V core operation & power-down mode
- Automatic power down when clock is inactive
- High Skew Tolerance: 1 full input clock cycle (15ns at 65 MHz)
- Pin-compatible with Si‡ 101, Si‡ 141
- Sync Detect: for Plug & Display “Hot Plugging”
- Cable Distance Support: over 5m with twisted-pair, fiber-optics ready
- Compliant with DVI 1.0 (DVI is backwards compatible with VESA® P&D™ and DFP)

SiI 141B Pin Diagram



Functional Block Diagram



Absolute Maximum Conditions

Note: Permanent device damage may occur if absolute maximum conditions are exceeded.
Functional operation should be restricted to the conditions described under Normal Operating Conditions.

Symbol	Parameter	Min	Typ	Max	Units
V_{CC}	Supply Voltage 3.3V	-0.3		4.0	V
V_I	Input Voltage	-0.3		V_{CC}+ 0.3	V
V_O	Output Voltage	-0.3		V_{CC}+ 0.3	V
T_A	Ambient Temperature (with power applied)	-25		105	°C
T_{STG}	Storage Temperature	-65		150	°C
θ_{JA}	Thermal Resistance (Junction to Ambient)		45		°C /W

Normal Operating Conditions

Symbol	Parameter	Min	Typ	Max	Units
V_{CC}	Supply Voltage	3.0	3.3	3.6	V
V_{CCN}	Supply Voltage Noise			100	mV_{P-P}
T_A	Ambient Temperature (with power applied)	0	25	70	°C

DC Digital I/O Specifications

Under normal operating conditions unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IH}	High-level Input Voltage		2			V
V_{IL}	Low-level Input Voltage				0.8	V
V_{OH}	High-level Output Voltage		2.4			V
V_{OL}	Low-level Output Voltage				0.4	V
V_{CINL}	Input Clamp Voltage[1]	I_{CL} = -18mA			GND -0.8	V
V_{CIPL}	Input Clamp Voltage[1]	I_{CL} = 18mA			IVCC + 0.8	V
V_{CONL}	Output Clamp Voltage[1]	I_{CL} = -18mA			GND -0.8	V
V_{COPL}	Output Clamp Voltage[1]	I_{CL} = 18mA			OVCC + 0.8	V
I_{IL}	Input Leakage Current		-10		10	µA

Note: [1] Guaranteed by design. Voltage undershoot or overshoot cannot exceed absolute maximum conditions for a pulse of greater than 3 ns or one third of the clock cycle.

DC Specifications

Under normal operating conditions unless otherwise specified. Low drive strength values, when ST=0, are shown in brackets.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{OHD}	Output High Drive Data and Controls	V_{OUT} = 2.4 ST=1 ST=0	 5.0 2.5	 10.3 5.2	 17.6 8.8	mA
I_{OLD}	Output Low Drive Data and Controls	V_{OUT} = 0.4 ST=1 ST=0	 -5.5 -2.8	 -8.3 -4.2	 -11.2 -5.6	mA
I_{OHC}	ODCK High Drive	V_{OUT} = 2.4 ST=1 ST=0	 10.1 5.0	 20.6 10.3	 35.1 17.6	mA
I_{OLC}	ODCK Low Drive	V_{OUT} = 2.0 ST=1 ST=0	 -11.1 -5.5	 -16.7 -8.3	 -22.4 -11.2	mA
V_{ID}	Differential Input Voltage Single Ended Amplitude		75		1000	mV
I_{PDL}	Output leakage current to ground in high impedance mode (PD, PDO = LOW)				10	µA
I_{PD}	Power-down Current[1]			50	100	µA
I_{CLKI}	Power-down Current	RXC± Inactive		4	7	mA
I_{PDO}	Power-down-output Current			125	155	mA
I_{CCR}	Receiver Supply Current ODCK=86MHz, 1-pixel/clock mode[2]	C_{LOAD} = 10pF R_{EXT_SWING} = 510 Ω Typical Pattern[3]		157	182	mA
		C_{LOAD} = 10pF R_{EXT_SWING} = 510 Ω Worst Case Pattern[4]		172	194	mA

Notes:
1 The transmitter must be in power-down mode, powered off, or disconnected for the current to be under this maximum.
2 For worst case I/O power consumption.
3 The Typical Pattern contains a gray scale area, checkerboard area, and text.
4 Black and white checkerboard pattern, each checker is one pixel wide.

AC Specifications

Under normal operating conditions unless otherwise specified. Low drive strength values, when ST=0, are given below.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
T_{DPS}	Intra-Pair (+ to -) Differential Input Skew	86 MHz			470	ps
T_{CCS}	Channel to Channel Differential Input Skew	86 MHz			7	ns
T_{IJIT}	Worst Case Differential Input Clock Jitter tolerance[1,2]	65 MHz			465	ps
		86 MHz			350	ps
D_{LHT}	Low-to-High Transition Time: Data and Controls (43 MHz, 2-pixel/clock, PIXS=1)	C_L = 10pF; ST = 1			3.5	ns
		C_L = 5pF; ST = 0			4.5	ns
	Low-to-High Transition Time: Data and Controls (65 MHz, 1-pixel/clock, PIXS=0)	C_L = 10pF; ST = 1			3.5	ns
		C_L = 5pF; ST = 0			4.5	ns
	Low-to-High Transition Time: ODCK (43 MHz, 2-pixel/clock, PIXS=1)	C_L = 10pF; ST = 1			1.6	ns
		C_L = 5pF; ST = 0			2.1	ns
	Low-to-High Transition Time: ODCK (65 MHz, 1-pixel/clock, PIXS=0)	C_L = 10pF; ST = 1			1.6	ns
		C_L = 5pF; ST = 0			2.1	ns
D_{HLT}	High-to-Low Transition Time: Data and Controls (43 MHz, 2-pixel/clock, PIXS=1)	C_L = 10pF; ST = 1			3.0	ns
		C_L = 5pF; ST = 0			4.2	ns
	High-to-Low Transition Time: Data and Controls (65 MHz, 1-pixel/clock, PIXS=0)	C_L = 10pF; ST = 1			3.0	ns
		C_L = 5pF; ST = 0			4.2	ns
	High-to-Low Transition Time: ODCK (43 MHz, 1-pixel/clock, PIXS=0)	C_L = 10pF; ST = 1			1.5	ns
		C_L = 5pF; ST = 0			1.9	ns
	High-to-Low Transition Time: ODCK (65 MHz, 1-pixel/clock, PIXS=0)	C_L = 10pF; ST = 1			1.5	ns
		C_L = 5pF; ST = 0			1.9	ns
T_{SETUP}	Data, DE, VSYNC, HSYNC, and CTL[3:1] Setup Time to ODCK falling edge (OCK_INV = 0) or to ODCK rising edge (OCK_INV = 1) *OCK_INV = 1	C_L = 10pF; ST = 1	3.6 3.0*			ns
		C_L = 5pF; ST = 0	18.4 19.0*			ns
T_{HOLD}	Data, DE, VSYNC, HSYNC, and CTL[3:1] Hold Time from ODCK falling edge, (OCK_INV = 0) or from ODCK rising edge (OCK_INV = 1) *OCK_INV = 0	C_L = 10pF; ST = 1	8.0 8.4*			ns
		C_L = 5pF; ST = 0	24.0 24.5*			ns
R_{CIP}	ODCK Cycle Time (1 pixel/clock)		11.6		40	ns
F_{CIP}	ODCK Frequency (1 pixel/clock)		25		86	MHz
R_{CIP}	ODCK Cycle Time (2 pixels/clock)		23.3		80	ns
F_{CIP}	ODCK Frequency (2 pixels/clock)		12.5		43	MHz
R_{CIH}	ODCK High Time 65 MHz, One Pixel / Clock, PIXS = 0 [3]	C_L = 10pF, ST=1 C_L = 5pF, ST=0	5.0 4.4			ns
	43 MHz, Two Pixel / Clock, PIXS = 1 [3]	C_L = 10pF, ST=1 C_L = 5pF, ST=0	9.0 8.2			ns
R_{CIL}	ODCK Low Time 65 MHz, One Pixel / Clock, PIXS = 0 [3]	C_L = 10pF, ST=1 C_L = 5pF, ST=0	6 5			ns
	43 MHz, Two Pixel / Clock, PIXS = 1 [3]	C_L = 10pF, ST=1 C_L = 5pF, ST=0	9 9			ns
T_{HSC}	Link disabled (DE inactive) to SCDT low[1]			160		ms
	Link disabled (Tx power down) to SCDT low [5]			200	250	ms
T_{FSC}	Link enabled (DE active) to SCDT high[6]				40	Falling DE edges
T_{CLKPD}	Delay from RXC+/- Inactive to high impedance outputs	RXC+/- = 25MHz			10	µs
T_{CLKPU}	Delay from RXC+/- active to data active	RXC+/- = 25MHz			100	µs
T_{PDL}	Delay from PD/ PDO Low to high impedance outputs				8	ns

Notes:
1 Jitter defined as per DVI 1.0 Specification, Section 4.6 *Jitter Specification*.
2 Jitter measured with Clock Recovery Unit as per DVI 1.0 Specification, Section 4.7 *Electrical Measurement Procedures*.
3 Output clock duty cycle is independent of the differential input clock duty cycle and the IDCK duty cycle.
4 The setup and hold timing for the data and controls relative to the ODCK rising edge (OCK_INV=1) is by design the same as the falling edge timing.
5 Measured when transmitter was powered down (see SiI/AN-0005 "PanelLink Basic Design /Application Guide," Section 2.4).
6 Refer to the transmitter datasheet for minimum DE high and low time
7 Data is active (i.e. not tri-stated) but not valid yet. Data and controls are valid only when SCDT goes high. See T_{FSC} and Figure 7.

Timing Diagrams

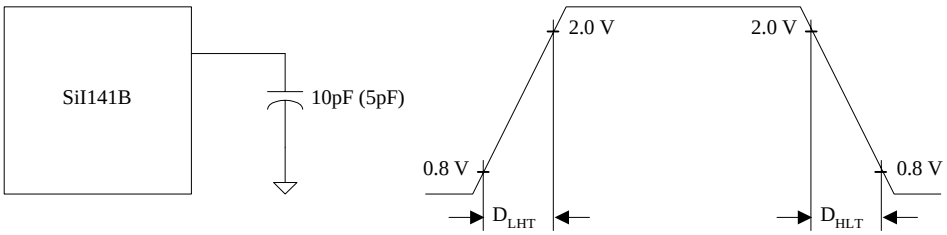


Figure 1. Digital Output Transition Times

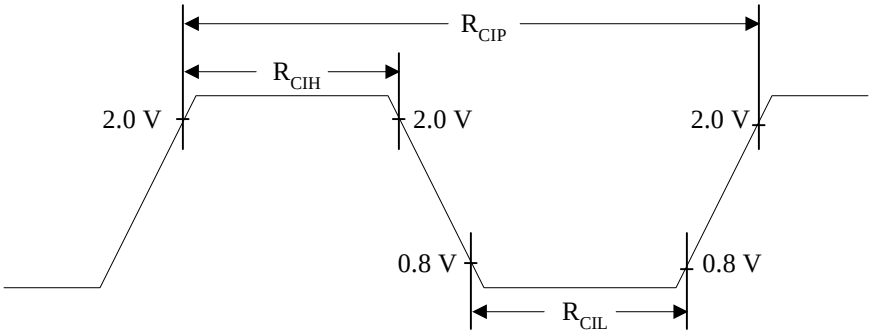


Figure 2. Receiver Clock Cycle/High/Low Times

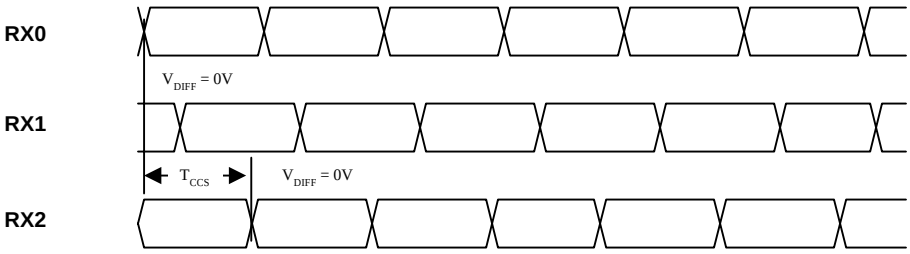


Figure 3. Channel-to-Channel Skew Timing

Output Timing

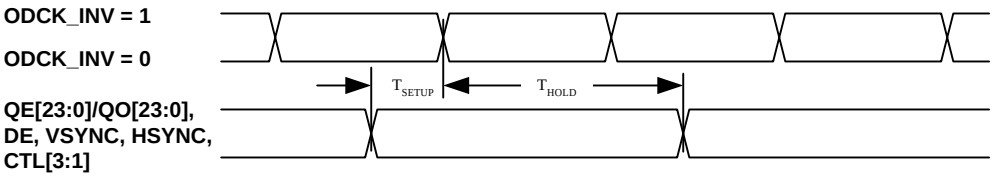


Figure 4. Output Data Setup/Hold Times to ODCK

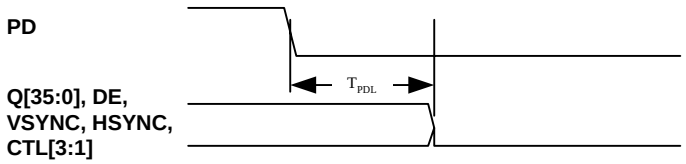


Figure 5. Output Signals Disabled Timing from PD Active

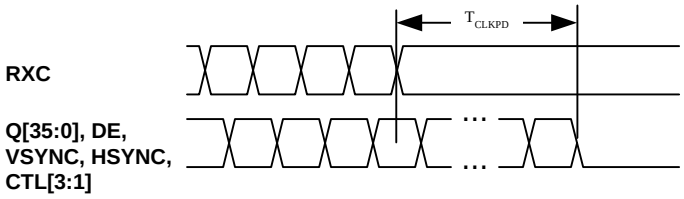


Figure 6. Output Signals Disabled Timing from Clock Inactive

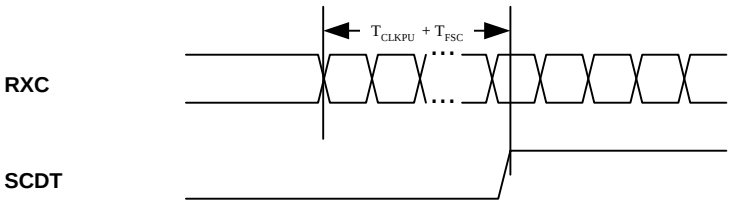


Figure 7. Wake-up on Clock Detect

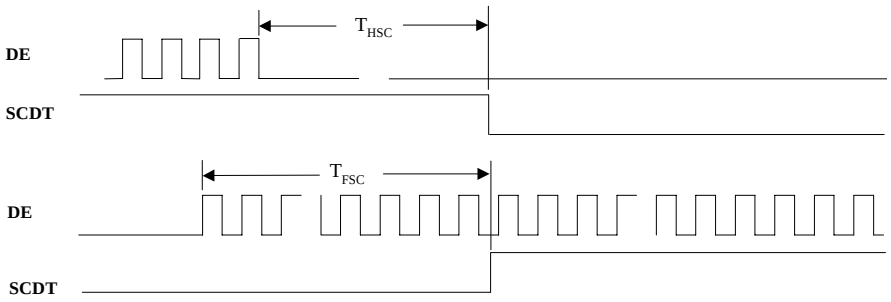


Figure 8. SCDT Timing from DE Inactive/Active

Output Pin Description

Pin Name	Pin #	Type	Description
Q35 – Q0	See SiI 141B Pin Diagram	Out	Output Data [35:0]. Output data is synchronized with output data clock (ODCK). When PIXS is low Q35-Q24 are low and Q23-Q0 output 24-bit/pixel data. When PIXS is high Q17-Q0 output the even numbered pixels (pixel 0, 2, 4, ... , etc.) and Q35-Q18 output the odd numbered pixels (pixel 1, 3, 5, ... , etc.). Refer to the TFT Signal Mapping (SiI/AN-0008) and DSTN Signal Mapping (SiI/AN-0007) application notes which tabulate the relationship between the input data to the transmitter and output data from the receiver. A low level on PD or PDO will put the output drivers into a high impedance (tri-state) mode. A weak internal pull-down device brings each output to ground.
ODCK	36	Out	Output Data Clock. A low level on PD or PDO will put the output drivers into a high impedance (tri-state) mode. A weak internal pull-down device brings each output to ground.
DE	41	Out	Output Data Enable. A low level on PD or PDO will put the output drivers into a high impedance (tri-state) mode. A weak internal pull-down device brings each output to ground.
HSYNC	12	Out	Horizontal Sync output control signal.
VSYNC	14	Out	Vertical Sync output control signal.
CTL1	8	Out	General output control signal 1. This pin is **not** controlled by PDO.
CTL2	9	Out	General output control signal 2
CTL3	10	Out	General output control signal 3. A low level on PD or PDO will put the output drivers into a high impedance (tri-state) mode. A weak internal pull-down device brings each output to ground.

Configuration Pin Description

Pin Name	Pin #	Type	Description
OCK_INV	80	In	ODCK Polarity. A low level selects normal ODCK output, which enables data latching on the falling edge. A high level (3.3V) selects inverted ODCK output, which enables data latching on the rising edge. Both conditions are for color TFT panel support. For color 24-bit DSTN panel support, please refer to the DSTN Signal Mapping (SiI/AN-0008-A) application note.
PIXS	5	In	Pixel Select. A low level indicates that output data is one pixel (up to 24-bit) per clock and a high level (3.3V) indicates that output data is two pixels (up to 36-bit) per clock.
DF0	6	In	Output Data Format. This pin controls clock and data output format. A low level indicates that ODCK runs continuously for color TFT panel support and a high level (3.3V) indicates that ODCK is stopped (LOW) for color 24-bit DSTN panel support when DE is low. Refer to the TFT Signal Mapping (SiI/AN-0007-A) and DSTN Signal Mapping (SiI/AN-0008-A) application notes for a table on TFT or DSTN panel support.
HSYNC_DEJTR	75	In	A low level enables the HSYNC de-jitter circuitry. A high level disables the de-jitter circuitry. If left unconnected, the circuitry defaults to disabled.
ST	79	In	Output Driver Strength. A low level indicates low drive. A high level indicates high drive.

Power Management Pin Description

Pin Name	Pin #	Type	Description
SCDT	7	Out	SyncDetect. A high level is output when DE is toggling. A low level is output when DE is inactive. See page 9.
PD	2	In	Power Down (active low). A high level (3.3V) indicates normal operation and a low level indicates power down mode. During power down mode all internal circuitry is powered down and digital I/O are set the same as when PDO is asserted. (see PDO pin description).
PDO	3	In	Power Down Output (active low). A high level indicates normal operation. A low level puts the output drivers only into a high impedance (tri-state) mode. A weak internal pull-down device brings each output to ground. There is an internal pull-up resistor on PDO that defaults the chip to normal operation if left unconnected. SCDT and CTL1 are not tri-stated by this pin. See explanation of clock detect on page 8-9.

Differential Signal Data Pin Description

Pin Name	Pin #	Type	Description
RX0+	70	Analog	TMDS Low Voltage Differential Signal input data pairs.
RX0-	71		
RX1+	67		
RX1-	68		
RX2+	64		
RX2-	65		
RXC+	74	Analog	TMDS Low Voltage Differential Signal input clock pair.
RXC-	73		
EXT_RES	76	Analog	Impedance Matching Control. Resistor value should be ten times the characteristic impedance of the cable. In the common case of 50Ω transmission line, an external 530Ω resistor must be connected between AVCC and this pin.

Reserved Pin Description

Pin Name	Pin #	Type	Description
RSVD	1	Out	This signal must be left unconnected.

Power and Ground Pin Description

Pin Name	Pin #	Type	Description
VCC	39	Power	Core VCC, must be set to 3.3V.
	50		
	61		
GND	11	Ground	Digital GND.
	37		
	62		
OVCC	15	Power	Output VCC, must be set to 3.3V.
	28		
	48		
OGND	4	Ground	Output GND.
	13		
	26		
	46		
AVCC	63	Power	Analog VCC, must be set to 3.3V.
	69		
AGND	66	Ground	Analog GND.
	72		
PVCC	77	Power	PLL VCC, must be set to 3.3V.
PGND	78	Ground	PLL GND.

Application Information

The SiI141B is pin for pin compatible with the SiI141 but includes two new features, HSYNC de-jitter and power down when the clock is inactive.

HSYNC de-jitter enables the 141B to operate properly even when the HSYNC signal contains jitter. Pin 75 is used to enable or disable this capability (a reserved pin tied high on the SiI141). Tying this pin low enables the HSYNC de-jitter circuitry while tying it high disables the circuitry. The HSYNC de-jitter circuitry operates normally with most VESA standard timings. Some DOS mode resolutions do not have timings that are a multiple of eight (HSYNC and VSYNC total times and front and back porch times are multiples of eight pixel times). If they are not a multiple of eight, operation is not guaranteed and the HSYNC de-jitter circuitry should be turned off. When HSYNC de-jitter is enabled, the circuitry will introduce anywhere from 0 to 7 CLK delays in the HSYNC signal relative to the output data.

The SiI141B includes a new power saving feature, power down with clock detect circuit. The SiI141B will go into a low power mode when there is no video clock coming from the transmitter. In this mode the entire chip is powered down except the clock detect circuitry. During this mode digital I/O are set to a high impedance (tri-state) mode. A weak internal pull-down device brings each output to ground. The device power down and wake-up times are shown in Figures 6 and 7.

The SiI141B also includes a sync detect feature for pin compatibility with SiI141. In both the SiI141 and SiI141B, SCDT goes low when DE is inactive.

In some application, SCDT is connected to the PDO pin to provide a power savings mode. In others, SCDT is connected to an external circuit to signal when an incoming video signal is available. These external devices may use an internal pull up which can cause problems.

If SCDT is connected to an external circuit which has an internal pull up, then SCDT will not stay low when no video signal is present. The recommended circuit to keep SCDT low is shown Figure 9. For most applications, Silicon Image recommends a pull down resistor of 1.5 KΩ. However, conditions within every design may vary. Please use the calculations below to determine the proper pull-down resistor value.

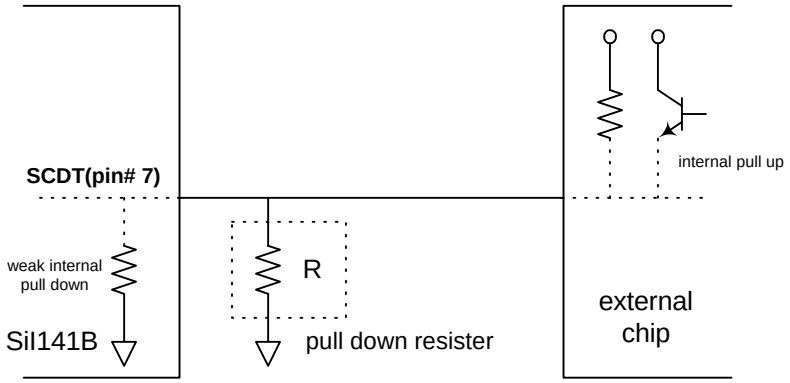


Figure 9. Schematic for SCDT connected to external device with pull up

The external pull down resistor value depends on the pull-up circuit in the external device and can be calculated with Equation [1] and [2] if the pull up is a passive circuit. If the pull up is an active circuit, please consult the manufacture of the other device.

The calculation for the maximum resistor value is shown in the equation [1] below. In powered down mode, low power consumption is achieved by making the resistor value as large as possible. Equation [1] determines the maximum value of R while ensuring that SCDT stays lower than V_{IL} of the external chip when SCDT goes into high impedance. The small current flowing into the SiI141B internal pull down resistor is ignored in equation [1].

Equation [1a]
$$\left[\frac{R}{R_{Pull-Up}+R}\right]\times V_{CCMAX} < V_{IL}$$

Equation [1b]
$$R < \left[\frac{\left(R_{Pull-Up}\times V_{IL}\right)}{\left(V_{cc\max}-V_{IL}\right)}\right]$$

Example :

Pull-up resistor value is 10 KΩ, V_{IL} of external chip is 0.8V, and maximum Vcc is 3.6V

R < 2,857ohms = (10 KΩ x 0.8V) / (3.6V – 0.8V)

The resistor value should be smaller than 2,857 KΩ.

The calculation for the minimum resistor value is shown in the equation [2]. The minimum value is set so the SCDT voltage exceeds V_{IH} of the external chip in normal operation. In equation [2], the small current flowing into the SiI141B internal pull-down resistor is ignored.

Equation [2]

$$R > \left[\frac{V_{CC}}{I_{OHDMIN}} \right] \text{ or } R > \left[\frac{V_{IH}}{I_{OHDMIN}} \right]$$

Example :
When ST(pin# 79) = 1,Vcc = 3.3V
R > 660Ω = Vcc (or V_{IH} of external chip) / Min I_{OHD} = 3.3V / 5.0mA

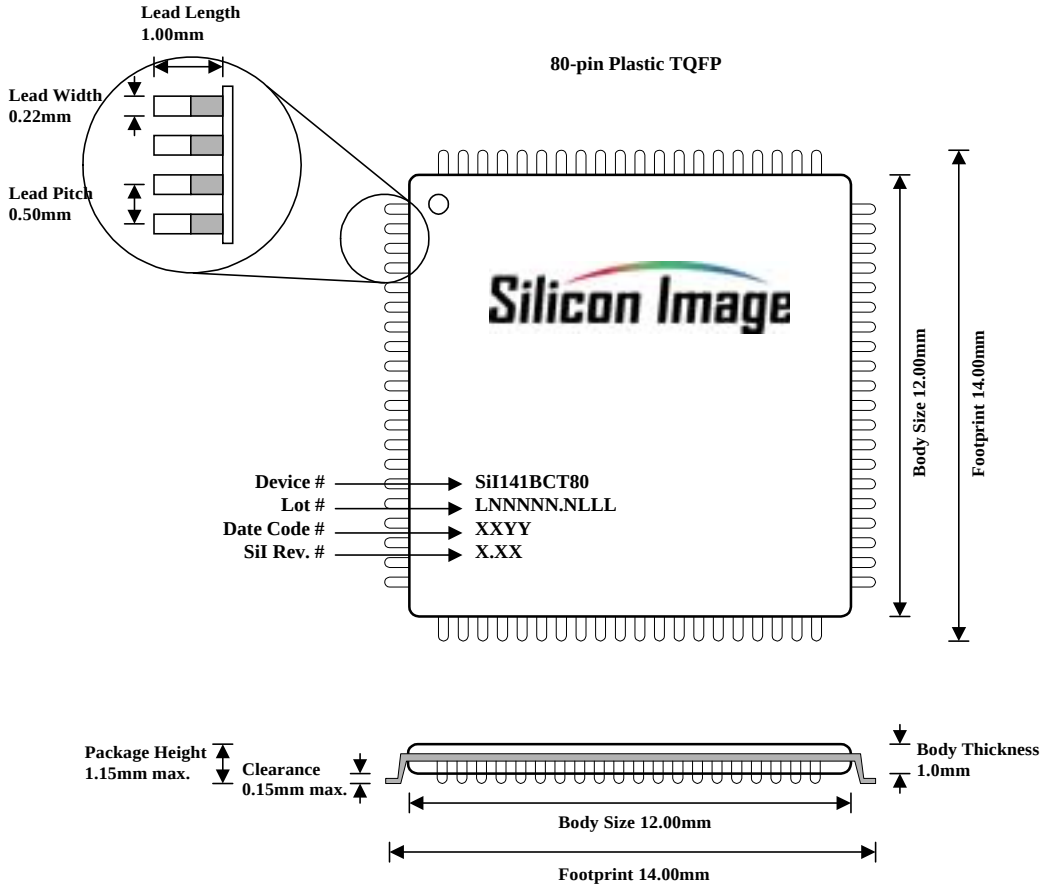
The resistor value should be larger than 660ohms

When ST(pin# 79) = 0,Vcc = 3.3V
R > 1,320Ω = Vcc (or V_{IH} of external chip) / Min I_{OHD} = 3.3V / 2.5mA

The resistor value should be larger than 1,320ohms.

These examples assume Vcc (or V_{IH}) of 3.3V, with a lower V_{IH}, the minimum pull down resistor value may be smaller.

80-pin TQFP Package Dimensions



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Ordering Information

Part Number: SiI141BCT80

Revision History

Revision	Date	Comment
A	11/00	Full release
B	1/01	Added application information concerning HSYNC de-jitter and power down on clock
C	5/01	Updated EXT_RES value for 50Ω transmission line.

Silicon Image, Inc.
1060 E. Arques Ave
Sunnyvale, CA 94086
USA

Tel: 408-616-4000
Fax: 408-830-9530
E-Mail: salessupport@siimage.com
Web: www.siimage.com
www.panellink.com