

OVERVIEW

SiliconDrive combines all the high performance, high reliability, and multiyear lifecycle benefits of the standard SiliconDrive with a comprehensive suite of patented and patent-pending technologies that provide multiple security options to safeguard application data and software IP in embedded systems.

Applications requiring advanced levels of security such as data recorders, wearable and field computers, medical monitoring and diagnostic equipment, POS systems, and voting machines are able to activate security options to protect application data and software IP from theft, falling into the wrong hands from deployments in high-risk areas, corruption, and accidental or malicious overwrites.

PowerArmor prevents data corruption and loss from power disturbances by integrating patented technology into every SiliconDrive.

SiSMART acts as an early warning system to eliminate unscheduled downtime by constantly monitoring and reporting the exact amount of remaining storage system useful life.

SiSecure is a comprehensive suite of user-selectable security technologies that solves the critical need for robust storage security for embedded systems applications that have a small footprint and low-power requirement.

SiSECURE

- PowerArmor Eliminates drive corruption.
- SiZone Data zones with different security parameters.
- SiKey Ties SiliconDrive to a specific host and/or software IP.
- SiProtect Protection software for password-required, read/write, or read-only access.
- SiSweep Ultra-fast data erasure.
- SiPurge Non-recoverable data erasure.

FEATURES

- Integrated PowerArmor, SiSMART, and SiSecure technologies
- Capacity range: 32MB to 8GB
- Supports both 8-bit and 16-bit data register transfers
- Supports dual-voltage 3.3V or 5V interface
- Data reliability <1 error in 10¹⁴ bits read
- MTBF 4,000,000 hours
- ATA-3 compliant
- Industry standard Type I CF form factor
- RoHS 5 of 6 compliant
- Supports PIO modes 0-4 and DMA modes 0-2



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REVISION HISTORY

| Document No. | Release Date | Changes |
|----------------|-------------------|--|
| 3150C-09DSR | February 2, 2009 | Updated: <ul style="list-style-type: none"> "System Reliability" table and changed the name to "Reliability." "Related Documentation" table. Added: <ul style="list-style-type: none"> "Projected Operational Life Span." |
| 3150C-08DSR | June 17, 2008 | Updated: <ul style="list-style-type: none"> "Overview." "SiliconDrive Technology" to "SiSecure." |
| 3150C-07DSR | May 14, 2008 | Updated: <ul style="list-style-type: none"> "Overview." <i>SiliconDrive Secure</i> to <i>SiSecure</i>. SiProtect information. |
| SSDS06-3150C-R | January 28, 2008 | Added a Note below the "DC Characteristics" table. |
| SSDS05-3150C-R | December 11, 2007 | Updated the t_{RWD} Maximum in the "True IDE Multiword DMA Read/Write Access Timing" table. |
| SSDS05-3150C-R | August 1, 2007 | Updated: <ul style="list-style-type: none"> Cylinder Low in the "Task File Register Specification" table. "Sample Label." |
| SSDS04-3150C-R | May 22, 2007 | <ul style="list-style-type: none"> Updated "SiliconDrive Secure Technology." Removed NOP command from the "ATA Command Set" table. |
| SSDS03-3150C-R | February 7, 2007 | Updated: <ul style="list-style-type: none"> V_{IH} symbol from 2.0 to 2.5 in the "DC Characteristics" table. "Common Memory Description and Operation" tables. |
| SSDS02-3150C-R | December 29, 2006 | Updated the -CS0, -CS1 signals in the "Signal Description" table. |
| SSDS01-3150C-R | July 6, 2006 | Updated the temperature in "Environmental Specifications" table. |
| SSDS00-3150C-R | June 8, 2006 | Initial release. |

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PHYSICAL SPECIFICATIONS

The SiliconDrive CF products are offered in an industry-standard Type I form factor. See "Part Numbering" on page 95 for details regarding CF capacities.

PHYSICAL DIMENSIONS

This section provides diagrams that describe the physical dimensions for the CF.

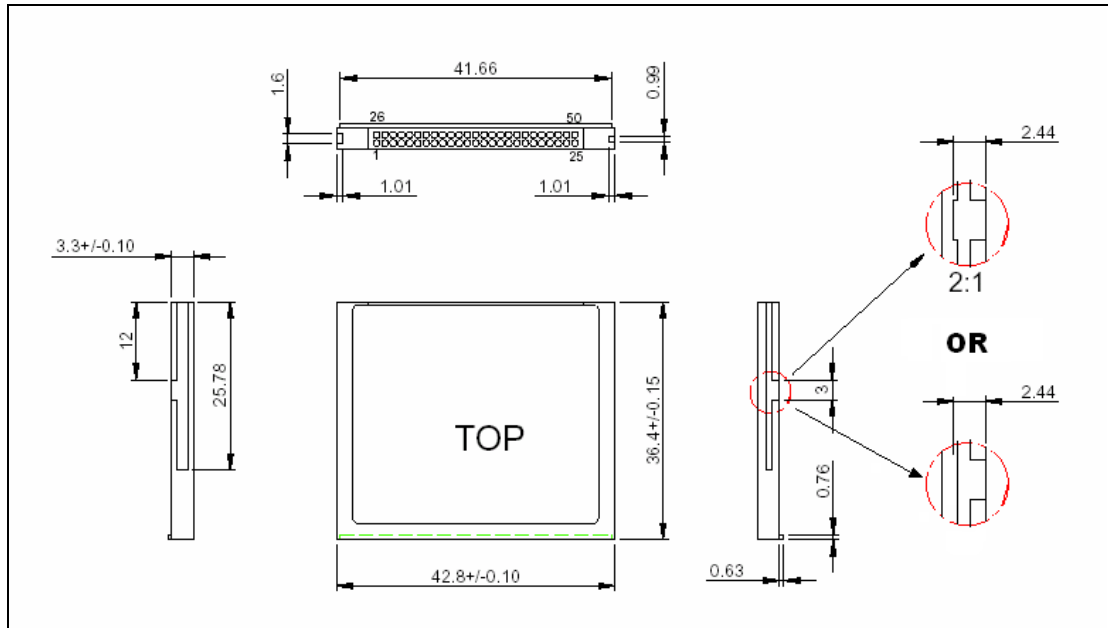


Figure 1: Physical Dimensions

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PRODUCT SPECIFICATIONS

Note: All SiliconDrive CF values quoted are typical at 25°C and nominal supply voltage.

SYSTEM PERFORMANCE

Table 1: System Performance

| | |
|---|---------------|
| Reset to Ready Startup Time (Typical/Maximum) | 200ms/400ms |
| Read Transfer Rate (Typical) | 8MBps |
| Write Transfer Rate (Typical) | 6MBps |
| Burst Transfer Rate | 16.7MBps |
| Controller Overhead (Command to DRQ) | 2ms (maximum) |

SYSTEM POWER REQUIREMENTS

Table 2: System Power Requirements

| | | |
|-------------------------|-----------|------------|
| DC Input Voltage | 3.3 ± 10% | 5.0 ± 10% |
| Sleep (Standby Current) | <0.5mA | <1.0mA |
| Read (Typical/Peak) | 20mA/75mA | 30mA/100mA |
| Write (Typical/Peak) | 30mA/75mA | 40mA/100mA |

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RELIABILITY**Table 3: Reliability**

| | |
|----------------|--|
| MTBF (@ 25°C) | 4,000,000 hours |
| Bit Error Rate | <1 non-recoverable error in 10 ¹⁴ bits read |

PROJECTED OPERATIONAL LIFE SPAN**Table 4: Operational Life Span**

| SiliconDrive Part# | Capacity | Service Life* | GB Written per Day |
|--------------------|----------|---------------|--------------------|
| SSD-C08G-3150 | 8GB | 324.3 Years @ | 135.2GB |
| SSD-C04G-3150 | 4GB | 162.2 Years @ | 135.2GB |
| SSD-C02G-3150 | 2GB | 81.1 Years @ | 135.2GB |
| SSD-C01G-3150 | 1GB | 40.5 Years @ | 135.2GB |
| SSD-C51M-3150 | 512MB | 20.3 Years @ | 135.2GB |
| SSD-C25M-3150 | 256MB | 10.1 Years @ | 135.2GB |
| SSD-C12M-3150 | 128MB | 5.1 Years @ | 135.2GB |
| SSD-C64M-3150 | 64MB | 2.5 Years @ | 135.2GB |
| SSD-C32M-3150 | 32MB | 1.3 Years @ | 135.2GB |

* There are unlimited read cycles. Service life is determined using SiliconSystems' LifeEst calculation at 100% duty cycle with 25% write cycles.

LifeEst is a comprehensive measurement that considers numerous factors to determine the projected life span of a SiliconDrive. A white paper that describes the benefits of LifeEst and how to calculate it can be found at http://www.siliconsystems.com/resources/Documents/Whitepaper/SiliconSystems_NAND_Evolution.pdf.

The actual life of a SiliconDrive is dependant on the customer usage model. SiSMART is a patented technology of SiliconSystems that enables host systems to monitor actual usage of a SiliconDrive in real time. SiSMART measures and reports the remaining life of a SiliconDrive. For more information on SiSMART, refer to the *Eliminating Unscheduled Downtime by Forecasting Useable Life* white paper at http://www.siliconsystems.com/technology/pdfs/SiliconDrive_SiSMART.pdf.

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PRODUCT CAPACITY SPECIFICATIONS

Table 5: Product Capacity Specifications

| Product Capacity | Capacity (Bytes) | Number of Sectors | Number of Cylinders | Number of Heads | Number of Sectors/Track |
|------------------|------------------|-------------------|---------------------|-----------------|-------------------------|
| 32MB | 32,702,464 | 63,872 | 499 | 4 | 32 |
| 64MB | 65,601,536 | 128,128 | 1001 | 4 | 32 |
| 128MB | 130,154,496 | 254,208 | 993 | 8 | 32 |
| 256MB | 260,571,136 | 508,928 | 994 | 16 | 32 |
| 512MB | 521,773,056 | 1,019,088 | 1011 | 16 | 63 |
| 1GB | 1,047,674,880 | 2,046,240 | 2030 | 16 | 63 |
| 2GB | 2,098,446,336 | 4,098,528 | 4066 | 16 | 63 |
| 4GB | 4,224,761,856 | 8,251,488 | 8186 | 16 | 63 |
| 8GB | 8,455,200,768 | 16,514,064 | 16,383* | 16 | 63 |

* = All IDE drives 8GB and larger use 16383 cylinders, 16 heads, and 63 sectors/track due to interface restrictions.

ENVIRONMENTAL SPECIFICATIONS

Table 6: Environmental Specifications

| | |
|-------------|---|
| Temperature | 0°C to 70°C (Commercial) -40°C to 85°C (Industrial) |
| Humidity | 8% to 95% non-condensing |
| Vibration | 16.3gRMS, MIL-STD-810F, Method 514.5, Procedure I, Category 24 |
| Shock | 1000G, Half-sine, 0.5ms Duration 50g Pk, MIL-STD-810F, Method 516.5, Procedure I |
| Altitude | 80,000ft, MIL-STD-810F, Method 500.4, Procedure II |

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ELECTRICAL SPECIFICATION

PIN ASSIGNMENTS

The following table describes the SiliconDrive CF 50-pin IDE connector signals.

Table 7: Pin Assignments

| Pin | PC Card Memory Mode | PC Card I/O Mode | IDE-ATA Mode | Pin | PC Card Memory Mode | PC Card I/O Mode | IDE-ATA Mode |
|-----|---------------------|------------------|-----------------|-----|---------------------|------------------|------------------|
| 1 | GND | GND | GND | 26 | CD1# | CD1# | CD1# |
| 2 | D3 | D3 | D3 | 27 | D11 ¹ | D11 ¹ | D11 ¹ |
| 3 | D4 | D4 | D4 | 28 | D12 ¹ | D12 ¹ | D12 ¹ |
| 4 | D5 | D5 | D5 | 29 | D13 ¹ | D13 ¹ | D13 ¹ |
| 5 | D6 | D6 | D6 | 30 | D14 ¹ | D14 ¹ | D14 ¹ |
| 6 | D7 | D7 | D7 | 31 | D15 ¹ | D15 ¹ | D15 ¹ |
| 7 | CE1# | CE1# | CE1# | 32 | CE2# | CE2# | CE2# |
| 8 | A10 | A10 | A10 | 33 | VS1# | VS1# | VS1# |
| 9 | OE# | OE# | OE# | 34 | IORD# | IORD# | IORD# |
| 10 | A9 | A9 | A9 ² | 35 | IOWR# | IOWR# | IOWR# |
| 11 | A8 | A8 | A8 ² | 36 | WE# | WE# | WE# |
| 12 | A7 | A7 | A7 ² | 37 | RDY/BSY | IREQ | RDY/BSY |
| 13 | V _{CC} | V _{CC} | V _{CC} | 38 | V _{CC} | V _{CC} | V _{CC} |
| 14 | A6 | A6 | A6 ² | 39 | CSEL# | CSEL# | CSEL# |
| 15 | A5 | A5 | A5 ² | 40 | VS2# | VS2# | VS2# |
| 16 | A4 | A4 | A4 ² | 41 | RESET# | RESET# | RESET# |
| 17 | A3 | A3 | A3 ² | 42 | WAIT# | WAIT# | WAIT# |
| 18 | A2 | A2 | A2 | 43 | INPACK# | INPACK# | DMARQ |
| 19 | A1 | A1 | A1 | 44 | REG# | REG# | DMACK# |
| 20 | A0 | A0 | A0 | 45 | BVD2 | SPKR# | DASP# |
| 21 | D0 | D0 | D0 | 46 | BVD1 | STSCHG# | PDIAG# |
| 22 | D1 | D1 | D1 | 47 | D8 ¹ | D8 ¹ | D8 ¹ |
| 23 | D2 | D2 | D2 | 48 | D9 ¹ | D9 ¹ | D9 ¹ |
| 24 | WP | -IOIS16 | -IOIS16 | 49 | D10 ¹ | D10 ¹ | D10 ¹ |
| 25 | CD2# | CD2# | CD2# | 50 | GND | GND | GND |

Notes:

1 = These signals are required only for 16-bit access, and not required when installed in 8-bit systems.

2 = Should be grounded by the host.

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SIGNAL DESCRIPTIONS

Table 8: Signal Descriptions

| Signal Name | Pin | Type | Description |
|-------------------------------|--|------|--|
| A10-A0 | 8, 10, 11, 12, 14, 15, 16, 17, 18, 19, 20 | I | These address lines along with the -REG signal are used to select the following: <ul style="list-style-type: none"> • The I/O port address registers within the SiliconDrive CF • The memory-mapped port address registers within the SiliconDrive CF • A byte in the card's information structure and its configuration control and status registers |
| A10-A0 (PC Card I/O mode) | | | This signal is the same as the PC Card Memory Mode signal. |
| A2-A0 (True IDE mode) | 18, 19, 20 | I | In true IDE mode, only A[2:0] are used to select the one of eight registers in the Task File. The remaining address lines should be grounded by the host. |
| BVD1 (PC Card memory mode) | 46 | I/O | This signal is asserted high, because BVD1 is not supported. |
| -STSCHG (PC Card I/O mode) | | | This signal is asserted low to alert the host to changes in the RDY/-BSY and Write Protect states while the I/O interface is configured. This signal's use is controlled by the Card Configuration and Status register. |
| -PDIAG (True IDE mode) | | | In the true IDE mode, this input/output is the Pass Diagnostic signal in the Master/Slave handshake protocol. |
| BVD2 (PC Card memory mode) | 45 | I/O | This signal is asserted high, as BVD2 is not supported. |

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Table 8: Signal Descriptions (Continued)

| Signal Name | Pin | Type | Description |
|--|--------|------|---|
| -SPKR (PC Card I/O mode) | | | This line is the Binary Audio output from the card. If the Card does not support the Binary Audio function, this line should be held negated. |
| -DASP (True IDE mode) | | | In the true IDE mode, this input/output is the Disk Active/Slave Present signal in the Master/Slave handshake protocol. |
| -CD1, -CD2 (PC Card memory mode) | 26, 25 | O | These Card Detect pins are connected to ground on the SiliconDrive CF, and are used by the host to determine that the SiliconDrive CF is fully inserted into its socket. |
| -CD1, -CD2 (PC Card I/O Mode) | | | This signal is the same for all modes. |
| -CD1, -CD2 (True IDE mode) | | | This signal is the same for all modes. |
| -CE1, -CE2 (PC Card memory mode) Card Enable | 7, 32 | I | <p>These input signals are used both to select the card and to indicate to the card whether a byte or a word operation is being performed.</p> <ul style="list-style-type: none"> -CE2 always accesses the odd byte of the word. -CE1 accesses the even byte or the odd byte of the word depending on A0 and -CE2. <p>A multiplexing scheme based on A0, -CE1, and -CE2 allows 8-bit hosts to access all data on D0-D7. See "Attribute Memory Read Operations" on page 22, "Attribute Memory Write Operations" on page 23, "Common Memory Read Operations" on page 40, and "Common Memory Write Operations" on page 40.</p> |

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Table 8: Signal Descriptions (Continued)

| Signal Name | Pin | Type | Description |
|--|-----|------|---|
| -CE1, -CE2 (PC Card I/O mode) Card Enable | | | This signal is the same as the PC Card Memory Mode signal. See " I/O Space Read Operations " on page 41 and " I/O Space Write Operations " on page 41. |
| -CS0, -CS1 (True IDE mode) | | | In the true IDE mode, -CS0 is the chip select for the task file registers while -CS1 is used to select the Alternate Status register and the Device Control register. |
| -CSEL (PC Card memory mode) | 39 | I | This signal is not used for this mode. |
| -CSEL (PC Card I/O mode) | | | This signal is not used for this mode. |
| -CSEL (True IDE mode) | | | This internally pulled-up signal is used to configure this device as a master or slave when configured in the true IDE mode. When this pin is: <ul style="list-style-type: none"> • Grounded, this device is configured as a master. • Open, this device is configured as a slave. |
| -INPACK (PC Card memory mode) | 43 | O | This signal is not used in this mode. |
| -INPACK (PC Card I/O mode) Input Acknowledge | | | This signal is asserted by the SiliconDrive CF when the card is selected and responding to an I/O read cycle at the address that is on the address bus. This signal is used by the host to control the enabling of any input data buffers between the SiliconDrive CF and the CPU. |

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Table 8: Signal Descriptions (Continued)

| Signal Name | Pin | Type | Description |
|----------------------------------|---|------|--|
| DMARQ (True IDE mode) | 43 | O | In true IDE mode, this signal is used for DMA transfers between the host and device. DMARQ is asserted by the device when the device is ready to transfer data to/from the host. The direction of data transfer is controlled by -IORD and -IOWR. This signal is used in a handshake manner with -DMACK (i.e., the device waits until the host asserts -DMACK before negating DMARQ, and reasserts DMARQ if there is more data to transfer). The DMARQ/-DMACK handshake is used to provide flow control during the transfer. |
| D15-D00 (PC Card memory mode) | 31, 30, 29, 28, 27, 49, 48, 47, 6, 5, 4, 3, 2, 23, 22, 21 | I/O | These lines carry the data, commands, and status information between the host and the controller. <ul style="list-style-type: none"> D00 is the LSB of the word's even byte. D08 is the LSB of the word's odd byte. |
| D15-D00 (PC Card I/O mode) | | | This signal is the same as the PC Card Memory Mode signal. |
| D15-D00 (True IDE mode) | | | In true IDE mode, all Task File operations occur in byte mode on the low-order bus D00-D07, while all data transfers are 16 bits using D00-D15. |
| GND (PC Card memory mode) | 1, 50 | - | Ground. |
| GND (PC Card I/O mode) | | | This signal is the same for all modes. |
| GND (True IDE mode) | | | This signal is the same for all modes. |

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Table 8: Signal Descriptions (Continued)

| Signal Name | Pin | Type | Description |
|--------------------------------|-----|------|--|
| -IORD (PC Card memory mode) | 34 | I | This signal is not used in this mode. |
| -IORD (PC Card I/O mode) | | | This is an I/O read strobe generated by the host. This signal gates I/O data onto the bus from the SiliconDrive CF when the card is configured to use the I/O interface. |
| -IORD (True IDE mode) | | | In true IDE mode, this signal has the same function as the PC Card I/O mode. |
| -IOWR (PC Card memory mode) | 35 | I | This signal is not used in this mode. |
| -IOWR (PC Card I/O mode) | | | The I/O write strobe pulse is used to clock I/O data on the Card data bus into the SiliconDrive CF controller registers when the SiliconDrive CF is configured to use the I/O interface. The clocking occurs on the negative-to-positive edge of the signal (the trailing edge). |
| -IOWR (True IDE mode) | | | In true IDE mode, this signal has the same function as the PC Card I/O mode. |
| -OE (PC Card memory mode) | 9 | I | This is an output enable strobe generated by the host interface, which is used to read: <ul style="list-style-type: none"> • Data from the SiliconDrive CF in memory mode. • The CIS and configuration registers. |
| -OE (PC Card I/O mode) | | | In PC Card I/O mode, this signal is used to read the CIS and configuration registers. |

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Table 8: Signal Descriptions (Continued)

| Signal Name | Pin | Type | Description |
|--|-----|------|--|
| -ATA SEL (True IDE mode) | | | To enable true IDE mode, this input should be grounded by the host. |
| -RDY/-BSY (PC Card memory mode) | 37 | O | <p>In memory mode, this signal is:</p> <ul style="list-style-type: none"> • Set high when the SiliconDrive CF is ready to accept a new data transfer operation. • Held low when the card is busy. <p>The host memory card socket must provide a pull-up resistor.</p> <p>At power-up and reset, the RDY/-BSY signal is held low (busy) until the SiliconDrive CF has completed its power-up or reset function. No access of any type should be made to the SiliconDrive CF during this time. The RDY/-BSY signal is held high (disabled from being busy) whenever the SiliconDrive CF has been powered up with +RESET continuously disconnected or asserted.</p> |
| -IREQ (PC Card I/O mode) Input Acknowledge | | | I/O Operation. After the SiliconDrive CF has been configured for I/O operation, this signal is used as -Interrupt Request. This line is strobed low to generate a pulse mode interrupt or held low for a level mode interrupt. |
| -IREQ (True IDE mode) | | | In true IDE mode, this signal is the active high Interrupt Request to the host. |

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Table 8: Signal Descriptions (Continued)

| Signal Name | Pin | Type | Description |
|--|--------|------|---|
| -REG (PC Card memory mode) Attribute Memory Select | 44 | I | This signal is used during memory cycles to distinguish between common memory and register (attribute) memory accesses. This signal is set: <ul style="list-style-type: none"> • High for common memory. • Low for attribute memory. |
| -REG (PC Card I/O mode) | | | The signal must also be active (low) during I/O cycles when the I/O address is on the bus. |
| -DMACK (True IDE mode) | | | In true IDE mode, this signal is used by the host in response to DMARQ to initiate DMA transfers. The DMARQ/-DMACK handshake is used to provide flow control during the transfer. When -DMACK is asserted, -CS0 and -CS1 are not asserted and transfers are 16-bits wide. |
| -RESET (PC Card memory mode) | 41 | I | When the pin is high, this signal resets the SiliconDrive CF. The SiliconDrive CF is reset only at power-up if this pin is left high or open from power-up. The SiliconDrive CF is also reset when the Soft Reset bit in the Card Configuration Option register is set. |
| -RESET (PC Card I/O mode) | | | This signal is the same as the PC Card Memory Mode signal. |
| -RESET (True IDE mode) | | | In the true IDE mode, this input pin is the active low hardware reset from the host. |
| V _{CC} (PC Card memory mode) | 13, 38 | - | +5V, +3.3V power. |

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Table 8: Signal Descriptions (Continued)

| Signal Name | Pin | Type | Description |
|---------------------------------------|--------|------|---|
| V _{CC} (PC Card I/O mode) | | | This signal is the same for all modes. |
| V _{CC} (True IDE mode) | | | This signal is the same for all modes. |
| -VS1, -VS2 | 33, 40 | O | Voltage Sense Signals. <ul style="list-style-type: none"> -VS1 is grounded so that the SiliconDrive CF CIS can be read at 3.3V. -VS2 is reserved by PC Card for a secondary voltage. |
| -VS1, -VS2 (PC Card I/O mode) | | | This signal is the same for all modes. |
| -VS1, -VS2 (True IDE mode) | | | This signal is the same for all modes. |
| -WAIT (PC Card memory mode) | 42 | O | The -WAIT signal is driven low by the SiliconDrive CF to signal the host to delay completion of a memory or I/O cycle that is in progress. |
| -WAIT (PC Card I/O mode) | | | This signal is the same as the PC Card Memory Mode signal. |
| -IORDY (True IDE mode) | | | In true IDE mode, this output signal may be used as IORDY. |
| -WE (PC Card memory mode) | 36 | I | This is a signal driven by the host and used for strobing memory write data to the registers of the SiliconDrive CF when the card is configured in the memory interface mode. This signal is also used for writing the configuration registers. |
| -WE (PC Card I/O mode) | | | In PC Card I/O mode, this signal is used for writing the configuration registers. |

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Table 8: Signal Descriptions (Continued)

| Signal Name | Pin | Type | Description |
|-------------------------------|-----|------|--|
| -WE (True IDE mode) | | | In true IDE mode, this input signal is not used and should be connected to V_{CC} by the host. |
| WP (PC Card memory mode) | 24 | O | Write Protect Memory Mode. The SiliconDrive CF does not have a write protect switch. This signal is held low after the completion of the reset initialization sequence. |
| -IOIS16 (PC Card I/O mode) | | | I/O Operation. When the SiliconDrive CF is configured for I/O operation, pin 24 is used for the -I/O Selected, which is a 16-bit port (-IOIS16) function. A low signal indicates that a 16-bit or odd byte only operation can be performed at the addressed port. |
| -IOIS16 (True IDE mode) | | | In true IDE mode, this output signal is asserted low when this device is expecting a word data transfer cycle. |

ABSOLUTE MAXIMUM RATINGS**Table 9: Absolute Maximum Ratings**

| Symbol | Parameter | Minimum | Maximum | Units |
|-----------|------------------------------|---------|---------|-------|
| T_s | Storage Temperature | -55 | 125 | °C |
| T_A | Operating Temperature | -40 | 85 | °C |
| V_{CC} | V_{CC} with Respect to GND | -0.3 | 6.7 | V |
| V_{in} | Input Voltage | -0.5 | 3.8 | V |
| V_{out} | Output Voltage | -0.3 | 3.6 | V |

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CAPACITANCE

Table 10: Capacitance

| Symbol | Parameter | Maximum | Units |
|-----------|---------------------------|---------|-------|
| C_{in} | Input Capacitance | 35 | pF |
| C_{out} | Output Capacitance | 35 | pF |
| $C_{I/O}$ | Bidirectional Capacitance | 35 | pF |

DC CHARACTERISTICS

Table 11: DC Characteristics

| Symbol | Parameter | 3.3 V $\pm 10\%$ | | 5V $\pm 10\%$ | | Units |
|-----------|-----------------------------|------------------|---------------------|---------------|---------------------|---------|
| | | Minimum | Maximum | Minimum | Maximum | |
| V_{CC} | Power Supply Voltage | 3.0 | 3.6 | 4.5 | 5.5 | V |
| I_{LI} | Input Leakage *(1) Current | - | 5 | - | 5 | μA |
| I_{LO} | Output Leakage *(1) Current | - | 5 | - | 5 | μA |
| V_{CCR} | V_{CC} Read Current | - | 50 | - | 80 | mA |
| V_{CCW} | V_{CC} Write Current | - | 50 | - | 80 | mA |
| V_{CCS} | V_{CC} Standby Current | - | 0.3 | - | 0.5 | mA |
| V_{IL} | Input Low Voltage | -0.3 | $0.3 \times V_{CC}$ | -0.3 | $0.3 \times V_{CC}$ | V |
| V_{IH} | Input High Voltage | 2.5 | $V_{CC} + 0.3$ | 2.5 | $V_{CC} + 0.3$ | V |
| V_{OL} | Output Low Voltage | - | 0.4 | - | 0.4 | V |
| V_{OH} | Output High Voltage | 2.4 | - | 2.4 | - | V |

*(1) Except the pulled-up/pulled-down pin.

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AC CHARACTERISTICS

Attribute and Common Memory Read Timing

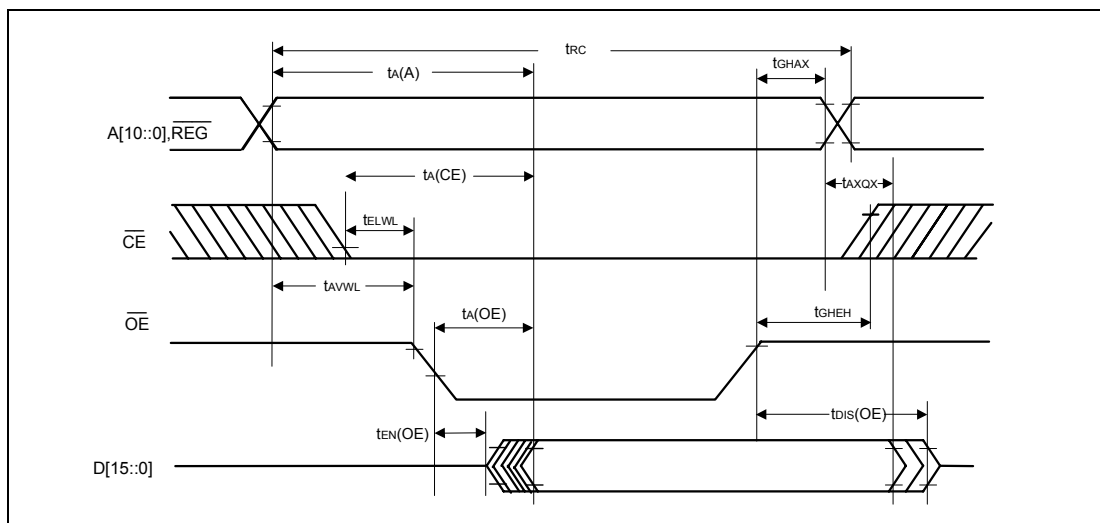


Figure 2: Attribute and Common Memory Read Timing Diagram

Table 12: Attribute and Common Memory Read Timing

| Symbol | Parameter | Minimum | Maximum | Units |
|---------------|------------------------------------|---------|---------|-------|
| t_{RC} | Read Cycle Time | 100 | - | ns |
| $t_{A(A)}$ | Address Access Time | - | 100 | ns |
| $t_{A(CE)}$ | Card Enable Access Time | - | 100 | ns |
| $t_{A(OE)}$ | Output Enable Access Time | - | 50 | ns |
| $t_{DIS(OE)}$ | Output Disable Time from OE | - | 50 | ns |
| $t_{EN(OE)}$ | Output Enable Time from OE | 5 | - | ns |
| t_{AXQX} | Data Valid from Address Change | 0 | - | ns |
| t_{AVWL} | Address Setup Time | 10 | - | ns |
| t_{AXQX} | Address Hold Time | 15 | - | ns |
| t_{ELWL} | Card Enable Setup Time before OE | 0 | - | ns |
| t_{GHEH} | Card Enable Hold Time following OE | 15 | - | ns |

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Attribute and Common Memory Write Timing

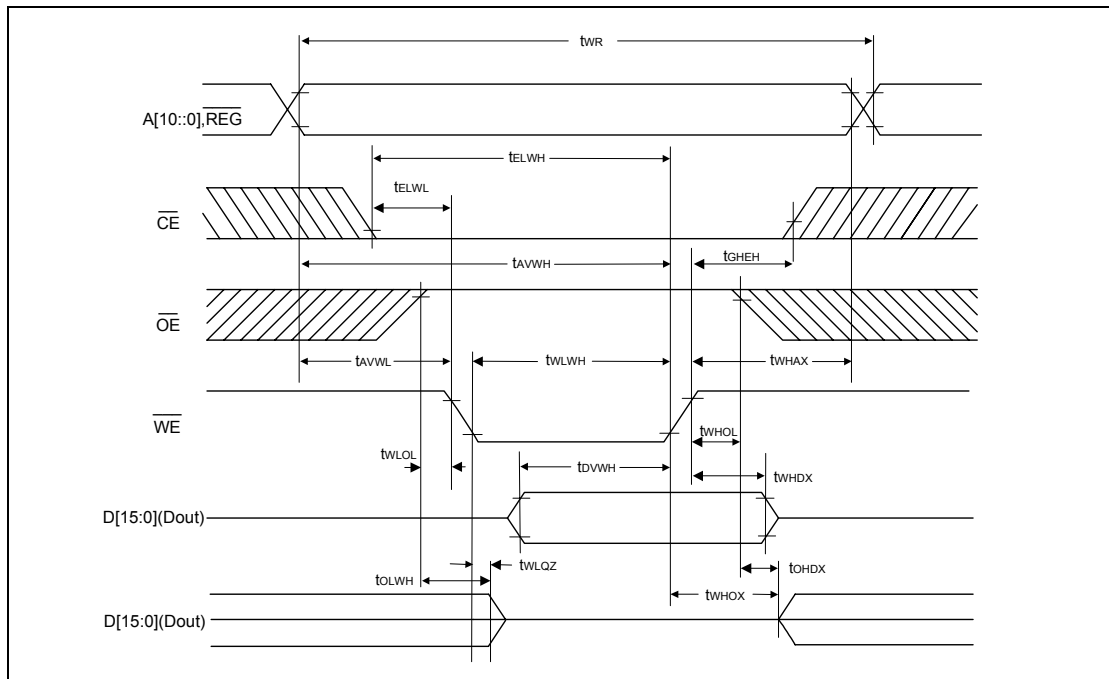


Figure 3: Attribute and Common Memory Write Timing Diagram

Table 13: Attribute and Common Memory Write Timing

| Symbol | Parameter | Minimum | Maximum | Units |
|------------|----------------------------------|---------|---------|-------|
| t_{WR} | Write Cycle Time | 100 | - | ns |
| t_{WLWH} | Write Pulse Width | 60 | - | ns |
| t_{AVWL} | Address Setup Time | 10 | - | ns |
| t_{AVWH} | Address Setup Time for WE | 70 | - | ns |
| t_{ELWH} | Card Enable Setup Time for WE | 70 | - | ns |
| t_{WHDX} | Data Hold Time | 10 | - | ns |
| t_{WHAX} | Write Recover Time | 15 | - | ns |
| t_{WLQZ} | Output Disable Time from WE | - | 75 | ns |
| t_{OLWH} | Output Disable Time from OE | - | 100 | ns |
| t_{WHOX} | Output Enable Time from WE | 5 | - | ns |
| t_{OHDX} | Output Enable Time from OE | 5 | - | ns |
| t_{WLOL} | Output Enable Setup for WE | 10 | - | ns |
| t_{WHOL} | Output Enable Hold from WE | 10 | - | ns |
| t_{ELWL} | Card Enable Setup Time before WE | 0 | - | ns |
| t_{GHEH} | Card Enable Hold Time from WE | 15 | - | ns |
| t_{DVWH} | Data Setup Time | 40 | - | ns |

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I/O Access Read Timing

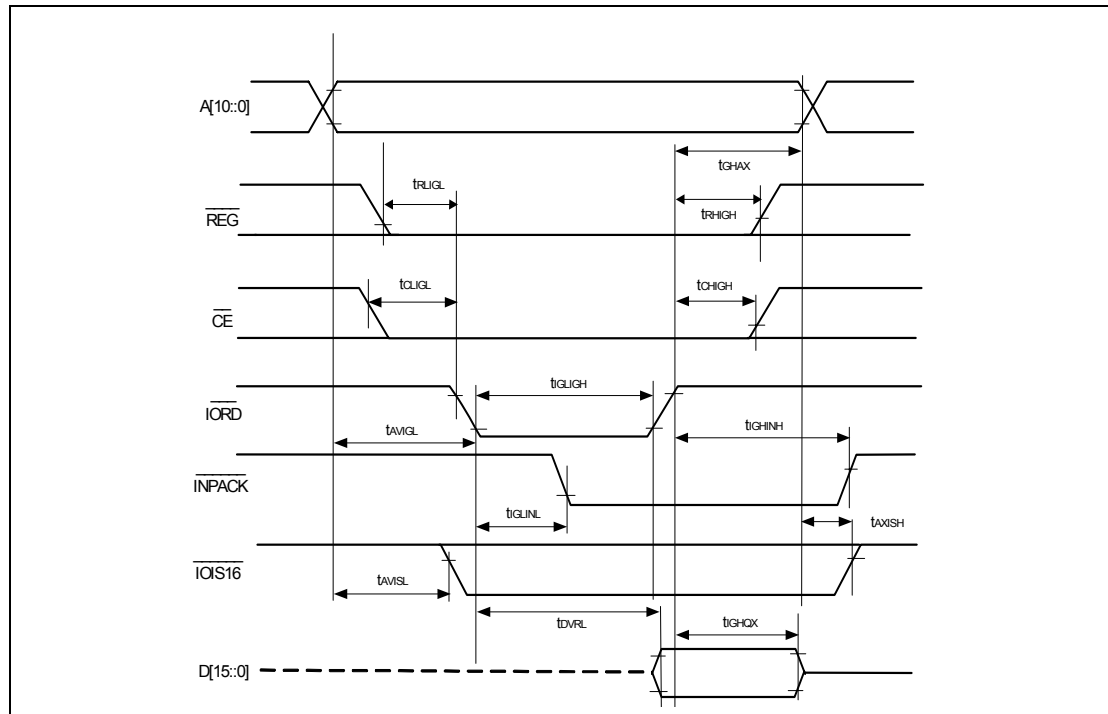


Figure 4: I/O Access Read Timing Diagram

Table 14: I/O Access Read Timing

| Symbol | Parameter | Minimum | Maximum | Units |
|--------------|-----------------------------------|---------|---------|-------|
| t_{DVRL} | Data Delay after IORD | - | 50 | ns |
| t_{IGHQX} | Data Hold following IORD | 5 | - | ns |
| t_{IGLIGH} | IORD Pulse Width | 65 | - | ns |
| t_{AVIGL} | Address Setup before IORD | 25 | - | ns |
| t_{GHAX} | Address Hold following IORD | 10 | - | ns |
| t_{CLIGL} | CE Setup before IORD | 5 | - | ns |
| t_{CHIGH} | CE Hold following IORD | 10 | - | ns |
| t_{RLIGL} | REG Setup before IORD | 5 | - | ns |
| t_{RHIGH} | REG Hold following IORD | 0 | - | ns |
| t_{IGLINL} | INPACK Delay falling from IORD | - | (1) | ns |
| t_{IGHINH} | INPACK Delay Rising from IORD | - | (1) | ns |
| t_{AVISL} | IOIS16 Delay Falling from Address | - | (1) | ns |
| t_{AXISH} | IOIS16 Delay Rising from Address | - | (1) | ns |

Note: (1) IOIS16 and INPACK are not supported.

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I/O Access Write Timing

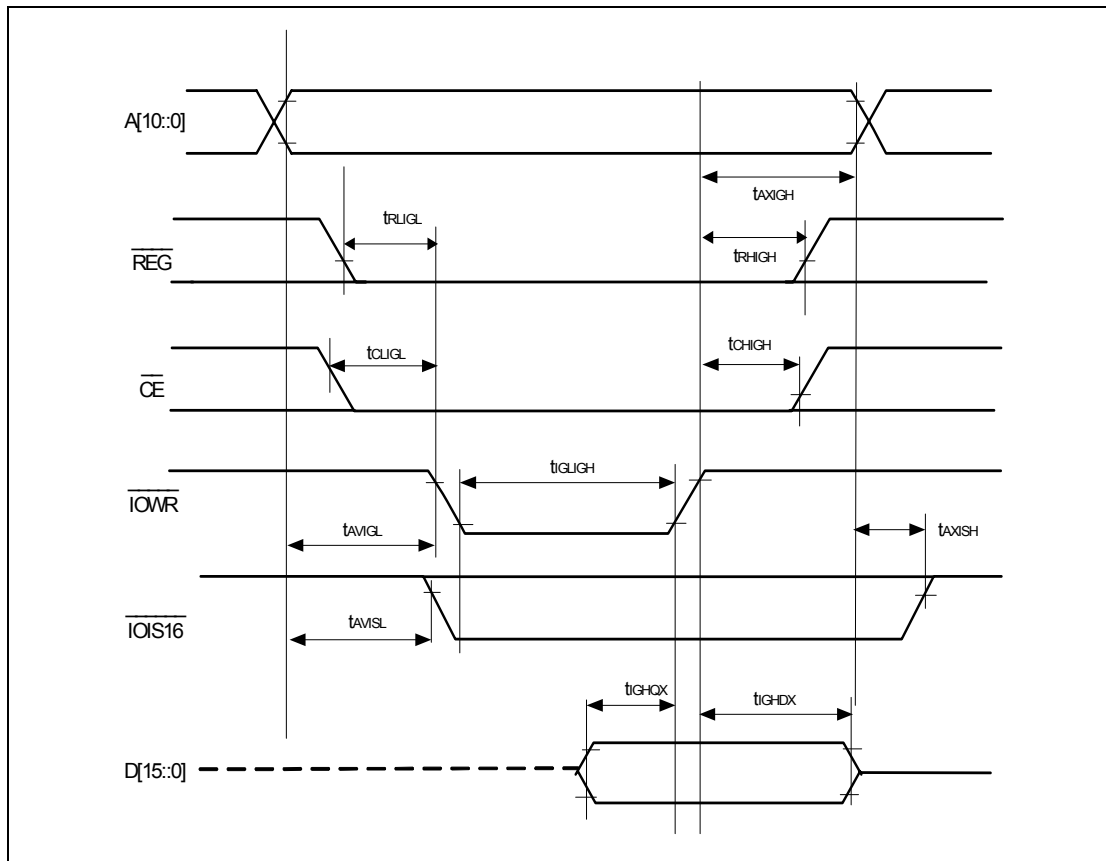


Figure 5: I/O Access Write Timing Diagram

Table 15: I/O Access Write Timing

| Symbol | Parameter | Minimum | Maximum | Units |
|--------------|-----------------------------------|---------|---------|-------|
| t_{IGHDX} | Data Hold following IOWR | 5 | - | ns |
| t_{IGHQX} | Data Setup before IOWR | 20 | - | ns |
| t_{IGLIGH} | IOWR Pulse Width | 65 | - | ns |
| t_{AVIGL} | Address Setup before IOWR | 25 | - | ns |
| t_{AXIGH} | Address Hold following IOWR | 10 | - | ns |
| t_{CLIGL} | CE Setup before IOWR | 5 | - | ns |
| t_{CHIGH} | CE Hold following IOWR | 10 | - | ns |
| t_{RLIGL} | REG Setup before IOWR | 5 | - | ns |
| t_{RHIGH} | REG Hold following IOWR | 0 | - | ns |
| t_{AVISL} | IOIS16 Delay Falling from Address | - | (1) | ns |
| t_{AXISH} | IOIS16 Delay Rising from Address | - | (1) | ns |

Note: (1) IOIS16 and INPACK are not supported.

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True IDE Read/Write Access Timing

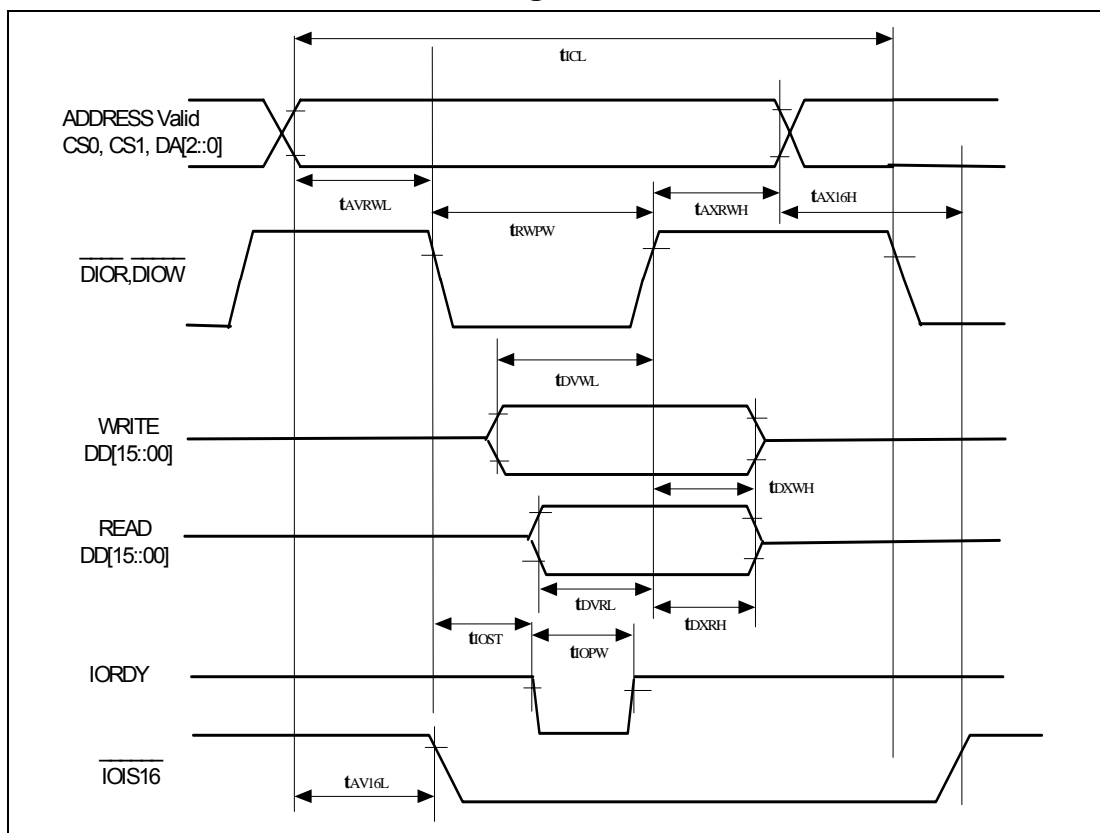


Figure 6: True IDE Read/Write Access Timing Diagram

Table 16: True IDE Read/Write Access Timing

| Symbol | Parameter | Minimum | Maximum | Units |
|-------------|--|---------|---------|-------|
| t_{ICL} | Cycle Time | 100 | - | ns |
| t_{AVRWL} | Address Valid to DIOR, DIOW Setup Time | 15 | - | ns |
| t_{RWPW} | DIOR, DIOW Pulse Width | 65 | - | ns |
| t_{DVWL} | DIOW Data Setup Time | 20 | - | ns |
| t_{DXWH} | DIOW Data Hold Time | 5 | - | ns |
| t_{DVRL} | DIOR Data Setup Time | 15 | - | ns |
| t_{DXRH} | DIOR Data Hold Time | 5 | - | ns |
| t_{AV16L} | Address Valid to IOCS16 Assertion | - | (1) | ns |
| t_{AX16H} | Address Valid to IOCS16 Negation | - | (1) | ns |
| t_{AXRWH} | DIOW, DIOR to Address Valid Hold Time | 10 | - | ns |
| t_{IOST} | IORDY Setup Time | - | (1) | ns |
| t_{IOPW} | IORDY Pulse Width | - | (1) | ns |

Note: (1) IOIS16 and INPACK are not supported.

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True IDE Multiword DMA Read/Write Access Timing

This function does not apply to SiliconDrives that have DMA disabled.

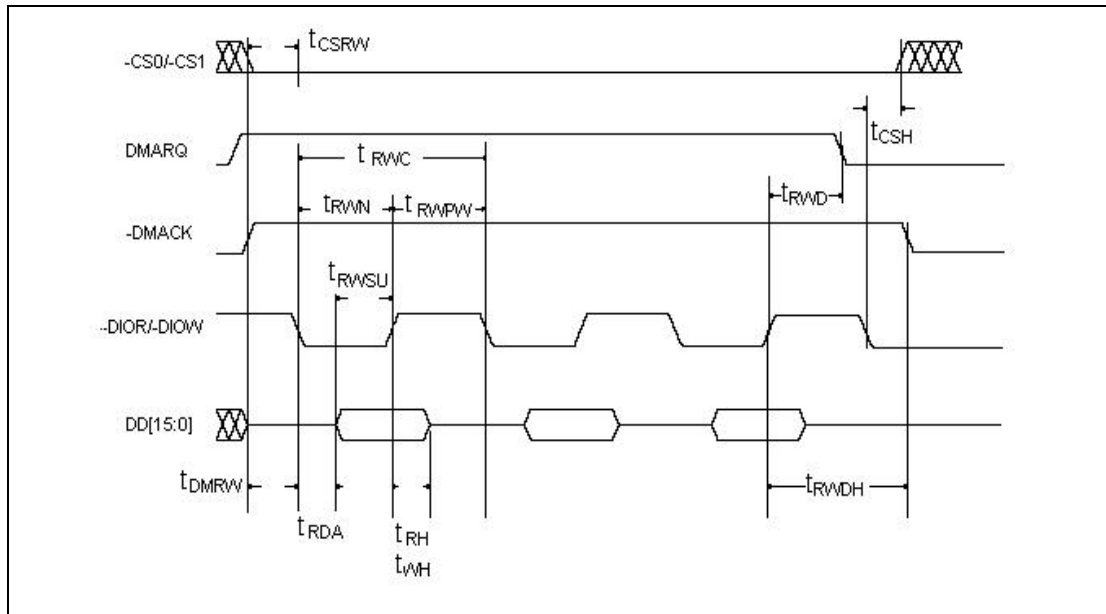


Figure 7: True IDE Multiword DMA Read/Write Access Timing

Table 17: True IDE Multiword DMA Read/Write Access Timing

| Symbol | Parameter | Minimum | Maximum | Units |
|------------|-------------------------------|---------|---------|-------|
| t_{RWC} | Cycle Time (mode 2) | 100 | - | ns |
| t_{RWPW} | DIOR/DIOW Pulse Width | 65 | - | ns |
| t_{RDA} | DIOR Data Access | - | 50 | ns |
| t_{RWSU} | DIOR/DIOW Data Setup Time | 15 | - | ns |
| t_{WH} | DIOW Data Hold Time | 5 | - | ns |
| t_{RH} | DIOR Data Hold Time | 5 | - | ns |
| t_{DMRW} | DMACK to DIOR/DIOW Setup Time | 0 | - | ns |
| t_{RWDH} | DIOR/DIOW to DMACK Hold Time | 5 | - | ns |
| t_{RWN} | DIOR/DIOW negated Pulse Width | 25 | - | ns |
| t_{RWD} | DIOR/DIOW to DMARQ Delay | - | 35 | ns |
| t_{CSRW} | CS(1:0) valid to DIOR/DIOW | 10 | - | ns |
| t_{CSH} | CS(1:0) Hold Time | 10 | - | ns |

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ATTRIBUTE MEMORY DESCRIPTION AND OPERATION

The attribute memory plane can be read or written to by asserting the REG# signal, qualified by the appropriate combination of CE1#, OE#, and WE#. An attribute memory map describing the type and location of the information maintained in the attribute memory plane is provided in ["Attribute Memory Map" on page 24](#).

With respect to SiliconDrive CF, attribute memory consists of two sections:

- Card Information Structure (CIS), which contains a description of the Card's capabilities and specifications.
- Function Configuration Registers (FCRs), which consists of four registers, that can be read or written to by a host to configure the Card for specific purposes.

ATTRIBUTE MEMORY READ OPERATIONS

Attribute memory read operations are enabled by asserting REG#, OE#, and CE1# low. Odd byte read operations from the attribute memory plane are not valid.

Table 18: Attribute Memory Read Operations

| Function Mode | REG# | CE1# | CE2# | A0 | OE# | WE# | D[15:8] | D[7:0] |
|----------------------|------|------|------|----|-----|-----|-----------|-----------|
| Standby | L | H | H | X | X | X | High-Z | High-Z |
| Byte Access | L | L | H | L | L | H | High-Z | Even |
| | L | H | L | H | L | H | High-Z | Not Valid |
| Word Access | L | L | L | X | L | H | Not Valid | Even |
| Odd Byte Only Access | L | L | H | X | H | H | Not Valid | High-Z |

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ATTRIBUTE MEMORY WRITE OPERATIONS

Attribute memory write operations are enabled by asserting REG#, WE#, and CE1# low. Odd byte write operations from the attribute memory plane are not valid.

Table 19: Attribute Memory Write Operations

| Function Mode | REG# | CE1# | CE2# | A0 | OE# | WE# | D[15:8] | D[7:0] |
|----------------------|-------------|-------------|-------------|-----------|------------|------------|----------------|---------------|
| Standby | L | H | H | X | X | X | High-Z | High-Z |
| Byte Access | L | L | H | L | H | L | High-Z | Even |
| | L | H | L | H | H | L | High-Z | Not Valid |
| Word Access | L | L | L | X | H | L | Not Valid | Even |
| Odd Byte Only Access | L | L | H | X | H | H | Not Valid | High-Z |

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ATTRIBUTE MEMORY MAP

As stated earlier, the Attribute Memory plane is comprised of two components, the CIS and the FCRs. The following tables detail the type, location, and read/write requirements for each of the four FCRs maintained in the attribute memory plane.

Table 20: Attribute Memory Map

| Register | Operation | Addr | CE1# | REG# | WE# | OE# |
|-------------------------------|-----------|------|------|------|-----|-----|
| Card Information Structure | Read | X | 0 | 0 | 1 | 0 |
| | Write | X | 0 | 0 | 0 | 1 |
| Configuration Option | Read | 200h | 0 | 0 | 1 | 0 |
| | Write | 200h | 0 | 0 | 0 | 1 |
| Card Configuration and Status | Read | 202h | 0 | 0 | 1 | 0 |
| | Write | 202h | 0 | 0 | 0 | 1 |
| Pin Replacement | Read | 204h | 0 | 0 | 1 | 0 |
| | Write | 204h | 0 | 0 | 0 | 1 |
| Socket and Copy | Read | 206h | 0 | 0 | 1 | 0 |
| | Write | 206h | 0 | 0 | 0 | 1 |

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CARD INFORMATION STRUCTURE

The CIS is data that describes the SiliconDrive CF, and is described by the CFA standard. This information can be used by the host system to determine a number of things about the Card that has been inserted. For information regarding the exact nature of this data and how to design the host software to interpret it, refer to the *PC Card Standard Metaformat Specification*.

Table 21: Card Information Structure

| Attribute Offset | Data | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Description of Contents | CIS Function |
|------------------|------|---|---|---|-------------|-------------------|---|---|---|---|--|
| 00h | 01h | CISTPL_DEVICE | | | | | | | | Device information tuple | Tuple code |
| 02h | 03h | - | | | | | | | | Link length is 3 bytes | Link to next tuple |
| 04h | D9h | Device Type Code Dh = I/O | | | W 1 | Device Speed 1 | | | | <ul style="list-style-type: none"> I/O device No WP Speed = 100ns | <ul style="list-style-type: none"> Device ID WPS Device speed |
| 06h | 01h | 1X | | | 2K | | | | | 2KB of address space | Device size |
| 08h | FFh | List End Marker | | | | | | | | End of device | END marker |
| 0Ah | 1Ch | CISTPL_DEVICE_OC | | | | | | | | Other conditions device in tuple code | Tuple code |
| 0Ch | 04h | TPL_LINK | | | | | | | | Link length is 4 bytes | Link to next tuple |
| 0Eh | 02h | EXT Reserved V _{CC} MWAIT | | | | | | | | 3V, wait is Not Used | Other conditions information field |
| 10h | D9h | Device Type | | | W P S | Device Speed | | | | <ul style="list-style-type: none"> Device type = DH: I/O Device WPS = 1: No WP Device speed = 1: 250ns | - |
| 12h | 01h | 1x | | | 2K units | | | | | 2KB of address space | Device size |
| 14h | FFh | List End Marker | | | | | | | | End of device | End marker |
| 16h | 18h | CISTPL_JEDEC_C | | | | | | | | JEDEC ID common memory | Tuple code |
| 18h | 02h | TPL_LINK | | | | | | | | Link length is 2 bytes | Link to next tuple |
| 1Ah | DFh | PCMCIA Manufacturer's JEDEC | | | | | | | | Manufacturer's ID code | - JEDEC ID |
| 1Ch | 01h | PCMCIA JEDEC Device Code | | | | | | | | Second byte of JEDEC ID | - |
| 1Eh | 20h | CISTPL_MANFID | | | | | | | | Manufacturer's ID code | Tuple code |
| 20h | 04h | TPL_LINK | | | | | | | | - | - |
| 22h | 00h | Low Byte of PCMCIA Manufacturer's Code | | | | | | | | JEDEC manufacturer's ID | Low byte of manufacturer's code |
| 24h | 00h | High Byte of PCMCIA Manufacturer's Code | | | | | | | | Code of 0, because the other byte is the JEDEC 1 byte manufacturer's ID | High byte of the manufacturer's code |
| 26h | 00h | Low Byte of Product Code | | | | | | | | Manufacturer's code for SiliconDrive CF | Low byte of the product code |
| 28h | 00h | High Byte of Product Code | | | | | | | | Manufacturer's code for SiliconDrive CF | High byte of the product code |
| 2Ah | 21h | CISTPL_FUNCID | | | | | | | | Function ID tuple | Tuple code |
| 2Ch | 02h | TPL_LINK | | | | | | | | Link length is 2 bytes | Link to next tuple |

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Table 21: Card Information Structure (Continued)

| Attribute Offset | Data | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Description of Contents | CIS Function |
|------------------|------|------------------------------------|---|-----|---|-----|----|----|----|--|--|
| 2Eh | 04h | TPLFID_FUNCTION = 04H | | | | | | | | Disk function, which may be silicon or removable | PC Card function code |
| 30h | 01h | Reserved | | | R | P | | | | <ul style="list-style-type: none"> R = 0: No BIOS ROM P = 1: Configure card at power-on | System initialization byte |
| 32h | 22h | CISTPL_FUNCE | | | | | | | | Function extension tuple | Tuple code |
| 34h | 02h | TPL_LINK | | | | | | | | Link length is 2 bytes | Link to next tuple |
| 36h | 01h | Disk Function Extension Tuple Type | | | | | | | | Disk interface type | Extension tuple type for disk |
| 38h | 01h | Disk Interface Type | | | | | | | | PC Card interface type | Interface type |
| 3Ah | 22h | CISTPL_FUNCE | | | | | | | | Function extension tuple | Tuple code |
| 3Ch | 03h | TPL_LINK | | | | | | | | Link length is 3 bytes | Link to next tuple |
| 3Eh | 02h | Disk Function Extension Tuple Type | | | | | | | | Basic PCMCIA-ATA extension tuple | Extension tuple type for disk |
| 40h | 04h | Reserved | | | D | U | S | V | | No Vpp, silicon, single drive <ul style="list-style-type: none"> V = 0: No Vpp required S = 0: Silicon U = 1: Unique serial number D = 0: Single drive on Card | Basic ATA option parameters byte 1 |
| 42h | 07h | R | I | E | N | P3 | P2 | P1 | P0 | <ul style="list-style-type: none"> P0: Sleep mode supported P1: Standby mode supported P2: Idle mode supported P3: Drive auto power control N: Some configuration excludes 3X7 E: Index bit is emulated I: Twin IOIS16# data register only R: Reserved | Basic ATA option parameters byte 2 |
| 44h | 1Ah | CISTPL_CONFIG | | | | | | | | Configuration tuple | Tuple code |
| 46h | 05h | TPL_LINK | | | | | | | | Link length is 5 bytes | Link to next tuple |
| 48h | 01h | RAS | | RMS | | RAS | | - | | <ul style="list-style-type: none"> RFS: Reserved RMS: TPCC RMSK size -1 = 0 RAS: TPCC_RADR size -1 = 1 1-byte register mask 2-byte configuration base address | Size of fields byte TPCC_SZ |
| 4Ah | 07h | TPCC_LAST | | | | | | | | Entry with configuration index of 7 is final entry in table | Last entry of configuration registers |
| 4Ch | 00h | TPCC_RADR (LSB) | | | | | | | | Configuration registers are located at 200H in REG space | Location of configuration registers |
| 4Eh | 02h | TPCC_RADR (MSB) | | | | | | | | - | - |
| 50h | 0Fh | Reserved | | | S | P | C | I | - | <ul style="list-style-type: none"> I: Configuration index C: Configuration and status P: Pin replacement S: Socket and copy | Configuration registers present mask TPCC_RMSK |
| 52h | 1Bh | CISTPL_TABLE_ENTRY | | | | | | | | Configuration table entry tuple | Tuple code |
| 54h | 0Bh | TPL_LINK | | | | | | | | Link length is 11 bytes | Link to next tuple |

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Table 21: Card Information Structure (Continued)

| Attribute Offset | Data | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Description of Contents | CIS Function | | |
|------------------|------|---------------------------------|----------|---------------------|----|----------------|----------|----|----|--|---|---|---|
| 56h | C0h | I | D | Configuration index | | | | | | Memory-mapped I/O configuration | Configuration table index byte TPCE_INDXX | | |
| | | | | | | | | | | <ul style="list-style-type: none"> I = 1: Interface byte follows D = 1: Default entry Configuration index = 0 | | | |
| 58h | C0h | W | R | P | B | Interface Type | | | | | Interface description field TPCE_IF | | |
| | | | | | | | | | | | <ul style="list-style-type: none"> W = 0: Wait not used R = 1: Ready active P = 0: WP used B = 0: BVD1 and BVD2 not used IF type = 0: Memory interface | | |
| 5Ah | A1h | M | MS | IR | IO | T | P | | | | | Feature selection byte TPCE_FS | |
| | | | | | | | | | | | | <ul style="list-style-type: none"> M = 1: Miscellaneous information present MS = 01: Memory space information single 2-byte length IR = 0: No interrupt information present IO = 0: No I/O port information present T = 0: No timing information present P = 1: V_{CC} only information | |
| 5Ch | 27h | R | DI | PI | AI | SI | HV | LV | NV | Nominal voltage only follows | Power parameters for V _{CC} | | |
| | | | | | | | | | | <ul style="list-style-type: none"> R: Reserved DI: Powerdown current information PI: Peak current information AI: Average current information SI: Static current information HV: Maximum voltage information LV: Minimum voltage information NV: Nominal voltage information | | | |
| 5Eh | 55h | X | Mantissa | | | | Exponent | | | | Nominal voltage = 5V | V _{CC} nominal value | |
| 60h | 4Dh | X | Mantissa | | | Exponent | | | | | V _{CC} nominal 4.5V | V _{CC} minimum value | |
| 62h | 5Dh | X | Mantissa | | | Exponent | | | | | V _{CC} nominal 5.5V | V _{CC} maximum value | |
| 64h | 75h | X | Mantissa | | | Exponent | | | | | Maximum average current over 10ms is 80mA | Maximum average current | |
| 66h | 08h | Length in 256 bytes pages (LSB) | | | | | | | | | | Length of memory space is 2KB | Memory space description structures (TPCE_MS) |
| 68h | 00h | Length in 256 bytes pages (MSB) | | | | | | | | | | Length of memory space is 2KB | Memory space description structures (TPCE_MS) |
| 6Ah | 21h | X | R | P | RO | AT | | - | | | <ul style="list-style-type: none"> X = 0: No more miscellaneous fields R: Reserved P = 1: Powerdown supported RO = 0: Not read only mode A = 0: Audio not supported T = 0: Single drive | Miscellaneous features field TPCE_MI | |
| 6Ch | 1Bh | CISTPL_TABLE_ENTRY | | | | | | | | | Configuration table entry tuple | Tuple code | |
| 6Eh | 06h | TPL_LINK | | | | | | | | | Link length is 6 bytes | Link to next tuple | |

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Table 21: Card Information Structure (Continued)

| Attribute Offset | Data | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Description of Contents | CIS Function | |
|------------------|------|--------------------|----------|---------------|----|----------------|----------|---|---|--|--|-------------------------------|
| 70h | 00h | I | D | IR | IQ | T | P | - | - | Memory-mapped I/O configuration <ul style="list-style-type: none"> I = 0: No interface byte D = 0: No default entry Configuration index = 0 | Configuration table index byte TPCE_INDXX | |
| 72h | 01h | M | MS | IR | IO | T | P | - | - | <ul style="list-style-type: none"> M = 0: No miscellaneous information MS = 00: No memory space information IR = 0: No interrupt information present IO = 0: No I/O port information present T = 0: No timing information present P = 1: V_{CC} only information | Feature selection byte TPCE_FS | |
| 74h | 21h | R | DI | PI | AI | SI | HV/LV/NV | | - | Nominal voltage only follows <ul style="list-style-type: none"> R: Reserved DI: Powerdown current information PI: Peak current information AI: Average current information SI: Static current information HV: Maximum voltage information LV: Minimum voltage information NV: Nominal voltage information | Power parameters for V _{CC} | |
| 76h | B5h | X | Mantissa | | | Exponent | | | - | - | Nominal voltage = 3.0 V | V _{CC} nominal value |
| 78h | 1Eh | Extension | | | | | | | - | - | +0.3 V | Extension byte |
| 7Ah | 4Dh | X | Mantissa | | | Exponent | | | - | - | Maximum average current over 10ms is 45 mA | Maximum average current |
| 7Ch | 1Bh | CISTPL_TABLE_ENTRY | | | | | | | - | - | Configuration table entry tuple | Tuple code |
| 7Eh | 0Dh | TPL_LINK | | | | | | | - | - | Link length is 10 bytes | Link to next tuple |
| 80h | C1h | I | D | Configuration | | | INDEX | | | Contiguous I/O mapped ATA registers configuration <ul style="list-style-type: none"> I = 1: Interface byte follows D = 1: Default entry Configuration index = 1 | Configuration table index byte TPCE_INDXX | |
| 82h | 41h | W | R | P | B | Interface Type | | | | <ul style="list-style-type: none"> W = 0: Wait not used R = 1: Ready active P = 0: WP not used B = 0: BVS1 and BVD2 not used IF type = 1: I/O interface | Interface description field TPCE_IF | |
| 84h | 99h | M | MS | IR | IO | T | P | - | - | <ul style="list-style-type: none"> M = 1: Miscellaneous information present MS = 00: No memory space information IR = 1: Interrupt information present IO = 1: I/O port information present T = 0: No timing information present P = 1: V_{CC} only information | Feature selection byte TPCE_FS | |

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Table 21: Card Information Structure (Continued)

| Attribute Offset | Data | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Description of Contents | CIS Function | |
|------------------|------|---------------------|----------|---------------------|----|----------|----------|----|----|--|--|---|
| 86h | 27h | R | DI | PI | AI | SI | HV | LV | NV | Nominal voltage only follows <ul style="list-style-type: none"> R: Reserved DI: Powerdown current information PI: Peak current information AI: Average current information SI: Static current information HV: Maximum voltage information LV: Minimum voltage information NV: Nominal voltage information | Power parameters for V _{CC} | |
| 88h | 55h | X | Mantissa | | | Exponent | | | | Nominal voltage = 5V | V _{CC} nominal value | |
| 8Ah | 4Dh | X | Mantissa | | | Exponent | | | | V _{CC} nominal 4.5V | V _{CC} minimum value | |
| 8Ch | 5Dh | X | Mantissa | | | Exponent | | | | V _{CC} nominal 5.5V | V _{CC} maximum value | |
| 8Eh | 75h | X | Mantissa | | | Exponent | | | | Maximum average current over 10ms is 80mA | Maximum average current | |
| 90h | 64h | R | S | E | I | O | AddrLine | | | <ul style="list-style-type: none"> S = 1: 16-bit hosts supported E = 1: 8-bit hosts supported IO AddrLine: 4 lines decoded | I/O space description field TPCE_IO | |
| 92h | F0h | S | P | L | M | V | B | I | N | <ul style="list-style-type: none"> S = 1: Share logic active P = 1: Pulse mode IRQ supported L = 1: Level mode IRQ supported M = 1: Bit mask of IRQs present V = 0: No vender unique IRQ B = 0: No bus error IRQ I = 0: No IO check IRQ N = 0: No NMI | Interrupt request description structure TPCE_IRQ | |
| 94h | FFh | IR | IR | IR | IR | IR | IR | IR | IR | SiliconSystems recommends the IRQ level to be routed 0 to 15 | Mask extension byte 1 TPCE_IRQ | |
| | | Q | Q | Q | Q | Q | Q | Q | Q | | | |
| | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | | | |
| 96h | FFh | IR | IR | IR | IR | IR | IR | IR | IR | SiliconSystems recommends routing to any normal, maskable IRQ. | Mask extension byte 2 TPCE_IRQ | |
| | | Q | Q | Q | Q | Q | Q | Q | Q | | | |
| | | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | | | |
| 98h | 21h | X | R | P | R | O | A | T | - | <ul style="list-style-type: none"> X = 0: No more miscellaneous fields R: Reserved P = 1: Powerdown supported RO = 0: Not read only mode A = 0: Audio not supported T = 0: Single drive | Miscellaneous features field TPCE_MI | |
| 9Ah | 1Bh | CISTPL__TABLE_ENTRY | | | | | | | | Configuration table entry tuple | Tuple code | |
| 9Ch | 06h | TPL_LINK | | | | | | | | Link length is 6 bytes | Link to next tuple | |
| 9Eh | 01h | I | D | Configuration Index | | | | | | | Contiguous I/O mapped ATA registers configuration | Configuration table index Byte TPCE_INDX |
| | | | | | | | | | | | <ul style="list-style-type: none"> I = 0: No Interface byte D = 0: No Default entry Configuration index = 1 | |

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Table 21: Card Information Structure (Continued)

| Attribute Offset | Data | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Description of Contents | CIS Function | |
|------------------|------|--------------------|----------|---------------------|----|----------------|----|----|----|--|--|--|
| A0h | 01h | M | MS | IR | IO | T | P | - | - | <ul style="list-style-type: none"> M = 0: No miscellaneous information MS = 00: No memory space information IR = 0: No interrupt information present IO = 0: No I/O port information present T = 0: No timing information present P = 1: V_{CC} only information | Feature selection byte TPCE_FS | |
| A2h | 21h | R | DI | PI | AI | SI | HV | LV | NV | <ul style="list-style-type: none"> R: Reserved DI: Powerdown current information PI: Peak current information AI: Average current information SI: Static current information HV: Maximum voltage information LV: Minimum voltage information NV: Nominal voltage information | Power parameters for V _{CC} | |
| A4h | B5h | X | Mantissa | | | Exponent | | | | | Nominal voltage = 3.0V | V _{CC} nominal value |
| A6h | 1Eh | X | Mantissa | | | Exponent | | | | | +0.3V | Extension byte |
| A8h | 4Dh | X | Mantissa | | | Exponent | | | | | Maximum average current over 10ms is 45mA | Maximum average current |
| AAh | 1Bh | CISTPL_TABLE_ENTRY | | | | | | | | Configuration table entry tuple | Extension byte | |
| ACh | 12h | TPL_LINK | | | | | | | | Link length is 18 bytes | Link to next tuple | |
| A Eh | C2h | I | D | Configuration Index | | | | | | | <ul style="list-style-type: none"> I = 1: Interface byte follows D = 1: default entry follows Configuration index = 2 | Configuration table index byte TPCE_IND _X |
| B0h | 41h | W | R | P | B | Interface Type | | | | <ul style="list-style-type: none"> W = 0: Wait not used R = 1: Ready active P = 0: WP not used B = 0: BVS1 and BVD2 not used IF type = 1: I/O interface | Interface description field TPCE_IF | |
| B2h | 99h | M | MS | IR | IO | T | P | - | - | <ul style="list-style-type: none"> M = 1: Miscellaneous information present MS = 00: No memory space information IR = 1: Interrupt information present IO = 1: I/O port information present T = 0: No timing information present P = 1: V_{CC} only information | Feature selection byte TPCE_FS | |
| B4h | 27h | R | DI | PI | AI | SI | HV | LV | NV | <ul style="list-style-type: none"> R: Reserved DI: Powerdown current information PI: Peak current information AI: Average current information SI: Static current information HV: Maximum voltage information LV: Minimum voltage information NV: Nominal voltage information | Power parameters for V _{CC} | |

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Table 21: Card Information Structure (Continued)

| Attribute Offset | Data | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Description of Contents | CIS Function |
|------------------|------|-------------------------|----------|---------------------|---|----------|----------|---------------------------------|---|---|---|
| B6h | 55h | X | Mantissa | | | Exponent | | | | Nominal voltage = 5V | V _{CC} nominal value |
| B8h | 4Dh | X | Mantissa | | | Exponent | | | | V _{CC} nominal 4.5V | V _{CC} minimum value |
| BAh | 5Dh | X | Mantissa | | | Exponent | | | | V _{CC} nominal 5.5V | V _{CC} maximum value |
| BCh | 75h | X | Mantissa | | | Exponent | | | | Maximum average current over 10ms is 80mA | Maximum average current |
| BEh | EAh | R | S | E | I | O | AddrLine | | | <ul style="list-style-type: none"> R = 1: Range follows S = 1: 16-bit hosts supported E = 1: 8-bit hosts supported IO AddrLines: 10 lines decoded | I/O space description field TPCE_IO |
| C0h | 61h | LS | AS | N Range | | | | | | <ul style="list-style-type: none"> LS = 1: Size of lengths is 1 byte AS = 2: Size of address is 2 bytes N Range = 1: Address Range-1 | I/O range format description |
| C2h | F0h | First I/O Base Address | | | | | | First I/O base address (LSB) | | | First I/O range address |
| C4h | 01h | First I/O Base Address | | | | | | First I/O base address (MSB) | | | - |
| C6h | 07h | First I/O Base Address | | | | | | First I/O length -1 | | | First I/O range length |
| C8h | F6h | Second I/O Base Address | | | | | | Second I/O base address (LSB) | | | Second I/O range address |
| CAh | 03h | Second I/O Base Address | | | | | | Second I/O base address (MSB) | | | |
| CCh | 01h | Second I/O Range Length | | | | | | Second I/O length -1 | | | Second I/O range length |
| CEh | EEh | S | P | L | M | IRQ | Level | | | <ul style="list-style-type: none"> S = 1: Share logic active P = 1: Pulse mode IRQ supported L = 1: Level mode IRQ supported M = 0: Bit mask of IRQs present — IRQ level is IRQ14 | Interrupt request description structure TPCE_IR |
| D0h | 21h | X | R | P | R | O | A | T | - | <ul style="list-style-type: none"> X = 0: No more miscellaneous fields R: Reserved P = 1: Powerdown supported RO = 0: Not read only mode A = 0: Audio not supported T = 0: Single drive | Miscellaneous features field TPCE_MI |
| D2h | 1Bh | CISTPL_TABLE_ENTRY | | | | | | Configuration table entry tuple | | | Tuple code |
| D4h | 06h | TPL_LINK | | | | | | Link length is 6 bytes | | | Link to next tuple |
| D6h | 02h | I | D | Configuration Index | | | | | | ATA primary I/O mapped configuration | Configuration table index byte TPCE_IND _X |
| D8h | 01h | I | D | Configuration Index | | | | | | Contiguous I/O mapped ATA registers configuration | Configuration table index byte TPCE_IND _X |

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Table 21: Card Information Structure (Continued)

| Attribute Offset | Data | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Description of Contents | CIS Function | |
|------------------|------|--------------------|----------|----|----|----------|----|----|------------------------|--|--------------------------------------|-------------------------------|
| DAh | 21h | M | MS | IR | IO | T | P | - | - | <ul style="list-style-type: none"> M = 0: No miscellaneous information MS = 00: No memory space information IR = 0: No interrupt information present IO = 0: No I/O port information present T = 0: No timing information present P = 1: V_{CC} only information | Feature selection byte TPCE_FS | |
| DCh | B5h | R | DI | PI | AI | SI | HV | LV | NV | <ul style="list-style-type: none"> R: Reserved DI: Powerdown current information PI: Peak current information AI: Average current information SI: Static current information HV: Maximum voltage information LV: Minimum voltage information NV: Nominal voltage information | Power parameters for V _{CC} | |
| DEh | 1Eh | X | Mantissa | | | Exponent | | | Nominal voltage = 3.0V | | | V _{CC} nominal value |
| E0h | 4Dh | Extension | | | | | | | | +0.3V | Extension byte | |
| E2h | 1Bh | CISTPL_TABLE_ENTRY | | | | | | | | Configuration table entry tuple | Tuple code | |
| E4h | 12h | TPL_LINK | | | | | | | | Link length is 18 bytes | Link to next tuple | |
| E6h | C3h | M | MS | IR | IO | T | P | - | - | <ul style="list-style-type: none"> M = 0: No miscellaneous information MS = 00: No memory space information IR = 0: No interrupt information present IO = 0: No I/O port information present T = 0: No timing information present P = 1: V_{CC} only information | Feature selection byte TPCE_FS | |
| E8h | 41h | R | DI | PI | AI | SI | HV | LV | NV | <ul style="list-style-type: none"> R: Reserved DI: Powerdown current information PI: Peak current information AI: Average current information SI: Static current information HV: Maximum voltage information LV: Minimum voltage information NV: Nominal voltage information | Power parameters for V _{CC} | |
| EAh | 99h | M | MS | IR | IO | T | P | - | - | <ul style="list-style-type: none"> M = 1: No miscellaneous information MS = 00: No Memory space information IR = 1: No interrupt information present IO = 1: No I/O port information present T = 0: No timing information present P = 01: V_{CC} only information | Feature selection byte TPCE_FS | |

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Table 21: Card Information Structure (Continued)

| Attribute Offset | Data | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Description of Contents | CIS Function |
|------------------|------|--------------------|----------|---------|----|----------|----------|----|----|--|---|
| ECh | 27h | R | DI | PI | AI | SI | HV | LV | NV | Nominal voltage only follows <ul style="list-style-type: none"> R: Reserved DI: Powerdown current information PI: Peak current information AI: Average current information SI: Static current information HV: Maximum voltage information LV: Minimum voltage information NV: Nominal voltage information | Power parameters for V _{CC} |
| EEh | 55h | X | Mantissa | | | Exponent | | | | Nominal voltage = 5V | V _{CC} nominal value |
| F0h | 4Dh | X | Mantissa | | | Exponent | | | | V _{CC} nominal 4.5V | V _{CC} minimum value |
| F2h | 5Dh | X | Mantissa | | | Exponent | | | | V _{CC} nominal 5.5V | V _{CC} maximum value |
| F4h | 75h | X | Mantissa | | | Exponent | | | | Maximum average current over 10ms is 80mA | Maximum average current |
| F6h | EAh | R | S | E | I | O | AddrLine | | | <ul style="list-style-type: none"> R = 1: Range follows S = 1: 16-bit hosts supported E = 1: 8-bit hosts supported IO AddrLines: 10 lines decoded | I/O space description field TPCE_IO |
| F8h | 61h | LS | AS | N Range | | | | | | <ul style="list-style-type: none"> LS = 1: Size of lengths is 1 byte AS = 2: Size of address is 2 bytes N Range = 1: Address range -1 | I/O range format description |
| FAh | 70h | - | | | | | | | | First I/O base address (LSB) | First I/O range address |
| FCh | 01h | - | | | | | | | | First I/O base address (MSB) | - |
| FEh | 07h | - | | | | | | | | First I/O length -1 | First I/O range length |
| 100h | 76h | - | | | | | | | | Second I/O base address (LSB) | Second I/O range address |
| 102h | 03h | - | | | | | | | | Second I/O base address (MSB) | - |
| 104h | 01h | - | | | | | | | | Second I/O length | Second I/O range length |
| 106h | EEh | S | P | L | M | IRQ | Level | | | <ul style="list-style-type: none"> S = 1: Share logic active P = 1: Pulse mode IRQ supported L = 1: Level mode IRQ supported M = 0: Bit mask of IRQs present — IRQ level is IRQ14 | Interrupt request description structure TPCE_IR miscellaneous features field TPCE_MI |
| 108h | 21h | X | R | P | R | O | A | T | - | <ul style="list-style-type: none"> X = 0: No more miscellaneous fields - R: Reserved P = 1: Powerdown supported RO = 0: Not read only mode A = 0: Audio not supported T = 0: Single drive | |
| 10Ah | 1Bh | CISTPL_TABLE_ENTRY | | | | | | | | Configuration table entry tuple | Tuple code |
| 10Ch | 06h | TPL_LINK | | | | | | | | Link length is 6 bytes | Link to next tuple |

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Table 21: Card Information Structure (Continued)

| Attribute Offset | Data | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Description of Contents | CIS Function | |
|------------------|------|----------------|----------|---------------------|----|----------|----|----|----|--|--|-------------------------------|
| 10Eh | 03h | I | D | Configuration Index | | | | | | ATA primary I/O mapped configuration | Configuration table index byte TPCE_INDIX | |
| | | | | | | | | | | <ul style="list-style-type: none"> I = 0: No interface byte D = 0: No default entry Configuration index = 2 | | |
| 110h | 01h | M | MS | IR | IO | T | P | | - | <ul style="list-style-type: none"> M = 0: No miscellaneous information MS = 00: No memory space information IR = 0: No interrupt information present IO = 0: No I/O port information present T = 0: No timing information present P = 1: V_{CC} only information | Feature selection byte TPCE_FS | |
| 112h | 21h | R | DI | PI | AI | SI | HV | LV | NV | Nominal voltage only follows | Power parameters for V _{CC} | |
| | | | | | | | | | | <ul style="list-style-type: none"> R: Reserved DI: Powerdown current information PI: Peak current information AI: Average current information SI: Static current information HV: Maximum voltage information LV: Minimum voltage information NV: Nominal voltage information | | |
| 114h | B5h | X | Mantissa | | | Exponent | | | | | Nominal voltage = 3.0V | V _{CC} nominal value |
| 116h | 1Eh | Extension | | | | | | | | +0.3V | Extension byte | |
| 118h | 4Dh | X | Mantissa | | | Exponent | | | | | Maximum average current over 10ms is 45mA | Maximum average current |
| 11Ah | 1Bh | CISTPL_MANFID | | | | | | | | Manufacturer's ID code | Tuple code | |
| 11Ch | 04h | TPL_LINK | | | | | | | | Link length is 4 bytes | Link to next tuple | |
| 11Eh | 07h | I | D | Configuration Index | | | | | | AT fixed disk secondary I/O 3.3V configuration | TPCE_INDIX | |
| 120h | 00h | M | MS | IR | IO | T | P | | - | P: Power information type | TPCL_FS | |
| 122h | 28h | - | | | | | | | | Manufacturer code for SiliconDrive CF | Reserved | |
| 124h | D3h | - | | | | | | | | Manufacturer code for SiliconDrive CF | Reserved | |
| 126h | 14h | CISTPL_NO_LINK | | | | | | | | No link control tuple | Tuple code | |
| 128h | 00h | - | | | | | | | | Link is 0 bytes | Link to next tuple | |
| 12Ah | 15h | CISTPL_VERS_1 | | | | | | | | Level 1 version | Tuple code | |
| 12Ch | 1Ah | TPL_LINK | | | | | | | | Link length is 26h bytes | Link to next tuple | |
| 12Eh | 04h | TPPLV1_MAJOR | | | | | | | | PC Card 2.0/JEIDA4.1 | END marker | |
| 130h | 01h | TPPLV1_MINOR | | | | | | | | PC Card 2.0/JEIDA4.1 | Tuple code | |
| 132h | 53h | - | | | | | | | | S | Information string | |
| 134h | 49h | - | | | | | | | | I | - | |
| 136h | 4Ch | - | | | | | | | | L | - | |
| 138h | 49h | - | | | | | | | | I | - | |
| 13Ah | 43h | - | | | | | | | | C | - | |

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Table 21: Card Information Structure (Continued)

| Attribute Offset | Data | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Description of Contents | CIS Function |
|------------------|------|---|---|---|---|---|---|---|---|-------------------------|--------------|
| 13Ch | 4Fh | | | | - | | | | | O | - |
| 13Eh | 4Eh | | | | - | | | | | N | - |
| 140h | 53h | | | | - | | | | | S | - |
| 142h | 59h | | | | - | | | | | Y | - |
| 144h | 53h | | | | - | | | | | S | - |
| 146h | 54h | | | | - | | | | | T | - |
| | 45h | | | | - | | | | | E | - |
| 14Ah | 4Dh | | | | - | | | | | M | - |
| 14Ch | 53h | | | | - | | | | | S | - |
| 14Eh | 00h | | | | - | | | | | Space | - |
| 150h | 56h | | | | - | | | | | V | - |
| 152h | 45h | | | | - | | | | | E | - |
| 154h | 52h | | | | - | | | | | R | - |
| 156h | 32h | | | | - | | | | | 2 | - |
| 158h | 2Eh | | | | - | | | | | - | - |
| 15Ah | 30h | | | | - | | | | | 0 | - |
| 15Ch | 30h | | | | - | | | | | 0 | - |
| | 00h | | | | - | | | | | - | - |
| 160h | FFh | | | | - | | | | | - | - |

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CONFIGURATION OPTION REGISTER (200H)

The Configuration Option register is used to configure the SiliconDrive CF, define the address decoding, and initiate the software RESET sequence.

Table 22: Configuration Option Register (200h)

| Operation | D ₇ | D ₆ | D ₅ | D ₄ | D ₃ | D ₂ | D ₁ | D ₀ |
|----------------|----------------|----------------|---------------------|----------------|----------------|----------------|----------------|----------------|
| Read/ Write | SRESET | LevIREQ | Configuration Index | | | | | |
| Default Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bit(s) | Description |
|---------------------|--|
| SRESET | When set, this bit initiates a software-reset sequence, which is equivalent to a power-on reset or hardware reset. |
| LevIREQ | IREQ# interrupt signal level mode select: <ul style="list-style-type: none"> • Logic 0 = Pulse mode • Logic 1 = Level mode |
| Configuration Index | <ul style="list-style-type: none"> • Memory-mapped mode 000000B • Independent I/O mode 000001B • Primary mode 000010B • Secondary mode 000011B |

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CONFIGURATION AND STATUS REGISTER (202H)

The Configuration and Status Register (CSR) informs the host of any status changes with regard to power-down.

Table 23: Configuration and Status Register (202h)

| Operation | D ₇ | D ₆ | D ₅ | D ₄ | D ₃ | D ₂ | D ₁ | D ₀ |
|---------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|
| Read | Changed | SigChg | IOis8 | 0 | 0 | PwrDn | Int | 0 |
| Write | Changed | SigChg | IOis8 | 0 | 0 | PwrDn | Int | 0 |
| Default Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bit(s) | Description |
|---------|--|
| Changed | Indicates that either CREADY (D5) or CWPort (D4) of the Pin Replacement register is set. Additionally, this bit changes state as the Powerdown (D2) bit changes. |
| SigChg | Outputs the inverse state of the Changed bit to the hardware interface signal STSCHG# at the card interface. |
| Iois8 | <p>Informs the host of the valid data bus width for the operations in progress:</p> <ul style="list-style-type: none"> • 0 = 16-bit data transfer • 1 = 8-bit data transfer |
| PwrDwn | Indicates the state of the Card, which is either operating -0 or powerdown mode 1. During powerdown mode, no commands are accepted. Additionally, the host may not initiate a powerdown request when the card is busy via the Status register or the Hardware RDY/BSY pin. |
| Int | Indicates the inverse of the IREQ# status signal. |

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PIN PLACEMENT REGISTER (204H)

Table 24: Pin Placement Register (204h)

| Operation | D ₇ | D ₆ | D ₅ | D ₄ | D ₃ | D ₂ | D ₁ | D ₀ |
|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|
| Read/ Write | CBVD1 | CBVD2 | CRDY | CWProt | RBVD1 | RBVD2 | RRDY | RWProt |
| Default Value | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 |

| Bit(s) | Description |
|--------|--|
| CRDY | Indicates a bit change in the RRDY (D1) bit. |
| CWProt | Indicates a bit change in the RWProt (D0) bit. |
| RRDY | When set: <ul style="list-style-type: none"> • High 1 informs the host that the card is ready • Low 0 state indicates the card is busy |
| RWProt | Indicates Write Protect is enabled when set to 1, and disabled when 0. |

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SOCKET AND COPY REGISTER (206H)

Table 25: Socket and Copy Register (206h)

| Operation | D ₇ | D ₆ | D ₅ | D ₄ | D ₃ | D ₂ | D ₁ | D ₀ |
|---------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|
| Read/Write | RFU | Copy Number | | | Socket Number | | | |
| Default Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bit(s) | Description |
|---------------|---|
| RFU | Reserved for future use. |
| Copy Number | <p>Indicates the card number. Allows the host to differentiate between identical cards by writing to the bit of the card that is being accessed. This value is compared to the DRV bit in the ATA Drive/Head register.</p> <ul style="list-style-type: none"> • Card 0: 000B = (D6, D5, D4) (default) • Card 1: 001B = (D6, D5, D4) (alternate) |
| Socket Number | The host writes the socket number that identifies the inserted card. |

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COMMON MEMORY DESCRIPTION AND OPERATION

Common memory space can be accessed when the SiliconDrive is configured in memory-mapped mode.

COMMON MEMORY READ OPERATIONS

Common memory read operations are issued by asserting CE1#, CE2#, or both, and OE# low, REG#, and WE# must be inactive.

Table 26: Common Memory Read Operations

| Function Mode | REG# | CE1# | CE2# | A0 | OE# | WE# | D[15:8] | D[7:0] |
|----------------------|------|------|------|----|-----|-----|---------|--------|
| Standby | X | H | H | X | X | X | High-Z | High-Z |
| Byte Access | H | L | H | L | L | H | High-Z | Even |
| | H | L | H | H | L | H | High-Z | Odd |
| Word Access | H | L | L | X | L | H | Odd | Even |
| Odd Byte Only Access | H | H | L | X | L | H | Odd | High-Z |

COMMON MEMORY WRITE OPERATIONS

Common memory write operations are issued by asserting CE1#, CE2#, or both, and WE# low, REG#, and OE# must be inactive.

Table 27: Common Memory Write Operations

| Function Mode | REG# | CE1# | CE2# | A0 | OE# | WE# | D[15:8] | D[7:0] |
|----------------------|------|------|------|----|-----|-----|---------|--------|
| Standby | X | H | H | X | X | X | High-Z | High-Z |
| Byte Access | H | L | H | L | H | L | High-Z | Even |
| | H | L | H | H | H | L | High-Z | Odd |
| Word Access | H | L | L | X | H | L | Odd | Even |
| Odd Byte Only Access | H | H | L | X | H | L | Odd | High-Z |

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I/O SPACE DESCRIPTION AND OPERATION**I/O SPACE READ OPERATIONS****Table 28: I/O Space Read Operations**

| Function Mode | REG# | CE1# | CE2# | A0 | IORD# | IOWR# | D[15:8] | D[7:0] |
|----------------------|------|------|------|----|-------|-------|---------|--------|
| Standby | X | H | H | X | X | X | High-Z | High-Z |
| Byte Access | L | L | H | L | L | H | High-Z | Even |
| | L | L | H | H | L | H | High-Z | Odd |
| Word Access | L | L | L | L | L | H | Odd | Even |
| I/O Inhibit | H | X | X | X | L | H | High-Z | High-Z |
| Odd Byte Only Access | L | H | L | X | L | H | Odd | High-Z |

I/O SPACE WRITE OPERATIONS**Table 29: I/O Space Write Operations**

| Function Mode | REG# | CE1# | CE2# | A0 | IORD# | IOWR# | D[15:8] | D[7:0] |
|----------------------|------|------|------|----|-------|-------|---------|--------|
| Standby | X | H | H | X | X | X | X | X |
| Byte Access | L | L | H | L | H | L | X | Even |
| | L | L | H | H | H | L | X | Odd |
| Word Access | L | L | L | L | H | L | Odd | Even |
| I/O Inhibit | H | X | X | X | H | L | X | X |
| Odd Byte Only Access | L | H | L | X | H | L | Odd | X |

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ATA AND TRUE IDE REGISTER DECODING

SiliconDrive can be configured as either a memory-mapped or an I/O device. As noted earlier, communication to and from the drive is accomplished using the ATA Command Block.

MEMORY-MAPPED REGISTER DECODING

In memory-mapped mode, the SiliconDrive registers are accessed via standard memory references (i.e., OE# and WE#). The ATA registers are mapped to common memory space in a 2KB window starting at address 0.

Table 30: Memory-Mapped Register Decoding

| Reg# | Offset | A10 | A9:A4 | A3 | A2 | A1 | A0 | OE# = L | WE# = L |
|------|--------|-----|-------|----|----|----|----|--------------------------|---------------------------|
| 1 | 0 | 0 | X | 0 | 0 | 0 | 0 | Even Data Read | Even Data Write |
| 1 | 1 | 0 | X | 0 | 0 | 0 | 1 | Error | Feature |
| 1 | 2 | 0 | X | 0 | 0 | 1 | 0 | Sector Count | Sector Count |
| 1 | 3 | 0 | X | 0 | 0 | 1 | 1 | Sector Number | Sector Number |
| 1 | 4 | 0 | X | 0 | 1 | 0 | 0 | Cylinder Low | Cylinder Low |
| 1 | 5 | 0 | X | 0 | 1 | 0 | 1 | Cylinder High | Cylinder High |
| 1 | 6 | 0 | X | 0 | 1 | 1 | 0 | Drive/Head | Drive/Head |
| 1 | 7 | 0 | X | 0 | 1 | 1 | 1 | Status | Command |
| 1 | 8 | 0 | X | 1 | 0 | 0 | 0 | Duplicate Even Data Read | Duplicate Even Data Write |
| 1 | 9 | 0 | X | 1 | 0 | 0 | 1 | Duplicate Odd Data Read | Duplicate Odd Data Write |
| 1 | D | 0 | X | 1 | 1 | 0 | 1 | Duplicate Error | Duplicate Feature |
| 1 | E | 0 | X | 1 | 1 | 1 | 0 | Alternate Status | Device Control |
| 1 | F | 0 | X | 1 | 1 | 1 | 1 | Drive Address | Reserved |
| 1 | X | 1 | X | X | X | X | 0 | Even Data Read | Even Data Write |
| 1 | X | 1 | X | X | X | X | 1 | Odd Data Read | Odd Data Write |

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INDEPENDENT I/O MODE REGISTER DECODING

Independent I/O mode or contiguous I/O mode requires the host to decode a continuous block of 16 I/O registers to select the SiliconDrive.

Table 31: Independent I/O Mode Register Decoding

| Reg# | Offset | A10 | A9:A4 | A3 | A2 | A1 | A0 | OE# = L | WE# = L |
|------|--------|-----|-------|----|----|----|----|--------------------------|---------------------------|
| 0 | 0 | X | X | 0 | 0 | 0 | 0 | Even Data Read | Even Data Write |
| 0 | 1 | X | X | 0 | 0 | 0 | 1 | Error | Feature |
| 0 | 2 | X | X | 0 | 0 | 1 | 0 | Sector Count | Sector Count |
| 0 | 3 | X | X | 0 | 0 | 1 | 1 | Sector Number | Sector Number |
| 0 | 4 | X | X | 0 | 1 | 0 | 0 | Cylinder Low | Cylinder Low |
| 0 | 5 | X | X | 0 | 1 | 0 | 1 | Cylinder High | Cylinder High |
| 0 | 6 | X | X | 0 | 1 | 1 | 0 | Drive/Head | Drive/Head |
| 0 | 7 | X | X | 0 | 1 | 1 | 1 | Status | Command |
| 0 | 8 | X | X | 1 | 0 | 0 | 0 | Duplicate Even Data Read | Duplicate Even Data Write |
| 0 | 9 | X | X | 1 | 0 | 0 | 1 | Duplicate Odd Data Read | Duplicate Odd Data Write |
| 0 | D | X | X | 1 | 1 | 0 | 1 | Duplicate Error | Duplicate Feature |
| 0 | E | X | X | 1 | 1 | 1 | 0 | Alternate Status | Device Control |
| 0 | F | X | X | 1 | 1 | 1 | 1 | Drive Address | Reserved |

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PRIMARY AND SECONDARY I/O MAPPED REGISTER DECODING

Table 32: Primary and Secondary I/O Mapped Register Decoding

| Reg# | A10 | A9:A4 Primary | A9:A4 Secondary | A3 | A2 | A1 | A0 | IORD# = L | IOWR# = L |
|------|-----|------------------|--------------------|----|----|----|----|---------------------|--------------------|
| 0 | X | 1Fyh | 17yh | 0 | 0 | 0 | 0 | Even Data Read | Even Data Write |
| 0 | X | 1Fyh | 17yh | 0 | 0 | 0 | 1 | Error | Feature |
| 0 | X | 1Fyh | 17yh | 0 | 0 | 1 | 0 | Sector Count | Sector Count |
| 0 | X | 1Fyh | 17yh | 0 | 0 | 1 | 1 | Sector Number | Sector Number |
| 0 | X | 1Fyh | 17yh | 0 | 1 | 0 | 0 | Cylinder Low | Cylinder Low |
| 0 | X | 1Fyh | 17yh | 0 | 1 | 0 | 1 | Cylinder High | Cylinder High |
| 0 | X | 1Fyh | 17yh | 0 | 1 | 1 | 0 | Drive/Head | Drive/Head |
| 0 | X | 1Fyh | 17yh | 0 | 1 | 1 | 1 | Status | Command |
| 0 | X | 3Fyh | 37yh | 0 | 1 | 1 | 0 | Alternate Status | Device Control |
| 0 | X | 3Fyh | 37yh | 0 | 1 | 1 | 1 | Drive Address | Reserved |

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TASK FILE REGISTER SPECIFICATION

The Task File registers are used for reading and writing the storage data in the SiliconDrive. The decoded addresses are as shown in the following table.

Table 33: Task File Register Specification

| CS0# | CS1# | DA02 | DA01 | DA00 | DIOR# = L | DIOW# = L |
|------|------|------|------|------|------------------|----------------|
| 0 | 1 | 0 | 0 | 0 | Data | Data |
| 0 | 1 | 0 | 0 | 1 | Error | Feature |
| 0 | 1 | 0 | 1 | 0 | Sector Count | Sector Count |
| 0 | 1 | 0 | 1 | 1 | Sector Number | Sector Number |
| 0 | 1 | 1 | 0 | 0 | Cylinder Low | Cylinder Low |
| 0 | 1 | 1 | 0 | 1 | Cylinder High | Cylinder High |
| 0 | 1 | 1 | 1 | 0 | Drive/Head | Drive/Head |
| 0 | 1 | 1 | 1 | 1 | Status | Command |
| 0 | 0 | X | X | X | Invalid | Invalid |
| 1 | 1 | X | X | X | High-Z | Not Used |
| 1 | 0 | 0 | X | X | High-Z | Not Used |
| 1 | 0 | 1 | 0 | X | High-Z | Not Used |
| 1 | 0 | 1 | 1 | 0 | Alternate Status | Device Control |
| 1 | 0 | 1 | 1 | 1 | Device Address | Not Used |

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ATA REGISTERS

DATA REGISTER

The Data register is a 16-bit register used to transfer data blocks between the host and drive buffers. The register may set to 8-bit mode by using the Set Features Command defined in "[Seek — 7Xh](#)" on page 77.

ERROR REGISTER

The Error register contains the error status, if any, generated from the last executed ATA command. The contents are qualified by the ERR bit being set in "[Status Register](#)" on page 53.

Table 34: Error Register

| Operation | D ₇ | D ₆ | D ₅ | D ₄ | D ₃ | D ₂ | D ₁ | D ₀ |
|---------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|
| Read | BBK | UNC | MC | IDNF | MCR | ABRT | TKNOF | AMNF |
| Default Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bit(s) | Description |
|--------|--|
| 7 | Bad Block Detected (BBK). Set when a bad block is detected. |
| 6 | Uncorrectable Data Error (UNC). Set when an uncorrectable error is encountered. |
| 5 | Media Changed (MC). Set to 0. |
| 4 | ID Not Found (IDNF). Set when the sector ID is not found. |
| 3 | MCR (Media Change Request). Set to 0. |
| 2 | Aborted Command (ABRT). Set when a command is aborted due to a drive error. |
| 1 | Track 0 Not Found (TKONF). Set when the execute drive diagnostic command is executed. |
| 0 | Address Mark Not Found (AMNF). Set in the case of a general error. |

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FEATURE REGISTER

The Feature register is command-specific and used to enable and disable interface features. This register supports only either odd or even byte data transfers.

Table 35: Feature Register

| Operation | D ₇ | D ₆ | D ₅ | D ₄ | D ₃ | D ₂ | D ₁ | D ₀ |
|------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|
| Read/Write | Feature Byte | | | | | | | |

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SECTOR COUNT REGISTER

The Sector Count register is used to read or write the sector count of the data for which an ATA transfer has been made.

Table 36: Sector Count Register

| Operation | D ₇ | D ₆ | D ₅ | D ₄ | D ₃ | D ₂ | D ₁ | D ₀ |
|---------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|
| Read/Write | Sector Count | | | | | | | |
| Default Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |

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SECTOR NUMBER REGISTER

The Sector Number register is set by the host to specify the starting sector number associated with the next ATA command to be executed. Following a qualified ATA command sequence, the device sets the register value to the last sector read or written as a result of the previous AT command.

When Logical Block Addressing (LBA) mode is implemented and the host issues a command, the contents of the register describe the Logical Block Number bits A[7:0]. Following an ATA command, the device loads the register with the LBA block number resulting from the last ATA command.

Table 37: Sector Number Register

| Operation | D ₇ | D ₆ | D ₅ | D ₄ | D ₃ | D ₂ | D ₁ | D ₀ |
|---------------|--|----------------|----------------|----------------|----------------|----------------|----------------|----------------|
| Read/Write | Sector Number (CHS Addressing) | | | | | | | |
| | Logical Block Number bits A07-A00 (LBA Addressing) | | | | | | | |
| Default Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |

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CYLINDER LOW REGISTER

The Cylinder Low register is set by the host to specify the cylinder number low byte. Following an ATA command, the content of the register is written by the device, identifying the cylinder number low byte.

In LBA mode, the 8-bit register maintains the contents of the Logical Block number address bits A15:A08.

Table 38: Cylinder Low Register

| Operation | D ₇ | D ₆ | D ₅ | D ₄ | D ₃ | D ₂ | D ₁ | D ₀ |
|---------------|--|----------------|----------------|----------------|----------------|----------------|----------------|----------------|
| Read/Write | Cylinder Number Low Byte (CHS Addressing) | | | | | | | |
| | Logical Block Number bits A15-A08 (LBA Addressing) | | | | | | | |
| Default Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

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CYLINDER HIGH REGISTER

The Cylinder High register is set by the host to specify the cylinder number high byte. Following an ATA command, the content of the register is set internally by the device, identifying the cylinder number high byte.

In LBA mode, the 8-bit register maintains the contents of the Logical Block number address bits A23:A16.

Table 39: Cylinder High Register

| Operation | D ₇ | D ₆ | D ₅ | D ₄ | D ₃ | D ₂ | D ₁ | D ₀ |
|---------------|--|----------------|----------------|----------------|----------------|----------------|----------------|----------------|
| Read/Write | Cylinder Number Low Byte (CHS Addressing) | | | | | | | |
| | Logical Block Number bits A23-A16 (LBA Addressing) | | | | | | | |
| Default Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

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DRIVE/HEAD REGISTER

The Drive/Head register is used by the host and the device to select the type of addressing (CHS or LBA), the drive letter, and either bits 3-0 of the head number in CHS mode or logical block number bits 27-24 in LBA mode.

Table 40: Drive/Head Register

| Operation | D ₇ | D ₆ | D ₅ | D ₄ | D ₃ | D ₂ | D ₁ | D ₀ |
|---------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|
| Read/Write | 1 | LBA | 1 | DRV | HS3 LBA27 | HS2 LBA26 | HS1 LBA25 | HS0 LBA24 |
| Default Value | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |

The Drive/Head register is used by the host to specify one of a pair of ATA drives present in the platform.

| Bit(s) | Description |
|--------|--|
| 6 | LBA. Selects between CHS (0) and LBA (1) addressing mode. |
| 4 | Drive Address (DRV). Indicates the drive number selected by the host, either 0 or 1. |
| 3-0 | <p>HS3 to 0. Indicates bits 3-0 of the head number in CHS addressing mode or LBA bits 27-24 in LBA mode.</p> <ul style="list-style-type: none"> • CHS to LBA conversion: $LBA = (C \times HpC + H) \times SpH + S - 1$ • LBA to CHS conversion: <ul style="list-style-type: none"> ◦ $C = LBA / (HpC \times SpH)$ ◦ $H = (LBA / SpH) \bmod (HpC)$ ◦ $S = (LBA \bmod (SpH)) + 1$ <p>...where:</p> <ul style="list-style-type: none"> ◦ C is the cylinder number ◦ H is the head number ◦ S is the sector count ◦ HpC is the head count per cylinder count ◦ SpH is the sector count per head count (track) |

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STATUS REGISTER

The Status register provides the device's current status to the host. The status register is an 8-bit read-only register. When the contents of the register are read by the host, the IREQ# bit is cleared.

Table 41: Status Register

| Operation | D ₇ | D ₆ | D ₅ | D ₄ | D ₃ | D ₂ | D ₁ | D ₀ |
|---------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|
| Read/Write | BSY | DRDY | DWF | DSC | DRQ | CORR | IDX | ERR |
| Default Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bit(s) | Description |
|--------|--|
| 7 | Busy (BSY). Set when the drive is busy and unable to process any new ATA commands. |
| 6 | Data Ready (DRDY). Set when the device is ready to accept ATA commands from the host. |
| 5 | Drive Write Fault (DWF). Always set to 0. |
| 4 | Drive Seek Complete (DSC). Set when the drive heads have been positioned over a specific track. |
| 3 | Data Request (DRQ). Set when a device is ready to transfer a word or byte of data to or from the host and the device. |
| 2 | Corrected Data (CORR). Always set to 0. |
| 1 | Index (IDX). Always set to 0. |
| 0 | Error (ERR). Set when an error occurs during the previous ATA command. |

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COMMAND REGISTER

The Command register specifies the ATA command code being issued to the drive by the host. Execution of the command begins immediately following the issuance of the command register code by the host.

Table 42: Command Register

| Operation | D ₇ | D ₆ | D ₅ | D ₄ | D ₃ | D ₂ | D ₁ | D ₀ |
|------------|------------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|
| Read/Write | ATA Command Code | | | | | | | |

See ["ATA Command Block and Set Description" on page 58](#) for a listing of the supported ATA commands.

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ALTERNATE STATUS REGISTER

The Alternate Status register is a read-only register indicating the status of the device, following the previous ATA command. See ["Status Register" on page 53](#) for specific details.

Table 43: Alternate Status Register

| Operation | D ₇ | D ₆ | D ₅ | D ₄ | D ₃ | D ₂ | D ₁ | D ₀ |
|---------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|
| Read/Write | BSY | DRDY | DWF | DSC | DRQ | CORR | IDX | ERR |
| Default Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

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DEVICE CONTROL REGISTER

The Device Control register is used to control the interrupt request and issue ATA software resets.

Table 44: Device Control Register

| Operation | D ₇ | D ₆ | D ₅ | D ₄ | D ₃ | D ₂ | D ₁ | D ₀ |
|-----------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|
| Write | - | - | - | - | 1 | SRST | nIEN | 0 |

| Bit(s) | Description |
|--------|--|
| 7-4 | Reserved bits. |
| 3 | Always set to 1. |
| 2 | Software Reset (SRST) . When set, resets the ATA software. |
| 1 | Interrupt Enable (nIEN) . When set, device interrupts are disabled. There is no function in the memory-mapped mode. |
| 0 | Always set to 0. |

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DEVICE ADDRESS REGISTER

The Device Address register is used to maintain compatibility with ATA disk drive interfaces.

Table 45: Device Address Register

| Operation | D ₇ | D ₆ | D ₅ | D ₄ | D ₃ | D ₂ | D ₁ | D ₀ |
|---------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|
| Read/Write | - | nWTG | nHS3 | nHS2 | nHS1 | nHS0 | nDS1 | nDS0 |
| Default Value | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 0 |

| Bit(s) | Description |
|--------|--|
| 7 | Reserved bit. |
| 6 | Write Gate (nWTG) . Low when a write to the device is in process. |
| 5-2 | nHS3 to nHS0 . The negated binary address of the currently selected head. |
| 1 | nDS1 . Low when drive 1 is selected and active. |
| 0 | nDS0 . Low when drive 0 is selected and active. |

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ATA COMMAND BLOCK AND SET DESCRIPTION

In accordance with the *ANSI ATA Specification*, the device implements seven registers that are used to transfer instructions to the device by the host. These commands follow the ANSI standard ATA protocol. A description of the ATA command block is provided in the following table.

Table 46: ATA Command Block and Set Description

| Operation | D ₇ | D ₆ | D ₅ | D ₄ | D ₃ | D ₂ | D ₁ | D ₀ |
|---------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|
| Feature | | | | | X | | | |
| Sector Count | | | | | X | | | |
| Sector Number | | | | | X | | | |
| Cylinder Low | | | | | X | | | |
| Cylinder High | | | | | X | | | |
| Drive Head | 1 | LBA | 1 | Drive | | | X | |
| Command | | | | | X | | | |

ATA COMMAND SET

Table 47: ATA Command Set

| Class | Command Name | Command Code | Registers Used | | | | | |
|-------|-----------------------------|--------------|----------------|----|----|----|----|-----|
| | | | FR | SC | SN | CY | DH | LBA |
| 1 | Check Power Mode | 98h, E5h | - | - | - | - | D | - |
| 1 | Execute Drive Diagnostics | 90h | - | - | - | - | D | - |
| 1 | Erase Sector | C0h | - | Y | Y | Y | Y | Y |
| 2 | Format Track | 50h | - | Y | - | Y | Y | Y |
| 1 | Identify Drive | ECh | - | - | - | - | D | - |
| 1 | Idle | 97h, E3h | - | Y | - | - | D | - |
| 1 | Idle Immediate | 95h, E1h | - | | - | - | D | - |
| 1 | Initialize Drive Parameters | 91h | - | Y | - | - | Y | - |
| 1 | Read Buffer | E4h | - | - | - | - | D | - |
| 1 | Read DMA* | C8h | - | Y | Y | Y | Y | Y |
| 1 | Read Multiple | C4h | - | Y | Y | Y | Y | Y |

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Table 47: ATA Command Set (Continued)

| Class | Command Name | Command Code | Registers Used | | | | | |
|-------|---------------------------|--------------|----------------|----|----|----|----|-----|
| | | | FR | SC | SN | CY | DH | LBA |
| 1 | Read Long Sector | 22h, 23h | - | - | Y | Y | Y | Y |
| 1 | Read Sector(s) | 20h, 21h | - | - | Y | Y | Y | Y |
| 1 | Read Verify Sector(s) | 40h, 41h | - | Y | Y | Y | Y | Y |
| 1 | Recalibrate | 1Xh | - | - | - | - | Y | - |
| 1 | Request Sense | 03h | - | - | - | - | D | - |
| 1 | Seek | 7Xh | - | - | Y | Y | Y | Y |
| 1 | Set Features | EFh | Y | - | - | - | D | - |
| 1 | Set Multiple Mode | C6h | - | Y | - | - | D | - |
| 1 | Set Sleep Mode | 99h, E6h | - | - | - | - | D | - |
| 1 | Standby | 96h, E2h | - | - | - | - | D | - |
| 1 | Standby Immediate | 94h, E0h | - | - | - | - | D | - |
| 1 | Translate Sector | 87h | - | Y | Y | Y | Y | Y |
| 1 | Wear Level | F5h | - | - | - | - | Y | - |
| 2 | Write Buffer | E8h | - | - | - | - | D | - |
| 1 | Write DMA* | CAh | - | Y | Y | Y | Y | Y |
| 2 | Write Long Sector | 32h, 33h | - | - | Y | Y | Y | Y |
| 3 | Write Multiple | C5h | - | Y | Y | Y | Y | Y |
| 3 | Write Multiple w/o Erase | CDh | - | Y | Y | Y | Y | Y |
| 2 | Write Sector(s) | 30h, 31h | - | Y | Y | Y | Y | Y |
| 2 | Write Sector(s) w/o Erase | 38h | - | Y | Y | Y | Y | Y |
| 3 | Write Verify | 3Ch | - | Y | Y | Y | Y | Y |

* = This function does not apply to SiliconDrives that have DMA disabled.

Notes:

- CY = Cylinder
- SC = Sector Count
- DH = Drive/Head
- SN = Sector Number
- FR = Feature LBA — LBA bit of the Drive/Head register (D denotes that only the drive bit is used)

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Check Power Mode — 98h, E5h

The Check Power Mode command verifies the device's current power mode. When the device is configured for standby mode or is entering or exiting standby, the BSY bit is set, the Sector Count register set to 00h, and the BSY bit is cleared. In idle mode, BSY is set and the Sector Count register is set to FFh. The BSY bit is then cleared and an interrupt is issued.

Table 48: Check Power Mode — 98h, E5h

| Register | D ₇ | D ₆ | D ₅ | D ₄ | D ₃ | D ₂ | D ₁ | D ₀ |
|---------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|
| Feature | | | | | X | | | |
| Sector Count | | | | | X | | | |
| Sector Number | | | | | X | | | |
| Cylinder Low | | | | | X | | | |
| Cylinder High | | | | | X | | | |
| Drive Head | X | X | X | Drive | | | | |
| Command | | | | | | | | 98h or E5h |

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Executive Drive Diagnostic — 90h

The Executive Drive Diagnostic performs an internal read write diagnostic test using (AA55h and 55AAh). If an error is detected in the read/write buffer, the Error register reports the appropriate diagnostic code.

Table 49: Executive Drive Diagnostic — 90h

| Register | D ₇ | D ₆ | D ₅ | D ₄ | D ₃ | D ₂ | D ₁ | D ₀ |
|---------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|
| Feature | | | | | X | | | |
| Sector Count | | | | | X | | | |
| Sector Number | | | | | X | | | |
| Cylinder Low | | | | | X | | | |
| Cylinder High | | | | | X | | | |
| Drive Head | X | X | X | | | | | Drive |
| Command | | | | | | | | 90h |

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Format Track — 50h

The Format Track command formats the common solid-state memory array.

Table 50: Format Track — 50h

| Register | D ₇ | D ₆ | D ₅ | D ₄ | D ₃ | D ₂ | D ₁ | D ₀ |
|---------------|--------------------------|----------------|----------------|----------------|------------------------|----------------|----------------|----------------|
| Feature | X | | | | | | | |
| Sector Count | Sector Count | | | | | | | |
| Sector Number | Sector Number (LBA7-0) | | | | | | | |
| Cylinder Low | Cylinder Low (LBA15-8) | | | | | | | |
| Cylinder High | Cylinder High (LBA23-16) | | | | | | | |
| Drive Head | 1 | LBA | 1 | Drive | Head Number (LBA27-24) | | | |
| Command | 50h | | | | | | | |

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Identify Drive — ECh

Issued by the host, the Identify Drive command provides 256 bytes of drive attribute data (i.e., sector size, count, and so on) The identify drive data structure is detailed in the following table.

Table 51: Identify Drive — ECh

| Register | D ₇ | D ₆ | D ₅ | D ₄ | D ₃ | D ₂ | D ₁ | D ₀ |
|---------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|
| Feature | | | | | X | | | |
| Sector Count | | | | | X | | | |
| Sector Number | | | | | X | | | |
| Cylinder Low | | | | | X | | | |
| Cylinder High | | | | | X | | | |
| Drive Head | X | X | X | Drive | | | X | |
| Command | | | | | ECh | | | |

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*Identify Drive — Drive Attribute Data***Table 52: Identify Drive — Drive Attribute Data**

| Word Address | Data Default | Bytes | Data Description |
|--------------|--|-------|---|
| 0 | 044Ah (fixed ID bit) in IDE mode 848A (removable ID bit) in PCMCIA memory and I/O modes | 2 | General configuration bit information <ul style="list-style-type: none"> • 15: Non-magnetic disk • 14: Formatting speed latency permissible gap needed • 13: Track Offset option supported • 12: Data Strobe Offset option supported • 11: Over 0.5% rotational speed difference • 10: Disk transfer rate >10Mbps • 9: 10Mbps >= disk transfer rate >5Mbps • 8: 5Mbps >= disk transfer rate • 7: Removable cartridge drive • 6: Fixed drive • 5: Spindle Motor Control option executed • 4: Over 15μs changing head time • 3: Non-MFM encoding • 2: Soft sector allocation • 1: Hard sector allocation • 0: Reserved |
| 1 | XXXXh | 2 | Number of cylinders |
| 2 | 0000h | 2 | Reserved |
| 3 | 00XXh | 2 | Number of heads |
| 4 | 0000h | 2 | Number of unformatted bytes per track |
| 5 | XXXXh | 2 | Number of unformatted bytes per sector |
| 6 | XXXXh | 2 | Number of sectors per track |
| 7-8 | XXXXh | 4 | Number of sectors per device |
| 9 | 0000h | 2 | Reserved |
| 10-19 | XXXXh | 20 | Serial number |

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Table 52: Identify Drive — Drive Attribute Data (Continued)

| Word Address | Data Default | Bytes | Data Description |
|--------------|--------------|-------|--|
| 20 | 0002h | 2 | Buffer type <ul style="list-style-type: none"> • 0000h: Not specified • 0001h: A single-ported, single-sector buffer • 0002h: A dual-ported multisector buffer • 0003h: A dual-ported multisector buffer with a read caching |
| 21 | 0002h | 2 | Buffer size in 512-byte increments |
| 22 | 0004h | 2 | Number of ECC bytes passed on read/write long commands |
| 23-26 | XXXXh | 8 | Firmware revision (eight ASCII characters) |
| 27-46 | XXXXh | 40 | Model number (40 ASCII characters) |
| 47 | 0001h | 2 | 7-0: Maximum number of sectors that can be transferred with a Read/Write Multiple command per interrupt |
| 48 | 0000h | 2 | Double word (32 bit) not supported |
| 49 | 0002h | 2 | <ul style="list-style-type: none"> • 11: IORDY supported • 9: LBA supported • 8: DMA supported |
| 50 | 0000h | 2 | Reserved |
| 51 | 0100h | 2 | 15-8: PIO data transfer cycle timing |
| 52 | 0000h | 2 | 15-8: DMA data transfer cycle timing |
| 53 | 0000h | 2 | <ul style="list-style-type: none"> • 1: Words 64-70 are valid • 0: Words 54-58 are valid |
| 54 | XXXXh | 2 | Current number of cylinders |
| 55 | XXXXh | 2 | Current number of heads |
| 56 | XXXXh | 2 | Current sectors per track |
| 57-58 | XXXXh | 4 | Current capacity in sectors |
| 59 | 010Xh | 2 | 7-0: Current sectors can be transferred with a Read/Write Multiple command per interrupt |
| 60-61 | XXXXh | 4 | Total number of sectors addressable in LBA mode |
| 62 | 0000h | 2 | Single-word DMA modes supported |

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Table 52: Identify Drive — Drive Attribute Data (Continued)

| Word Address | Data Default | Bytes | Data Description |
|--------------|--------------|-------|---|
| 63 | 0407h | 2 | Multiword DMA modes supported |
| 64 | 0003h | 2 | PIO modes supported |
| 65 | 0078h | 2 | Minimum DMA transfer cycle time per word (ns) |
| 66 | 0078h | 2 | Manufacturer's recommended DMA transfer cycle time (ns) |
| 67 | 0078h | 2 | Minimum PIO transfer cycle time without flow control (ns) |
| 68 | 0078h | 2 | Minimum PIO transfer cycle time with IORDY flow controls (ns) |
| 69-127 | 0000h | 118 | Reserved |
| 128-159 | 0000h | 64 | Vendor-unique |
| 160-255 | 0000h | 192 | Reserved |

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Idle — 97h, E3h

When issued by the host, the device's internal controller sets the BSY bit, enters the Idle mode, clears the BSY bit, and generates an interrupt. If the sector count is non-zero, it is interpreted as a timer count with each count being 5ms, and the automatic power-down mode is enabled. If the sector count is zero, the automatic power-down mode is disabled.

Table 53: Idle — 97h, E3h

| Register | D ₇ | D ₆ | D ₅ | D ₄ | D ₃ | D ₂ | D ₁ | D ₀ |
|---------------|------------------------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|
| Feature | X | | | | | | | |
| Sector Count | Timer Count (5ms increments) | | | | | | | |
| Sector Number | X | | | | | | | |
| Cylinder Low | X | | | | | | | |
| Cylinder High | X | | | | | | | |
| Drive Head | X | X | X | Drive | X | | | |
| Command | 97h or E3h | | | | | | | |

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Idle Immediate — 95h, E1h

When issued by the host, the device's internal controller sets the BSY bit, enters Idle Mode, clears the BSY bit, and issues an interrupt. The interrupt is issued whether or not the Idle mode is fully entered.

Table 54: Idle Immediate — 95h, E1h

| Register | D ₇ | D ₆ | D ₅ | D ₄ | D ₃ | D ₂ | D ₁ | D ₀ |
|---------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|
| Feature | | | | | X | | | |
| Sector Count | | | | | X | | | |
| Sector Number | | | | | X | | | |
| Cylinder Low | | | | | X | | | |
| Cylinder High | | | | | X | | | |
| Drive Head | X | X | X | Drive | | | X | |
| Command | 95h or E1h | | | | | | | |

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Initialize Drive Parameters — 91h

Initialize Drive Parameters allows the host to set the sector counts per track and the head counts per cylinder to 1 Fixed. Upon issuance of the command, the device sets the BSY bit and associated parameters, clears the BSY bit, and issues an interrupt.

Table 55: Initialize Drive Parameters — 91h

| Register | D ₇ | D ₆ | D ₅ | D ₄ | D ₃ | D ₂ | D ₁ | D ₀ |
|---------------|----------------------------------|----------------|----------------|----------------|--------------------------------------|----------------|----------------|----------------|
| Feature | X | | | | | | | |
| Sector Count | Sector Count (Number of Sectors) | | | | | | | |
| Sector Number | X | | | | | | | |
| Cylinder Low | X | | | | | | | |
| Cylinder High | X | | | | | | | |
| Drive Head | X | 0 | X | Drive | Head Number (Number of Heads — 1) | | | |
| Command | 91h | | | | | | | |

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Recalibrate — 1Xh

The Recalibrate command sets the cylinder low and high, head number to 0h, and sector number to 1h in CHS mode. In LBA mode (i.e., LBA = 1), the sector number is set to 0h.

Table 56: Recalibrate — 1Xh

| Register | D ₇ | D ₆ | D ₅ | D ₄ | D ₃ | D ₂ | D ₁ | D ₀ |
|---------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|
| Feature | | | | | X | | | |
| Sector Count | | | | | X | | | |
| Sector Number | | | | | X | | | |
| Cylinder Low | | | | | X | | | |
| Cylinder High | | | | | X | | | |
| Drive Head | 1 | LBA | 1 | Drive | | | X | |
| Command | | | | | | | | 1Xh |

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Read Buffer — E4h

The Read Buffer command allows the host to read the contents of the sector buffer. When issued, the device sets the BSY bit and sets up the sector buffer data in preparation for the read operation. When the data is ready, the DRQ bit is set and the BSY bit in the Status register are set and cleared, respectively.

Table 57: Read Buffer — E4h

| Register | D ₇ | D ₆ | D ₅ | D ₄ | D ₃ | D ₂ | D ₁ | D ₀ |
|---------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|
| Feature | | | | | X | | | |
| Sector Count | | | | | X | | | |
| Sector Number | | | | | X | | | |
| Cylinder Low | | | | | X | | | |
| Cylinder High | | | | | X | | | |
| Drive Head | X | X | X | Drive | | | X | |
| Command | | | | | E4h | | | |

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Read DMA — C8h

The Read DMA command allows the host to read data using the DMA transfer protocol.

Note: This function does not apply to SiliconDrives that have DMA disabled.

Table 58: Read DMA — C8h

| Register | D ₇ | D ₆ | D ₅ | D ₄ | D ₃ | D ₂ | D ₁ | D ₀ |
|---------------|--------------------------|----------------|----------------|----------------|------------------------|----------------|----------------|----------------|
| Feature | X | | | | | | | |
| Sector Count | Sector Count | | | | | | | |
| Sector Number | Sector Number (LBA7-0) | | | | | | | |
| Cylinder Low | Cylinder Low (LBA15-8) | | | | | | | |
| Cylinder High | Cylinder High (LBA23-16) | | | | | | | |
| Drive Head | 1 | LBA | 1 | Drive | Head Number (LBA27-24) | | | |
| Command | C8h | | | | | | | |

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Read Multiple — C4h

The Read Multiple command executes similarly to the Read Sector command, with the exception that interrupts are issued only when a block containing the counts of sectors defined by the Set Multiple command is transferred.

Table 59: Read Multiple — C4h

| Register | D ₇ | D ₆ | D ₅ | D ₄ | D ₃ | D ₂ | D ₁ | D ₀ |
|---------------|--------------------------|----------------|----------------|----------------|------------------------|----------------|----------------|----------------|
| Feature | X | | | | | | | |
| Sector Count | Sector Count | | | | | | | |
| Sector Number | Sector Number (LBA7-0) | | | | | | | |
| Cylinder Low | Cylinder Low (LBA15-8) | | | | | | | |
| Cylinder High | Cylinder High (LBA23-16) | | | | | | | |
| Drive Head | 1 | LBA | 1 | Drive | Head Number (LBA27-24) | | | |
| Command | C4h | | | | | | | |

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Read Sector — 20h, 21h

The Read Sector command allows the host to read sectors 1 to 256 as specified in the Sector Count register. If the sector count is set to 0h, all 256 sectors of data are made available. When the command code is issued and the first sector of data has been transferred to the buffer, the DRQ bit is set. The Read Sector command is terminated by writing the cylinder, head, and sector number of the last sector read in the task file. On error, the read operation is aborted in the errant sector.

Table 60: Read Sector — 20h, 21h

| Register | D ₇ | D ₆ | D ₅ | D ₄ | D ₃ | D ₂ | D ₁ | D ₀ |
|---------------|--------------------------|----------------|----------------|----------------|------------------------|----------------|----------------|----------------|
| Feature | X | | | | | | | |
| Sector Count | Sector Count | | | | | | | |
| Sector Number | Sector Number (LBA7-0) | | | | | | | |
| Cylinder Low | Cylinder Low (LBA15-8) | | | | | | | |
| Cylinder High | Cylinder High (LBA23-16) | | | | | | | |
| Drive Head | 1 | LBA | 1 | Drive | Head Number (LBA27-24) | | | |
| Command | 20h or 21h | | | | | | | |

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Read Long Sector(s) — 22h, 23h

The Read Long Sector(s) command operates similarly to the Read Sector(s) command, with the exception that it transfers requested data sectors and ECC data. The long instruction ECC byte transfer for Long commands is a byte transfer at a fixed length of 4 bytes.

Table 61: Read Long Sector(s) — 22h, 23h

| Register | D ₇ | D ₆ | D ₅ | D ₄ | D ₃ | D ₂ | D ₁ | D ₀ |
|---------------|--------------------------|----------------|----------------|----------------|------------------------|----------------|----------------|----------------|
| Feature | X | | | | | | | |
| Sector Count | X | | | | | | | |
| Sector Number | Sector Number (LBA7-0) | | | | | | | |
| Cylinder Low | Cylinder Low (LBA15-8) | | | | | | | |
| Cylinder High | Cylinder High (LBA23-16) | | | | | | | |
| Drive Head | 1 | LBA | 1 | Drive | Head Number (LBA27-24) | | | |
| Command | 22h or 23h | | | | | | | |

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Read Verify Sector(s) — 40h, 41h

The Read Verify Sector(s) command operates similarly to the Read Sector(s) command, with the exception that it does not set the DRQ bit and does not transfer data to the host. When the requested sectors are verified, the onboard controller clears the BSY bit and issues an interrupt.

Table 62: Read Verify Sector(s) — 40h, 41h

| Register | D ₇ | D ₆ | D ₅ | D ₄ | D ₃ | D ₂ | D ₁ | D ₀ |
|---------------|--------------------------|----------------|----------------|----------------|------------------------|----------------|----------------|----------------|
| Feature | X | | | | | | | |
| Sector Count | Sector Count | | | | | | | |
| Sector Number | Sector Number (LBA7-0) | | | | | | | |
| Cylinder Low | Cylinder Low (LBA15-8) | | | | | | | |
| Cylinder High | Cylinder High (LBA23-16) | | | | | | | |
| Drive Head | 1 | LBA | 1 | Drive | Head Number (LBA27-24) | | | |
| Command | 40h or 41h | | | | | | | |

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Seek — 7Xh

The Seek command seeks and picks up the head to the tracks specified in the task file. When the command is issued, the solid-state memory chips do not need to be formatted. After an appropriate amount of time, the DSC bit is set.

Table 63: Seek — 7Xh

| Register | D ₇ | D ₆ | D ₅ | D ₄ | D ₃ | D ₂ | D ₁ | D ₀ |
|---------------|--------------------------|----------------|----------------|----------------|------------------------|----------------|----------------|----------------|
| Feature | X | | | | | | | |
| Sector Count | X | | | | | | | |
| Sector Number | Sector Number (LBA7-0) | | | | | | | |
| Cylinder Low | Cylinder Low (LBA15-8) | | | | | | | |
| Cylinder High | Cylinder High (LBA23-16) | | | | | | | |
| Drive Head | 1 | LBA | 1 | Drive | Head Number (LBA27-24) | | | |
| Command | 7Xh | | | | | | | |

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Set Features — EFh

The Set Features command allows the host to configure the feature set of the device according to the attributes listed in [Table 65](#).

Table 64: Set Features — EFh

| Register | D ₇ | D ₆ | D ₅ | D ₄ | D ₃ | D ₂ | D ₁ | D ₀ |
|---------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|
| Feature | Feature | | | | | | | |
| Sector Count | X | | | | | | | |
| Sector Number | X | | | | | | | |
| Cylinder Low | X | | | | | | | |
| Cylinder High | X | | | | | | | |
| Drive Head | X | X | X | Drive | X | | | |
| Command | EFh | | | | | | | |

Table 65: Set Features' Attributes

| Feature | Operation |
|---------|---|
| 01h | Enable 8-bit data transfer |
| 66h | Disable reverting to power on defaults |
| 81h | Disable 8-bit data transfer |
| BBh | 4 bytes of data apply on Read/Write Long commands |
| CCh | Enable revert to power on defaults |

On power-up or following a hardware reset, the device is set to the default mode 81h.

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Set Multiple Mode — C6h

The Set Multiple Mode command allows the host to access the drive via Read Multiple and Write Multiple ATA commands. Additionally, the command sets the block count (i.e., the number of sectors within the block) for the Read/Write Multiple command. The sector count per block is set in the Sector Count register.

Table 66: Set Multiple Mode — C6h

| Register | D ₇ | D ₆ | D ₅ | D ₄ | D ₃ | D ₂ | D ₁ | D ₀ |
|---------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|
| Feature | X | | | | | | | |
| Sector Count | Sector Count | | | | | | | |
| Sector Number | X | | | | | | | |
| Cylinder Low | X | | | | | | | |
| Cylinder High | X | | | | | | | |
| Drive Head | X | X | X | Drive | X | | | |
| Command | C6h | | | | | | | |

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Set Sleep Mode — 99h, E6h

The Set Sleep Mode command allows the host to set the device in sleep mode. When the onboard controller transitions to sleep mode, it clears the BSY bit and issues an interrupt. The device interface then becomes inactive. Sleep mode can be exited by issuing either a hardware or software reset.

Table 67: Set Sleep Mode — 99h, E6h

| Register | D ₇ | D ₆ | D ₅ | D ₄ | D ₃ | D ₂ | D ₁ | D ₀ |
|---------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|
| Feature | | | | | X | | | |
| Sector Count | | | | | X | | | |
| Sector Number | | | | | X | | | |
| Cylinder Low | | | | | X | | | |
| Cylinder High | | | | | X | | | |
| Drive Head | X | X | X | Drive | | | X | |
| Command | | | | | | | | 99h or E6h |

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Standby — 96h, E2h

When the Standby command is issued by the host, it transitions the device into standby mode. If the Sector Count register is set to a value other than 0h, the Auto Powerdown function is enabled and the device returns to Idle mode.

Table 68: Standby — 96h, E2h

| Register | D ₇ | D ₆ | D ₅ | D ₄ | D ₃ | D ₂ | D ₁ | D ₀ |
|---------------|---------------------------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|
| Feature | X | | | | | | | |
| Sector Count | Timer Count (5ms x Timer Count) | | | | | | | |
| Sector Number | X | | | | | | | |
| Cylinder Low | X | | | | | | | |
| Cylinder High | X | | | | | | | |
| Drive Head | X | X | X | Drive | X | | | |
| Command | 96h or E2h | | | | | | | |

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Standby Immediate — 94h, E0h

When the Standby Immediate command is issued by the host, it transitions the device into standby mode.

Table 69: Standby Immediate — 94h, E0h

| Register | D ₇ | D ₆ | D ₅ | D ₄ | D ₃ | D ₂ | D ₁ | D ₀ |
|---------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|
| Feature | | | | | X | | | |
| Sector Count | | | | | X | | | |
| Sector Number | | | | | X | | | |
| Cylinder Low | | | | | X | | | |
| Cylinder High | | | | | X | | | |
| Drive Head | X | X | X | Drive | | | X | |
| Command | 94h or E0h | | | | | | | |

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Write Buffer — E8h

The Write Buffer command allows the host to rewrite the contents of the 512- byte data buffer with the wanted data.

Table 70: Write Buffer — E8h

| Register | D ₇ | D ₆ | D ₅ | D ₄ | D ₃ | D ₂ | D ₁ | D ₀ |
|---------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|
| Feature | | | | | X | | | |
| Sector Count | | | | | X | | | |
| Sector Number | | | | | X | | | |
| Cylinder Low | | | | | X | | | |
| Cylinder High | | | | | X | | | |
| Drive Head | X | X | X | Drive | | | X | |
| Command | E8h | | | | | | | |

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Write DMA — CAh

The Write DMA command allows the host to write data using the DMA transfer protocol.

Note: This function does not apply to SiliconDrives that have DMA disabled.

Table 71: Write DMA — CAh

| Register | D ₇ | D ₆ | D ₅ | D ₄ | D ₃ | D ₂ | D ₁ | D ₀ |
|---------------|-------------------------|----------------|----------------|----------------|-----------------------|----------------|----------------|----------------|
| Feature | X | | | | | | | |
| Sector Count | Sector Count | | | | | | | |
| Sector Number | Sector Number (LBA7-0) | | | | | | | |
| Cylinder Low | Cylinder Low(LBA15-8) | | | | | | | |
| Cylinder High | Cylinder High(LBA23-16) | | | | | | | |
| Drive Head | X | LBA | X | Drive | Head Number(LBA27-24) | | | |
| Command | CAh | | | | | | | |

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Write Multiple — C5h

The Write Multiple command operates in the same manner as the Write Sector command. When issued, the device sets the BSY bit within 400ns and generates an interrupt at the completion of a transferred block of sectors. The DRQ bit is set at the beginning of a block transfer.

Table 72: Write Multiple — C5h

| Register | D ₇ | D ₆ | D ₅ | D ₄ | D ₃ | D ₂ | D ₁ | D ₀ |
|---------------|-------------------------|----------------|----------------|----------------|-----------------------|----------------|----------------|----------------|
| Feature | X | | | | | | | |
| Sector Count | Sector Count | | | | | | | |
| Sector Number | Sector Number (LBA7-0) | | | | | | | |
| Cylinder Low | Cylinder Low(LBA15-8) | | | | | | | |
| Cylinder High | Cylinder High(LBA23-16) | | | | | | | |
| Drive Head | X | LBA | X | Drive | Head Number(LBA27-24) | | | |
| Command | C5h | | | | | | | |

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Write Sector(s) — 30h, 31h

The Write Sector(s) command writes from 1 to 256 sectors as specified in the Sector Count register. A sector count of 0 requests 256 sectors. When issued, the device sets the BSY bit within 400ns and generates an interrupt at the completion of a transferred block of sectors. The DRQ bit is set at the beginning of a block transfer.

Table 73: Write Sector(s) — 30h, 31h

| Register | D ₇ | D ₆ | D ₅ | D ₄ | D ₃ | D ₂ | D ₁ | D ₀ |
|---------------|--------------------------|----------------|----------------|----------------|------------------------|----------------|----------------|----------------|
| Feature | X | | | | | | | |
| Sector Count | Sector Count | | | | | | | |
| Sector Number | Sector Number (LBA7-0) | | | | | | | |
| Cylinder Low | Cylinder Low (LBA15-8) | | | | | | | |
| Cylinder High | Cylinder High (LBA23-16) | | | | | | | |
| Drive Head | X | LBA | X | Drive | Head Number (LBA27-24) | | | |
| Command | 30h or 31h | | | | | | | |

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Write Long Sector(s) — 32h, 33h

The Write Long Sector(s) command operates in the same manner as the Write Sector command — when issued, the device sets the BSY bit within 400ns and generates an interrupt at the completion of a transferred block of sectors. The DRQ bit is set at the beginning of a block transfer.

Table 74: Write Long Sector(s) — 32h, 33h

| Register | D ₇ | D ₆ | D ₅ | D ₄ | D ₃ | D ₂ | D ₁ | D ₀ |
|---------------|--------------------------|----------------|----------------|----------------|------------------------|----------------|----------------|----------------|
| Feature | X | | | | | | | |
| Sector Count | Sector Count | | | | | | | |
| Sector Number | Sector Number (LBA7-0) | | | | | | | |
| Cylinder Low | Cylinder Low (LBA15-8) | | | | | | | |
| Cylinder High | Cylinder High (LBA23-16) | | | | | | | |
| Drive Head | X | LBA | X | Drive | Head Number (LBA27-24) | | | |
| Command | 32h or 33h | | | | | | | |

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Erase Sector(s) — C0h

The Erase Sector(s) command is issued prior to the issuance of a Write Sector(s) or Write Multiple w/o Erase command.

Table 75: Erase Sector(s) — C0h

| Register | D ₇ | D ₆ | D ₅ | D ₄ | D ₃ | D ₂ | D ₁ | D ₀ |
|---------------|--------------------------|----------------|----------------|----------------|------------------------|----------------|----------------|----------------|
| Feature | X | | | | | | | |
| Sector Count | Sector Count | | | | | | | |
| Sector Number | Sector Number (LBA7-0) | | | | | | | |
| Cylinder Low | Cylinder Low (LBA15-8) | | | | | | | |
| Cylinder High | Cylinder High (LBA23-16) | | | | | | | |
| Drive Head | X | LBA | X | Drive | Head Number (LBA27-24) | | | |
| Command | C0h | | | | | | | |

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Request Sense — 03h

The Request Sense command identifies the extended error codes generated by the preceding ATA command. The Request Sense command must be issued immediately following the detection of an error via the Error register.

Table 76: Request Sense — 03h

| Register | D ₇ | D ₆ | D ₅ | D ₄ | D ₃ | D ₂ | D ₁ | D ₀ |
|---------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|
| Feature | | | | | X | | | |
| Sector Count | | | | | X | | | |
| Sector Number | | | | | X | | | |
| Cylinder Low | | | | | X | | | |
| Cylinder High | | | | | X | | | |
| Drive Head | 1 | X | 1 | Drive | | | X | |
| Command | | | | | | | | 03h |

The extended error codes are defined in the following table.

Table 77: Extended Error Codes

| Extended Error Codes | Description |
|-------------------------|--|
| 00h | No error detected |
| 01h | Self test is OK (no error) |
| 09h | Miscellaneous error |
| 20h | Invalid command |
| 21h | Invalid address (requested head or sector invalid) |
| 2Fh | Address overflow (address too large) |
| 35h, 36h | Supply or generated voltage out of tolerance |
| 11h | Uncorrectable ECC error |
| 18h | Corrected ECC error |
| 05h, 30h-32h, 37h, 3Eh | Self test of diagnostic failed |
| 10h, 14h | ID not found |
| 3Ah | Spare sectors exhausted |
| 1Fh | Data transfer error/aborted command |
| 0Ch, 38h, 3Bh, 3Ch, 3Fh | Computed media format |
| 03h | Write/erase failed |

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Translate Sector — 87h

The Translate Sector command is not currently supported by the SiliconSystems' SiliconDrive. If the host issues this command, the device responds with 0x00h in the data register.

Table 78: Translate Sector — 87h

| Register | D ₇ | D ₆ | D ₅ | D ₄ | D ₃ | D ₂ | D ₁ | D ₀ |
|---------------|--------------------------|----------------|----------------|----------------|------------------------|----------------|----------------|----------------|
| Feature | X | | | | | | | |
| Sector Count | Sector Count | | | | | | | |
| Sector Number | Sector Number (LBA7-0) | | | | | | | |
| Cylinder Low | Cylinder Low (LBA15-8) | | | | | | | |
| Cylinder High | Cylinder High (LBA23-16) | | | | | | | |
| Drive Head | 1 | LBA | 1 | Drive | Head Number (LBA27-24) | | | |
| Command | 87h | | | | | | | |

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Wear-Level — F5h

The Wear-Level command is supported as an NOP command for the purposes of backward compatibility with the ANSI AT attachment standard. This command sets the Sector Count register to 0x00h.

Table 79: Wear-Level — F5h

| Register | D ₇ | D ₆ | D ₅ | D ₄ | D ₃ | D ₂ | D ₁ | D ₀ |
|---------------|-------------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|
| Feature | X | | | | | | | |
| Sector Count | Completion Status | | | | | | | |
| Sector Number | X | | | | | | | |
| Cylinder Low | X | | | | | | | |
| Cylinder High | X | | | | | | | |
| Drive Head | X | X | X | Drive | Flag | | | |
| Command | F5h | | | | | | | |

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Write Multiple w/o Erase — CDh

The Write Multiple w/o Erase command functions identically to the Write Multiple command, with the exception that the implied pre-erase (i.e., Erase Sector(s) command) is not issued prior to writing the sectors.

Table 80: Write Multiple w/o Erase — CDh

| Register | D ₇ | D ₆ | D ₅ | D ₄ | D ₃ | D ₂ | D ₁ | D ₀ |
|---------------|--------------------------|----------------|----------------|----------------|------------------------|----------------|----------------|----------------|
| Feature | X | | | | | | | |
| Sector Count | Sector Count | | | | | | | |
| Sector Number | Sector Number (LBA7-0) | | | | | | | |
| Cylinder Low | Cylinder Low (LBA15-8) | | | | | | | |
| Cylinder High | Cylinder High (LBA23-16) | | | | | | | |
| Drive Head | X | LBA | X | Drive | Head Number (LBA27-24) | | | |
| Command | CDh | | | | | | | |

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Write Sector(s) w/o Erase — 38h

The Write Sector(s) w/o Erase command functions similar to the Write Sector command, with the exception that the implied pre-erase (i.e., Erase Sector(s) command) is not issued prior to writing the sectors.

Table 81: Write Sector(s) w/o Erase — 38h

| Register | D ₇ | D ₆ | D ₅ | D ₄ | D ₃ | D ₂ | D ₁ | D ₀ |
|---------------|--------------------------|----------------|----------------|----------------|------------------------|----------------|----------------|----------------|
| Feature | X | | | | | | | |
| Sector Count | Sector Count | | | | | | | |
| Sector Number | Sector Number (LBA7-0) | | | | | | | |
| Cylinder Low | Cylinder Low (LBA15-8) | | | | | | | |
| Cylinder High | Cylinder High (LBA23-16) | | | | | | | |
| Drive Head | X | LBA | X | Drive | Head Number (LBA27-24) | | | |
| Command | 38h | | | | | | | |

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Write Verify — 3Ch

The Write Verify command verifies each sector immediately after it is written. This command performs identically to the Write Sector(s) command, with the added feature of verifying each sector written.

Table 82: Write Verify — 3Ch

| Register | D ₇ | D ₆ | D ₅ | D ₄ | D ₃ | D ₂ | D ₁ | D ₀ |
|---------------|--------------------------|----------------|----------------|----------------|------------------------|----------------|----------------|----------------|
| Feature | X | | | | | | | |
| Sector Count | Sector Count | | | | | | | |
| Sector Number | Sector Number (LBA7-0) | | | | | | | |
| Cylinder Low | Cylinder Low (LBA15-8) | | | | | | | |
| Cylinder High | Cylinder High (LBA23-16) | | | | | | | |
| Drive Head | X | LBA | X | Drive | Head Number (LBA27-24) | | | |
| Command | 3Ch | | | | | | | |

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PART NUMBERING

NOMENCLATURE

The following table defines the SiliconDrive CF part numbering scheme.

Table 83: Part Numbering Nomenclature

| | | | | |
|------------------------------|----------|---|----------|---|
| SSD- | C | YYY | T | -3150 Part number suffix — contact your SiliconSystems' Sales Representative |
| | | | | Temperature Range: • Blank = Commercial • I = Industrial |
| | | Capacity: 32M = 32MB to 08G = 8GB | | |
| | | Form Factor: • C = CF • D = 2.5" Drive • M = Module • P = PC Card | | |
| SiliconSystems' SiliconDrive | | | | |

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PART NUMBERS

The following table lists the SiliconDrive's part numbers.

Table 84: Part Numbers

| Part Number | Capacity |
|------------------|----------|
| SSD-C08G(I)-3150 | 8GB |
| SSD-C04G(I)-3150 | 4GB |
| SSD-C02G(I)-3150 | 2GB |
| SSD-C01G(I)-3150 | 1GB |
| SSD-C51M(I)-3150 | 512MB |
| SSD-C25M(I)-3150 | 256MB |
| SSD-C12M(I)-3150 | 128MB |
| SSD-C64M(I)-3150 | 64MB |
| SSD-C32M(I)-3150 | 32MB |

SAMPLE LABEL

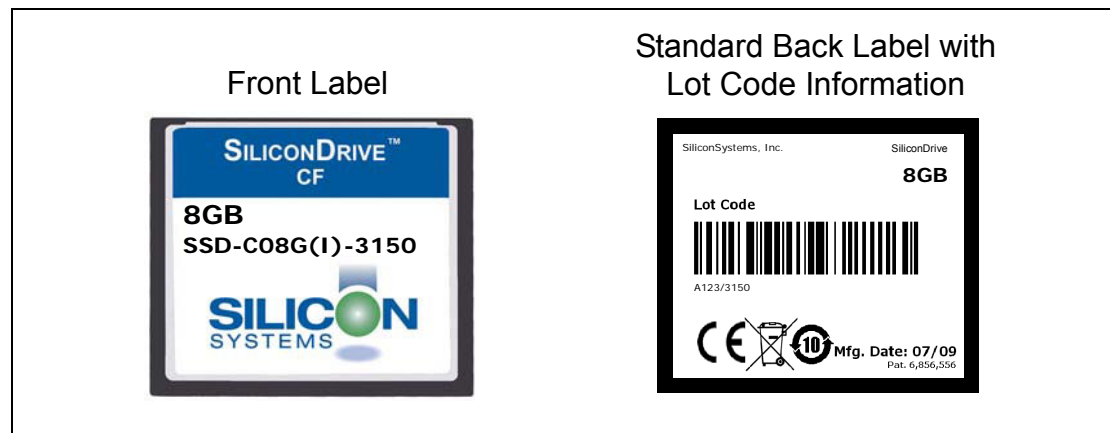


Figure 8: Sample Label

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RELATED DOCUMENTATION

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Table 85: Related Documentation

| SiliconDrive | | |
|---|---|------------------------|
| Application-Specific Description | | Document Number |
| Technology | | |
| PowerArmor | Eliminates drive corruption. | WP-007-0xR |
| SiProtect | Protection software for password-required, read/write, or read-only access. | WP-003-0xR |
| SiSweep | Ultra-fast data erasure. | SiSecure-0xANR |
| SiPurge | Non-recoverable data erasure. | SiSecure-0xANR |

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