SCH5027E

Super I/O with Temperature Sensing, Quiet Auto Fan and Glue Logic with PECI

PRODUCT FEATURES

Data Brief

- General Features
  - 3.3 Volt Operation (SIO Block is 5 Volt Tolerant)
  - LPC Interface
  - Programmable Wake-up Event Interface
  - PC99, PC2001 Compliant
  - ACPI 2.0 Compliant
  - Multiplexed Command, Address and Data Bus
  - Serial IRQ Interface Compatible with Serialized IRQ Support for PCI Systems
  - PME Interface
  - ISA Plug-and-Play Compatible Register Set
  - 25 General Purpose Input/Output Pins
  - System Management Interrupt
- PECI Interface
  - Supports PECI REQUEST# and PECI AVAILABLE signalling
- AC Power Failure Recovery
- Watchdog Timer
- 2.88MB Super I/O Floppy Disk Controller
  - Licensed CMOS 765B Floppy Disk Controller
  - Software and Register Compatible with SMSC's Proprietary 82077AA Compatible Core
  - Supports One Floppy Drive
  - Configurable Open Drain/Push-Pull Output Drivers
  - Supports Vertical Recording Format
  - 16-Byte Data FIFO
  - 100% IBM® Compatibility
  - Detects All Overrun and Underrun Conditions
  - Sophisticated Power Control Circuitry (PCC) Including Multiple Powerdown Modes for Reduced Power Consumption
  - DMA Enable Logic
  - Data Rate and Drive Control Registers
  - 480 Address, Up to Eight IRQ and Three DMA Options
  - Support 3 Mode FDD
- Enhanced Digital Data Separator
  - 2 Mbps, 1 Mbps, 500 Kbps, 300 Kbps, 250 Kbps Data Rates
  - Programmable Precompensation Modes
- Serial Ports
  - Two Full Function Serial Ports
  - High Speed NS16C550A Compatible UARTs with Send/Receive 16-Byte FIFOs
  - Supports 230k and 460k Baud
  - Programmable Baud Rate Generator
  - Modem Control Circuitry
  - 480 Address and 15 IRQ Options
- Infrared Port
  - Multiprotocol Infrared Interface
  - IrDA 1.0 Compliant
  - SHARP ASK IR
  - 480 Addresses, Up to 15 IRQ
- Multi-Mode™ Parallel Port with ChiProtect™
  - Standard Mode IBM PC/XT®, PC/AT®, and PS/2™ Compatible Bi-directional Parallel Port
  - Enhanced Parallel Port (EPP) Compatible - EPP 1.7 and EPP 1.9 (IEEE 1284 Compliant)
  - IEEE 1284 Compliant Enhanced Capabilities Port (ECP)
  - ChiProtect Circuitry for Protection
  - 960 Address, Up to 15 IRQ and Three DMA Options
- Keyboard Controller
  - 8042 Software Compatible
  - 8 Bit Microcomputer
  - 2k Bytes of Program ROM
  - 256 Bytes of Data RAM
  - Four Open Drain Outputs Dedicated for Keyboard/Mouse Interface
  - Asynchronous Access to Two Data Registers and One Status Register
  - Supports Interrupt and Polling Access
  - 8 Bit Counter Timer
  - Port 92 Support
  - Fast Gate A20 and KRESET Outputs
- Motherboard GLUE Logic
  - IDE Reset Output
  - (4) Buffered PCI Reset Outputs with software controlled reset capability - default transparent
  - Front Panel Reset Debouncing and Power Good Signal Generation
  - Power Supply Turn On Circuitry with Support for power button on PS/2 Keyboard
  - Resume Reset Signal Generation
  - SMBus Isolation Circuitry (2 sets external and 1 set internal for Hardware Monitoring Block)
  - SMBus 2.0 compliant interface for Hardware Monitoring
  - LED Control (2)
- Fan Control
  - 5 PWM (Pulse width Modulation) Outputs
  - Low frequency and high frequency PWM support
  - 6 Fan Tachometer Inputs
  - Programmable automatic fan control based on temperature
  - Interrupt Pin for out-of-limit Fantach Events
  - Fantach events generate PME's

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- Temperature Monitor
  - Monitoring of Two Remote Thermal Diodes
  - Processor temperature monitoring by PECI
  - Internal Ambient Temperature Measurement
  - Limit Comparison of all Monitored Values
  - Interrupt Pin for out-of-limit Temperature Indication
  - Thermal events generate PME's
  - Configurable offset for internal or external temperature channels.
- Voltage Monitor
  - Monitor Power supplies (2 at 1.125V, one at 5V, one each for Vccp, Vbat, VTR, and VCC)
  - Limit Comparison of all Monitored Values
  - Interrupt Pin for out-of-limit Voltage Indication
  - Voltage events generate PME's
- Security Features
  - Security Key Register (32 byte) for Device Authentication
- 3 VID (Voltage Identification) Inputs
- Phoenix Keyboard BIOS ROM
- 128 Pin QFP, Lead-Free RoHS Compliant Package

ORDER NUMBER:

SCH5027E-NW FOR 128 PIN, QFN LEAD-FREE ROHS COMPLIANT PACKAGE

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General Description

The SCH5027E is a 3.3V (Super I/O Block is 5V tolerant) PC99/PC2001 compliant Super I/O controller with an LPC interface. SCH5027E also includes Hardware Monitoring capabilities, enhanced Security features, Power Control logic and Motherboard Glue logic.

The SCH5027E's hardware monitoring capability includes temperature, voltage and fan speed monitoring. It has the ability to alert the system to out-of-limit conditions and automatically control the speeds of multiple fans. There are four analog inputs for monitoring external voltages, two at 1.125V, one at 5V and one at 2.25V for Vccp (core processor voltage). There is also internal monitoring of the SIO's VCC, VTR, and Vbat power supplies. The SCH5027E is capable of monitoring two external diodes, one internal ambient temperature sensor or retrieving temperatures from external processors that implement the PECI interface. The PECI implementation in the SCH5027E includes support for the PECI REQUEST# and PECI AVAILABLE signals that are used to wake processors from the C3/C4sleep states. There are three pulse width modulation (PWM) outputs with high frequency support that may be controlled by the auto fan block, as well as four fan tachometer inputs. There are two additional software controlled PWM inputs with associated tachometer inputs that may be used to monitor fans. The nHWM_INT pin is implemented to indicate out-of-limit temperature, voltage, and FANTACH conditions. The hardware monitoring block of the SCH5027E is accessible via the System Management Bus (SMBus). The same interrupt event reported on the nHWM_INT pin also creates PME wakeup events and speaker alarm annunciation.

The SCH5027E also allows for a two or three piece linear fan function.

The Motherboard Glue logic includes various power management and system logic including generation of nRSMRST, SMBus buffers, and buffered PCI reset outputs.

The SCH5027E incorporates complete legacy Super I/O functionality including an 8042 based keyboard and mouse controller, an IEEE 1284, EPP, and ECP compatible parallel port, one serial port that is 16C550A UART compatible, one IrDA 1.0 infrared ports, and a floppy disk controller with SMSC's true CMOS 765B core and enhanced digital data separator, The true CMOS 765B core provides 100% compatibility with IBM PC/XT and PC/AT architectures and is software and register compatible with SMSC's proprietary 82077AA core. System related functionality, which offers flexibility to the system designer, General Purpose I/O control functions, control of two LED's, and fan control using fan tachometer inputs and pulse width modulator (PWM) outputs.

The SCH5027E is ACPI 1.0/2.0 compatible and therefore supports multiple low power-down modes. It incorporates sophisticated power control circuitry (PCC), which includes support for keyboard and mouse wake-up events.

The SCH5027E supports the ISA Plug-and-Play Standard register set (Version 1.0a). The I/O Address, DMA Channel and hardware IRQ of each logical device in the SCH5027E may be reprogrammed through the internal configuration registers. There are up to 480 (960 - Parallel Port) I/O address location options, a Serialized IRQ interface, and Three DMA channels.

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Block Diagram

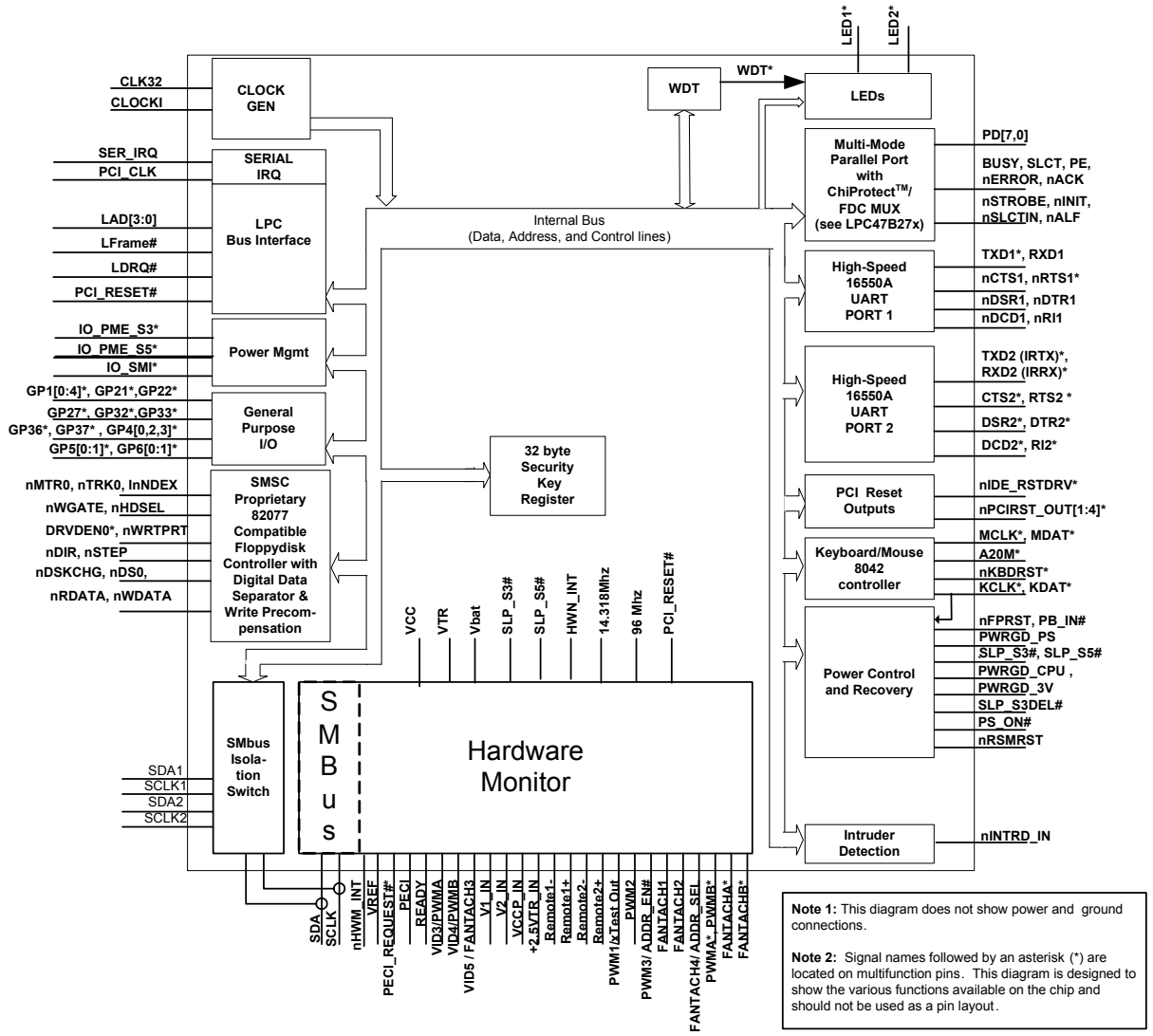

Figure 1 SCH5027E Block Diagram

PRODUCT PREVIEW

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Chapter 2 Package Outline

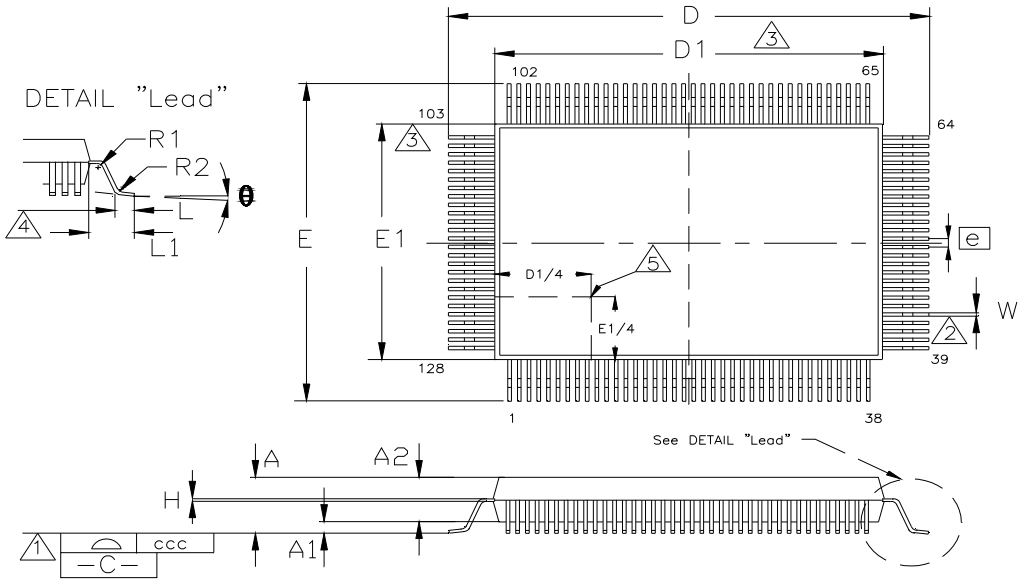

Figure 3 128 Pin QFP Package Outline, 14X20X2.7 Body, 3.2 mm Footprint

Table 1 128 Pin QFP Package Parameters

	MIN	NOMINAL	MAX	REMARKS
A	~	~	3.4	Overall Package Height
A1	0.05	~	0.5	Standoff
A2	2.55	~	3.05	Body Thickness
D	23.00	23.20	23.40	X Span
D1	19.90	20.00	20.10	X body Size
E	17.00	17.20	17.40	Y Span
E1	13.90	14.00	14.10	Y body Size
H	0.09	~	0.20	Lead Frame Thickness
L	0.73	0.88	1.03	Lead Foot Length
L1	~	1.60	~	Lead Length
e	0.50 Basic			Lead Pitch
q	0^o	~	7^o	Lead Foot Angle
W	0.10	~	0.30	Lead Width
R1	0.08	~	~	Lead Shoulder Radius
R2	0.08	~	0.30	Lead Foot Radius
ccc	~	~	0.08	Coplanarity

Notes:
1. Controlling Unit: millimeter.
2. Controlling Unit: millimeter.
3. Tolerance on the position of the leads is ± 0.04 mm maximum.
4. Package body dimensions D1 and E1 do not include the mold protrusion.
5. Maximum mold protrusion is 0.25 mm.
6. Dimension for foot length L measured at the gauge plane 0.25 mm above the seating plane.
7. Details of pin 1 identifier are optional but must be located within the zone indicated.

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