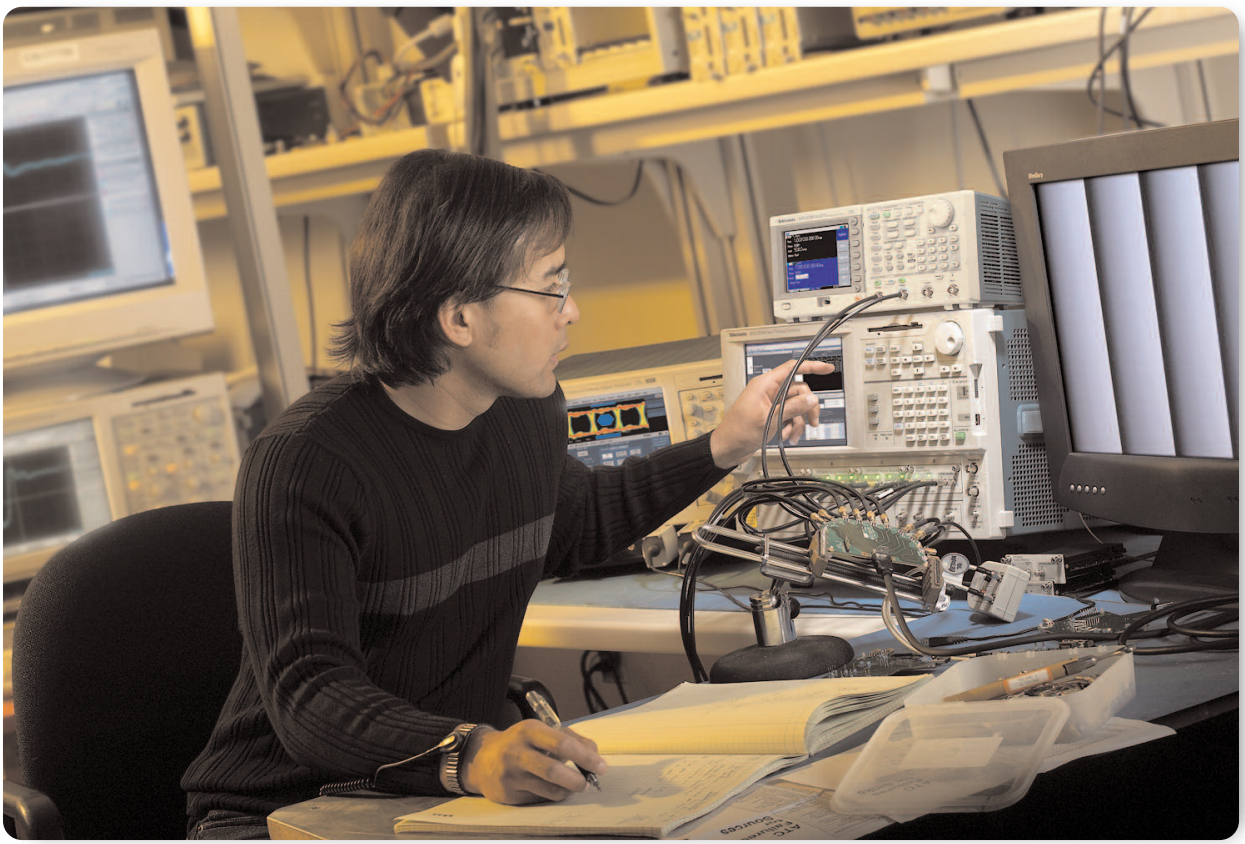
# HDMI Compliance and Sink Characterization Using the DTG5000 Series Data Timing Generator



## Introduction

The High Definition Multimedia Interface (HDMI) is an emerging consumer electronics standard that is fast gaining acceptance by manufacturers of digital entertainment products. HDMI offers an efficient one-cable interface for High Definition (HD) video and audio content between receiver/playback devices and display devices.

Typical receiver/playback devices include cable boxes, DVD players, satellite receivers, and High Definition tuners as well as personal computers. Display devices connected via HDMI include LCD displays, plasma displays, and projection units. Thanks to the simplicity of setup and the resulting quality of the presentation, consumers are accepting HDMI as a “must-have” item for the full HD experience.

HDMI uses the existing Digital Video Interface (DVI) architecture and adds capability for High Definition Audio and High-Bandwidth Digital Content Protection (HDCP). The latter technology enables true copy protection of high-quality digital movie content. HDCP is receiving an enthusiastic response from the entertainment industry, which is advocating its use in all HD consumer products.

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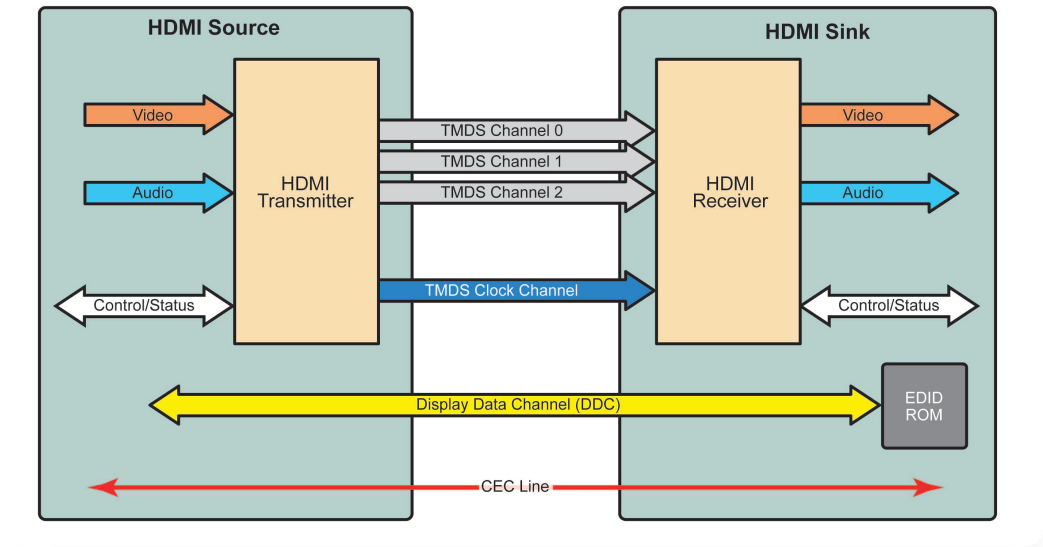



▶ **Figure 1.** *HDMI pixel data flow and organization from Source to Sink.*

HDMI supports standard, enhanced, or HD video as well as standard or multi-channel surround audio. The interface offers uncompressed digital video and a bandwidth of up to 5 gigabytes per second through one small connector instead of several cables and connectors as in the past. In addition, HDMI enables communication between the video source and the digital television (DTV). HDMI development is overseen by HDMI Founders including Sony, Hitachi, Panasonic (Matsushita Electric Industrial), Silicon Image, Philips, Thomson (RCA) and Toshiba.

The HDMI Founders have stipulated that all HDMI products must pass a battery of required compliance tests to qualify to use the HDMI logo. This compliance testing will ensure true interoperability and accordingly, customer satisfaction. Today, these tests can only be performed at an HDMI Authorized Testing Centers (ATC). Pre-compliance testing during the design and manufacturing stages greatly increases the likelihood of successfully passing the final compliance tests at the ATC. Pre-compliance testing can save valuable time and resources.

This technical brief discusses the equipment required for pre-compliance and compliance testing to the HDMI physical layer Compliance Test Specifications (CTS).

## HDMI Technical Characteristics

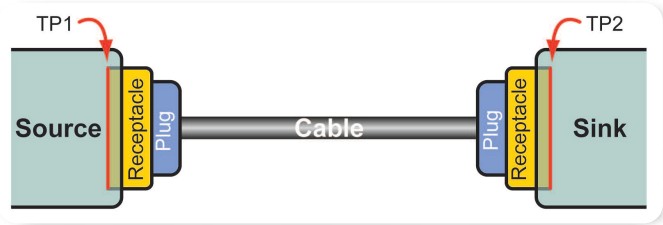
HDMI uses a high-speed serial interface that is based on transition-minimized differential signaling (TMDS) to send data to the receiver. TMDS signals transition between “on” and “off” states using an algorithm that minimizes the number of transitions to avoid excessive levels of electromagnetic interference (EMI) on the cable. The differential signal amplitude is +3.3 volts, terminated in 50 Ω with 500 mV nominal amplitude transitions (from +2.8 V to +3.3 V).

| Standard | Display Resolution | Data Rate | Clock Frequency |
|---|---|---|---|
| VGA | 640 x 480 | 252 Mb/s | 25.2 MHz |
| SVGA | 800 x 600 | 400 Mb/s | 40 MHz |
| XGA | 1024 x 768 | 650 Mb/s | 65 MHz |
| SXGA | 1280 x 1024 | 1080 Mb/s | 108 MHz |
| UXGA | 1600 x 1200 | 1620 Mb/s | 162 MHz |
| 640 x 480p | 640 x 480 | 252 Mb/s | 25.2 MHz |
| 720 x 480p | 720 x 480 | 270.27 Mb/s | 27.027 MHz |
| 576p | 768 x 576 | 270 Mb/s | 27 MHz |
| 720p | 1280 x 720 | 742.5 Mb/s | 74.25 MHz |
| 1080i | 1920 x 1080 | 742.5 Mb/s | 74.25 MHz |

▸ **Table 1.** *Standards and respective data rates.*

The basic TMDS transmission line is made up of three data channels and a clock channel. Data consists of 8-bit pixels (256 discrete levels) in each of three channels (R/G/B). These are encoded into ten-bits words using 8B/10B encoding to minimize transitions and to remove the DC component. The signals have rise times on the order of 100 picoseconds. A pair of TMDS lines is used when higher data rates are needed. Figure 1 shows the flow of pixel data from the graphics controller or Source device to the digital Sink receiver.

TMDS data rates range from 22.5 megapixels per second (Mpps) to 165 Mpps, equivalent to or up to 1.65 G bits per second at the maximum clock rate of 165 MHz. The data rate depends on the display resolution. The relationships of display resolution, bit rate and clock frequency are shown in the Table 1.




▸ **Figure 2.** *Test points for HDMI measurements.*

## Compliance Testing Tools and Solutions - DTG5000 Series

The goal of compliance testing is to ensure interoperability among the many hundreds of different HDMI devices from as many manufacturers. By conforming to published HDMI specifications, a device manufacturer can pave the way for a new product's acceptance in the marketplace.

Testing should also ensure that the designs are robust enough to withstand the harsh treatment they can expect to receive in the real world. As new displays become more rugged, the devices that use them will find their way into less sheltered environments than in the past. Therefore, new devices should be tested to comply with standards under a variety of operating conditions, not just “nominal” or best-case conditions. Test parameters should reach out beyond the basic limits defined in the specifications.

Figure 2 illustrates the major elements of the HDMI transmission system: Source, Cable and Sink. The Source signals are tested at TP1 while the Sink devices are tested at TP2. For testing cables, measurements must be performed at both TP1 and TP2.

| Electrical | Signals | Test | CTS Test ID | Test Point |
|---|---|---|---|---|
| Source | Clock and/or Data | Data Eye Diagram | 7-10 | TP1 |
| | | Clock Jitter | 7-9 | TP1 |
| | | Clock Duty Cycle | 7-8 | TP1 |
| | | Overshoot/Undershoot | 7-5 | TP1 |
| | | Rise/Fall Time | 7-4 | TP1 |
| | | Inter-pair Skew | 7-6 | TP1 |
| | Data-Data | Inter-pair Skew | 7-6 | TP1 |
| | Single-ended | Intra-pair Skew | 7-7 | TP1 |
| | | Low Level Output Voltage (VL) | 7-2 | TP1 |
| Sink | | Jitter Tolerance | 8-7 | TP2 |
| | | Minimum Differential Sensitivity | 8-5 | TP2 |
| | | Intra-pair Skew | 8-6 | TP2 |
| | | Differential Impedance | 8-8 | TP2 |
| Cable | | Data Eye Diagram | 5-3 | TP1, TP2 |

▸ **Table 2.** *Core HDMI tests.*

Most HDMI product developers want to perform pre-compliance testing; they have a clear incentive to ensure interoperability and compatibility. While it is recommended to perform as many tests as possible, certain core tests are an essential part of compliance. Table 2 summarizes some of the above core tests.

Transmitter or Source signal characteristics can be effectively characterized by measuring signals at test point TP1 to ensure that they are within standard timing, jitter and voltage margins.

The oscilloscope is of course the key platform for observing signals at these test points. The digital storage oscilloscopes (DSO) and digital phosphor oscilloscopes (DPO) in the Tektronix TDS family can be paired with the TDSHT3 application software package for HDMI work. TDSHT3 provides accurate automated Source measurements for HDMI compliance, including those summarized in Table 2. For more information about this subject, refer to the Tektronix application note titled Physical Layer Compliance Testing for HDMI Using TDSHT3 HDMI Compliance Test Software (available at wwww.tektronix.com).

This balance of this technical brief will concentrate on the equipment and procedures for compliance and characterization measurements on HDMI Sink devices and cables.

## HDMI Sink Tests

### Jitter Tolerance

One of the most critical characteristics of a Sink device is its tolerance to jitter in the incoming signal. The HDMI standard defines the limit as 0.3 x $T_{BIT}$; the term $T_{BIT}$ is HDMI syntax for “unit interval.” The test approach is straightforward: specified amounts of jitter are injected in steps into the transmitted TMDS signal. Each step increases the jitter amount from low to high until the sink device fails to recover the signal. The amount of jitter at which this failure occurs is compared against the published limits for compliance.

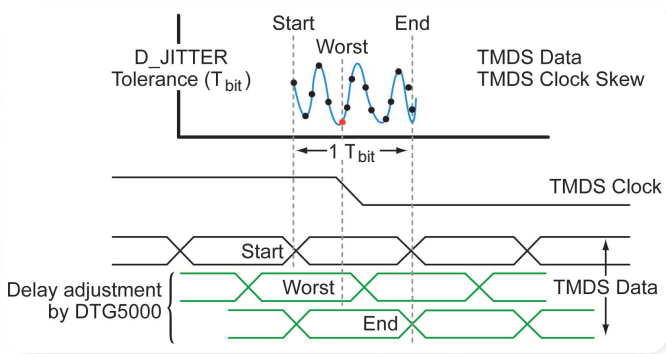
The jitter tolerance testing is performed in the following broad steps:

1. **Determining Worst-case Clock-Data skew:** The skew in data is varied until the worst point is determined. This test is performed over several iterations as illustrated in Figure 3. The signal generator providing the TMDS is then set to produce this worst-case level of skew.
2. **Measuring Jitter Margins:** several measurements involve injecting a specified amount of jitter to the clock signal path. Three measurements are performed over two test cases. Again, these Data and Clock components are injected only into the system clock path. The measurements and test cases are as follows:
   - Data Jitter amplitude ($D_{jw}$)
     - Data Jitter Frequency at 500 KHz and Clock Jitter Frequency at 10 MHz
   - Data Jitter Frequency at 1 MHz and Clock Jitter Frequency at 7 MHz.
   - Worst Data Jitter Amplitude
     - Data Jitter Frequency at 500 KHz and Clock Jitter Frequency at 10 MHz
     - Data Jitter Frequency at 1 MHz and Clock Jitter Frequency at 7 MHz.
   - Worst Clock Jitter Amplitude
     - Data Jitter Frequency at 500 KHz and Clock Jitter Frequency at 10 MHz
     - Data Jitter Frequency at 1 MHz and Clock Jitter Frequency at 7 MHz.

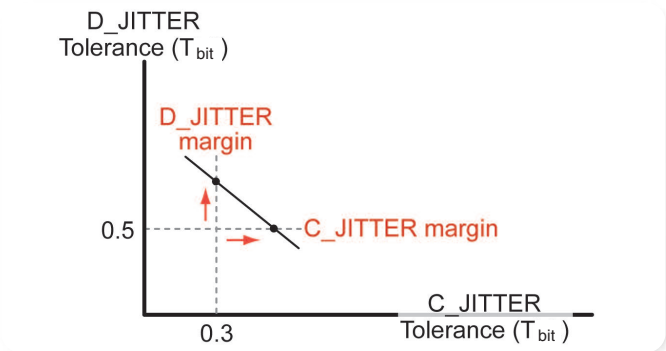
Figure 4 explains the measurement criteria for D_JITTER and C_JITTER margins. The tests need to be performed at all pixel clock rates supported by the device under test. Because of the many parameters to be adjusted and the tight margins, this test can be rather complex and time-consuming.

### Minimum Differential Sensitivity

The minimum differential sensitivity test is common to many serial standards. The test confirms that the Sink meets interoperability requirements even when it




▸ **Figure 3.** *Determining worst-case jitter tolerance.*




▸ **Figure 4.** *Measurement criteria for jitter margins.*

experiences attenuated differential voltage swings.

A TMDS signal generator with the ability to change amplitude is the proper tool for this test. The source is used to generate a Sink-supported 27 MHz video format that repeats the RGB gray ramp signal from 0 to 255 during each video period. The test starts at 170 mV $V_{DIFF}$ on all pairs, then the differential signal amplitude is reduced in steps of 20 mV until the Sink device reports an error. If the minimum $V_{DIFF}$ to which the Sink responds without error is less than 150 mV, the device passes the test. The test stops when minimum $V_{DIFF}$ reaches 70 mV. Another important element of this test is that it is performed at two different $V_{ICM}$ (common-mode voltage) settings, namely 3.0 V and 3.13 V. The DTG5000 Series offers a specific termination voltage capability that allows the generation of the TMDS signals at the appropriate levels without the requirement for external adapters such as Bias Tees.

| Sink Test Instrument Requirements | Jitter Tolerance | Min. Diff. Sensitivity | Intra-Pair Skew | Remarks |
|---|---|---|---|---|
| Digital Storage Oscilloscope | • | • | • | 16M record length |
| Differential Probes | • | • | • | > 2 ea |
| TPA-R Test Adapter Set | • | • | • | 013-A012-50 |
| TPA-P Test Adapter Set | • | • | • | 013-A013-50 |
| 12 SMA Cables | • | • | • | 174-1428-00 |
| JAE Cable Emulator | • | | | 74.25, 27MHz |
| DC Power Supply | • | • | • | +5V |
| GPIB USB Controller | • | • | • | NI GPIB-USB-B |
| GPIB Cable | • | • | • | |
| **Characterization Solution** | | | | |
| Data Timing Generator | • | • | • | DTG5274 w/ 3 DTGM30 (Note[1]) |
| Arbitrary Waveform Generator | • | | | AWG710/B (Note[1]) |
| 1) SMA-BNC adaptor | • | | | 015-1018-00 |
| Cable from DTG DC O/P Pin-to-SMA at Bias Tee (2 nos.) | • | | | 012-1506-00 + 015-0671-00 + 015-1018-00 (Note[1]) |
| SMA(m) - SMA(f) Cables (2) | • | | | (Note[1]) |
| Mini-Circuits Bias Tee (2 nos.) | • | | | ZFBT-4R2GW (Note[1]) |
| **Compliance Solution** | | | | |
| Data Timing Generator | • | • | • | DTG5274 w/ 3 DTGM30/ 1 DTGM32 |
| Function Generator up to 10MHz | • | | | 2 channel AFG3022, 3102 or 3252 |
| 2) SMA-BNC adaptor | • | | | 015-1018-00 |
| 2) SMA Cables | • | | | 174-1428-00 |

▶ **Table 3.** *Equipment for sink jitter tolerance tests.*

### Intra-Pair Skew

The Sink device also must tolerate a certain amount of intra-pair skew, that is, timing skew (misalignment) within respective differential TMDS pairs. The CTS standard defines a limit of 0.4 x $T_{BIT}$ for intra-pair skew tolerance.

The test starts by setting the clock and data pairs to zero skew and then increasing the intra-pair skew in steps of 0.1 x $T_{BIT}$ until the Sink device displays an error. The maximum skew setting that still provides error-free Sink operation is defined as the intra-pair skew; this result is compared against the published limit. If the skew tolerance is greater than 0.4 x $T_{BIT}$, the device is considered compliant with the standard. The DTG5000 Series uses its unique differential timing offset capability in conjunction with 2 channels of a differential DTGM30 module to fulfill this specific test requirement.

[1]There are two recommended solutions for the Jitter Tolerance test; one for characterization and one for compliance. Using the AWG710B as the jitter generator allows for jitter profiles beyond compliance standards, which is appropriate for characteriziation work. Using the DTGM32 as the jitter generator will enable testing up to the compliance specifications.

### Hardware Requirements: Test Equipment and Peripherals For Sink Tests

Table 3 summarizes the measurement equipment and accessories (probes, cables, etc.) required for the sink tests just described. The list includes many products recommended in the current version of the HDMI compliance test specifications. Note that the requirements for characterization and compliance testing differ somewhat, necessitating a selection of tools contingent on the task at hand[1].

In addition to the items in Table 3, instruments such as digital multimeters, protocol analyzers and LCR meters are required for certain HDMI compliance tests beyond the scope of this document.

The high bandwidths, differential signaling, and complex stimulus requirements of the HDMI architecture place rigorous demands on the instrumentation used in compliance and characterization testing. The following headings summarize some essential points to consider when choosing test equipment for HDMI test applications.

### Digital Storage Oscilloscope/Digital Phosphor Oscilloscope

HDMI jitter tolerance tests require a minimum record length of 16 megapoints (16M) in the oscilloscope. In addition, the instrument must offer a means for recovering the embedded clock (the HDMI specification prescribes software-based clock recovery) for eye diagram measurements. The Tektronix TDS family of digital storage oscilloscopes (DSO) and digital phosphor oscilloscopes (DPO) can be equipped with integrated TDSHT3 application software for automated HDMI clock recovery, eye diagram measurements, and more. The TDS7404B, with its four input channels, 4 GHz bandwidth, and 20 megasample-per-second sample rate, is a good match for HDMI measurements.

### Data Timing Generator

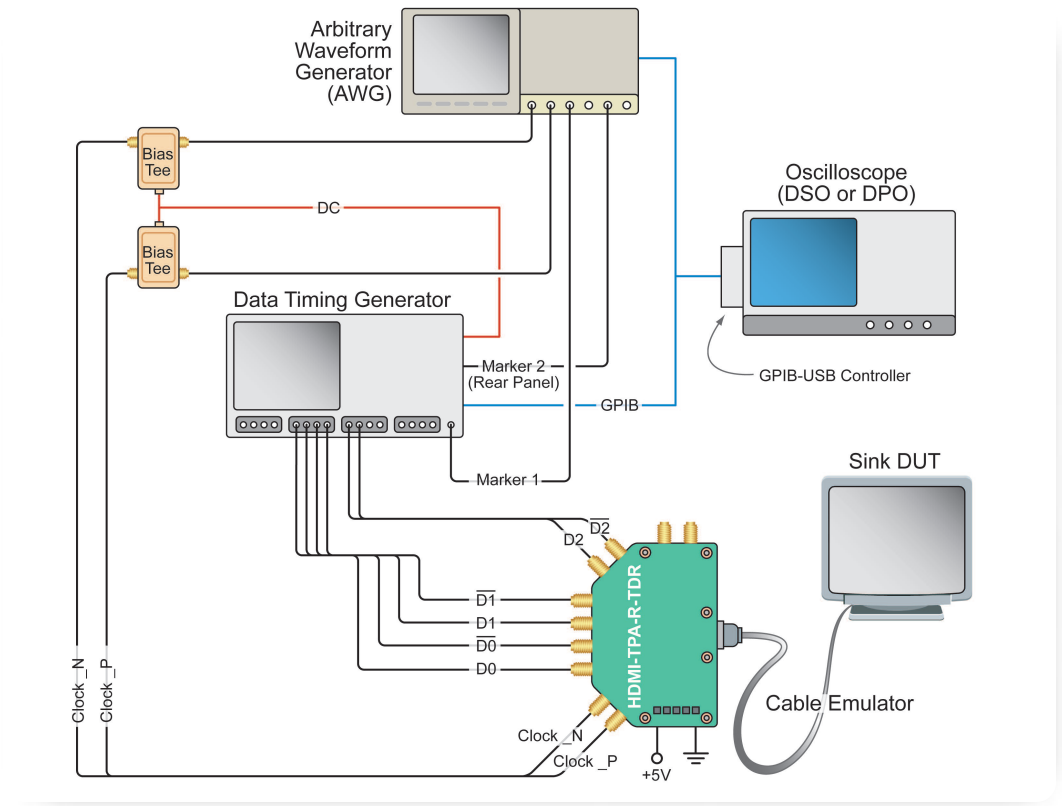
The stimulus source (generator) that provides the TMDS signal plays a pivotal role in HDMI Sink tests. The key challenge for a TMDS signal generator is to provide the needed range of highly accurate signals, and to provide precise control of the signal parameters. For example, differential sensitivity tests require an amplitude resolution of 20 mV. Intra-pair skew tests require precise delay settings with sub-picosecond resolution.

Historically, TMDS data signals have been generated by aggregations of custom devices designed for narrow output ranges and/or test conditions.

The Tektronix DTG5000 Series Data Timing Generator offers a complete stimulus solution for HDMI sink testing. The DTG5000 Series combines the power of a data generator with the capabilities of a pulse generator to provide a wide range and variety of accurate test signals on multiple output channels simultaneously. The user operates a set of simple graphic controls to set the signal parameters and variables.

Every DTG5000 Series instrument is configured from a mainframe and plug-in output modules to provide the desired number and type of signals. Channels may be single-ended or differential, depending on the test requirement. Output terminals of the plug-in channel modules are SMA connectors that can easily be converted to HDMI connectors using optional TPA test adapter accessories.

The DTG5274 Data Timing Generator with its maximum sample rate of 2.7 Gb/s or the DTG5334 with its sample rate of 3.35 Gb/s maximum rate are the mainframes of choice for HDMI applications. Both can support the maximum resolution of a UXGA device with the required data rate of 1.62 Gb/s; both offer controllable voltage levels that support all TMDS, timing, and jitter parameters.




▸ **Figure 5.** *Sink jitter tolerance test setup using an AWG as the jitter source.*

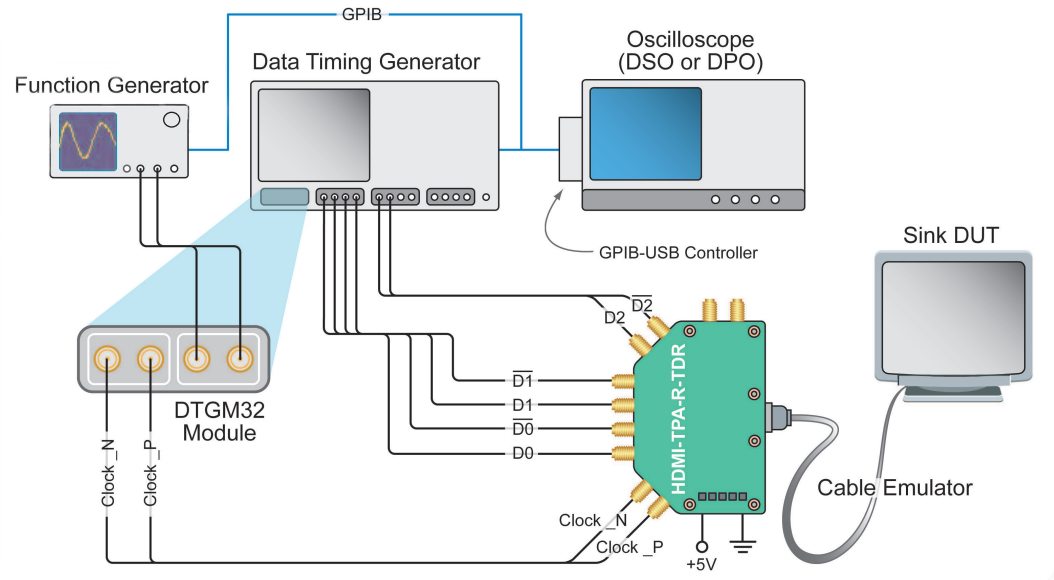
Jitter tolerance tests require a variable amount of jitter to be imposed on signals being sent to the device under test. The DTG5000 Series instruments are fully compatible with either of two recommended jitter solutions. One solution pairs the DTG5000 Series with an arbitrary waveform generator for either compliance or characterization work; the other, lower-cost solution involves a jitter generator module plugged into the DTG5000 Series mainframe and driven by an external function generator. Both approaches provide the necessary modulated jitter profiles for the generated clock signal as follows:

– **Arbitrary Waveform Generator (AWG) Method:** This solution taps the full power of the DSO and its TDSHT3 application software, the DTG5000 Series instrument, and the AWG.

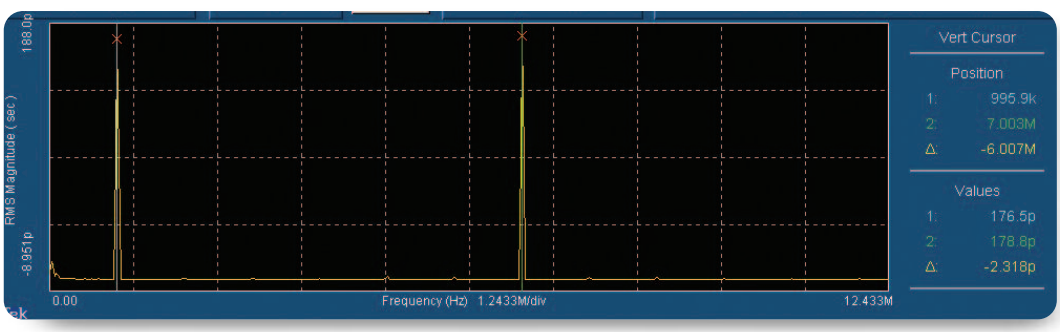
The TDSHT3 software generates the specific jitter modulation waveform and sends it to the AWG710B, which in turn acts as the clock source for the jitter tolerance test. The jitter is steadily increased by the software until the device fails. The data lines are then verified by the oscilloscope for compliance.

The AWG has two digital “Marker” outputs that can be used for synchronization, among other purposes. In HDMI sink testing, one marker connects to the DTG5000 Series external clock input while the second marker connects to the DTG5000 Series trigger input, both providing synchronization. Data signals for the device under test are sourced by the DTG5000 Series. Bias Tees are required to bring the AWG710B out put's clock signals up to the required TMDS levels. Conveniently, these Bias Tees can be powered by the built-in DC output on the DTG5000 Series. The AWG method is able to stress the device beyond the compliance specification levels, making it suitable for characterization work. Figure 5 illustrates the layout of a test configuration using the AWG method.


▶ **Figure 6.** *DTGM32 Jitter Generation Module.*




▶ **Figure 7.** *Sink jitter tolerance test setup using a function generator to the jitter modulation source for the DTGM32 module.*



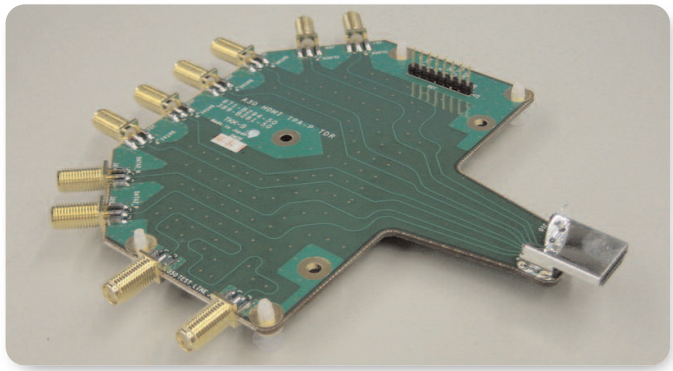

▶ **Figure 8.** *Spectral display of jitter at 1 MHz and 7 MHz.*

– DTGM32 and Function Generator Method: This approach is ideal for quick verification and cost-effective pre-compliance testing. The method uses a DTGM32 module (Figure 6) plugged into the DTG5000 Series mainframe, in conjunction with a 2 channel function generator to add the required jitter content. Figure 7 depicts this scheme. The DTGM32 module allows jitter components to be added to its output. The jitter amplitude is controlled by the input amplitude of the jitter source, in this case a Tektronix AFG3102. An input level of 1 volt produces up to 2 ns peak-to-peak jitter. Figure 8 illustrates a jitter spectrum produced using this method with 1 MHz and 7 MHz added.

### Test Adapters

The approach using the DTGM32 and the AFG allows for thorough compliance and pre compliance testing with a much simpler setup than the AWG method. This method was designed for pre/compliance testing only since the maximum available jitter just meets specification requirement. If testing is required above the specification (as in characterization), then the AWG method would be the recommended solution.

Reliable connections are key to maintaining precision and signal integrity for all HDMI tests. There are two types of test adapter sets available. For most of the Sink tests devices, the plug-type adapters (TPA-P) set and receptacle-type adapters (TPA-R) set are well suited for making the primary connection to the Device-under-test (DUT). Figure 9 shows a TPA-P plug-type test adapter.



▸ **Figure 9.** *TPA-P-TDR (013-A013-50) adapter.*

*DTG5000 Series Files Used in HDMI Compliance Test by TDSHT3*

| Test | | Pix Clock | 861B ID | Filename | Type | Image | Description |
|---|---|---|---|---|---|---|---|
| Sink 8-5 | Minimum Diff. Sensitivity | 25.2 MHz | 480 p@60 Hz | 640x480 p 60 Hz.dtg | | | |
| | | 27.027 MHz | 480 p@60 Hz | 720x480 p 60 Hz.dtg | US | | |
| | | 27.0 MHz | 576 p@50 Hz | 720x576 p 50 Hz.dtg | EU | | Normal |
| | | 74.25 MHz | 1080 i@60 Hz | 1920x1080 i 60 Hz.dtg | US | | |
| | | 74.25 MHz | 720 p@50 Hz | 1280x720 p 50 Hz.dtg | EU | | |
| | | 148.5 MHz | 1080 p@60 Hz | 1920x1080 p 60 Hz.dtg | | | |
| Sink 8-6 | Intra-Pair Skew | 25.2 MHz | 480 p@60 Hz | 640x480 p 60 Hz IP.dtg | | | |
| | | 27.027 MHz | 480 p@60 Hz | 720x480 p 60 Hz IP.dtg | US | | |
| | | 27.0 MHz | 576 p@50 Hz | 720x576 p 50 Hz IP.dtg | EU | | Diff. Timing Offset |
| | | 74.25 MHz | 1080 i@60 Hz | 1920x1080 i 60 Hz IP.dtg | US | | |
| | | 74.25 MHz | 720 p@50 Hz | 1280x720 p 50 Hz IP.dtg | EU | | |
| | | 148.5 MHz | 1080 p@60 Hz | 1920x1080 p 60 Hz IP.dtg | | Gray RGB | |
| Sink 8-7 | Jitter Tolerance | 25.2 MHz | 480 p@60 Hz | 640x480 p 60 Hz.dtg | | | |
| | | 27.027 MHz | 480 p@60 Hz | 720x480 p 60 Hz.dtg | US | | |
| | | 27.0 MHz | 576 p@50 Hz | 720x576 p 50 Hz.dtg | EU | | |
| | | 74.25 MHz | 1080 i@60 Hz | 1920x1080 i 60 Hz.dtg | US | | Normal |
| | | 74.25 MHz | 720 p@50 Hz | 1280x720 p 50 Hz.dtg | EU | | |
| | | 148.5 MHz | 1080 p@60 Hz | 1920x1080 p 60 Hz.dtg | | | |
| Cable 5-3 | Cable Data Eye Diagram | 27.027 MHz | 480 p@60 Hz | 720x480 p 60 Hz CT.dtg | US | | |
| | | 27.0 MHz | 576 p@50 Hz | 720x576 p 50 Hz CT.dtg | EU | | |
| | | 74.25 MHz | 1080 i@60 Hz | 1920x1080 i 60 Hz CT.dtg | US | | VH=3.3 V VL=2.9 V |
| | | 74.25 MHz | 720 p@50 Hz | 1280x720 p 50 Hz CT.dtg | EU | | |
| | | 148.5 MHz | 1080 p@60 Hz | 1920x1080 p 60 Hz CT.dtg | | | |
| | | | Most Likely Test Condition | | | | |
| | | | Optional | | | | |
| | | | Only If The Maximum Is 27MHz | | | | |

▸ **Table 4.** *DTG5000 Series files used by TDSHT3 in HDMI compliance tests.*

### Software Tools For Sink Tests

Sink tests, like Source tests, can take a lot of time. In case of Sink tests, there is the complexity of controlling several tools to conclude a measurement, as well as the challenge of precisely setting jitter parameters. All this makes automation an implicit requirement.

The TDSHT3 application package described earlier is optimized to speed HDMI testing and compliance work. TDSHT3 makes uses the GPIB interface to remotely control various parameters. The oscilloscope connects to the DTG5000 Series using a GPIB cable and to the AWG or arbitrary function generator using a GPIB-USB-B cable or E-Net to GPIB converter (available from National Instruments).

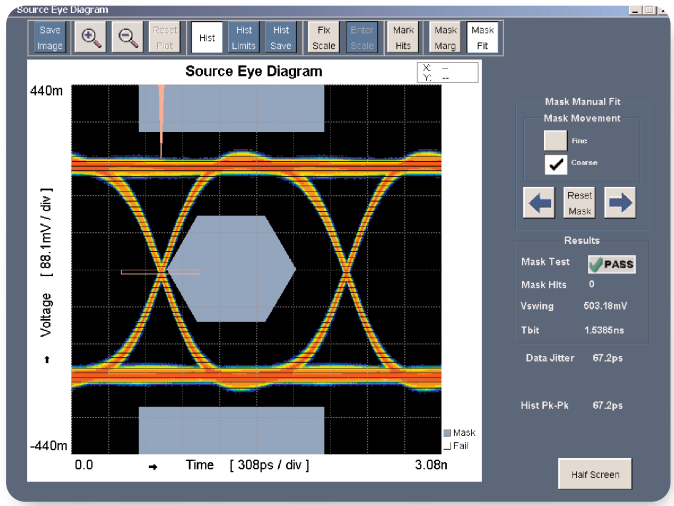
Many HDMI test setups and measurements reside within the TDSHT3 application; others can be downloaded at www.tek.com. Table 4 lists the standard setups, and the CTS tests to which they apply.

### Testing HDMI Cables

HDMI cables can be characterized in either or both of two ways: time-domain reflectometry (TDR) and eye diagram testing. The TDR technique uses a digital sampling oscilloscope to measure the impedance characteristics of a cable with great precision, but cannot verify waveform quality.

Eye diagram testing involves displaying a waveform that consists of rising and falling edges superimposed in such a way that there is an “eye” opening bounded on all sides by positive-going and negative-going transitions. Typically there is a region within this opening that must not be violated by any waveform data point. To do so would indicate insufficient signal amplitude, slow rise or fall times, jitter, or a combination of these aberrations.

The DTG5000 Series can produce standard HDMI signals for use as test data in eye diagram mask testing to reveal the true waveform performance of the cable. First, transmitter performance can be verified by inserting the test data signals ahead of the transmitter and performing the eye mask test at the transmitter output. Once this is confirmed, the test data signals can be inserted at the beginning of the cable and eye mask testing performed with the TDSHT3 package at the end. If jitter violates the eye mask, the cable has insufficient bandwidth. If the signals have insufficient level, the cable loss is too high. Figure 10 is an eye diagram captured by the TDSHT3 application software package.




▸ **Figure 10.** *HDMI eye diagram captured with TDSHT3 application software.*

## Conclusion

Compliance testing of HDMI Sink devices is no longer limited to the use of custom data sources and tedious manual methods. The DTG5000 Series high performance data generators solve the problem by providing a full complement of highly accurate data signals with precise control over the signal parameters. Testing to DVI/HDMI standards receiver products over a wide range of operating conditions can now be automated using simple, graphical controls and a set of industry-standard adapter accessories.

## References

1. HDMI Specifications Version 1.0
2. Compliance Test Specifications (CTS) Version 1.0a
3. Physical Layer Compliance Testing for HDMI Using TDSHT3 HDMI Compliance Test Software (Tektronix Application Note 61W-17974-1)

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