

# 800mA, Single-Input, Single Cell Li-Ion Battery Solar Charger with Power Path

This user's guide describes the features and operation of the bq24210EVM Evaluation Module (EVM). The EVM assists users in evaluating the bq24210 solar chager. The EVM is also called the HPA678. The manual includes the bq24210EVM bill of materials, board layout, and schematic.

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Introduction www.ti.com

#### 1 Introduction

#### 1.1 EVM Features

- Evaluation Module for bq24210
- 800mA, Single-Input, Single Cell Li-Ion Battery Solar Charger with Power Path
- · Resistor-programmable setting for charge current and input voltage dynamic power management
- · LED Indication for Status
- Test Points for Key Signals Available for Testing Purpose Easy Probe Hook-up
- Jumpers Available Easy to Change Setting

### 1.2 General Description

The bq24210 series of devices are highly integrated Li-ion linear chargers devices targeted at space-limited portable applications. The high input voltage range with input overvoltage protection supports low-cost unregulated adapters. The input voltage regulation loop with programmable input voltage regulation threshold make it suitable for charging from alternative power sources, such as solar panel or inductive charging pad. The IC has a single power output that charges the battery. A system load can be placed in parallel with the battery as long as the average system load does not keep the battery from charging fully during the 10 hour safety timer.

The battery is charged in three phases: conditioning, constant current and constant voltage. In all charge phases, an internal control loop monitors the IC junction temperature and reduces the charge current if an internal temperature threshold is exceeded.

For details, see BQ24210 data sheet (SLUSA76).

# 1.3 I/O Description

Table 1. I/O Description

Jack	Description
J1-VBUS	Positive input
J1–GND	Negative input
J2-BAT	Charger output
J2-GND	Ground
J2-TS	Temperature qualification input
J3-GND	Ground
J3-VDPM	Programs the input voltage regulation threshold
J3-CHG	Charge status indication
J3- <del>EN</del>	Chip enable control
J3- <del>PG</del>	Power present indication
J4-ISET	Programs the fast-charge current setting
J4-VTSB	TS bias reference voltage pin, regulated output
J4-GND	Ground



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#### 1.4 Control and Key Parameters Setting

Table 2. Control and Key Parameters Setting

Jack	Description	Factory Setting
JP1	Programs the fast-charge current setting. 500mA when JP1 ON; external setting when JP1 OFF	Jumper OFF (external setting)
JP2	Connect /EN and /PG together when JP2 ON to enable charger when power present	Jumper OFF (external /EN)
JP3	Programs the input voltage regulation threshold. 4.5V when JP3 ON; external setting when JP3 OFF.	Jumper OFF (external setting)
JP4	Limited power charge mode (LPCM) when JP4 ON; normal operation when JP4 OFF	Jumper OFF (normal operation)
JP5	Select external TS input or internal TS setting 1-2: External TS input 2-3: Internal TS setting	Jumper ON 1-2 (external TS)
JP6	The pull-up power source supplies for the LEDs 1-2: BAT 2-3: VBUS	Jumper ON 2-3 (VBUS)
JP7	Charger ON/OFF command 1-2: OFF 2-3: ON	Jumper ON 1-2 (charger OFF)

#### 1.5 Recommendd Operating Conditions

**Table 3. Recommendd Operating Conditions** 

	Description	Min	Тур	Max	Unit	Notes
Supply voltage, V <sub>BUS</sub>	Input voltage	4.5		7.3	V	
Battery voltage, V <sub>BAT</sub>	Voltage applied at VBAT terminal of J2	0		4.2	V	
Supply current	Maximum input current	0		0.8	Α	
Charge current, I <sub>chrg</sub>	Battery charge current	0		0.8	Α	
Operating junction temperature range, T <sub>J</sub>		0		125	°C	

An external resistor is used to program the VBUS\_DPM. The programming resistor, R<sub>VDPM</sub> is dictated by the following equation:

$$R_{VDPM} = \frac{\left(VBUS_{\_DPM} - VBUS_{\_DPM\_1}\right)}{KVBUS_{\_DPM}}$$

(1)

#### Where:

VBUS\_DPM is the desired input voltage regulation voltage threshold;

VBUS\_DPM 1 is the built-in offset threshold, nominally 3.5V

 $K_{\text{VBUS\_DPM}}$  is a gain factor found in the electrical specification. If VDPM pin is shorted to VSS, the VBUS\_DPM should be clamped to 3.65V.

If the VDPM pin is floated (open circuit), the IC operates in Battery Tracking Mode. In this case, VBUS DPM threshold is internally set as V<sub>TRK</sub>, which is BAT+100mV (BAT>3.65V) or 3.75V (BAT≤3.4V).

Connecting JP3 set 4.5V VDPM on EVM.

An external resistor is used to program the output current (50-800mA). The equation for charge current is:

$$R_{ISET} = \frac{K_{ISET}}{I_{OUT}}$$

(2)

Where, I<sub>OUT</sub> is the desired fast charge current; K<sub>ISET</sub> is a gain factor found in the spec.

The termination and pre-charge current are internally set at 10% and 20% of fast charge current respectively. The pre-charge-to-fast-charge, V<sub>low</sub> threshold is set to 2.5V.

Connecting JP1 set 500mADC for fast charge current and 100mADC for pre-charge current on EVM.



Test Summary www.ti.com

### 2 Test Summary

# 2.1 Definitions

This procedure details how to configure the HPA678 evaluation board. On the test procedure, the following naming conventions are followed.

VXXX: External voltage supply name (VBUS, VBAT)

LOADW: External load name (LOADR, LOADI)

V(TPyyy): Voltage at internal test point (TPyyy). For example, V(TP1) means the voltage at TP1.

V(Jxx): Voltage at jack terminal (Jxx).

V(XXX): Voltage at (XXX). For example, V(VDPM) means the voltage at the test point which is

marked "VDPM".

V(XXX, YYY): Voltage across point XXX and YYY.

I(JXX(YYY)): Current going out from the YYY terminal of jack XX.

Jxx(BBB): Terminal or pin BBB of jack xx

Jxx ON: Internal jumper Jxx terminals are shorted Jxx OFF: Internal jumper Jxx terminals are open

Jxx (-YY-) ON: Internal jumper Jxx adjacent terminals marked as "YY" are shorted

Measure:→A,B Check specified parameters A, B. If measured values are not within specified limits the

unit under test has failed.

Observe  $\rightarrow$ A,B Observe if A, B occur. If they do not occur, the unit under test has failed.

Assembly drawings have location for jumpers, test points and individual components

#### 2.2 Safety

- 1. Safety Glasses are to be worn.
- 2. This test must be performed by qualified personnel trained in electronics theory and understand the risks and hazards of the assembly to be tested.
- 3. ESD precautions must be followed while handling electronic assemblies while performing this test.
- 4. Precautions should be observed to avoid touching areas of the assembly that may get hot or present a shock hazard during testing.

#### 2.3 Quality

1. Test data shall be made available upon request by Texas Instruments.

## 2.4 Apparel

- 1. Electrostatic smock
- 2. Electrostatic Gloves or finger cots
- 3. Safety Glasses
- 4. Ground ESD wrist strap



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# 2.5 Equipment

#### 2.5.1 Power Supplies

Power Supply #1 (PS#1): a power supply capable of supplying 20-V at 1-A is required.

#### 2.5.2 Loads

LOAD #1 A 20V (or above), 1A (or above) electronic load that can operate at constant current and constant voltage mode.

Or: equivalent.

#### 2.5.3 Meters

Four Fluke 75 multi-meters, (equivalent or better)

Or: Two equivalent voltage meters and two equivalent current meters.

The current meters must be capable of measuring 1A+ current.

### 2.6 Equipment Setup

- 1. Set the power supply #1 (PS#1) for 6.5V ± 200mVDC, 1A ± 0.1A current limit and then turn off supply.
- 2. Connect the output of PS#1 in series with a current meter (multi-meter) to J1 (VBUS, GND).
- 3. Connect a voltage meter across J1 (VBUS, GND).
- 4. Connect Load #1 in series with a current meter to J2 (VBAT, GND). Turn off Load #1.
- 5. Connect a voltage meter across J2 (VBAT, GND).
- 6. Check all jumper shunts. JP1: OFF; JP2: OFF; JP3: OFF; JP4: OFF; JP5: connect 1-2 (External TS); JP6: connect 2-3 (VBUS); JP7: connect 1-2 (charger OFF).

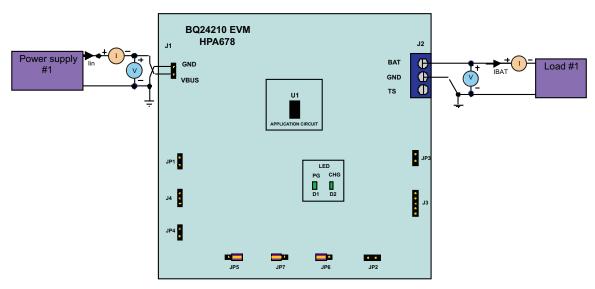


Figure 1. Original Test Setup for HPA678 (bq24210 EVM)



PCB Layout Guideline www.ti.com

#### 2.7 Procedure

#### 2.7.1 Power Supply

Make sure EQUIPMENT SETUP steps are followed.

Disconnect LOAD #1. Turn on PS#1. **Measure**  $\rightarrow$  V(J1(VBUS)) = 6.5V  $\pm$  200mV **Measure**  $\rightarrow$  V(J2(VBAT)) = 0V  $\pm$  200mV **Measure**  $\rightarrow$  V(J4(VTSB)) = 0V  $\pm$  200mV **Observe**  $\rightarrow$  D1 (PG) ON, D2 (CHG) OFF

# 2.7.2 Charger Enable and Battery Detection

Connect JP1; Connect 2-3 of JP7 (Charger ON)  $\textit{Measure} \rightarrow V(J4(VTSB)) = 2.2V \pm 300 \text{mV}$  Connect 2-3 of JP5 (Internal TS); Adjust R6 until  $V(JP4-1) = 0.7V \pm 200 \text{mV}$   $\textit{Measure} \rightarrow V(J2(VBAT)) = 4.2V 200 \text{mV}$   $\textit{Observe} \rightarrow D1$  (PG) ON, D2 (CHG) OFF

# 2.7.3 Charge Current/Voltage Regulation

Reconnect LOAD#1. Turn on. Use the constant voltage mode. Connect JP1; Set the output voltage to be 2.2V.  $\textit{Measure} \rightarrow I(J2(VBAT)) = 0.1A \pm 50mA$   $\textit{Observe} \rightarrow D1 \text{ (PG) ON, D2 (CHG) ON}$  Increase the voltage of LOAD#1 to be 3.5 V.  $\textit{Measure} \rightarrow I(J2(VBAT)) = 0.5A \pm 100mA$   $\textit{Observe} \rightarrow D1 \text{ (PG) ON, D2 (CHG) ON}$ 

#### 2.7.4 VDPM ((Input Voltage Regulation) Setting)

Disconnect J3, measure the resistance between J3-1 to GND (6.65kΩ ±10%)

#### 2.7.5 Test Complete

Turn off the power supply and remove all connections from the unit under test (UUT).

#### 3 PCB Layout Guideline

- It is critical that the exposed thermal pad on the backside of the bq24210 package be soldered to the PCB ground. Make sure there are sufficient thermal vias right underneath the IC, connecting to the ground plane on the other layers.
- 2. Decoupling capacitors for VBUS, BATC should make the interconnections to the IC as short as possible.
- 3. Take the EVM layout for design reference.



# 4 Bill of Materials, Board Layout and Schematics

# 4.1 Bill of Materials

**Table 4. Bill of Materials** 

-001	RefDes	Value	Description	SIZE	Part Number	MFR
1	C1	10 μF	Capacitor, Ceramic, 25V,X7R, 10%	1206	STD	STD
2	C2, C4	0.1 μF	Capacitor, Ceramic, 25V, X7R, 10%	0603	STD	STD
1	C3	10 μF	Capacitor, Ceramic, 6.3V, X7R, 10%	0805	STD	STD
0	C5, C6	Open	Capacitor, Ceramic, 25V, X7R, 10%	0603	STD	STD
2	D1, D2	LTST-C190CKT	Diode, LED, Red, 1.8-V, 20-mA, 20-mcd	0603	LTST-C190CKT	Liteon
1	D3	BZX84C5V1-7	Diode, Zener, 5.1V, 350-mW	SOT-23	BZX84C5V1-7	Diodes
1	J1	PEC02SAAN	Header, Male 2-pin, 100mil spacing,	0.100 inch x 2	PEC02SAAN	Sullins
1	J2	ED555/3DS	Terminal Block, 3-pin, 6-A, 3.5mm	0.41 x 0.25 inch	ED555/3DS	OST
1	J3	PEC05SAAN	Header, Male 5-pin, 100mil spacing	0.100 inch x 5	PEC05SAAN	Sullins
1	J4	PEC03SAAN	Header, Male 3-pin, 100mil spacing	0.100 inch x 3	PEC03SAAN	Sullins
4	JP1, JP2, JP3, JP4	PEC02SAAN	Header, 2-pin, 100mil spacing,	0.100 inch x 2	PEC02SAAN	Sullins
3	JP5, JP6, JP7	PEC03SAAN	Header, 3 pin, 100mil spacing,	0.100 inch x 3	PEC03SAAN	Sullins
1	R1	21.5k	Resistor, Chip, 1/16W, 1%	0603	STD	STD
2	R2, R4	1.50K	Resistor, Chip, 1/16W, 1%	0603	STD	STD
1	R3	750	Resistor, Chip, 1/16W, 1%	0603	STD	STD
1	R5	6.65k	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R6	100k	Potentiometer, 1/4 Cermet, 12-Turn, Top-Adjust	0.25 x 0.17 inch	3266W-1-104LF	Bourns
1	R7	4.75k	Resistor, Chip, 1/16-W, 1%	0603	STD	STD
0	TP1, TP2, TP3	Open	Test Point, 0.020 Hole		STD	STD
1	U1	BQ24210DCQ	IC, 800mA, Single-Input, Single Cell Li-Ion Battery Solar Charger with bi-directional Power Path	TDFN-10	BQ24210DCQ	TI
7	_		Shunt, 100-mil, Black	0.1	929950-00	ЗМ
1	_		PCB		HPA678	Any
1	_		Label	1.25 x 0.25 inch	THT-13-457-10	Brady



# 4.2 Board Layout

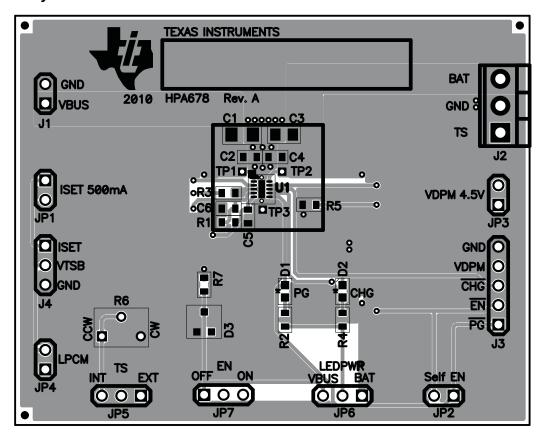


Figure 2. Top Assembly



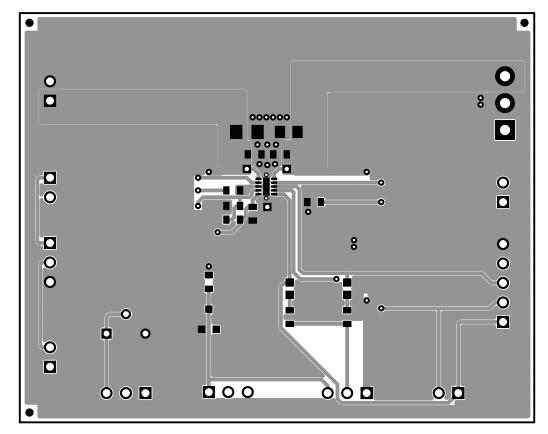


Figure 3. Top Layer



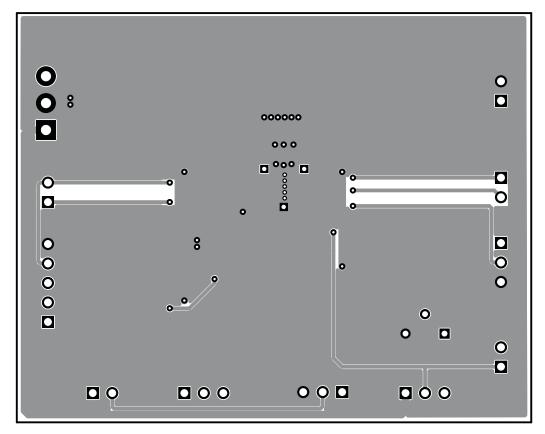


Figure 4. Bottom Layer



# 4.3 Schematics

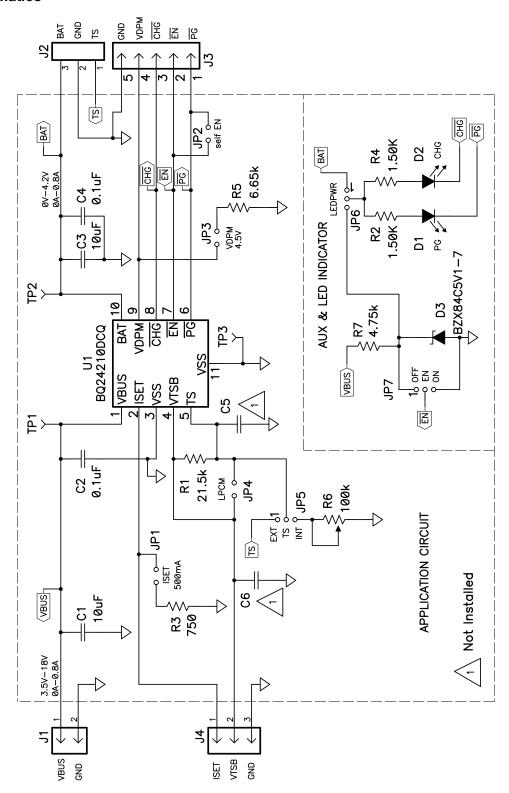


Figure 5. bq24210 EVM Schematic

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#### **EVM Warnings and Restrictions**

It is important to operate this EVM within the input voltage range of 4.5 V to 7.3 V and the output voltage range of 0 V to 4.2 V.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 60°C. The EVM is designed to operate properly with certain components above 125°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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