

10.9MHz–1175MHz Low Phase Noise Clock Evaluation Board

User's Guide

March 2007

Serial Link Products

SCAU020

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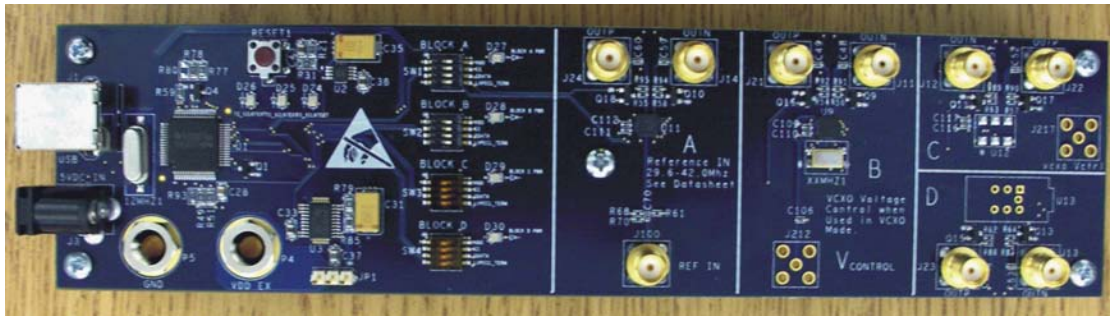


Figure 1. CDCE421EVM Evaluation Board

Features:

- Easy-to-use evaluation module generates low phase noise clocks between 10.9MHz–1175MHz
- Simple device programming via host-powered USB port
- Fast configuration through provided software GUI
- Total board power provided either through USB port or separate 3.3V and ground connections
- LVC MOS input interface or crystal input
- Standard 6-pin XO package connection available (for CDCE421-enabled XO devices)

1 General Description

The CDCE421 is a high-performance, low phase noise clock generator. It has two fully integrated, low-noise, liquid crystal (LC)-based voltage-controlled oscillators (VCOs) that operate in the 1.75GHz–2.35GHz range.

The CDCE421 has an integrated crystal oscillator circuitry that operates in conjunction with an external AT-cut crystal to produce a stable frequency reference for the PLL-based frequency synthesizer. A 3.3V LVC MOS level input can also be used instead of a crystal to provide a PLL frequency reference.

The evaluation module (EVM) is designed to quickly demonstrate the electrical performance of the device. This fully assembled and factory-tested EVM allows complete validation of all device functions for a variety of applications. Throughout this document, the acronym *EVM* and the phrases *evaluation module* and *evaluation board* are synonymous with the CDCE421EVM. [Figure 1](#) illustrates the CDCE421EVM.

For optimum performance, the board is equipped with 50Ω SMA connectors and well-controlled 50Ω impedance microstrip transmission lines.

2 Signal Path and Control Circuitry

The CDCE421 can accept a 27MHz—38.33MHz frequency input from either an LVCMOS source (up to 3.3V) or a crystal in the same frequency range.

The CDCE421EVM is divided into four blocks. The programming section and device power for each sector can be enabled or disabled through individual switches provided for each block. For example, in order to enable power and programming for Block A, the switch must be in the setting shown in Figure 2. The other blocks are enabled and disabled with the respective switches in the same manner.

The CDCE421 output frequency is always an integer multiple or integer divide of the input frequency, and is determined through selection of VCO1 or VCO2 and the appropriate prescaler and output divider, based on the [CDCE421 data sheet](#).

The loop filter selection affects the output frequency phase noise and should be considered in conjunction with the type of input used.

In LVDS mode, the device can achieve up to 500MHz output. In LVPECL mode, the device can achieve 1175MHz output. The output signaling level and LVPECL termination are selectable through the software interface.

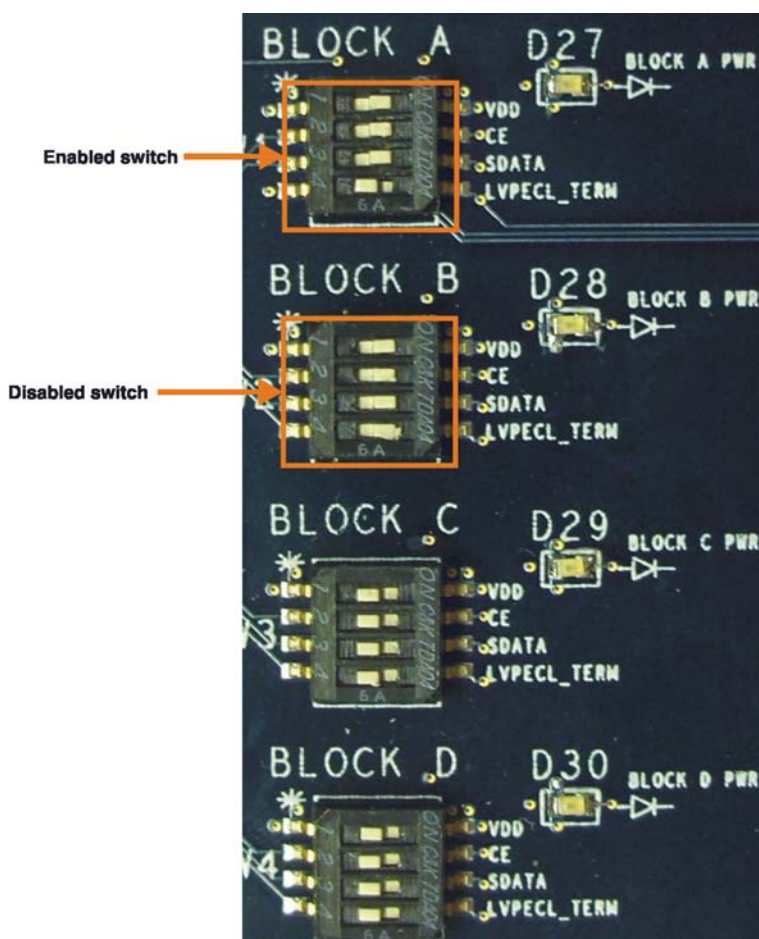


Figure 2. CDCE421EVM Programming Blocks

3 Block Description

This section discusses the four EVM blocks.

3.1 Block A

Block A includes a CDCE421 QFN device that accepts an LVCMOS reference input through the vertical SMA input connector (Ref Input) which is ac-coupled onto the board.

3.2 Block B

This block includes a CDCE421 QFN device that uses an AT-cut crystal. This block can be used as either an XO or a VCXO. For use as an XO or VCXO, the crystal should be mounted on either of the two crystal footprints on the board. A vertical SMA input connector must also be installed on the provided footprint to be used as the control voltage input for use as a VCXO.

3.3 Block C

Block C includes a CDCE41 device in its bare die form, packaged within a 5x7 oscillator. The oscillator package also includes a fixed frequency crystal with a specified load and range. Oscillators with different frequency crystals that contain a CDCE421 device can be obtained through [Pletronics](#).

3.4 Block D

The fourth block, D, includes a socket fitting the oscillator part used in Block C.

4 Software-Selectable Options

The provided EVM software is controlled through a graphical user interface (GUI). The software allows users to easily send commands to the CDCE421 through the host-powered USB interface. The EVM includes a slave USB controller that transmits the commands to the single-pin programming interface included on the CDCE421. DC power for the USB controller can be provided either from the 5V power pin in the USB cable or by using an external 5V ac adapter (plugged into the slot available on the EVM).

In addition to writing commands to the CDCE421 SRAM while the board is powered, software commands can also be stored in either the nonvolatile USB microcontroller memory or the EEPROM included within the CDCE421. This architecture allows users to start the EVM in the desired state without requiring additional programming at power-up.

Note that the CDCE421 does have a permanent EEPROM lock mode. When this mode is selected, the embedded EEPROM in the CDCE421 cannot be changed. This mode is useful when setting final configurations.

5 Installing the Software GUI and USB Driver

The CDCE421EVM software can be installed on a PC running the Microsoft Windows® 2000 operating system or higher (including Windows XP®).

To start software installation, run the *ChronosSetup.msi* file (available on the CD shipped with the EVM). [Figure 3](#) appears. Be sure to note the installation folder; the USB driver must be installed in the same after setup completes and the USB cable is connected. See [Figure 4](#).

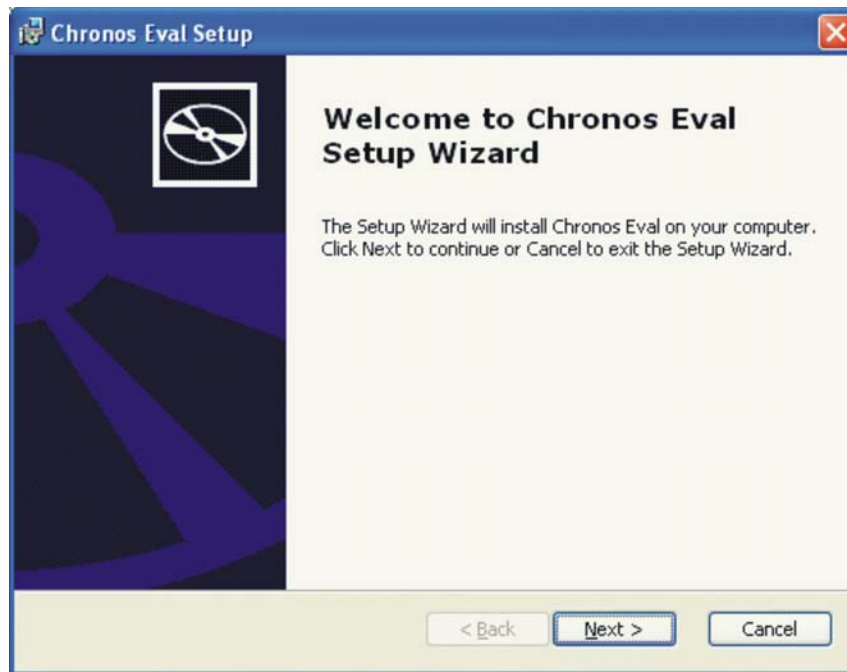
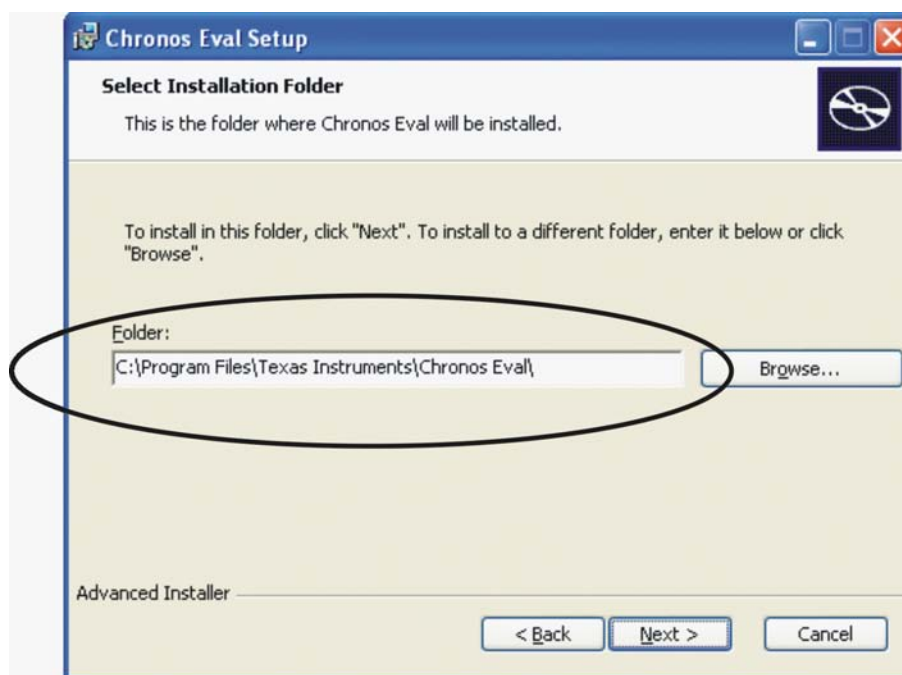


Figure 3. Software Installation Screen



Note the program file location; the USB controller driver is in the same location.

Figure 4. Installation Prompt

After the setup wizard completes, start the GUI interface from the **Start** menu (Start→Texas Instruments→Chronos Eval→TICronosGUI.exe).

Connect the USB cable to the EVM. If Microsoft Windows prompts you for an appropriate driver, do **not** use the automatic search option. Select a manual installation. When prompted for the driver location, browse to the Chronos GUI file folder that was created during installation. (If the operating system does not ask for a driver, no additional action is needed.)

Once the USB driver installation completes, the GUI software should connect properly and be ready for use. A green light in the USB communication box indicates a good USB connection; a red light indicates a faulty USB connection. If the connection is not established, attempt to re-install the drivers.

6 ChronosGUI

Figure 5 shows the Chronos GUI used to navigate the EVM software.

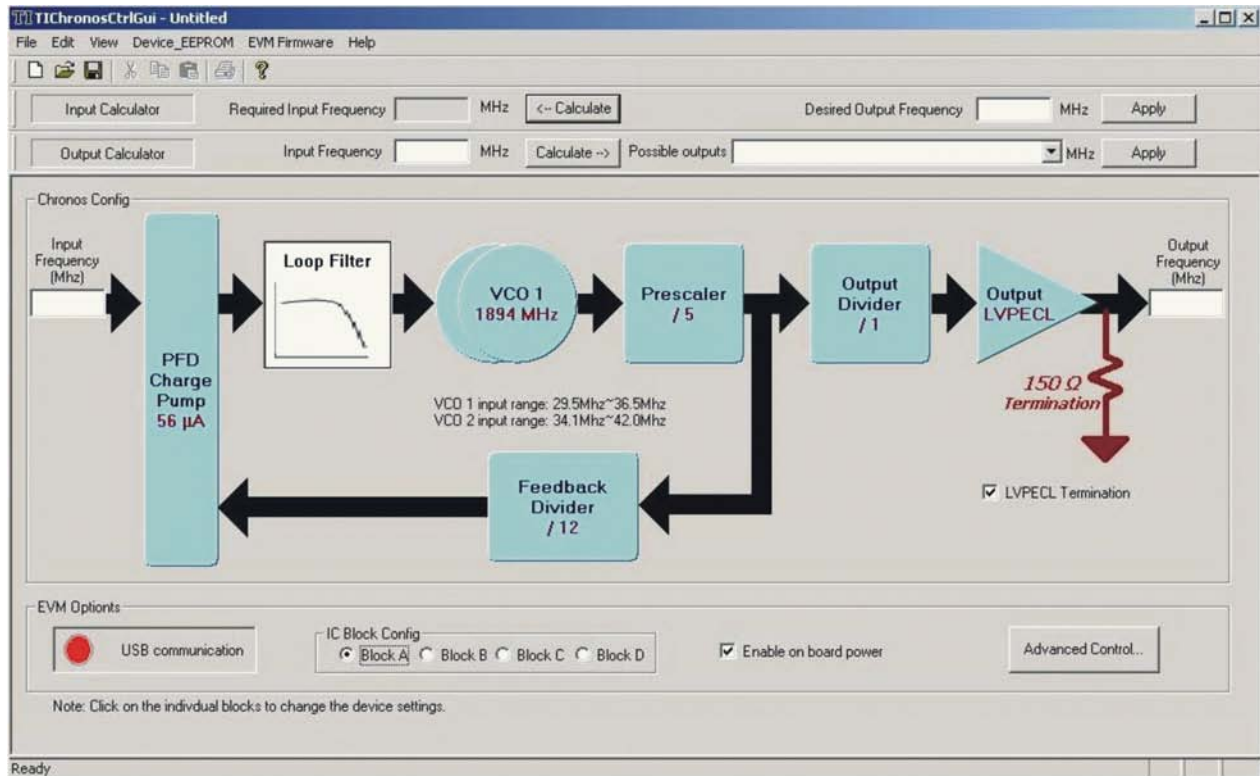


Figure 5. TI Chronos Software GUI

6.1 Using Software-Enabled Automatic PLL Selection

The software illustration Figure 5 shows the on-chip PLL structure of the CDCE421. Through this screen, the user can change the Input Frequency, PFD Charge Pump, Loop Filter, and Output Type. The other features are selected by the software; user-selectable options are described in this section.

Step 1. IC Block Configuration and Input Calculator.

Before programming the PLL, the specific EVM block that is being programmed must be selected in the *IC Block Config* section of the GUI. For any block in the EVM being used, the first row of calculations is useful when trying to investigate the input frequency to the CDCE421 needed to obtain a desired output frequency. The input frequency is obtained by pressing the **Calculate** button.

Step 2. Store Crystal Frequency.

If a crystal input is used for Block B of the EVM, the crystal frequency must be entered into the space provided; click on the **Device EEPROM** drop-down menu at the top of the software GUI. A menu item labeled *Save Block B–XTAL Freq to EEPROM* appears; this menu item must be selected. The crystal

frequency should be entered here in this format: **xx.xxx** (specified in MHz).

Step 3. Output Calculator and Apply PLL Settings.

The second row of calculations is used to obtain the PLL settings necessary to achieve a particular output frequency provided a given input frequency to CDCE421. The input must be entered in the second row as well as the location provided at the input of the PLL block diagram. After the **Calculate** button is pressed, the adjacent drop-down menu populates with several choices for the given input. The desired output can then be chosen from this list. Choosing one output sets the divider settings within the PLL. Clicking *Apply* next to the drop-down menu results in writing the PLL settings to the SRAM. If LVPECL output is desired, click **Output Type** until the LVPECL option displays. This option automatically enables onboard LVPECL termination. If LVDS output is desired, use **Output Type** to select the LVDS option.

Step 4. PLL Bandwidth Select.

If the user wants to adjust the PLL bandwidth, click the **Loop Filter** block, bringing a pop-up screen as shown in [Figure 6](#).

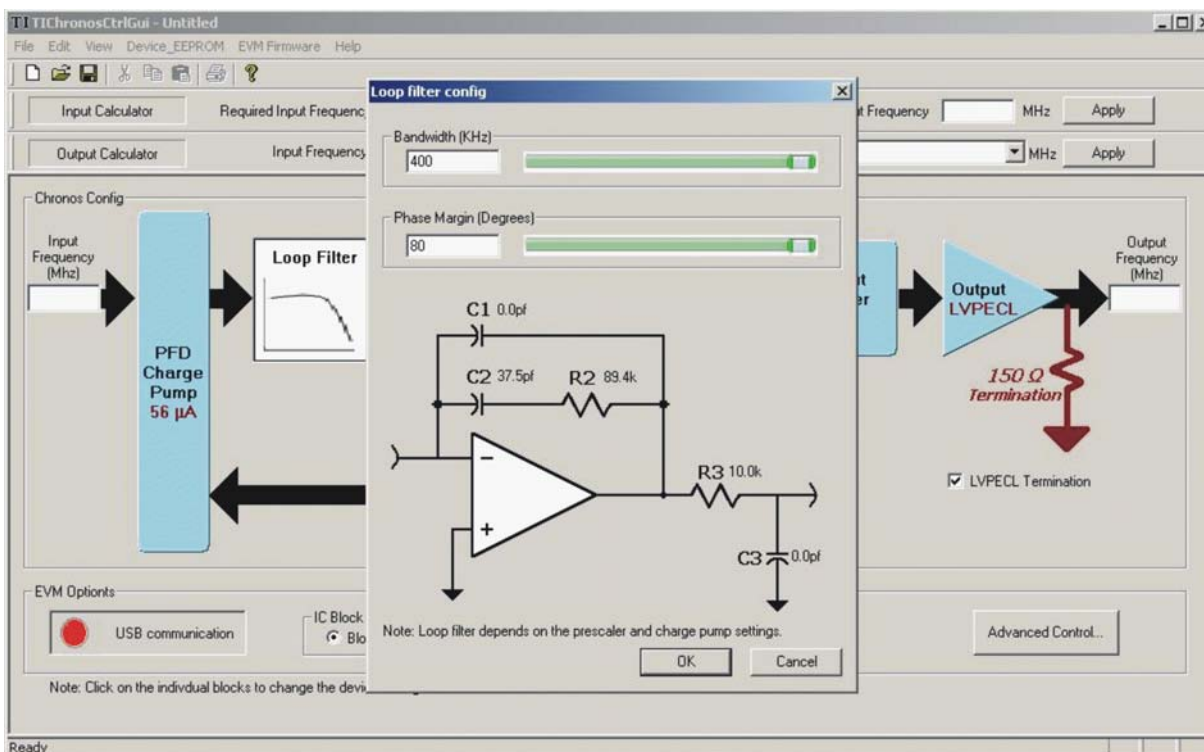


Figure 6. Chronos GUI—Loop Filter Configuration Pop-Up

For a clean reference input to the CDCE421 (for example, from an oscillator or crystal), the maximum bandwidth and phase margin setting must be used: 400kHz bandwidth and 80 degrees. The Phase Frequency Detector (PFD) charge pump current must be set to its maximum, 224µA. The PFD charge pump current can be set by clicking on the **PDF Charge Pump** block, presenting a drop-down menu with the various charge pump current settings.

For a dirty reference input to the CDCE421, the minimum bandwidth of 50kHz must be used. Additionally, to reduce the output jitter for a dirty input, the phase margin can also be reduced to near its minimum (30 degrees), depending on the integration limits of the jitter that are important for a given application. To reduce the output jitter further, the charge pump current can be reduced to its minimum (56µA), depending on the integration limits of the jitter.

Step 5. Write to CDCE421 EEPROM.

To write any particular setting to the EEPROM (locking or nonlocking), the **Device EEPROM** drop-down menu (at the top of the screen) must be selected. This menu contains the items *Write settings to EEPROM (No locking)* and *Write settings to EEPROM (Locking)*. Choose the appropriate option after setting the desired PLL configurations to write to the EEPROM in its appropriate mode.

6.2 Manual PLL Block Selection (Advanced Control)

The advanced control screen helps to set the PLL without having to manually alter the individual blocks within the PLL. If a user is familiar with PLL operation, one may activate individual control of the PLL blocks by clicking on the **Advanced Control** button, activating the window shown in [Figure 7](#).

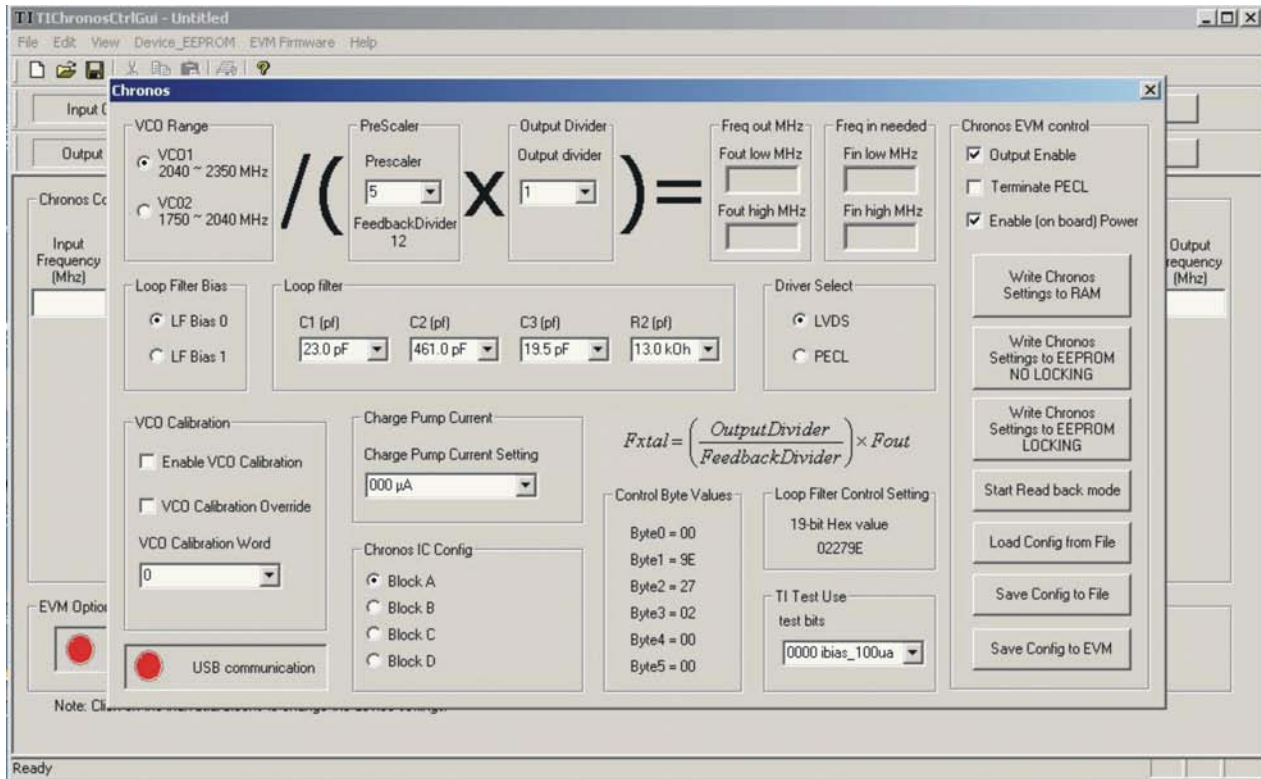


Figure 7. Chronos GUI—Manual PLL Block Selection Pop-Up

Table 1 lists the various menu items in this screen.

Table 1. Software Settings Description

Section	Function
VCO Select	Selects between VCO1 and VCO2. Only one VCO can be used during operation. See CDCE421 data sheet for VCO tuning ranges.
Prescaler	The prescaler selection is determined in conjunction with VCO and output divider selection. See the CDCE421 data sheet to determine the proper setting.
Output Divider	The output divider is determined in conjunction with the VCO and prescaler settings. See the CDCE421 data sheet to determine the proper setting.
Driver Select	Selects between LVPECL or LVDS output.
PECL Config	This option should be activated when using LVPECL output. When selected, the USB controller enables the onboard LVPECL termination.
Charge Pump Current	Selects appropriate charge pump current. See Figure 6 and Figure 7 for recommended configurations.
Loop Filter Bias Select	Bias 0 should be used at all times. Bias 1 is a test mode reserved for factory use.
Loop Filter	Selects the loop filter C and R values. See Figure 6 and Figure 7 for recommended configurations.
VCO Calibration	When <i>Enable VCO Calibration</i> is selected, the CDCE421 uses its internal calibration circuit to lock the PLL loop. <i>VCO Calibration Override</i> should not be checked. TI uses manual calibration for test modes.
TI Test Use	Setting should be kept at 0000 <i>ibias_100ua</i> . Other settings are for TI use only.
Chronos IC Config	Select <i>Use U13 programming socket</i> for rapid programming of Chronos-enabled devices. Select <i>Use U8 DIE/U9 QFN socket</i> if the EVM is using a direct-mounted die or a QFN-mounted device (typical configuration). Select <i>Use U12XTAL EVAL</i> if using the optional 6-pin XO mounting pads (for Chronos-enabled oscillators).
Chronos Control	Select <i>Enable Power</i> to run the entire board from the host USB voltage. In this mode, the EVM does not need an external 3.3V power supply. If this option is not selected, then an external 3.3V supply and ground connection must be attached. Select <i>Output Enable</i> to provide a clock output. When not selected, the output goes to a high-Z state. Push <i>Write Chronos settings to RAM</i> to download settings into the CDCE421 on-chip volatile SRAM. These settings are lost upon device power-down. Push <i>Write Chronos settings to EEPROM NO LOCKING</i> when ready to store the configuration in the CDCE421 nonvolatile EEPROM. The settings are available after device power-down. The settings can be changed at a later time. Push <i>Write Chronos settings to EEPROM LOCKING</i> only if the settings are permanent and final. After this selection, the EEPROM is locked and cannot be altered at a later time.
USB Communication	A bright red light indicates that USB is not connected or not communicating properly. A green light indicates that a proper USB connection exists.

7 Configuring the Board

The CDCE421EVM can be powered from the USB power supply or from an external source. The CDCE421EVM only needs a USB cable attached for programming purposes; however, for test measurements it is recommended to also use an external 3.3V power supply. Test measurements can also be taken with only the USB supplied power. Note that because of USB power variance, results may degrade. It is also possible to program the CDCE421 and then disconnect the USB cable with minor board configuration changes. To enable power and programming of any of the four blocks on the CDCE421EVM, the respective switch must be turned on [as explained earlier](#).

7.1 Programming and Testing Configuration (USB Cable Attached)—Default Configuration

By default, the CDCE421EVM is configured to operate with the USB cable attached and a 3.3V power supply added to AUX VDD and GND. In this configuration, the USB microcontroller is powered by the USB port 5V supply while the CDCE421 is powered by the 3.3V external supply. This setup is optimal for programming the CDCE421 device while also taking measurements. This configuration removes the power variations inherent with USB power supplies by isolating the CDCE421 from the USB supply.

7.2 Programming Configuration (USB Cable Attached)

The CDCE421EVM can also use power supplied through the USB cable as its sole power source. However, because of power-supply variance in the USB supply, this configuration is not recommended for most measurements. Users are advised to enable this setup for saving configuration settings to the CDCE421 and later powering the device from its internal memory. (This option is useful if there is not a USB port available in a lab or test area.) In this configuration, JP1 must be moved from its default position to the new position shown in [Figure 8](#). The **Enable onboard power** checkbox must be selected on the EVM software, followed by pushing the **Apply** button (see [Figure 5](#)).

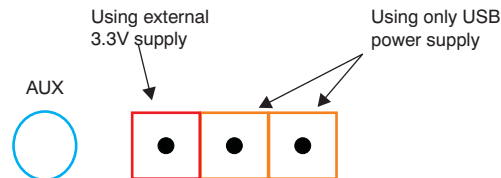


Figure 8. JP1 Setting for USB Programming Configuration

7.3 Testing Configuration from a Saved Configuration (with USB Cable Removed After Programming)

When operating the CDCE421 without the USB programming cable (useful in lab settings where a PC is not immediately available at a lab station), the CDCE421EVM must be preprogrammed in one of the two configurations discussed above, and then reconfigured for external power supply usage.

Before making these board modifications, the CDCE421 settings must be saved with one of the two USB cable attached configurations. The *Write Chronos Settings to EEPROM NO LOCKING* software button must be used to save the CDCE421 settings to its internal EEPROM. After the settings are saved, the USB cable can be removed. Once the cable has been disconnected, JP1 should be in the *Using External 3.3V Supply* position (as shown in [Figure 8](#)). The EVM is now ready for use without the USB cable connected. The CDCE421 will always start from its saved configuration state in this mode.

If the CDCE421 must be isolated from the microcontroller, the switch corresponding to the block in use should be set to **OFF** for *CE_x*, *SDATA_x*, and *LVPECL_TERM_x* where *x* represents the block name (see [Figure 9](#)). The power line switch for the respective block, however, should remain on. This sequence also allows the user to remove the USB cable without affecting performance while the CDCE421 is powered on.

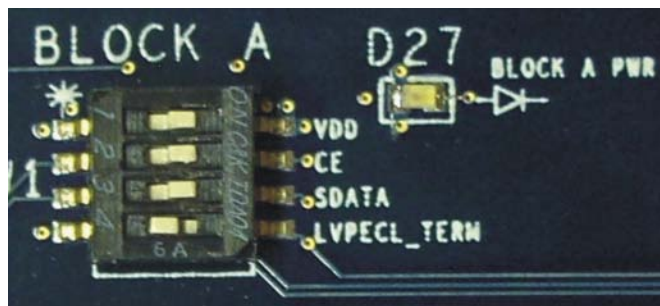


Figure 9. CDCE421EVM Block Switch Off

8 Schematics and Layout

Figure 10 through Figure 14 show the printed circuit board (PCB) schematics.

Note: Board layouts are not to scale. These figures are intended to show how the board is laid out; they are not intended to be used for manufacturing CDCE421EVM PCBs.

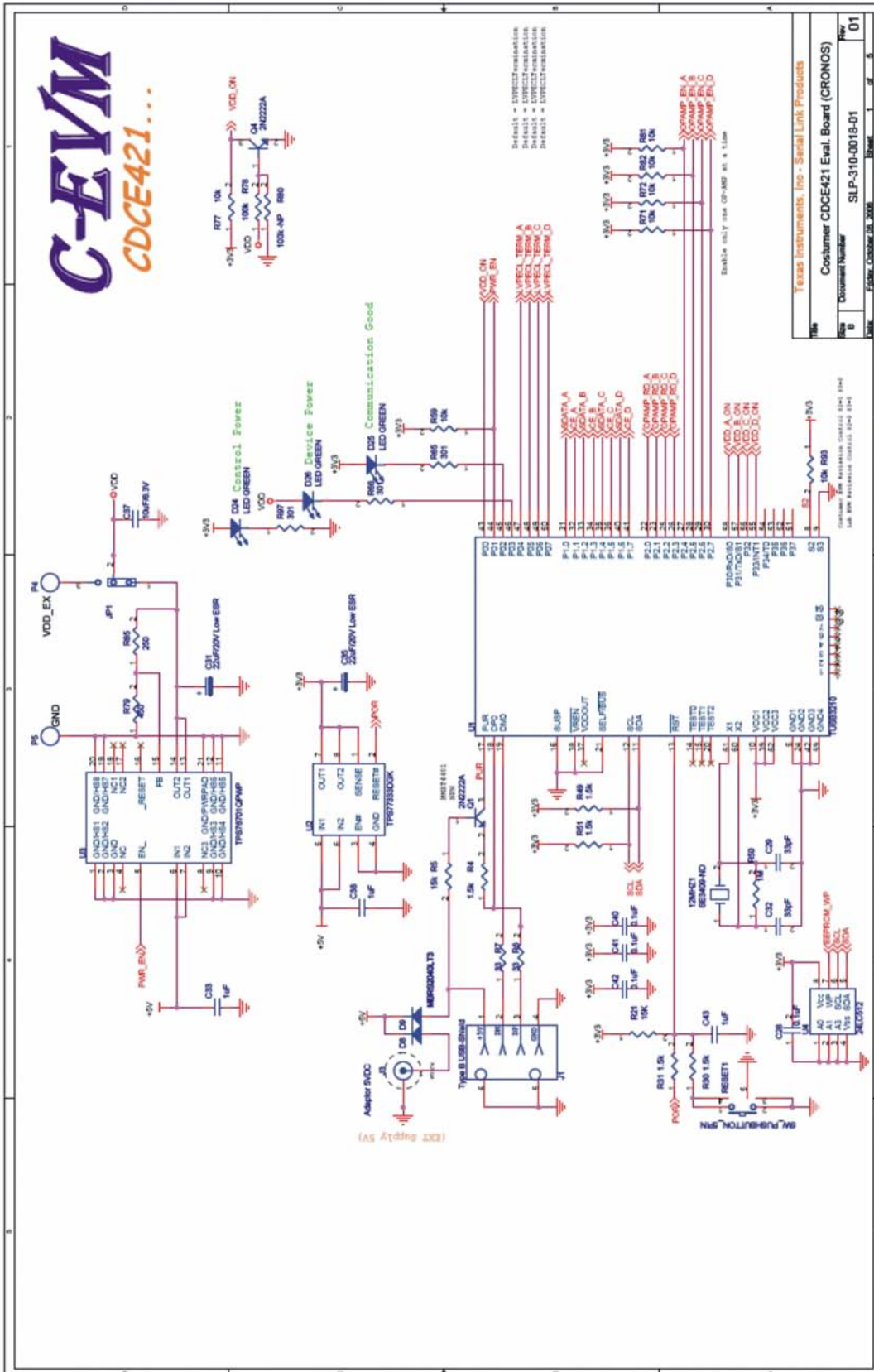


Figure 10. CDCE421EVM Board Schematic

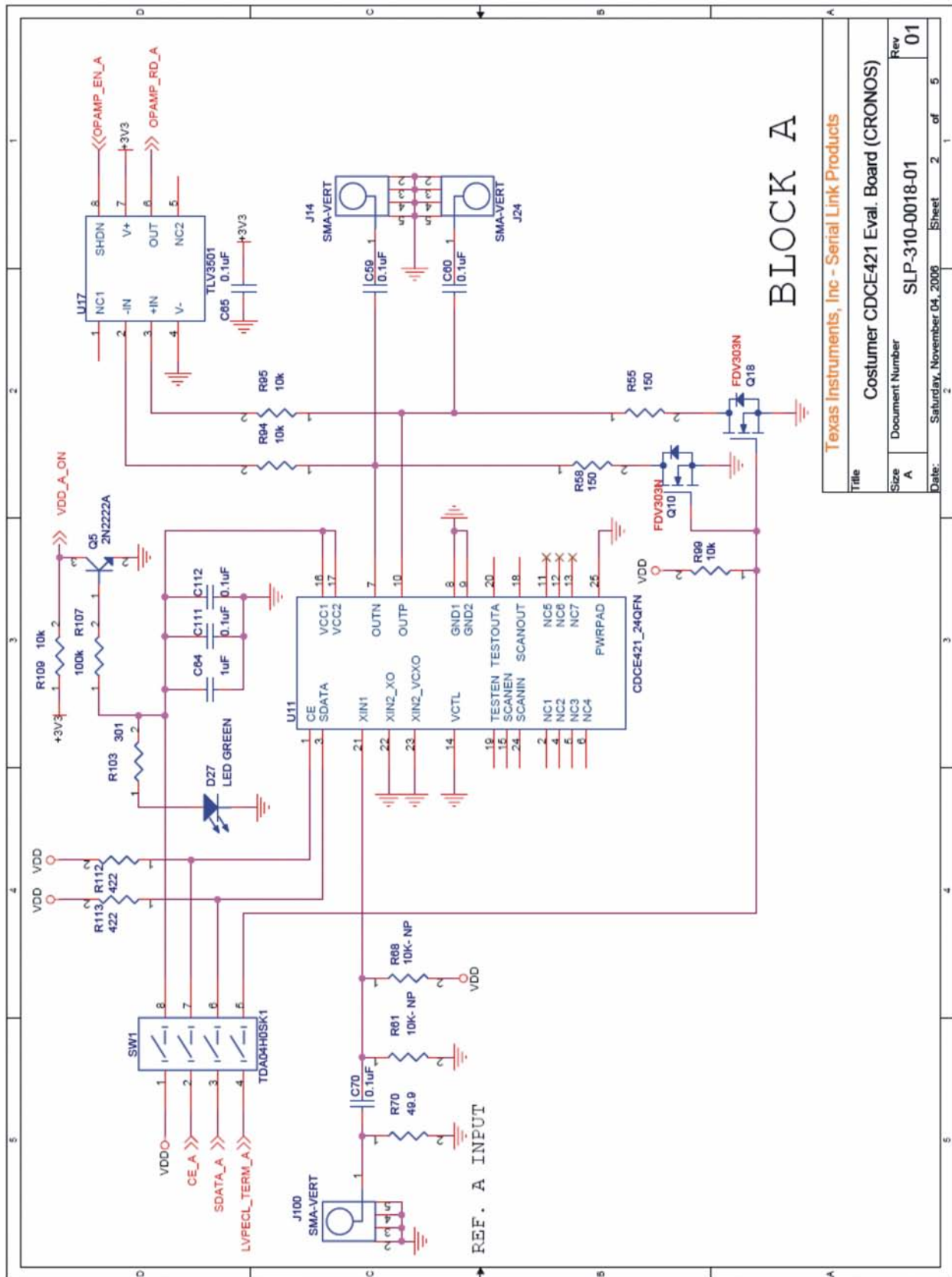
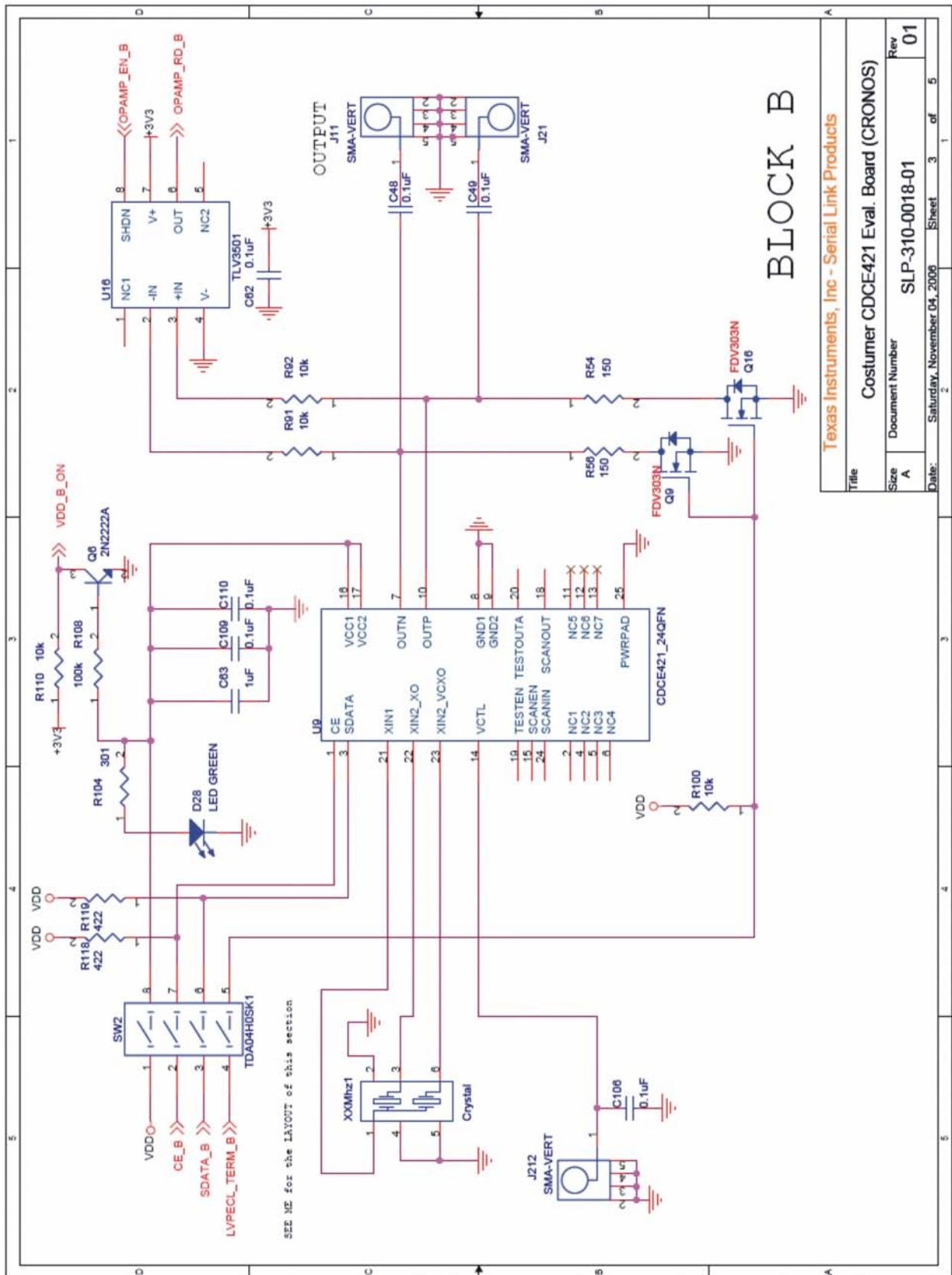


Figure 11. CDCE421EVM Board—Block A Schematic



Title		Customer CDCE421 Eval. Board (CRONOS)		
Size	A	Document Number	SLP-310-0018-01	
Rev	01	Date:	Saturday, November 04, 2006	Sheet 3 of 5

Figure 12. CDCE421EVM Board—Block B Schematic

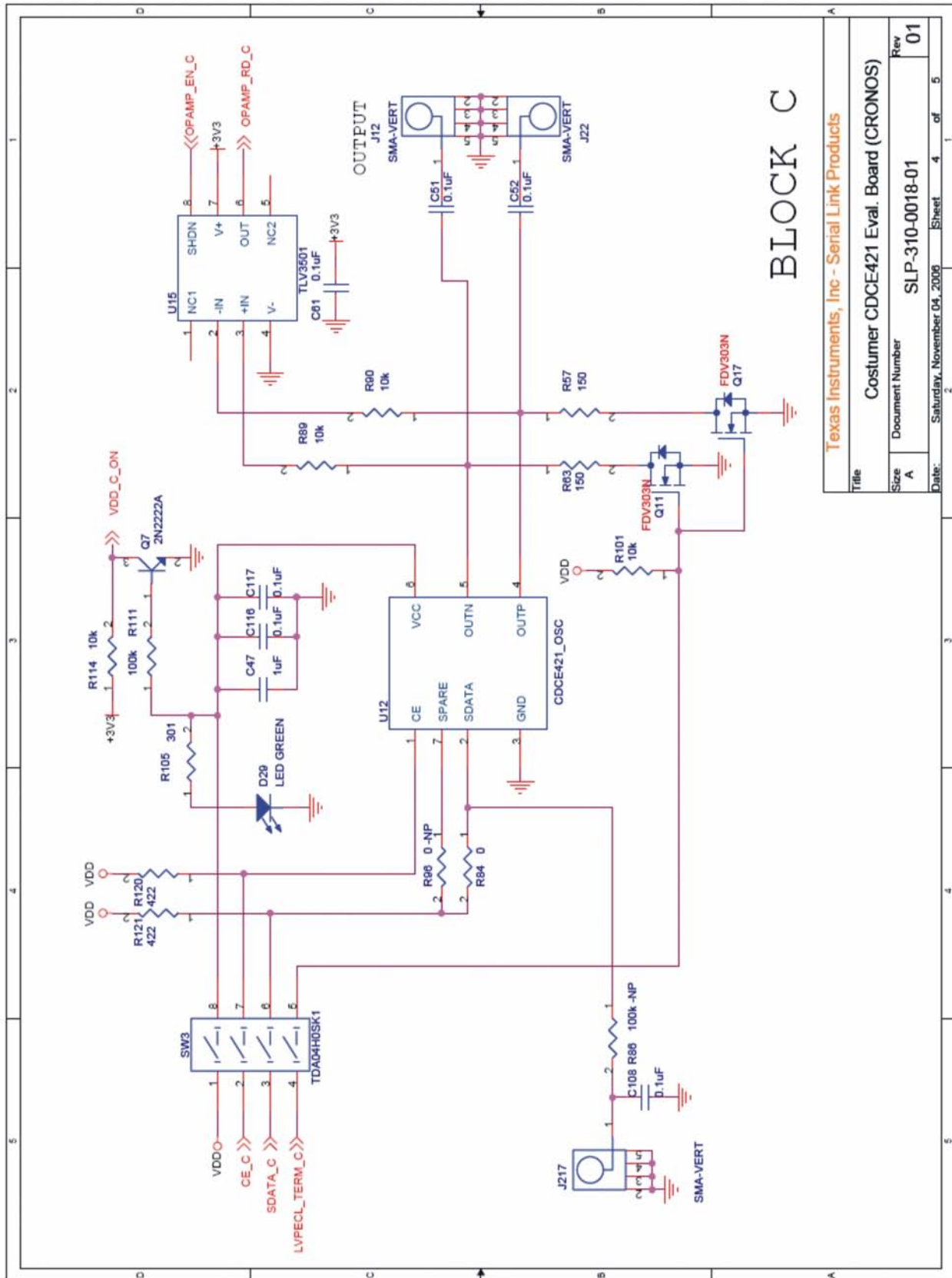
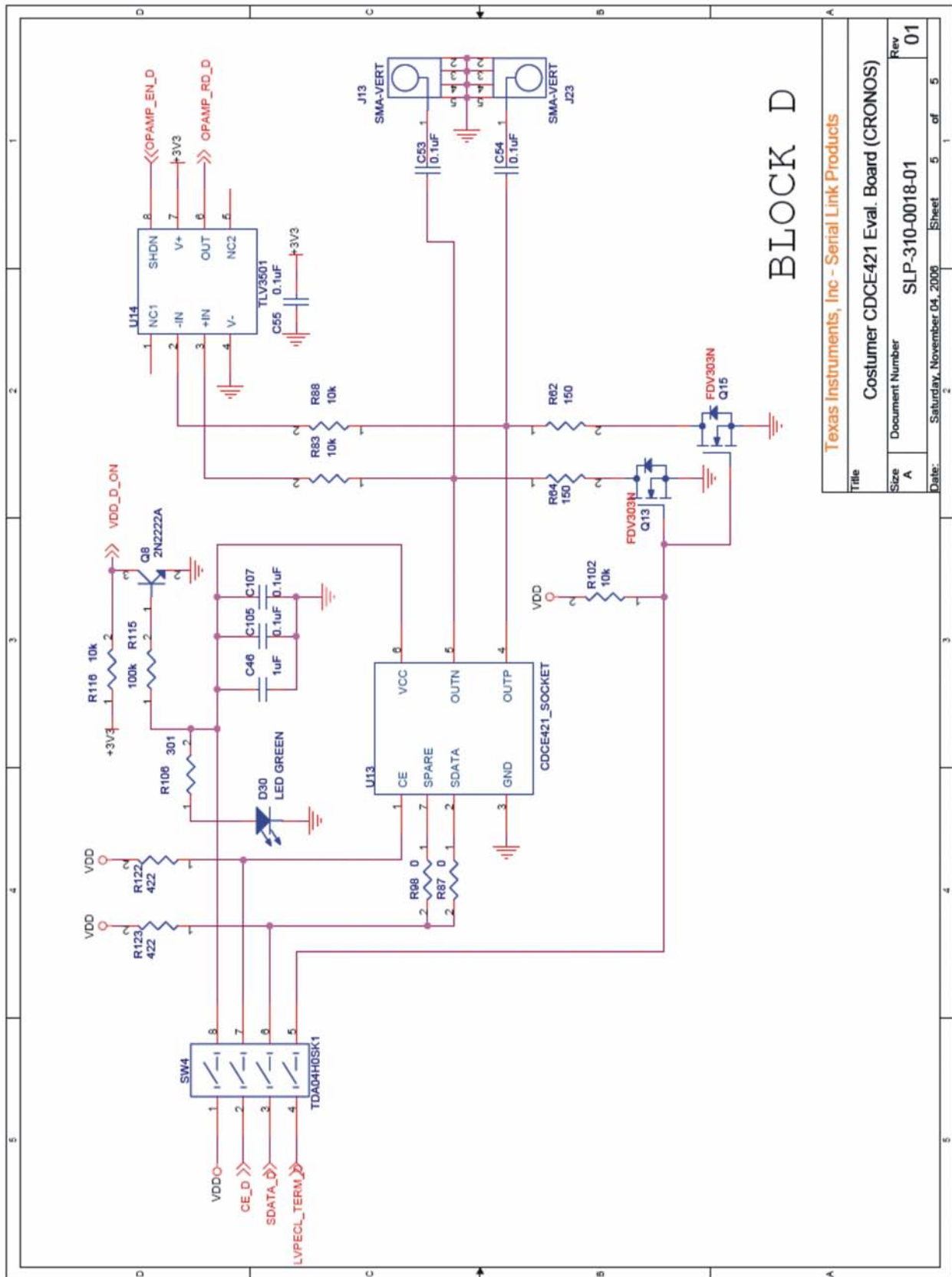


Figure 13. CDCE421EVM Board—Block C Schematic



Title		Texas Instruments, Inc - Serial Link Products		
Document Number		Customer CDCE421 Eval. Board (CRONOS)		
Size	A	Document Number	SLP-310-0018-01	Rev
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Figure 14. CDCE421EVM Board—Block D Schematic

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EVM WARNINGS AND RESTRICTIONS

It is important to operate this EVM within the input voltage range of $-0.5V$ to $4.0V$ and the output voltage range of $0V$ to $3.6V$.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

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During normal operation, some circuit components may have case temperatures greater than $+120^{\circ}C$. The EVM is designed to operate properly with certain components above $+85^{\circ}C$ as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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