TOSHIBA

NTDPJTV05

TECHNICAL TRAINING MANUAL
N5SS CHASSIS

PROJECTION TELEVISION

TW40F80

Only the different points from the training manual “N5SS chassis” with its file No. 026-9506 are described on this manual.
For other parts common with “N5SS chassis”, please refer to the original manual with its file No. 026-9506.

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SECTION I: OUTLINE

1. FEATURE

The TW40F80 is a first PJ-TV with a wide screen aspect ratio of 16:9 we introduce to North U.S.A. markets.

As the basic chassis N5SS chassis is used.

The future of the model TW40F80 is the use of the N5SS chassis. This chassis introduces a new bus system, developed by the PHILIPS company, called the I^2C (or IIC) bus. IIC stands for Inter-Integrated Circuit control. This bus coordinates the transfer of data and control between ICs inside the TV. It is a bi-directional serial bus consisting of two lines, named SDA (Serial DATA), and SCL (Serial CLOCK). This bus control system is made possible through the use of digital-to analog converters built into the ICs, allowing them to be addressed and controlled by strings of digital instructions.

The TW40F80 is a first wide TV with a double window system we introduce to North U.S.A. markets.

The size of the main and sub screens separated in left and right on the screen is the same as each other. So it is possible to enjoy two programs or video and TV program at the same time.

The sub screen is equipped wit 9 screen search function and this is very convenient convenient to search a program you desire.

Note:

Only the different points from the manual "N5SS Chassis" with its file No. 026-9506 are described on this manual. For other parts common with "N5SS Chassis", please refer to the original manual with its File No. 026-9506.

2. MERITS OF BUS SYSTEM

2-1. Improved Serviceability

Most of the adjustments previously made by resetting variable resistors and/or capacitors can be made on the new chassis by operating the remote control and seeing the results on the TV screen. This allows seeing adjustments to be made without removing servicing speed and efficiency.

2-2. Reduction of Parts Count

The use of digital-to-analog converters built into the ICs, allowing them to be controlled by software, has eliminated or reduced the requirement for many discrete parts such as potentiometers and trimmers, etc.

2-3. Quality Control

This central control of the adjustment data makes it easier to understand, analyze, and review the data, thus improving quality of the product.

3. SPECIFICATIONS

C-Chassis

	Model	TW56F80	TW40F80	TP61F90	TP61F80	TP55F80	TP55F81	TP50F90	TP50F60	TP50F61	TP50F50	TP50F51
GENERAL	CRT	7"	7"	7"	7"	7"	7"	7"	7"	7"	7"	7"
	CRT Source	Hitach	Hitach	Hitach	Hitach	Hitach	Hitach	Hitach	Hitach	Hitach	Hitach	Hitach
	Remote H/U	Intell	Univ	Intell	Univ	Univ	Univ	Intell	Univ	Univ.	A-Univ	A-Univ
	RMT Keys	52 key	36 key	52 key	36 key	36 key	36 key	52 key	36 key	36 key	42 key	42 key
	PIP	2-TN	2-TN	2-TN	2-TN	2-TN	2-TN	2-TN	2-TN	2-TN	1-TN	1-TN
SOUND	Dolby Surr	ProLgc		ProLgc	Dy-Sur	Dy-Sur	Dy-Sur	ProLgc				
	Surround	Dsp4Ch	●	Dsp4Ch	Dsp4Ch	Dsp4Ch	Dsp4Ch	Dsp4Ch	●	●	●	●
	SAP	●	●	●	●	●	●	●	●	●	●	●
	Cyclone											
	SBS	●	●	●	●	●	●	●	●	●	●	●
	Audio (W)	28W	28W	28W	28W	28W	28W	28W	28W	28W	28W	28W
	Center	+20W		20W				20W				
	Rear	+20W		20W	20W	20W	20W	20W				
PICTURE	Comb-Filter	3D-Y/C	3D-Y/C	3D-Y/C	3D-Y/C	DIG	DIG	DIG	DIG	DIG	DIG	DIG
	DQF			●	●	●	●					
	Scan-Modul	●	●	●	●	●	●	●	●	●	●	●
	VCC	●	●									
	Black-Expan	●	●	●	●	●	●	●	●	●	●	●
	Color-D.E	●	●	●	●	●	●	●	●	●	●	●
	Pic-Prefer	●	●	●	●	●	●	●	●	●	●	●
	Color-Temp	●	●	●	●	●	●	●	●	●	●	●
	Flesh-Tone	●	●	●	●	●	●	●	●	●	●	●
	Nois-Reduce	●	●	●	●	●	●	●	●	●	●	●
	Hori-Resolu	800	800	800	800	800	800	800	800	800	800	800
OTHERS	Fav-Channel	●	●	●	●	●	●	●	●	●	●	●
	Ch-Label	●	●	●	●	●	●	●	●	●	●	●
	3-Language	●	●	●	●	●	●	●	●	●	●	●
	Clock	●	●	●	●	●	●	●	●	●	●	●
	Ch-Lock/Off	●	●	●	●	●	●	●	●	●	●	●
	C.Caption	●	●	●	●	●	●	●	●	●	●	●
	EDS		●		●	●	●		●	●	●	●
	New-OSD	●	●	●	●	●	●	●	●	●		
	S/Sight	●		●				●				
TERMINAL	S-Video In	1+1	1+1	1+1	1+1	1+1	1+1	1+1	1+1	1+1	1	1
	AV-In/Out	1+2/1	1+2/1	1+2/1	1+2/1	1+2/1	1+2/1	1+2/1	1+2/1	1+2/1	2/1	2/1
	Front-Term	●	●	●	●	●	●	●	●	●		
	A(Var)-Out	●	●	●	●	●	●	●	●	●	●	●
	2RF-Term	●	●	●	●	●	●	●	●	●		
	SPK-Term	●	●	●	●	●	●	●	●	●	●	●
	PIP Audio			●				●				
	C-Ch-Input				●	●	●					
	E/Jack											
	S/S-Jack	●		●				●				
ACCE	IR-B & 75W	●		●				●				
	Adapter	●	●	●	●	●	●	●	●	●	●	●
	Rod-Antenna											
	SPK-Box	●		●	●			●				
	EZ RMT	●		●				●				
*	Cabinet	TW56D90	40W30E	TP61E90	TP61E80	TP55E80	TP55E81	New	New	New	New	New

4. FRONT VIEW

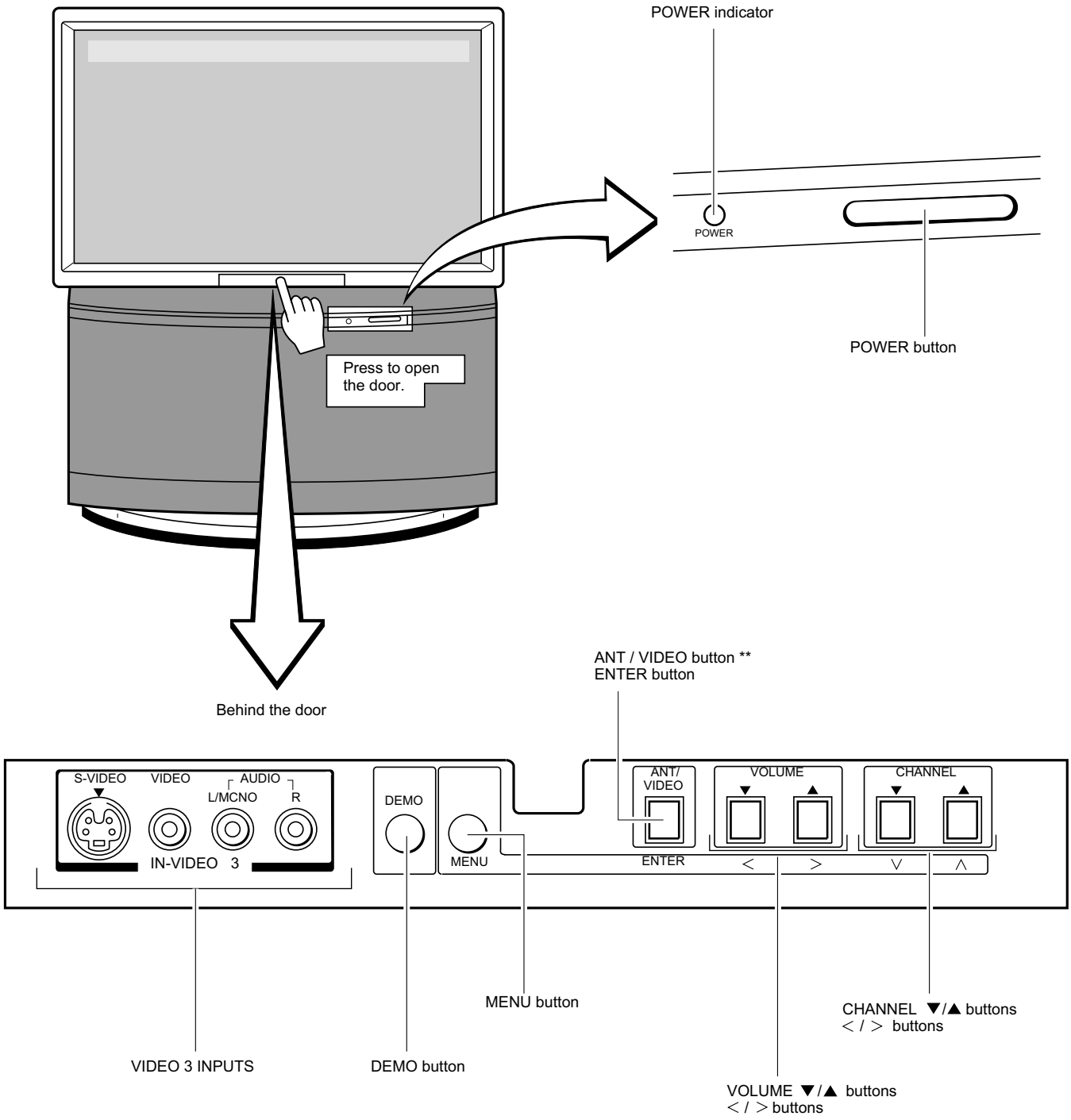


Fig. 1-1

Note: [No] Owner's manual page.

5. REAR VIEW

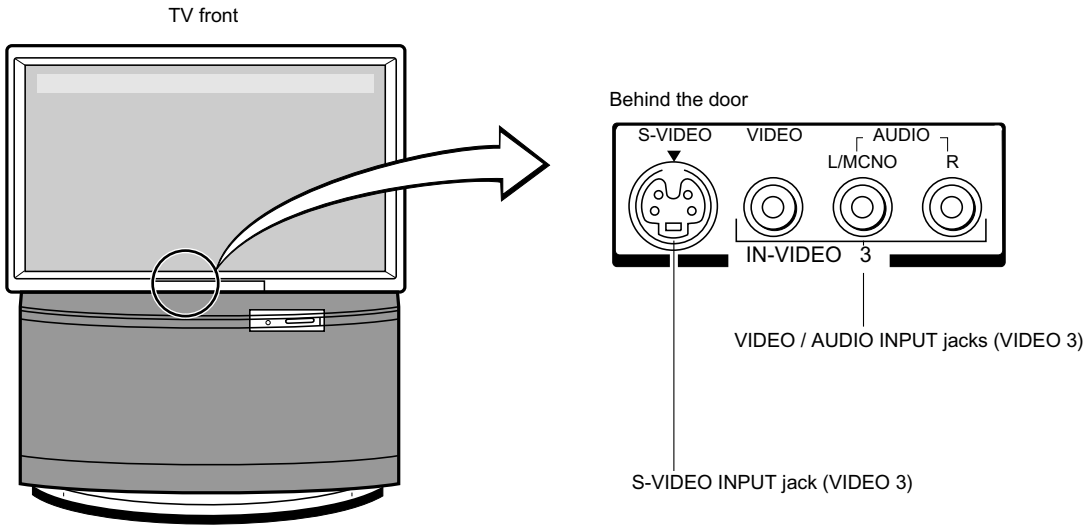


Fig. 1-2

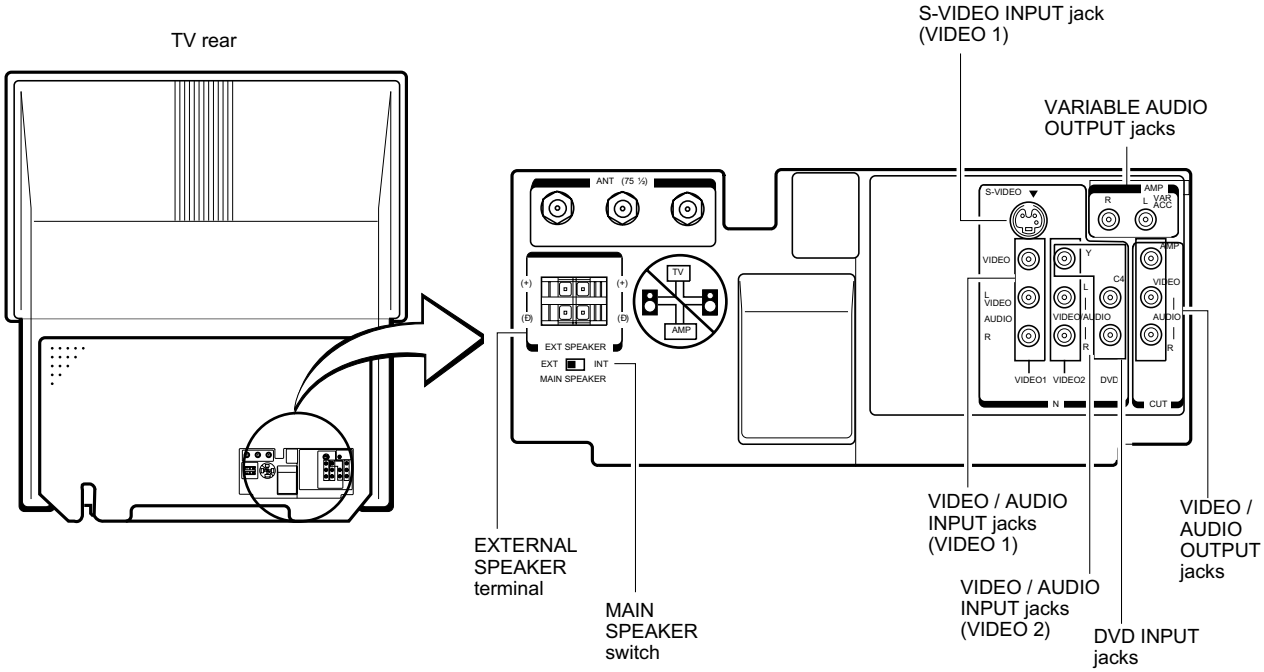


Fig. 1-3

6. REMOTE CONTROL VIEW

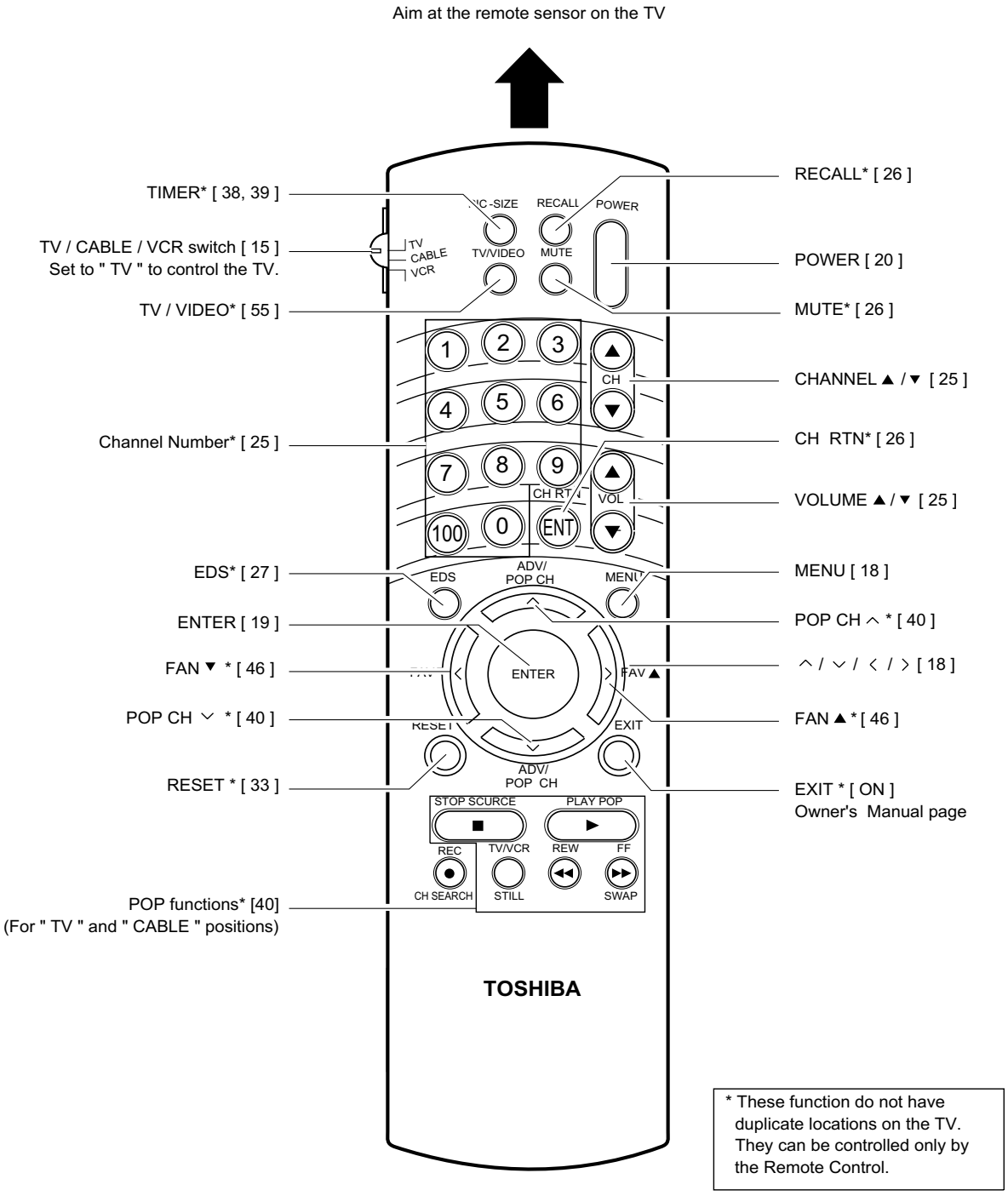


Fig. 1-4

Note: [No] Owner's Manual page.

7. CHASSIS LAYOUT

MODE1	TUNER	DOLBY	DSP	F.SUR	COHB	FDS	N.OSD	STARSIGHT
TW40F80	2			●	3DYC	●	●	
TW56F80	2	PRO	4CH		3DYC		●	●

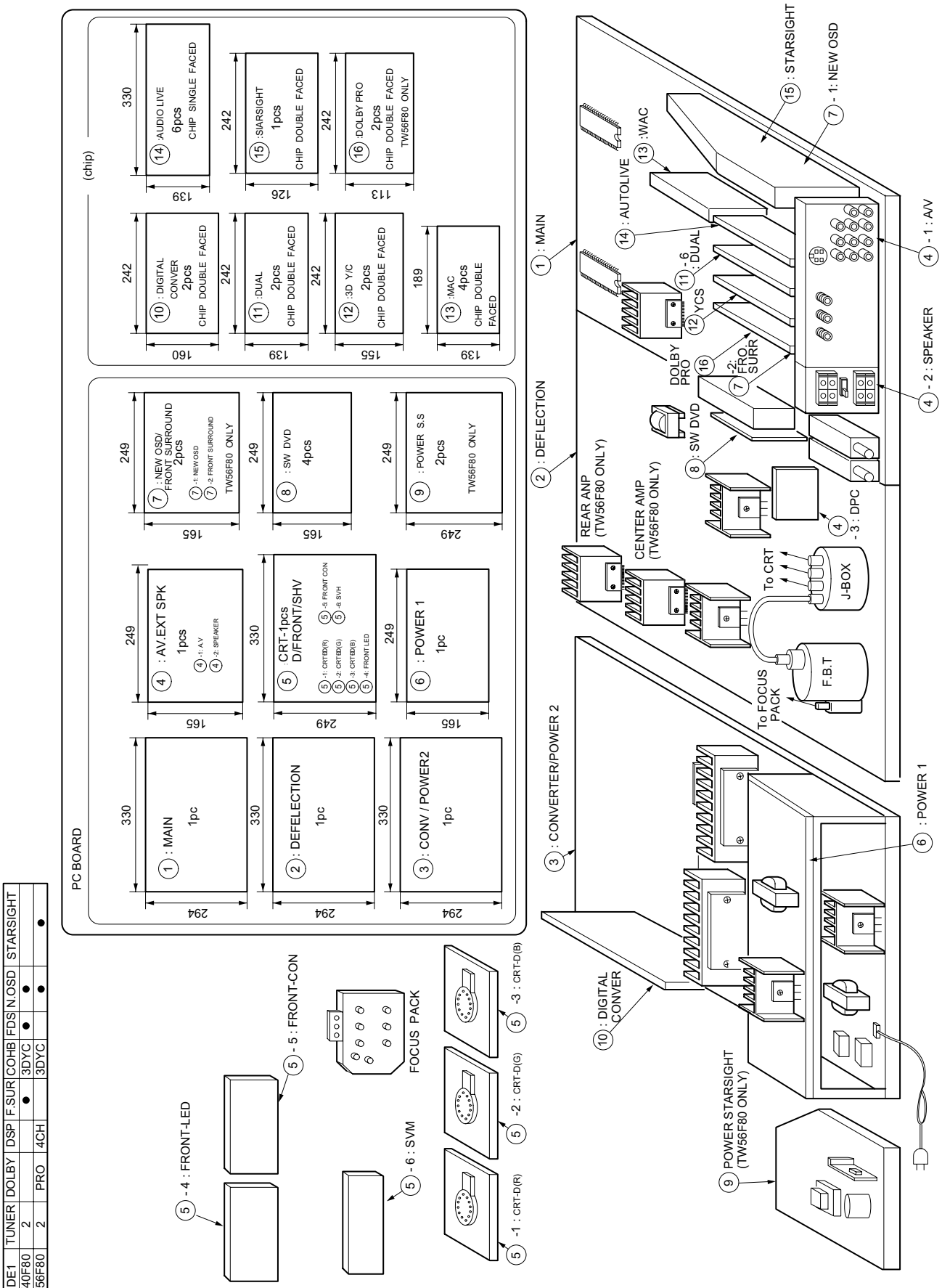


Fig. 1-5

8. CONSTRUCTION OF CHASSIS

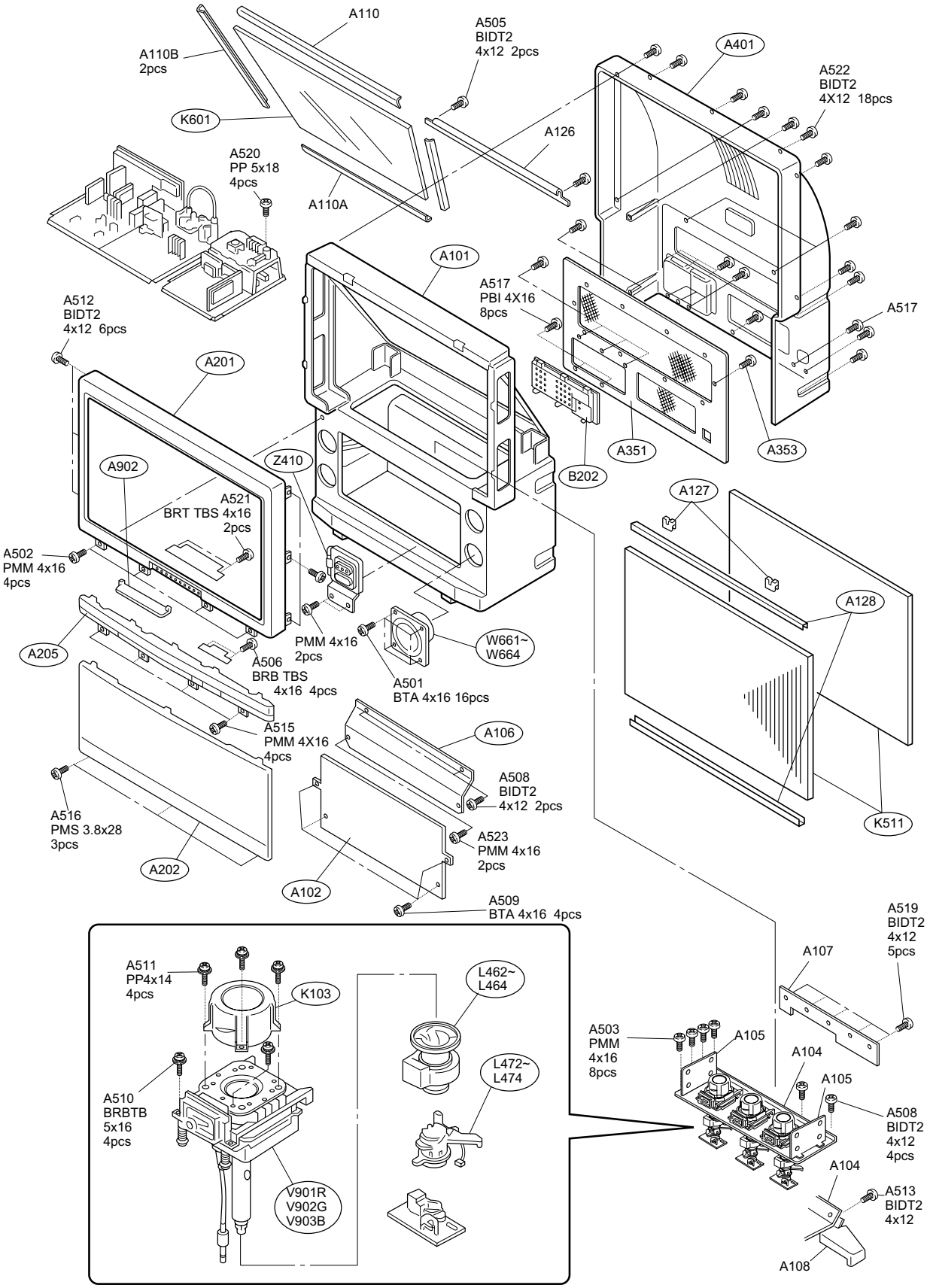


Fig. 1-6

SECTION II: TUNER, IF/MTS/S. PRO MODULE

1. CIRCUIT BLOCK

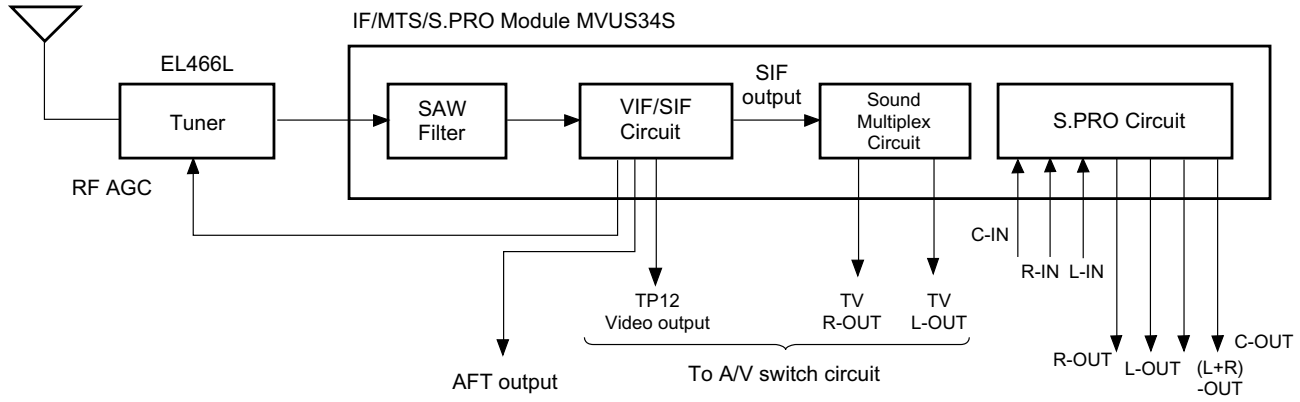


Fig. 2-1 Block diagram

1-1. Outline

(1) RF signals sent from an antenna are converted into intermediate frequency band signals (video: 45.75 MHz, audio: 41.25 MHz) in the tuner. (Hereafter, these signals are called IF signals.)

(2) The IF signals are band-limited in passing through a SAW filter.

(3) The IF signals band-limited are detected in the VIF circuit to develop video and AFT signals.

(4) The band-limited IF signals are detected in the SIF circuit and the detected output is demodulated by the audio multiplexer, developing R and L channel outputs. These outputs are fed to the A/V switch circuit.

(5) A sound processor (S.PRO.) is provided.

1-2. Major Features

(1) The VIF/SIF circuit is fabricated into a small module by using chip parts considerably.

(2) As the tuner, EL466L that which contains an integrated PLL circuit is employed.

(3) Wide band double SAW filter F1802R used.

(4) FS (frequency synthesizer) type channel selection system employed.

(5) VIF/SIF circuit uses PLL sync detection system to improve performances shown below:

- Telop buzz in video over modulation
- DP, DG characteristics (video high-fidelity reproduction)
- Cross color characteristic (coloring phenomenon at color less high frequency signal objects)

(6) HIC SBX1637A-22 is used in the audio multiplexer circuit to minimize the size with increased performance.

(7) As a sound control processor, TA1217N is used. I^2C-bus data control the DAC inside the IC to perform switching of the audio multiplexer modes.

1-3. Audio Multiplex Demodulation Circuit

The sound multiplex composite signal FM-detected in the PIF circuit enters pin 12 of HIC (hybrid IC) in passing through the separation adjustment VR RV2 and amplified. After the amplification, the signal is split into two: one enters a de-emphasis circuit, and only the main signal with the L-R signal and a SAP signal removed enters the matrix circuit. At the same time, the other passes through various filters and trap circuits, and the L-R signal is AM-demodulated, and the SAP is FM-demodulated.

Then, both are fed to the matrix circuit. At the same time, each of the stereo pilot signal fH and the SAP pilot signal 5fH is also demodulated to obtain an identification voltage. With the identification voltage thus obtained and the user control voltage are used to control the matrix.

The audio signals obtained by demodulating the sound multiplex signal develop at pin 10 and 11 of HIC and develop the terminals of 12 and 14 of the module.

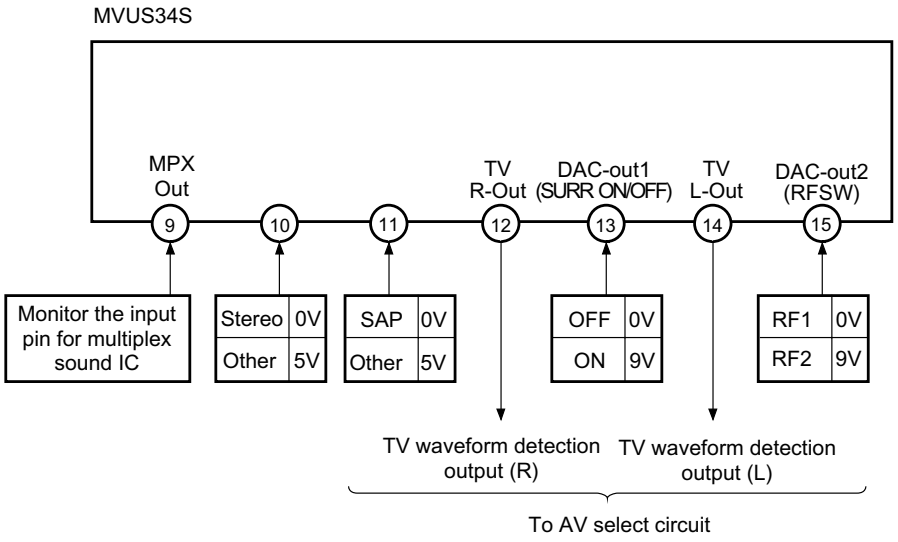


Fig. 2-2 Block diagram of MVUS34S

Table 2-1 Matrix for broadcasting conditions and reception mode

Broad-casted	Switching mode	Output		OSD display	
		12 pin (R)	14 pin (L)	Stereo	SAP
Stereo	STE	R	L	●	–
	SAP	R	L	●	–
	MONO	L+R	L+R	●	–
Mono	STE	L+R	L+R	–	–
	SAP	L+R	L+R	–	–
	MONO	L+R	L+R	–	–
Stereo + SAP	STE	R	L	●	●
	SAP	SAP	SAP	●	●
	MONO	L+R	L+R	●	●
Mono + SAP	STE	L+R	L+R	–	●
	SAP	SAP	SAP	–	●
	MONO	L+R	L+R	–	●

● : Available, – : Not available

Note:

Of the mode selection voltages, switching voltages for STE, SAP, MONO do not output outside the module.

They are used inside the module to control the BUS.

1-4. A.PRO Section (Audio Processor)

The S.PRO section has following functions.

(1) Woofer processing (L+R output)

(2) High band, low band, balance control

(3) Sound volume control, cyclone level control

(4) Cyclone ON/OFF

All these processing are carried out according to the BUS signals sent from a microcomputer.

Fig. 2-3 shows a block diagram of the A.PRO IC.

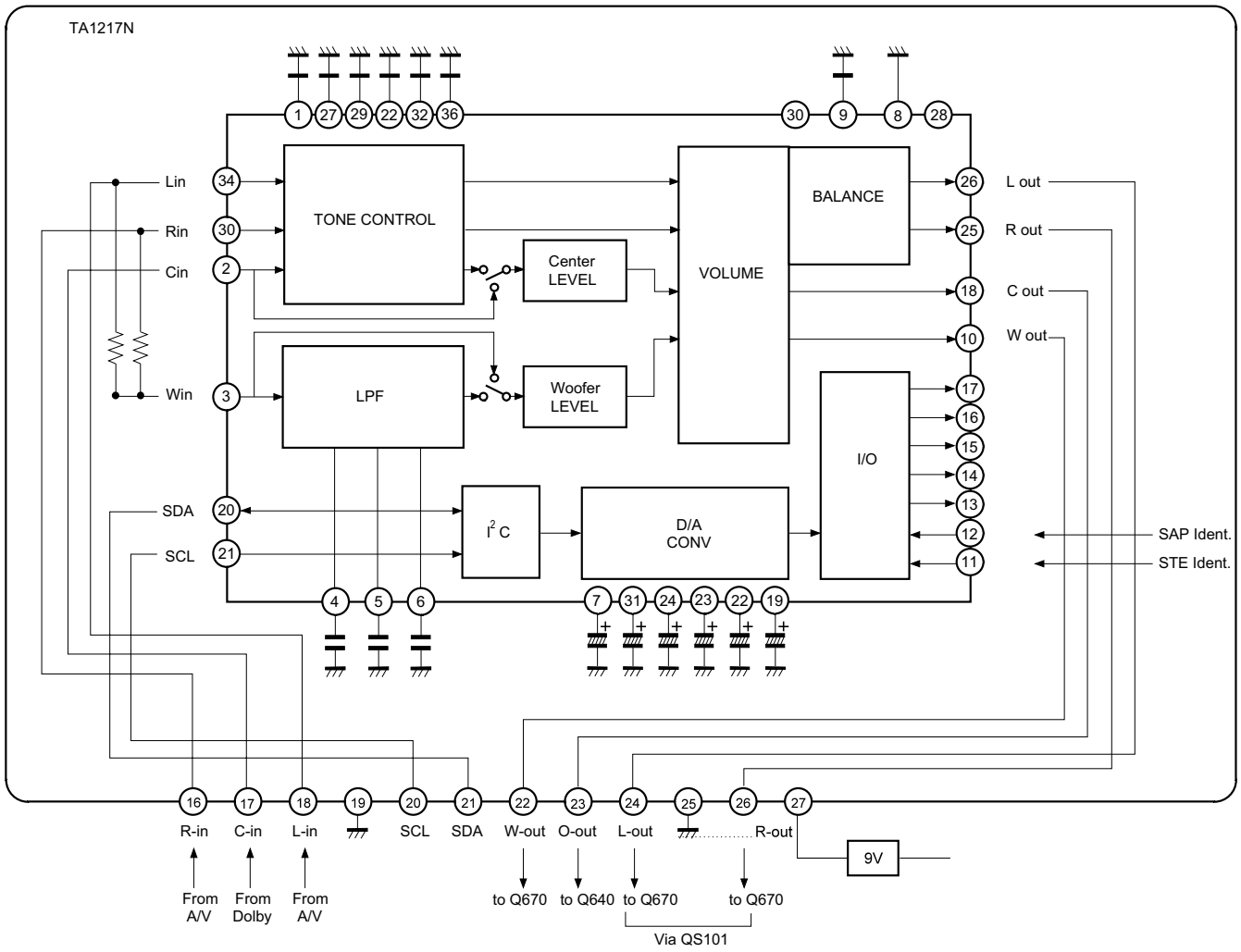


Fig. 2-3 A.PRO block diagram

Configuration of the audio circuit and signal flow are given in Fig. 2-4

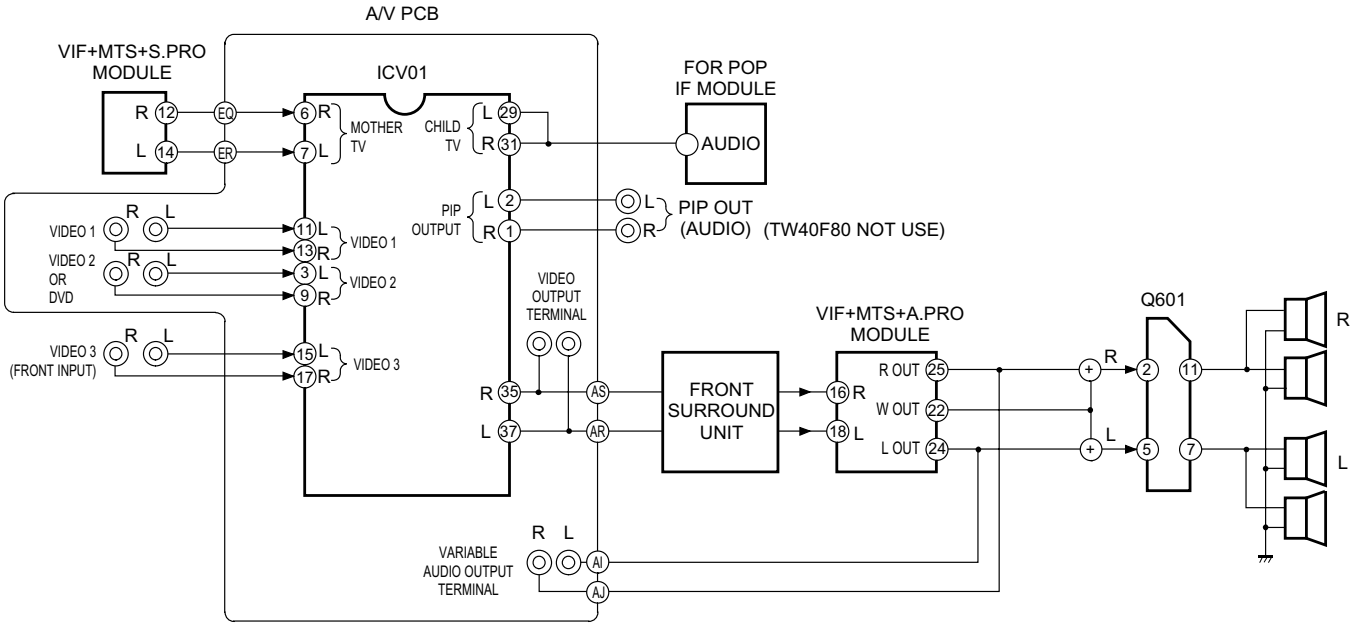


Fig. 2-4

2. POP TUNER

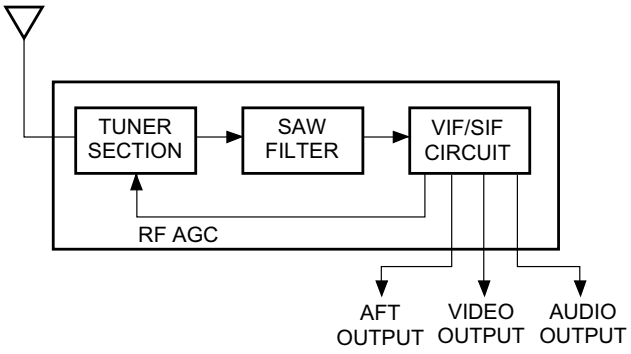


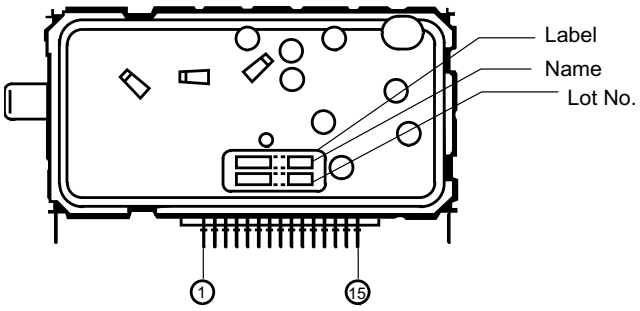
Fig. 2-5

2-1. Outline

The POP tuner (EL922L) consists of a tuner and an IF block integrated into one unit. The tuner receives RF signals induced on an antenna and develops an AFT output, video output, and audio output.

The tuner has receive channels of 181 as in the tuner for the main screen and it is also controlled through the I^2C-bus.

As the IC for the IF, a PLL complete sync detection plus audio inter carrier system are employed.



Terminal No.	Name
1	NC
2	32V
3	S-CLOCK
4	S-DATA
5	NC
6	ADDRESS
7	5V
8	RF AGC
9	9V
10	AUDIO
11	GND
12	AFT
13	NC
14	GND
15	VIDEO

Fig. 2-6 Tuner terminal layout

SECTION III: CHANNEL SELECTION CIRCUIT

1. OUTLINE OF CHANNEL SELECTION CIRCUIT SYSTEM

The channel selection circuit in the N5SS chassis employs a bus system which performs a central control by connecting a channel selection microcomputer to a control IC in each circuit block through control lines called a bus. In the bus system which controls each IC, the I^2C bus system (two line bus system) developed by Philips Co. Ltd. in the Netherlands has been employed.

The ICs controlled by the I^2C bus system are: IC for V/C/D signal processing (Q501), IC for A/V switching (QV01), IC for non volatile memory (QA02), Main and sub U/V tuners (H001, HY01), IC for deflection distortion correction (Q302), IC for POP and Double Window signal processing (QY03), IC for closed caption control (QM01), IC for WAC control (QX01), IC for 3D-YCS (QZ01), IC for AUTOLIVE (QK06).

Differences from N5SS chassis are as follows;

1. On-screen function inside microcomputer is used. Separate IC is not used for on-screen.
2. The microcomputer does not have the closed caption function, but controls separate IC for closed caption.
3. The system uses two channels of I^2C bus. One is only for non-volatile memory.

2. OPERATION OF CHANNEL SELECTION CIRCUIT

Toshiba made 8 bit microcomputer TLCS-870 series for TV receiver, TMP87CS38N-3320 is employed for QA01.

With this microcomputer, each IC and circuit shown below are controlled.

(1) CONTROL OF VIDEO/CHROMA/DEF SIGNAL PROCESS IC (Q501 Toshiba TA1222AN)

- Adjustments for uni-color, brightness, tint, color gain, sharpness and PIP uni-color
- Setting of adjustment memory values for sub-brightness, sub-color and sub-tint, etc.
- Setting of memory values for video parameters such as white balance (RGB cutoff, GB drive) and γcorrection, etc.
- Setting of video parameters of video modes (Standard, Movie, Memory)

(2) CONTROL OF A/V SWITCH IC (QV01 Toshiba TA1218N)

- Performs source switching for main screen and sub screen
- Performs source switching for TV and three video inputs

(3) CONTROL OF NON-VOLATILE MEMORY IC (QA02 Microchip 24LC08BI/P)

- Memorizes data for video and audio signal adjustment values, volume and woofer adjustment values, external input status, etc.
- Memorizes adjustment data for white balance (RGB cutoff, GB drive), sub-brightness, sub color, sub tint, etc.
- Memorizes deflection distortion correction value data adjusted for each unit.

(4) CONTROL OF U/V TUNER UNIT (H001 Toshiba ELA12L, HY01 Toshiba EL922L)

- A desired channel can be tuned by transferring a channel selection frequency data (divided ratio data) to the I^2C bus type frequency synthesizer equipped in the tuner, and by setting a band switch data which selects the UHF or VHF band.

(5) CONTROL OF DEFLECTION DISTORTION CORRECTION IC (Q302 Toshiba TA8859P)

- Sets adjustment memory value for vertical amplitude, linearity, horizontal amplitude, parabola, corner, trapezoid distortion.

(6) CONTROL OF POP & Double Window SIGNAL PROCESS IC (QY03 Toshiba TC9092AF, QY91 Sony CXP85116B-514Q)

- Controls ON/OFF and 9 pictures serch of POP.

(7) CONTROL OF CLOSED CAPTION/EDS (QM01 Motorola XC144144P)

- Controls Closed Caption/EDS.

(8) CONTROL OF WAC (QX01 Toshiba TC9097F)

- Controls Wide Aspect.

(9) CONTROL OF 3D-YCS (QZ01 Toshiba TC9086F)

- Controls ON/OFF of 3 Dimension Y/C separator.

(10) CONTROL OF VERTICAL AMPLITUDE (QK06 Toshiba TMP87CM36N)

- Controls Wide Mode.

(11) CONTROL OF OSD (Do not I^2C BUS) (QR60 Fujitsu MB90091)

- Controls of OSD Menu.

3. MICROCOMPUTER

Microcomputer TMP87CS38N-3320 has 60k byte of ROM capacity and equipped with OSD function inside.

The specification is as follow.

- Type name : TMP87CS38N-3320
- ROM : 60k byte
- RAM : 2k byte
- Processing speed : 0.5μs (at 8MHz with Shortest command)
- Package : 42 pin shrink DIP
- I^2C-BUS : two channels
- PWM : 14 bit x 1, 7 bit x 9
- ADC : 8 bit x 6 (Successive comparison system, Conversion time 20ms)

IIC device controls through I^2C bus. (Timing chart : See Fig. 3-1)

- LED uses big current port for output only.
- For clock oscillation, 8MHz ceramic oscillator is used.
- I^2C has two channels. One is for EPROM only.
- Self diagnosis function which utilizes ACK function of I^2C is equipped
- Function indication is added to service mode.
- Remote control operation is equipped, and the control by set no touch is possible. (Bus connector in the conventional bus chassis is deleted.)
- Substantial self diagnosis function
  - (1) B/W composite video signal generating function (micom inside, green crossbar added)
  - (2) Generating function of audio signal equivalent to 1kHz (micom inside)
  - (3) Detecting function of power protection circuit operation
  - (4) Detecting function of abnormality in IIC bus line
  - (5) Functions of LED blink indication and OSD indication
  - (6) Block diagnosis function which uses new VCD and AV SW

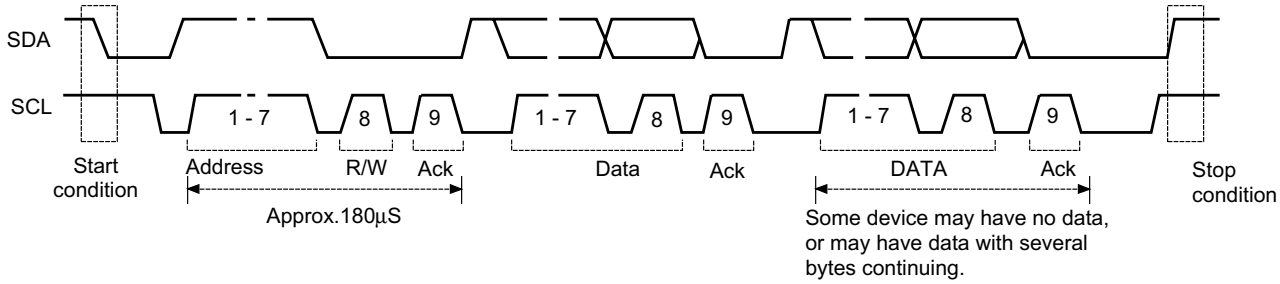


Fig. 3-1

4. MICROCOMPUTER TERMINAL FUNCTION

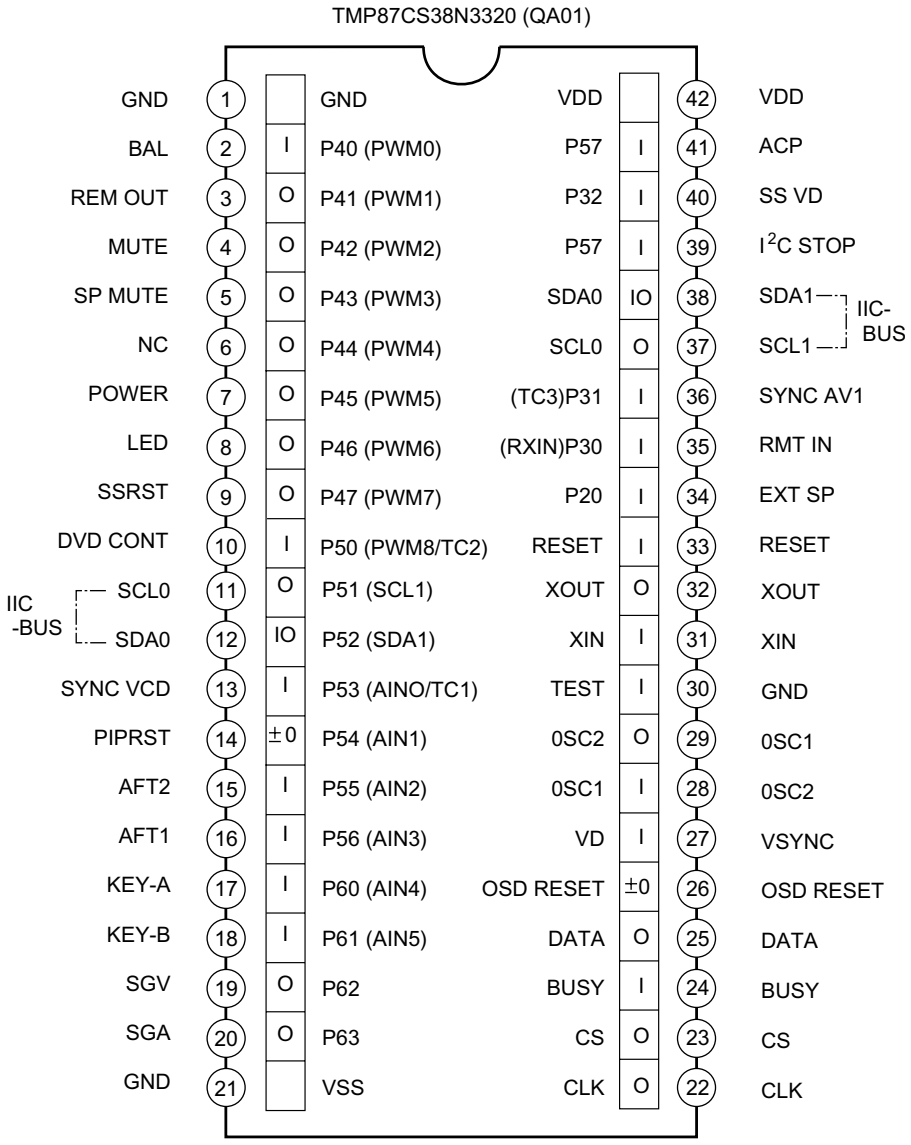


Fig. 3-2

<< MICROCOMPUTER TERMINAL NAME AND OPERATION LOGIC >>

No.	Terminal Name	Function	In/Out	Logic	Remarks
1	GND				0V
2	BAL	INPUT BALANCE	Out	PWM out	
3	REM OUT	REMOTE CONTROL SIGNAL OUT	Out	Remote control output	
4	MUTE	SOUND MUTE OUT	Out	Sound mute output	
5	SP MUTE	SPEAKER MUTE	Out	In muting = H	
6	DEF POW		Out		
7	POWER	POWER ON/OFF OUT	Out	Power control In ON = H	
8	LED	POWER LED OUTPUT	Out	Power LED on-control LED lighting = L	
9	SS RST	STARSIGHT RESET	Out	Reset = L	0V
10	DVD CONT	DVD CONTROL	Out	DVD = L, Other = H	0V
11	SCL0	IIC BUS CLOCK OUT	Out	IIC bus clock output 0	
12 13	SDA0 SYNC VCD	IIC BUS DATA IN/OUT H SYNC INPUT	In/Out In	IIC bus data input/output 0 Main picture H. sync signal input	
14	PIP RST	PIP RESET	Out	Reset = L	
15	AFT2 IN		In	Sub tuner AFT S-curve input	
16	AFT1	UV MAIN S-CURVE SIGNAL	In	Main tuner AFT S-curve signal input	
17	KEY A	LOCAL KEY INPUT	In	Local key detection: 0 to 5V	
18	KEY B	LOCAL KEY INPUT	In	Local key detection: 0 to 5V	
19	SGV	TEST SIGNAL OUT	Out	Test signal output In normal = L	0V
20	SGA	TEST AUDIO OUT	Out	Test audio output In normal = L	0V
21	VSS	POWER GROUNDING	—	0V: Gounding voltage	0V
22	CLK	CLOCK OSD	Out		At display on: Pulse
23	CS	CHIP SELECT	Out		At display on: Pulse
24	BUSY	BUSY OSD	In		At display on: Pulse
25	DATA	DATA OSD	Out		At display on: Pulse
26	OSD RESET	RESET OSD	Out	Reset = L	
27	VSYNC		In	VSYNC	Pulse
28	OSC1	DISPLAY CLOCK	Out	4.5MHz	Pulse
29	OSC2	DISPLAY CLOCK	In		Pulse
30	TEST	TEST MODE	In	GND fixed	0V
31	XIN	SYSTEM CLOCK	In	System clock input	8MHz pulse
32	XOUT	SYSTEM CLOCK	Out	System clock output 8MHz	8MHz pulse
33	RESET	SYSTEM RESET	In	System reset input (In reset = L)	5V
34	EXT SP	EXTERNAL SPEAKER	In	EXTERNAL = L, INT = H	
35	RMT IN	REMOTE CONTROL SIGNAL INPUT	In	In remote control pulse input = L	In reception of remote pulse
36	SYNC AV1	HSYNC INPUT	In	External H. sync signal input	Pulse
37	SCL1	IIC BUS CLOCK OUT	Out	IIC bus clock output 1	Pulse
38	SDA1	IIC BUS DATA IN/OUT	In/Out	IIC bus data input/output 1	Pulse
39	I^2C STP	IIC BUS STOP	In	STOP = L	
40	SS VD	STARSIGHT VD	In	VSYNC for Starsight	Pulse
41	ACP	NSYNC INPUT	In	AC pulse input	
42	VDD	POWER	—	5V	5V

5. EEPROM (QA02)

EEPROM (Non volatile memory) has function which, in spite of power-off, memorizes the such condition as channel selecting data, last memory status, user control and digital processor data. The capacity of EEPROM is 8k bits.

Type name is 24LC08BI/P or ST24C08CB6, and those are the same in pin allocation and function, and are exchangeable each other. This IC controls through I^2C bus. The power supply of EEPROM and MICOM is common. Pin function of EEPROM is shown in Fig. 3-3.

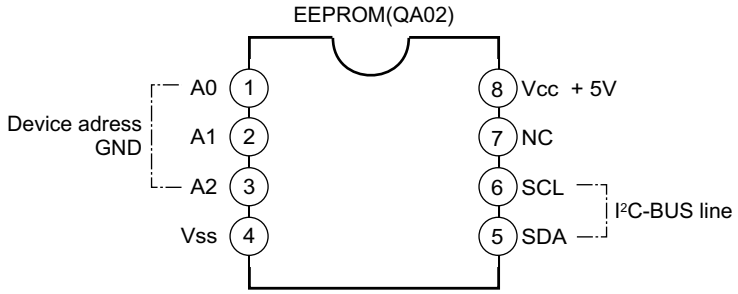


Fig. 3-3

6. ON SCREEN FUNCTION

The OSD system of TW40F80 employs the external OSD IC (QR60, MB90091) to obtain high quality OSD.

QR60 is controlled by the microprocessor QA01 with the exclusive control signals of CLK, DATA, CS, BUSY, RESET.

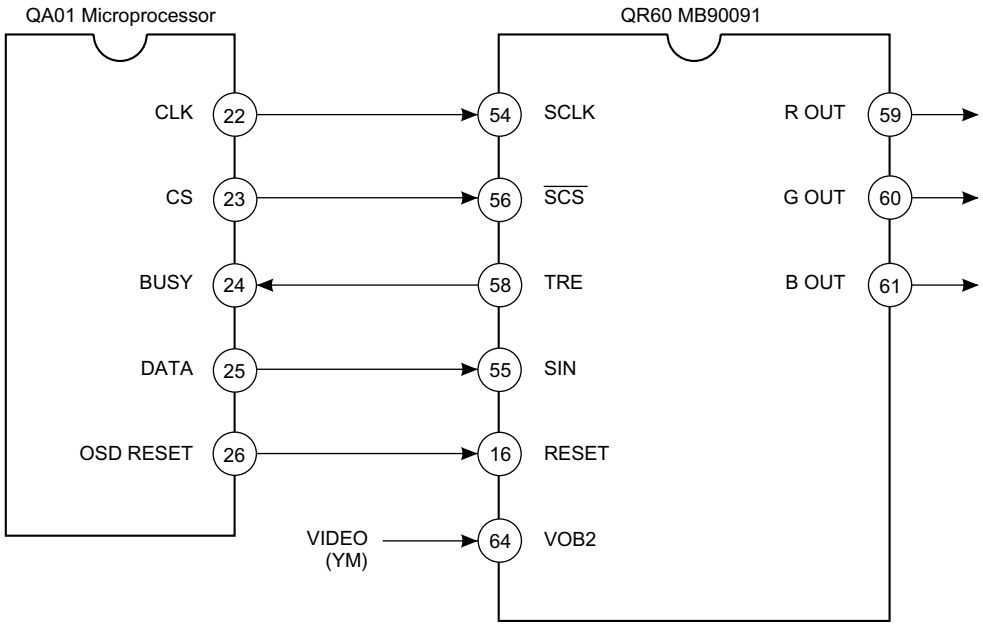


Fig. 3-4

7. SYSTEM BLOCK DIAGRAM

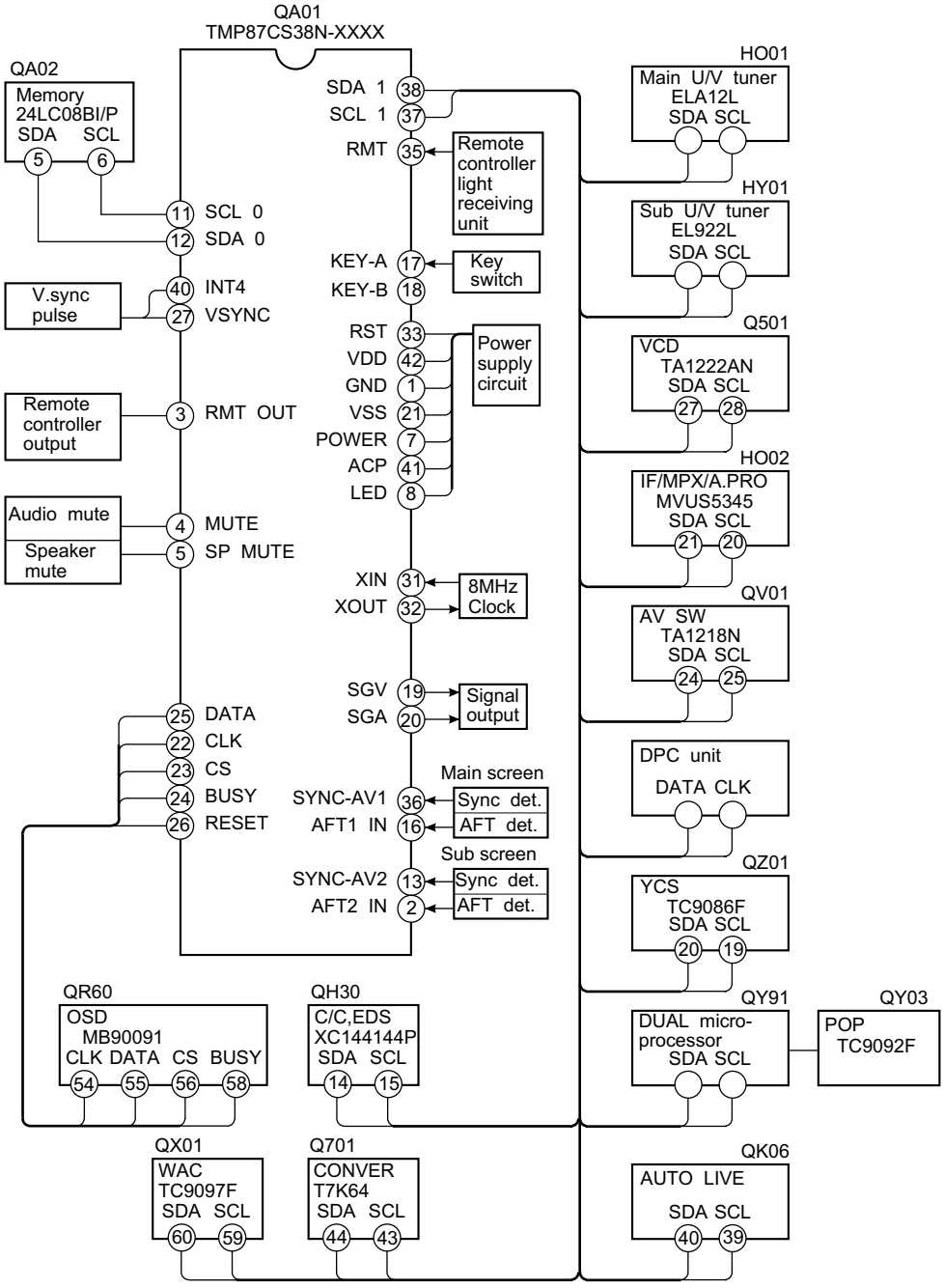


Fig. 3-5

8. LOCAL KEY DETECTION METHOD

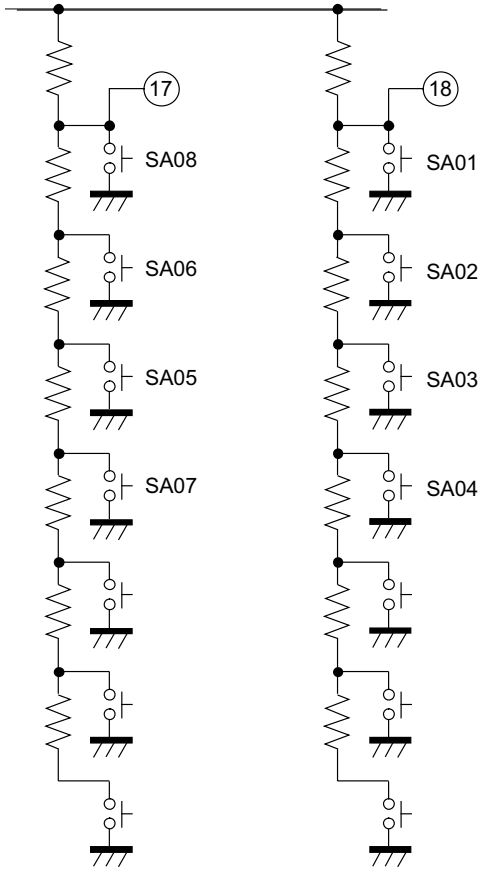


Fig. 3-6 Local key assignment

Local key detection in the N5SS chassis is carried out by using analog like method which detects a voltage appears at local key input terminals (pins 17 and 18) of the microcomputer when a key is pushed. With this method using two local key input terminals (pins 17 and 18), key detection up to maximum 14 keys will be carried out.

The circuit diagram shown left is the local key circuit. As can be seen from the diagram, when one of keys among SA-01 to SA-08 is pressed, each of two input terminals (pins 17 and 18) developes a voltage V_{IN} corresponding to the key pressed. (The voltage measurement and key identification are carried out by an A/D converter inside the microprocessor and the software.

Table 3-1 Local key assignment

Key No.	Function	Key No.	Function
SA-02	POWER	SA-01	DEMO START/STOP
SA-03	CH UP		
SA-04	CH DN		
SA-05	VOL UP		
SA-06	VOL DN		
SA-07	ANT/VIDEO, ADV		
SA-08	MENU		

9. REMOTE CONTROL CODE ASSIGNMENT

Code	Custom codes are 40-BFH (TV set for North U.S.A.)			
	Function	Applicable to remote control	Applicable to TV set	Conti-nuity
00H	0 Channel	●	●	
01H	1 Channel	●	●	
02H	2 Channel	●	●	
03H	3 Channel	●	●	
04H	4 Channel	●	●	
05H	5 Channel	●	●	
06H	6 Channel	●	●	
07H	6 Channel	●	●	
08H	8 Channel	●	●	
09H	8 Channel	●	●	
0AH	100 Channel	●	●	
0BH	ANT 1/2	●	●	
0CH	RESET		●	
0DH	AUDIO		●	
0EH	PICTURE/FUNC		●	
0FH	TV/VIDEO	●	●	
10H	MUTE	●	●	
11H	CHANNEL SEARCH	●	●	
12H	POWER	●	●	
13H	MTS	●	●	
14H	ADD/ERASE			
15H	TIMER/CLOCK	●	●	
16H	AUTO PROGRAM			
17H	CHANNEL RETURN	●	●	
18H	DSP/SUR (TV/CATV)		●	
19H	CONTROL UP	●	●	●
1AH	VOLUME UP	●	●	●
1BH	CHANNEL UP	●	●	●
1CH	RECALL	●	●	
1DH	CONTROL DOWN	●	●	●
1EH	VOLUME DOWN	●	●	●
1FH	CHANNEL DOWN	●	●	●
40H	PIP LOCATE ↑			
41H	PIP LOCATE ↓			
42H	PIP LOCATE →			
43H	PIP LOCATE ←			
44H	CARVER			
45H	SURROUND UP			
46H	SURROUND DOWN			
47H	VOCAL ZOOM			
48H	CHANNEL LOCK			
49H				
4AH	PIP CHANNEL UP	●	●	●
4BH	PIP CHANNEL DOWN	●	●	●
4CH	PIP STILL/RELEASE	●	●	
4DH	PIP ZOOM, ZOOM SIZE			
4EH	PIP LOCATE (CH SEARCH)		●	
4FH	PIP SOURCE	●	●	

Code	Custom codes are 40-BFH (TV set for North U.S.A.)			
	Function	Applicable to remote control	Applicable to TV set	Conti-nuity
50H	PIP STILL	●	●	
51H	PIP ON/OFF	●	●	
52H	Do not use. Old type core power ON			
53H	PIP SWAP	●	●	
54H	PIC SIZE	●	●	
55H	DSP F/R			
56H	WIDE/SCROLL			
57H	CAPTION		●	
58H	EXIT	●	●	
59H	CYCLONE, SBS		●	
5AH	SET UP		●	
5BH	OPTION			
5CH	SUB WOOFER UP			
5DH	SUB WOOFER DOWN			
5EH				
5FH				
80H	MENU	●	●	
81H	EDS	●	●	
82H	ADV UP	●	●	
83H	ADV DWN	●	●	
84H				
85H	GUIDE			
86H	THEME			
87H	LIST			
88H	PIP CONTROL			
89H	ENTER/TUNE	●	●	
8AH	PAGE UP			
8BH	DATA UP			
8CH	PAGE DN			
8DH	DATA DN			
8EH	CANCEL			
8FH	REC			
90H				
91H				
92H	Do not use. Old type core power ON			
93H				
94H				
95H				
96H				
97H	NOISE CLEAN			
98H				
99H				
9AH	PIP VOLUME UP			
9BH				
9CH	PIP CONTROL			
9DH				
9EH	PIP VOLUME DOWN			
9FH				

Code	Custom codes are 40-BFH (TV set for North U.S.A.)		
	Function	Applicable to TV set	Conti-nuty
A0H	SUB-BRIGHT ADJUSTMENT	●	
A1H	G. DRIVE ADJUSTMENT	●	
A2H	B. DRIVE ADJUSTMENT	●	
A3H			
A4H	CUTOFF DRIVE 40H INITIALIZING, HORIZONTAL ONE LINE	●	
A5H	R. CUTOFF ADJUSTMENT	●	
A6H	G. CUTOFF ADJUSTMENT	●	
A7H	B. CUTOFF ADJUSTMENT	●	
A8H	MEMORY ALL AREA INITIALIZE	●	
A9H	PIP BRIGHT ADJUSTMENT	●	
AAH	SUB CONTRAST ADJUSTMENT	●	
ABH	HOR, VER PICTURE POSITON ADJUSTMENT	●	
ACH	SUB COLOR ADJUSTMENT	●	
ADH	SUB TINT ADJUSTMNET	●	
AEH	ADJUSTMENT-UP	●	●
AFH	ADJUSTMENT-DOWN	●	●
B0H	HORIZONTAL ONE LINE: SERVICE	●	
B1H	DSP ON/OFF	●	
B2H	TEXT-1	●	
B3H	TV/PIP VIDEO CHANGE-OVER	●	
B4H	CAPTION-1	●	
B5H			
B6H			
B7H	TV/CABLE CHANGE-OVER IN SAME TIME ON MAN AND SUB	●	
B8H	HOTEL SETTING MENU		
B9H	DATA 4 TIMES SPEED UP	●	●
BAH	DATA 4 TIMES SPEED DOWN	●	●
BBH	CHANGE-OVER OF HOTEL/NORMAL		
BCH	PIP CENTER	●	
BDH	M MODE	●	
BEH	CAPTON OFF	●	
BFH	ALL CHANNEL PRESET		
C0H		●	
C1H	DIRECT WIDE 1	●	
C2H	DIRECT FULL		
C3H			
C4H			
C5H			
C6H			
C7H			
C8H			
C9H			
CAH			
CBH			
CCH			
CDH			
CEH			
CFH			

Code	Custom codes are 40-BFH (TV set for North U.S.A.)		
	Function	Applicable to TV set	Conti-nuty
D0H			
D1H			
D2H	Do not use. Old type core power ON		
D3H			
D4H			
D5H			
D6H			
D7H	PIP VIDEO ADJ.		
D8H	STILL, FRAME ADVANCE		
D9H			
DAH	SPEED		
DBH			
DCH	ZOOM		
DDH			
DEH			
DFH			
E0H	PINCUTION/EW CORER (PARA/CNR)	●	
E1H	VERTICAL S-CUVE CORRECTION/ VERTICAL M-CURVE CORRECTION (VSC/FVC)	●	
E2H			
E3H			
E4H			
E5H			
E6H			
E7H			
E8H			
E9H		●	
EAH	HORIZONTAL WIDTH (WID/PARA)	●	
EBH	TRAPEZOIDE CORRECTION (TRAP)		
ECH	TEST TONE		
EDH	DOLBY	●	
EEH	3 DIMENTIONAL Y/C SEPARATION	●	
EFH	DPC	●	
E0H	STANDARD (HEIGHT LINEARITY) (VLIN/HIT)	●	
E1H	WIDE (HEIGHT ® LINEARITY) (VLIN)	●	
F2H	SCROOL	●	
F3H	WIDE 1, 2, 3		
F4H			
F5H			
F6H			
F7H			
F8H			
F9H			
FAH			
FBH			
FCH			
FDH			
FEH			
FFH			

9-1. Optional Setting for Each Model

MODELS	OPT0									OPT1								
	D7	D6	D5	D4	D3	D2	D1	D0	HEX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
CN35F90	0	*	0	0	*	0	0	*	00H	0	0	0	0	0	0	*	*	00H
CN35F95	0	*	0	0	*	0	0	*	00H	0	0	0	0	0	0	*	*	00H
CX35F70	1	*	0	1	*	0	1	*	02H	0	0	0	0	0	0	*	*	00H
TW56F80	0	*	0	0	*	0	1	*	02H	0	0	0	1	1	1	*	*	1CH
TW40F80	1	*	0	1	*	0	1	*	92H	0	0	0	1	1	0	*	*	18H
TP61F90	0	*	0	0	*	0	1	*	02H	0	0	0	1	1	1	*	*	1CH
TP61F80	0	*	0	1	*	0	1	*	12H	0	0	0	1	0	0	*	*	18H
TP55F80	0	*	0	1	*	0	1	*	12H	0	0	0	1	0	0	*	*	10H
TP55F81	0	*	0	1	*	0	1	*	12H	0	0	0	1	0	0	*	*	10H
TP50F90	0	*	0	0	*	0	1	*	02H	0	0	0	1	0	1	*	*	14H
TP50F60	1	*	0	1	*	0	1	*	92H	0	0	0	1	0	0	*	*	10H
TP50F61	1	*	0	1	*	0	1	*	92H	0	0	0	1	0	0	*	*	10H
	DSP0/SRD1	NOT USED	PP0/MP1	SS/0 NONSS/1	NOT USED	Normal 0/f0 STOP 1	CYC0/SBS1	NOT USED		Normal 0/Free run 1	MODE: Fixed Normal00 STD: 01 HRC: 10 1RC: 11		NON0/CONV1	NON0/3DYC	NON0/DOLBY1	NOT USED	NOT USED	

- When the character generation is changed from MB90091-107 TO MB90091-108, D5 bit of OPT0 in the design data should be set to “1”.

10. ENTERING TO SERVICE MODE

1. PROCEDURE

(1) Press once MUTE key of remote hand unit to indicate MUTE on screen.

(2) Press again MUTE key of remote hand unit to keep pressing until the next procedure.

(3) In the status of above (2), wait for disappearing of indication on screen.

(4) In the status of above (3), press MENU (Channel setting) key on TV set.

2. Service mode is not memorized as the last-memory.
3. During service mode, indication S is displayed at upper right corner on screen.

11. TEST SIGNAL SELECTION

1. In OFF state of test signal, SGA terminal (Pin 20) and SGV terminal (Pin 21) are kept “L” condition.
2. The function of VIDEO test signal selection is cyclically changed with VIDEO key (remote unit).

Table 3-2

Test Signal No.	Name of Pattern
0	Signal OFF
1	All black signal + R single color (OSD)
2	All black signal + G single color (OSD)
3	All black signal + B single color (OSD)
4	All black signal
5	All white signal
6	W/B
7	Black cross bar
8	White cross bar
9	Black cross hatch
10	White cross hatch
11	White cross dot
12	Black cross dot
13	H signal (bright area)
14	H signal (dark area)
15	Black cross + G signal color

(3) SGA (audio test signal) output should be square wave of 1 kHz.

12. SERVICE ADJUSTMENT

1. ADJUSTMENT MENU INDICATION ON/OFF : MENU key (on TV set)
2. During display of adjustment menu, the followings are effective.
   a) Selection of adjustment item :
      POS UP/DN key (on TV/remote unit)
   b) Adjustment of each item :
      VOL UP/ DN key (on TV / remote unit)
   c) Direct selection of adjustment item
      R CUTOFF : 1 POS (remote unit)
      G CUTOFF : 2 POS (remote unit)
      B CUTOFF : 3 POS (remote unit)
   d) Data setting for PC unit adjustment
      SUB CONTRAST : 4 POS (remote unit)
      SUB COLOR : 5 POS (remote unit)
      SUB TINT : 6 POS (remote unit)
   e) Horizontal line ON/OFF : VIDEO (on TV set)
   f) Test signal selection : VIDEO (remote unit)
   * In service mode, serviceable items are limited.

3. Test audio signal ON / OFF : 8 POS (remote unit)
   * Test audio signal : 1 kHz

4. Self check display : 9 POS (remote unit)
   * Cyclic display (including ON/OFF)

5. Initialization of memory :
   CALL (remote unit) + POS UP (on TV set)
6. Initialization of self check data :
   CALL (remote unit) + POS DN (on TV set)
7. BUS OFF :
   CALL (remote unit) + VOL UP (on TV set)

13. FAILURE DIAGNOSIS PROCEDURE

Model of N5SS chassis is equipped with self diagnosis function inside for trouble shooting.

13-1. Contents to be Confirmed by Customer

Table 3-3

Contents of self diagnosis	Display items and actual operation
A. DISPLAY OF FAILURE INFORMATION IN NO PICTURE (Condition of display)	Power indicator lamp blinks and picture does not come.
1. When power protection circuit operates;	1. Power indicator red lamp blinks. (0.5 seconds interval)
2. When I^2C-BUS line is shorted;	2. Power indicator red lamp blinks. (1 seconds interval)
	If these indication appears, repairing work is required.

13-2. Contents to be Confirmed in Service Work (Check in self diagnosis mode)

Table 3-4

Contents of self diagnosis	Display items and actual operation
Contents of self diagnosis < Countermeasure in case that phonomenon always arises > B. Detection of shortage in BUS line. C. Check of comunication status in BUS line. D. Check of signal line by sync signal detection. E. Indication of part code of microcomputer (QA01). F. Number of operation of power protection circuit.	Display items and actual operation (Example of screen display) SELF CHECK NO. 239XXXX ← Part coce of QA01 ← E POWER: 000000 ← Number of operation of power protection circuit ← F BUS LINE: OK ← Short check of bus line ← B BUS CONT: OK ← Communication check of busline ← C BLOCK: UV V1 V2 ← D QV01, QV01S

13-3. Executing Self Diagnosis Function

[CAUTION]

(1) When executing block diagnosis, get the desired input mode (U/V BS VIDEO1, 2, 3) screen, and then enter the self diagnosis mode.

(2) When diagnos other input mode, do again diagnosis operation.

13-3-1. Procedure

(1) Set to service mode.

(2) Pressing “9” key on remote unit displays self diagnosis result on screen.

Every pressing changes mode as below.

SERVICE mode → SELF DIAGNOSIS mode

(3) To exit from service mode, turn power off.

13-4. Understanding Self Diagnosis Indication

In case that phenomenon always arises. See Fig. 3-7 .

(Example of screen display)

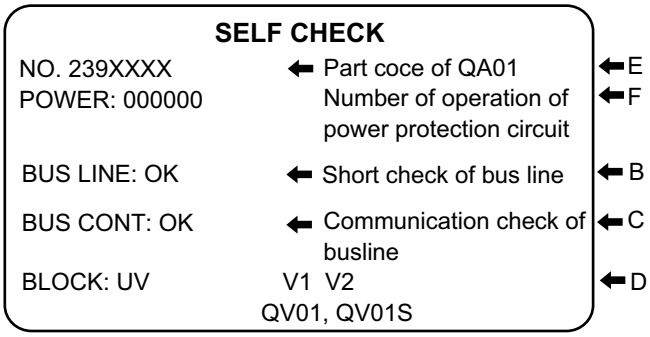


Fig. 3-7

Table 3-5

Item	Contents	Instruction of results
BUS LINE	Detection of bus line short	Indication of OK for normal result, NG for abnormal
BUS CONT	Communication state of bus line	Indication of OK for normal result Indication of failure place in abnormality (Failure place to be indicated) QA02 NG, H001 NG, Q501 NG, H002 NG, QV01 NG, Q302 NG, QY02 NG, HY01 NG, QD04 NG, QM01 NG, Q701 NG **Note:** The indication of failure place is only one place though failure places are plural. When repair of a failure place finishes, the next failure place is indicated. (The order of priority of indication is left side.)
BLOCK: UV1 UV2 V1 V2	The sync signal part in each video signal supplied from each block is detected. Then by checking the existence or non of sync part, the result of self diagnosis is displayed on screen. Besides, when “9” key on remote unit is pressed, diagnosis operation is first executed once.	* Indication by color • Normal block : Green • Non diagnosis block : Cyan

13-4-1. Clearing method of self diagnosis result

In the error count state of screen, press “CHANNEL DOWN” button on TV set pressing “DISPLAY” button on remote unit.

CAUTION:

All ways keep the following caution, in the state of service mode screen.

- Do not press “CHANNEL UP” button. This will cause initialization of memory IC. (Replacement of memory IC is required.)
- Do not initialize self diagnosis result. This will change user adjusting contents to factory setting value. (Adjustment is required.)

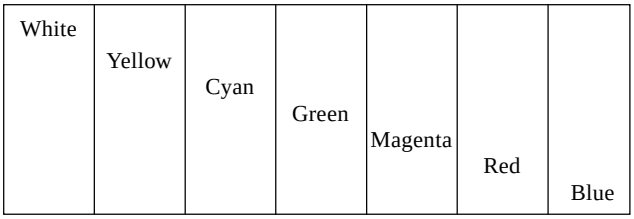
13-4-2. Method utilizing inner signal

(VIDEO INPUT 1 terminal should be open.)

(1) With service mode screen, press VIDEO button on remote unit. If inner video signal can be received, QV01 and after are normal.

(2) With service mode screen, press “8” button on remote unit. If sound of 1 kHz can be heard, QV01 and after are normal.

* By utilizing signal of VIDEO input terminal, each circuit can be checked. (Composite video signal, audio signal)

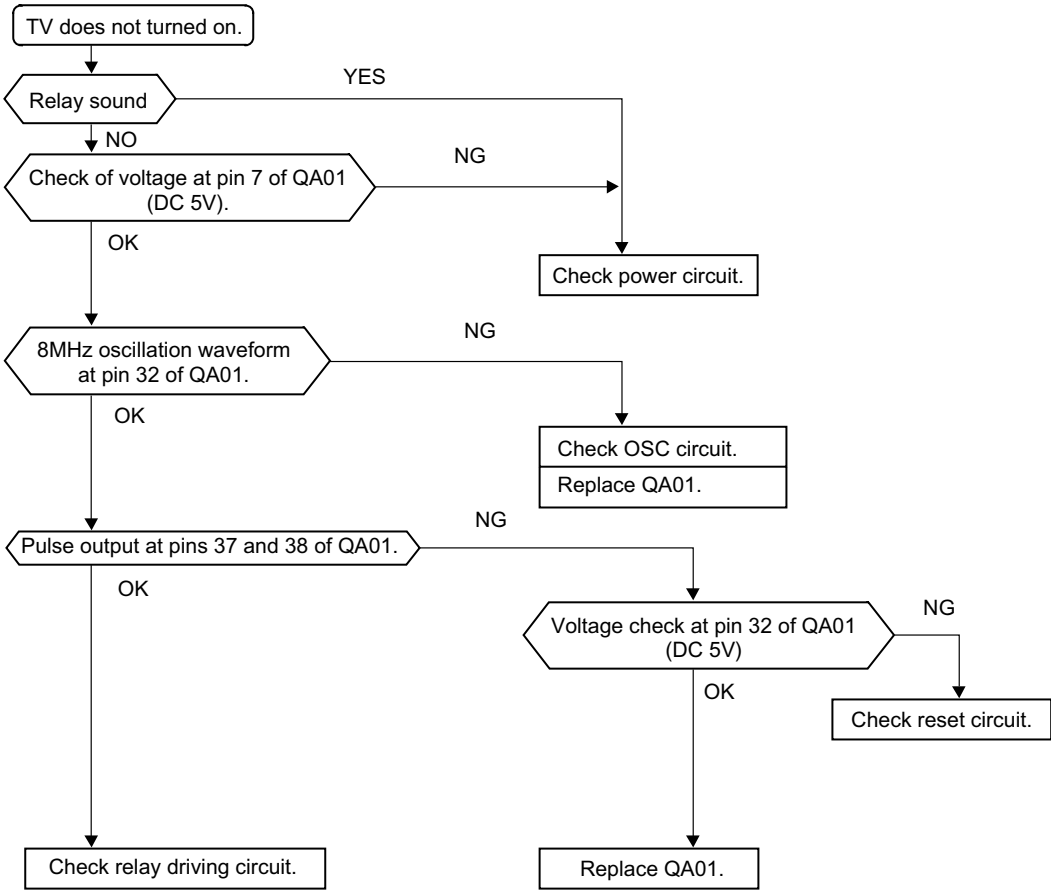


(COLOR BAR SIGNAL)

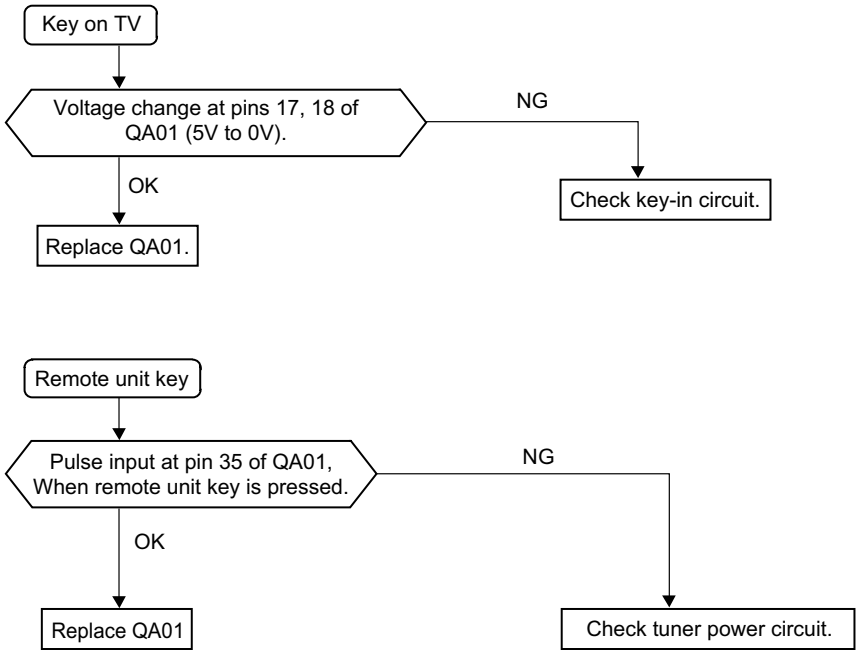
Color elements are positioned in sequence of high brightness.

14. TROUBLESHOOTING CHART

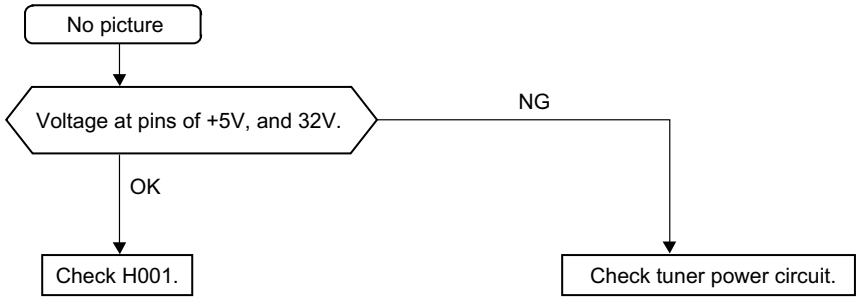
14-1. TV does Not Turned ON



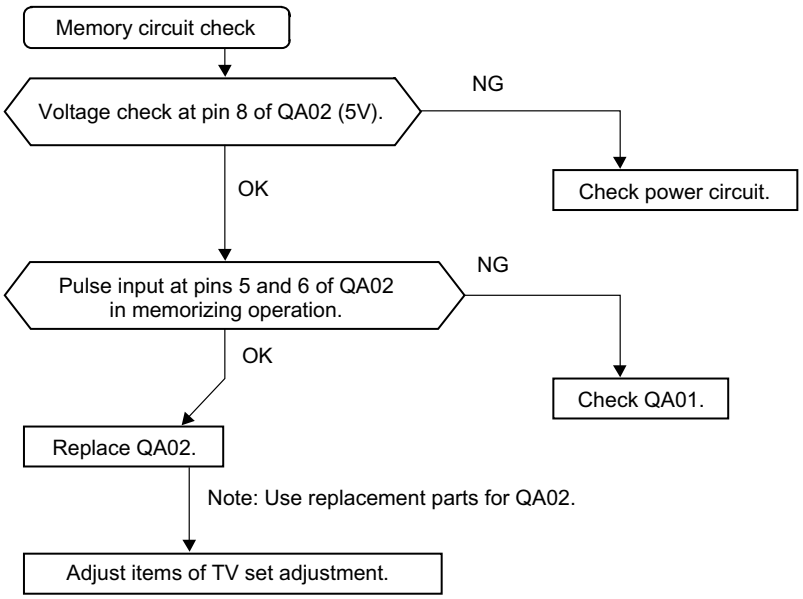
14-2. No Acception of KEY-IN



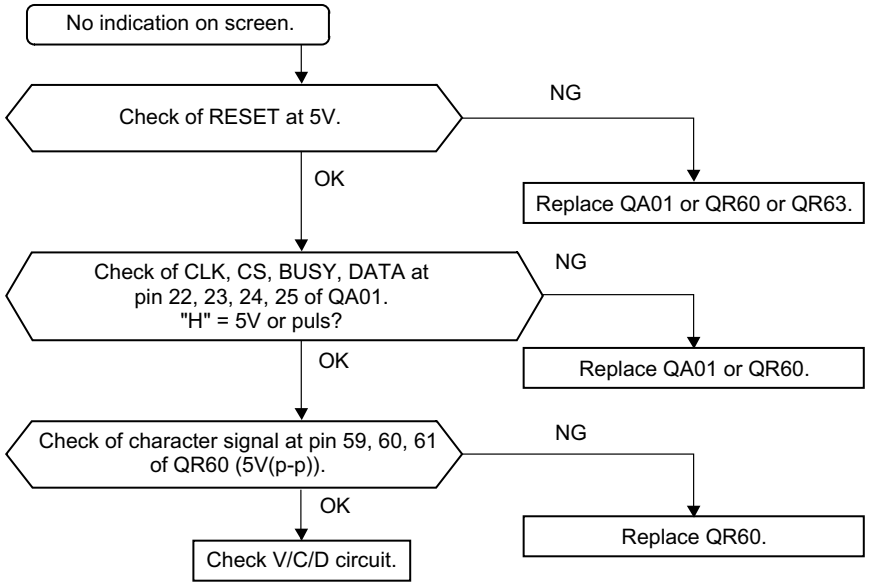
14-3. No Picture (Snow Noise)



14-4. Memory Circuit Check



14-5. No Indication On Screen



SECTION IV: DVD SWITCH CIRCUIT

1. DVD SWITCH BLOCK DIAGRAM

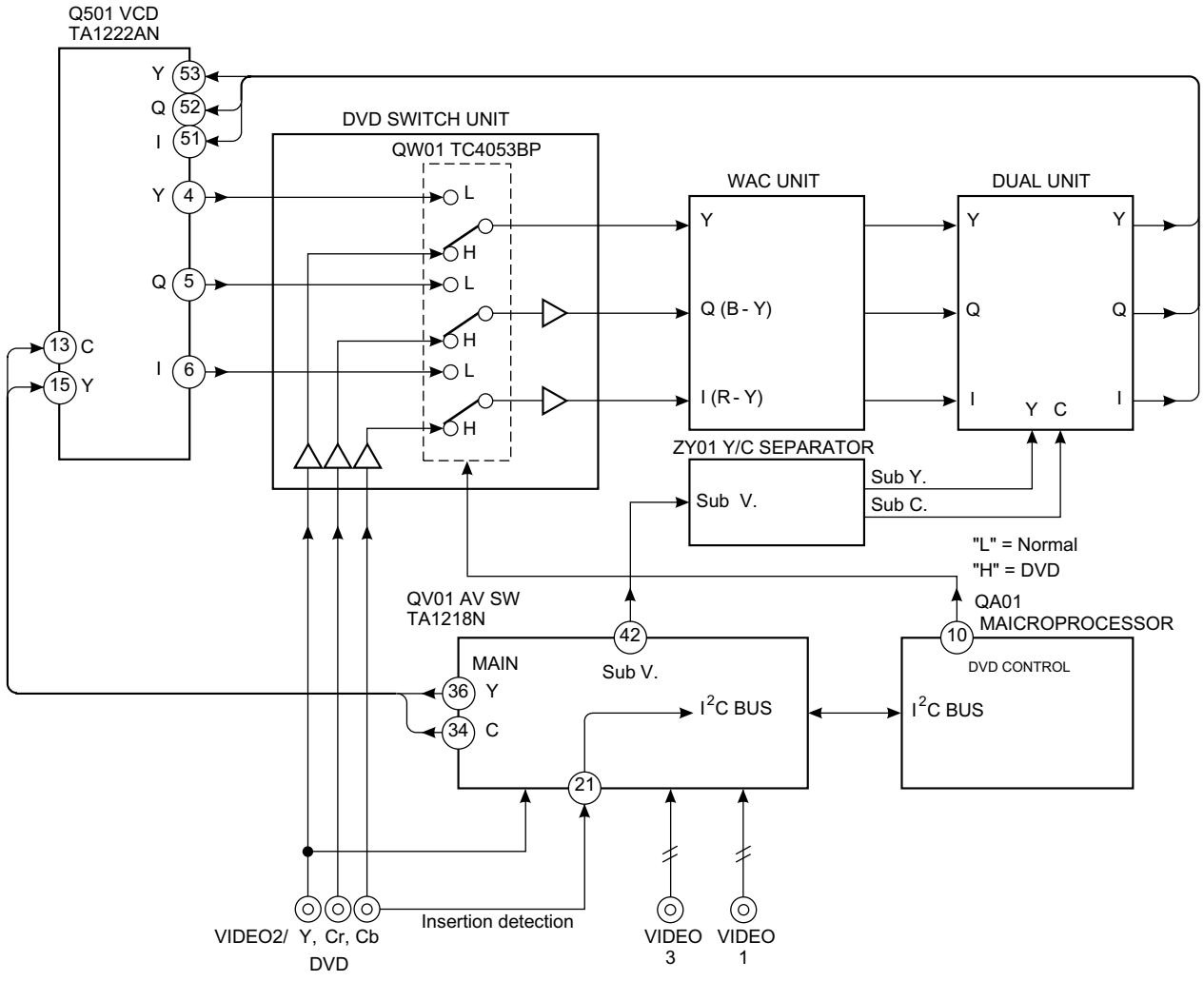


Fig. 4-1

2. OUTLINE

In this model, the DVD input terminals are provided in order to receive the color difference signals (Y, Cr, Cb) output from a DVD player.

The luminance (Y) signal input for DVD input uses the VIDEO input terminal in common with the VIDEO 2 input. The terminals for color difference signal inputs Cr (R – Y) and Cb (B – Y) are used exclusively.

The input identification for VIDEO 2 and DVD is carried out by setting pin 21 of QV01 TA1218N (AV SW IC) from "L" to "H" when the cable is connected to the Cb input terminal with a switch equipped.

The main microprocessor QA01 sets pin 10 of QA01 from "L" to "H" through I^2C bus when pin 21 of AW SW IC develops "H".

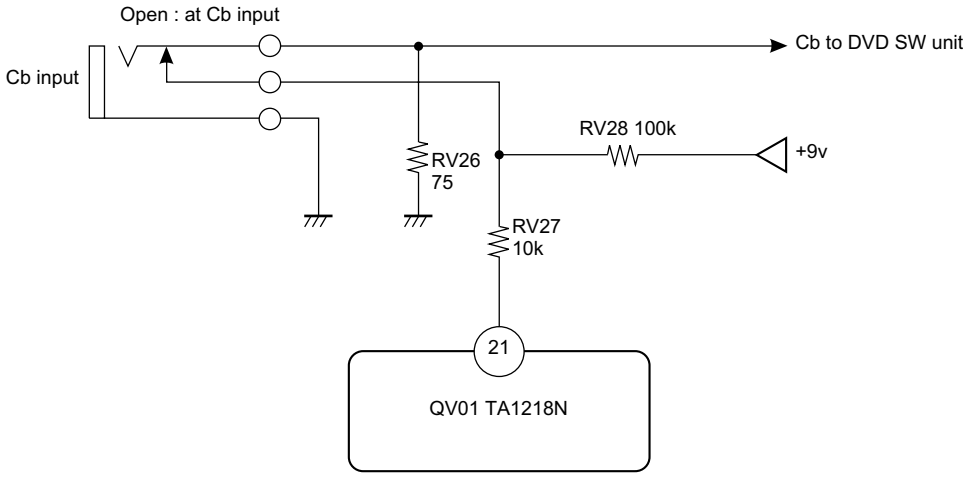


Fig. 4-2

SECTION V: WAC CIRCUIT

1. OUTLINE

A wide aspect conversion (hereafter called WAC) process (3/4 compression process in 4:3 mode and 1/2 compression process on left screen in double window mode) is performed inside the WAC unit (PB6348) in TW40F80.

Screen modes for TF40F80 contain THEATER WIDE1, THEATER WIDE 2, THEATER WIDE3, FULL, NORMAL and DOUBLE WINDOW modes. The video signal compression is carried out only when either the NORMAL or DOUBLE WINDOW mode is selected. In the modes other than the NORMAL and DOUBLE WINDOW mode, the video signal input to WAC unit is output without performing any process.

The screen in the DOUBLE WINDOW mode creates a single screen by superimposing the left screen processed in the WAC unit on the right screen processed in the DUAL unit.

On the left screen, the video signal sent is time-compressed to 1/2 in horizontal direction to fit in the left half of the wide screen with 16:9 aspect ratio. In this case, a black level of DC is attached on the right half of the screen in this circuit. However, this is superimposed on the right screen, so nothing is visible on the screen.

In the normal screen, the video signal is 3/4 time-compressed and side panels in the black level are added on sides of the screen.

2. CIRCUIT OPERATION

2-1. Configuration

The WAC unit consists of a wide aspect conversion IC (QX01, TC9097F, working as a central device), clock generation IC (QX02, TA8667F), switch IC (QX03, TC4053BF), and peripheral circuits (LPF, AMP, emitter follower, etc.). The QX01 (TC9097F) contains an A/D converter, D/A converter, clamp circuit, VCO circuit, etc. and performs compression process, etc. inside the IC for analog video signals entered according to controls through IIC bus, thus providing the signal as an analog signal.

2-2. Operation

2-2-1. Signal Flow

Fig. 5-1 shows a block diagram of this circuit. A Y signal entered through pin 6 of PX01 passes a low pass filter an a 6 dB amplifier, and enters pin 3 of QX01. On the other hand, I and Q signals enter through pin 4 and 5 of PX01, and pass a low pass filter and amplifiers in the same way as the Y signal, and enter pins 1 and 78 of QX01 respectively.

The Y , I and Q signals entered are clamped by built-in clamp circuit, converted into digital signals by the built-in A/D converter. Moreover, their read/write operations are rated up by twice or 3/4 times to perform a compression process of 1/2 or 3/4 times inside the built-in line memory. And then, a black level signal is added to the open area (right half, or both sides of screen). Next, the signal is converted to an analog Y, I, and Q signals by a built-in D/A converter and output from pins 17, 13, and 9. Parameters of 1/2, 3/4 phase of the video signal, phase of the side panel, etc. are controlled through I^2C bus, control signals of which enters from pins 7 and 8 of PX01.

Thus processed signals are fed to a low pass filter to remove high frequency noises generated in QX01 and then fed to the QX03 switching IC. The compressed signal and a not compressed signal entered from PX01 are directly fed to QX03, and switched by a signal showing compression/not compression (NCS = output from pin 61 of QX01 and fed to the receive unit through pins 5, 6, and 7 of PX02.

2-2-2. Clock Generation

The system clock for QX01 is generated by QX02 according to an H reference signal supplied from pin 3 of PX02 and fed to QX01 through QX19 and QX40. (The frequency is adjusted to 28.7 ± 0.2 MHz with LX18).

The compressing operation is carried out by setting the write clock to 1/2 or 3/4 times by the built-in VCO with the reading clock fed to pin 47 of QX01.

2-2-3. Timing Pulse Generation

Moreover, the WAC unit generates following timing pulses.

(1) VPout

Reference signal entered through pin 2 of PX02 enters pin 3 of QX01, and outputs at pin 8 of PX02 after delayed by an amount required. The vertical reference signal is output in modes other than the normal and double window and fed to the vertical circuit. Accordingly, the raster becomes an horizontal one when the unit is disconnected.

(2) HVBLK

This pulse is a timing pulse showing a black extension mask period in the normal and double window modes. It outputs at pin 1 of PX02 and enters pin 30 of Q501 in the receive unit.

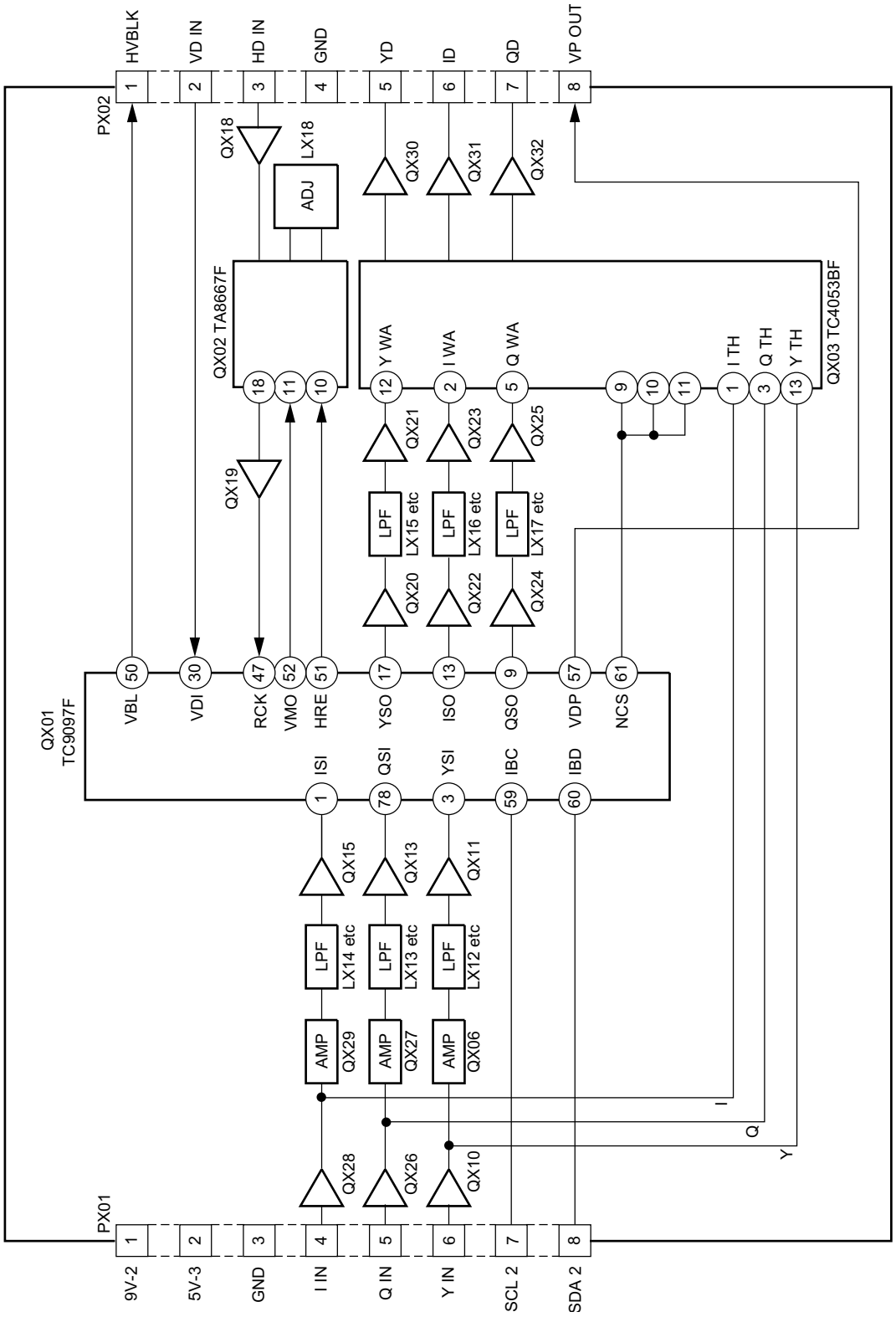


Fig. 5-1 Wide aspect conversion unit block diagram (PB6348)

- **Pin Function**

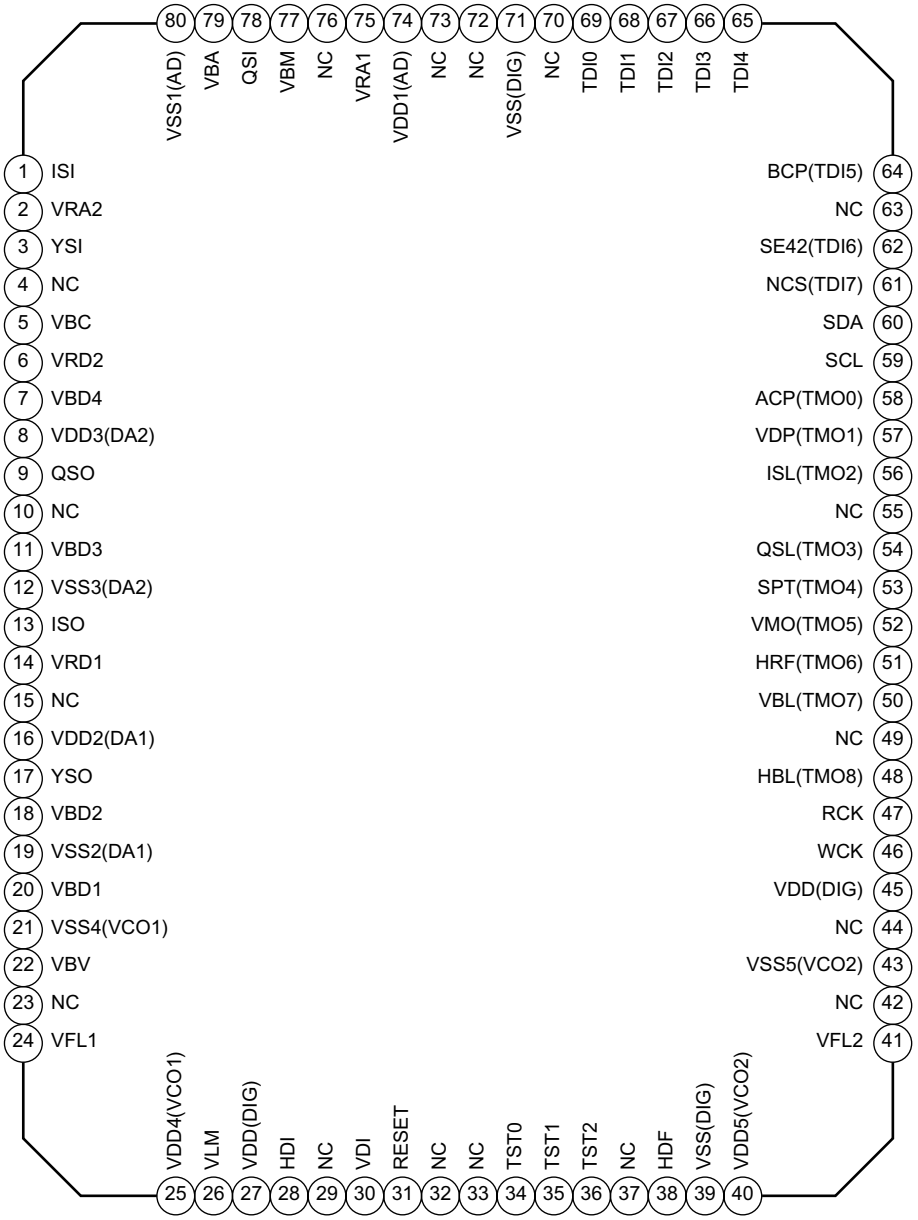


Fig. 5-2 Pin function of TC9097F (QFP 80 pin)

Table 5-1 Names and functions of TC9097F

No.	Name	I/O	Function
1	ISI	I	I color signal input
2	VRA2	–	Reference voltage (low level) for AD1, AD2
3	YSI	I	Y signal input
4	NC	–	–
5	VBC	–	Bias for clamp 1
6	VBD2	–	Reference voltage for DA2, DA3
7	VBD4	–	Bias 2 (high level) for DA2, DA3
8	AVDD	–	Analog power
9	QSO	O	Q color signal output
10	NC	–	–
11	VBD3	–	Bias 2 (low level) for DA2, DA3
12	AGND	–	Analog ground
13	ISO	O	I signal output
14	VRD1	–	Reference voltage for DA1
15	NC	–	–
16	AVDD	–	Analog power
17	YSO	O	Y signal output
18	VBD2	–	Bias 1 (high level) for DA1
19	AGND	–	Analog ground
20	VBD1	–	Bias 2 (high level) for DA1
21	AGND	–	Analog ground
22	NC	–	–
23	VFV	I	Connected to VSS or VDD
24	VFL1	–	Connected to VDD
25	AVDD	–	Analog power
26	VLM	–	1/2 VDD for line memory
27	VDD	–	Digital power
28	HDI	I	Composite sync signal input
29	NC	–	–
30	VD1	I	V sync signal input
31	RESET	I	Reset input (Normally: High level, Reset: Low level)
32	NC	–	–
33	NC	–	–
34	TST0	I	Test mode setting (normally connected to VSS)
35	TST1	I	Test mode setting (normally connected to VSS)
36	TST2	I	Test mode setting (normally connected to VDD)
37	NC	–	–

No.	Name	I/O	Function
38	HDF	I	Ext. H sync signal input
39	GND	–	Digital ground
40	AVDD	–	Analog power
41	VFL2	I	Loop filter for VCO2
42	NC	–	–
43	AGND	–	Analog ground
44	CKSEL	–	VDD
45	VDD	–	Digital power
46	WCK	–	Ext. clock input (memory write clock)
47	RCK	O	Ext. clock input (memory read clock)
48	HBL	–	H blanking signal
49	NC	–	
50	VBL	–	V blanking signal
51	HRF	O	H AFC reference signal
52	VMO	–	H AFC mask signal
53	SPT	–	Side panel timing signal
54	QSL	–	Q signal select pulse
55	NC	O	–
56	ISL	–	I signal select pulse
57	VDP	–	V drive pulse
58	ACP	–	Later stage clamp pulse
59	SCL	–	I^2C SCL signal input
60	SDA	–	I^2C SDA signal input/output
61	NCS	I	Prefilter switch signal 1
62	SE42	–	Prefilter switch signal 2
63	NC	–	–
64	BCP	–	Prestage clamp pulse output
65	TD14	–	Test input (normally connected to VSS)
66	TD13	I	Test input (normally connected to VSS)
67	TD12	–	Test input (normally connected to VSS)
68	TD11	I	Test input (normally connected to VSS)
69	TD10	I	Test input (normally connected to VSS)
70	NC	–	–
71	GND	–	Digital ground
72	NC	I	
73	NC	I	
74	AVDD	I	Analog power
75	VRA1	–	Reference voltage for AD1, AD2

No.	Name	I/O	Function
76	NC	–	–
77	VBM	–	Bias for MPX, clamp 2
78	QSI	I	Q color signal input
79	VBA	–	Bias for AD1, AD2
80	AGND	–	Analog ground

3. BLOCK DIAGRAM

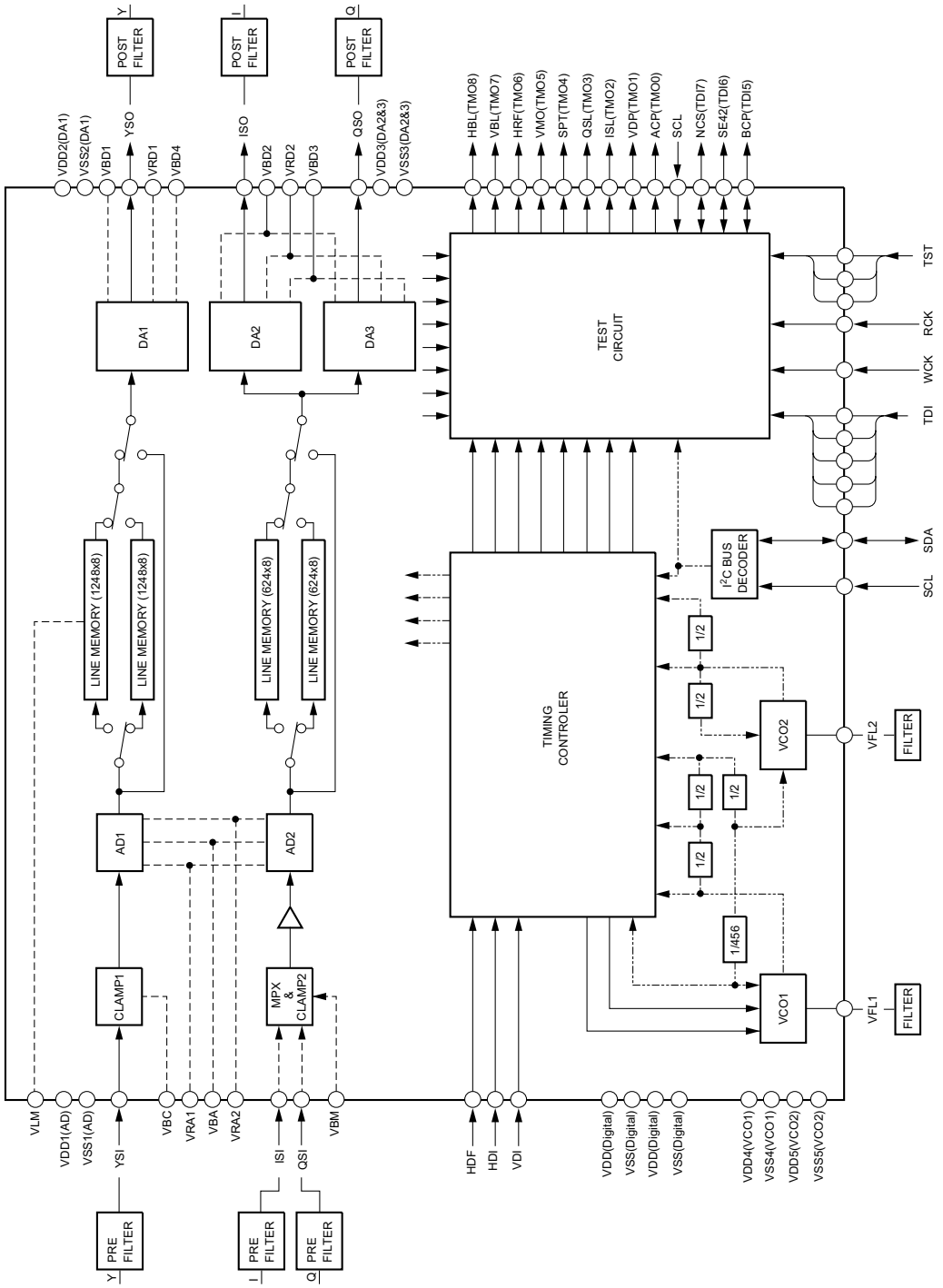
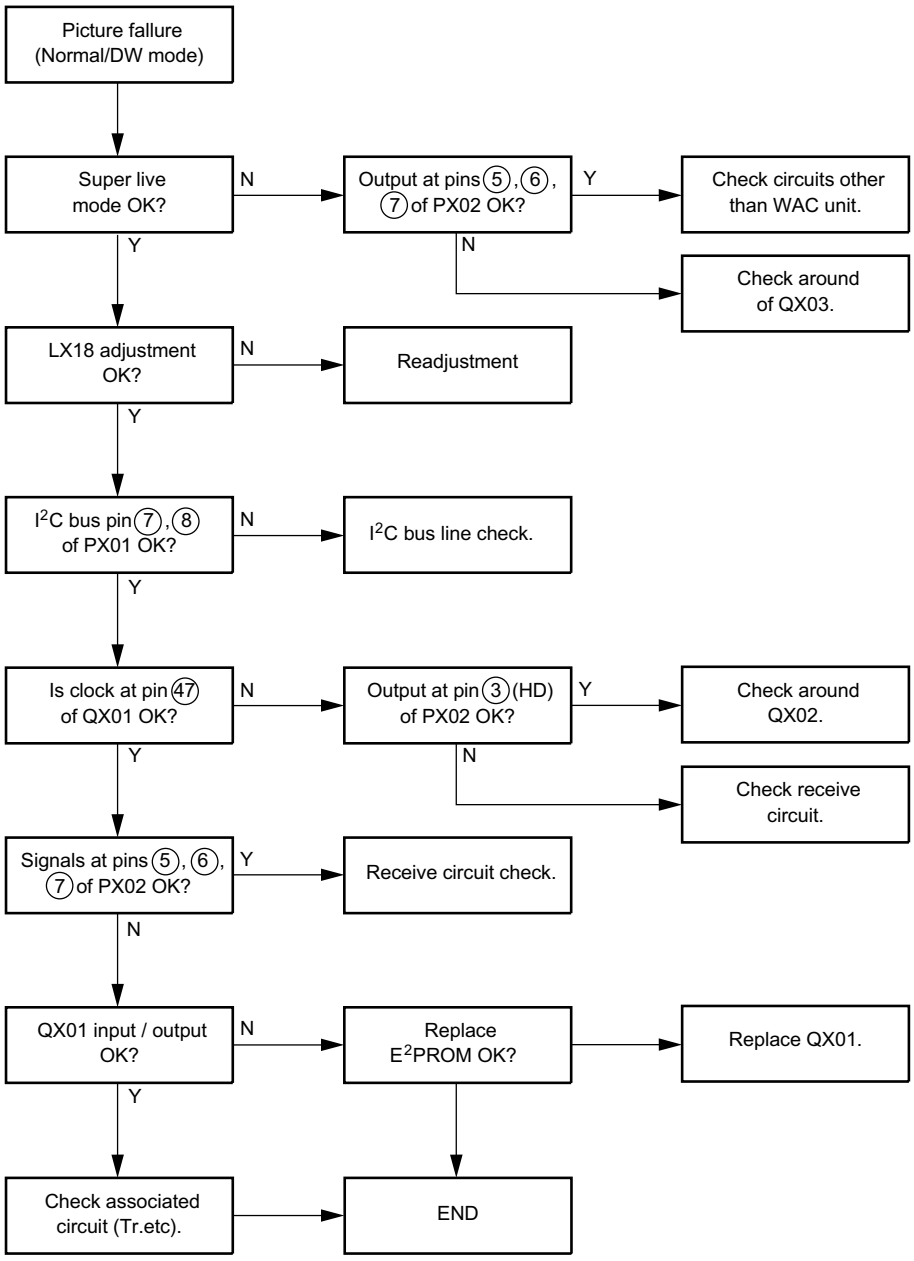


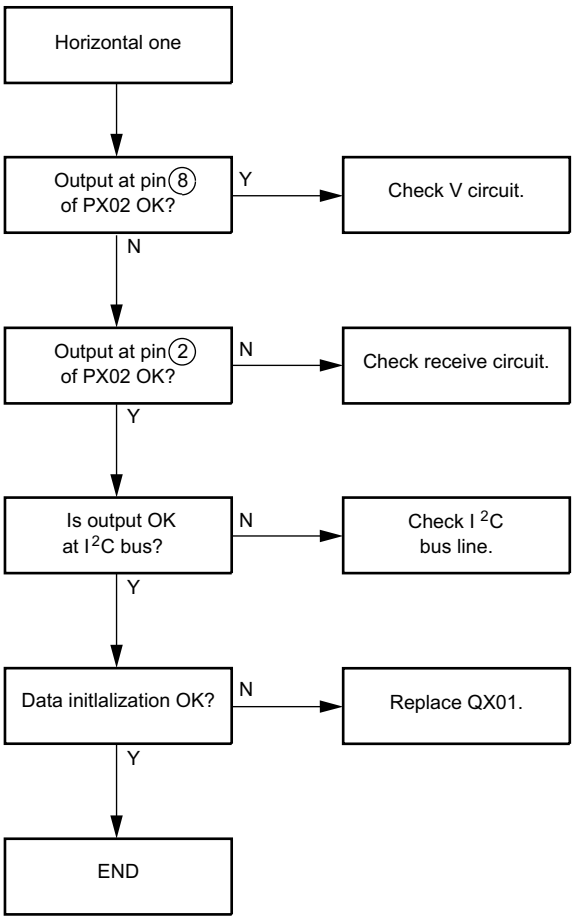
Fig. 5-3 TC9097F system block diagram

4. WIDE ASPECT CONVERSION CIRCUIT FAILURE ANALYSIS PROCEDURES

4-1. Left Screen Picture Failure in Normal Mode/Double Window Modes (No Picture, Sync Distributed)



4-2. Raster Horizontal One



4-2-1. Adjustment Method

(1) Disconnect any video inputs

(2) Open RX-40.

(3) Connect frequency counter to QX19 emitter.

(4) Adjust LX18 until frequency reading of “28.7 MHz ± 0.5 MHz” is obtained.

SECTION VI: DUAL CIRCUIT

1. OUTLINE

DUAL circuit performs the signal process, etc. on the sub screen and is composed of the followings as shown in Fig. 6-1.

- Video/color/deflection (V/C/D) process
- On-screen display (OSD) superimposing process
- Sub-screen process, memory
- Main/Sub screen picture superimposing process
- Sub screen control microprocessor

2. PRINCIPLES OF OPERATION

DUAL circuit is composed of the following functions.

(1) Double window sub screen 1/2 compression process

(2) Sub screen still process

(3) 9-screen multi-search process

(4) Main/Sub screen superimposing process by YIQ signal.

- **9-screen multi-search process**

The sub screen process IC (TC9092AF) is the IC using the programmable technology and can realize various functions such as sub screen 1/2 compression, 9-screen multi-search, etc. by switching the program.

The 9-screen multi-search process is carried out by selecting the channel on the right half of the wide screen with 16:9 aspect ratio and the picture images received are projected on the 9 screens from the upper left screen in order.

The search is carried out by approx. every 2 seconds repeatedly. When the next picture image is searched, the picture image on the previous screen becomes a still picture. When the 9 screens are finished projecting (to the picture image on the right bottom screen), the search operation is carried out repeatedly from the upper left screen.)

3. SYSTEM COMPONENT DIAGRAM OF DUAL UNIT

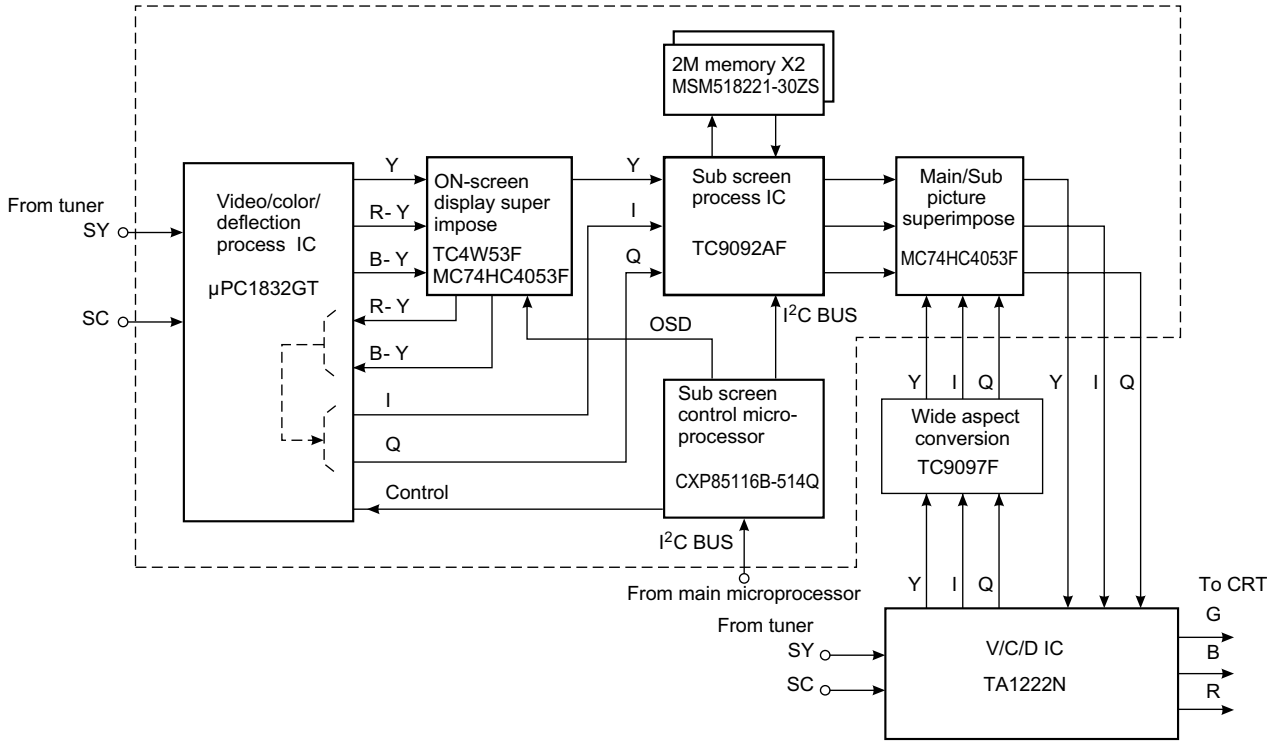


Fig. 6-1

4. CIRCUIT OPERATION

4-1. Video/Color/Deflection Process Section

The video/color/deflection section is shown in Fig. 6-2.

The luminance signal is supplied from pin Y08 of PY01 and its frequency bandwidth is limited by the low pass filter (LPF) and then input to pin 36 of V/C/D IC (VIDEO IN). The Y signal output from pin 12 of PY01 superimposes the character signal on the video signal by QY49 and QY44, and then output to the sub screen process section.

QY49 and QY44 work as the analog switches. When the screen is displayed in DW, the switch operation is not carried out and the same signal as the input signal is output, and when the 9-screen multi-search process is carried out, the switch operation is carried out.

The OSD signal superimposes the shade of character signal by QY49 and the character signal by QY44 on Y signal.

On the other hand, the color signal is supplied from pin Y15 of PY01, limited its frequency bandwidth by the band pass filter (BPF) and then input to pin 34 of QY01 (COLOR IN). The color difference signals of the demodulated signal (R – Y) and (B – Y) are output from pins 13 and 14 of QY01. In the same way as the Y signal, the (R – Y) and (B – Y) signals are superimposed on the character signal with OSD signal by QY44.

The GBR matrix circuit which converts the Y, R – Y and B – Y signals into three primary color signal of G, B and R is used to convert the (R – Y) and (B – Y) signals into I and Q signals.

In the GBR matrix circuit, each G, B and R output is output as G – Y, B – Y and R signals when the Y signal is not input. Then the B – Y signal is converted to Q signal, R – Y to I signal pseudically by turning the phase by an angle of 33°.

Thus, R – Y and B – Y signals are input to pins 18 and 19 of QY01, and the output signals from pins 23 and 24 are developed as the I and Q converted signals pseudically. The amplitude of the signals is amplified by 6 dB amplifier of QY23 and the signals are output to the sub screen process section.

Since the sync signal is added to the luminance signal, the signal is input to pin 39 of QY01 (SYNC SEP IN) and the sync signals of HD and VD are output to pins 10 and 11 of QY01. The HD signal is waveshaped by QY42.

The HD signal (WHD1, WHD2) is used as the horizontal pulse for sub screen write and the VD signal (WVD) is as the vertical pulse for sub screen write in the sub screen process section.

In the sub screen microcomputer section, various kinds of control signals (brightness, density, hue, etc.) are output from the sub screen control microprocessor QY91 and the signals are used for the level matching adjustment. So the setting for the sub screen cannot be made by the user. Furthermore, the OSD signal for OSD superimposing is output.

The sub screen process IC control program is stored in the nonvolatile memory of the sub screen control microprocessor QY91 in order to control the sub screen process IC (TC9092AF), and the data is sent via I^2C bus.

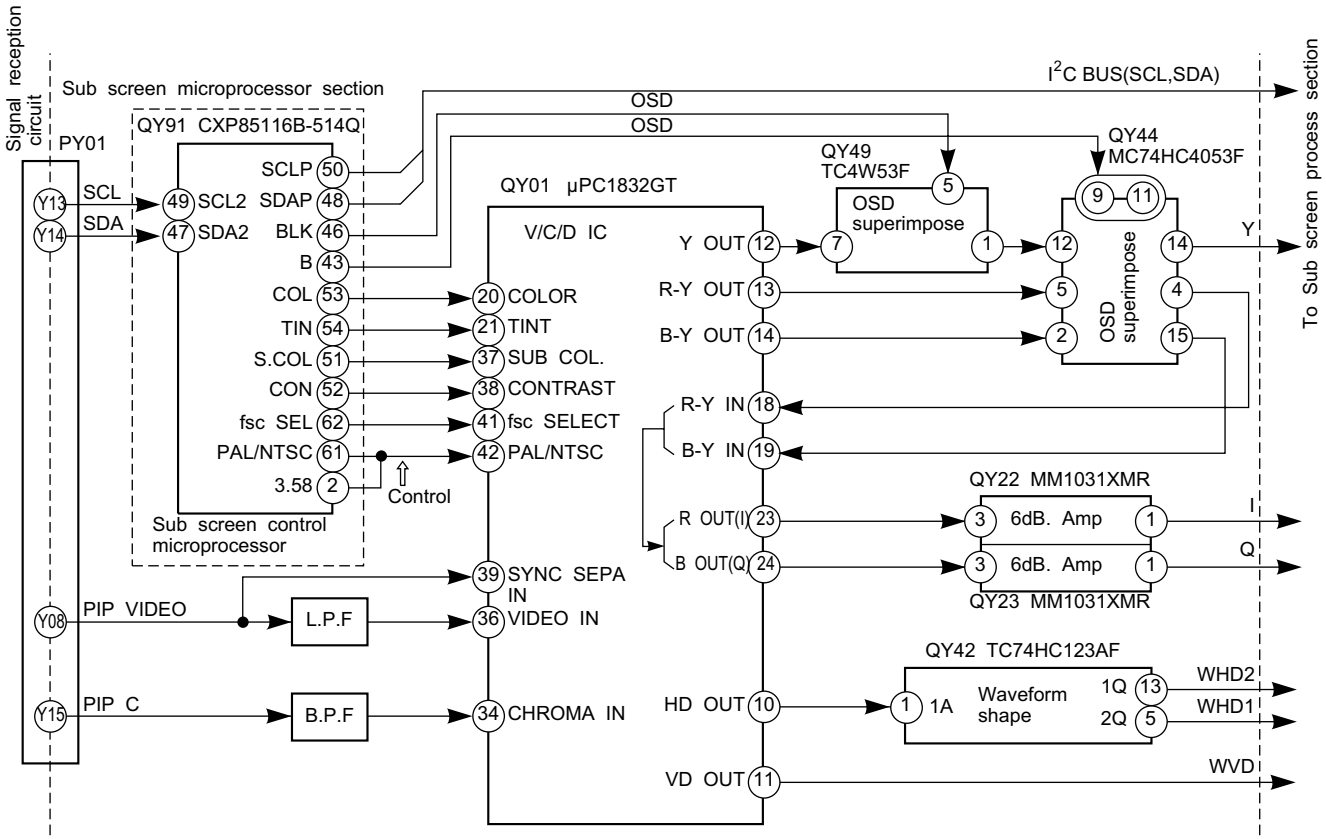


Fig. 6-2

4-2. Sub Screen Process Section

The sub screen process section is shown in Fig. 6-3.

The Y, I and Q signals from the video/color/deflection process section are limited in their frequency bandwidth by the LPF in the prceeding stage and input to pins 6, 13 and 15 of QY03.

The frequency of 18.5 MHz generated by LY102 is multiplied by 1/2 inside QY03. The Y signal is sampled by 9.25 MHz and the I and Q signals are sampled by 4.63 MHz (1/2 frequency to multiplex) and then the signals are converted into 8-bit digital signals.

The horizontal sync signal WHD (the signal mixed with WHD1 and WHD2 by QY43) for writing input to pins 21 and 20 of QY03 and the vertical sync signal WVD for trigger writing on the field memory QY10 and QY11.

The horizontal sync signal RHD for reading-out and the vertical sync signal RVD for reading out input to pins 75 and 77 of QY03 trigger the reading at 18.0 MHz which is created by 2/3-multiplying 27.0 MHz developed in LY101and then output as the analog signal.

The Y, I and Q signals converted for the sub screen are output from pins 95, 100 and 97 of QY03. The output signals are used for the input signals compressed by 1/2 in the horizontal direction in the double window mode and for the input signal compressed by 1/6 in the horizontal direction and by 1/3 in the vertical direction in 9-screen multi-search mode.

Then the signals are smoothed by the LPF in the next stage then input to the main/sub screen superimposing section.

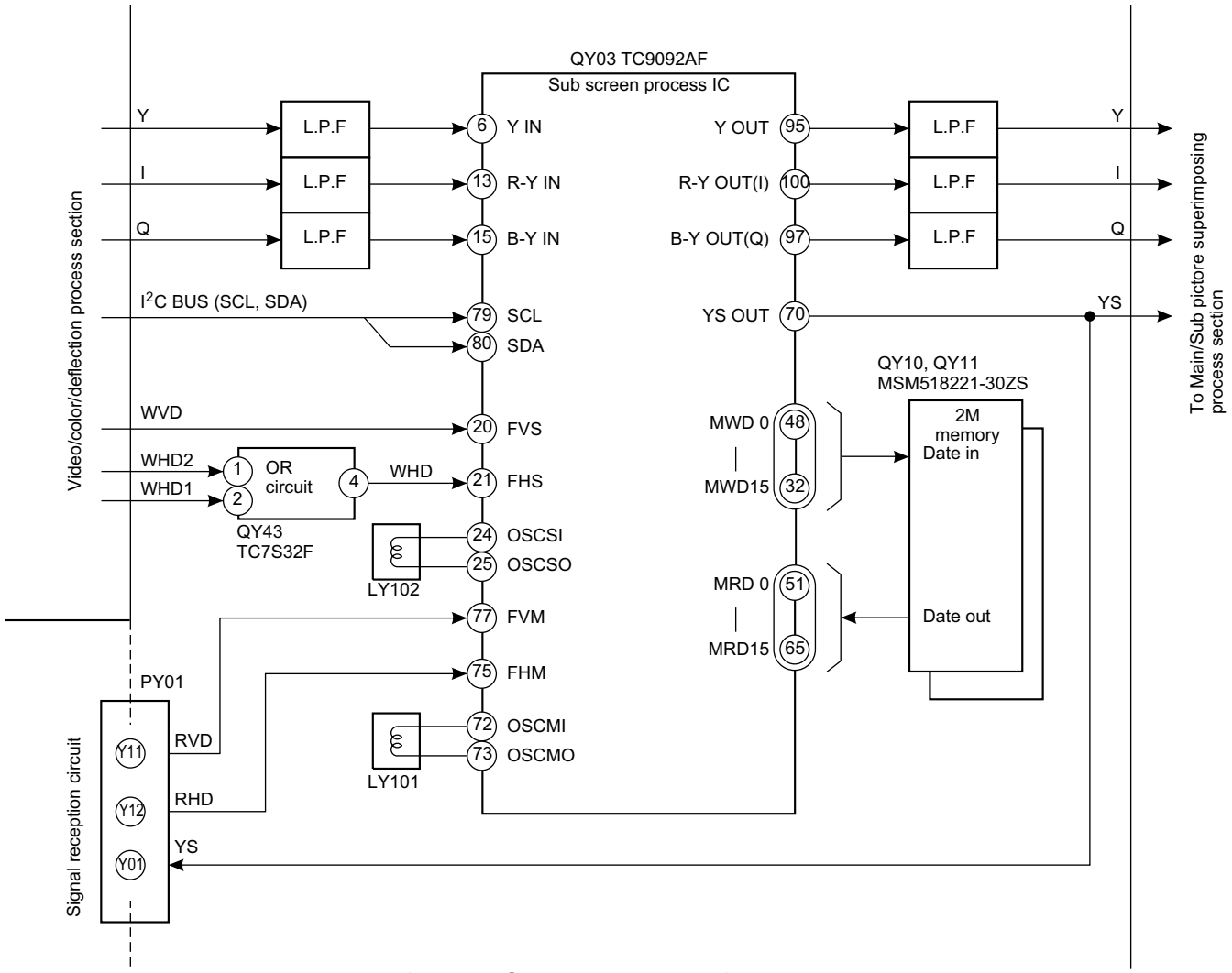


Fig. 6-3 Sub screen process section

4-3. Main/Sub Screen Superimposing Section

The main/sub screen superimposing section is shown in Fig. 6-4.

The sub screen Y, I and Q signals sent from the sub screen process section and the main screen Y, I and Q signals sent from the digital unit through the receive circuit and etnered pins 3, 2, and 1 of PY02 are clamped at a same electrical potential and the former are fed to pins 1, 3, 13 and the latter fed to pins 2, 5 and 12 of QY48.

The clamp circuit contains a clamp pulse waveshaping SCP at pin 4 of PY02, analog switches for ever-voltage source E, QY46 and QY47 and clamp capacitors CY230 ~ CY232, CY238 ~ CY240.

QY48 is an analog switch to feed the Y, I and Q signals for either sub screen or main screen to pins 15, 4 and 14 by the YS signal voltage fed to pins 9, 10 and 11. When the YS signal develops high, QY48 selects the signals for the sub screen and when low, QY48 selects the signals for the main screen. Consequently, the signals for both the main and sub screens are superimposed each other.

In normal mode (with only the main screen picture displayed), the YS signal voltage always goes low and the Y, I and Q signals from the digital unit are developed at pins 15, 4 and 14 of QY48.

The Y, I and Q signals for the main/sub screens superimposed are developed at pins Y05, Y06 and Y04 of PY01 and then supplied to the receive circuit.

The Y, I and Q signals for the main/sub screens superimposed inside the receive circuit are entered to pins 53, 51 and 52 of Q501 (TA1222N) and then fed to CRT. The video signal is processed in Q501 without distinguishing the signals for main and sub screens, so the high picture quality can be obtained equally for both the screens.

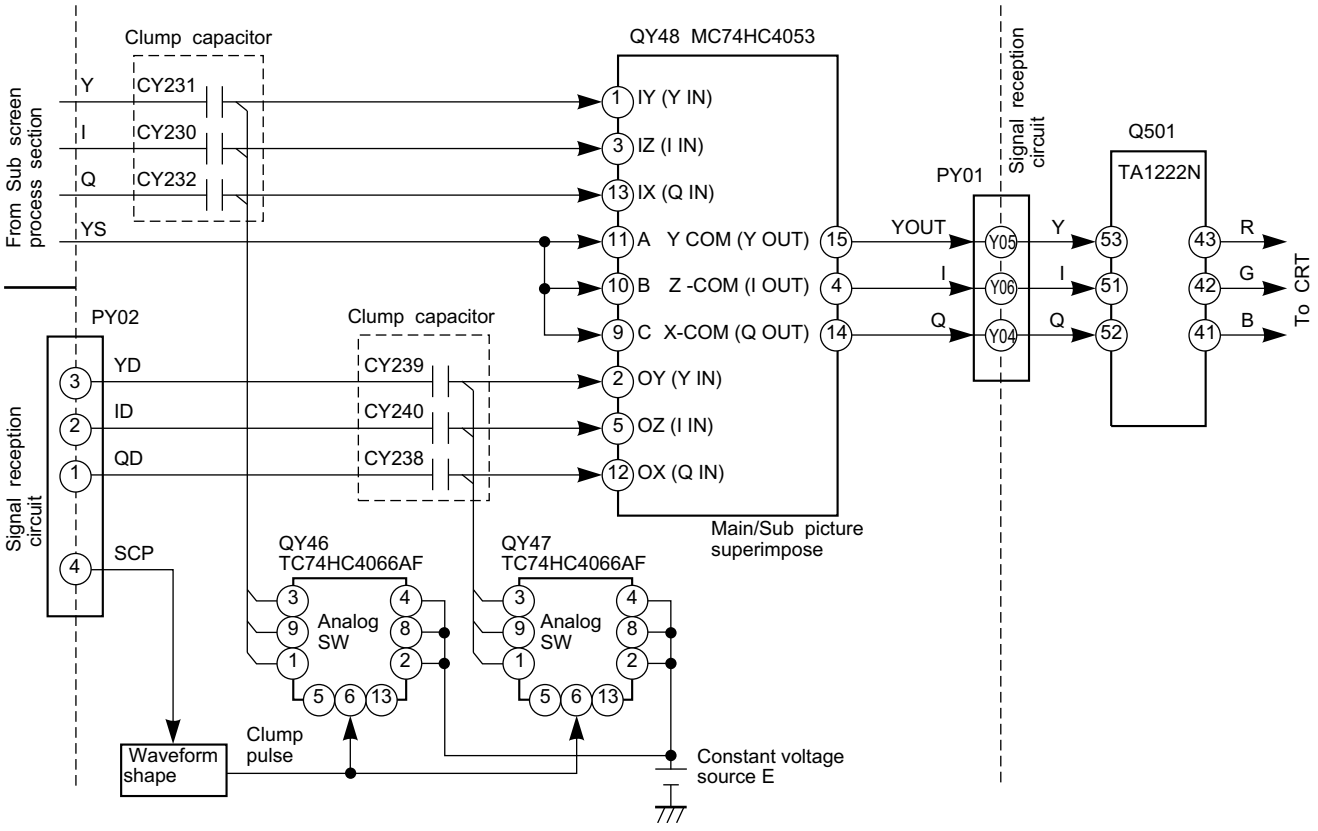


Fig. 6-4 Main/Sub screen superimposing section

5. TERMINAL FUNCTION, DESCRIPTION AND BLOCK DIAGRAM OF MAIN IC

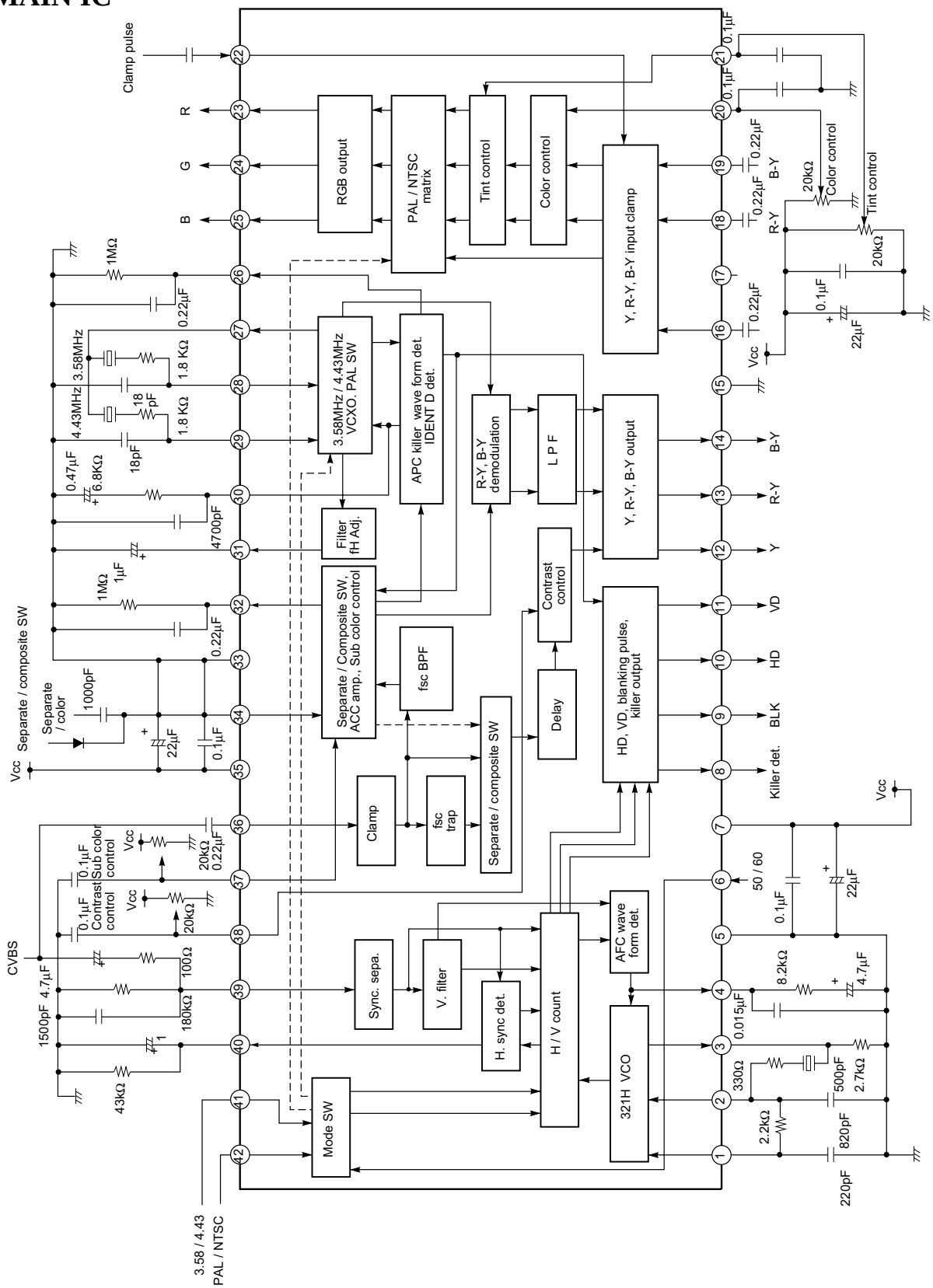


Fig. 6-5 QY01 μPC1832GT internal block diagram

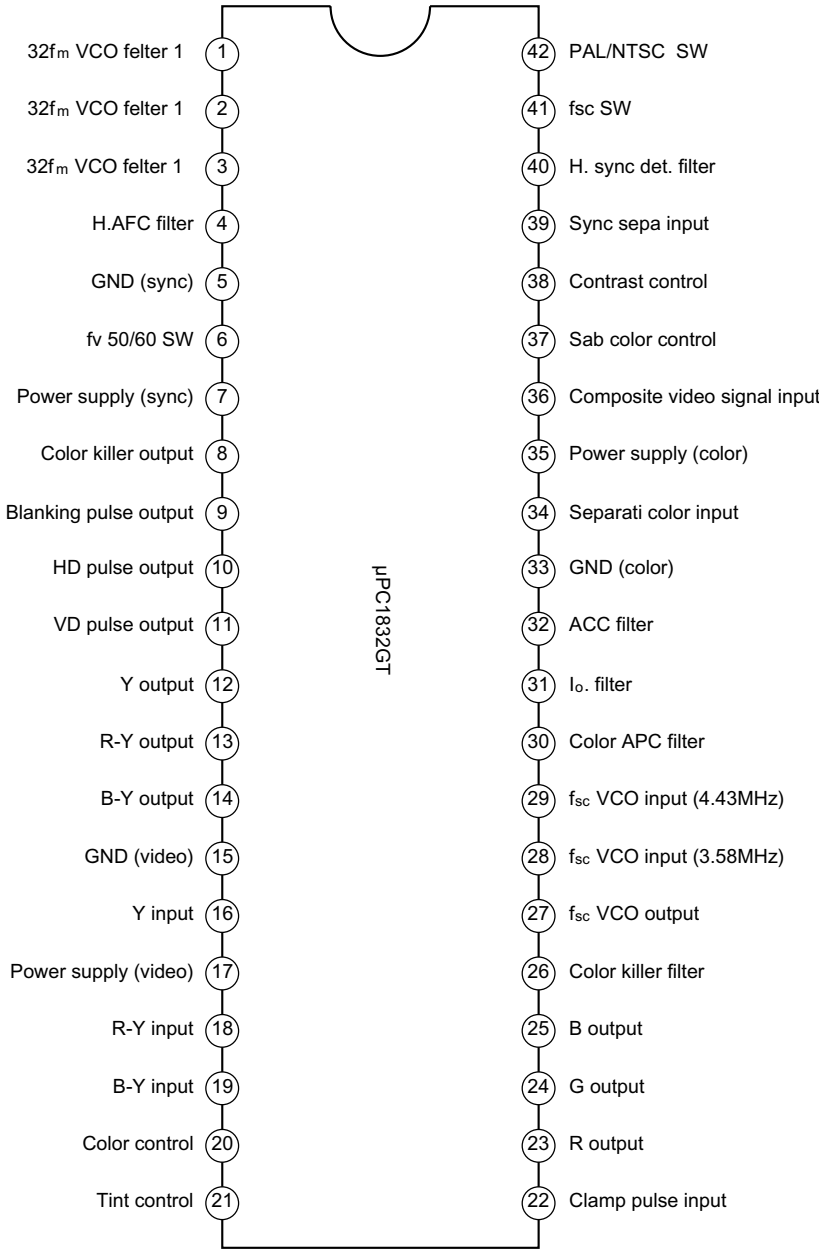


Fig. 6-6 QY01 μPC1832GT pin layout

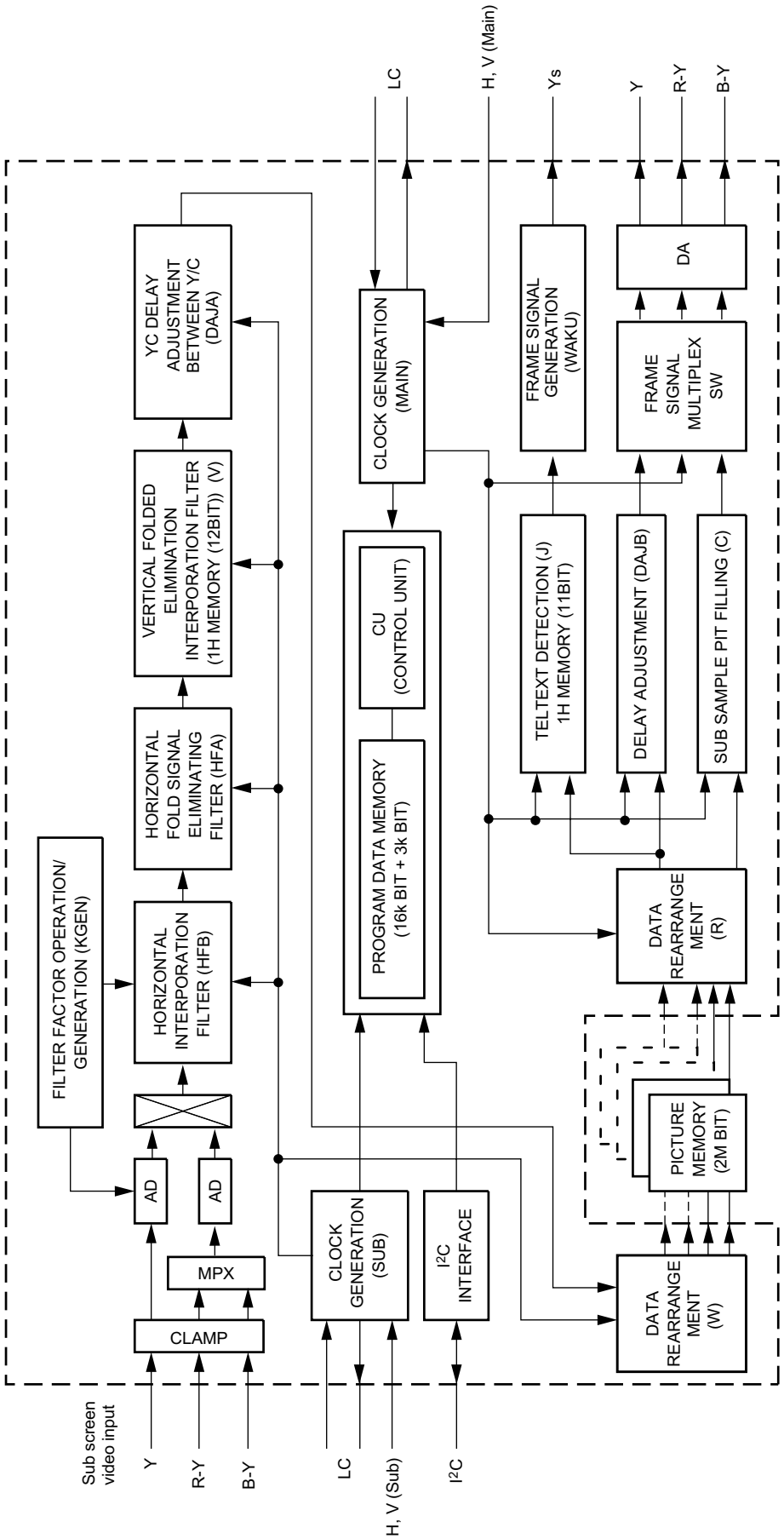


Fig. 6-7 QY03 TC9092AF internal block diagram

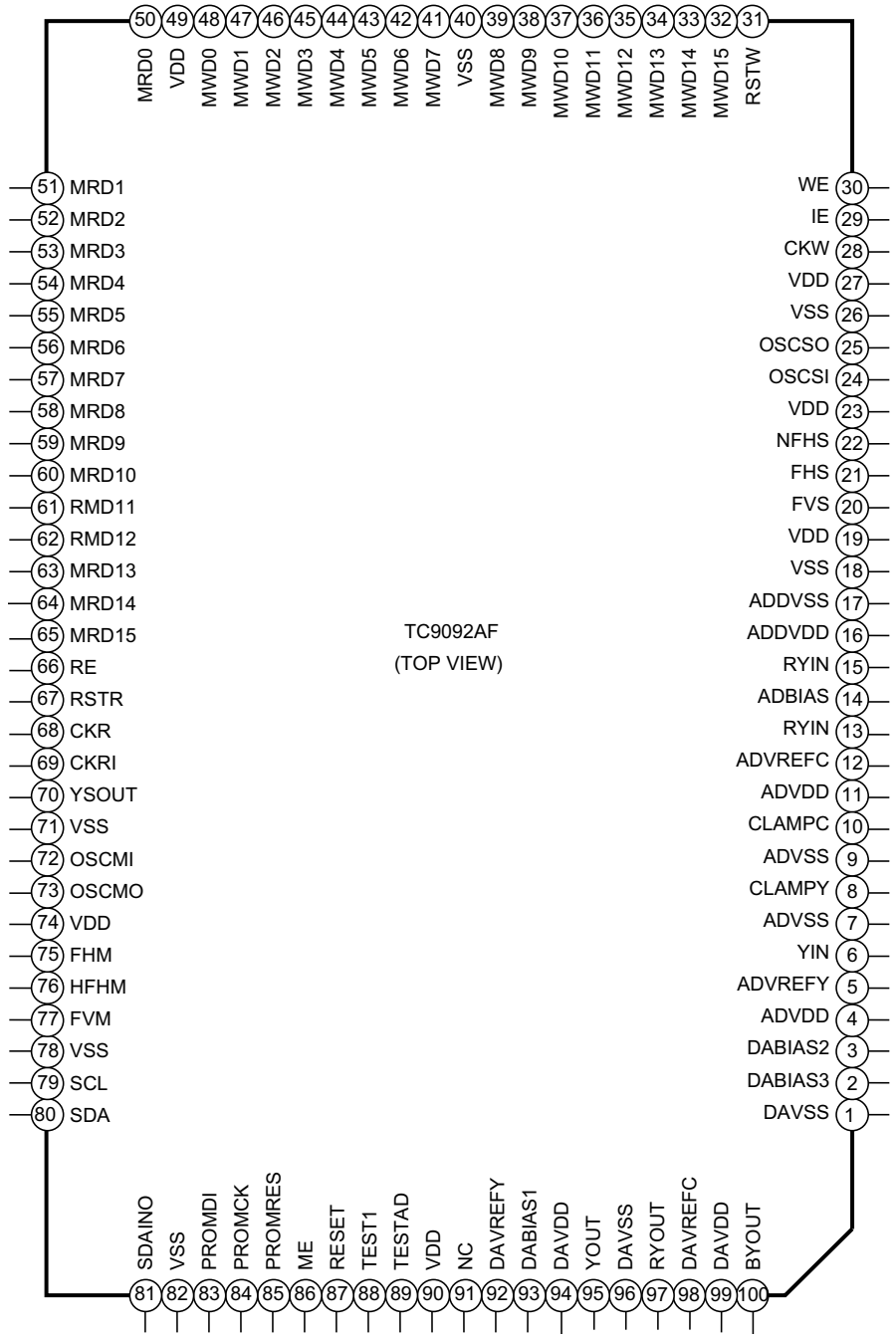


Fig. 6-8 QY03 TC9092AF pin layout

Table 6-1 QY03 TC9092AF pin list (No. 1)

No.	Pin name	I/O	Pin function
1	DAVSS		D/A GND
2	DABIAS3		D/A bias condenser connection terminal
3	DABIAS2		D/A bias condenser connection terminal
4	ADVDD		A/D power supply
5	ADVREFY	I	A/D Y reference condenser connection terminal
6	YIN	I	A/D Y input terminal
7	ADVSS		A/D GND
8	CLAMPY		Y clamp bias condenser connection terminal
9	ADVSS		A/D GND
10	CLAMPY		C clamp bias condenser connection terminal
11	ADVDD		A/D power supply
12	ADVREFC	I	A/D reference condenser connection terminal
13	RYIN	I	A/D R – Y input terminal
14	ADBIAS		A/D bias condenser connection terminal
15	BYIN	I	A/D B– Y input terminal
16	ADDVDD		A/D digital power supply
17	ADDVSS		A/D digital GND
18	VSS		Digital GND
19	VDD		Digital power supply
20	FVS	I	Sub screen vertical sync signal input
21	FHS	I	Sub screen horizontal sync signal input
22	NFHS	I	Sub screen horizontal sync signal reversing input
23	VDD		Digital power supply
24	OSCSI	I	Oscillator connection terminal sub input
25	OSCSO	O	Oscillator connection terminal sub output
26	VSS		Digital GND
27	VDD		Digital power supply
28	CKW	O	Serial write clock output terminal
29	IE	O	Input enable output terminal
30	WE	O	Write enable output terminal
31	RSTW	O	Reset write output terminal
32	MWD15	O	Data output terminal
33	MWD14	O	Data output terminal
34	MWD13	O	Data output terminal
35	MWD12	O	Data output terminal
36	MWD11	O	Data output terminal
37	MWD10	O	Data output terminal
38	MWD9	O	Data output terminal
39	MWD8	O	Data output terminal
40	VSS		Digital GND
41	MWD7	O	Data output terminal
42	MWD6	O	Data output terminal
43	MWD5	O	Data output terminal
44	MWD4	O	Data output terminal
45	MWD3	O	Data output terminal
46	MWD2	O	Data output terminal
47	MWD1	O	Data output terminal
48	MWD0	O	Data output terminal
49	VDD		Digital power supply
50	MRD0	I	Data input terminal

Table 6-2 QY03 TC9092AF pin list (No. 2)

No.	Pin name	I/O	Pin function
51	MRD1	I	Data input terminal
52	MRD2	I	Data input terminal
53	MRD3	I	Data input terminal
54	MRD4	I	Data input terminal
55	MRD5	I	Data input terminal
56	MRD6	I	Data input terminal
57	MRD7	I	Data input terminal
58	MRD8	I	Data input terminal
59	MRD9	I	Data input terminal
60	MRD10	I	Data input terminal
61	MRD11	I	Data input terminal
62	MRD12	I	Data input terminal
63	MRD13	I	Data input terminal
64	MRD14	I	Data input terminal
65	MRD15	I	Data input terminal
66	RE	O	Read enable output terminal
67	RSTR	O	Read reset output terminal
68	CKR	O	Serial read clock output terminal
69	CKRI	I	Memory read clock input
70	YSOUT	O	Ys signal output terminal
71	VSS		Digital GND
72	OSCMI	I	Oscillator connection terminal main input
73	OSCMO	O	Oscillator connection terminal main output
74	VDD		Digital power supply
75	FHM	I	Main screen horizontal sync signal input
76	NFHM	I	Main screen horizontal sync signal reversing input
77	FVM	I	Main screen vertical sync signal input
78	VSS		Digital GND
79	SCL	I	I^2C CK input terminal
80	SDA	BID	I^2C data I/O terminal
81	SDAINO	O	I^2C data direction output terminal, Test output terminal
82	VSS		Digital GND
83	PROMDI	I	ROM data input terminal
84	PROMCK	O	ROM clock output terminal
85	PROMRES	O	ROM RESET output terminal
86	ME	I	MEMORY polarity control input terminal
87	RESET	I	RESET input terminal
88	TEST1	I	TEST input terminal
89	TESTAD	I	AD/DA TEST input terminal
90	VDD		Digital power supply
91	NC		
92	DAVREFY	I	D/A Y reference voltage input terminal (4V)
93	DABIAS1		D/A bias condenser connection terminal
94	DAVDD		D/A power supply
95	YOUT	O	D/A Y output terminal
96	DAVSS		D/A GND
97	RYOUT	O	D/A R – Y output terminal
98	DAVREFC	I	D/A C reference voltage input terminal (3V)
99	DAVDD		D/A power supply
100	BYOUT	O	D/A B – Y output terminal

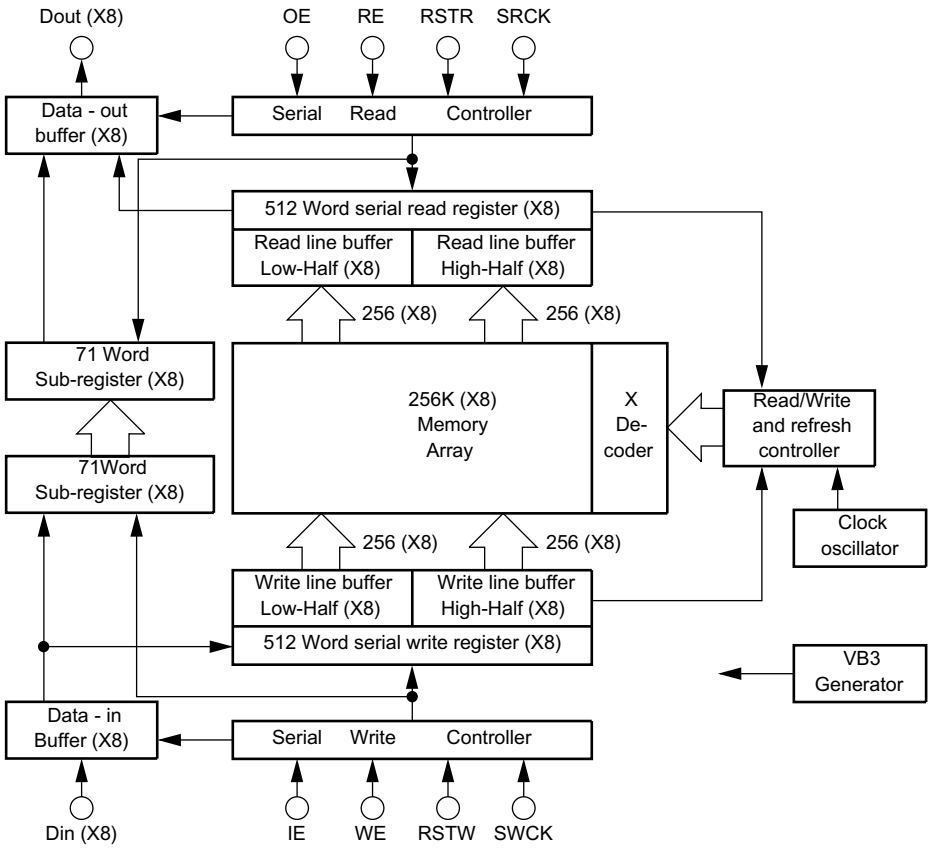
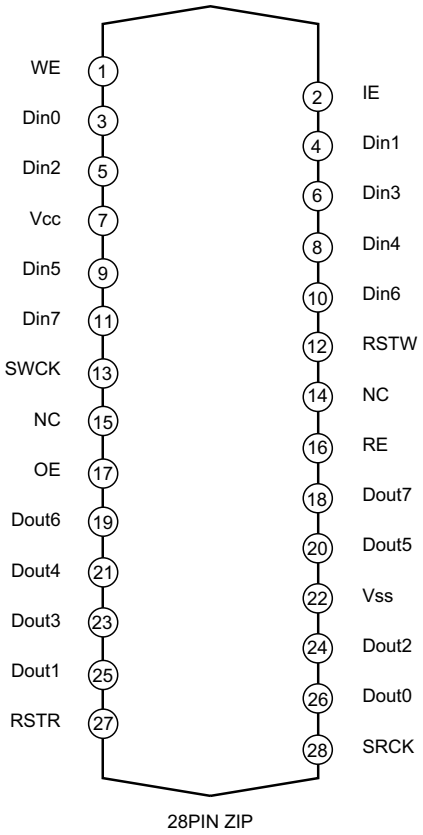


Fig. 6-9 QY10/QY11 M518221-30ZS internal block diagram



Terminal name	Function
SWCK	Serial write clock
SRCK	Serial read clock
WE	Write enable
RE	Read enable
IE	Input enable
OE	Output enable
RSTW	Reset write
RSTR	Reset read
Din 0 – 7	Data input
Dout 0 – 7	Data output
V_{CC}	Power supply (+5V)
V_{SS}	Ground (0V)
NC	Not connected

Fig. 6-10 QY10/QY11 M518221-30ZS pin layout

SECTION VII: 3-DIMENSION Y/C SEPARATOR CIRCUIT

1. OUTLINE

The 3D YC separation circuit uses a comb filter with a frame memory and ideally separates the Y (luminance) and color signal for still parts of a picture, thus providing a clean picture without:

(1) Dot interference causing at border areas of color pictures.

(2) Excess color in vertical direction.

However in a moving picture, as the picture moves between the first and second frames, good separation is not obtained.

To prevent this, a motion detection is carried out in the 3D YC separation (hereafter called YCS) unit (PB6347). When a picture moving is detected a 2D YC separation using a line memory is switched in and when not detected or for a still picture 3D YC separation is switched in, thereby correcting defects both the systems have and performing the ideal YC separation. The motion detection accuracy and smoothness of the switching, etc. are controlled through the IIC bus.

After completion of the Y and S signal separation, a vertical contour correction is carried out for the Y signal.

2. CIRCUIT DESCRIPTION

2-1. Configuration

The YCS unit consists of a YC separation IC (QZ01, TC9086F) which plays major roles, 2 Mbyte field memory (QZ02, QZ03), clock generation IC (QZ04, TA8667F), and peripheral circuits (LPF, AMP,emitter followers, etc.).

Of the above circuit blocks, QZ01 (TC9086F) includes an A/D converter, D/A converter, clamp circuit, 4fsc PLL circuit, 1 line dot countermeasure circuit, vertical contour correction logic circuit, etc. and provides a high separation with less variations.

2-2. Circuit Description

Fig. 7-1 shows a block diagram of the YCS circuit.

(1) A video signal sent through the AV switching circuit passes the input terminal (DG) and enters the YCS unit.

(2) The video signal entered is limited in its band width in passing through an aliasing distortion elimination LPF consisting of LZ22, etc. , and then enters pin 56 of QZ01.

(3) At the same time, a fsc (3.58 MHz) signal being oscillated in the video signal color IC (Q501, AN1222AN) is fed to pin 28 of QZ01 and converted into a 4fsc (14.32 MHz), a drive clock frequency inside the IC.

(4) The video signal entered pin 56 of QZ01 is processed inside the IC and a luminance (Y) signal is developed at pin 48 of QZ01 and the color signal at the pin 51.

(5) The Y signal developed at pin 48 of QZ01 passes a LPF (LZ20, etc.) which eliminates the clock signal component, amplified by a 6dB amplifier QZ21, etc. and comes out from the DC terminal as the Y signal.

(6) At the same time, the color signal developed at pin 51 of QZ01 passes a LPF (LZ21, etc.) which eliminates the clock component, amplified by 6dB by QZ23, etc. and comes out from DD terminal through a buffer of QZ24 as the C signal.

(7) QZ04 is generating a clock signal used to read and write the digital data between QZ03 and QZ04 based on the video signal.

(QZ16 emitter: 28.6 MHz ± 0.2 MHz, adjusted by LZ25.)

- **Terminal description (PZ01)**

No.	Signal name	Voltage
DH	Comb through	Comb through pulse for ED2 ID signal period (V frequency), 5V
DC	Y-Comb	2V(p-p)
DE	9V	+9V ± 0.5V
DD	C-Comb	0.6V(p-p) at burst
DB	GND	GND
DG	V-AV	2V(p-p)
DA	5V	+5V ± 0.5V
DF	fsc	0.4V(p-p), 3.58 MHz
DI	SDA1	IIC bus data, 5V
DJ	SCL1	IIC bus clock, 5V

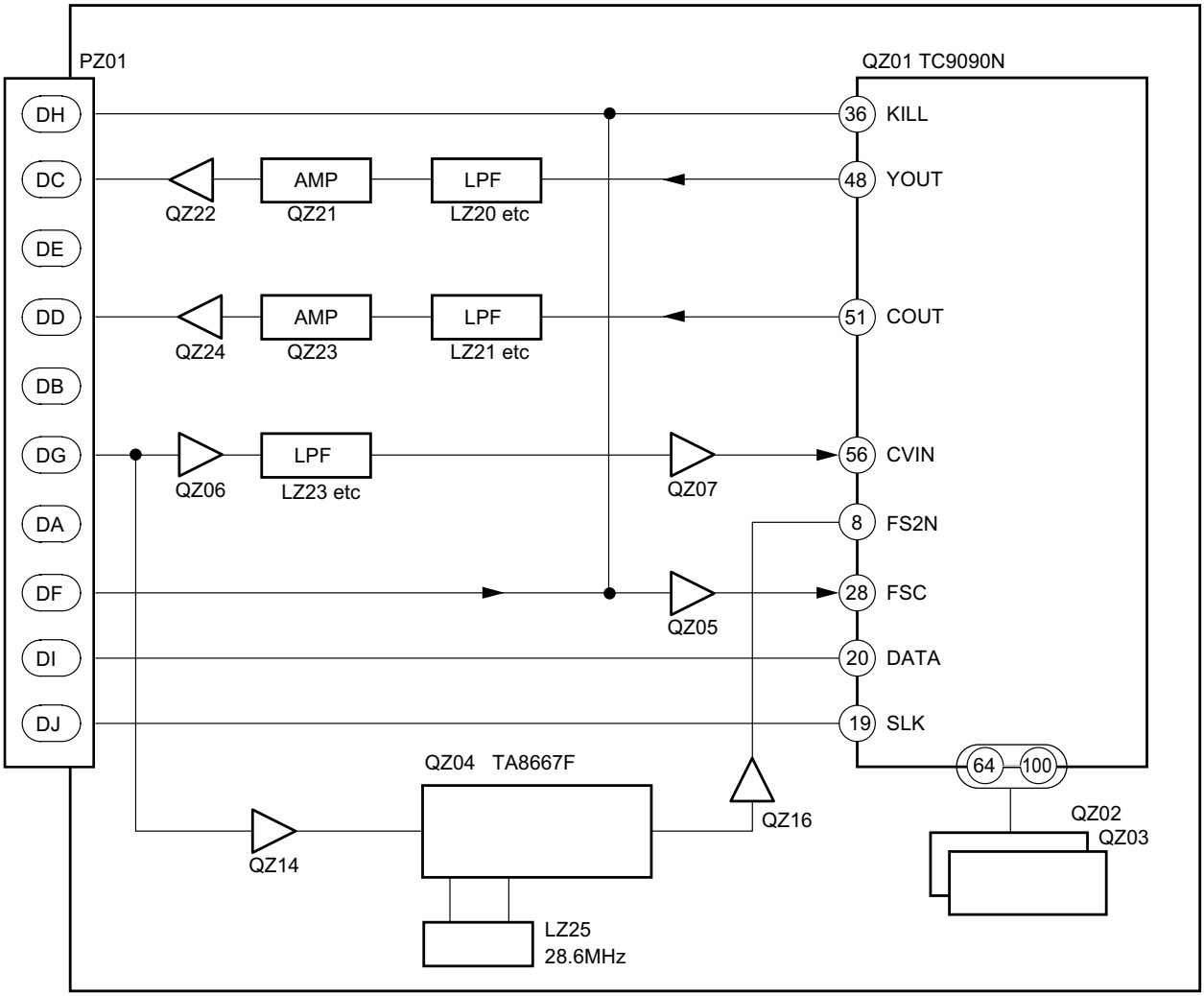


Fig. 7-1 3-dimension Y/C separator unit block diagram

SECTION VIII: VERTICAL OUTPUT CIRCUIT

1. OUTLINE

The sync separation circuit, V pulse circuit, and blanking circuit are provided inside Q501 (TA1222AN). The saw tooth wave generation circuit and amplifier (V driver circuit) are provided inside Q302 (TA8859AP).

Q301 (LA7833S) contains the pump up circuit and the output circuit. V screen position switching function which lowers the V raster position by flowing an opposite DC current into the deflection yoke. This circuit is used selecting SUBTITLE and CINEMA MODE.

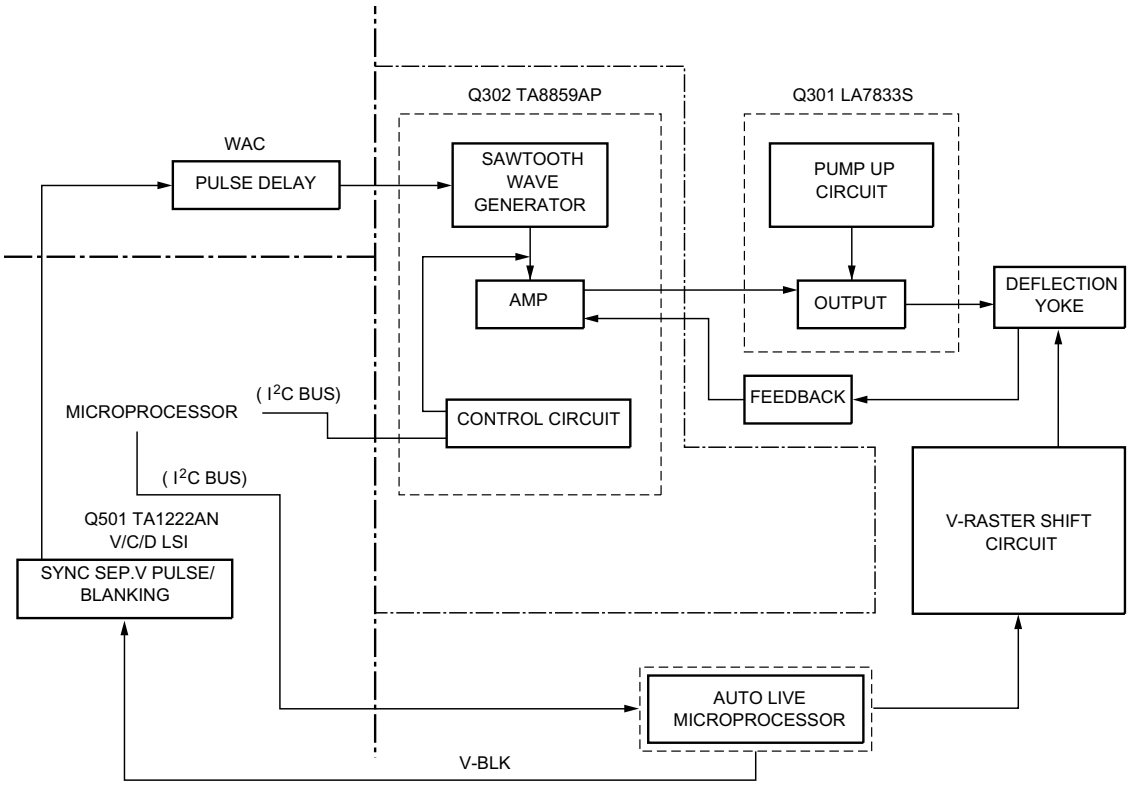


Fig. 8-1

1-1. Theory of Operation

The purpose of the V output circuit is to provide a sawtooth wave signal with good linearity in V period to the deflection yoke.

When a switch S is opened, an electric charge charged up to a reference voltage VP discharges in an constant current rate, and a reference sawtooth voltage generates at point ⓐ.

This voltage is applied to (+) input (non-inverted input) of an differential amplifier, A. As the amplification factor of A is sufficiently high, ⓐ deflection current flows so that the voltage V2 at point ⓒ becomes equal to the voltage at point ⓐ.

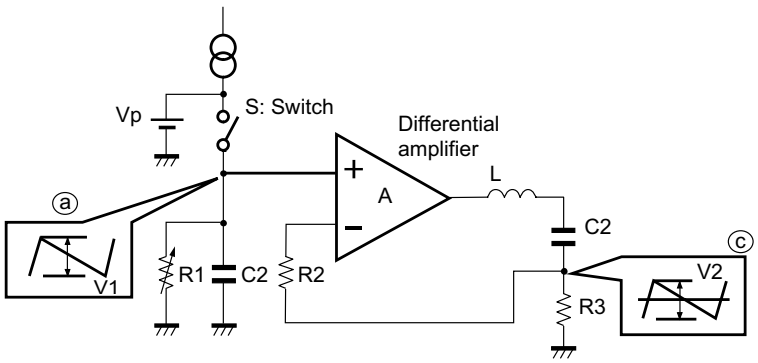


Fig. 8-2

2. V OUTPUT CIRCUIT

2-1. Actual Circuit

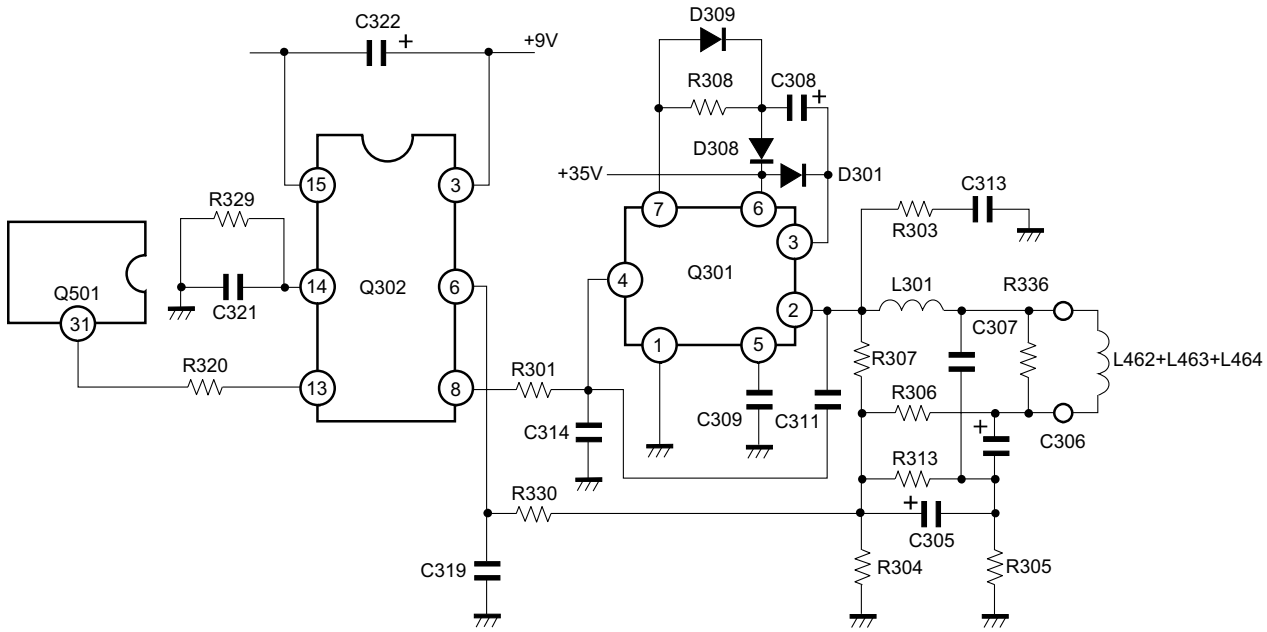


Fig. 8-3

2-2. Sawtooth Waveform Generation

2-2-1. Circuit Operation

The sawtooth waveform generation circuit consists of as shown in Fig. 8-4. When a trigger pulse enters pin 13, it is differentiated in the waveform shape circuit and only the falling part is detected by the trigger detection circuit, to the waveform generation circuit is not susceptible to variations of input pulse width.

The pulse generation circuit also works to fix the V ramp voltage at a reference voltage when the trigger pulse enters, so it can prevent the sawtooth wave start voltage from variations by horizontal components, thus improving interlacing characteristics.

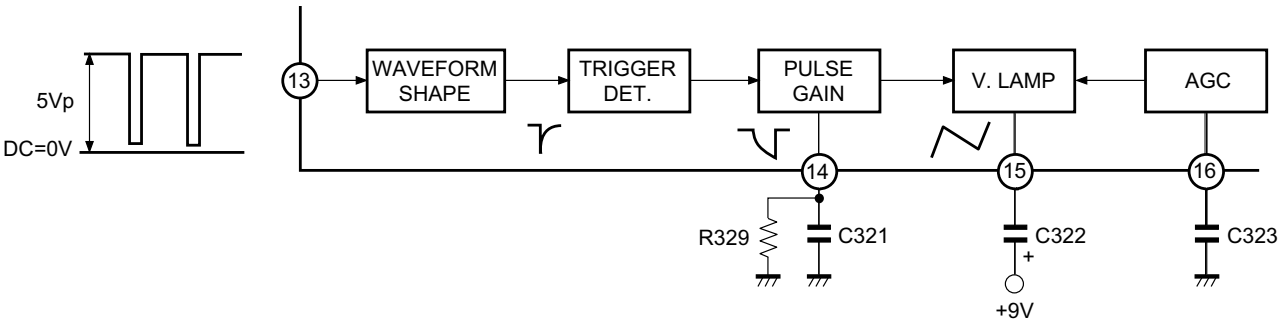


Fig. 8-4

2-3. V Output

2-3-1. Circuit Operation

The V output circuit consists of a V driver circuit Q302, Pump-up circuit and output circuit Q301, and external circuit components.

(1) Q2 amplifies its input fed from pin 4 of Q301, Q3, Q4 output stage connected in a SEPP amplifies the current and supplies a sawtooth waveform current to a deflection yoke.

Q3 turns on for first half of the scanning period and allows a positive current to flow into the deflection yoke (Q3 ® DY ® C306 ® R305 ® GND), and Q4 turns on for last half of the scanning period and allows a negative current to flow into the deflection yoke (R305 ® C306 ® DY ® Q4). These operations are shown in Fig. 8-5.

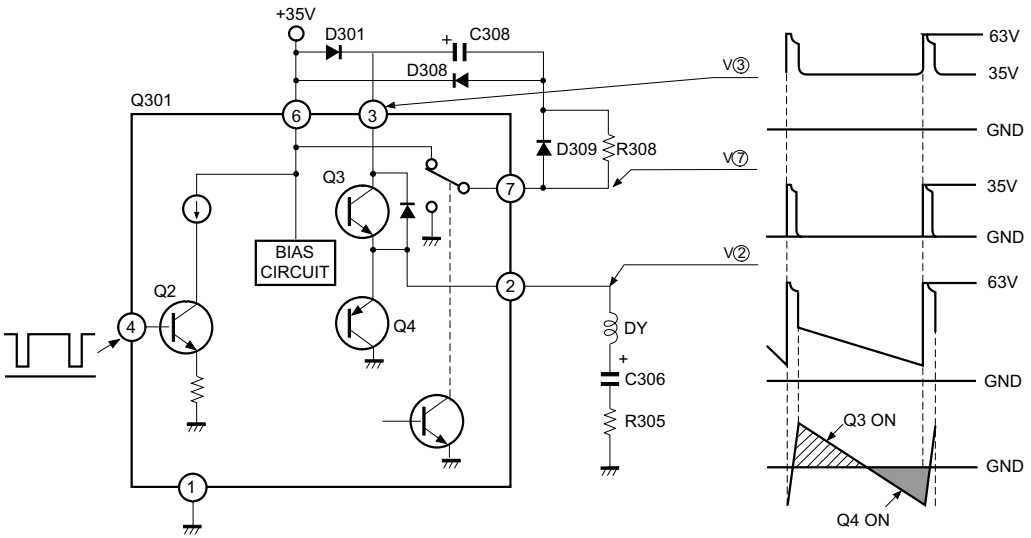


Fig. 8-5

(2) In Fig. 8-6 (a), the power Vcc is expressed as a fixed level, and the positive and negative current flowing into the deflection yoke is a current (d) = current (b) + (c) in Fig. 8-6, and the emitter voltage of Q3 and Q4 is expressed as (e).

(3) Q3 collector loss is i1 x Vce1 and the value is equal to multiplication of Fig. 8-6 (b) and slanted section of Fig. 8-6 (e), and Q4 collector loss is equal to multiplication of Fig. 8-6 (c) and dotted section of Fig. 8-6 (e).

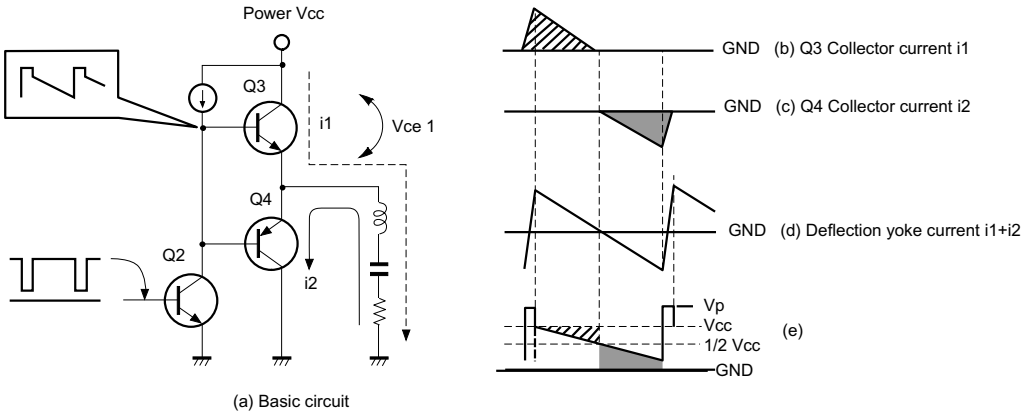


Fig. 8-6

(4) To decrease the collector loss of Q3, the power supply voltage is decreased during scanning period as shown in Fig. 8-7, and VCE1 decreases and the collector loss of Q3 also decreases.

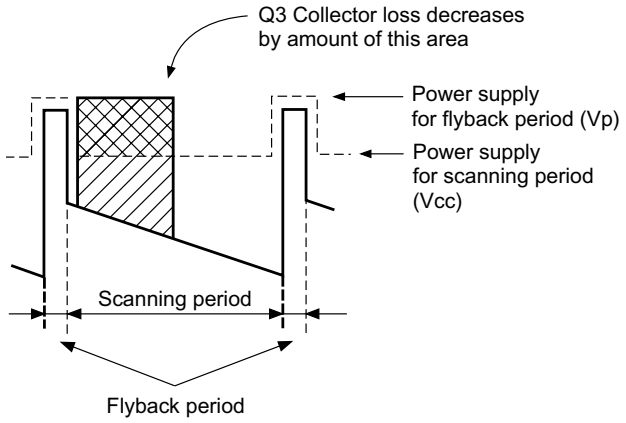


Fig. 8-7 Output stage power supply voltage

(5) In this way, the circuit which switches power supply circuit during scanning period and flyback period is called a pump-up circuit. The purpose of the pump-up circuit is to return the deflection yoke current rapidly for a short period (within the flyback period) by applying a high voltage for the flyback period. The basic operation is shown in Fig. 8-8.

(6) Since pin 7 of a transistor switch inside Q301 is connected to the ground for the scanning period, the power supply (pin 3) of the output stage shows a voltage of (VCC – VF), and C308 is charged up to a voltage of (VCC – VF – VR) for this period.

(7) First half of flyback period

Current flows into L462 + L465 + L464 ® D1 ® C308 ® D308 ® VCC (+35V) ® GND ® R305 ® C306 ® L462 + L463 + L464 in this order, and the voltage across these is:

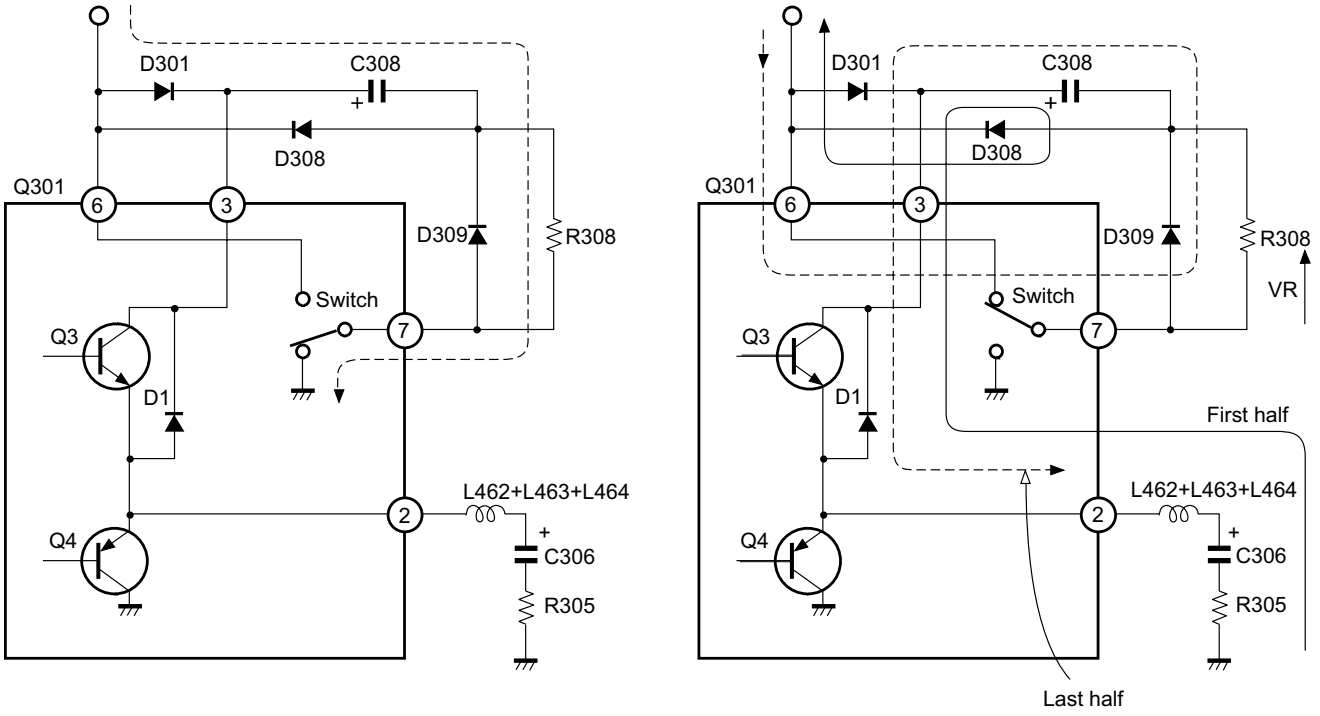
VP = VCC + VF + (VCC – VF – VR) + VF about 63V is applied to pin 3. In this case, D301 is cut off.

(8) Last half of flyback period

Current flows into VCC ® switch ® D309 ® C308 ® Q301 (pin 3) ® Q3 ® L462 + L463 + L464 ® C306 ® R305 in this order, and a voltage of

VP = VCC – VCE (sat) – VF + (VCC – VF – VR) – VCE (sat), about 56V is applied to pin 3.

(9) In this way, a power supply voltage of about 35V is applied to the output stage for the scanning period and about 63V for flyback period.



(a) Scanning period

(b) Flyback period

Fig. 8-8

2-4. V Linearity Characteristic Correction

2-4-1. S-character Correction (Up-and Down-ward Extension Correction)

A parabola component developed across C306 is integrated by R306 and C305, and the voltage is applied to pin 6 of Q302 to perform S-character correction.

2-4-2. Up-and Down-ward Linearity Balance

A voltage developed at pin 2 of Q301 is divided with resistors R307 and R303, and the voltage is applied to pin 6 of Q301 to improve the linearity balance characteristic.

3. PROTECTION CIRCUIT FOR V DEFLECTION STOP

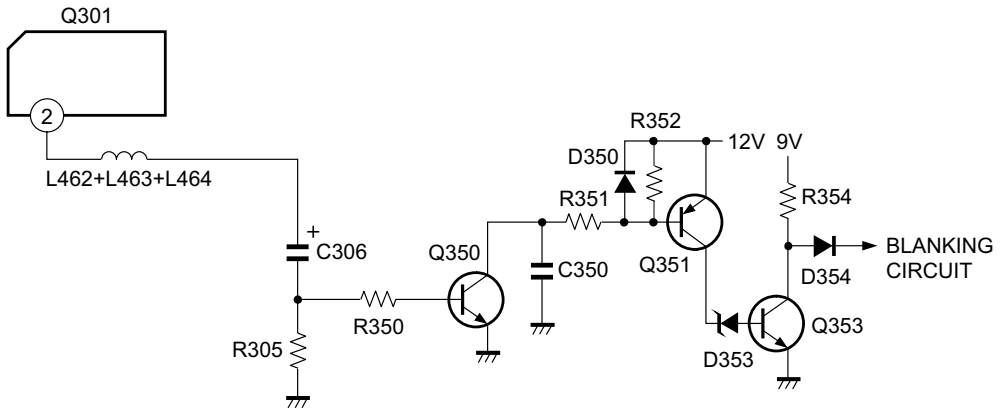


Fig. 8-9

When the deflection current is not supplied to the deflection coils, one horizontal line appears on the screen. If this condition is not continued for a long time, no trouble will occur in a conventional TV. But in the projection TV, all the electron beams are directly concentrated at the fluorescent screen because of no shadow mask used, and burns out the screen instantly.

To prevent this, the stop of the V deflection is detected when the horizontal one line occurs, and the video signals are blanked out so that the electron beams are not emitted.

When the V deflection circuit is operating normally, a sawtooth wave voltage is obtained across (R305), so Q350 repeats on-off operation in cycle of V sync. In this case, the collector voltage of Q35 is set to develop less than (12V-V_{BE} (Q351)) with R352 and C350 as shown in Fig. 8-9. Accordingly, Q351 and Q353 are continuously turned on. As a result, diode D354 is turned off, giving no influence on the blanking operation.

Next, when the V deflection stops, the voltage across (R305) does not develop, so Q350 turns off, and both the Q351 and Q353 are turned off. Then, the picture blanking terminal pin 13 of ICA05 is set to high through R354 and D354 connected to 90V power line, BLANKING CIRCUIT ON thus cutting off the projection tubes.

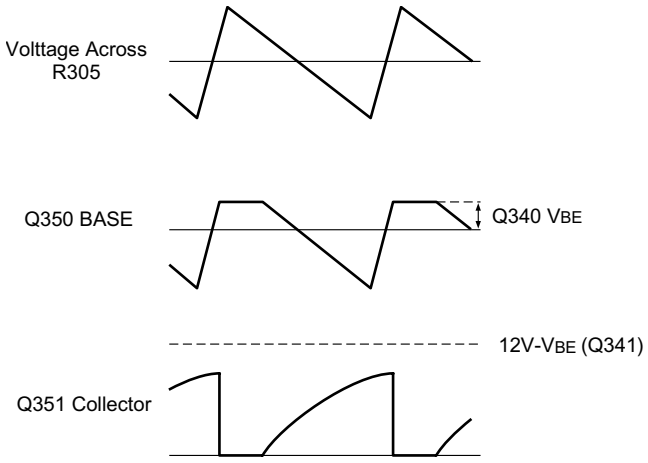


Fig. 8-10

3-1. +35V Over Current Protection Circuit

The over current protection circuit cuts off the power supply relay when it detects abnormal current increased in the +35V power line due to failure of the vertical deflection circuit.

3-1-1. Theory of Operation

Fig. 8-11 shows the circuit diagram of the over current protection circuit. When the load current of the +35V line increases, the voltage across a resistor of T370 will also increase.

When the voltage increases across R370. and the voltage developed across R371 becomes higher than the Vbs of Q370, Q370 turns on and a voltage develops across R374 due to the collector current flowing. When this voltage increases to a value higher than about 7V, Z801 operates, thus cutting off the power relay. When the circuit operates, a power LED provided will turn on and off in red.

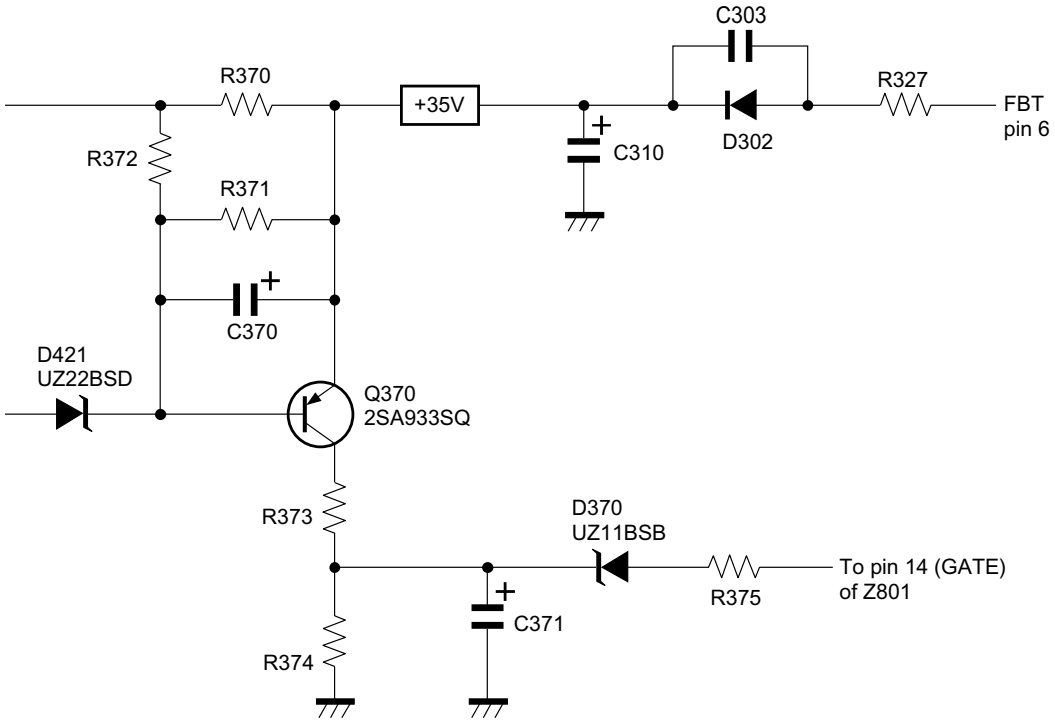


Fig. 8-11

4. RASTER POSITION SWITCHING CIRCUIT

4-1. Outline

When the vertical screen position adjustment is carried out on the projection TV, DC current is directly flown in the vertical deflection yoke and the raster cannot be moved up and down. (Because the raster is moved, the color distortion may occur.) Accordingly, the vertical screen position adjustment is carried out by the following method. (Only in CINEMA and SUBTITLE mode)

V sync pulse output from Q501 sync. separation circuit is once input to WAC, delayed and then output. The deflection circuit operates with the delayed sync signal. The screen upper side position moves up and down by varying the delay time. When the vertical position adjustment is carried out by WAC, the followings must be considered.

WAC becomes "through" except for CINEMA and SUBTITLE mode.

The phase of the output V sync must not advance from that of WAC input V sync. If it advances, Vertical jitter may occur when performing the search operation and the vertical position adjustment of a VTR.

So, adjust the center of the picture to the center of the screen in advance under the output V sync delayed.

To do this, lower the raster position by flowing a DC current to the deflection yoke in the CINEMA and SUBTITLE mode.

The operation above is carried out by the vertical screen position SW circuit.

4-2. Operation

When CINEMA and SUBTITLE are selected in the screen mode, a zoom signal is input to the base of Q362 from the autolive circuit and Q362 turns on. Then, Q363 turns off and the base of Q364 develops H and Q364 turns on. The inverted DC current flows into the vertical deflection yoke from +35V power supply line.

Fig. 8-12

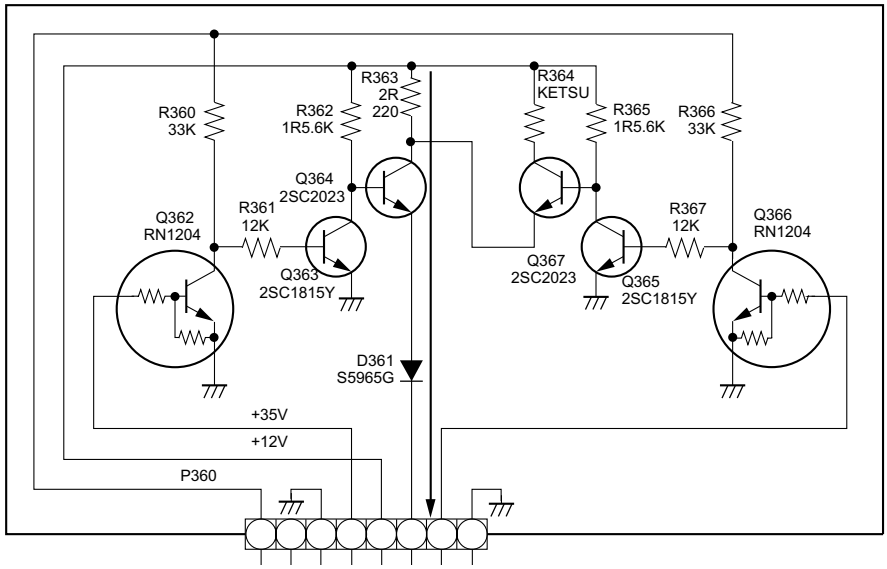
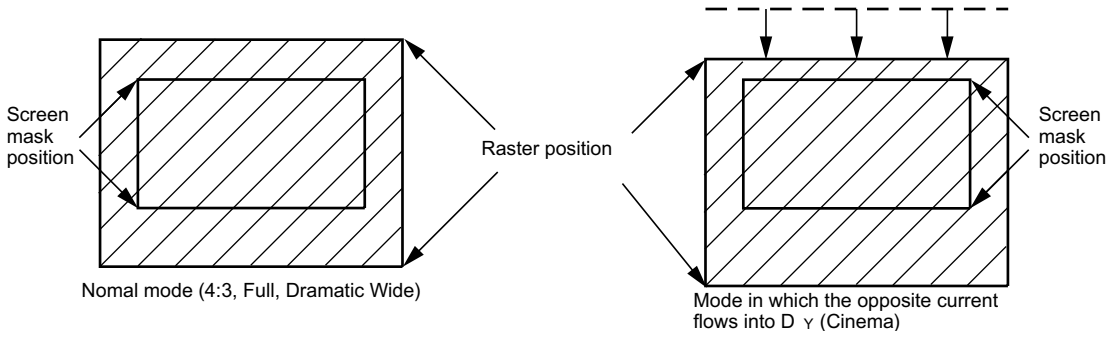


Fig. 8-13



SECTION IX: HORIZONTAL DEFLECTION CIRCUIT

1. OUTLINE

The H deflection circuit works to deflect a beam from left to right by flowing a sawtooth waveform of 15.625 kHz/15.735 kHz into the DY H deflection coil.

2. HORIZONTAL DRIVE CIRCUIT

The H drive circuit works to start the H output circuit by applying H VCC (Q501 DEF power source) to pin 22 of Q501 (TA1222N) and a bias to the H drive transistor Q402 at the main power on.

2-1. Theory of Operation

(1) When the power switch is on, the main power supply of 125V starts to rise. At the same time, AF power supply 38V also rises.

(2) With 38V line risen, Q430 base voltage which is created by dividing the audio power with R433 and D430 also rises. Then, the transistor Q430 turns on and the H VCC is applied from the audio power line through R432 and D431 to pin 22 of Q501.

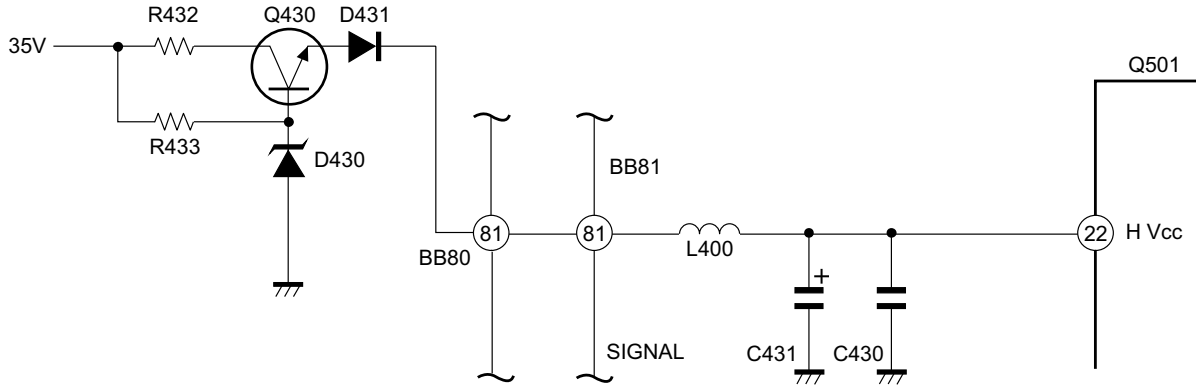


Fig. 9-1 H drive circuit block diagram

3. BASIC OPERATION OF HORIZONTAL DRIVE

A sufficient current must flow into base of the horizontal output transistor to rapidly make it into a saturated (ON) condition or a cut off (OFF) condition. For this purpose, a drive amplifier is provided between the oscillator circuit and the output circuit to amplify and to waveshape the pulse voltage.

3-1. Theory of Operation

(1) The horizontal drive circuit works as a so called switching circuit which applies a pulse voltage to the output transistor base and makes the transistor on when the voltage swings in forward direction and off in reverse direction.

(2) To turn on the output transistor completely and to make the internal impedance low, a sufficiently high, forward drive voltage must be applied to the base and heavy base current ib must be flown. On the contrary, to completely turn off the transistor, a sufficiently high, reverse voltage must be applied to the base.

(3) When the transistor is on (collector current is maximum) condition with the sufficiently high forward voltage applied to the base, the transistor can not be turned off immediately, if a reverse base bias is applied to the base because minority carriers storaged in the base can not be reduced to zero instantly. That is, a reverse current flows through an external circuit and gradually reduces to zero. The time lag required for the base current to disappear is called a storage time and falling time.

(4) To shorten the storage time and the falling time, a sufficiently high reverse bias voltage must be applied to allow a heavy reverse current to flow. This operation also stabilizes operation of the horizontal output transistor.

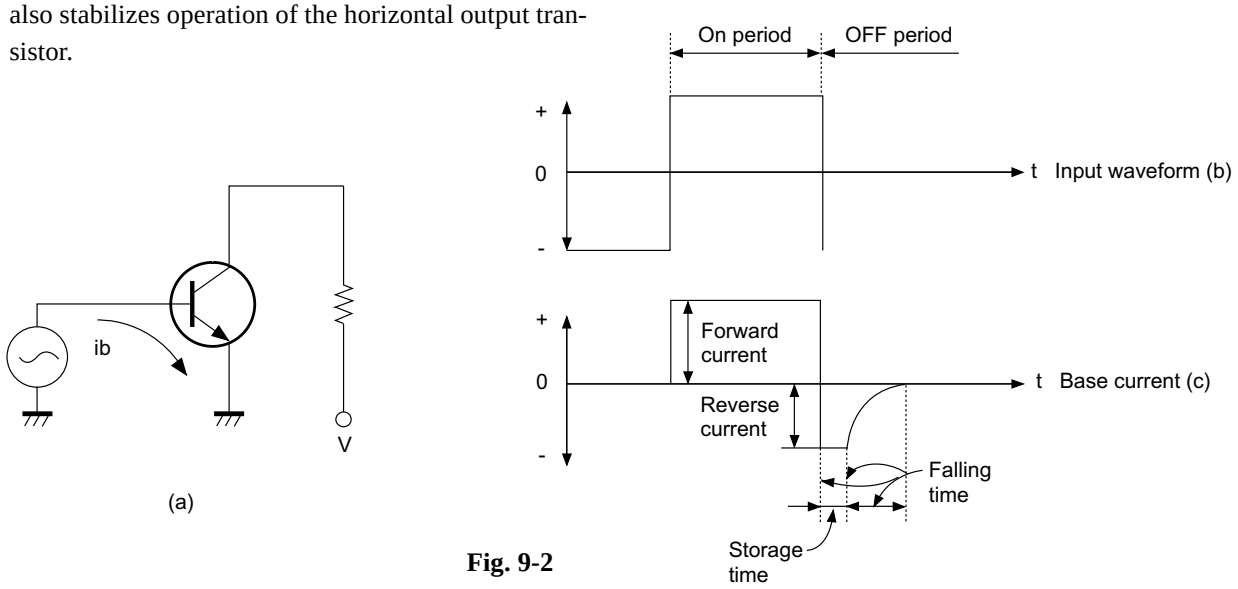


Fig. 9-2

3-2. Circuit Description

In the N5SS chassis, the off drive system is employed.

(1) When Q1 inside Q501 is turned on, Q402 base is forward biased through 9V ® pin 22 of Q501 (H. VCC) ® pin 23 of Q501 (H. Out) ® R411/R410 resistor divider, and then, Q402 collector current flows through 125V ® R416 ® T401. In this case, the H output transistor Q404 turns on with the base-emitter reverse biased because of the off drive system employed.

(2) On the contrary, when Q1 inside IC501 is off (pin 8 is 0V), base-emitter bias of Q402 becomes 0V and Q402 turns off, and a collector pulse as shown in Fig. 9-3 develops at the collector.

The voltage is stepped down and Q404 is forward biased with this voltage, thus turning on Q404.

(3) In this way, by stepping down the voltage developed at primary winding of the drive transformer and by applying it to Q404, a sufficient base current flows into Q404 base, thereby switching the Q404.

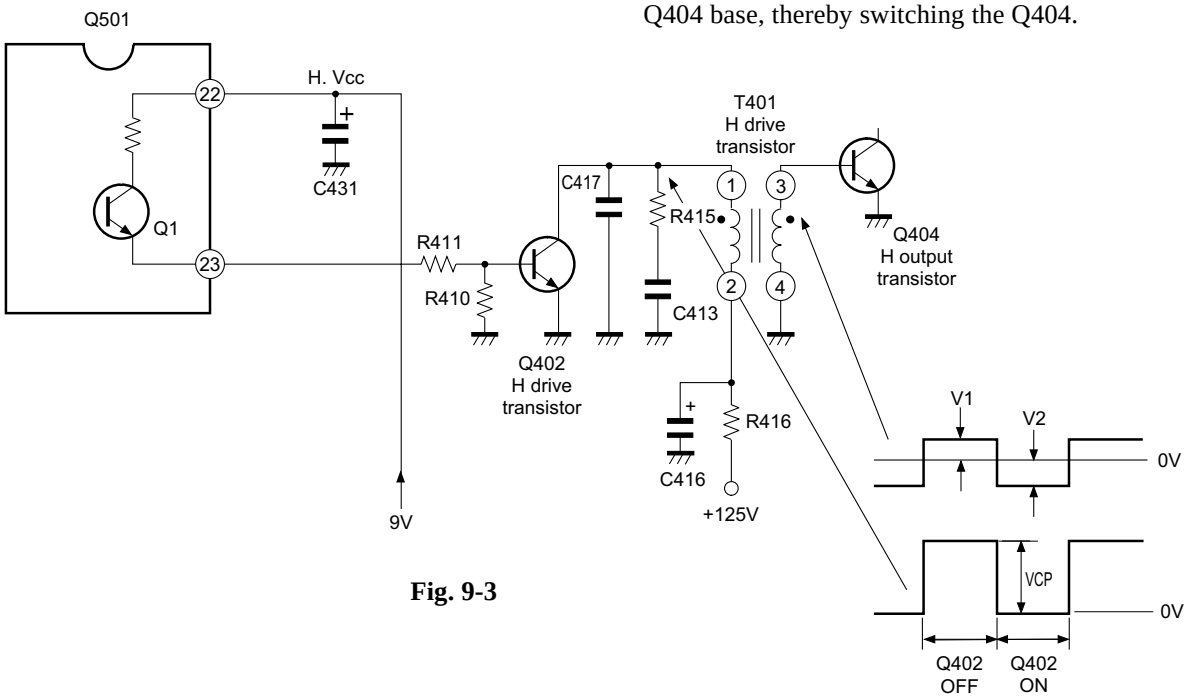


Fig. 9-3

4. HORIZONTAL OUTPUT CIRCUIT

The horizontal output circuit applies a 15.625 kHz/15.734 kHz sawtooth wave current to the deflection coil with mutual action of the horizontal output transistor and the damper diode, and deflects the electron beam from left to right in horizontal direction.

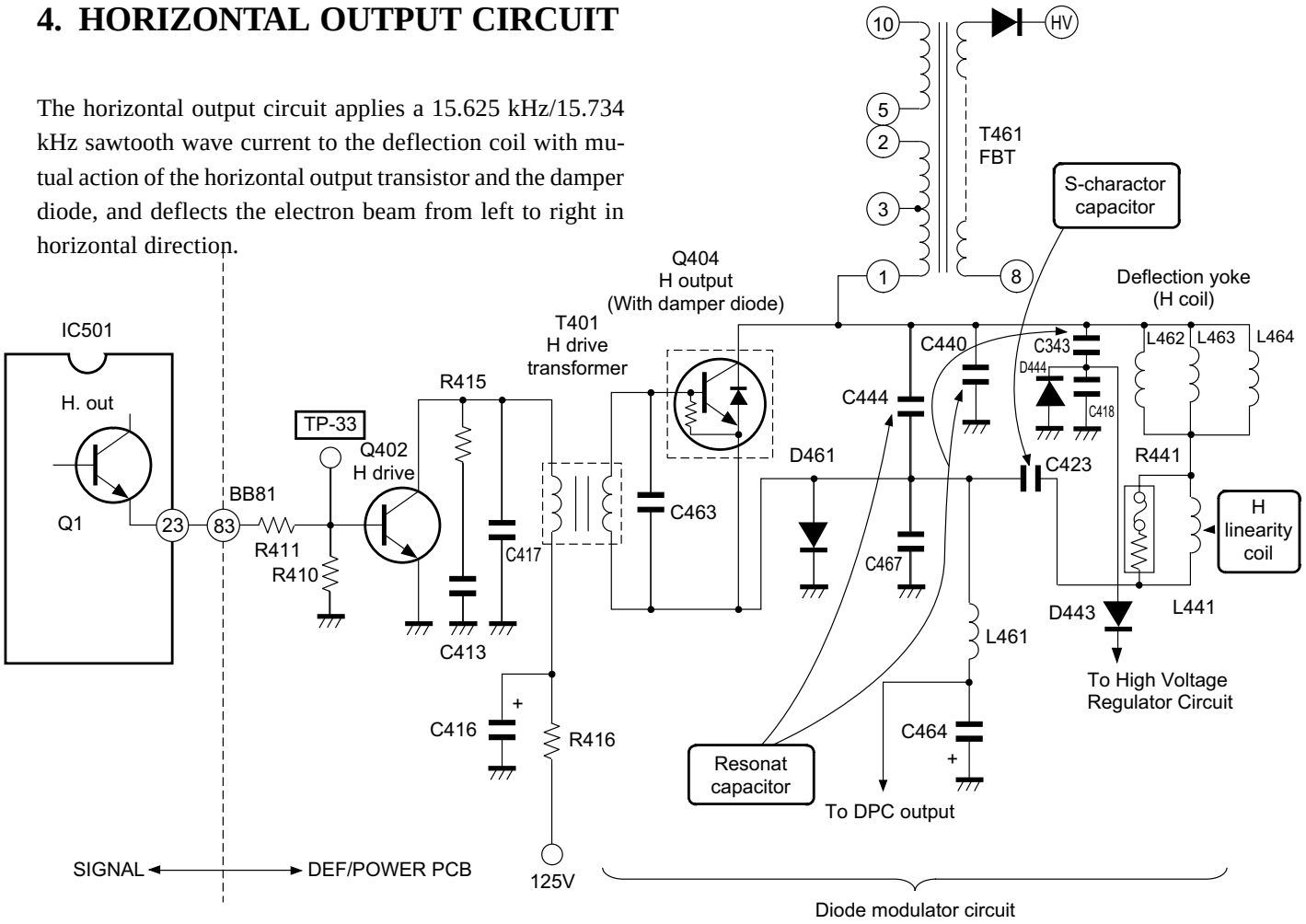


Fig. 9-4

4-1. Theory of Operation

4-1-1. Operation of Basic Circuit

(1) To perform the horizontal scanning, a 15.625 kHz/ 15.735 kHz sawtooth wave current must be flown into the horizontal deflection coil. Theoretically speaking, this operation can be made with the circuit shown in Fig. 9-5 (a) and (b).

(2) As the switching operation of the circuit can be replaced with switching operation of a transistor and a diode, the basic circuit of the horizontal output can be expressed by the circuit shown in Fig. 9-5 (a). That is, the transistor can be turned on or off by applying a pulse across the base emitter. A forward switching current flows for on-period, and a reverse switching current flows through the diode for off-period. This switching is automatically carried out. The diode used for this purpose is called a damper diode.

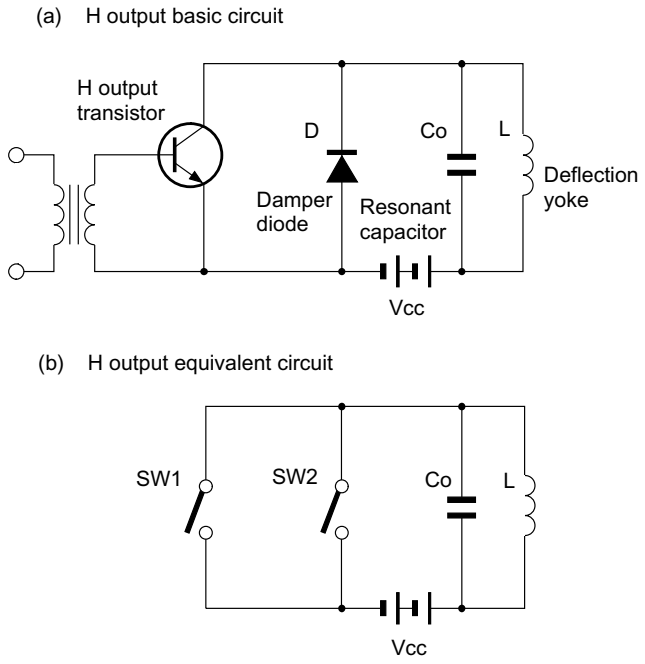


Fig. 9-5

Description of the basic circuit

1. t1~t2:

A positive pulse is applied to base of the output transistor from the drive circuit, and a forward base current is flowing. The output transistor is turned on in sufficient saturation area. As a result, the collector voltage is almost equal to the ground voltage and the deflection current increases from zero to a value in proportionally. (The current reaches maximum at t2, and a right half of picture is scanned up to this period.)

2. t2:

The base drive voltage rapidly changes to negative at t2 and the base current becomes zero. The output transistor turns off, collector current reduces to zero, and the deflection current stops to increase.

3. t2~t3:

The drive voltage turns off at t2, but the deflection current can not reduce to zero immediately because of inherent nature of the coil and continues to flow, gradually decreasing by charging the resonant capacitor C0. At the same time, the capacitor voltage or the collector voltage is gradually increases, and reaches maximum voltage when the deflection current reaches zero at t3. Under this condition, all electromagnetic energy in the deflection coil at t2 is transferred to the resonant capacitor in a form of electrostatic energy.

4. t3~t4:

Since the charged energy in the resonant capacitor discharges through the deflection coil, the deflection current increases in reverse direction, and voltage at the capacitor gradually reduces. That is, the electrostatic energy in the resonant capacitor is converted into a electromagnetic energy in this process.

5. t4:

When the discharge is completed, the voltage reduces to zero, and the deflection current reaches maximum value in reverse direction. The t2~t4 is the horizontal flyback period, and the electron beam is returned from right end to the left end on the screen by the deflection current stated above. The operation for this period is equivalent to a half cycle of the resonant phenomenon with L and C0, and the flyback period is determined by L and C0.

6. t4~t6:

For this period. C0 is charged with the deflection current having opposite polarity to that of the deflection current stated in "3.", and when the resonant capacitor voltage exceeds VCC, the damper diode D conducts. The deflection current decreases along to an exponential function (approximately linear) curve and reaches zero at t6. Here, operation returns to the state described under "1.", and the one period of the horizontal scanning completes. For this period a left half of the screen is scanned.

In this way, in the horizontal deflection scanning, a current flowing through the damper diode scans the left half of the screen; the current developed by the horizontal output transistor scans the right half of the screen; and for the flyback period, both the damper diode and the output transistor are cut off and the oscillation current of the circuit is used. Using the oscillation current improves efficiency of the circuit. That is, about a half of deflection current (one fourth in terms of power) is sufficient for the horizontal output transistor.

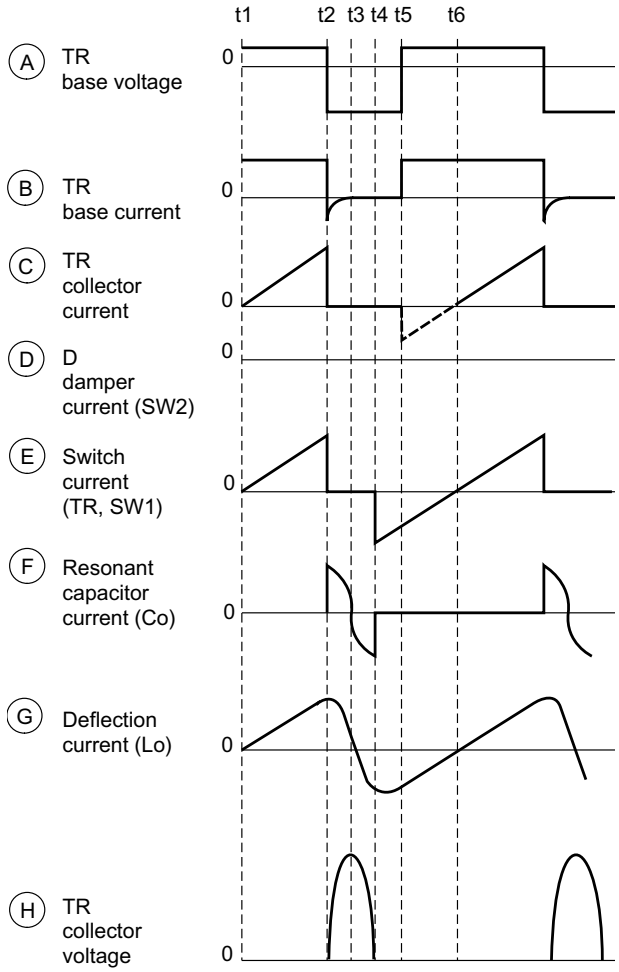


Fig. 9-6

Amplitude Correction

To vary horizontal amplitude, it is necessary to vary a sawtooth wave current flowing into the deflection coil. These are two methods to vary the current; a method which varies L_H by connecting a variable inductance L in series with the deflection yoke, and a method which varies power supply voltage (across S-character capacitor) for the deflection yoke.

As the DPC circuits is used in the this chassis, the later method which varies the deflection yoke power supply voltage by modifying the bus data is used.

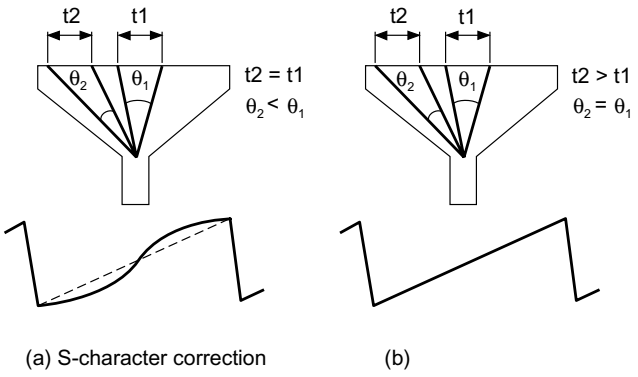


Fig. 9-7

4-1-2. Linearity Correction (LIN)

(1) S-curve Correction (S Capacitor)

Pictures are expanded at left and right ends of the screen even if a sawtooth current with good linearity flows in the deflection coil when deflection angle of a picture tube increases. This is because projected image sizes on the screen are different at screen center area and the circumference area as shown in Fig. 9-7. To suppress this expansion at the screen circumference, it is necessary to set the deflection angle q_1 to a large value (rapidly deflecting the electron beam) at the screen center area, and to set the deflection angle q_2 to a small value (scanning the electron beam slowly) at the circumference area as shown in Fig. 9-7.

In the horizontal output circuit shown in Fig. 9-8, capacitor C_S connected in series with the deflection coil L_H is to block DC current. By properly selecting the value of C_S and by generating a parabolic voltage developed by integrating the deflection coild current across the S capacitor, and by varying the deflection yoke voltage with the voltage, the scanning speed is decreased at beginning and end of the scanning, and increased at center area of the screen. The S curve correction is carried out in this way, thereby obtaining pictures with good linearity.

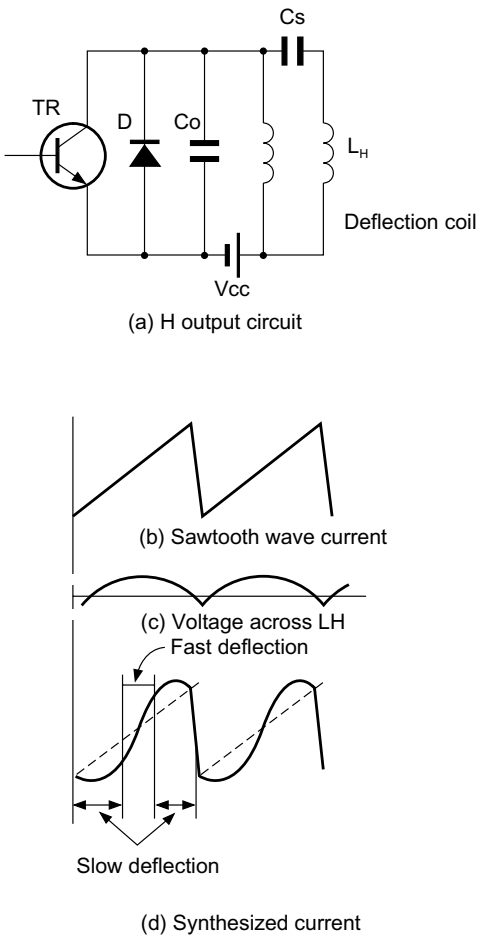


Fig. 9-8

(2) Left-right Asymmetrical Correction (LIN coil)

In the circuit shown in Fig. 9-9 (a), the deflection coil current iH does not flow straight as shown by a dotted line in the Fig. 9-9 (b) if the linearity coil does not exist, by flows as shown by the solid line because of effect of the diode for a first scanning (screen left side) and effect of resistance of the deflection coil for later half period of scanning (screen right side). That is, the deflection current becomes a sawtooth current with bad linearity, resulting in reproducing of asymmetrical pictures at left and right sides of the screen (left side expanded, right side compressed).

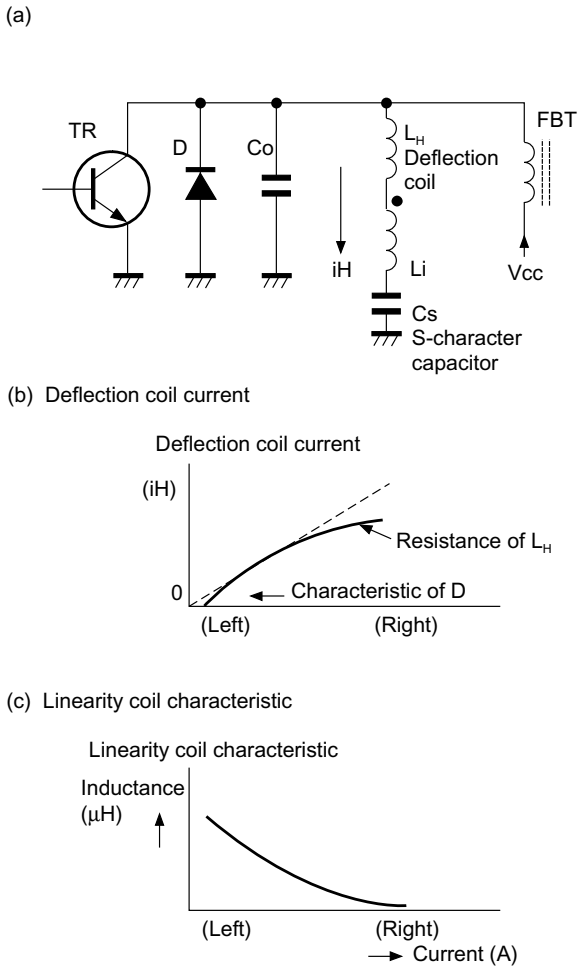


Fig. 9-9 Linearity coil

When a horizontal linearity coil L_1 with a current characteristic as shown in Fig. 9-9 (c) is used, left side picture will be compressed and right side picture will be expanded because the inductance is high at the left side on the screen and low at the right side. The left-right asymmetrical correction is carried out in this way, and pictures with good linearity in total are obtained.

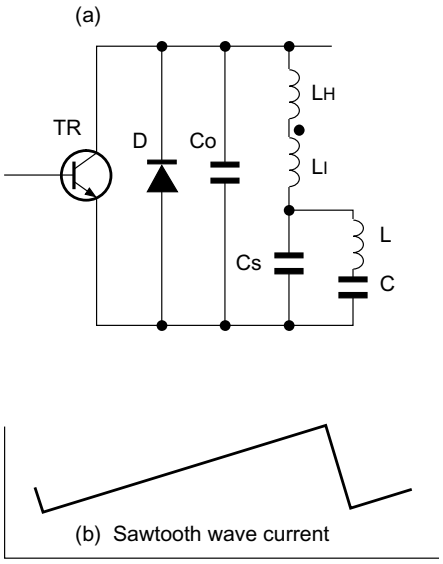


Fig. 9-10

4-2. White Peak Bending Correction Circuit

4-2-1. Outline

White peak area in screen picture may sometimes cause bending in picture. See figure below.

In TP48E60 series, correction signal which video ripple in video output circuit power supply 200V is input to pin 24 (Bending correction terminal) of Q501. This corrects white peak bending.

4-2-2. Operation Theory

Fig. 9-11 shows circuit diagram. Video ripple in video output circuit power supply 200V suffers DC cut by C475, and is inverted in Q470, then input to pin 24 of Q501 via C481. Pin 24 of Q501 is a bending correction terminal. The voltage which is applied to this terminal, controls phase of video signal to correct white peak bending.

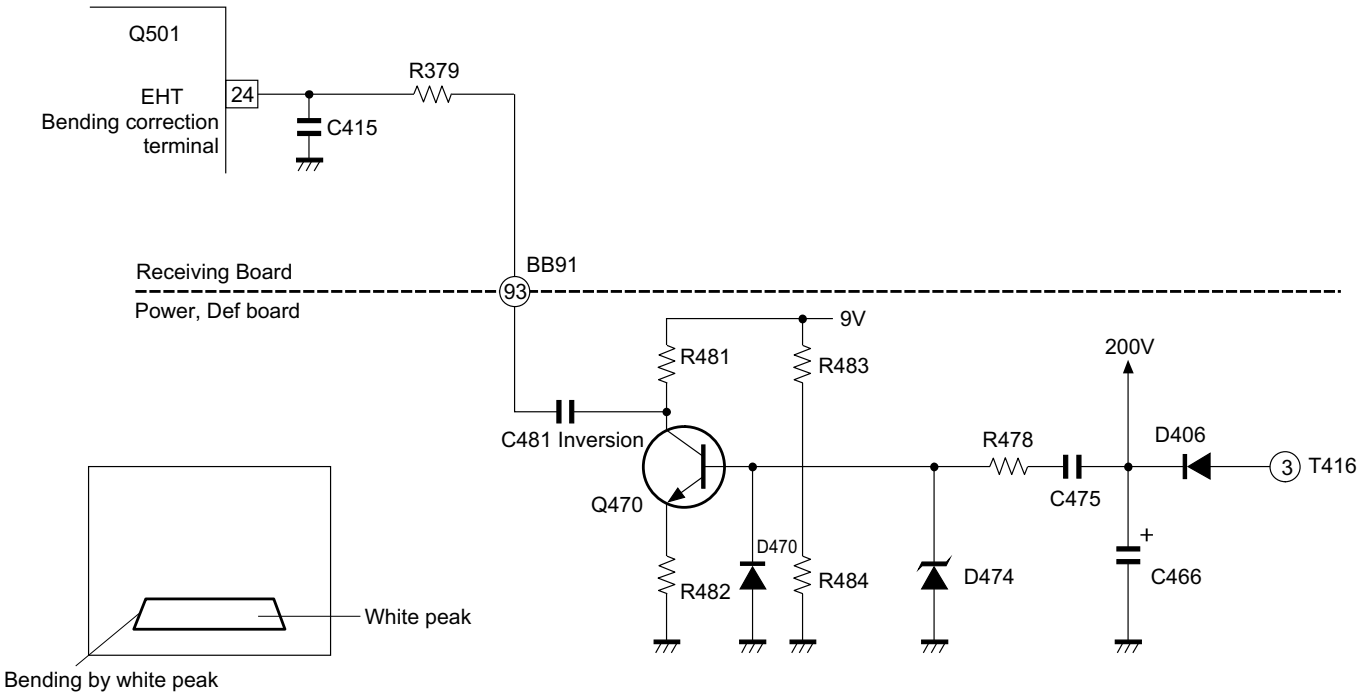


Fig. 9-11 White peak bending correction circuit

4-3. H Blanking

4-3-1. Outline

The H blanking circuit applies a blanking precisely for the horizontal flyback period so that undesirable pictures folding does not appear at screen ends.

This unit allows the users to adjust an horizontal amplitude adjustment, so, picture quality at screen ends will be improved. This is one of the purposes of the blanking circuit.

4-3-2. Theory of Operation

The H blanking circuit determines the flyback period precisely from the AFC pulse in the FBT and applies the period to emitter of the video output stage transistor on the CRT-D PC board.

4-3-3. Circuit Operation

As can be seen from Fig. 9-12, the flyback period of the AFC pulse in the FBT starts at a negative side from 0V. To detects this, the DC component is cut with C493. This is, C493 is always charged through D487 with a negative side (about –17V) of the AFC pulse. As a result, a voltage at point A in the waveform rises from the ground level. This waveform is sliced in a circuit (R486, D486) to detect the flyback period. Thus obtained voltage is applied to Q901, Q911, and Q921 through D904, D914, D927 and cuts off them thereby blanking the resters.

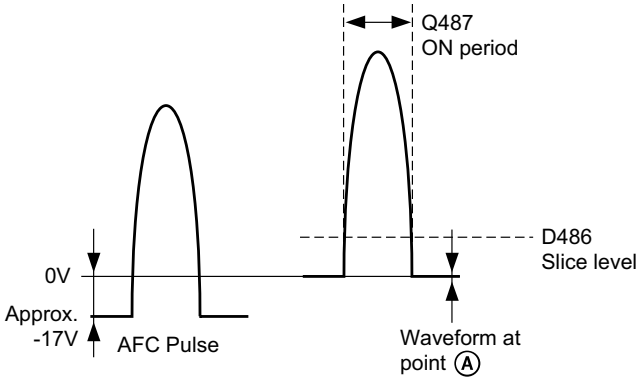


Fig. 9-12

Fig. 9-13

4-4. 200V Low Voltage Protection

4-4-1. Outline

When the video output power supply 200V is stopped by some abnormality occurence, the current inside CPT increases abnormally. So the CPT may be damaged. To prevents this, a 200V low voltage protection circuit is provided.

4-4-2. Theory of Operation

Fig. 9-14 shows a connection diagram.

Under a normal condition Q340 is always on because of about 210V supplied from the 200V line. Accordingly Q340 collector is kept at about 6.2V or the zener voltage of D341 and Q341 is turned off.

If some abnormality occurs and 200V line voltage lowers by less than about 160V. Q340 turns off and its collector voltage rises. So Q341 turns on. With Q341 turned on the voltage at pin 14 of Z801 (expander) exceeds a threshold voltage and pin 16 of Z80 is high level and makes the power relay turn off.

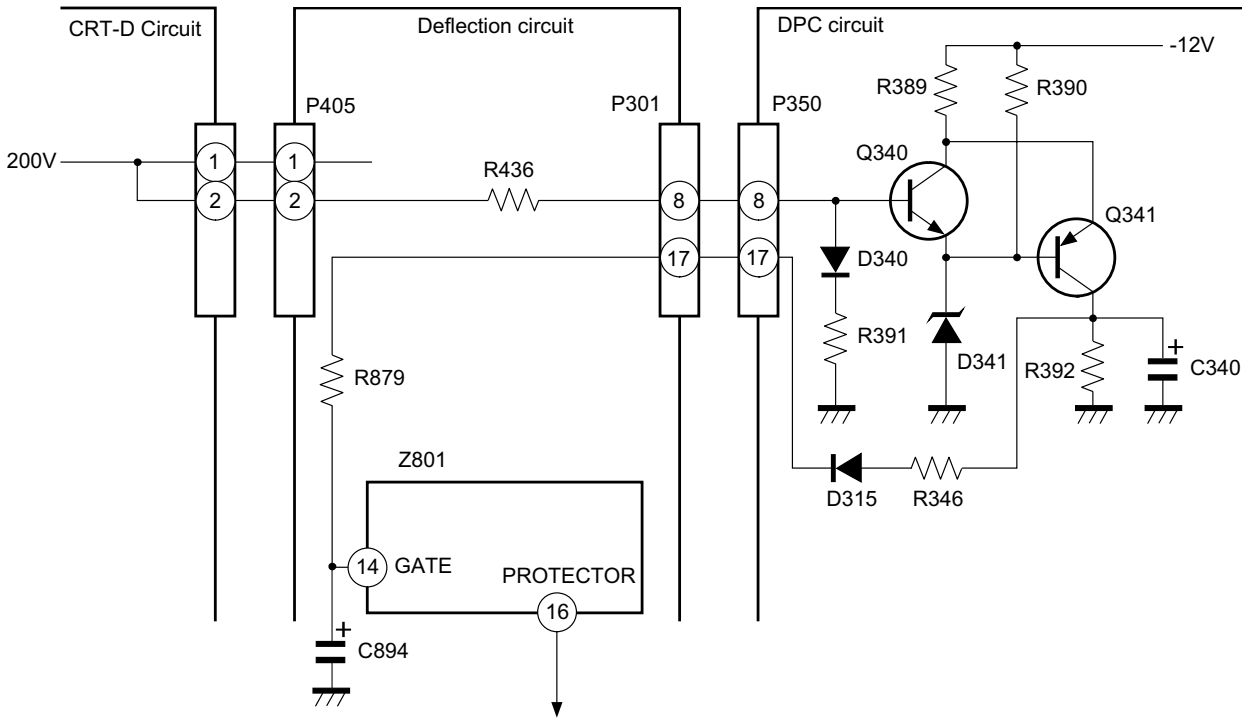


Fig. 9-14

5. HIGH VOLTAGE GENERATION CIRCUIT

The high voltage generation circuit develops an anode voltage for the picture tube, focus, screen, CRT heater, video output (210V) and so on by stepping up the pulse voltage developed for flyback period of the horizontal output circuit with the FBT, and supplies the power to various circuit.

5-1. Theory of Operation

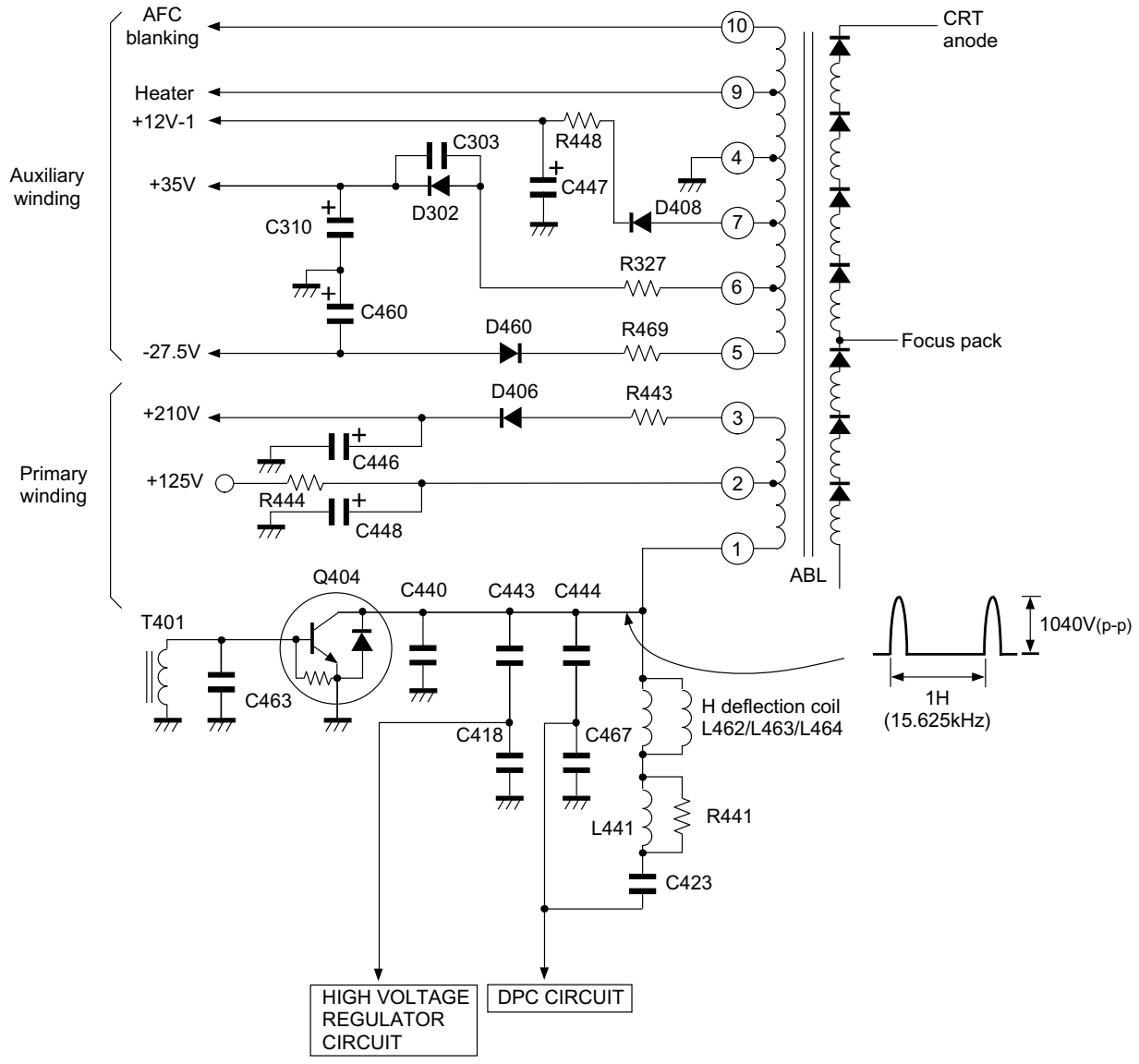


Fig. 9-15

5-1-1. +210V

For the flyback period, pulses are stacked up to DC +125V with FBT, and the voltage is rectified by D406 and filtered by C446.

5-1-2. +35V, 12V

Pin 4 of the FBT is grounded and the shaded area of negative pulse developed for opposite period of the flyback period is rectified, thus developing better regulation power supply.

5-1-3. –27V

As a power for the DPC circuit, a negative pulse signal is rectified by D460 and filtered with C460, thus developing the –27V.

5-1-4. High Voltage

Singular rectification system which uses a harmonics non-resonant type FBT is employed and a better high voltage regulation is obtained, so amplitude variation of pictures becomes low.

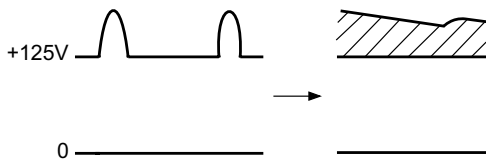


Fig. 9-16

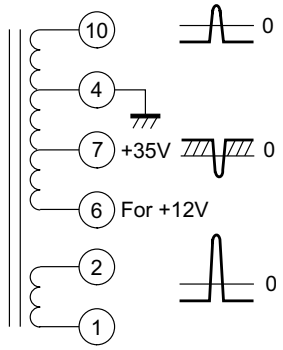


Fig. 9-17

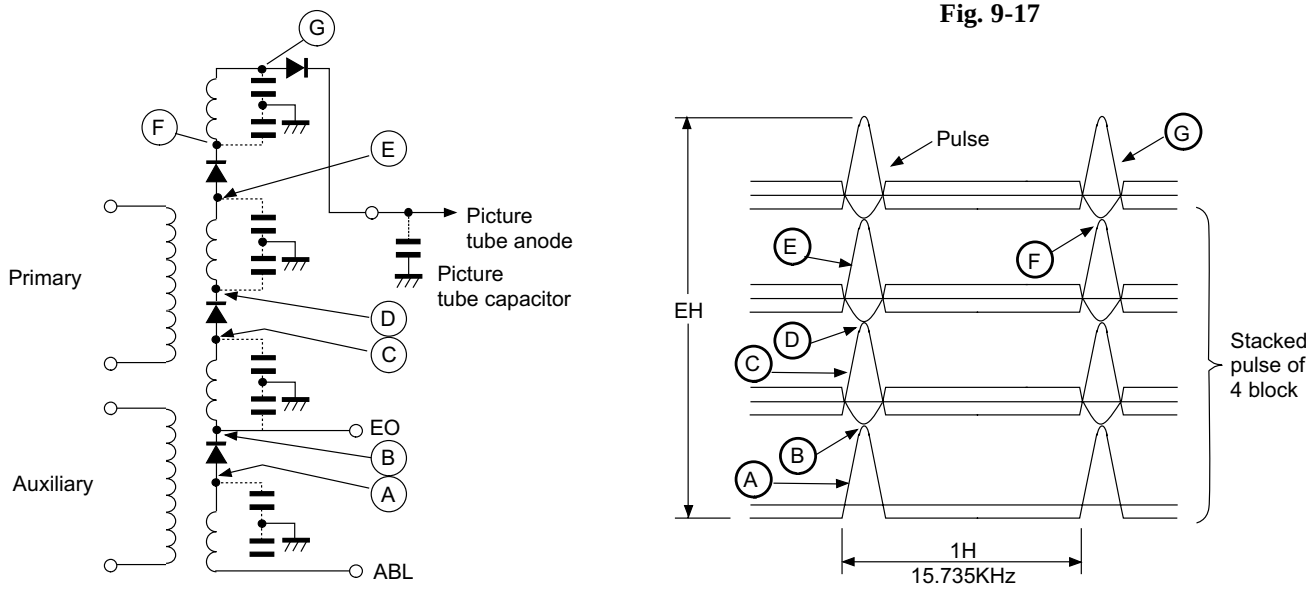


Fig. 9-18

5-2. Operation Theory of the Harmonic Non-Resonant System and Tuned Waveforms

The high voltage coil is of film multi-layer winding type and the coils are isolated into seven blocks. Each block is connected through a diode.

The basic operation is described in the case of 4 blocks construction for simplification. Positive or negative pulse determined by stray capacitance of each coil develops at terminal points (Ⓐ,Ⓑ,Ⓒ,Ⓓ,Ⓔ,Ⓕ,Ⓖ) of each coil as shown in Fig. 9-18, and these pulses are stacked as shown, thus developing the high voltage.

Moreover, a capacitance between the internal and external coatings of the picture tube works as a smoothing capacitor.

Focus voltage is obtained at point EO.

6. HIGH VOLTAGE CIRCUIT

6-1. High Voltage Regulator

6-1-1. Outline

Generally, four kinds of methods exist to stabilize a high voltage in high voltage output circuits using the FBT:

(1) Stabilization by varying the power supply voltage.

(2) Stabilization by varying L value with a saturable reactance connected in series with the primary winding of the FBT.

(3) Stabilization by varying equivalent capacitance of the resonant capacitor C0.

(4) Stabilization by superimposing a DC or pulse (this varies the high voltage) on a lower voltage side of the high voltage winding of the FBT.

In this unit, pulse transformer is eliminated and the regulator circuit using the method (3) is employed. The block diagram is shown in Fig. 9-19.

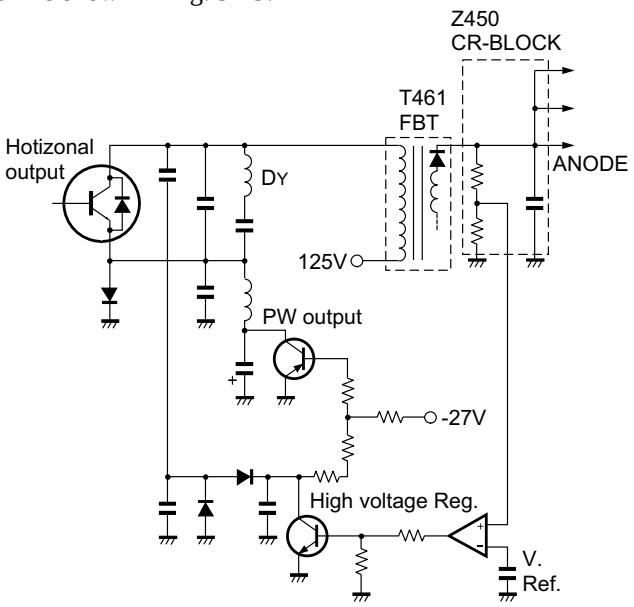


Fig. 9-19 Basic circuit for high voltage regulator emplyed in the unit

6-1-2. Theory of Operation

Fig. 9-20 shows a basic circuit of the high voltage regulator used in the unit.

The high voltage regulator circuit splits a resonant capacitor C0 to C1 and C2. thereby dividing the collector voltage (V_{CP}) of the H output transistor with C1 and C2.

Here, assume each voltage developed across C1 and C2 as V_{CP1} and V_{CP1}, respectively,

each relation can be expressed by the above equations ① ~ ③ .

$$V_{CP1} = \frac{C2}{C_1 + C_2} V_{CP} \quad \text{——————} ①$$

$$V_{CP2} = \frac{C2}{C_1 + C_2} V_{CP} \quad \text{——————} ②$$

$$V_{CP} = \frac{C2}{C_1 + C_2} V_{CP2} \quad \text{——————} ③$$

The V_{CP2} developed across C2 is DC-clamped with a diode D1 and the resultant voltage is smoothed with a diode D2 and a capacitor C3. Thus processed voltage is obtained at the point Ⓑ. This voltage is used to provide a base current for the transistor Q1 or to flow the collector current. The voltage at the point Ⓑ decreases with the circuit impedance and finally lowers up to a V_{CE} saturation voltage of Q1.

Then, V_{CP2} is not clamped by D2 with the voltage at the point Ⓑ. Since the V_{CP} is expressed as a sum of V_{CP1} and V_{CP2} as shown by equation ③, V_{CP} decreases by amount the V_{CP2} is decreased. This varies the high voltage.

Q1 collector current is controlled by Q1 base current which is an output of the comparison inverted amplifier. That is, the Q1 base current is controlled by a voltage obtained by comparing a detection voltage of the top breeder of the FBT (9.1V) and a DC voltage of 9V.

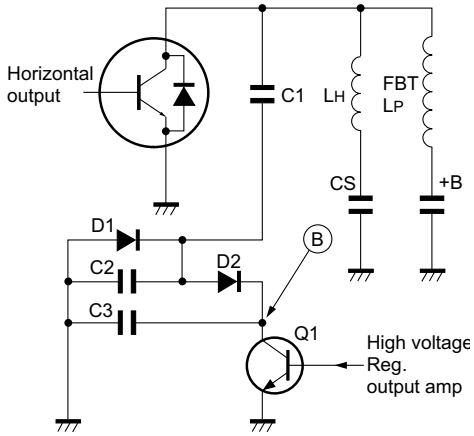


Fig. 9-20

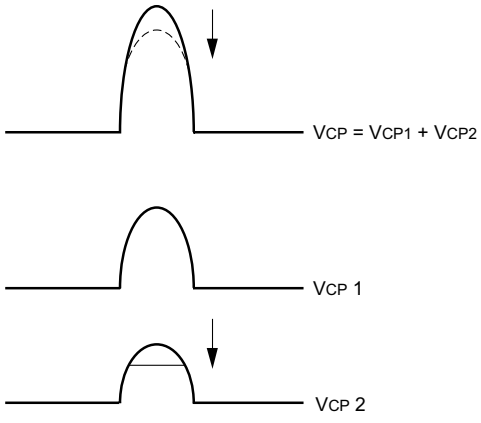


Fig. 9-21

6-1-3. Actual

Fig. 9-22 shows the actual circuit used in the unit.

A resonant capacitor C0 is also split into two capacitors C443 and C444 in this circuit. The high voltage regulator cirucits is structured by splitting the C443 to two capacitors of C443 and C448.

Here, assume a high voltage increases and the detection voltage E_D' obtained by dividing the high voltage also increases in proportional to the high voltage. This makes the voltage E_D increase at pin 7. (The voltage is impedance transformed by a voltage follower circuit consisting of op amplifier Q483 at pin 7.)

The voltage E_D and a 9V reference voltage developed by a 3-terminal regulator Q420 are compared. When the E_D increases, the voltage at pin 2 of Q483 differential amplifier also increases, and the base current I_B of the high voltage transistor Q480 increases.

As a result, Q480 collector current increases and Q480 collector voltage (at the point Ⓑ) decreases. Then, a peak value of V_{CP2} across C418 is clamped by the diode D443 at the collector voltage lowered, and the collector voltage V_{CP} of Q404 (H output transistor) obtained as a sum of the voltage V_{CP1} across C443 and V_{CP2} across L418 decreases. Then, the high voltage also decreases.

When the high voltage lowers, the corrective operation is carried out in reverse order.

* Resustors R451, R452, R453 and R455 are used to correct undersirable influence (H amplitude increase at minimum I_H) by the H amplidude regulator.

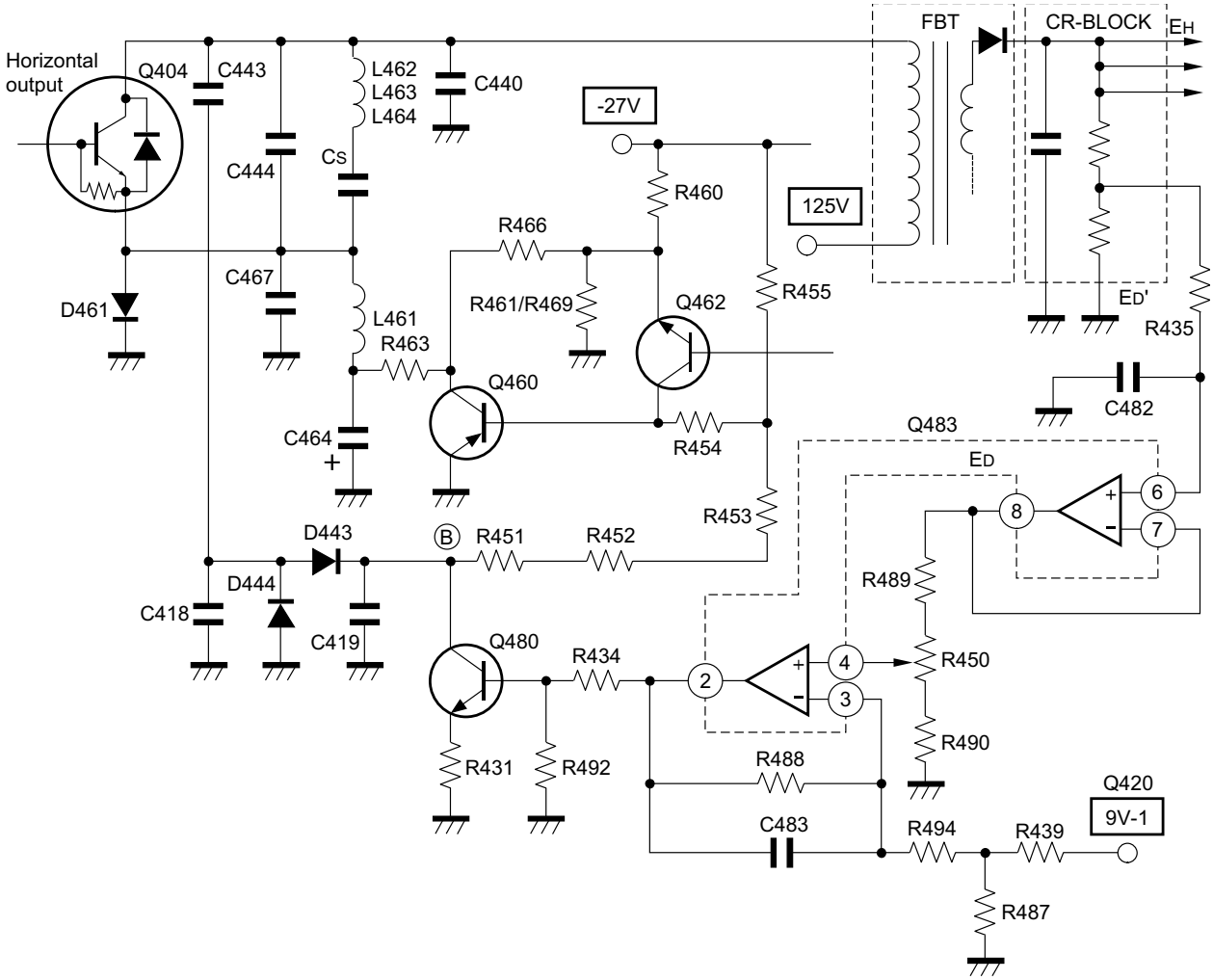


Fig. 9-22 Actual high voltage regulator circuit

7. X-RAY PROTECTION CIRCUIT

7-1. Outline

In case picture tube using high voltage, when high voltage rises abnormally due to components failure and circuit malfunction, there is possible danger that X-RAY leakage increases to affect human body. To prevent it, X-RAY protection circuit is equipped.

7-2. Operation

Figure 9-23 shows the circuit diagram. Supposing high voltage rises abnormally due to some reason, pulse at pin 9 of T461 also rises, and detection voltage E_D rectified by D471 and C471 in X-RAY protection circuit rises. When E_D rises, emitter voltage of Q464 divided by R459 and R462 becomes higher than [zener voltage (6.2V) of D458 + Q464 VBE]. This causes Q464 turns on to supply base current to Q463. Then Q463 turns on. By this Tr6 and Tr6 turn on to make ON/OFF pulse at pin 7of QA01 in low level, Q846 and Q845 turns off, then relay SR81 turns off. Tr6 and Tr7 are in thyristor-connection, and 5V of power holds protection operation until main power switch is turned off. During circuit operation, power LED near main power switch blinks turn on and off in red.

Caution:

- To restart TV set, repair failure first.

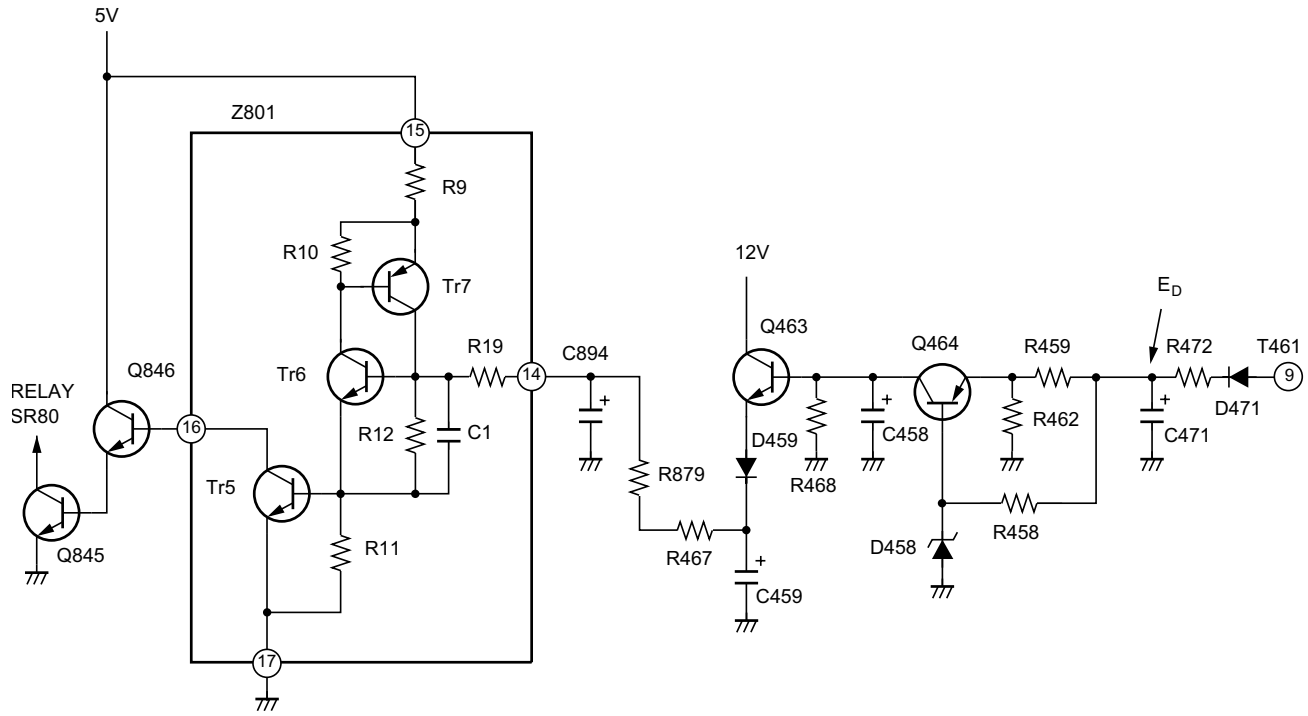


Fig. 9-23 X-RAY protection circuit

8. OVER CURRENT PROTECTION CIRCUIT

8-1. Outline

If main power (125V) current increases abnormally due to components failure, there is possible danger of the secondary damage like failure getting involved in other part failure, and abnormal heating. To prevent this, over current protection circuit is equipped, which detects current of main B line to turn off power relay in abnormal situation.

8-2. Operation

Fig. 9-24 shows over current protection circuit. When the current of main B line increases abnormally due to the shortage in load of main B line, voltage drop arises across R470. By this voltage drop, when base-emitter voltage of Tr8 in protector module (Z801) becomes approx. 0.7V or more, Tr8 turns on, and the voltage by divided ratio of R15 and R16 is applied to cathode of ZD4. When this voltage becomes higher than zener voltage of ZD4, ZD4 turns on to supply base current to base of Tr6 via R14. This causes Tr5 ON and voltage at pin 16 of Z801 becomes low.

Therefore, QB30 and Q843 turns off to set SR81 OFF. Tr6 and Tr7 in Z801 are in thyristor-connection, and power 5V-1 supplied at pin 15 keeps protection operation for standby power until main power switch is turned off. During circuit operation, power LED near main power switch blinks in red.

Caution:

- To restart TV set, repair failure first.

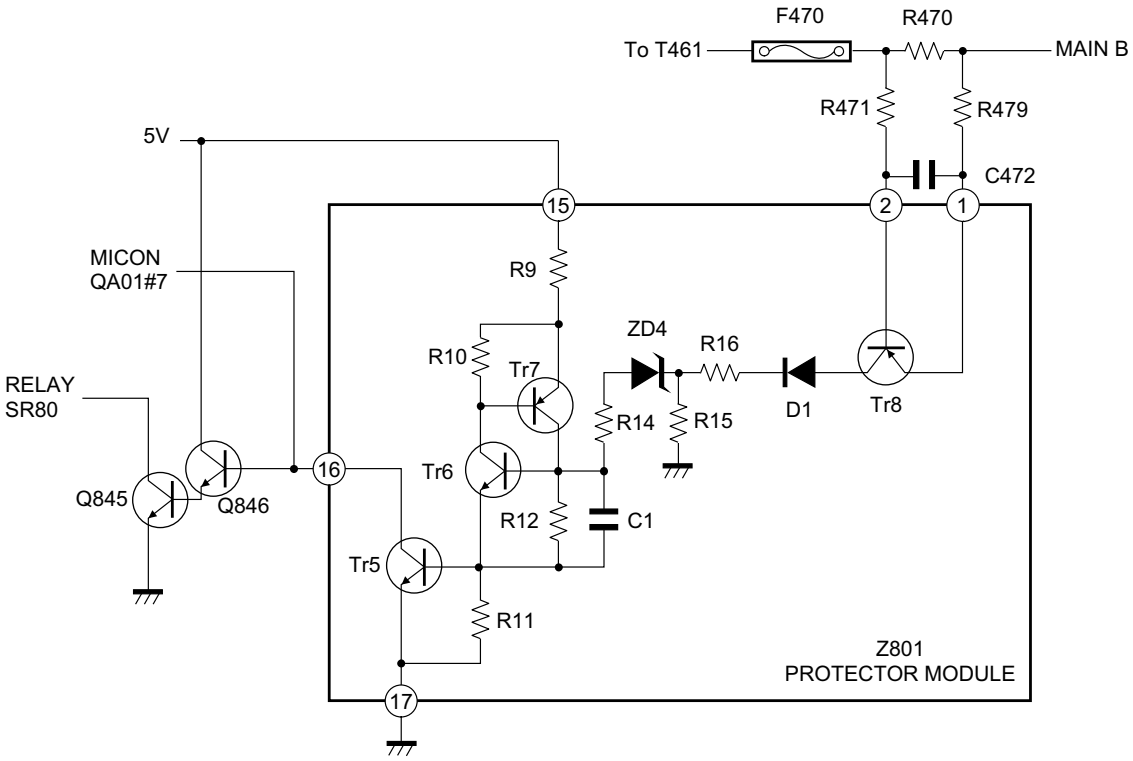


Fig. 9-24 Over current protection circuit

SECTION X: DEFLECTION DISTORTION CORRECTION CIRCUIT

(SIDE DPC CIRCUIT)

1. DEFLECTION DISTORTION CORRECTION IC (TA8859CP)

1-1. Outline

The deflection distortion correction IC (TA8859CP), in combination with a V/C/D IC (TA1222AN) which has a V pulse output, performs correction for various deflection distortions and V output through the I^2C bus control. All the I^2C bus controls are carried out by a microcomputer and can be controlled with the remote control.

1-2. Functions and Features

The IC has functions of V RAMP voltage generation, V amplitude automatic switching (50/60 Hz), V linearity correction, V amplification, EHT correction, side pincushion correction, I^2C bus interface, etc. and controls following items through the I^2C bus lines.

(1) V amplitude

(2) V linearity

(3) V S-character correction

(4) V picture position (neutral voltage setting)

(5) V M-character correction

(6) V EHT correction

(7) H amplitude

(8) L and R pin-cushion distortion correction I (entire area) – Not used for this model.

(9) L and R pin-cushion distortion correction II (corner portions at top and bottom) – Not used for this model.

(10) H trapezoid distortion correction – Not used for this model.

(11) H EHT correction

(12) V AGC time constant switching

1-3. Block Diagram

Fig. 10-1 shows a block diagram of the basic circuit.

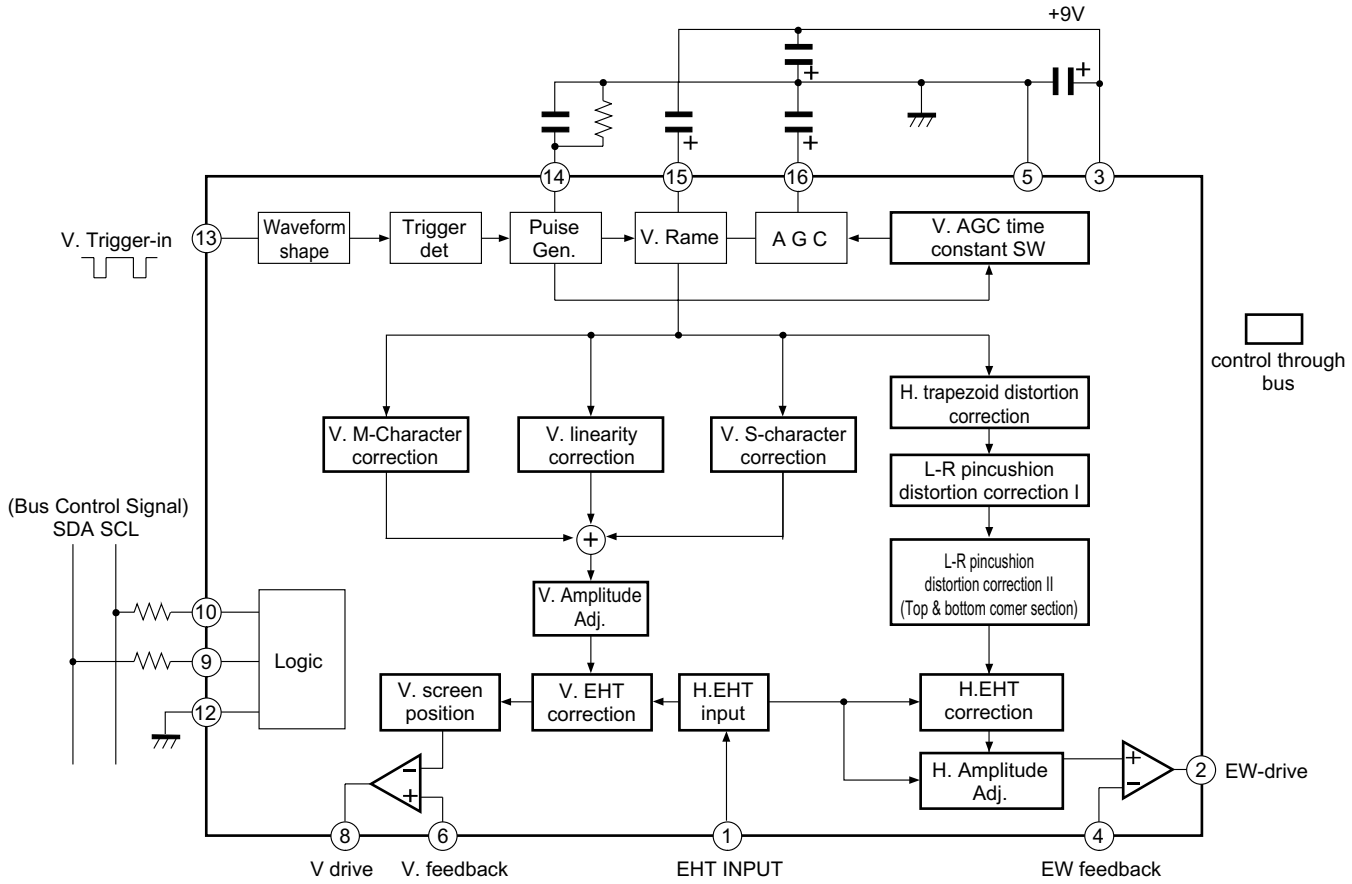


Fig. 10-1

2. DIODE MODULATOR CIRCUIT

In N5SS, the distortion correction is carried out by the ditigal convergence circuit. So the component of the diode modulator circuit is the same as that of conventional television, because it is used only for the horizontal oscillation adjustment.

Fig. 10-2 shows a basic circuit of the diode modulator used in the N5SS.

A key point in the modulation circuit shown in Fig. 10-2 is to develop a negative pulse at point Ⓑ.

In this circuit, a current loop of the resonant circuit for flyback period is shown by an arrow, and the energy stored in L_{DY} is transferred to resonant capacitors Cr, Crm in passing through Cr, Crm, C_S when the scanning completes. As a result, a positive, horizontal pulse as shown in Fig. 10-3 a) will appear at Cr, and the current flows into Crm with the direction as shown. Then a pulse as shown in Fig. 10-3 b) develops at the point Ⓑ.

On the other hand, since constant amplitude pulses across Cr, as shown in Fig. 10-3, are applied to the primary winding, the high voltage of FBT also develops a constant voltage.

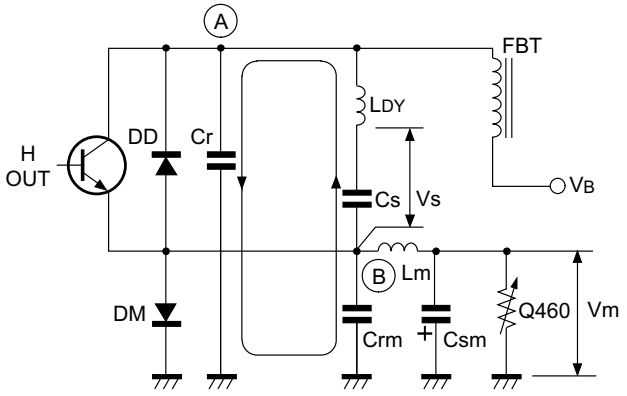


Fig. 10-2

When the negative pulse developed at the point Ⓑ is integrated with Lm and Csm, its average value appears at Csm as a negative voltage.

By modulating this voltage with Q460, a waveform of Vm is obtained as shown in Fig. 10-3 b). As a result, the voltage V_S which is the sum of the power supply voltage V_B and the Vm is applied across the S-curve capacitor C_S. The V_S becomes as a power source for the deflection yoke as shown in Fig. 10-4, is applied to the horizontal deflection yoke.

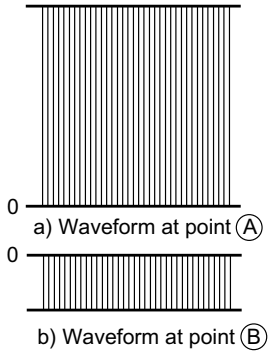


Fig. 10-3

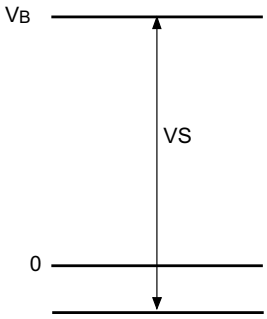


Fig. 10-4

3. ACTUAL CIRCUIT

In the actual circuit, the resonant capacitor is split into two as shown in Fig. 10-7. One, C440, is inserted between the collector of the H. OUT transistor and ground and another C444 inserted between the collector and emitter. In Fig. 10-5, C440 is expressed as C_1 and C444 as C_2, and the resonant current path for the flyback period is shown by arrows.

In a conventional circuit, when brightness of a picture tube varies, high voltage current varies and the high voltage also varies. As a result, horizontal amplitude also varies.

However, in this circuit, the horizontal amplitude variation can be suppressed to near zero if the high voltage current varies with variation of the high voltage.

When the scanning period completes, the energy stored in the deflection yoke L_{DY} is transferred to the resonant capacitor in a form of current I_Y. In this case, the current is split into two; I_{Y1} passing through C_1, C_3 and I_{Y2} passing through C_2. In the same way, the energy stored in the primary winding of the FBT is transferred to the resonant capacitor in the form of I_P. In this case, the current (path) is also split into two; I_{P1} passing through C_1 and I_{P2} passing through C_2, C_3. Concequently, the current differences between I_{Y1} and I_{P2} (I_{Y1}-I_{P2}) passes through C_3.

When the high voltage current I_H reduces with a dark picture, the current I_P in the primary circuit decreases, so I_{P1} and I_{P2} also decrease. However, a current flowing into (I_{Y1}-I_{P2}) increases as I_{P2} decreases. As a result, the pulse developing at the point Ⓑ increases and the voltage Vm at Csm also increases as shown in Fig. 10-8. That is, when a dark picture appears, the voltage across S-curve capacitor C_S increases as shown in Fig. 10-8, the high voltage rises, and the horizontal amplitude is going to decrease. But, as V_S increases, the deflection yoke current increases and this works to increase the horizontal amplitude. Accordingly, if the brightness of picture changes, the horizontal amplitude is maintained at a constant value. This is one of the fine features the circuit has.

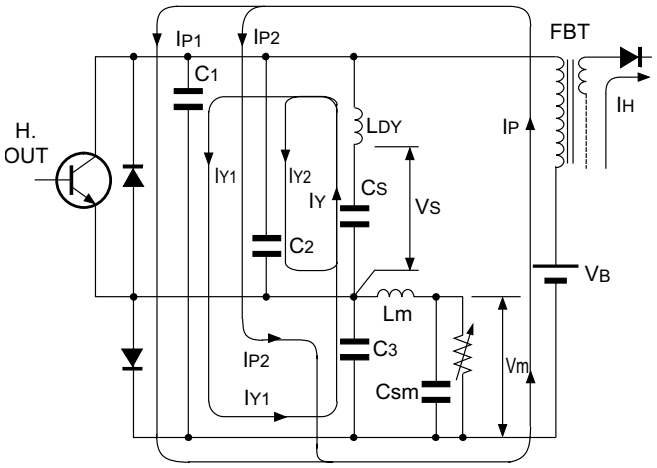


Fig. 10-5

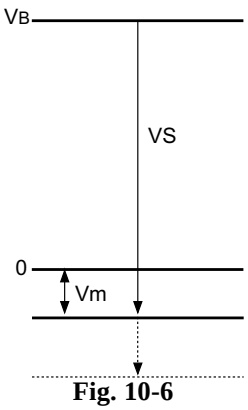


Fig. 10-6

3-1. Basic Operation and Current Path

3-1-1. Later Half Scanning Period

When the power is turned on, the power supply voltage V_B is applied to C_S and Csm, and the C_S acts as a power source for a later half of the scanning period for which the H. OUT transistor is turned on, and the deflection current I_Y flows in the path as shown below.

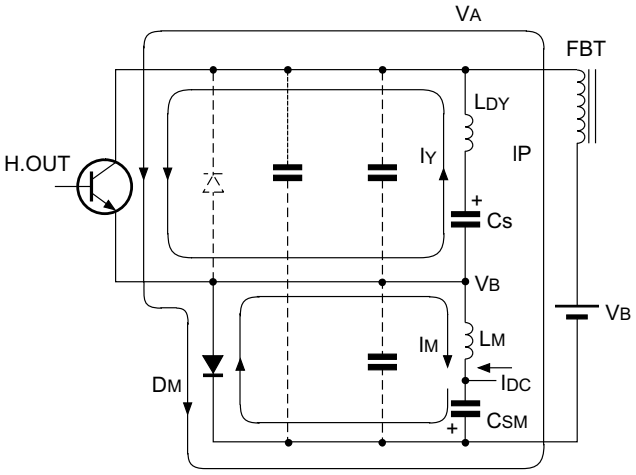


Fig. 10-7

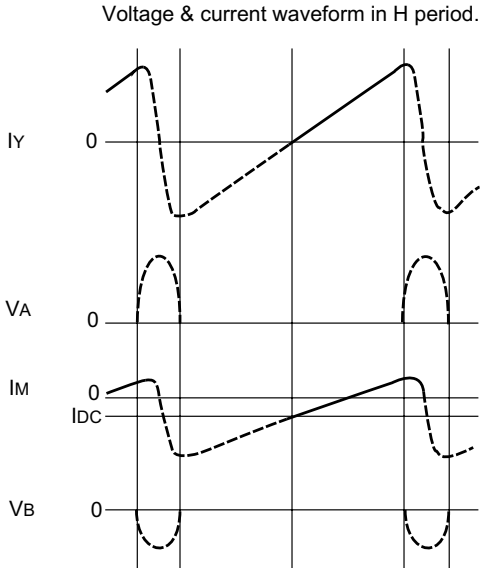


Fig. 10-8

3-1-2. First Half Scanning Period

When the base drive current decreases and the H. OUT transistor is turned off, each energy stored in L_{DY}, Lm, L_P of FTB is transferred to C_1, C_2 and C_3, respectively, and the resonant current becomes zero at a center of the flyback period. Then, V_A and V_B pulses show a maximum amplitude.

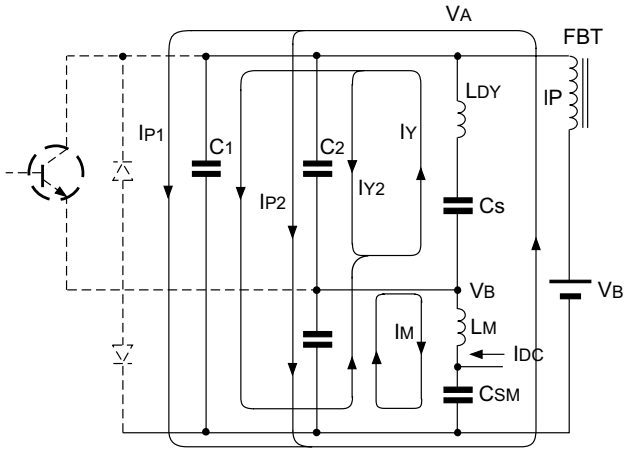


Fig. 10-9

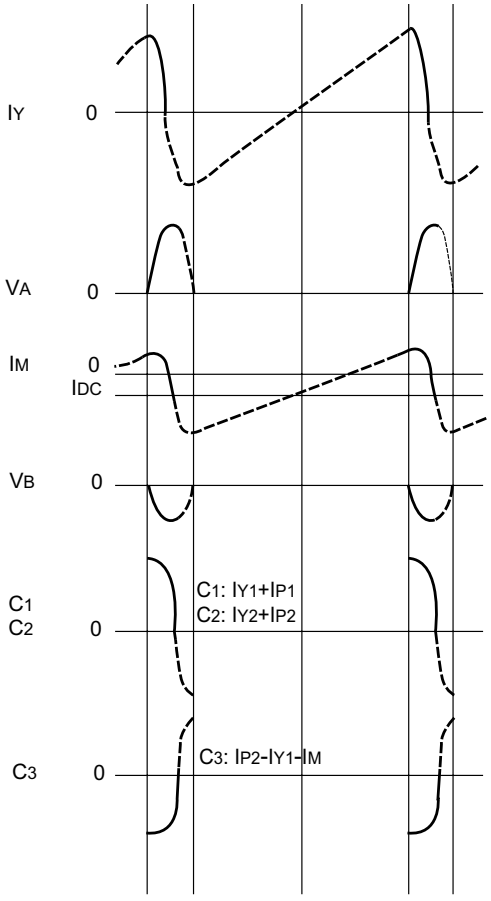


Fig. 10-10

3-1-3. Later Half of Flyback Period

All energy in the coil has been transferred to the resonant capacitors at the center of the flyback period, and the voltage shows the maximum value. However, during next half of the flyback period, the energy of the resonat capacitor is discharged as a reverse current through respective coil. When the discharge has been completed, V_A and V_B becomes zero, and the deflection current in reverse direction becomes the maximum.

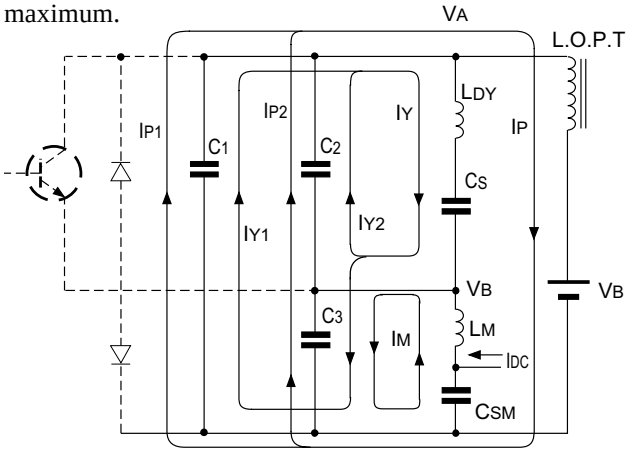


Fig. 10-11

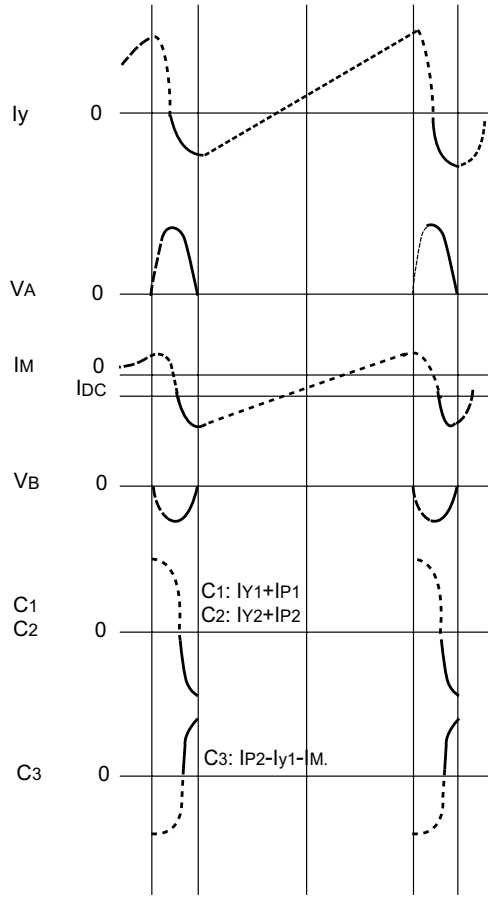


Fig. 10-12

3-1-4. First Half of Scanning Period

When the flyback period completes, the damper diode D_D and the modulation diode D_M turn on, and the I_Y and I_M proportionally decrease from the maximum value to zero. The H. OUT transistor is turned on just preceding at the center of the scanning period, and repeats the steps 3-1-1 through 3-1-4 stated above.

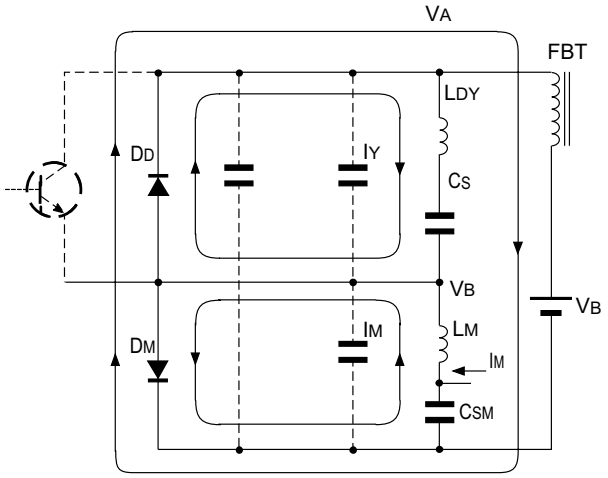


Fig. 10-13

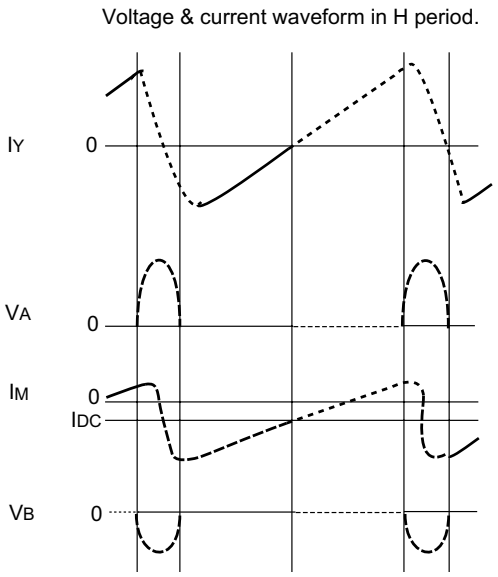


Fig. 10-14

SECTION XI: DIGITAL CONVERGENCE CIRCUIT

1. OUTLINE

The digital convergence circuit develops outputs to correct screen distortion and perform color matching. The digital convergence circuit used is of an all digital type and allows good adjustments in comprise with a conventional analog type circuit.

Followings are features of the digital convergence circuit.

1) No adjustment controls (volumes)
2) Registration accuracy increased.
3) Space saved
4) Adjustment by a remote control

The data adjusted are classed into 4 screens for each screen mode. These data are stored on E^2PROMs inside the unit. The memory size used in this case is 4 Kbits per one screen.

Each screen adjustment is carried out by calling the adjustment screen with the remote control unit supplied and the adjustment is carried out according to the dimensions specified for each screen. The control of the unit is carried out in the I^2C format.

2. CIRCUIT DESCRIPTION

2-1. Configuration

Fig. 11-1 shows a block diagram. The digital convergence unit consists of Q701 T7K64 which plays a major role, Q707 PLL circuit which locks a sync entered, Q713 E^2PROM to store the data, and Q703-5 D/A converter which develops a correction wave form.

The output signal from the Q703 – 705 D/A converter is amplified and wave form shaped by Q715, Q717 and Q719, and comes out from the unit.

The clock signal for the PLL is adjusted by L719 to a reference frequency of 32 ± 0.1MHz under no input status.

A test pattern generator is also built inside Q701 and develops R, G, B signals and a Ys switching signal.

2-2. Circuit Description

(1) With the power turned on, the unit is reset and enters an operation standby status. And a sync signal of the unit enters external Q707 and Q701. The signal entered Q707 is counted down by a counter inside the Q701 and this is used as the reference clock. Q701 works in synchronization with the reference clock signal and the sync signal.

(2) A command is sent from the microcomputer in the unit and Q701 is set up to load the data in Q713 to the internal RAM. (8 (horizontal) x 7 (vertical) x 3 (color))

(3) Q701 transfers a serial data specified to Q703 – 705 according to the RAM data. In this case, interpolation for the RAM data is automatically carried out by a built -in digital filter inside Q701.

(4) The serial data sent from Q701 are digital-analog converted by Q703 – 705, thus developing the analog type wave form.

(5) The signals sent from Q703 – 705 are amplified Q715, Q717, Q719, respectively, and then filtered in the next stage to smooth and shape the wave form. Thus processed signals are used as H and V correction wave forms for R, G, and B signals.

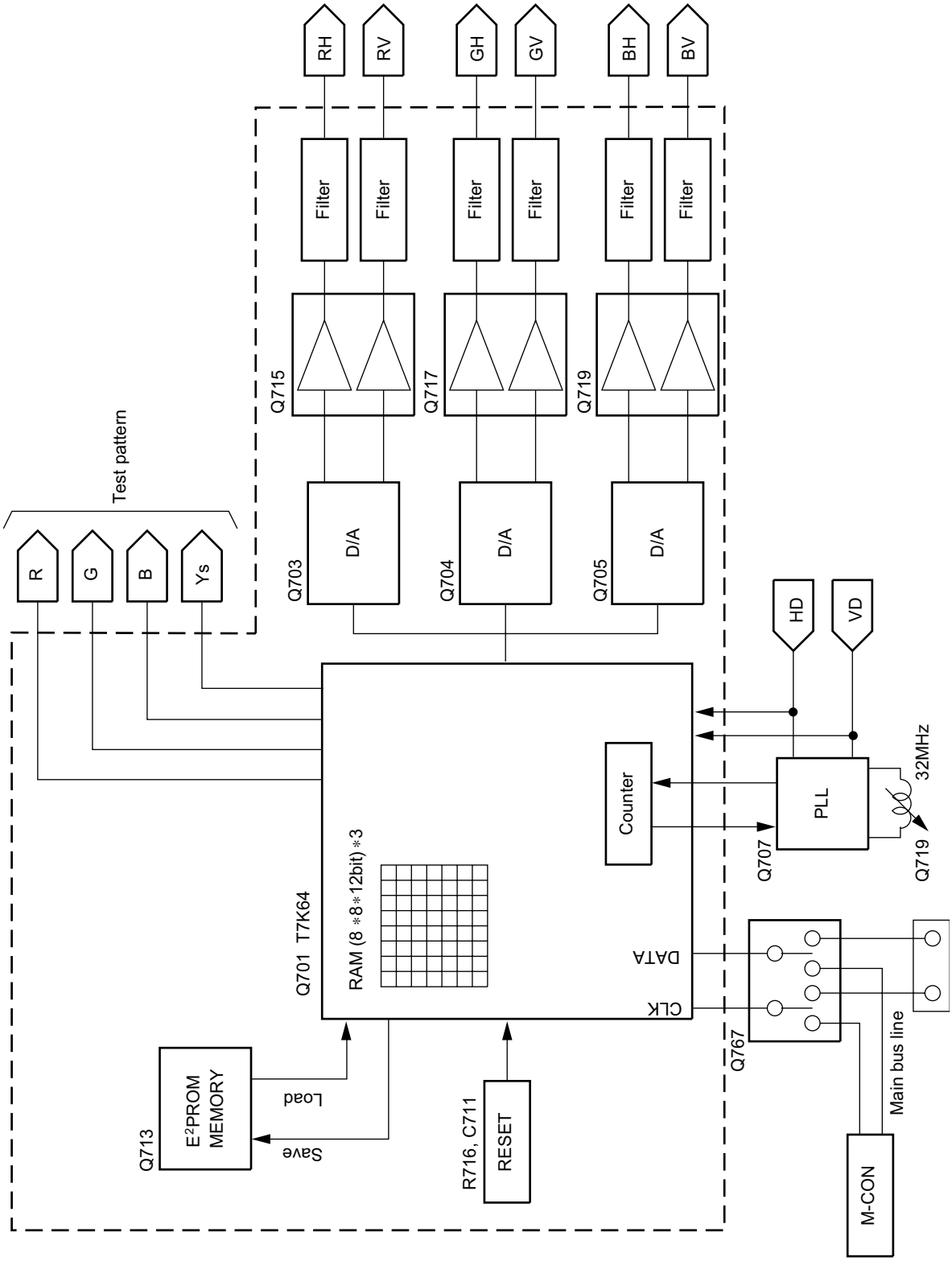


Fig. 11-1 Block diagram

3. PICTURE ADJUSTMENT

Four screens for Normal/Full, Theater wide 1, Theater Wide 2, Theater Wide 3 are provided for the adjustments. When making the adjustments, receive the U/VHF or CABLE broadcasting signal or the built-in pattern signal of the microprocessor to make a synchronization with the frequency of the adjusting screen with the unit..

This adjustment program is prepared as the microprocessor function of the set and it is possible to adjust by the remote controller attached.

3-1. Outline of the Modification Process of the Storing Adjustment Data

Set the convergence adjustment screen.

The adjusted data is stored in the memory inside Q713 E^2CPROM which is a non-volatile memory.

The RAM data inside Q701 is lost when the power turns off. So the initial operation status is set by the software command from the microprocessor QA01 every time when the unit turns on.

The data adjusted manually through the screen by displaying the adjusting screen on the display is once written on RAM inside Q701. Adjust each adjusting point and store the modified total data on RAM as correct one into Q713 E^2PROM.

The adjustment is carried out for each screen mode, and its order is as follows; Normal/Full ® Theater Wide 1 ® theater Wide 2 ® Theater Wide 3. (When the adjustment value is saved after adjusting Normal/Full, the microprocessor calculates the adjustment values for Theater Wide 1, 2 and 3 based on the adjustment value of Normal/Full mode and sets the values for Theater Wide 1, 2 and 3 to the closed values to require minimum adjustment.)

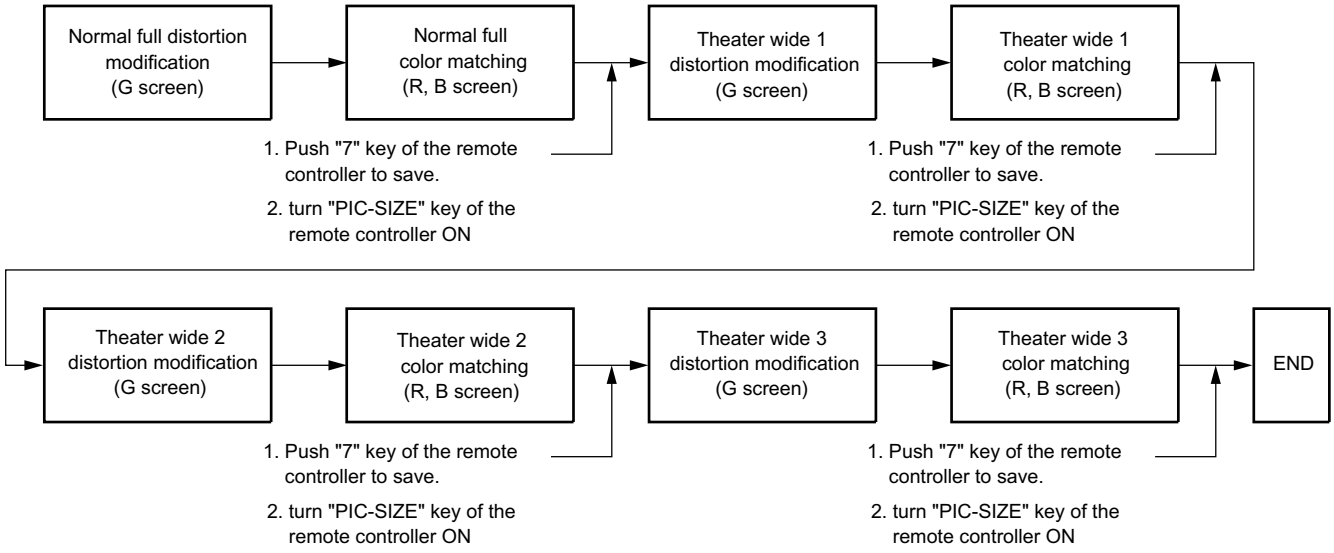


Fig. 11-2

3-2. Service Mode

3-2-1. Outline

The service mode, one of the functions this unit provides, is controlled by the microprocessor QA01 and .

This mode is set by the special operation to avoid the easy operation by the user. Move the cursor to between the adjustment points of 8*7/each color and modify the data directly. Before entering the service mode, perform the center adjustment using the color unmatching adjustment in the user menu.

3-2-2. Entering/Exiting Mode

When the “MUTE” key on the remote controller is pressed, the screen display appears. Pushing the “MUTE” key again disappears the screen display.

In this status, when the “MENU” key on the set console is pushed while pushing the “MUTE” key, S is displayed on the upper right of the screen. When the “MENU” key is pressed again, the service data is displayed on the upper left on the screen.

When “7” key on the remote controller is pressed in this status, the screen changes to display the cross hatch screen (the first screen described later) and the convergence adjustment screen appears.

When “7” key is pressed again, the data storing operation is automatically carried out and the cross hatch + data display screen (the second screen described later) appears.

When “7” key is pressed furthermore, the display returns to the initial screen.

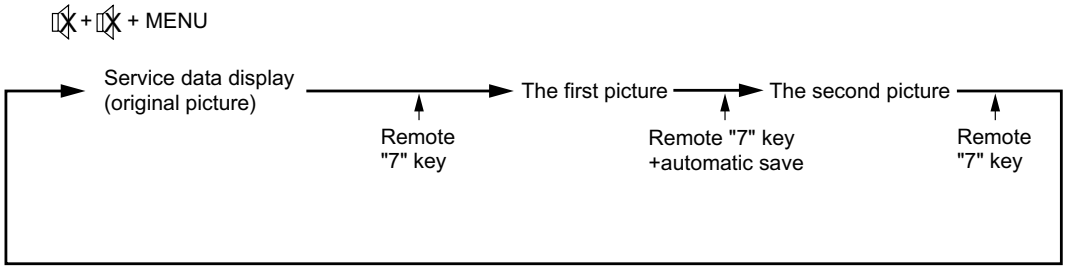


Fig. 11-3

Note:

When changing the convergence correction data, always be sure to perform the automatic storing operation. If the power turns off without carrying out the automatic storing operation, the modified data is lost.

3-2-3. Initial screen

The screen mode is Normal/Full screen mode.

Correction point: Vertical 8 * Horizontal 7 (® and - marks are the adjusting points.)

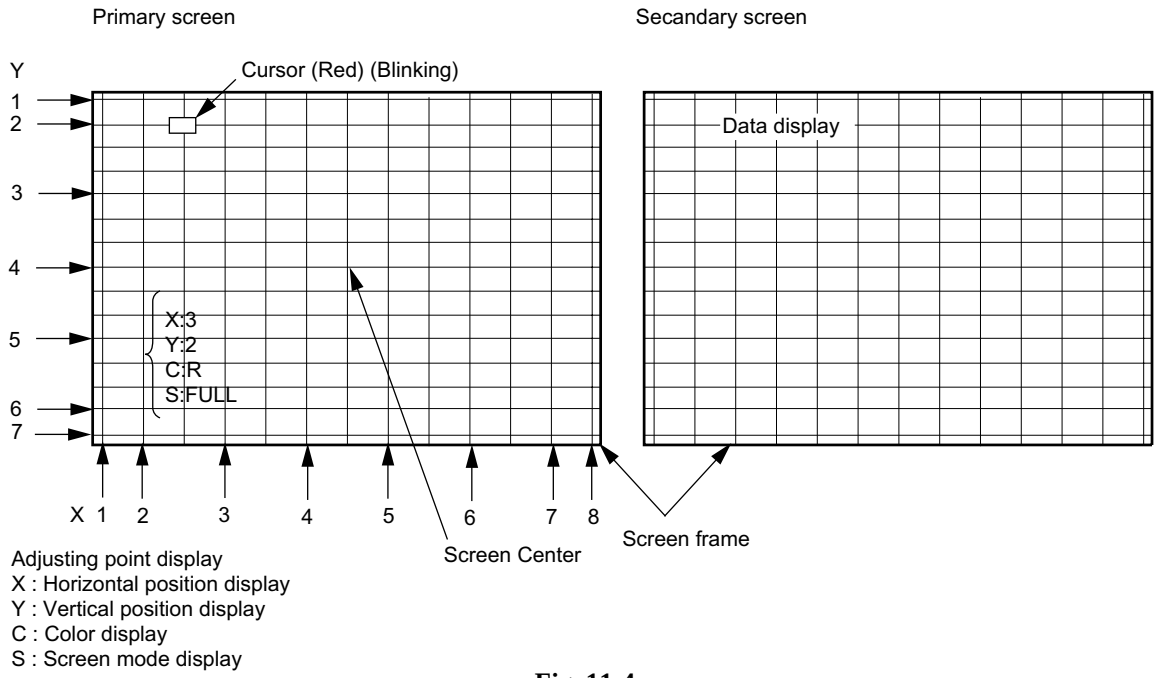


Fig. 11-4

(1) First screen:

The initial cross hatch screen appears. The pattern colors are displayed with 3 colors. The cursor color is red and left blinking.

When the modification is carried out, the last memory status is displayed.

Cursor mode:

Lighting: Data modification mode

Blinking: Cursor move mode

The display color shows the color which can modify the data.

(2) Second screen

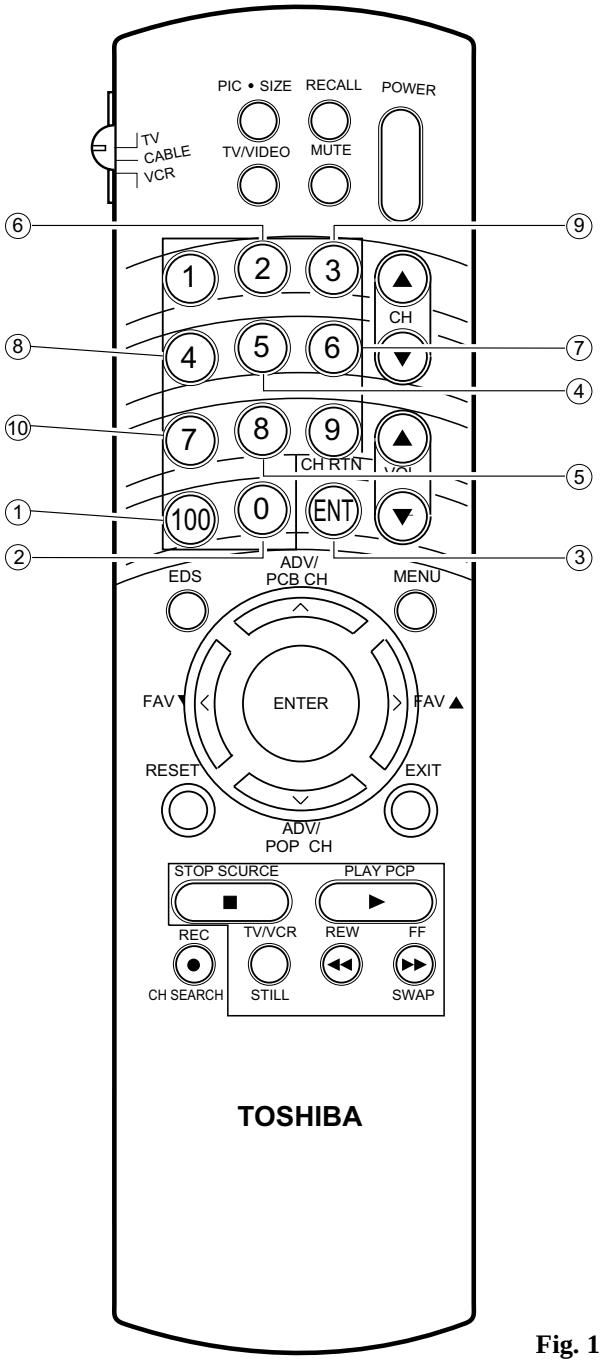
When changing from the first screen to second screen, the convergence correction waveform is mute for 1 second. The modified data for this period is sent to Q713 E^2PROM from Q071 RAM and then stored.

The second screen is displayed upper left of the first screen, so the convergence adjustment cannot be carried out when the second screen is displayed.

Note:

- The adjusted data is automatically stored when the display changes from the first screen to the second screen. So be sure to perform this operation after adjustment completes.
- Adjustment should be carried out with a corresponding signal received.

3-2-4. Key function of remote control unit



① 100 Key ..... Red test pattern ON/OFF
② 0 Key ..... Green test pattern ON/OFF
③ ENT Key ..... Blue test pattern ON/OFF
④ 5 Key ..... Cursor shift/data change mode chang over
⑤ 8 Key ..... Cursor down/adjusting point down
⑥ 2 Key ..... Cursor UP/adjusting point UP
⑦ 6 Key ..... Cursor right/adjusting point right
⑧ 4 Key ..... Cursor left/adjusting point left
⑨ 3 Key ..... Cursor color change
⑩ 7 Key ..... Data save

Fig. 11-5

3-2-5. Operation procedure

(1) Set the screen to Normal or Full mode using the PIC-SIZE key on the remote controller.

(2) Set the unit to the service mode with MUTE + MUTE + MENU keys pressed. (Entering to S mode.)

(3) Set the unit to the convergence adjusting mode by pressing the “7” key on the remote controller. (Fist screen)

(4) Select the pattern to display by pressing 100, 0, ENT on the remote controller.

(Red adjustment; 100 ... ON, 0 ... ON, ENT... OFF)

(Green adjustment; 100 ... OFF, 0 ... ON, ENT... ON)

(Blue adjustment; 100 ... ON, 0 ... OFF, ENT... ON)

(5) Select the color to adjust by pressing “3” key on the remote controller.

(6) Confirm that the cursor is in the movable status (the cursor blinking status).

(7) Select the adjusting position by pressing “8”, “4” and “6”.

(8) When the adjusting position is determined, press “5” key on the remote controller to enter the cursor blinking status.

(9) Set the cursor to the adjusting position by pressing “2”, “8”, “4” and “6”, and perform the pattern distortion correction and color matching adjustments.

(10) Press “5” key again and move the cursor. Perform the adjustment in the same way as described above.

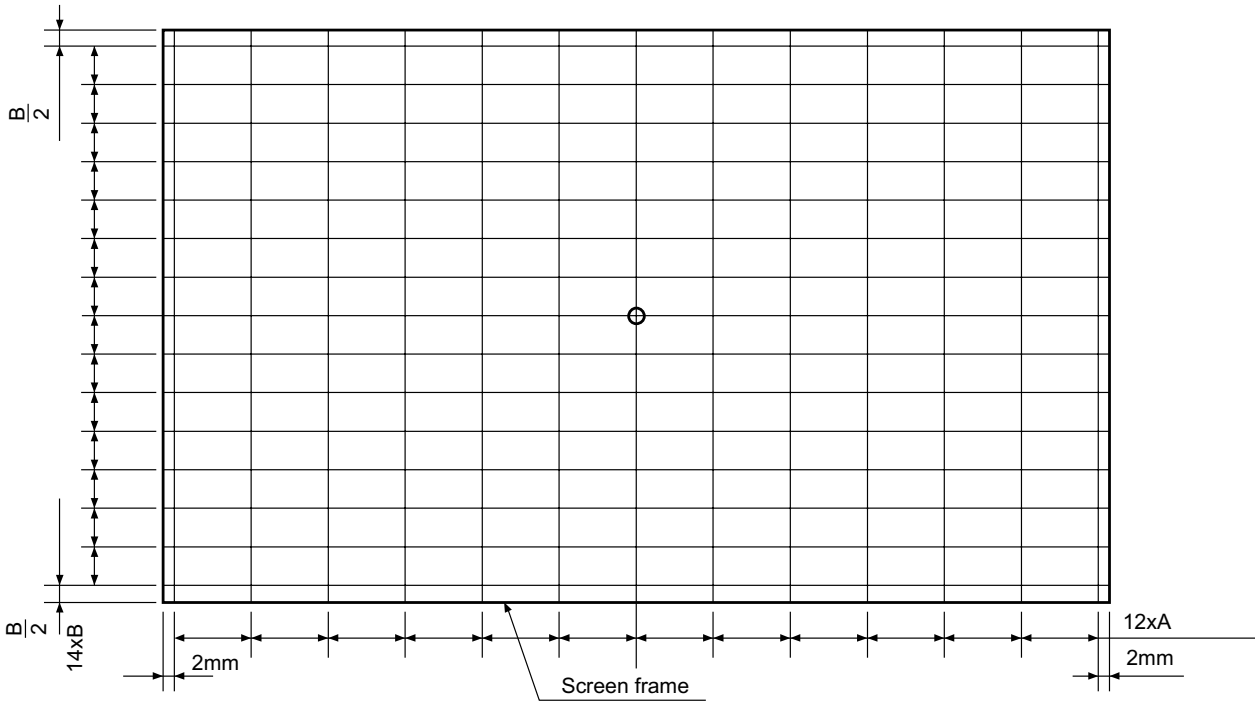
(11) After the adjustment completes, perform the automatic storing operation by pressing “7” key.

(12) In the same way as described above, adjust WIDE 1, WIDE 2 and WIDE 3 screens using PIC-SIZE key.

(13) When all of the screen mode adjustment complete, perform the automatic storing operation by pressing “7” key.

3-3. Each Screen Adjustment Method

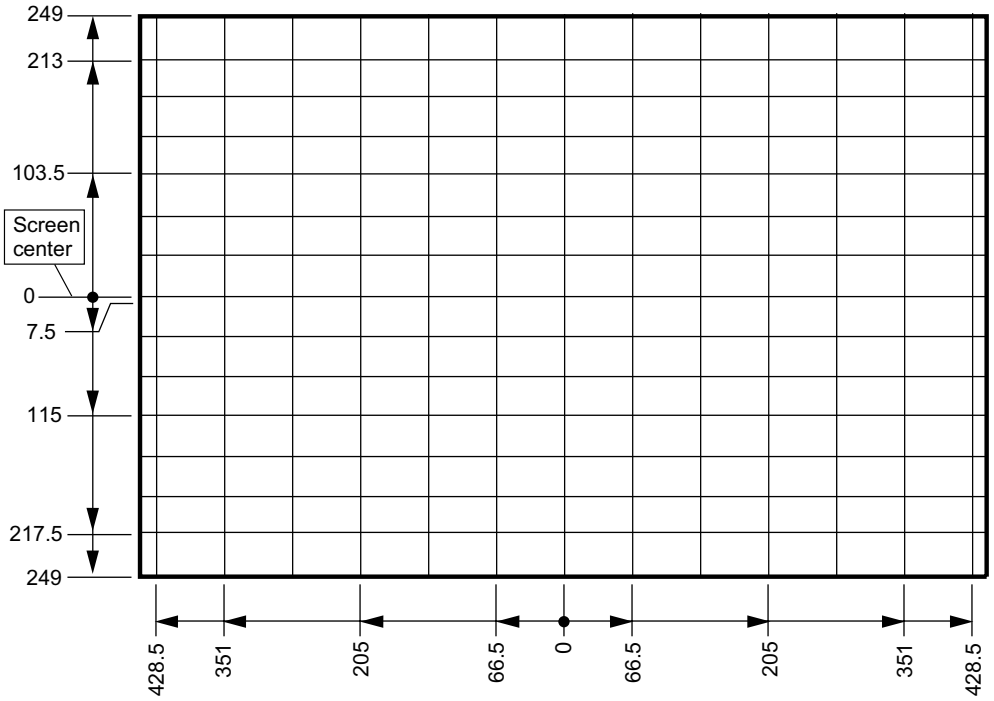
3-3-1. Normal/Full



40 inches 16:9 Screen size: Horizontal 885mm x Vertical 498mm
Dimension A: 73.5mm Dimension B: 33.2mm

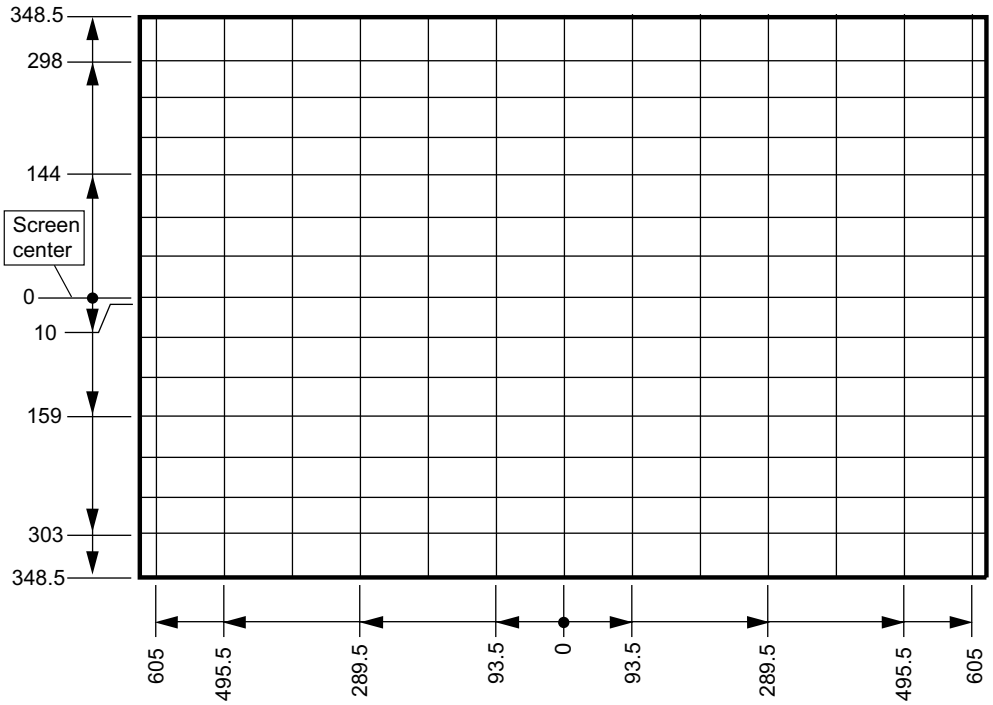
Fig. 11-6

3-3-2. Theater Wide1



40 inches 16:9 Screen size: Horizontal 885mm x Vertical 498mm

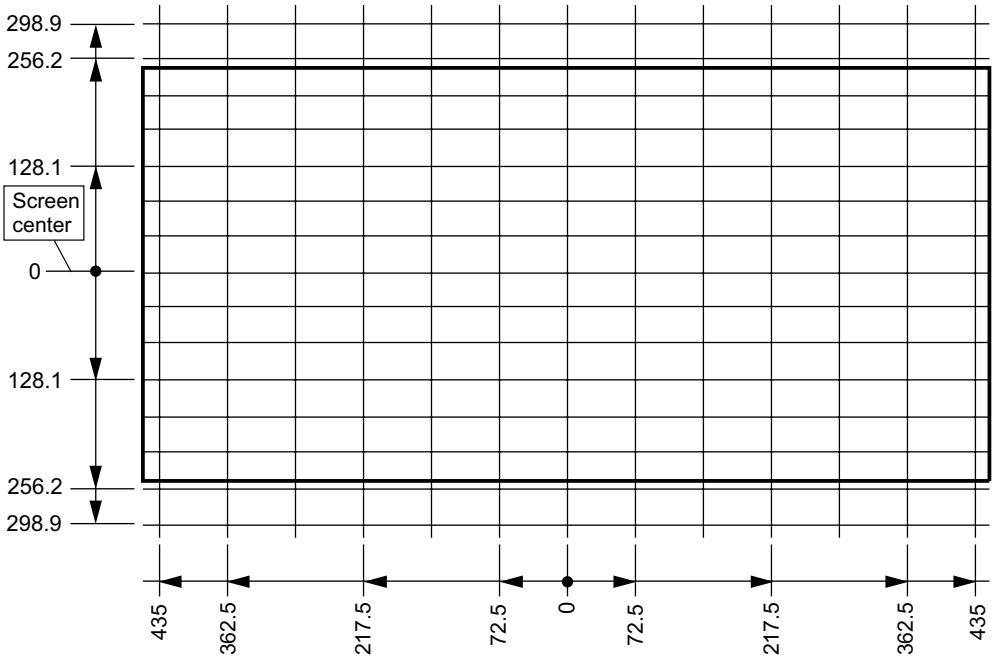
Fig. 11-7



56 inches 16:9 Screen size: Horizontal 1239mm x Vertical 697mm

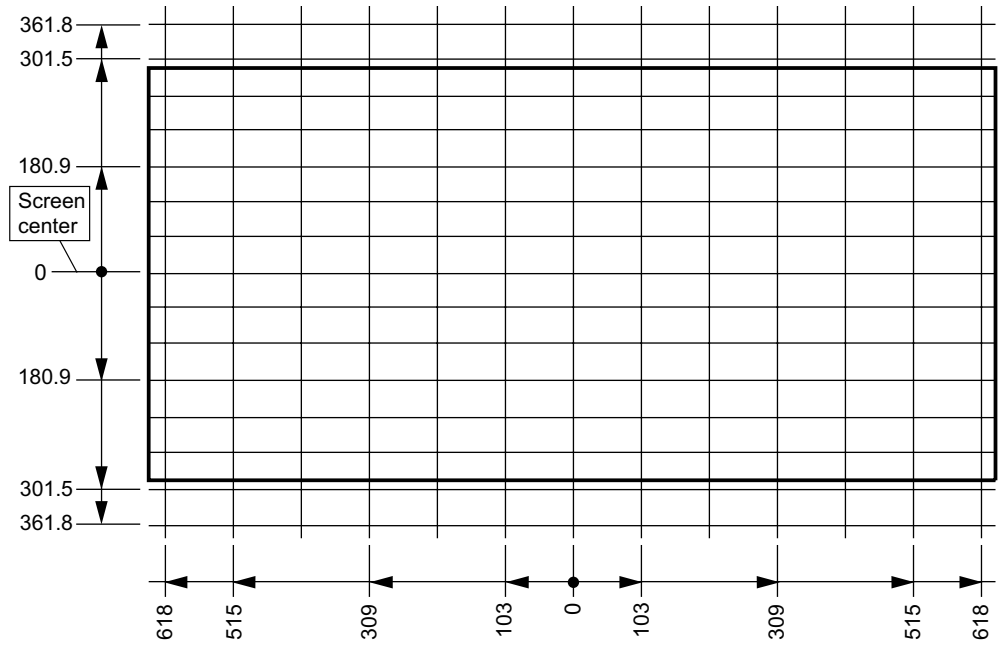
Fig. 11-8

3-3-3. Theater Wide 2



40 inches 16:9 Screen size: Horizontal 885mm x Vertical 498mm

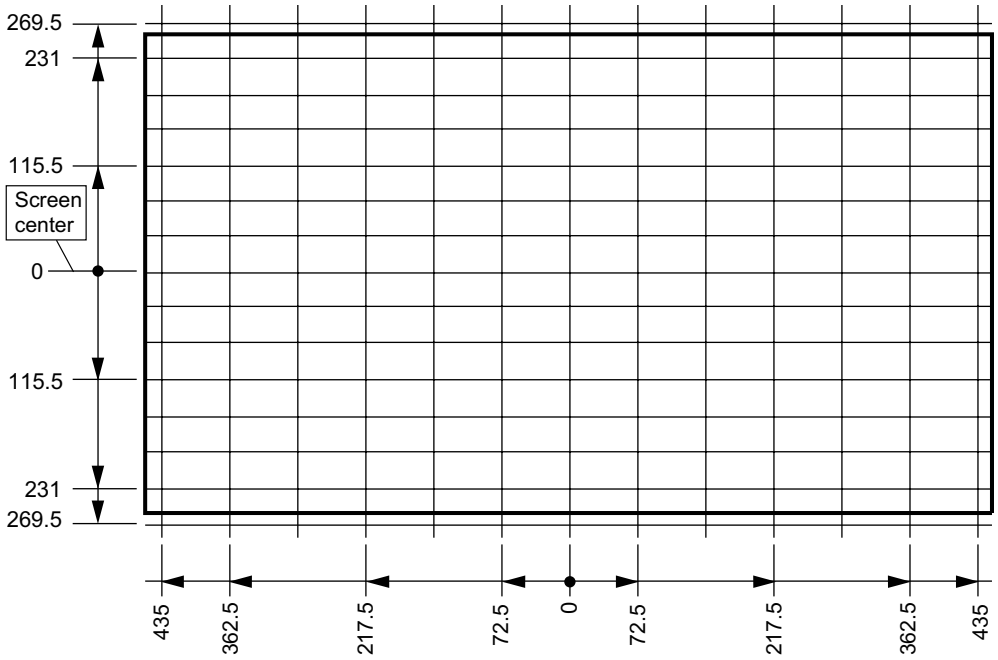
Fig. 11-9



56 inches 16:9 Screen size: Horizontal 1239mm x Vertical 697mm

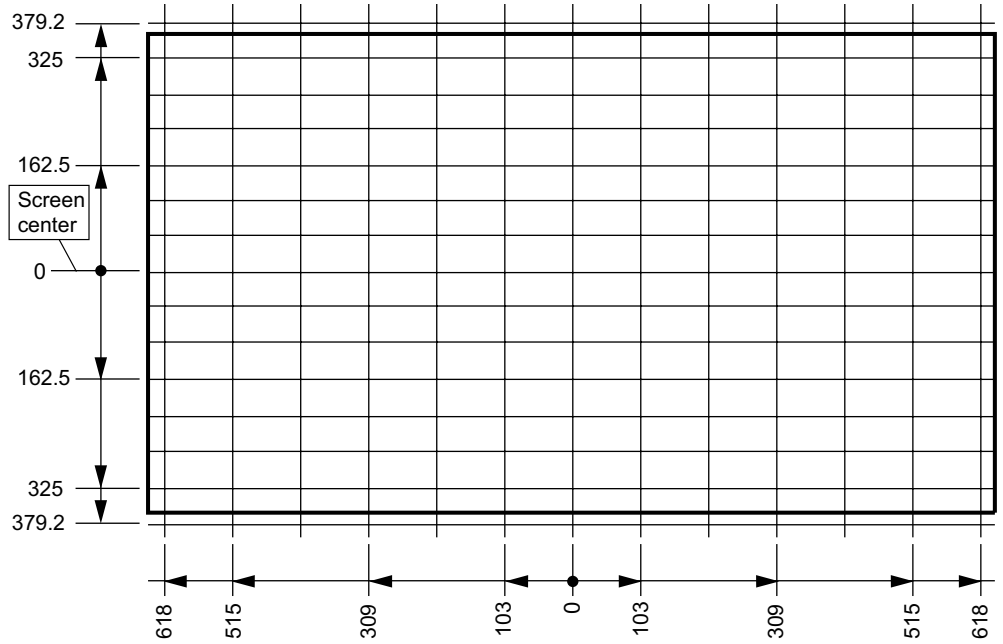
Fig. 11-10

3-3-4. Theater Wide 3



40 inches 16:9 Screen size: Horizontal 885mm x Vertical 498mm

Fig. 11-11



56 inches 16:9 Screen size: Horizontal 1239mm x Vertical 697mm

Fig. 11-12

4. CASE STUDY

In many cases, a color deviation will be corrected by returning the HIT and WID data for the main deflection side to the initial values.

Followings are cases which need readjustment of the convergence by all means.

4-1. When CRT is Replaced.

When the CRT is replaced, readjustment of the main deflection and color matching will be necessary. Perform the adjustments as follows.

(1) Replace two CRTs, blue and red.

(2) Perform horizontal adjustments for blue and red yokes to the green CRT. Mount the yokes and velocity modulation coils + alignments so that they closely touches the CRT without any clearance.

(3) Adjust the red and blue alignments. (refer to item Detailed adjustments for alignments)

(4) Perform the center adjustment for the blue CRT center and the red CRT center to the green CRT center with the centering magnets.

(5) Adjust the HIT, WID data to obtain the data which gives the most precision to the green.

(6) Perform the color matching in terms of the convergence for each screen. In this case, do not move the green.

(7) After completion of the convergence adjustment for each screen, replace the green CRT. For the green CRT, repeat the steps 2-5 to make the color matching in terms of the convergence by using the red and blue as the reference.

4-2. When Convergence Unit is Replaced

When replacing the convergence units, all screens must be adjusted basically. However, performing the adjustment as shown below will reduce the procedures considerably.

(1) Replace the memory (Q713) for the new unit with the memory (Q713) for the failure unit. Mount the convergence unit on the set and the screen status before replacement will be directly reproduced.

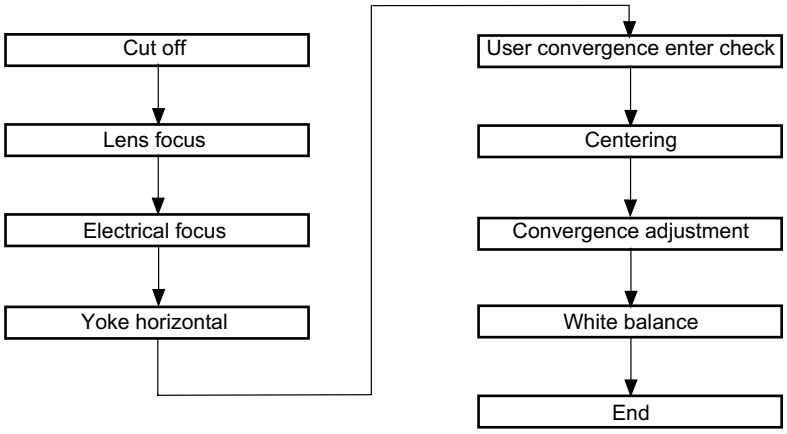
(2) Mount the new unit with the old memory installed in combination on the set, and turn on the set. A screen as if it is moving vertically or horizontally will appear.

(3) Adjust each center of green, red, and blue with the centering magnets again.

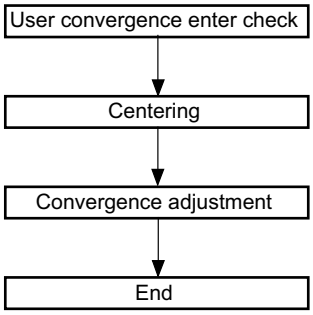
(4) Check to see color deviation and screen size deviation among the colors. If deviated, perform the adjustment for the main deflection and the color matching for the convergence.

5. TROUBLESHOOTING

5-1. Adjusting Procedure in Replacing CRT



5-2. Adjusting Procedure in Replacing Convergence Unit/Main Def



6. CONVERGENCE OUTPUT CIRCUIT

6-1. Outline

This circuit current-amplifies digital convergence correction signal at output circuit, and drives by convergence yoke to perform picture adjustment.

Digital convergence output signal 6ch adjustment is done.

(H-R/G/B) (V-R/G/B)

6-2. Circuit Description

6-2-1. Signal flow

Signal which is corrected by digital convergence, is output to P708 (V, H R/G/B);

is input to Q751 (V) R/G/B, and is output to P713, P714 and P715;

is input to Q752 (H) R/G/B, and is output to P713, P714 and P715.

6-2-2. Over current protection circuit

All currents of Power supply, -15V, +15V and +30V are detected to protect CONV-OUT IC from damage due to output short of CONV-OUT.

Current value: Normal ± 15V approx. 700mA

+30V approx. 200mA

Detecting curren ±15V approx. 1.8A or more

+30V approx. 700mA or more protecting operation

6-2-3. Pump-up source

CONV-OUT IC Q752 (H)

Pin 10 (+15V/H, PV)

Pin 5 (+30V)

By HD input signal, pump-up is done only in horizontal retracing time.

6-2-4. CONV-OUT mute

In power-on operation, transistors Q765 and Q766 are made turned ON, and –15V is applied to pin 3 of CONV-OUT IC. These cause mute operation on CONV-OUT.

6-2-5. Operation of IC

1) Q764 (TC74HC4050AP)

Sync signal which is input from P711 1 VD, 2 HD, is, through buffer, supplied to digital convergence P708.

2) 3-terminal source

Q754 (+5V) Q755 (+9V) Q756 (-9V)

Source for digital convergence

3) Q767 (TC4066BP)

P711 4 SDAM, 5 SCLM : microcomputer. Busline, through Q767, is input to Digital Convergence P709, and is controlled.

4) To adjust from outside of digital convergence :

Put adjusting jig into 6P socket of P720. Iscs turns from H to L, switch of Q767 is changed over. Then busline from microcomputer is cut off.

P720 3 SCLU, 4 SDAU

Controlled by external adjusting jig.

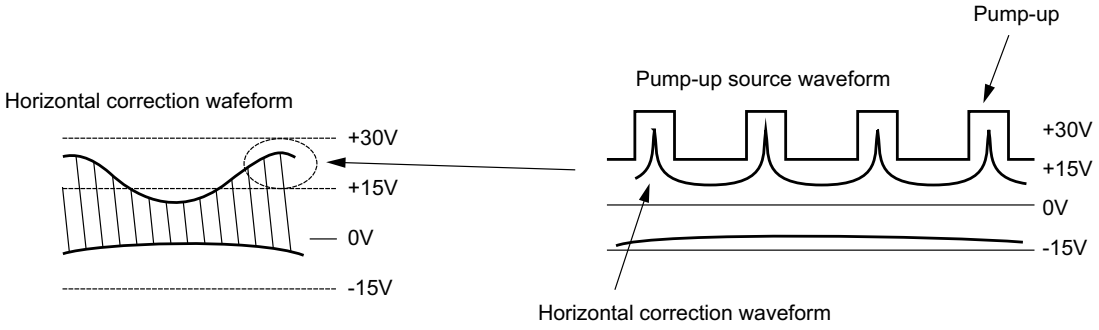


Fig. 11-13

6-3. Convergence Block Diagram

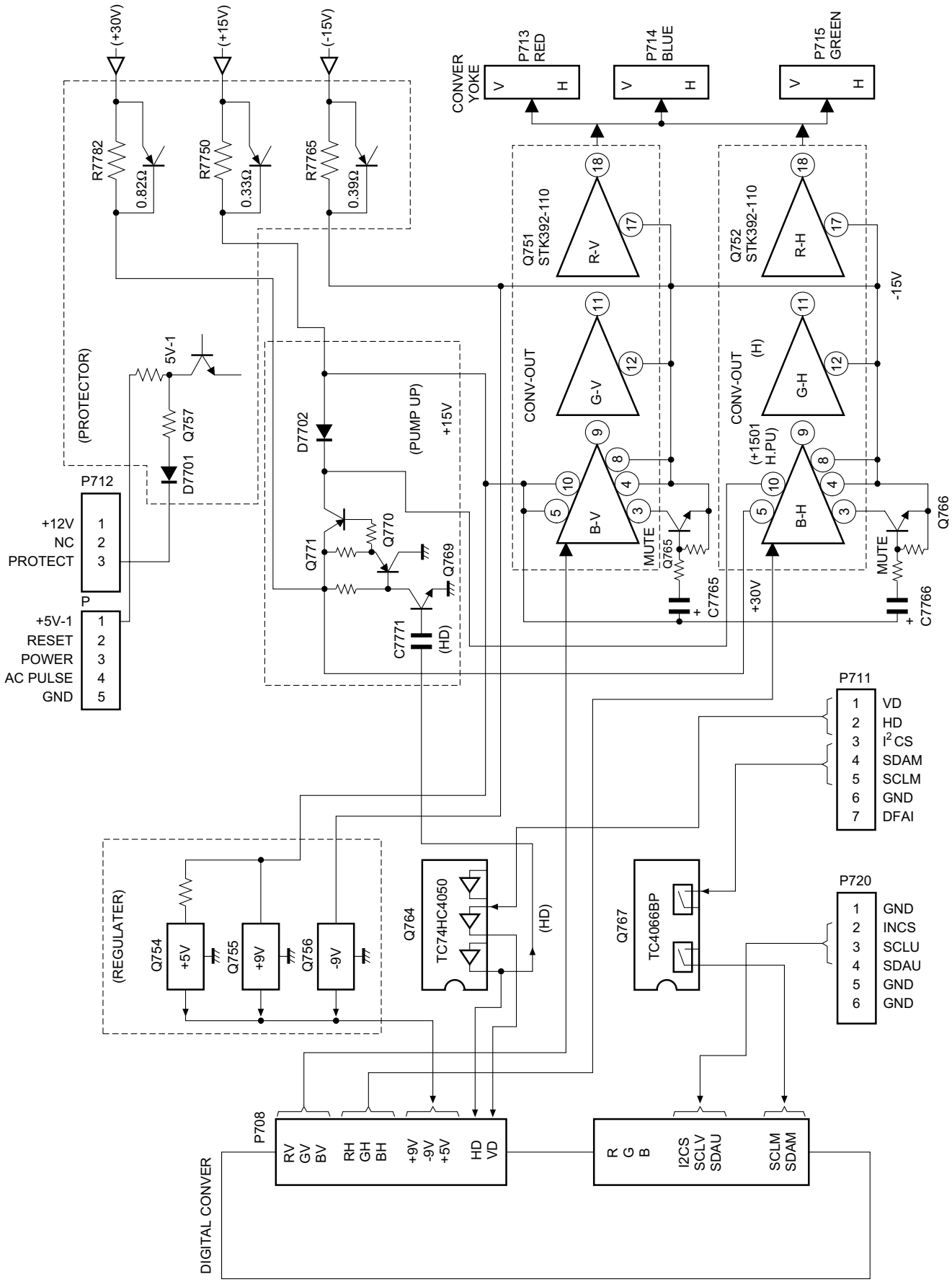


Fig. 11-14

7. CONVERGENCE TROUBLESHOOTING CHART

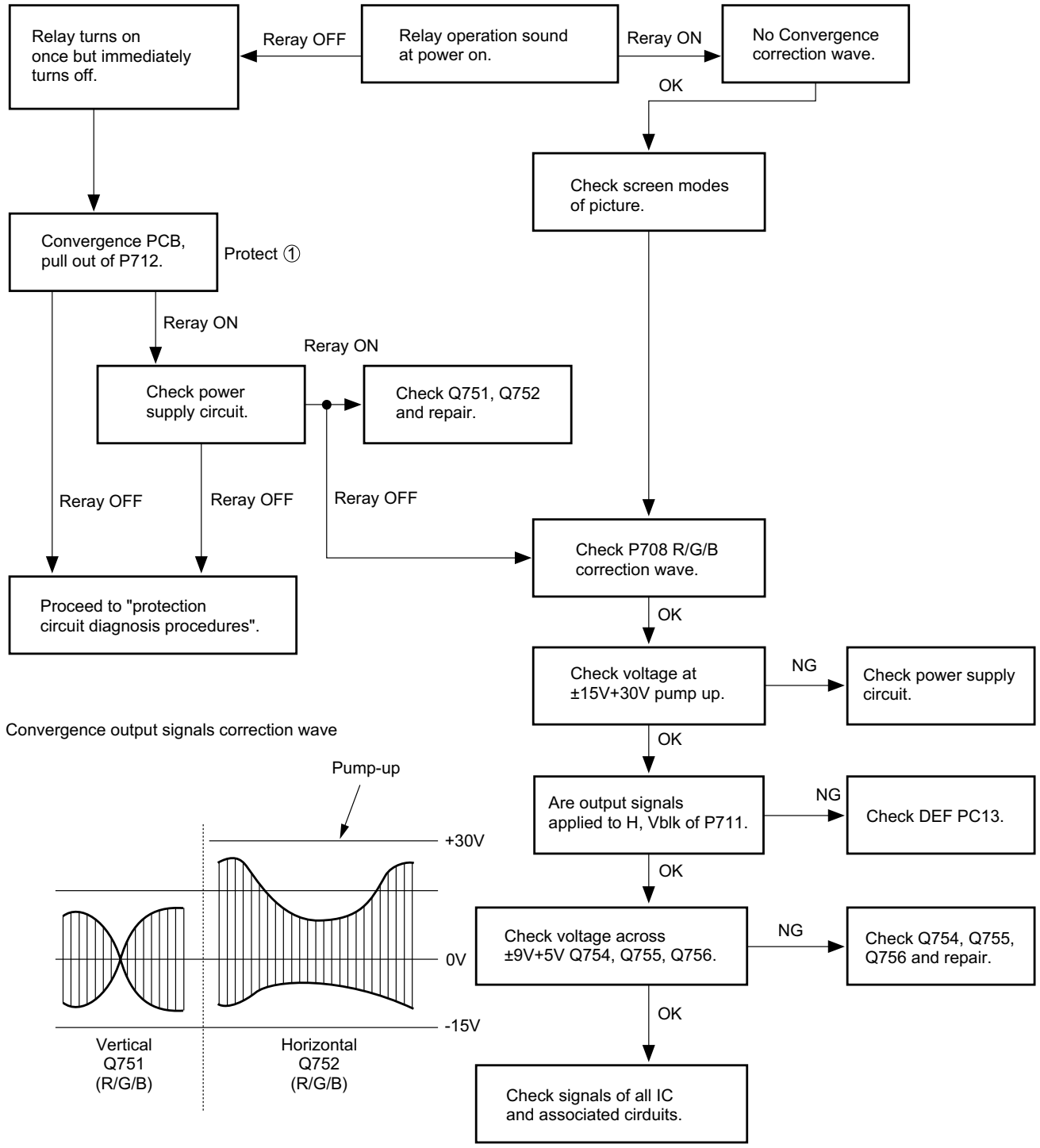


Fig. 11-6