COMPAQ

# Technical Reference Guide

*For the*

# Compaq iPAQ Internet Device

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COMPAQ iPAQ Internet Device

***TRG***

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***Technical Reference Guide***
*For the*
**Compaq iPAQ Internet Device**

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# Chapter 1
# INTRODUCTION

## 1.1 ABOUT THIS GUIDE

This guide provides technical information about the Compaq iPAQ Family of Internet Devices. This document includes information regarding system design, function, and features that can be used by programmers, engineers, technicians, and system administrators.

This guide and any applicable addendum are available online at the following location:

http://www.compaq.com/support/techpubs/technical_reference_guides/index.html

### 1.1.1 USING THIS GUIDE

The chapters of this guide primarily describe the hardware and firmware elements and primarily deal with the system board and the power supply assembly. The appendices contain general information about standard peripheral devices such as the keyboard.

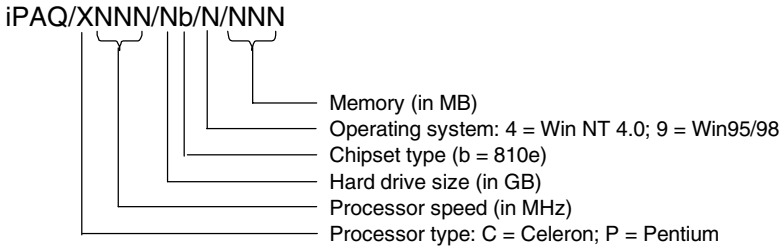
### 1.1.2 ADDITIONAL INFORMATION SOURCES

For more information on chipset components mentioned in this guide refer to the indicated manufacturers' documentation, which may be available at the following online sources:

- Compaq Computer Corporation: http://www.compaq.com
- Intel Corporation: http://www.intel.com
- Standard Microsystems Corporation: http://www.smsc.com

## 1.2 MODEL NUMBERING CONVENTION

The model numbering convention for Compaq iPAQ units is as follows:



## 1.3 NOTATIONAL CONVENTIONS

### 1.3.1 VALUES

Hexadecimal values are indicated by a numerical or alpha-numerical value followed by the letter "h." Binary values are indicated by a value of ones and zeros followed by the letter "b." Numerical values that have no succeeding letter can be assumed to be decimal.

### 1.3.2 RANGES

Ranges or limits for a parameter are shown using the following methods:

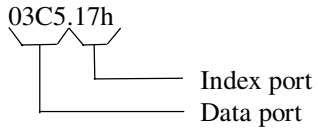
Example A: Bits <7..4> = bits 7, 6, 5, and 4.
Example B: IRQ3-7, 9 = IRQ signals 3 through 7, and IRQ signal 9

### 1.3.3 SIGNAL LABELS

Signal names are indicated using abbreviations, acronyms, or, if possible, the full signal name in all capital letters. Signals that are meant to be active (asserted) low are indicated with a dash immediately following the name.

### 1.3.4 REGISTER NOTATION AND USAGE

This guide uses standard Intel naming conventions in discussing the microprocessor's (CPU) internal registers. Registers that are accessed through programmable I/O using an indexing scheme are indicated using the following format:




In the example above, register 03C5.17h is accessed by writing the index port value 17h to the index address (03C4h), followed by a write to or a read from port 03C5h.

### 1.3.5 BIT NOTATION

Bit values are labeled with bit <0> representing the least-significant bit (LSb) and bit <7> representing the most-significant bit (MSb) of a byte. Bytes, words, double words, and quad words are typically shown with most-significant portions on the left or top and the least-significant portions on the right or bottom respectively.

## 1.4 COMMON ACRONYMS AND ABBREVIATIONS

Table 1-1 lists the acronyms and abbreviations used in this guide.

**Table 1-1.**
Acronyms and Abbreviations

| Acronym/Abbreviation | Description |
|---|---|
| A | ampere |
| AC | alternating current |
| ACPI | Advanced Configuration and Power Interface |
| A/D | analog-to-digital |
| AGP | Accelerated graphics port |
| API | application programming interface |
| APM | advanced power management |
| AOL | Alert-ON-LAN |
| ASIC | application-specific integrated circuit |
| AT | 1) attention (modem commands) 2) 286-based PC architecture |
| ATA | AT attachment (IDE protocol) |
| ATAPI | AT attachment w/packet interface extensions |
| AVI | audio-video interleaved |
| AVGA | Advanced VGA |
| BAT | Basic assurance test |
| BCD | binary-coded decimal |
| BIOS | basic input/output system |
| bis | second/new revision |
| BitBLT | bit block transfer |
| BNC | Bayonet Neill-Concelman (connector) |
| bps or b/s | bits per second |
| BSP | Bootstrap processor |
| BTO | Built to order |
| CAS | column address strobe |
| CD | compact disk |
| CD-ROM | compact disk read-only memory |
| CDS | compact disk system |
| CF | carry flag |
| CGA | color graphics adapter |
| Ch | channel |
| cm | centimeter |
| CMC | cache/memory controller |
| CMOS | complimentary metal-oxide semiconductor (configuration memory) |
| Cntlr | controller |
| Cntrl | control |
| codec | compressor/decompressor |
| CPQ | Compaq |
| CPU | central processing unit |
| CRT | cathode ray tube |
| CSM | Compaq system management / Compaq server management |
| CTO | Configure to order |
| DAA | direct access arrangement |
| DAC | digital-to-analog converter |
| DC | direct current |
| DCH | DOS compatibility hole |
| DDC | Display Data Channel |
| DF | direction flag |

*Continued*

**Table 1-1.** Acronyms and Abbreviations *Continued*

| Acronym/Abbreviation | Description |
|---|---|
| DIMM | dual inline memory module |
| DIN | Deutche IndustriNorm (connector standard) |
| DIP | dual inline package |
| DMA | direct memory access |
| DMI | Desktop management interface |
| dpi | dots per inch |
| DRAM | dynamic random access memory |
| DRQ | data request |
| EDID | extended display identification data |
| EDO | extended data out (RAM type) |
| EEPROM | electrically eraseable PROM |
| EGA | enhanced graphics adapter |
| EIA | Electronic Industry Association |
| EISA | extended ISA |
| EPP | enhanced parallel port |
| EIDE | enhanced IDE |
| ESCD | Extended System Configuration Data (format) |
| EV | Environmental Variable (data) |
| ExCA | Exchangeable Card Architecture |
| FIFO | first in / first out |
| FL | flag (register) |
| FM | frequency modulation |
| FPM | fast page mode (RAM type) |
| FPU | Floating point unit (numeric or math coprocessor) |
| FPS | Frames per second |
| ft | foot |
| GB | gigabyte |
| GMCH | Graphics/memory controller hub |
| GND | ground |
| GPIO | general purpose I/O |
| GPOC | general purpose open-collector |
| GART | Graphics address re-mapping table |
| GUI | graphics user interface |
| h | hexadecimal |
| HW | hardware |
| hex | hexadecimal |
| Hz | hertz |
| ICH | I/O controller hub |
| IDE | integrated drive element |
| IEEE | Institute of Electrical and Electronic Engineers |
| IF | interrupt flag |
| I/F | interface |
| in | inch |
| INT | interrupt |
| I/O | input/output |
| IPL | initial program loader |
| IrDA | InfraRed Data Association |
| IRQ | interrupt request |
| ISA | industry standard architecture |
| JEDEC | Joint Electron Device Engineering Council |
| Kb / KB | kilobits / kilobytes (x 1024 bits / x 1024 bytes) |
| Kb/s | kilobits per second |
| kg | kilogram |
| KHz | kilohertz |
| kv | kilovolt |

*Continued*

**Table 1-1.** Acronyms and Abbreviations *Continued*

| Acronym/Abbreviation | Description |
|---|---|
| lb | pound |
| LAN | local area network |
| LCD | liquid crystal display |
| LED | light-emitting diode |
| LIF | low insertion force (socket) |
| LPC | Low pin count |
| LSI | large scale integration |
| LSb / LSB | least significant bit / least significant byte |
| LUN | logical unit (SCSI) |
| MCH | Memory controller hub |
| MMX | multimedia extensions |
| MPEG | Motion Picture Experts Group |
| ms | millisecond |
| MSb / MSB | most significant bit / most significant byte |
| mux | multiplex |
| MVA | motion video acceleration |
| MVW | motion video window |
| *n* | variable parameter/value |
| NIC | network interface card/controller |
| NiCad | nickel cadmium |
| NiMH | nickel-metal hydride |
| NMI | non-maskable interrupt |
| NRZI | Non-return-to-zero inverted |
| ns | nanosecond |
| NT | nested task flag |
| NTSC | National Television Standards Committee |
| NVRAM | non-volatile random access memory |
| OEM | original equipment manufacturer |
| OS | operating system |
| PAL | 1. programmable array logic 2. phase altering line |
| PC | Internet Device |
| PCI | peripheral component interconnect |
| PCM | pulse code modulation |
| PCMCIA | Internet Device Memory Card International Association |
| PF | parity flag |
| PIN | personal identification number |
| PIO | Programmed I/O |
| POST | power-on self test |
| PROM | programmable read-only memory |
| PTR | pointer |
| RAM | random access memory |
| RAS | row address strobe |
| rcvr | receiver |
| RF | resume flag |
| RGB | red/green/blue (monitor input) |
| RH | Relative humidity |
| RIMM | RDRAM inline memory module |
| RMS | root mean square |
| ROM | read-only memory |
| RPM | revolutions per minute |
| RTC | real time clock |
| R/W | read/write |

*Continued*

**Table 1-1.** Acronyms and Abbreviations *Continued*

| Acronym/Abbreviation | Description |
|---|---|
| SCSI | small computer system interface |
| SDRAM | Synchronous Dynamic RAM |
| SEC | Single Edge-Connector |
| SECAM | sequential colour avec memoire (sequential color with memory) |
| SF | sign flag |
| SGRAM | Synchronous Graphics RAM |
| SIMD | Single instruction multiple data |
| SIMM | single in-line memory module |
| SIT | system information table |
| SMART | Self Monitor Analysis Report Technology |
| SMI | system management interrupt |
| SMM | system management mode |
| SMRAM | system management RAM |
| SPD | serial presence detect |
| SPP | standard parallel port |
| SRAM | static RAM |
| SSE | Streaming SIMD extensions |
| STN | super twist pneumatic |
| SVGA | super VGA |
| SW | software |
| TAD | telephone answering device |
| TAFI | Temperature-sensing And Fan control Integrated circuit |
| TAM | telephone answering machine |
| TCP | tape carrier package |
| TF | trap flag |
| TFT | thin-film transistor |
| TIA | Telecommunications Information Administration |
| TPE | twisted pair ethernet |
| TPI | track per inch |
| TTL | transistor-transistor logic |
| TV | television |
| TX | transmit |
| UART | universal asynchronous receiver/transmitter |
| UDMA | Ultra DMA |
| URL | Uniform resource locator |
| us / µs | microsecond |
| USB | Universal Serial Bus |
| UTP | unshielded twisted pair |
| V | volt |
| VESA | Video Electronic Standards Association |
| VGA | video graphics adapter |
| vib | vibrato |
| VLSI | very large scale integration |
| VRAM | Video RAM |
| W | watt |
| WOL | Wake on LAN |
| WRAM | Windows RAM |
| ZF | zero flag |
| ZIF | zero insertion force (socket) |

# Chapter 2
# SYSTEM OVERVIEW

## 2.1 INTRODUCTION

The Compaq iPAQ Family of Internet Devices provides affordable business solutions with the focus on internet access and mainstream performance. Based on an Intel Celeron or Pentium III processor with the Intel 810e chipset, these systems are designed to maximize the effectiveness of internet and intranet usage while simplifying system management.


**Figure 2–1.** Compaq iPAQ Internet Device with Monitor

This chapter includes the following topics:

## 2.2 FEATURES AND OPTIONS

This section describes the standard features and available options.

### 2.2.1 STANDARD FEATURES

The following standard features are available on all models:

- Celeron or Pentium III processor
- 810e Chipset
- Two DIMM sockets for system memory
- AC'97 audio subsystem w/Compaq Premier Sound and front panel mic and headphone jacks
- MuliBay device mount w/hot-swap support
- Extended IDE controller supporting UATA/66 mode
- Hard drive fault prediction
- Two USB ports on front panel
- Network interface controller
- VGA analog output (1600 x 1200 max resolution)
- APM 1.2 power management support
- Plug 'n Play compatible (with ESCD support)
- Intelligent Manageability support
- Energy Star compliant
- Security features including:
    - Setup and power-on passwords
    - DriveLock for MultiBay hard drive
    - I/O interface disabling
    - Administrator password
    - Network service boot
    - Asset tracking tag
    - UUID
    - Cable lock provision
- Compaq Easy-Access keyboard w/Windows support
- Mouse

Table 2-1 shows the differences in features between the iPAQ models:

**Table 2-1.**
iPAQ Feature Difference Matrix

| | Legacy-Free | | Legacy-Light | |
|---|---|---|---|---|
| | **Celeron-Based** | **Pentium-based** | **Celeron-Based** | **Pentium-Based** |
| 4-MB Display cache | No | Yes | No | Yes |
| Rear panel USB ports | 3 | 3 | 0 | 0 |
| Serial port | 0 | 0 | 1 | 1 |
| Parallel port | 0 | 0 | 1 | 1 |
| Keyboard/mouse connection | USB | USB | PS/2 | PS/2 |

## 2.2.2 OPTIONS

The following items are available as options for all models and may be included in the standard configuration of some models:

| | | |
|---|---|---|
| ♦ | System Memory: | 32-MB DIMM (non-ECC)<br>64-MB DIMM (non-ECC)<br>128-MB DIMM (non-ECC)<br>256-MB DIMM (non-ECC) |
| ♦ | Hard drives: | 4.3 or 8.4 GB UATA/66 hard drive |
| ♦ | MultiBay drives: | 24x CD-ROM drive<br>4x DVD-ROM drive<br>Super Disk LS-120 Power Drive<br>6.0 GB hard drive |

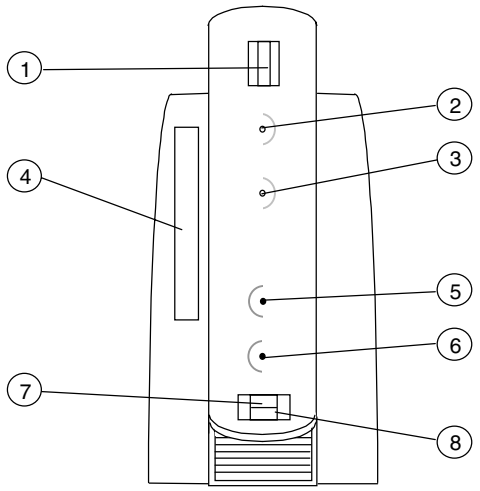
## 2.3 MECHANICAL DESIGN

The Compaq iPAQ Internet Device uses a minitower form factor featuring a smaller footprint and reduced height than previous minitowers, allowing easy floor or desktop positioning. Commonly used audio and USB connections are accessible from the front panel. There are slight differences between the legacy-light and legacy-free models, most notably in the rear panel layouts.

**NOTE:** For detailed information on servicing the Internet Device refer to the applicable Maintenance and Service Guide.

### 2.3.1 CABINET LAYOUTS

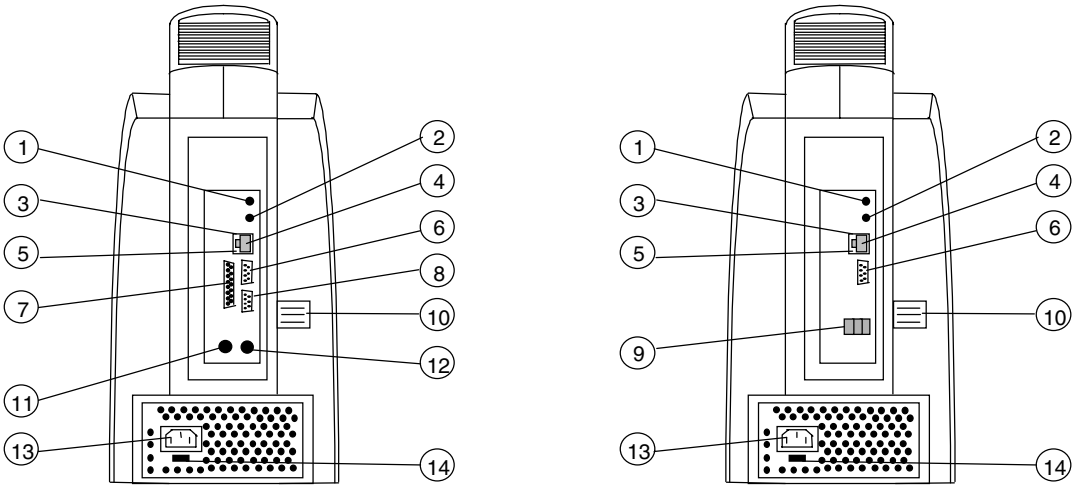
#### 2.3.1.1 Front View




| Item | Description |
|---|---|
| 1 | Power Button |
| 2 | Power LED |
| 3 | Hard drive activity LED |
| 4 | MultiBay device bay (accepts 5.25”/12.7 mm storage device) |
| 5 | Microphone In Jack |
| 6 | Headphone Out Jack |
| 7 | USB port 3 jack |
| 8 | USB port 4 jack |

**Figure 2–2.** Compaq iPAQ Internet Device, Front View

### 2.3.1.2 Rear Views




Legacy-Light Legacy-Free

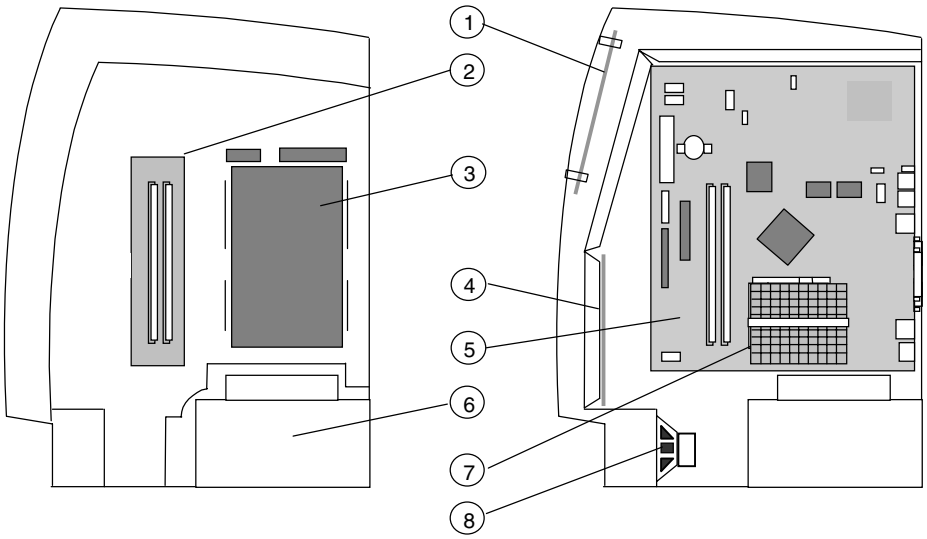
| Item | Description | Item | Description |
|---|---|---|---|
| 1 | Audio line output | 2 | Audio line input |
| 3 | Network activity LED indicator | 4 | Network I/F jack |
| 5 | Network speed LED indicator | 6 | VGA monitor connector |
| 7 | Parallel I/F connector | 8 | Serial I/F connector |
| 9 | USB port connectors (left-to-right; 0,1, 2) | 10 | MultiBay device eject button |
| 11 | PS/2 mouse connector | 12 | PS/2 keyboard connector |
| 13 | AC line in connector | 14 | Line voltage select switch |

**Figure 2–3.** Compaq iPAQ Internet Device, Rear Views

## 2.3.2 CHASSIS LAYOUT

The internal assemblies are accessible from the right side of the system unit. The right side (carbon-colored) cover is easily removable allowing quick access to the DIMM sockets through an access opening and to the hard drive. Access to the system board and processor requires removing the right chassis access panel.

**NOTE:** For a detailed description on servicing the unit refer to the applicable Maintenance and Service Guide.

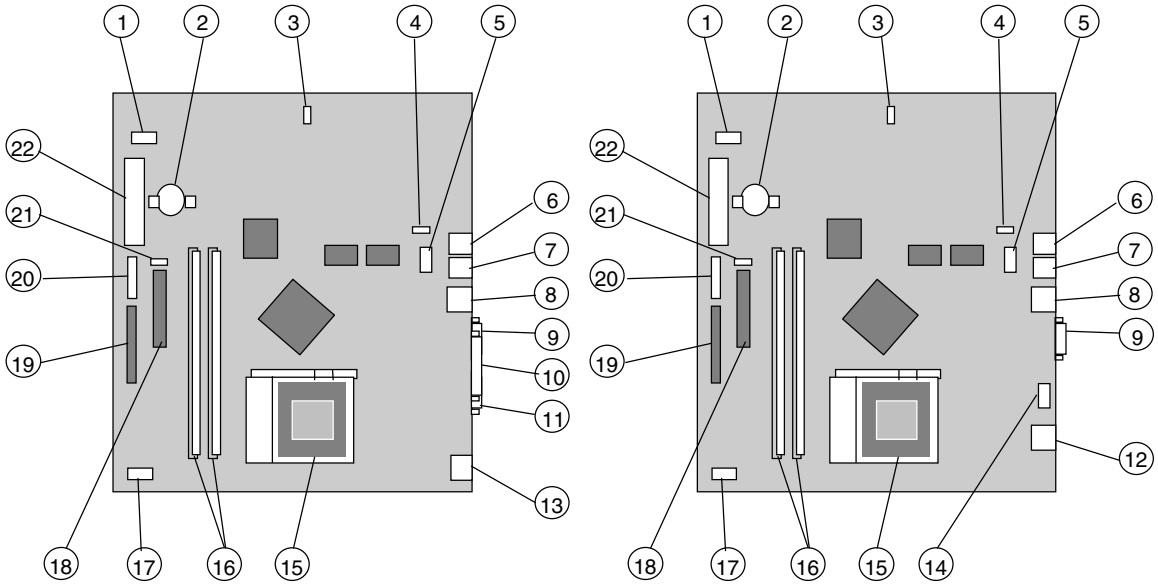



| Item | Description |
|---|---|
| 1 | Power button/LED board (PCA# 010647) |
| 2 | DIMM socket access |
| 3 | Hard drive in 3.5” 1/3 height bay |
| 4 | Audio I/O board (PCA# 010650) |
| 5 | System board (PCA# 161014 or 161015) |
| 6 | Power supply assembly |
| 7 | Processor |
| 8 | Speaker |

**Figure 2–4.** Compaq iPAQ Internet Device Chassis Layout, Ride Side View

## 2.3.3 SYSTEM BOARD LAYOUTS

The Compaq iPAQ Internet Device uses a FlexATX-type (9.0 x 7.5 inch) system board. Two variations are available; a legacy-light board and a legacy-free board.




Legacy Light (PCA# 161014) Legacy Free (PCA# 161015)

| Item | Description |
|---|---|
| 1 | USB ports 3 and 4 (front panel) header |
| 2 | Battery |
| 3 | BIOS ROM configuration jumper |
| 4 | Speaker connector |
| 5 | Audio microphone/headphone header |
| 6 | Audio line out jack |
| 7 | Audio line in jack |
| 8 | Network connector |
| 9 | VGA monitor connector |
| 10 | Parallel I/F connector |
| 11 | Serial I/F connector |
| 12 | USB ports 0, 1, 2 connectors |
| 13 | PS/2 mouse connector (top), PS/2 keyboard connector (bottom) |
| 14 | Serial I/F header |
| 15 | PGA370 processor socket |
| 16 | DIMM sockets |
| 17 | Processor (boxed) fan header |
| 18 | IDE (primary) 40-pin connector |
| 19 | IDE (secondary) 50-pin connector |
| 20 | Power button/LED indicator connector |
| 21 | CD audio header |
| 22 | Power supply connector |

NOTE:
Refer to Chapter 7 “Power and Signal Distribution” for header pinouts.

**Figure 2–5.** Compaq iPAQ System Board Layouts

## 2.4 SYSTEM ARCHITECTURE

The Compaq iPAQ Internet Device features an Intel Celeron or Pentium III processor and the 810e chipset. As indicated in the following table and shown in Figure 2-6, four architectural configurations are available:

- Legacy-free with Celeron processor
- Legacy-free with Pentium III processor
- Legacy-light with Celeron processor
- Legacy-light with Pentium III processor

Legacy-free systems provide five Universal Serial Bus (USB) ports for connecting peripherals (including the supplied USB mouse and USB keyboard). Legacy light systems provide two USB ports along with the traditional PS/2 connectors for the supplied mouse and keyboard as well as parallel and serial port connectors.

All systems use the 810e chipset. The 810e chipset includes the 82810e-DC100 GMCH designed to provide control for SDRAM and also integrates an AGP 2X graphics controller. Pentium III-based systems come with an additional 4-MB display cache to compliment the graphics controller.

The 810e chipset also includes an 82801 I/O Controller Hub (ICH) that provides two IDE interfaces, two USB interfaces, and a PCI bus controller. The 82802 Firmware Hub (FWH) component is loaded with Compaq BIOS

Table 2-1 lists differences between system architectures:

**Table 2-2.**
Architectural Comparison

| | Legacy Free | | Legacy Light | |
|---|---|---|---|---|
| | **Celeron-Based** | **Pentium III-Based** | **Celeron-Based** | **Pentium III-Based** |
| Host bus (FSB)speed [1] | 66 MHz | 100 MHz | 66 MHz | 100 MHz |
| 4-MB Display Cache? | No | Yes | No | Yes |
| PS/2 Mouse/Keyboard? | No | No | Yes | Yes |
| Serial port? | No | No | Yes | Yes |
| Parallel port? | No | No | Yes | Yes |
| # of USB ports | 5 | 5 | 2 | 2 |

NOTES:
[1] As configured with 500-MHz processor.

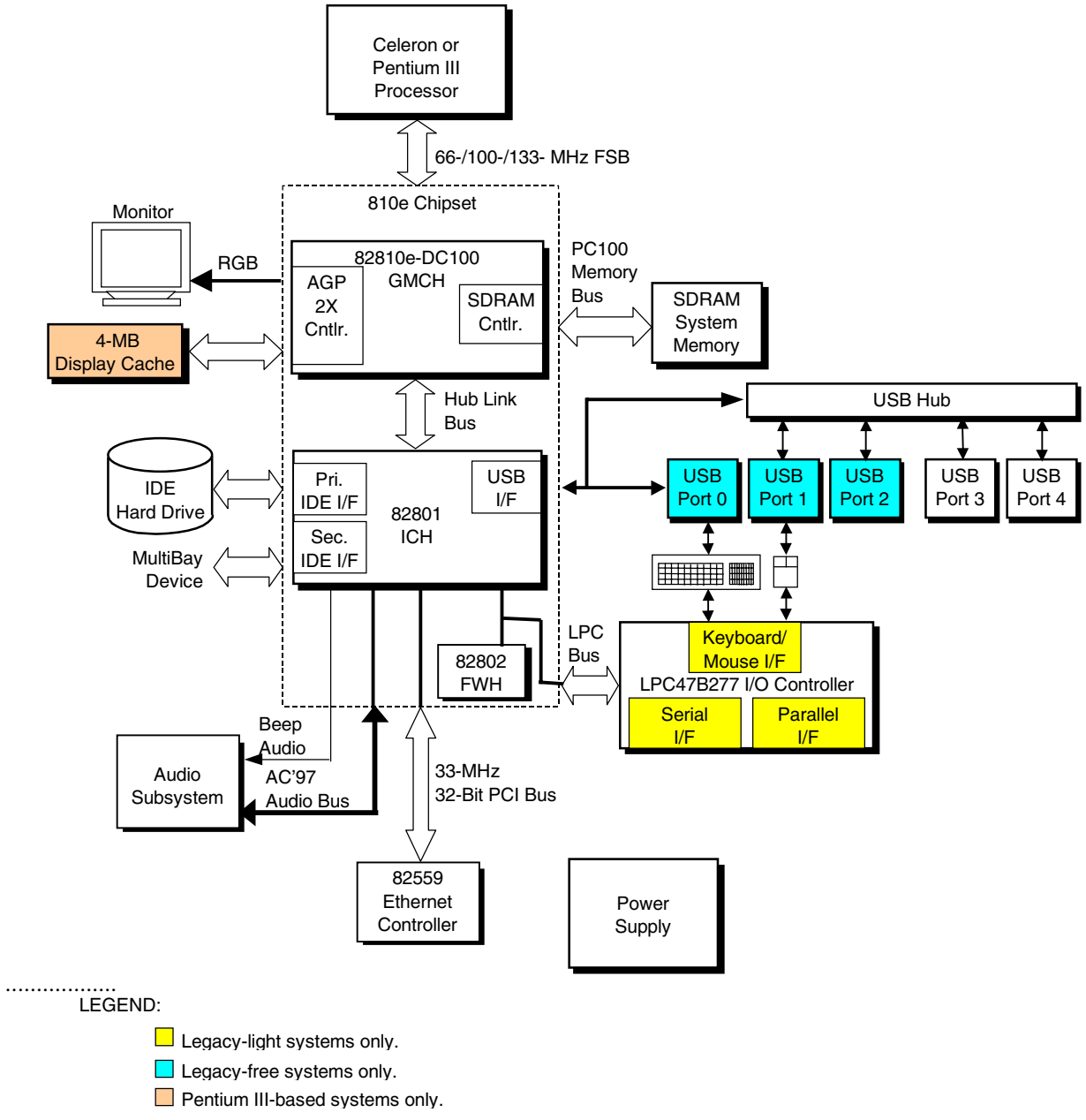



**Figure 2–6.** Compaq iPAQ Architecture, Block diagram

### 2.4.1 PROCESSORS

The Compaq iPAQ family includes models based on Celeron and Pentium III processors. These processors are backward-compatible with software written for the Pentium II, Pentium MMX, Pentium Pro, Pentium, and x86 microprocessors. Both processor architectures include a floating-point unit and first and secondary caches providing enhanced performance for multimedia applications.

#### 2.4.1.1 Celeron Processor

Select Compaq iPAQ systems use the Intel Celeron processor. The Celeron processor provides economical performance and is compatible with software written for previous generation processors such as Pentium II, Pentium MMX, Pentium, and x86 processors. Featuring a Pentium-type core architecture, the Celeron processor integrates a dual-ALU CPU with a floating-point unit, 32-KB first-level cache, and 128-KB second level cache, all of which operate at full processing (CPU) speed. The Celeron processor includes MMX technology for enhanced multimedia performance.

The Celeron processor uses a PGA370 package with a heat sink.

#### 2.4.1.2 Pentium III Processor

The Intel Pentium III processor used on select systems represents the maximum performance processor for Compaq iPAQs. The Pentium III processor is compatible with software written for Celeron, Pentium II, Pentium MMX, Pentium, and x86 processors.

The Pentium III processor core integrates a dual-ALU CPU with a floating-point unit and 32-KB first-level cache operating at processing (CPU) speed. Featuring .18-micron technology, the Pentium III processor features 256 kilobytes of secondary cache included on the CPU die and operating at full processor speed.

The Pentium III processor includes MMX technology for enhanced multimedia performance. Also included are 70 additional streaming SIMD extensions (SSE) for enhancing 3D graphics and speech processing performance and a serial number function useful for asset tracking.

The Pentium III processor employed in these systems uses a Flip-Chip (FC) PGA370 package and heat sink.

### 2.4.1.3 Processor Upgrading

All models of the Compaq iPAQ use the PGA370 zero-insertion force (ZIF) socket for processor mounting as shown in Figure 2-7. Raising the Lock/Unlock handle of the socket in the vertical position allows the processor to be removed or inserted into the socket. Lowering the Lock/Unlock handle in the down (horizontal) position locks the processor in place. Factory configurations use processors fitted with passive heat sinks. Upgrade (boxed) processors may be fitted with a heat sink/fan assembly with a power cable that attaches to the fan power header provided on the system board.

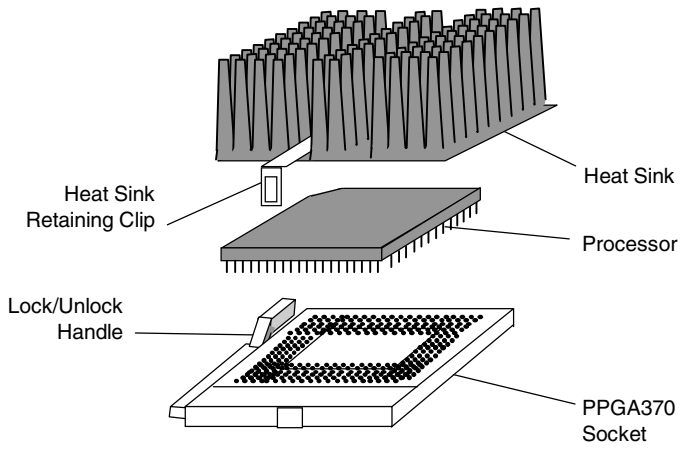



**Figure 2–7.** Processor Assembly and Mounting

The processor clock frequency is automatically set by chipset logic, eliminating the need for setting DIP switches when upgrading the processor.

**WARNING:** The system board is designed handle a maximum processor current load of 18 amps. Installing a replacement processor that draws more than 18 amps of current may damage the processor and/or the system board.

## 2.4.2 CHIPSET

The Compaq iPAQ employs the Intel 810e chipset, which is designed to compliment the processor and provide the central point for the system's data transactions.

The chipset is composed of a graphics memory controller hub (GMCH), an I/O controller hub (ICH), and a firmware hub (FWH). Table 2-3 shows the functions provided by the components of the chipset.

**Table 2-3.**
Intel 810e Chipset Components

| Component Type | Function |
|---|---|
| 82810e-DC100 Graphics/Memory Controller Hub(GMCH) | AGP 2X graphics controller (i740 equivalent)<br>SDRAM controller supporting 2 PC100 DIMMs<br>66-/100-/133-MHz FSB<br>PCI bus I/F |
| 82801AA I/O Controller Hub (ICH) | LPC bus I/F<br>SMBus I/F<br>IDE I/F with UATA/66 support<br>AC '97 audio controller<br>RTC/CMOS<br>IRQ controller<br>Power management logic<br>USB I/F (2) |
| 82802 Firmware Controller Hub (FWH) | Loaded with Compaq BIOS<br>Random number generator |

## 2.4.3 SUPPORT COMPONENTS

Input/output functions not provided by the chipset are handled by other support components. Some of these components also provide "housekeeping" and various other functions as well. Table 2-4 shows the functions provided by the support components.

**Table 2-4.**
Support Component Functions

| Component Name | Function | Notes |
|---|---|---|
| LPC47B277 I/O Controller | Keyboard and pointing device I/F | [1] |
| | Diskette I/F | [2] |
| | Serial I/F | [1] |
| | Parallel I/F | [1] |
| | AGP, PCI reset generation | |
| | ISA serial IRQ converter | |
| | Power button logic | |
| | Slow speed detection | |
| | S3 regulator controller | |
| | GPIO ports | |
| AD1881 Audio Codec | Audio mixer | |
| | Digital-to-analog converter | |
| | Analog-to-digital converter | |
| | Analog I/O:<br>Mic input<br>Line input<br>CD input<br>Line output | |
| 82559 Ethernet Controller [1] | Network interface controller | |
| | PHY interface | |

NOTE:
[1] Implemented on legacy-light models only.
[2] Not available for actual use but may be enabled to satisfy OS requirements.

## 2.4.4 SYSTEM MEMORY

These systems utilize Synchronous DRAM (PC100 SDRAM, non-ECC only). Two DIMM sockets are provided and accessible through an access opening once the right side cover has been removed.

### 2.4.5 MASS STORAGE

In a standard configuration the Compaq iPAQ supports two mass storage devices; one internal IDE hard drive mounted on the right side and a removeable-media IDE device (CD-ROM, DVD, or LS-120 Power Drive, etc.) mounted in the MultiBay on the left side. This system uses SMART drives for the internal IDE device. An adapter is available that allows a secondary IDE hard drive to be installed in the MultiBay. The MultiBay supports hot-swapping of mass storage devices **except for hard drives**. The Compaq iPAQ supports the DriveLock feature for MultiBay hard drives, providing enhanced security for removeable hard drives.

### 2.4.6 SERIAL AND PARALLEL INTERFACES

The legacy-light models include a serial port and a parallel port accessible at the rear of the chassis. The serial port is RS-232-C/16550-compatible and supports standard baud rates up to 115,200 as well as two high-speed baud rates of 230K and 460K , and utilize a DB-9 connector. The parallel interface is Enhanced Parallel Port (EPP1.9) and Enhanced Capability Port (ECP) compatible, and supports bi-directional data transfers through a DB-25 connector. These interfaces may be disabled through Setup for enhanced security

### 2.4.7 UNIVERSAL SERIAL BUS INTERFACE

Legacy-light models feature two front panel-accessible Universal Serial Bus (USB) ports that provide a 12Mb/s interface for peripherals. Legacy-free models also include three additional USB ports on the rear panel to accommodate the USB keyboard and mouse supplied with those models. The USB provides hot plugging/unplugging (Plug 'n Play) functionality.

### 2.4.8 GRAPHICS SUBSYSTEM

All models use the graphics controller integrated into the 82810e/DC-100 GMCH component of the 810e chipset. This graphics controller is the equivalent of the Intel i740 controller and provides up to 1600 x 1200 2D resolution using the AGP 2X interface. Pentium III-based systems also include 4 megabytes of local display cache for higher 3D performance.

## 2.4.9 AUDIO SUBSYSTEM

The audio subsystem features an AC'97 specification-based design and uses the integrated AC97 audio controller of the chipset and an AC'97-compliant audio codec. Microphone and headphone jacks are accessible on the front panel and line input and output jacks are provided on the rear panel. A low-distortion 5-watt amplifier drives a long-excursion speaker for optimum sound.

## 2.5 SPECIFICATIONS

This section includes the environmental, electrical, and physical specifications for the Compaq iPAQ Series Internet Devices. Where provided, metric statistics are given in parenthesis. All specifications subject to change without notice.

**Table 2-5.**
Environmental Specifications

| Parameter | Operating | Nonoperating |
|---|---|---|
| Air Temperature | 50° to 95° F (10° to 35° C) | -24° to 140° F (-30° to 60° C) |
| Shock | N/A | 60.0 g for 2 ms half-sine pulse |
| Vibration | 0.000215g^ 2/Hz, 10-300 Hz [1] | 0.0005g^ 2/Hz, 10-500 Hz [1] |
| Humidity | 90% RH @ 36° C (no hard drive) | 95% RH @ 36° C |
| Maximum Altitude | 10,000 ft (3048 m) | 30,000 ft (9,144 m) |

NOTE:
[1] 0.5 grms nominal

**Table 2-6.**
Electrical Specifications

| Parameter | U.S. | International |
|---|---|---|
| Input Line Voltage: | | |
| Nominal: | 110 - 120 VAC | 200 - 240 VAC |
| Maximum: | 90 - 132 VAC | 180 - 264 VAC |
| Input Line Frequency Range: | | |
| Nominal: | 50 - 60 Hz | 50 - 60 Hz |
| Maximum: | 47 - 63 Hz | 47 - 63 Hz |
| Power Supply: | | |
| Maximum Continuous Power | 90 watts | 90 watts |
| Maximum Line Current Draw | 2.5 amps | 1.25 amps |

**Table 2-7.**
Physical Specifications

| Parameter | Standard | Metric |
|---|---|---|
| Height | 11.80 in | 29.97 cm |
| Width | 5.66 in | 14.38 cm |
| Depth | 9.44 in | 23.98 cm |
| Weight | 10.7 lb | 4.8 kg |

**Table 2-8.**
MultiBay 24x CD-ROM Drive Specifications
(SP# 161685-B21)

| Parameter | Measurement |
|---|---|
| Interface Type / Protocol | IDE / ATAPI |
| Transfer Rate: | |
| Max. Sustained | 3.6 MB/s |
| Burst | 16.6 MB/s |
| Media Type | Mode 1,2, Mixed Mode, CD-DA, Photo CD, Cdi, CD-XA |
| Capacity: | |
| Mode 1, 12 cm | 550 MB |
| Mode 2, 12 cm | 640 MB |
| 8 cm | 180 MB |
| Center Hole Diameter | 15 mm |
| Disc Diameter | 8/12 cm |
| Disc Thickness | 1.2 mm |
| Track Pitch | 1.6 um |
| Laser | |
| Beam Divergence | 53.5 +/- 1.5 ° |
| Output Power | 53.6 0.14 mW |
| Type | GaAs |
| Wave Length | 790 +/- 25 nm |
| Average Access Time: | |
| Random | 140 ms |
| Full Stroke | 300 ms |
| Audio Output Level | 0.7 Vrms |
| Cache Buffer | 128 KB |

**Table 2-9.**
MultiBay 4x DVD-ROM Drive Specifications
(SP# 161685-B21)

| Parameter | Measurement |
|---|---|
| Interface Type / Protocol | IDE / ATAPI |
| Transfer Rate: | |
| Max. Sustained (off disk) | 5.41 MB/s |
| Data Bus Burst | 16.6 MB/s |
| Media Types | DVD (single/double layer), DVD-5, DVD-9, DVD-10, CD-ROM Modes 1 or 2, CD-DA, Photo CD, Cdi, CD-XA |
| Capacity: | |
| Mode 1, 12 cm | 550 MB |
| Mode 2, 12 cm | 640 MB |
| 8 cm | 180 MB |
| Center Hole Diameter | 15 mm |
| Disc Diameter | 8 or 12 cm |
| Disc Thickness | 1.2 mm |
| Track Pitch | 1.6 um |
| Average Access Time: | |
| DVD: | |
| Random | <170 ms |
| Full Stroke | <280 ms |
| CD: | |
| Random | <130 ms |
| Full stroke | <225 ms |
| Audio Output Level | 0.7 Vrms |
| Cache Buffer | 512 KB |

**Table 2-10.**
Hard Drive Specifications

| Parameter | 4.3 GB | 6.0 GB [1] | 8.4 GB |
|---|---|---|---|
| P/N | 158738 | 161684 | 158739 |
| Interface / Protocol Type | IDE / UATA-4 | IDE / UATA-4 | IDE / UATA-4 |
| Drive Type | 65 | 65 | 65 |
| Drive Size | 3.5/5.25 in | 2.5/5.25 in | 5.25 in |
| Interface Transfer Rate (max.) | 66.6 MB/s | 66.6 MB/s | 66.6 MB/s |
| Max. Seek Time (w/settling) | | | |
| Single Track | 2.0 ms | 4.0 ms | 4.75 ms |
| Average | 9.5 ms | 12.0 ms | 14.9 ms |
| Full Stroke (max) | 19.0 ms | 23.0 ms | 27 ms |
| Disk Format (logical): | | | |
| # of Cylinders | 8419 | 13424 | 16383 |
| # of Data Heads | 15 | 15 | 16 |
| # of Sectors per Track | 63 | 63 | 63 |
| Rotation Speed | 5400 RPM | 4200 RPM | 5400 RPM |
| Drive Fault Prediction | SMART II | SMART II | SMART III |

NOTE:

[1] For use in MultiBay.

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# Chapter 3
# PROCESSOR/ MEMORY SUBSYSTEM

## 3.1 INTRODUCTION

This chapter describes the processor/cache memory subsystem of the Compaq iPAQ Internet Device featuring a Celeron or Pentium III processor and the 810e chipset (Figure 3-1). The 810e chipset supports up to two SDRAM DIMMs and integrates an i740 3D graphics controller (covered in Chapter 6).

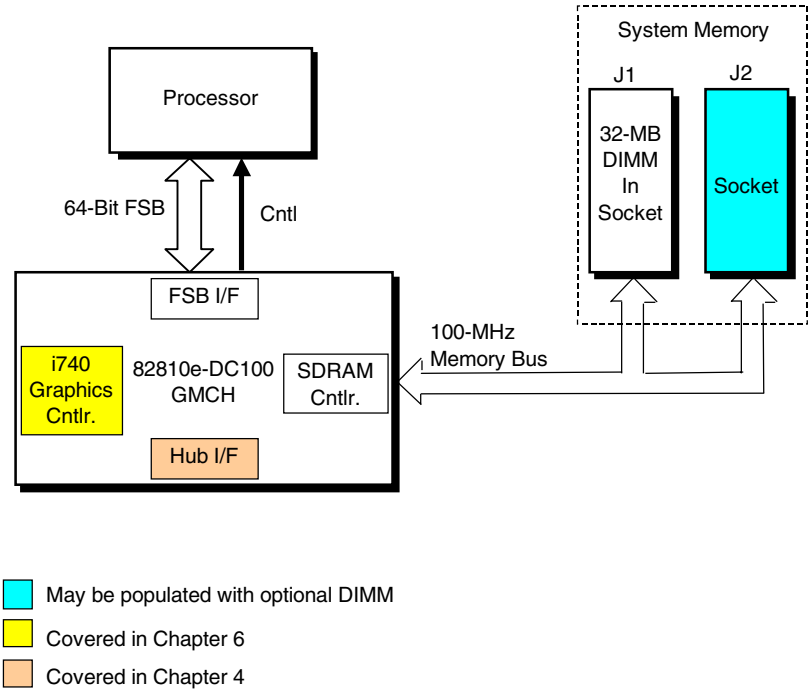



**Figure 3–1.** Processor/Memory Subsystem Architecture

This chapter includes the following topics:

## 3.2 PROCESSOR

The Compaq iPAQ is configured as either a Celeron-based or Pentium III-based system.

### 3.2.1 CELERON PROCESSOR

The Celeron processor (Figure 3-2) uses a dual-ALU CPU with branch prediction and MMX support, floating point unit (FPU) for math coprocessing, a 32-KB primary (L1) cache, and a 128-KB secondary (L2) cache. All internal functions, except for the front side bus interface (FSB I/F), operate at processor speed.

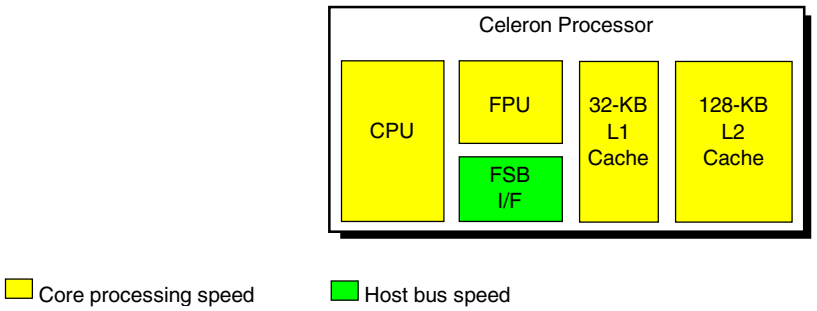



**Figure 3–2.** Celeron Processor Internal Architecture

The Celeron processor is software-compatible with earlier generation Pentium II, Pentium MMX, Pentium, and x86 processors. The MMX support provided by the Celeron consists of 57 special instructions for accelerating multimedia communications applications. Such applications often involve computing-intensive loops that can take up as much as 90 percent of the CPU's execution time. Using a parallel-processing technique called single-instruction multiple-data (SIMD), MMX logic processes data 64 bits at a time. Specific applications that can benefit from MMX technology include 2D/3D graphics, audio, speech recognition, video codecs, and data compression.

The Celeron-based systems ship with a Celeron 500 installed. The 82810-DC100 GMCH supports the processors listed in the following table:

**Table 3-1.**
Celeron Processor Statistical Comparison

| Processor | Core/L1/L2 Freq. | FSB Freq. | Core Voltage | Power Consumption |
|---|---|---|---|---|
| Celeron 500 | 500 MHz | 66 MHz | 2.0 v | Na |
| Celeron 533 | 533 MHz | 66 MHz | 2.0 v | Na |

## 3.2.2 PENTIUM III PROCESSOR

The Pentium III processor's architecture (Figure 3-3) includes the same core functionality as described previously for the Celeron processor but includes a larger L2 cache and additional processing features.

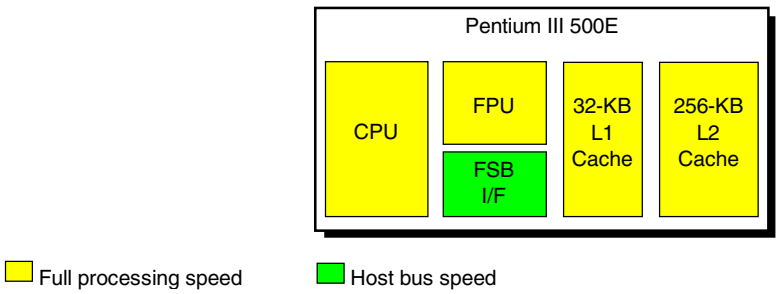



**Figure 3–3.** Pentium III Processor Internal Architecture

**Table 3-2.**
Pentium III Processor Statistical Comparison

| Processor | CPU/L1 Speed | L2 Size / Speed | Core Voltage | FSB Speed |
|---|---|---|---|---|
| Pentium III 500E | 500 MHz | 256 KB @ 500 MHz | 1.60 VDC | 100 MHz |
| Pentium III 533 | 533 MHz | 512 KB @ 266 MHz | 2.00 VDC | 100 MHz |
| Pentium III 533B | 533 MHz | 512 KB @ 266 MHz | 2.05 VDC | 133 MHz |
| Pentium III 533EB | 533 MHz | 256 KB @ 533 MHz | 1.65 VDC | 133 MHz |
| Pentium III 550 | 550 MHz | 512 KB @ 275 MHz | 2.00 VDC | 100 MHz |
| Pentium III 550E | 550 MHz | 256 KB @ 550 MHz | 1.60 VDC | 100 MHz |
| Pentium III 600 | 600 MHz | 512 KB @ 300 MHz | 2.05 VDC | 100 MHz |
| Pentium III 600B | 600 MHz | 512 KB @ 300 MHz | 2.05 VDC | 133 MHz |
| Pentium III 600E | 600 MHz | 256 KB @ 600 MHz | 1.65 VDC | 100 MHz |
| Pentium III 600EB | 600 MHz | 256 KB @ 600 MHz | 1.65 VDC | 133 MHz |
| Pentium III 667 | 667 MHz | 256 KB @ 667 MHz | 1.65 VDC | 133 MHz |
| Pentium III 700 | 700 MHz | 256 KB @ 700 MHz | 1.65 VDC | 100 MHz |
| Pentium III 733 | 733 MHz | 256 KB @ 733 MHz | 1.65 VDC | 133 MHz |

The Pentium III processor is software-compatible with Celeron, Pentium II, Pentium MMX, Pentium, and x86 processors. The Pentium III processor also features 70 FPU-based streaming SIMD extensions (SSE) that, when implemented by appropriate software, can enhance 3D transforming and speech processing operations. Operating system requirements for SSE support are as follows:

| Operating System | Level of SSE Support |
|---|---|
| Windows 95 | No SSE support |
| Windows 98, OSR0 | SSE support though ISV and OpenGL 6.1 applications only |
| Windows 98, OSR1 | SSE support though ISV, OpenGL, and DirectX applications |
| Windows 2000 | SSE support with ISV, OpenGL, and DirectX applications |
| Windows NT 4.0 | SSE support requires driver and Service Pack 4 (SP5 recommended) |

### 3.2.3 PROCESSOR UPGRADING

All units use the PGA370 ZIF mounting socket and ship with either a Celeron 500E or a Pentium III 500E installed. To replace the processor, use the following procedure:

1. Power down the system and disconnect the power cord.
2. Remove the right outer (carbon) panel.
3. Disconnect and remove the hard drive.
4. Remove the right chassis access panel.
5. After insuring that you have been properly grounded, remove the heatsink retaining clip and then the heatsink itself.
6. Lift the release arm of the PGA370 socket to the upright position.
7. Lift the processor package from the socket.

Replacement of the new processor is a reversal of steps 1-7. The use of "boxed" processors may also require the connection of a power cable from the processor's heatsink-mounted fan to a header on the system board. When replacing the processor it is recommended that the replacement processor be of the same family as the existing processor (i.e., Celeron for Celeron, or Pentium for Pentium).

**WARNING**: **Upgrading to a faster processor is possible provided that the new processor does not draw more than 18 amps of current. Using a processor that draws in excess of 18 amps may create a thermal condition and damage the system board**

The processor core voltage and operating frequency are automatically set early in power cycle process. No DIP switch settings are involved in replacing the processor.

## 3.3 MEMORY SUBSYSTEM

The 810e chipset supports PC100 SDRAM for system memory. The memory interface consists of a 64-bit data bus operating at 100 MHz providing a maximum throughput rate of 800 MB/s. The system board provides two 168-pin SDRAM DIMM sockets that accommodate single- or double-sided DIMMs. **This system is designed for using non-ECC DIMMs only**.

If using memory modules from third party suppliers the following DIMM type is recommended: **100-MHz unbuffered RAM supporting CAS latency (CL) 2 or 3 with a data access time (clock-to-data out) of 9.0 ns or less @ CL=2 or CL=3**.

> **NOTE:** The 82810/82810e GMCH performs memory accesses at 100 MHz regardless of the FSB frequency.

The RAM type and operating parameters are detected during POST by the system BIOS using the serial presence detect (SPD) method. This method employs an $I^2C$ bus to communicate with an EEPROM on each installed DIMM. The EEPROM holds the type and operating parameter data.

The supported format complies with the JEDEC specification for 128-byte EEPROMs. This system also provides support for 256-byte EEPROMs to include additional Compaq-added features such as part number and serial number. The SPD format as supported in this system is shown in Table 3-3.

The key SPD bytes that BIOS checks for compatibility are 2, 9, 10, 18, 23, and 24. **If BIOS detects EDO DIMMs a "memory incompatible" message will be displayed and the system will halt.** If ECC DIMMs are used, all DIMMs installed must be ECC for ECC benefits (error logging) to be realized.

Once BIOS determines the DIMM type the DRAM speed and CAS latency is checked based on the following criteria:

| Bus Speed | Cycle Time | Access from Clock |
|---|---|---|
| 100 MHz | 10 ns | 6 ns @ 50 pf loading |

> **NOTE:** Refer to chapter 8 for a description of the BIOS procedure of interrogating DIMMs.

Only CAS latencies of 2 or 3 are supported. If DIMMs with unequal CAS latencies are installed then operation will occur based on the DIMM with the greatest latency.

If an incompatible DIMM is detected the NUM LOCK will blink for a short period of time during POST and an error message may or may not be displayed before the system hangs.

The SPD address map is shown below.

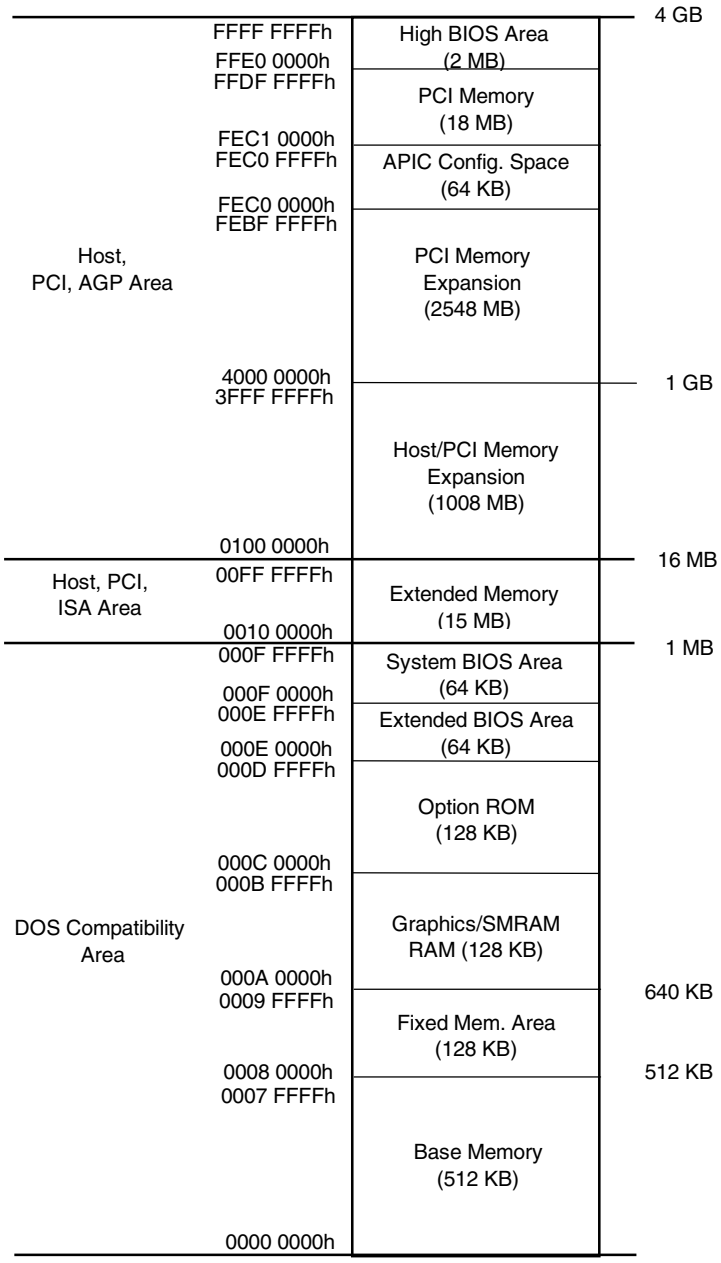
**Table 3-3.**
SPD Address Map (SDRAM DIMM)

| Byte | Description | Notes | Byte | Description | Notes |
|---|---|---|---|---|---|
| 0 | No. of Bytes Written Into EEPROM | [1] | 27 | Min. Row Prechge. Time | [7] |
| 1 | Total Bytes (#) In EEPROM | [2] | 28 | Min. Row Active to Delay | [7] |
| 2 | Memory Type | | 29 | Min. RAS to CAS Delay | [7] |
| 3 | No. of Row Addresses On DIMM | [3] | 30, 31 | Reserved | |
| 4 | No. of Column Addresses On DIMM | | 32..61 | Superset Data | [7] |
| 5 | No. of Module Banks On DIMM | | 62 | SPD Revision | [7] |
| 6, 7 | Data Width of Module | | 63 | Checksum Bytes 0-62 | |
| 8 | Voltage Interface Standard of DIMM | | 64-71 | JEP-106E ID Code | [8] |
| 9 | Cycletime @ Max CAS Latency (CL) | [4] | 72 | DIMM OEM Location | [8] |
| 10 | Access From Clock | [4] | 73-90 | OEM's Part Number | [8] |
| 11 | Config. Type (Parity, Nonparity, etc.) | | 91, 92 | OEM's Rev. Code | [8] |
| 12 | Refresh Rate/Type | [4] [5] | 93, 94 | Manufacture Date | [8] |
| 13 | Width, Primary DRAM | | 95-98 | OEM's Assembly S/N | [8] |
| 14 | Error Checking Data Width | | 99-125 | OEM Specific Data | [8] |
| 15 | Min. Clock Delay | [6] | 126, 127 | Reserved | |
| 16 | Burst Lengths Supported | | 128-131 | Compaq header "CPQ1" | [9] |
| 17 | No. of Banks For Each Mem. Device | [4] | 132 | Header checksum | [9] |
| 18 | CAS Latencies Supported | [4] | 133-145 | Unit serial number | [9] [10] |
| 19 | CS# Latency | [4] | 146 | DIMM ID | [9] [11] |
| 20 | Write Latency | [4] | 147 | Checksum | [9] |
| 21 | DIMM Attributes | | 148-255 | Reserved | [9] |
| 22 | Memory Device Attributes | | | | |
| 23 | Min. CLK Cycle Time at CL X-1 | [7] | | | |
| 24 | Max. Acc. Time From CLK @ CL X-1 | [7] | | | |
| 25 | Min. CLK Cycle Time at CL X-2 | [7] | | | |
| 26 | Max. Acc. Time From CLK @ CL X-2 | [7] | | | |

NOTES:

[1] Programmed as 128 bytes by the DIMM OEM
[2] Must be programmed to 256 bytes.
[3] High order bit defines redundant addressing: if set (1), highest order RAS# address must be re-sent as highest order CAS# address.
[4] Refer to memory manufacturer's datasheet
[5] MSb is Self Refresh flag. If set (1), assembly supports self refresh.
[6] Back-to-back random column addresses.
[7] Field format proposed to JEDEC but not defined as standard at publication time.
[8] Field specified as optional by JEDEC but required by this system.
[9] Compaq usage. This system requires that the DIMM EEPROM have this space available for reads/writes.
[10] Serial # in ASCII format (MSB is 133). Intended as backup identifier in case vender data is invalid. Can also be used to indicate s/n mismatch and flag system adminstrator of possible system Tampering.
[11] Contains the socket # of the module (first module is "1"). Intended as backup identifier (refer to note [10]).

Figure 3-4 shows the system memory map.




NOTE: All locations in memory are cacheable. Base memory is always mapped to DRAM. The next 128 KB fixed memory area can, through the north bridge, be mapped to DRAM or to PCI space. Graphics RAM area is mapped to PCI or AGP locations.

**Figure 3–4.** System Memory Map

## 3.4 SUBSYSTEM CONFIGURATION

The 82810e-DC100 GMCH component provides the configuration function for the processor/memory subsystem. Table 3-4 lists the configuration registers used for setting and checking such parameters as memory control and PCI bus operation. These registers reside in the PCI Configuration Space and accessed using the methods described in Chapter 4, section 4.2.

**Table 3-4.**
Host/PCI Bridge Configuration Registers (GMCH, Function 0)

| PCI Config. Addr. | Register | Reset Value | PCI Config. Addr. | Register | Reset Value |
|---|---|---|---|---|---|
| 00, 01h | Vender ID | 8086h | 6A, 6Bh | DRAM Control Reg. | 00h |
| 02, 03h | Device ID | 7190h | 6C..6Fh | Memory Buffer Strength | 55h |
| 04, 05h | Command | 0006h | 70h | Multi-Transaction Timer | 00h |
| 06, 07h | Status | 0210h | 71h | CPU Latency Timer | 10h |
| 08h | Revision ID | -- | 72h | SMRAM Control | 02h |
| 09..0Bh | Class Code | -- | 90h | Error Command | 00h |
| 0Dh | Latency Timer | 00h | 91h | Error Status Register 0 | 00h |
| 0Eh | Header Type | 00h | 92h | Error Status Register 1 | 00h |
| 10..13h | Aperture Base Config. | 8 | 93h | Reset Control | 00h |
| 50, 51h | PAC Config. Reg. | 00h | A0..A3h | AGP Capability Identifier | N/A |
| 53h | Data Buffer Control | 83h | A4..A7h | AGP Status | N/A |
| 55..56h | DRAM Row Type | 00h | A8..ABh | AGP Command | 00h |
| 57h | DRAM Control | 01h | B0..B3h | AGP Control | 00h |
| 58h | DRAM Timing | 00h | B4h | Aperture Size | 0000h |
| 59..5Fh | PAM 0..6 Registers | 00h | B8..BBh | Aperture Translation Table | 0000h |
| 60..67h | DRAM Row Boundary | 01h | BCh | Aperture I/F Timer | 00h |
| 68h | Fixed DRAM Hole | 00h | BDh | Low Priority Timer | 00h |

NOTES:
Refer to Intel Inc. documentation for detailed description of registers.
Assume unmarked locations/gaps as reserved.

# Chapter 4
# SYSTEM SUPPORT

## 4.1 INTRODUCTION

This chapter covers subjects dealing with basic system architecture and support functions. Topics covered are:



This chapter covers functions provided by off-the-shelf chipsets and therefore describes only basic aspects of these functions as well as information unique to Compaq iPAQ Internet Devices. For detailed information on specific components, refer to the applicable manufacturer's documentation.

## 4.2 PCI BUS OVERVIEW

**NOTE:** This section describes the PCI bus in general and highlights bus implementation in this particular system. For detailed information regarding PCI bus operation, refer to the *PCI Local Bus Specification Revision 2.2.*

This system implements a 32-bit Peripheral Component Interconnect (PCI) bus (spec. 2.2) operating at 33 MHz. The PCI bus handles address/data transfers through the identification of devices and functions on the bus. A device is typically defined as a component that resides on the PCI bus (although some components such as the GMCH and ICH are organized as multiple devices). A function is defined as the end source or target of the bus transaction. A device may contain one or more functions.

This system use two PCI buses. The PCI bus #0 is internal to the 810e chipset and divided by the hub link bus. The PCI bus #1 is used by the NIC function (Figure 4-1). As this system is designed for simplicity of system management, **the PCI buses are not available for expansion purposes.**

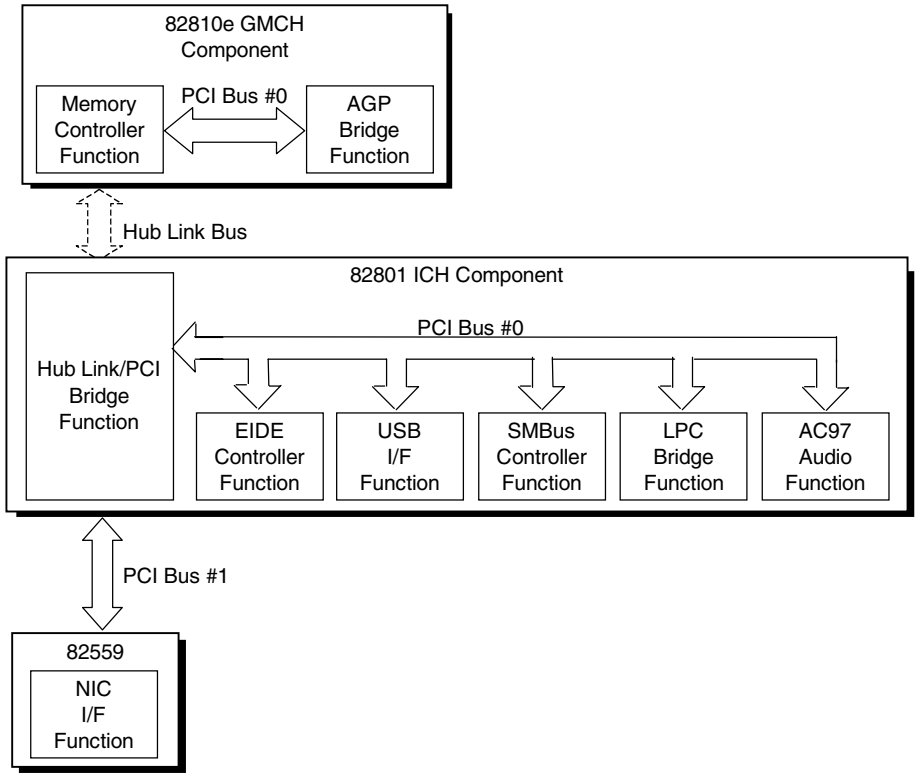



**Figure 4-1.** PCI Bus Devices and Functions

### 4.2.1 PCI BUS TRANSACTIONS

The PCI bus consists of a 32-bit path (AD31-00 lines) that uses a multiplexed scheme for handling both address and data transfers. A bus transaction consists of an address cycle and one or more data cycles, with each cycle requiring a clock (PCICLK) cycle. High performance is realized during burst modes in which a transaction with contiguous memory locations requires that only one address cycle be conducted and subsequent data cycles are completed using auto-incremented addressing. Four types of address cycles can take place on the PCI bus; I/O, memory, configuration, and special. Address decoding is distributed (left up to each device on the PCI bus).

#### 4.2.1.1 I/O and Memory Cycles

For I/O and memory cycles, a standard 32-bit address decode (AD31..0) for byte-level addressing is handled by the appropriate PCI device. For memory addressing, PCI devices decode the AD31..2 lines for dword-level addressing and check the AD1,0 lines for burst (linear-incrementing) mode. In burst mode, subsequent data phases are conducted a dword at a time with addressing assumed to increment accordingly (four bytes at a time).

#### 4.2.1.2 Configuration Cycles

Devices on the PCI bus must comply with PCI protocol that allows configuration of that device by software. In this system, configuration mechanism #1 (as described in the PCI Local Bus specification Rev. 2.1) is employed. This method uses two 32-bit registers for initiating a configuration cycle for accessing the configuration space of a PCI device. The configuration address register (CONFIG_ADDRESS) at 0CF8h holds a value that specifies the PCI bus, PCI device, and specific register to be accessed. The configuration data register (CONFIG_DATA) at 0CFCh contains the configuration data.

**PCI Configuration Address Register**
**I/O Port 0CF8h, R/W, (32-bit access only)**

| Bit | Function |
|---|---|
| 31 | Configuration Enable<br>0 = Disabled<br>1 = Enable |
| 30..24 | Reserved - read/write 0s |
| 23..16 | Bus Number. Selects PCI bus |
| 15..11 | PCI Device Number. Selects PCI device for access |
| 10..8 | Function Number. Selects function of selected PCI device. |
| 7..2 | Register Index. Specifies config. reg. |
| 1,0 | Configuration Cycle Type ID.<br>00 = Type 0<br>01 = Type 1 |

**PCI Configuration Data Register**
**I/O Port 0CFCh, R/W, (8-, 16-, 32-bit access)**

| Bit | Function |
|---|---|
| 31..0 | Configuration Data. |

Figure 4-2 shows how the loading of 0CF8h results in a Type 0 configuration cycle on the PCI bus. The Device Number (bits <15..11> determines which one of the AD31..11 lines is to be asserted high for the IDSEL signal, which acts as a "chip select" function for the PCI device to be configured. The function number (CF8h, bits <10..8>) is used to select a particular function within a PCI component.

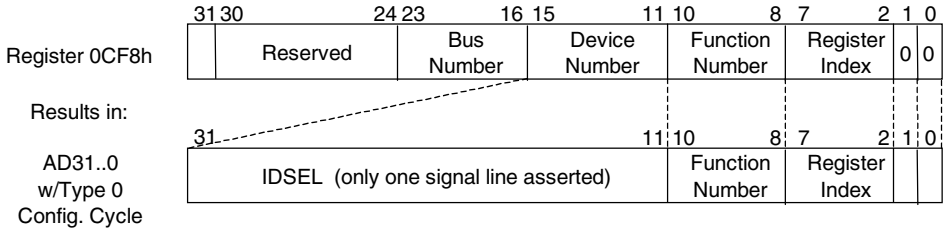



**Figure 4-2.** Type 0 Configuration Cycle

Type 0 configuration cycles are used for configuring devices on PCI bus # 0. Type 1 configuration cycles (reg. 0CF8h bits <1,0> = 01b) are passed on to PCI bus # 1. Table 4-1 shows the standard configuration of device numbers for components and slots residing on a PCI bus.

**Table 4-1.**
PCI Component Configuration Access

| PCI Component | Function # | Device # | PCI Bus # |
|---|---|---|---|
| 82810e GMCH: | | | |
| Memory Controller | 0 | 0 (00h) | 0 |
| AGP Bridge | 0 | 1(01h) | 0 |
| AGP slot | 0 | 0 (00h) | 2 |
| 82801 ICH: | | | |
| PCI Bridge | 0 | 30 (1Eh) | 0 |
| LPC Bridge | 0 | 31 (1Fh) | 0 |
| EIDE Controller | 1 | 31 (1Fh) | 0 |
| USB I/F | 2 | 31 (1Fh) | 0 |
| SMBus Controller | 3 | 31 (1Fh) | 0 |
| AC97 Audio Controller | 5 | 31 (1Fh) | 0 |
| AC97 Modem Controller | 6 | 31 (1Fh) | 0 |
| 82559 Network I/F Controller | 0 | 2 (02h) | 1 |

NOTES:
Not implemented.

The register index (CF8h, bits <7..2>) identifies the 32-bit location within the configuration space of the PCI device to be accessed. All PCI devices can contain up to 256 bytes of configuration data (Figure 4-3), of which the first 64 bytes comprise the configuration space header.

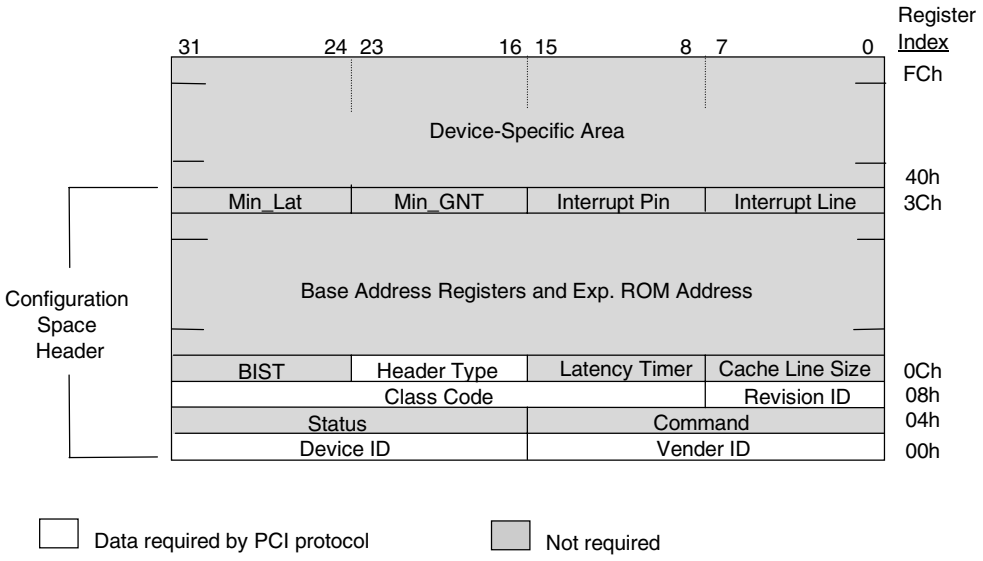



**Figure 4-3.** PCI Configuration Space Map

Each PCI device is identified with a vender ID (assigned to the vender by the PCI Special Interest Group) and a device ID (assigned by the vender). The device and vender IDs for the devices on the system board are listed in Table 4-2.

**Table 4-2.**
System Board PCI Device Identification

| PCI Device | Vender ID | Device ID |
|---|---|---|
| 82810e GMCH: | | |
| Memory Controller | 8086h | 2500h |
| AGP Bridge | 8086h | 2501h |
| 82801 ICH: | | |
| PCI Bridge | 8086h | 2418h |
| LPC Bridge | 8086h | 2410h |
| EIDE Controller | 8086h | 2411h |
| USB I/F | 8086h | 2412h |
| SMBus Controller | 8086h | 2413h |
| AC97 Audio Controller | 8086h | 2415h |
| 82559 Network I/F Controller | 8086h | 1229h |

### 4.2.2 PCI INTERRUPT MAPPING

The PCI bus provides for four interrupt signals; INTA-, INTB-, INTC-, and INTD-. These signals may be generated by on-board PCI devices or by devices installed in the PCI slots. In order to minimize latency, INTx- signal routing from the interrupt controller of the ICH to PCI slots/devices is distributed evenly as shown below:

| Intr. Cntlr. | AGP Cntlr. | Audio Cntlr. | NIC_I/F | USB_I/F |
|---|---|---|---|---|
| INTA- | INTA- | -- | -- | -- |
| INTB- | INTB- | INTB- | -- | -- |
| INTC- | -- | -- | -- | -- |
| INTD- | -- | -- | INTA- | INTD- |

NOTE:

Interrupts generated by PCI devices can be configured to share the standard AT (IRQn) interrupt lines. Two devices that share a single PCI interrupt must also share the corresponding AT interrupt.

### 4.2.3 PCI POWER MANAGEMENT SUPPORT

This system complies with the PCI Power Management Interface Specification (rev 1.0). The PCI Power Management Enable (PME-) signal is supported by the 810 and 820 chipsets and allows compliant PCI and AGP peripherals to initiate the power management routine.

### 4.2.4 PCI SUB-BUSSES

The 810e chipset implements two data busses that supplement the PCI bus:

- Hub Link Bus
- LPC Bus

#### 4.2.4.1 Hub Link Bus

The 810e chipset implements a Hub Link bus between the GMCH and the ICH. The Hub Link bus handles transactions at a 66-MHz rate using PCI-type protocol. This bus is transparent to software and not accessible for expansion purposes.

#### 4.2.4.2 LPC Bus

The 82801 ICH implements a Low Pin Count (LPC) bus for handling transactions to and from the 47B277 Super I/O Controller as well as the 82802 FWH. The LPC bus transfers data a nibble (4 bits) at a time at a 33-MHz rate. This bus is transparent to software and not accessible for expansion purposes.

### 4.2.5 PCI CONFIGURATION

PCI bus operations, especially those that involve ISA bus interaction, require the configuration of certain parameters such as PCI IRQ routing, DMA channel configuration, RTC control, port decode ranges, and firmware hub (FWH) access control. These parameters are handled by the LPC I/F bridge function (PCI function #0, device 31) of the ICH component and configured through the PCI configuration space registers listed in Table 4-3. Configuration is provided by BIOS at power-up but re-configurable by software.

**Table 4-3.**
LPC Bridge Configuration Registers
(ICH, Function 0, Device 31)

| PCI Config. Addr. | Register | Reset Value | PCI Config. Addr. | Register | Reset Value |
|---|---|---|---|---|---|
| 00, 01h | Vender ID | 8086h | 88h | Device 31 Error Config. | 00h |
| 02, 03h | Device ID | 2410h | 8Ah | Device 31 Error Status | 00h |
| 04, 05h | Command | 000Fh | 90, 91h | PCI DMA Configuration | 0000h |
| 06, 07h | Status | 0280h | A0-CFh | Power Management | |
| 08h | Revision ID | 00h | D0-D3h | General Control | 0's |
| 09-0Bh | Class Code | 00h | D4-D7h | General Status | F00h |
| 0Eh | Header Type | 01h | D8h | RTC Configuration | 00h |
| 40-43hh | ACPI Base Address | 1 | E1h | COM Port Decode Range | 00h |
| 44h | ACPI Control | 00h | E2h | DD & LPT Port Dec. Range | 00h |
| 4E, 4Fh | BIOS Control | 0000h | E3h | FWH Decode Enable | 80h |
| 54h | TCO Control | 80h | E4, E5h | LPC I/F Decode Range 1 | 0000h |
| 58-5Bh | GPIO Base Address | 1 | E6, E7h | LPC I/F Enables | 0000h |
| 5Ch | GPIO Control | 00h | E8h | FWH Select | |
| 60-63h | PCI IRQ Routing Cntrl. | 80h | EC, EDh | LPC I/F Decode Range 2 | 0000h |
| 64h | Serial IRQ Control | 10h | F2, F3h | Functions Disable | 00 |

NOTE: Assume unmarked locations/gaps as reserved.

## 4.3 AGP BUS OVERVIEW

> **NOTE:** This section provides a brief overview of AGP bus operation. For a detailed description of AGP bus operations refer to the *AGP Interface Specification* available at the following AGP forum web site: http://www.agpforum.org/index.htm

The Accelerated Graphics Port (AGP) bus is specifically designed as an economical yet high-performance interface for graphics adapters, especially those designed for 3D operations. The AGP interface is designed to give graphics adapters dedicated pipelined access to system memory for the purpose of off-loading texturing, z-buffering, and alpha blending used in 3D graphics operations. By off-loading a large portion of 3D data to system memory the AGP graphics adapter only requires enough memory for frame buffer (display image) refreshing.

As this system is designed for simplicity of system management, **the AGP bus is not available for expansion purposes.**

### 4.3.1 BUS TRANSACTIONS

The operation of the AGP bus is based on the 66-MHz PCI specification but includes additional mechanisms to increase bandwidth. During the configuration phase the AGP bus acts in accordance with PCI protocol. Once graphics data handling operation is initiated, AGP-defined protocols take effect. The AGP graphics adapter acts generally as the AGP master, but can also behave as a "PCI" target during fast writes from the GMCH or MCH.

Key differences between the AGP interface and the PCI interface are as follows:

- Address phase and associated data transfer phase are disconnected transactions. Addressing and data transferring occur as contiguous actions on the PCI bus. On the AGP bus a request for data and the transfer of data may be separated by other operations.
- Commands on the AGP bus specify system memory accesses only. Unlike the PCI bus, commands involving I/O and configuration are not required or allowed. The system memory address space used in AGP operations is the same linear space used by PCI memory space commands, but is further specified by the graphics address re-mapping table (GART) of the north bridge component.
- Data transactions on the AGP bus involve eight bytes or multiples of eight bytes. The AGP memory addressing protocol uses 8-byte boundaries as opposed to PCI's 4-byte boundaries. If a transfer of less than eight bytes is needed, the remaining bytes are filled with arbitrary data that is discarded by the target.
- Pipelined requests are defined by length or size on the AGP bus. The PCI bus defines transfer lengths with the FRAME- signal.

There are two basic types of transactions on the AGP bus: data requests (addressing) and data transfers. These actions are separate from each other.

#### 4.3.1.1 Data Request

Requesting data is accomplished in one of two ways; either multiplexed addressing (using the AD lines for addressing/data) or demultiplexed ("sideband") addressing (using the SBA lines for addressing only and the AD lines for data only). Even though there are only eight SBA lines (as opposed to the 32 AD lines) sideband addressing maximizes efficiency and throughput by allowing the AD lines to be exclusively used for data transfers. Sideband addressing occurs at the same rate (1X or 2X) as data transfers. The differences in rates will be discussed in the next section describing data transfers. Note also that sideband addressing is limited to 48 bits (address bits 48-63 are assumed zero). The GMCH and MCH components support both SBA and AD addressing, but the method and rate is selected by the AGP graphics adapter.

#### 4.3.1.2 Data Transfers

Data transfers use the AD lines and occur as the result of data requests described previously. Each transaction resulting from a request involves at least eight bytes, requiring the 32 AD lines to handle at least two transfers per request. The 82810e MCH supports two transfer rates: 1X and 2X. Regardless of the rate used, the speed of the bus clock is constant at 66 MHz. The following subsections describe how the use of additional strobe signals makes possible higher transfer rates.

##### AGP 1X Transfers

During a AGP 1X transfer the 66-MHz CLK signal is used to qualify the control and data signals. Each 4-byte data transfer is synchronous with one CLK cycle so it takes two CLK cycles for a minimum 8-byte transfer (Figure 4-4 shows two 8-byte transfers). The GNT- and TRDY- signals retain their traditional PCI functions. The ST0..3 signals are used for priority encoding, with "000" for low priority and "001" indicating high priority. The signal level for AGP 1X transfers may be 3.3 or 1.5 VDC.

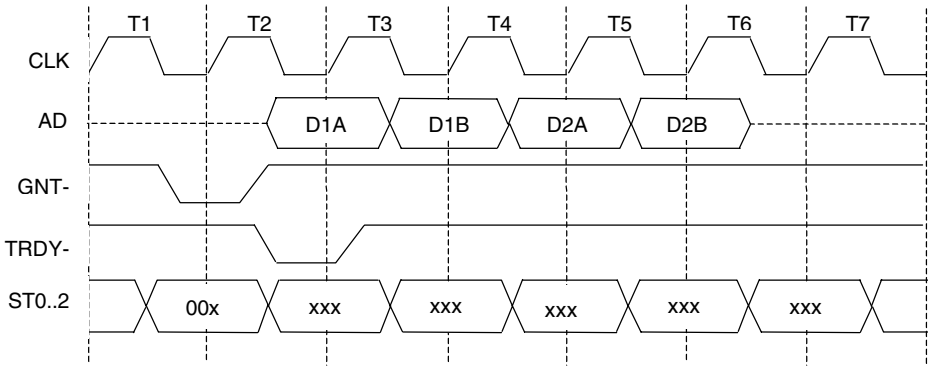



**Figure 4-4.** AGP 1X Data Transfer (Peak Transfer Rate: 266 MB/s)

## AGP 2X Transfers

During AGP 2X transfers, clocking is basically the same as in 1X transfers except that the 66-MHz CLK signal is used to qualify only the control signals. The data bytes are latched by an additional strobe (AD_STBx) signal so that an 8-byte transfer occurs in one CLK cycle (Figure 4-5). The first four bytes (DnA) are latched by the receiving agent on the falling edge of AD_STBx and the second four bytes (DnB) are latched on the rising edge of AD_STBx. The signal level for AGP 2X transfers may be 3.3 or 1.5 VDC.

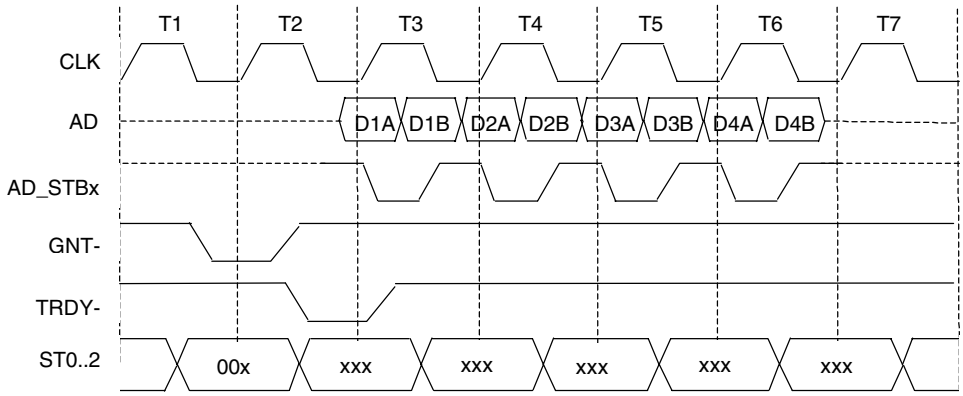



**Figure 4-5.** AGP 2X Data Transfer (Peak Transfer Rate: 532 MB/s)

## 4.3.2 AGP CONFIGURATION

AGP bus operations require the configuration of certain parameters involving system memory access by the AGP graphics adapter. The AGP bus interface is configured as a PCI device integrated within the north bridge (MCH, device 1) component. The AGP function is, from the PCI bus perspective, treated essentially as a PCI/PCI bridge and configured through PCI configuration registers (Table 4-4). Configuration is accomplished by BIOS during POST.

> **NOTE:** Configuration of the AGP bus interface involves functions 0 and 1 of the MCH. Function 0 registers (listed in Table 3-4) include functions that affect basic control (GART) of the AGP.

**Table 4-4.**
PCI/AGP Bridge Function Configuration Registers
(GMCH, Function 1)

| PCI Config. Addr. | Register | Reset Value | PCI Config. Addr. | Register | Reset Value |
|---|---|---|---|---|---|
| 00, 01h | Vender ID | 8086h | 1Bh | Sec. Master Latency Timer | 00h |
| 02, 03h | Device ID | 7191h | 1Ch | I/O Base Address | F0h |
| 04, 05h | Command | 0000h | 1Dh | I/O Limit Address | 00h |
| 06, 07h | Status | 0220h | 1E, 1Fh | Sec. PCI/PCI Status | 02A0h |
| 08h | Revision ID | 00h | 20, 21h | Memory Base Address | FFF0h |
| 0A, 0Bh | Class Code | 0406h | 22, 23h | Memory Limit Address | 0000h |
| 0Eh | Header Type | 01h | 24, 25h | Prefetch Mem. Base Addr. | FFF0h |
| 18h | Primary Bus Number | 00h | 26, 27h | Prefetch Mem. Limit Addr. | 0000h |
| 19h | Secondary Bus Number | 00h | 3Eh | PCI/PCI Bridge Control | 80h |
| 1Ah | Subordinate Bus Number | 00h | 3F-FFh | Reserved | 00h |

NOTE:
Assume unmarked locations/gaps as reserved. Refer to Intel documentation for detailed register descriptions.

The AGP graphics adapter (actually its resident controller) is configured as a standard PCI device.

## 4.4 INTERRUPTS

The microprocessor uses two types of interrupts; maskable and nonmaskable. A maskable interrupt can be enabled or disabled within the microprocessor by the use of the STI and CLI instructions. A nonmaskable interrupt cannot be masked off within the microprocessor but may be inhibited by hardware or software means external to the microprocessor.

### 4.4.1 MASKABLE INTERRUPTS

The maskable interrupt is a hardware-generated signal used by peripheral functions within the system to get the attention of the microprocessor. Peripheral functions produce a unique INTA-D (PCI) or IRQ0-15 (ISA) signal that is routed to interrupt processing logic that asserts the interrupt (INTR-) input to the microprocessor. The microprocessor halts execution to determine the source of the interrupt and then services the peripheral as appropriate.

Figure 4-6 shows the routing of PCI and ISA interrupts. Most IRQs are routed through the I/O controller, which contains a serializing function. A serialized interrupt stream is applied to the 82801 ICH.

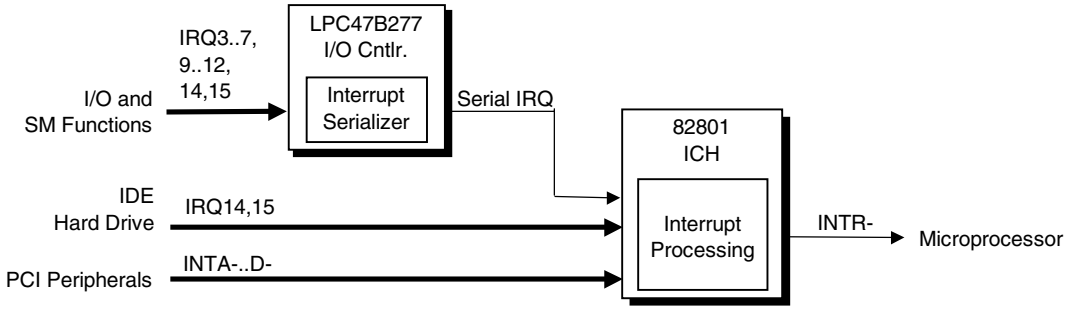



**Figure 4-6.** Maskable Interrupt Processing, Block Diagram

The 82801 ICH component, which includes the equivalent of two 8259 interrupt controllers cascaded together, handles the decoding of the serial interrupt stream (Serial IRQ signal) as well as interrupts IRQ14 and 15 from the IDE hard drives. The ICH also receives the PCI interrupt signals (INTA-..INTD-) from PCI devices. The PCI interrupts can be configured by PCI Configuration Registers 60h..63h to share the standard ISA interrupts (IRQn). The power-up default configuration has the PIRQn disabled. Table 4-13 lists the standard source configuration for maskable interrupts and their priorities. If more than one interrupt is pending, the highest priority (lowest number) is processed first.

The 82801 ICH is configured to handle interrupts in 8259-mode.

**Table 4-5.**
Maskable Interrupt Priorities and Assignments

| Priority | Signal Label | Source (Typical) | Notes |
|---|---|---|---|
| 1 | IRQ0 | Interval timer 1, counter 0 | |
| 2 | IRQ1 | PS/2 Keyboard | [1] |
| 3 | IRQ8- | Real-time clock | |
| 4 | IRQ9 | Unused | |
| 5 | IRQ10 | Unused | |
| 6 | IRQ11 | Unused | |
| 7 | IRQ12 | PS/2 Mouse | [1] |
| 8 | IRQ13 | Coprocessor (math) | |
| 9 | IRQ14 | IDE primary I/F | |
| 10 | IRQ15 | IDE secondary I/F | |
| 11 | IRQ3 | Unused | |
| 12 | IRQ4 | Serial port (COM1) | [1] |
| 13 | IRQ5 | Unused | |
| 14 | IRQ6 | Unused | |
| 15 | IRQ7 | Parallel port (LPT1) | [1] |
| -- | IRQ2 | NOT AVAILABLE (Cascade from interrupt controller 2) | |

NOTE:
[1] Legacy-light models only

Interrupts generated by PCI devices can be configured to share the standard AT (IRQn) interrupt lines. Also, PCI interrupts are hardwired for even distribution to minimize latency (see section 4.2.2 “PCI Interrupt Mapping”).

Maskable Interrupt processing is controlled and monitored through standard AT-type I/O-mapped registers. These registers are listed in Table 4-6.

**Table 4-6.**
Maskable Interrupt Control Registers

| I/O Port | Register |
|---|---|
| 020h | Base Address, Int. Cntlr. 1 |
| 021h | Initialization Command Word 2-4, Int. Cntlr. 1 |
| 0A0h | Base Address, Int. Cntlr. 2 |
| 0A1h | Initialization Command Word 2-4, Int. Cntlr. 2 |

The initialization and operation of the interrupt control registers follows standard AT-type protocol.

## 4.4.2 NON-MASKABLE INTERRUPTS

Non-maskable interrupts cannot be masked (inhibited) within the microprocessor itself but may be maskable by software using logic external to the microprocessor. There are two non-maskable interrupt signals: the NMI- and the SMI-. These signals have service priority over all maskable interrupts, with the SMI- having top priority over all interrupts including the NMI-.

### 4.4.2.1 NMI- Generation

The Non-Maskable Interrupt (NMI-) signal can be generated by one of the following actions:

- Parity errors detected on the ISA bus (activating IOCHK-).
- Parity errors detected on a PCI bus (activating SERR- or PERR-).
- Microprocessor internal error (activating IERRA or IERRB)

The IOCHK-, SERR-, and PERR- signals are routed through the ICH component, which in turn activates the NMI to the microprocessor.

The NMI Status Register at I/O port 061h contains NMI source and status data as follows:

**NMI Status Register 61h**

| Bit | Function |
|---|---|
| 7 | NMI Status:<br>0 = No NMI from system board parity error.<br>1 = NMI requested, read only |
| 6 | IOCHK- NMI:<br>0 = No NMI from IOCHK-<br>1 = IOCHK- is active (low), NMI requested, read only |
| 5 | Interval Timer 1, Counter 2 (Speaker) Status |
| 4 | Refresh Indicator (toggles with every refresh) |
| 3 | IOCHK- NMI Enable/Disable:<br>0 = NMI from IOCHK- enabled<br>1 = NMI from IOCHK- disabled and cleared (R/W) |
| 2 | System Board Parity Error (PERR/SERR) NMI Enable:<br>0 = Parity error NMI enabled<br>1 = Parity error NMI disabled and cleared (R/W) |
| 1 | Speaker Data (R/W) |
| 0 | Inteval Timer 1, Counter 2 Gate Signal (R/W)<br>0 = Counter 2 disabled<br>1 = Counter 2 enabled |

Functions not related to NMI activity.

After the active NMI has been processed, status bits <7> or <6> are cleared by pulsing bits <2> or <3> respectively.

The NMI Enable Register (070h, <7>) is used to enable/disable the NMI signal. Writing 80h to this register masks generation of the NMI-. Note that the lower six bits of register at I/O port 70h affect RTC operation and should be considered when changing NMI- generation status.

#### 4.4.2.2 SMI- Generation

The SMI- (System Management Interrupt) is typically used for power management functions. When power management is enabled, inactivity timers are monitored. When a timer times out, SMI- is asserted and invokes the microprocessor's SMI handler. The SMI- handler works with the APM BIOS to service the SMI- according to the cause of the timeout.

Although the SMI- is primarily used for power managment the interrupt is also employed for the QuickLock/QuickBlank functions as well.

## 4.5 INTERVAL TIMER

The interval timer generates pulses at software (programmable) intervals. A 8254-compatible timer is integrated into the 82801 component. The timer function provides three counters, the functions of which are listed in Table 4-7.

**Table 4-7.**
Interval Timer Functions

| Counter | Function | Gate | Clock In | Clock Out |
|---|---|---|---|---|
| 0 | System Clock | Always on | 1.193 MHz | IRQ0 |
| 1 | Refresh | Always on | 1.193 MHz | Refresh Req. |
| 2 | Speaker Tone | Port 61, bit<0> | 1.193 MHz | Speaker Input |

The interval timer is controlled through the I/O mapped registers listed in Table 4-8.

**Table 4-8.**
Interval Timer Control Registers

| I/O Port | Register |
|---|---|
| 040h | Read or write value, counter 0 |
| 041h | Read or write value, counter 1 |
| 042h | Read or write value, counter 2 |
| 043h | Control Word |

## 4.6 SYSTEM CLOCK DISTRIBUTION

These systems use a CK133 clock generator (for 820-based systems) or a CK Whitney or ICS92250-16 clock generator (for 810/810e-based systems). Table 4-9 lists the system board clock signals and how they are distributed.

**Table 4-9.**
Clock Generation and Distribution

| Frequncy/Signal | Source | Destination |
|---|---|---|
| 66, 100, or 133 MHz (CPUCLK) [1] | CLK Gen. | Processor, GMCH |
| 100 MHz | CK | DIMM sockets |
| 48 MHz | " | 82801 ICH, 47B277 I/O Cntlr. |
| 33 MHz (PCICLK) | " | 82801 ICH |
| 14.31818 MHz | Crystal | CK133 |
| 14.31818 MHz | CLK Gen | 82801 ICH |

NOTE:
[1] Depending on processor speed.

## 4.7 REAL-TIME CLOCK AND CONFIGURATION MEMORY

The Real-time clock (RTC) and configuration memory (also referred to as "CMOS") functions are provided by the 82801 ICH component and is MC146818-compatible. As shown in the following figure, the 82801 ICH component provides 256 bytes of battery-backed RAM divided into two 128-byte configuration memory areas. The RTC uses the first 14 bytes (00-0Dh) of the standard memory area. All locations of the standard memory area (00-7Fh) can be directly accessed using conventional OUT and IN assembly language instructions through I/O ports 70h/71h, although the suggested method is to use the INT15 AX=E823h BIOS call. Also note that CMOS locations above 3Fh are used for the control and status of features that should be handled through BIOS function INT15h, AX=E845h.

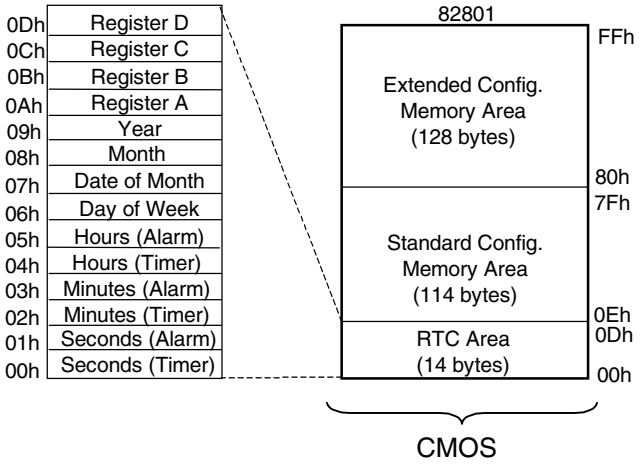



**Figure 4-7.** Configuration Memory Map

A lithium 3-VDC battery is used for maintaining the RTC and configuration memory while the system is powered down. During system operation a wire-Ored circuit allows the RTC and configuration memory to draw power from the power supply. The battery is located in a battery holder on the system board and has a life expectancy of four to eight years. When the battery has expired it is replaced with a Renata CR2032 or equivalent 3-VDC lithium battery.

Table 4-10 lists the mapping of the configuration memory.

**Table 4-10.**
Configuration Memory (CMOS) Map

| Location | Function | Location | Function |
|---|---|---|---|
| 00-0Dh | Real-time clock | 24h | System board ID |
| 0Eh | Diagnostic status | 25h | System architecture data |
| 0Fh | System reset code | 26h | Auxiliary peripheral configuration |
| 10h | Diskette drive type | 27h | Speed control external drive |
| 11h | Reserved | 28h | Expanded/base mem. size, IRQ12 |
| 12h | Hard drive type | 29h | Miscellaneous configuration |
| 13h | Security functions | 2Ah | Hard drive timeout |
| 14h | Equipment installed | 2Bh | System inactivity timeout |
| 15h | Base memory size, low byte/KB | 2Ch | Monitor timeout, Num Lock Cntrl |
| 16h | Base memory size, high byte/KB | 2Dh | Additional flags |
| 17h | Extended memory, low byte/KB | 2Eh-2Fh | Checksum of locations 10h-2Dh |
| 18h | Extended memory, high byte/KB | 30h-31h | Total extended memory tested |
| 19h | Hard drive 1, primary controller | 32h | Century |
| 1Ah | Hard drive 2, primary controller | 33h | Miscellaneous flags set by BIOS |
| 1Bh | Hard drive 1, secondary controller | 34h | International language |
| 1Ch | Hard drive 2, secondary controller | 35h | APM status flags |
| 1Dh | Enhanced hard drive support | 36h | ECC POST test single bit |
| 1Eh | Reserved | 37h-3Fh | Power-on password |
| 1Fh | Power management functions | 40-FFh | Feature Control/Status |

NOTES:
Assume unmarked gaps are reserved.
Higher locations (>3Fh) contain information that should be accessed using the INT15, AX=E845h BIOS function (refer to Chapter 8 for BIOS function descriptions).

## 4.7.1 CMOS ARCHIVE

There is no provision for clearing the contents of the configuration memory (CMOS). During POST, a copy of the CMOS data is written to a sector of the 82802 FWH. This means that changes to CMOS will be stored on the following boot. Should the system hang during boot as the result of corrupted CMOS data, then a Power Button Override boot should be invoked with the following procedure:

1. Initiate a power cycle by pressing and releasing the Power button, then pressing and holding the power button for about four seconds so that the system should record a power button override event.
2. Power down the system.
3. Press and release the power button, initiating a boot sequence. The system should detect the occurrence of a power button override event and will load the CMOS archive data stored in the FWH allowing a successful boot. All passwords and settings used in the previous successful boot would be restored.

## 4.7.2 STANDARD CMOS LOCATIONS

The following paragraphs describe standard configuration memory locations 0Ah-3Fh. These locations are accessible through using OUT/IN assembly language instructions using port 70/71h or BIOS function INT15, AX=E823h.

### RTC Control Register A, Byte 0Ah

| Bit | Function |
|---|---|
| 7 | Update in Progress. Read only.<br>0 = Time update will not occur before 2444 us<br>1 = Time update will occur within 2444 us |
| 6..4 | Divider Chain Control. R/W.<br>00x = Oscillator disabled.<br>010 = Normal operation (time base frequency = 32.768 KHz).<br>11x = Divider chain reset. |
| 3..0 | Periodic Interrupt Control. R/W. Specifies the periodic interrupt interval.<br>0000 = none 1000 = 3.90625 ms<br>0001 = 3.90625 ms 1001 = 7.8125 ms<br>0010 = 7.8125 ms 1010 = 15. 625 ms<br>0011 = 122.070 us 1011 = 31.25 ms<br>0100 = 244.141 us 1100 = 62.50 ms<br>0101 = 488.281 us 1101 = 125 ms<br>0110 = 976.562 us 1110 = 250 ms<br>0111 = 1.953125 ms 1111 = 500 ms |

### RTC Control Register B, Byte 0Bh

| Bit | Function |
|---|---|
| 7 | Time Update Enable/disable<br>0 = Normal operation, 1 = Disable time updating for time set |
| 6 | Periodic Interrupt Enable/Disable.<br>0 = Disable, 1 = Enable interval specified by Register A |
| 5 | Alarm Interrupt Enable/disable<br>0 = Disabled, 1 = Enabled |
| 4 | End-of-Update Interrupt Enable/Disable<br>0 = Disabled, 1 = Enabled |
| 3 | Reserved (read 0) |
| 2 | Time/Date Format Select<br>0 = BCD format, 1 = Binary format |
| 1 | Time Mode<br>0 = 12-hour mode, 1 = 24-hour mode |
| 0 | Automatic Daylight Savings Time Enable/Disable<br>0 = Disable<br>1 = Enable (Advance 1 hour on 1st Sunday in April, retreat 1 hour on last Sunday in October). |

### RTC Status Register C, Byte 0Ch

| Bit | Function |
|---|---|
| 7 | If set, interrupt output signal active (read only) |
| 6 | If set, indicates periodic interrupt flag |
| 5 | If set, indicates alarm interrupt |
| 4 | If set, indicates end-of-update interrupt |
| 3..0 | Reserved |

### RTC Status Register D, Byte 0Dh

| Bit | Function |
|---|---|
| 7 | RTC Power Status<br>0 = RTC has lost power<br>1 = RTC has not lost power |
| 6..0 | Reserved |

**Configuration Byte 0Eh, Diagnostic Status**

Default Value = 00h

This byte contains diagnostic status data.

**Configuration Byte 0Fh, System Reset Code**

Default Value = 00h

This byte contains the system reset code.

**Configuration Byte 10h, Diskette Drive Type**

| Bit | Function |
|---|---|
| 7..4 | Primary (Drive A) Diskette Drive Type |
| 3..0 | Secondary (Drive B) Diskette Drive Type |

Valid values for bits <7..4> and bits <3..0>:

0000 = Not installed
0001 = 360-KB drive
0010 = 1.2-MB drive
0011 = 720-KB drive
0100 = 1.44-MB/1.25-MB drive
0110 = 2.88-MB drive
(all other values reserved)

**Configuration Byte 12h, Hard Drive Type**

| Bit | Function |
|---|---|
| 7..4 | Primary Controller 1, Hard Drive 1 Type:<br>0000 = none 1000 = Type 8<br>0001 = Type 1 1001 = Type 9<br>0010 = Type 2 1010 = Type 10<br>0011 = Type 3 1011 = Type 11<br>0100 = Type 4 1100 = Type 12<br>0101 = Type 5 1101 = Type 13<br>0110 = Type 6 1110 = Type 14<br>0111 = Type 7 1111 = other (use bytes 19h) |
| 3..0 | Primary Controller 1, Hard Drive 2 Type:<br>0000 = none 1000 = Type 8<br>0001 = Type 1 1001 = Type 9<br>0010 = Type 2 1010 = Type 10<br>0011 = Type 3 1011 = Type 11<br>0100 = Type 4 1100 = Type 12<br>0101 = Type 5 1101 = Type 13<br>0110 = Type 6 1110 = Type 14<br>0111 = Type 7 1111 = other (use bytes 1Ah) |

**Configuration Byte 13h, Security Functions**

Default Value = 00h

| Bit | Function |
|---|---|
| 7 | Reserved |
| 6 | QuickBlank Enable After Standby:<br>0 = Disable<br>1 = Enable |
| 5 | Administrator Password:<br>0 = Not present<br>1 = Present |
| 4 | Reserved |
| 3 | Diskette Boot Enable:<br>0 = Enable<br>1 = Disable |
| 2 | QuickLock Enable:<br>0 = Disable<br>1 = Enable |
| 1 | Network Server Mode/Security Lock Override:<br>0 = Disable<br>1 = Enable |
| 0 | Password State (Set by BIOS at Power-up)<br>0 = Not set<br>1 = Set |

**Configuration Byte 14h, Equipment Installed**

Default Value (standard configuration) = 03h

| Bit | Function |
|---|---|
| 7,6 | No. of Diskette Drives Installed:<br>00 = 1 drive 10 = 3 drives<br>01 = 2 drives 11 = 4 drives |
| 5..2 | Reserved |
| 1 | Coprocessor Present<br>0 = Coprocessor not installed<br>1 = Coprocessor installed |
| 0 | Diskette Drives Present<br>0 = No diskette drives installed<br>1 = Diskette drive(s) installed |

**Configuration Bytes 15h and 16h, Base Memory Size**

Default Value = 280h

Bytes 15h and 16h hold a 16-bit value that specifies the base memory size in 1-KB (1024) increments. Valid base memory sizes are 512 and 640 kilobytes .

**Configuration Bytes 17h and 18h, Extended Memory Size**

Bytes 17h and 18h hold a 16-bit value that specifies the extended memory size in 1-KB increments.

### Configuration Bytes 19h-1Ch, Hard Drive Types

Byte 19h contains the hard drive type for drive 1 of the primary controller if byte 12h bits <7..4> hold 1111b. Byte 1Ah contains the hard drive type for drive 2 of the primary controller if byte 12h bits <3..0> hold 1111b. Bytes1Bh and 1Ch contain the hard drive types for hard drives 1 and 2 of the secondary controller.

### Configuration Byte 1Dh, Enhanced IDE Hard Drive Support

Default Value = F0h

| Bit | Function |
|---|---|
| 7 | EIDE - Drive C (83h) |
| 6 | EIDE - Drive D (82h) |
| 5 | EIDE - Drive E (81h) |
| 4 | EIDE - Drive F (80h) |
| 3..0 | Reserved |

Values for bits <7..4> :

0 = Disable

1 = Enable for auto-configure

### Configuration Byte 1Fh, Power Management Functions

Default Value = 00h

| Bit | Function |
|---|---|
| 7..4 | Reserved |
| 3 | Slow Processor Clock for Low Power Mode<br>0 = Processor runs at full speed<br>1 = Processor runs at slow speed |
| 2 | Reserved |
| 1 | Monitor Off Mode<br>0 = Turn monitor power off after 45 minutes in standby<br>1 = Leave monitor power on |
| 0 | Energy Saver Mode Indicator (Blinking LED)<br>0 = Disable<br>1 = Enable |

### Configuration Byte 24h, System Board Identification

Default Value = 7Eh

Configuration memory location 24h holds the system board ID.

### Configuration Byte 25h, System Architecture Data

Default Value = 0Bh

| Bit | Function |
|---|---|
| 7..4 | Reserved |
| 3 | Unmapping of ROM:<br>0 = Allowed<br>1 = Not allowed |
| 2 | Reserved |
| 1,0 | Diagnostic Status Byte Address<br>00 = Memory locations 80C00000h-80C00004h<br>01 = I/O ports 878h-87Ch<br>11 = neither place |

### Configuration Byte 26h, Auxiliary Peripheral Configuration

Default Value = 00h

| Bit | Function |
|---|---|
| 7,6 | I/O Delay Select<br>00 = 420 ns (default)<br>01 = 300 ns<br>10 = 2600 ns<br>11 = 540 ns |
| 5 | Alternative A20 Switching<br>0 = Disable port 92 mode<br>1 = Enable port 92 mode |
| 4 | Bi-directional Print Port Mode<br>0 = Disabled<br>1 = Enabled |
| 3 | Graphics Type<br>0 = Color<br>1 = Monochrome |
| 2 | Hard Drive Primary/Secondary Address Select:<br>0 = Primary<br>1 = Secondary |
| 1 | Diskette I/O Port<br>0 = Primary<br>1 = Secondary |
| 0 | Diskette I/O Port Enable<br>0 = Primary<br>1 = Secondary |

### Configuration Byte 27h, Speed Control/External Drive

Default Value = 00h

| Bit | Function |
|---|---|
| 7 | Boot Speed<br>0 = Max MHz<br>1 = Fast speed |
| 6..0 | Reserved |

### Configuration Byte 28h, Expanded and Base Memory, IRQ12 Select

Default Value = 00h

| Bit | Function |
|---|---|
| 7 | IRQ12 Select<br>0 = Mouse<br>1 = Expansion bus |
| 6,5 | Base Memory Size:<br>00 = 640 KB<br>01 = 512 KB<br>10 = 256 KB<br>11 = Invalid |
| 4..0 | Internal Compaq Memory:<br>00000 = None<br>00001 = 512 KB<br>00010 = 1 MB<br>00011 = 1.5 MB<br>.<br>.<br>11111 = 15.5 MB |

### Configuration Byte 29h, Miscellaneous Configuration Data

Default Value = 00h

| Bit | Function |
|---|---|
| 7..5 | Reserved |
| 4 | Primary Hard Drive Enable (Non-PCI IDE Controllers)<br>0 = Disable<br>1 = Enable |
| 3..0 | Reserved |

### Configuration Byte 2Ah, Hard Drive Timeout

Default Value = 02h

| Bit | Function |
|---|---|
| 7..5 | Reserved |
| 4..0 | Hard Drive Timeout (index to SIT timeout record) |

### Configuration Byte 2Bh, System Inactivity Timeout

Default Value = 23h

| Bit | Function |
|---|---|
| 7 | Reserved |
| 6,5 | Power Conservation Boot<br>00 = Reserved<br>01 = PC on<br>10 = PC off<br>11 = Reserved |
| 4..0 | System Inactive Timeout. (Index to SIT system timeout record)<br>00000 = Disabled |

### Configuration Byte 2Ch, ScreenSave and NUMLOCK Control

Default Value = 00h

| Bit | Function |
|---|---|
| 7 | Reserved |
| 6 | Numlock Control<br>0 = Numlock off at power on<br>1 = Numlock on at power on |
| 5 | Screen Blank Control:<br>0 = No screen blank<br>1 = Screen blank w/QuickLock |
| 4..0 | ScreenSave Timeout. (Index to SIT monitor timeout record)<br>000000 = Disabled |

### Configuration Byte 2Dh, Additional Flags

Default Value = 00h

| Bit | Function |
|---|---|
| 7..5 | Reserved |
| 4 | Memory Test<br>0 = Test memory on power up only<br>1 = Test memory on warm boot |
| 3 | POST Error Handling (BIOS Defined)<br>0 = Display "Press F1 to Continue" on error<br>1 = Skip F1 message |
| 2..0 | Reserved |

### Configuration Byte 2Eh, 2Fh, Checksum

These bytes hold the checksum of bytes 10h to 2Dh.

### Configuration Byte 30h, 31h, Total Extended Memory Tested

This location holds the amount of system memory that checked good during the POST.

### Configuration Byte 32h, Century

This location holds the Century value in a binary coded decimal (BCD) format.

### Configuration Byte 33h, Miscellaneous Flags

Default Value = 80h

| Bit | Function |
|---|---|
| 7 | Memory Above 640 KB<br>0 = No, 1 = Yes |
| 6 | Reserved |
| 5 | Weitek Numeric Coprocessor Present:<br>0 = Not installed, 1 = Installed |
| 4 | Standard Numeric Coprocessor Present:<br>0 = Not installed, 1 = Installed |
| 3..0 | Reserved |

### Configuration Byte 34h, International Language Support

Default Value = 00h

**Configuration Byte 35h, APM Status Flags**

Default Value = 11h

| Bit | Function |
|---|---|
| 7..6 | Power Conservation State:<br>00 = Ready<br>01 = Standby<br>10 = Suspend<br>11 = Off |
| 5,4 | Reserved |
| 3 | 32-bit Connection:<br>0 = Disconnected, 1 = Connected |
| 2 | 16-bit Connection<br>0 = Disconnected, 1 = Connected |
| 1 | Real Mode Connection<br>0 = Disconnected, 1 = Connected |
| 0 | Power Management Enable:<br>0 = Disabled<br>1 = Enabled |

**Configuration Byte 36h, ECC POST Test Single Bit Errors**

Default Value = 01h

| Bit | Function |
|---|---|
| 7 | Row 7 Error Detect |
| 6 | Row 6 Error Detect |
| 5 | Row 5 Error Detect |
| 4 | Row 4 Error Detect |
| 3 | Row 3 Error Detect |
| 2 | Row 2 Error Detect |
| 1 | Row 1 Error Detect |
| 0 | Row 0 Error Detect |

0 = No single bit error detected.
1 = Single bit error detected.

**Configuration Byte 37h-3Fh, Power-On Password**

These eight locations hold the power-on password.

## 4.7.3 CMOS FEATURE BITS

Configuration memory above location 3Fh is used for storing special features that are accessed using BIOS function INT15, AX=E845h. Refer to Chapter 8 for more information on accessing the feature bits with BIOS.

## 4.8 SYSTEM MANAGEMENT

This section describes functions having to do with security, power management, temperature, and overall status. These functions are handled by hardware and firmware (BIOS) and generally configured through the Setup utility.

### 4.8.1 SECURITY FUNCTIONS

These systems include various features that provide different levels of security. Note that this subsection describes **only the hardware/firmware functionality** (including that supported by Setup) and does not describe security features that may be provided by Setup and/or the operating system and application software.

#### 4.8.1.1 System Passwords

This system supports two passwords; Setup and Power-On, either or both of which may be enabled through Setup.

> **NOTE:** The system hardware does not provide a CMOS-clearing feature, therefore should both the Setup and Power-On password be lost or forgotten then a special utility and BIOS function is required, allowing the use of a service password based on the unit serial number and date. **The utility can be invoked only as a network application through Compaq Customer Support.**

##### Setup Password

The Setup password is enabled and entered through the Setup utility. Once set, any changes affected through Setup require the Setup password to be entered. Should the Setup password be forgotten the Setup utility will be un-accessible for changes. Should the Power On password be enabled but forgotten, the Setup password may be used to access the Setup utility and a new Power On password be set.

##### Power On Password

The Power On password is enabled and set through the Setup utility. Once set, the boot sequence can be completed only when the correct Power On password is entered.

#### 4.8.1.2 DriveLock Passwords

This system supports the DriveLock security feature for a compatible hard drive installed in the Multibay. DriveLock, when enabled, prevents unauthorized access to hard drive data by requiring a master and/or user password to be entered for access to data on the hard drive. Although this function is configured through the Setup utility, the password information is stored in a reserved area on the hard drive (i.e., the password(s) move(s) with the hard drive).

> **NOTE:** The DriveLock feature is designed primarily for business environments, especially where a removable Multibay hard drive(s) may be shared between several systems. Since the loss of (forgetting) both DriveLock passwords to a drive will result in that drive being unusable, it is strongly advised that this feature be invoked and managed by a system administrator. For detailed user information consult the appropriate user/reference guide for this system.

### 4.8.2 POWER MANAGEMENT

This system provides baseline hardware support of ACPI- and APM-compliant firmware and software. Key power-consuming components (processor, chipset, I/O controller, and fan) can be placed into a reduced power mode either automatically or by user control. The system can then be brought back up ("wake-up") by events defined by the ACPI specification. The ACPI wake-up events supported by this system are listed as follows:

| ACPI Wake-Up Event | System Wakes From |
|---|---|
| Power Button | Suspend or soft-off |
| RTC Alarm | Suspend or soft-off |
| Wake On LAN (w/NIC) | Suspend or soft-off |
| PME | Suspend or soft-off |
| Serial Port Ring | Suspend or soft-off |
| USB | Suspend only |
| Keyboard | Suspend only |
| Mouse | Suspend only |

### 4.8.3 THERMAL SENSING AND COOLING

All systems feature a variable-speed fan (mounted as a part of the power supply assembly) controlled by thermal sensing logic. All systems also include a header for connection to a fan that may be included in some processor upgrade kits (known as "boxed processors").

The system should be operated with all covers in place to ensure proper cooling of the system board components.

## 4.9 SYSTEM I/O MAP

Table 4-20 lists the fixed addresses of the input/output (I/O) ports.

**Table 4-20.**
System I/O Map

| I/O Port | Function |
|---|---|
| 0000..000Fh | DMA Controller 1 |
| 0020..0021h | Interrupt Controller 1 |
| 0040..0043h | Timer 1 |
| 0060h | Keyboard Controller Data Byte |
| 0061h | NMI, Speaker Control |
| 0064h | Keyboard Controller Command/Status Byte |
| 0070h | NMI Enable, RTC/Lower CMOS Index |
| 0071h | RTC Data |
| 0080..008Fh | DMA Page Registers |
| 0092h | Port A, Fast A20/Reset |
| 00A0..00A1h | Interrupt Controller 2 |
| 00B2h, 00B3h | APM Control/Status Ports |
| 00C0..00DFh | DMA Controller 2 |
| 0170..0177h | Hard Drive (IDE) Controller 2 |
| 01F0..01FFh | Hard Drive (IDE) Controller 1 |
| 0201..024Fh | Audio subsystem control (primary & secondary addresses) |
| 0278..027Bh | Parallel Port (LPT2) |
| 02F8..02FFh | Serial Port (COM2) |
| 0371.. 0375h | Diskette Drive Controller Alternate Addresses |
| 0376h | IDE Controller Alternate Address |
| 0377h | IDE Controller Alternate Address, Diskette Drive Controller Alternate Address |
| 0378..037Fh | Parallel Port (LPT1) |
| 0388..038Bh | FM synthesizer (alias addresses) |
| 03B0..03DFh | Graphics Controller |
| 03E8..03EFh | Serial Port (COM3) |
| 03F0..03F5h | Diskette Drive Controller Primary Addresses |
| 03F6, 03F7h | Diskette Drive Controller Primary Addresses, Hard Drive Controller Primary Addresses |
| 03F8..03FFh | Serial Port (COM1) |
| 04D0, 04D1h | Master, Slave Edge/Level INTR Control Register |
| 0C00, 0C01h | PCI IRQ Mapping Index, Data |
| 0C06, 0C07h | Reserved - Compaq proprietary use only |
| 0C50, 0C51h | System Management Configuration Registers (Index, Data) |
| 0C52h | General Purpose Port |
| 0C7Ch | Machine ID |
| 0CF8h | PCI Configuration Address (dword access only) |
| 0CF9h | Reset Control Register |
| 0CFCh | PCI Configuration Data (byte, word, or dword access) |
| FF00..FF07h | IDE Bus Master Register |

NOTE: Assume unmarked gaps are reserved/unused.

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# Chapter 5
# INPUT/OUTPUT INTERFACES

## 5.1 INTRODUCTION

This chapter describes the standard (i.e., system board) interfaces that provide input and output (I/O) porting of data and specifically discusses interfaces that are controlled through I/O-mapped registers. The following I/O interfaces are covered in this chapter:



## 5.2 ENHANCED IDE INTERFACE

The enhanced IDE (EIDE) interface consists of primary and secondary controllers integrated into the 82801 ICH component of the chipset. The system board includes two IDE connectors, a 40-pin connector that is associated with the primary controller that controls the internal hard drive and a 50-pin connector associated with the secondary controller that controls the device in the Multibay. Each controller can be configured independently for the following modes of operation:

- Programmed I/O (PIO) mode – CPU controls drive transactions through standard I/O mapped registers of the IDE drive.
- 8237 DMA mode – CPU offloads drive transactions using DMA protocol with transfer rates up to 16 MB/s.
- Ultra ATA/33 and /66 modes – Preferred bus mastering source-synchronous protocol providing transfer rates of 33 and 66 MB/s respectively.

> **NOTE:** Although the EIDE interface can electrically handle four EIDE devices, the form factor of the unit chassis allows only two devices to be installed.

### 5.2.1 IDE PROGRAMMING

The IDE interface is configured as a PCI device during POST and controlled through I/O-mapped registers at runtime.

Hard drives types not found in the ROM's parameter table are automatically configured as to (soft)type by DOS as follows:

Primary controller: drive 0, type 65; drive 1, type 66
Secondary controller: drive 0, type 68; drive 1, type 15

Non-DOS (non-Windows) operating systems may require using Setup (F10) for drive configuration.

### 5.2.1.1 IDE Configuration Registers

The IDE controller is configured as a PCI device with bus mastering capability. The PCI configuration registers for the IDE controller function (PCI device #31, function #1) are listed in Table 5-1.

**Table 5-1.**
EIDE PCI Configuration Registers (82801, Device 31/Function 1)

| PCI Conf. Addr. | Register | Reset Value | PCI Conf. Addr. | Register | Reset Value |
|---|---|---|---|---|---|
| 00-01h | Vender ID | 8086h | 24-2Bh | Reserved | 0's |
| 02-03h | Device ID | 2411h | 2C, 2Dh | Subsystem Vender ID | 8086h |
| 04-05h | PCI Command | 0000h | 2E, 2Fh | Subsystem ID | 2411h |
| 06-07h | PCI Status | 0280h | 30-3Fh | Reserved | 0's |
| 08h | Revision ID | 00h | 40-43h | Primary IDE Timing | 0000h |
| 09h | Programming | 80h | 44h | Secondary IDE Timing | 00h |
| 0Ah | Sub-Class | 01h | 48h | Sync. DMA Control | 00h |
| 0Bh | Base Class Code | 01h | 4A-4Bh | Sync. DMA Timing | 0000h |
| 0Dh | Master Latency Timer | 0000h | 54h | EIDE I/O Config.Register | 00h |
| 0Eh | Header Type | 80h | F8-FBh | Manufacturer's ID | |
| 0F-1Fh | Reserved | 00h | FC-FFh | Reserved | |
| 20-23h | BMIDE Base Address | 1h | -- | -- | -- |

NOTE:
Assume unmarked gaps are reserved and/or not used.

### 5.2.1.2 IDE Bus Master Control Registers

The IDE interface can perform PCI bus master operations using the registers listed in Table 5-2. These registers occupy 16 bytes of variable I/O space set by software and indicated by PCI configuration register 20h in the previous table.

**Table 5-2.**
IDE Bus Master Control Registers

| I/O Addr. Offset | Size (Bytes) | Register | Default Value |
|---|---|---|---|
| 00h | 1 | Bus Master IDE Command (Primary) | 00h |
| 02h | 1 | Bus Master IDE Status (Primary) | 00h |
| 04h | 4 | Bus Master IDE Descriptor Pointer (Pri.) | 0000 0000h |
| 08h | 1 | Bus Master IDE Command (Secondary) | 00h |
| 0Ah | 2 | Bus Master IDE Status (Secondary) | 00h |
| 0Ch | 4 | Bus Master IDE Descriptor Pointer (Sec.) | 0000 0000h |

NOTE:
Unspecified gaps are reserved, will return indeterminate data, and should not be written to.

## 5.2.2 IDE CONNECTOR

This system uses a standard 40-pin connector for the primary IDE device and connects (via a cable) to the hard drive installed in the right side drive bay. Note that some signals are re-defined for UATA/33 and UATA/66 modes, which require a special 80-conductor cable (supplied) designed to reduce cross-talk. Device power is supplied through a separate connector.

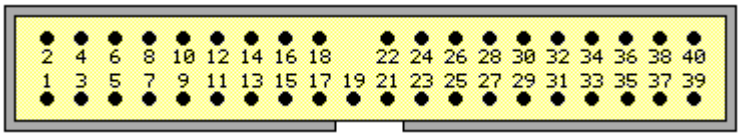



**Figure 5-1.** 40-Pin Primary IDE Connector (on system board).

**Table 5-3.**
40-Pin Primary IDE Connector Pinout

| Pin | Signal | Description | Pin | Signal | Description |
|---|---|---|---|---|---|
| 1 | RESET- | Reset | 21 | DRQ | DMA Request |
| 2 | GND | Ground | 22 | GND | Ground |
| 3 | DD7 | Data Bit <7> | 23 | IOW- | I/O Write [1] |
| 4 | DD8 | Data Bit <8> | 24 | GND | Ground |
| 5 | DD6 | Data Bit <6> | 25 | IOR- | I/O Read [2] |
| 6 | DD9 | Data Bit <9> | 26 | GND | Ground |
| 7 | DD5 | Data Bit <5> | 27 | IORDY | I/O Channel Ready [3] |
| 8 | DD10 | Data Bit <10> | 28 | CSEL | Cable Select |
| 9 | DD4 | Data Bit <4> | 29 | DAK- | DMA Acknowledge |
| 10 | DD11 | Data Bit <11> | 30 | GND | Ground |
| 11 | DD3 | Data Bit <3> | 31 | IRQn | Interrupt Request [4] |
| 12 | DD12 | Data Bit <12> | 32 | IO16- | 16-bit I/O |
| 13 | DD2 | Data Bit <2> | 33 | DA1 | Address 1 |
| 14 | DD13 | Data Bit <13> | 34 | DSKPDIAG | Pass Diagnostics |
| 15 | DD1 | Data Bit <1> | 35 | DA0 | Address 0 |
| 16 | DD14 | Data Bit <14> | 36 | DA2 | Address 2 |
| 17 | DD0 | Data Bit <0> | 37 | CS0- | Chip Select |
| 18 | DD15 | Data Bit <15> | 38 | CS1- | Chip Select |
| 19 | GND | Ground | 39 | HDACTIVE- | Drive Active (front panel LED) [5] |
| 20 | -- | Key | 40 | GND | Ground |

NOTES:

[1] On UATA/33 and /66 modes, re-defined as STOP.
[2] On UATA/33 and /66 mode reads, re-defined as DMARDY-.
On UATA/33 and /66 mode writes, re-defined as STROBE.
[3] On UATA/33 and /66 mode reads, re-defined as STROBE-.
On UATA/33 and /66 mode writes, re-defined as DMARDY-.
[4] Primary connector wired to IRQ14, secondary connector wired to IRQ15.
[5] Pin 39 is used for spindle sync and drive activity (becomes SPSYNC/DACT-) when synchronous drives are connected.

The system board includes a 50-pin connector for the secondary IDE drive that is installed in the MultiBay mounting position on the left side of the chassis. This interface includes power and audio signals. The 50-pin system/daughter board connector is illustrated below followed by the pinout.

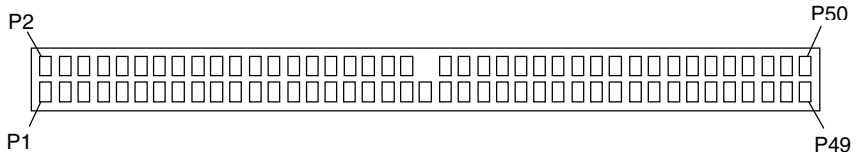



**Figure 5-2.** 50-Pin Secondary IDE Connector (on system and daughter boards).

**Table 5-4.**
50-Pin Secondary IDE Connector Pinout

| Pin | Signal | Description | Pin | Signal | Description |
|---|---|---|---|---|---|
| 1 | AUD L | Left channel audio | 2 | AUD R | Right channel audio |
| 3 | AUD RTN | Audio return | 4 | AUD RTN | Audio return |
| 5 | NC | Not connected | 6 | MBAY | Multibay device sense |
| 7 | RST | Reset | 8 | GND | Ground |
| 9 | D7 | Data Bit <7> | 10 | D8 | Data Bit <8> |
| 11 | D6 | Data Bit <6> | 12 | D9 | Data Bit <9> |
| 13 | D5 | Data Bit <5> | 14 | D10 | Data Bit <10> |
| 15 | D4 | Data Bit <4> | 16 | D11 | Data Bit <11> |
| 17 | D3 | Data Bit <3> | 18 | D12 | Data Bit <12> |
| 19 | D2 | Data Bit <2> | 20 | D13 | Data Bit <13> |
| 21 | D1 | Data Bit <1> | 22 | D14 | Data Bit <14> |
| 23 | D0 | Data Bit <0> | 24 | D15 | Data Bit <15> |
| 25 | GND | Ground | 26 | -- | (Key Space) |
| 27 | DDRQ1 | Data request | 28 | GND | Ground |
| 29 | I/O W- | I/O write | 30 | GND | Ground |
| 31 | I/O R- | I/O read | 32 | GND | Ground |
| 33 | I/OCHRDY | I/O channel ready | 34 | P_ALE | Cable select |
| 35 | ACK1- | Acknowledge | 36 | GND | Ground |
| 37 | IRQ15 | Interrupt request 15 | 38 | IO16 | 16-bit I/O transfer |
| 39 | AD1 | Address bit <1> | 40 | PDIAG | Diagnostic |
| 41 | AD0 | Address bit <0> | 42 | AD2 | Address bit <2> |
| 43 | CS1 | Chip select <1> | 44 | CS3 | Chip select <3> |
| 45 | ACT- | Activity | 46 | GND | Ground |
| 47 | Vcc | +5 VDC | 48 | Vcc | +5 VDC logic power |
| 49 | GND | Ground | 50 | NC | Not connected |

## 5.3 DISKETTE DRIVE INTERFACE

**NOTE:** The Compaq iPAQ **does not** support a diskette drive. However, the LPC47B277 I/O controller contains a diskette drive controller that may need to be enabled (with Setup) to satisfy the requirements of some operating systems. This will result in device manager applications indicating the presence of a diskette drive that in fact is **not** available.

## 5.4 SERIAL INTERFACE

The legacy-light models include a serial interface to transmit and receive asynchronous serial data with external devices. The serial interface function is provided by the LPC47B277 I/O controller component that includes a NS16C550-compatible UART.

△ **NOTE:** Legacy-free models do not have an externally accessible serial port, but do have an internal serial header to satisfy the serial port requirements of some operating systems.

The UART supports the standard baud rates up through 115200, and also special high speed rates of 239400 and 460800 baud. The baud rate of the UART is typically set to match the capability of the connected device. While most baud rates may be set at runtime, **baud rates 230400 and 460800 must be set during the configuration phase.**

### 5.4.1 RS-232 INTERFACE

On the legacy-light system, the UART is associated with a DB-9 connector that complies with EIA standard RS-232-C. The DB-9 connector is shown in the following figure and the pinout of the connector is listed in Table 5-5.

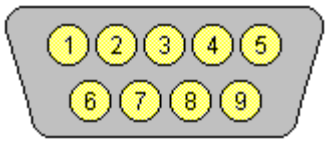



**Figure 5-3.** Serial Interface Connector (Male DB-9 as viewed from rear of chassis)

**Table 5-5.**
DB-9 Serial Connector Pinout

| Pin | Signal | Description | Pin | Signal | Description |
|---|---|---|---|---|---|
| 1 | CD | Carrier Detect | 6 | DSR | Data Set Ready |
| 2 | RX Data | Receive Data | 7 | RTS | Request To Send |
| 3 | TX Data | Transmit Data | 8 | CTS | Clear To Send |
| 4 | DTR | Data Terminal Ready | 9 | RI | Ring Indicator |
| 5 | GND | Ground | -- | -- | -- |

The standard RS-232-C limitation of 50 feet (or less) of cable between the DTE (computer) and DCE (modem) should be followed to minimize transmission errors. Higher baud rates may require shorter cables.

## 5.4.2 SERIAL TEST INTERFACE

Legacy-free systems do not provide an externally accessible serial port but do include a serial header connector on the system board to satisfy some the requirements of some operating systems. The test header and pinout is shown in the following figure:

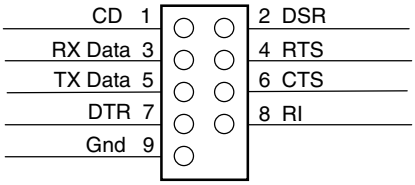



**Figure 5-4.** Serial Interface Header (on legacy-free system board)

## 5.4.3 SERIAL INTERFACE PROGRAMMING

Programming the serial interfaces consists of configuration, which occurs during POST, and control, which occurs during runtime.

### 5.4.3.1 Serial Interface Configuration

The serial interface must be configured for a specific address range (COM1, COM2, etc.) and also must be activated before it can be used. Address selection and activation of the serial interface are affected through the PnP configuration registers of the LPC47B277 I/O controller. The serial interface configuration registers are listed in the following table:

**Table 5-6.**
Serial Interface Configuration Registers

| Index Address | Function | R/W |
|---|---|---|
| 30h | Activate | R/W |
| 60h | Base Address MSB | R/W |
| 61h | Base Address LSB | R/W |
| 70h | Interrupt Select | R/W |
| F0h | Mode Register | R/W |

NOTE:
Refer to LPC47B277 data sheet for detailed register information.

### 5.4.3.2 Serial Interface Control

The BIOS function INT 14 provides basic control of the serial interface. The serial interface can be directly controlled by software through the I/O-mapped registers listed in Table 5-7.

**Table 5-7.**
Serial Interface Control Registers

| COM1 Addr. | COM2 Addr. | Register | R/W |
|---|---|---|---|
| 3F8h | 2F8h | Receive Data Buffer | R |
| | | Transmit Data Buffer | W |
| | | Baud Rate Divisor Register 0 (when bit 7 of Line Control Reg. Is set) | W |
| 3F9h | 2F9h | Baud Rate Divisor Register 1 (when bit 7 of Line Control Reg. Is set) | W |
| | | Interrupt Enable Register:<br><7..4> Reserved (always 0's)<br><3> Modem status interrupt enable (active high) (CTS, DSR, RI, CD)<br><2> Rx line status interrupt enable (active high) (Overrun, parity, framing error)<br><1> Tx holding register empty interrupt enable (active high)<br><0> Baud rate divisor interrupt enable (active high) | R/W |
| 3FAh | 2FAh | Interrupt ID Register:<br><7,6> FIFO Enable/Disable: 0 = disable, 1 = enable<br><5,4> Reserved<br><3..1> Interrupt Source:<br>000 = Modem status 100,101 = Reserved<br>001 = TX holding reg. Empty 110 = Character time-out<br>010 = RX data available 111 = Reserved<br>011 = RX line status<br><0> Interrupt pending (if cleared) | R |
| | | FIFO Control Register:<br><7,6> RX Trigger Level: 00 = 1 byte, 01 = 4 bytes, 10 = 8 bytes, 11 = 14 bytes<br><5..3> Rerserved<br><2> TX FIFO reset (active high)<br><1> RX FIFO reset (active high)<br><0> FIFO Enable/Disable: 0 = Disable TX/RX FIFO's, 1 = Enable TX/RX FIFO's | W |
| 3FBh | 2FBh | Line Control Register:<br><7> Register acces control:<br>0 = RX buffer, TX holding, divisor rate registers are accessable.<br>1 = Divisor rate register is accessable<br><6> Break control (forces SOUT singla low if set)<br><5> Stick parity (if set, even parity bit is 0, odd parity bit is 1)<br><4> Parity type: 0 = odd, 1 = even<br><3> Parity enable: 0 = disabled, 1 = enabled<br><2> Stop bit: 0 = 1 stop bit, 1 = 2 stop bits<br><1,0> Word size: 00 = 5 bits, 01 = 6 bits, 10 = 7 bits, 11 = 8 bits | R/W |
| 3FCh | 2FCh | Modem Control Register:<br><7..5> Reserved<br><4> Internal loopback enabled (if set)<br><3> Serial I/F interrupts enabled (if set)<br><2> Reserved<br><1> RTS signal active (if set)<br><0> DTR signal active (if set) | R/W |
| 3FDh | 2FDh | Line Status Register:<br><7> Parity error, framing error, or Break condition (if set)<br><6> TX holding and TX shift registers are empty (if set)<br><5> TX holding register is empty (if set)<br><4> Break interrupt has occurred (if set)<br><3> Framing error has occurred (if set)<br><2> Parity error has occurred (if set)<br><1> Overrun error has occurred (if set)<br><0> Data register ready to be read (if set) | R |
| 3FEh | 2FEh | Modem Status:<br><7..4> DCD-, RI-, DSR, CTS (respectively) active (if set)<br><3..0> DCD-, RI-, DSR, CTS (respectively) changed state since last read (if set) | R |

## 5.5 PARALLEL INTERFACE

The legacy-light models include a parallel interface for connection to a peripheral device that has a compatible interface, the most common being a printer. The parallel interface function is integrated into theLPC47B277 I/O controller component and provides bi-directional 8-bit parallel data transfers with a peripheral device. The parallel interface supports three main modes of operation:

- Standard Parallel Port (SPP) mode
- Enhanced Parallel Port (EPP) mode
- Extended Capabilities Port (ECP) mode

These three modes (and their submodes) provide complete support as specified for an IEEE 1284 parallel port.

### 5.5.1 STANDARD PARALLEL PORT MODE

The Standard Parallel Port (SPP) mode uses software-based protocol and includes two sub-modes of operation, compatible and extended, both of which can provide data transfers up to 150 KB/s. In the compatible mode, CPU write data is simply presented on the eight data lines. A CPU read of the parallel port yields the last data byte that was written.

The following steps define the standard procedure for communicating with a printing device:

1. The system checks the Printer Status register. If the Busy, Paper Out, or Printer Fault signals are indicated as being active, the system either waits for a status change or generates an error message.
2. The system sends a byte of data to the Printer Data register, then pulses the printer STROBE signal (through the Printer Control register) for at least 500 ns.
3. The system then monitors the Printer Status register for acknowledgment of the data byte before sending the next byte.

In extended mode, a direction control bit (CTR 37Ah, bit <5>) controls the latching of output data while allowing a CPU read to fetch data present on the data lines, thereby providing bi-directional parallel transfers to occur.

The SPP mode uses three registers for operation: the Data register (DTR), the Status register (STR) and the Control register (CTR). Address decoding in SPP mode includes address lines A0 and A1.

### 5.5.2 ENHANCED PARALLEL PORT MODE

In Enhanced Parallel Port (EPP) mode, increased data transfers are possible (up to 2 MB/s) due to a hardware protocol that provides automatic address and strobe generation. EPP revisions 1.7 and 1.9 are both supported. For the parallel interface to be initialized for EPP mode, a negotiation phase is entered to detect whether or not the connected peripheral is compatible with EPP mode. If compatible, then EPP mode can be used. In EPP mode, system timing is closely coupled to EPP timing. A watchdog timer is used to prevent system lockup.

Five additional registers are available in EPP mode to handle 16- and 32-bit CPU accesses with the parallel interface. Address decoding includes address lines A0, A1, and A2.

### 5.5.3 EXTENDED CAPABILITIES PORT MODE

The Extended Capabilities Port (ECP) mode, like EPP, also uses a hardware protocol-based design that supports transfers up to 2 MB/s. Automatic generation of addresses and strobes as well as Run Length Encoding (RLE) decompression is supported by ECP mode. The ECP mode includes a bi-directional FIFO buffer that can be accessed by the CPU using DMA or programmed I/O. For the parallel interface to be initialized for ECP mode, a negotiation phase is entered to detect whether or not the connected peripheral is compatible with ECP mode. If compatible, then ECP mode can be used.

Ten control registers are available in ECP mode to handle transfer operations. In accessing the control registers, the base address is determined by address lines A2-A9, with lines A0, A1, and A10 defining the offset address of the control register. Registers used for FIFO operations are accessed at their base address + 400h (i.e., if configured for LPT1, then 378h + 400h = 778h).

The ECP mode includes several sub-modes as determined by the Extended Control register. Two submodes of ECP allow the parallel port to be controlled by software. In these modes, the FIFO is cleared and not used, and DMA and RLE are inhibited.

## 5.5.4 PARALLEL INTERFACE PROGRAMMING

Programming the parallel interface consists of configuration, which typically occurs during POST, and control, which occurs during runtime.

### 5.5.4.1 Parallel Interface Configuration

The parallel interface must be configured for a specific address range (LPT1, LPT2, etc.) and also must be enabled before it can be used. When configured for EPP or ECP mode, additional considerations must be taken into account. Address selection, enabling, and EPP/ECP mode parameters of the parallel interface are affected through the PnP configuration registers of the LPC47B347 I/O controller. Address selection and enabling are automatically done by the BIOS during POST but can also be accomplished with the Setup utility and other software.

The parallel interface configuration registers are listed in the following table:

**Table 5-8.**
Parallel Interface Configuration Registers

| Index Address | Function | R/W | Reset Value |
|---|---|---|---|
| 30h | Activate | R/W | 00h |
| 60h | Base Address MSB | R/W | 00h |
| 61h | Base Address LSB | R/W | 00h |
| 70h | Interrupt Select | R/W | 00h |
| 74h | DMA Channel Select | R/W | 04h |
| F0h | Mode Register | R/W | 00h |
| F1h | Mode Register 2 | R/W | 00h |

### 5.5.4.2 Parallel Interface Control

The BIOS function INT 17 provides simplified control of the parallel interface. Basic functions such as initialization, character printing, and printer status are provide by subfunctions of INT 17. The parallel interface is controllable by software through a set of I/O mapped registers. The number and type of registers available depends on the mode used (SPP, EPP, or ECP). Table 5-9 lists the parallel registers and associated functions based on mode.

**Table 5-9.**
Parallel Interface Control Registers

| I/O Address | Register | SPP Mode Ports | EPP Mode Ports | ECP Mode Ports |
|---|---|---|---|---|
| Base | Data | LPT1,2,3 | LPT1,2 | LPT1,2,3 |
| Base + 1h | Printer Status | LPT1,2,3 | LPT1,2 | LPT1,2,3 |
| Base + 2h | Control | LPT1,2,3 | LPT1,2 | LPT1,2,3 |
| Base + 3h | Address | -- | LPT1,2 | -- |
| Base + 4h | Data Port 0 | -- | LPT1,2 | -- |
| Base + 5h | Data Port 1 | -- | LPT1,2 | -- |
| Base + 6h | Data Port 2 | -- | LPT1,2 | -- |
| Base + 7h | Data Port 3 | -- | LPT1,2 | -- |
| Base + 400h | Parallel Data FIFO | -- | -- | LPT1,2,3 |
| Base + 400h | ECP Data FIFO | -- | -- | LPT1,2,3 |
| Base + 400h | Test FIFO | -- | -- | LPT1,2,3 |
| Base + 400h | Configuration Register A | -- | -- | LPT1,2,3 |
| Base + 401h | Configuration Register B | -- | -- | LPT1,2,3 |
| Base + 402h | Extended Control Register | -- | -- | LPT1,2,3 |

Base Address:
LPT1 = 378h
LPT2 = 278h
LPT3 = 3BCh

The following paragraphs describe the individual registers. Note that only the LPT1-based addresses are given in these descriptions.

#### Data Register, I/O Port 378h

Data written to this register is presented to the data lines D0-D7. A read of this register when in SPP-compatible mode yields the last byte written. A read while in SPP-extended or ECP mode yields the status of data lines D0-D7 (i.e., receive data).

In ECP mode in the forward (output) direction, a write to this location places a tagged command byte into the FIFO and reads have no effect.

### Status Register, I/O Port 379h, Read Only

This register contains the current printer status. Reading this register clears the interrupt condition of the parallel port.

| Bit | Function |
|---|---|
| 7 | Printer Busy (if 0) |
| 6 | Printer Acknowledgment Of Data Byte (if 0) |
| 5 | Printer Out Of Paper (if 1) |
| 4 | Printer Selected/Online (if 1) |
| 3 | Printer Error (if 0) |
| 2 | Reserved |
| 1 | EPP Interrupt Occurred (if set while in EPP mode) |
| 0 | EPP Timeout Occurred (if set while in EPP mode) |

### Control Register, I/O Port 37Ah

This register provides the printer control functions.

| Bit | Function |
|---|---|
| 7,6 | Reserved |
| 5 | Direction Control for PS/2 and ECP Modes:<br>0 = Forward. Drivers enabled. Port writes to peripheral (default)<br>1 = Backward. Tristates drivers and data is read from peripheral |
| 4 | Acknowledge Interrupt Enable<br>0 = Disable ACK interrupt<br>1 = Enable interrupt on rising edge of ACK |
| 3 | Printer Select (if 0) |
| 2 | Printer Initialize (if 1) |
| 1 | Printer Auto Line Feed (if 0) |
| 0 | Printer Strobe (if 0) |

### Address Register, I/O Port 37Bh (EPP Mode Only)

This register is used for selecting the EPP register to be accessed.

### Data Port Registers 0-3, I/O Ports 37C-Fh (EPP Mode Only)

These registers are used for reading/writing data. Port 0 is used for all transfers. Ports 1-3 are used for transferring the additional bytes of 16- or 32-bit transfers through port 0.

### FIFO Register, I/O Port 7F8h (ECP Mode Only)

While in ECP/forward mode, this location is used for filling the 16-byte FIFO with data bytes. Reads have no effect (except when used in Test mode). While in ECP/backward mode, reads yield data bytes from the FIFO.

### Configuration Register A, I/O Port 7F8h (ECP Mode Only)

A read of this location yields 10h, while writes have no effect.

### Configuration Register B, I/O Port 7F9h (ECP Mode, Read Only)

A read of this location yields the status defined as follows:

| Bit | Function |
|---|---|
| 7 | Reserved (always 0) |
| 6 | Status of Selected IRQ*n*. |
| 5,4 | Selected IRQ Indicator:<br>00 = IRQ7<br>11 = IRQ5<br>All other values invalid. |
| 3 | Reserved (always 1) |
| 2..0 | Reserved (always 000) |

### Extended Control Register B, I/O Port 7FAh (ECP ModeOnly)

This register defines the ECP mode functions.

| Bit | Function |
|---|---|
| 7..5 | ECP Submode Select:<br>000 = Standard forward mode (37Ah <5> forced to 0). Writes are controlled by software and FIFO is reset.<br>001 = PS/2 mode. Reads and writes are software controlled and FIFO is reset.<br>010 = Parallel Port FIFO forward mode (37Ah <5> forced to 0). Writes are hardware controlled.<br>011 = ECP FIFO mode. Direction determined by 37Ah, <5>. Reads and writes are hardware controlled. |
| 4 | ECP Interrupt Mask:<br>0 = Interrupt is generated on ERR- assertion.<br>1 = Interrupt is inhibited. |
| 3 | ECP DMA Enable/Disable.<br>0 = Disabled<br>1 = Enabled |
| 2 | ECP Interrupt Generation with DMA<br>0 = Enabled<br>1 = Disabled |
| 1 | FIFO Full Status (Read Only)<br>0 = Not full (at least 1 empty byte)<br>1 = Full |
| 0 | FIFO Empty Status (Read Only)<br>0 = Not empty (contains at least 1 byte)<br>1 = Empty |

## 5.5.5 PARALLEL INTERFACE CONNECTOR

Figure 5-5 and Table 5-10 show the connector and pinout of the parallel interface connector. Note that some signals are redefined depending on the port's operational mode.

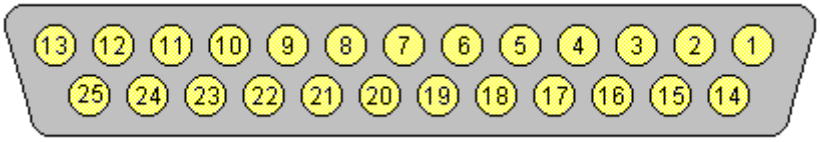



**Figure 5-5.** Parallel Interface Connector (Female DB-25 as viewed from rear of chassis)

**Table 5-10.**
DB-25 Parallel Connector Pinout

| Pin | Signal | Function | Pin | Signal | Function |
|---|---|---|---|---|---|
| 1 | STB- | Strobe / Write [1] | 14 | LF- | Line Feed [2] |
| 2 | D0 | Data 0 | 15 | ERR- | Error [3] |
| 3 | D1 | Data 1 | 16 | INIT- | Initialize Paper [4] |
| 4 | D2 | Data 2 | 17 | SLCTIN- | Select In / Address. Strobe [1] |
| 5 | D3 | Data 3 | 18 | GND | Ground |
| 6 | D4 | Data 4 | 19 | GND | Ground |
| 7 | D5 | Data 5 | 20 | GND | Ground |
| 8 | D6 | Data 6 | 21 | GND | Ground |
| 9 | D7 | Data 7 | 22 | GND | Ground |
| 10 | ACK- | Acknowledge / Interrupt [1] | 23 | GND | Ground |
| 11 | BSY | Busy / Wait [1] | 24 | GND | Ground |
| 12 | PE | Paper End / User defined [1] | 25 | GND | Ground |
| 13 | SLCT | Select / User defined [1] | -- | -- | -- |

NOTES:

[1] Standard and ECP mode function / EPP mode function
[2] EPP mode function: Data Strobe
ECP modes: Auto Feed or Host Acknowledge
[3] EPP mode: user defined
ECP modes:Fault or Peripheral Req.
[4] EPP mode: Reset
ECP modes: Initialize or Reverse Req.

## 5.6 KEYBOARD/POINTING DEVICE INTERFACE

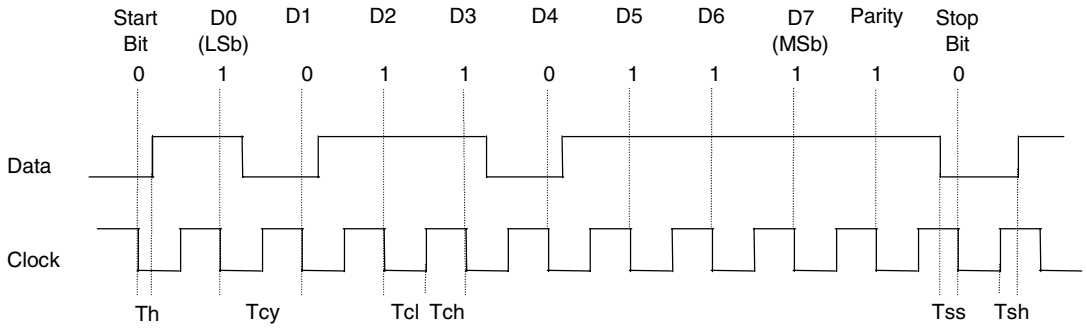
The legacy-light models include PS/2-type keyboard/pointing device interfaces for the connection of a standard enhanced keyboard and a mouse. (Legacy-free models use USB ports for keyboard/mouse connections.) The keyboard/pointing device interface function is provided by the LPC47B277 I/O controller component, which integrates 8042-compatible keyboard controller logic (hereafter referred to as simply the "8042") to communicate with the keyboard and pointing device using bi-directional serial data transfers. The 8042 handles scan code translation and password lock protection for the keyboard as well as communications with the pointing device. This section describes the interface itself. The keyboard is discussed in the Appendix C.

### 5.6.1 KEYBOARD INTERFACE OPERATION

The data/clock link between the 8042 and the keyboard is uni-directional for Keyboard Mode 1 and bi-directional for Keyboard Modes 2 and 3. (These modes are discussed in detail in Appendix C). This section describes Mode 2 (the default) mode of operation.

Communication between the keyboard and the 8042 consists of commands (originated by either the keyboard or the 8042) and scan codes from the keyboard. A command can request an action or indicate status. The keyboard interface uses IRQ1 to get the attention of the CPU.

The 8042 can send a command to the keyboard at any time. When the 8042 wants to send a command, the 8042 clamps the clock signal from the keyboard for a minimum of 60 us. If the keyboard is transmitting data at that time, the transmission is allowed to finish. When the 8042 is ready to transmit to the keyboard, the 8042 pulls the data line low, causing the keyboard to respond by pulling the clock line low as well, allowing the start bit to be clocked out of the 8042. The data is then transferred serially, LSb first, to the keyboard (Figure 5-6). An odd parity bit is sent following the eighth data bit. After the parity bit is received, the keyboard pulls the data line low and clocks this condition to the 8042. When the keyboard receives the stop bit, the clock line is pulled low to inhibit the keyboard and allow it to process the data.




| Parameter | Minimum | Maximum |
|---|---|---|
| Tcy (Cycle Time) | 0 us | 80 us |
| Tcl (Clock Low) | 25 us | 35 us |
| Tch (Clock High) | 25 us | 45 us |
| Th (Data Hold) | 0 us | 25 us |
| Tss (Stop Bit Setup) | 8 us | 20 us |
| Tsh (Stop Bit Hold) | 15 us | 25 us |

**Figure 5-6.** 8042-To-Keyboard Transmission of Code EDh, Timing Diagram

Control of the data and clock signals is shared by the 8042and the keyboard depending on the originator of the transferred data. Note that the clock signal is always generated by the keyboard. After the keyboard receives a command from the 8042, the keyboard returns an ACK code. If a parity error or timeout occurs, a Resend command is sent to the 8042.

Table 5-11 lists and describes commands that can be issued by the 8042 to the keyboard.

**Table 5-11.**
8042-To-Keyboard Commands

| Command | Value | Description |
|---|---|---|
| Set/Reset Status Indicators | EDh | Enables LED indicators. Value EDh is followed by an option byte that specifies the indicator as follows:<br>Bits <7..3> not used<br>Bit <2>, Caps Lock (0 = off, 1 = on)<br>Bit <1>, NUM Lock (0 = off, 1 = on)<br>Bit <0>, Scroll Lock (0 = off, 1 = on) |
| Echo | EEh | Keyboard returns EEh when previously enabled. |
| Invalid Command | EFh/F1h | These commands are not acknowledged. |
| Select Alternate Scan Codes | F0h | Instructs the keyboard to select another set of scan codes and sends an option byte after ACK is received:<br>01h = Mode 1<br>02h = Mode 2<br>03h = Mode 3 |
| Read ID | F2h | Instructs the keyboard to stop scanning and return two keyboard ID bytes. |
| Set Typematic Rate/Display | F3h | Instructs the keyboard to change typematic rate and delay to specified values:<br>Bit <7>, Reserved - 0<br>Bits <6,5>, Delay Time<br>00 = 250 ms<br>01 = 500 ms<br>10 = 750 ms<br>11 = 1000 ms<br>Bits <4..0>, Transmission Rate:<br>00000 = 30.0 ms<br>00001 = 26.6 ms<br>00010 = 24.0 ms<br>00011 = 21.8 ms<br>:<br>11111 = 2.0 ms |
| Enable | F4h | Instructs keyboard to clear output buffer and last typematic key and begin key scanning. |
| Default Disable | F5h | Resets keyboard to power-on default state and halts scanning pending next 8042 command. |
| Set Default | F6h | Resets keyboard to power-on default state and enable scanning. |
| Set Keys - Typematic | F7h | Clears keyboard buffer and sets default scan code set. [1] |
| Set Keys - Make/Brake | F8h | Clears keyboard buffer and sets default scan code set. [1] |
| Set Keys - Make | F9h | Clears keyboard buffer and sets default scan code set. [1] |
| Set Keys - Typematic/Make/Brake | FAh | Clears keyboard buffer and sets default scan code set. [1] |
| Set Type Key - Typematic | FBh | Clears keyboard buffer and prepares to receive key ID. [1] |
| Set Type Key - Make/Brake | FCh | Clears keyboard buffer and prepares to receive key ID. [1] |
| Set Type Key - Make | FDh | Clears keyboard buffer and prepares to receive key ID. [1] |
| Resend | FEh | 8042 detected error in keyboard transmission. |
| Reset | FFh | Resets program, runs keyboard BAT, defaults to Mode 2. |

Note:
[1] Used in Mode 3 only.

## 5.6.2 POINTING DEVICE INTERFACE OPERATION

The pointing device (typically a mouse) connects to a 6-pin DIN-type connector that is identical to the keyboard connector both physically and electrically. The operation of the interface (clock and data signal control) is the same as for the keyboard. The pointing device interface uses the IRQ12 interrupt.

## 5.6.3 KEYBOARD/POINTING DEVICE INTERFACE PROGRAMMING

Programming the keyboard interface consists of configuration, which occurs during POST, and control, which occurs during runtime.

### 5.6.3.1 8042 Configuration

The keyboard/pointing device interface must be enabled and configured for a particular speed before it can be used. Enabling and speed parameters of the 8042 logic are affected through the PnP configuration registers of the LPC47B347 I/O controller. Enabling and speed control are automatically set by the BIOS during POST but can also be accomplished with the Setup utility and other software.

The keyboard interface configuration registers are listed in the following table:

**Table 5-12.**
Keyboard Interface Configuration Registers

| Index Address | Function | R/W |
|---|---|---|
| 30h | Activate | R/W |
| 70h | Primary Interrupt Select | R/W |
| 72h | Secondary Interrupt Select | R/W |
| F0h | Reset and A20 Select | R/W |

### 5.6.3.2 8042 Control

The BIOS function INT 16 is typically used for controlling interaction with the keyboard. Sub-functions of INT 16 conduct the basic routines of handling keyboard data (i.e., translating the keyboard's scan codes into ASCII codes). The keyboard/pointing device interface is accessed by the CPU through I/O mapped ports 60h and 64h, which provide the following functions:

- Output buffer reads
- Input buffer writes
- Status reads
- Command writes

Ports 60h and 64h can be accessed using the IN instruction for a read and the OUT instruction for a write. Prior to reading data from port 60h, the "Output Buffer Full" status bit (64h, bit <0>) should be checked to ensure data is available. Likewise, before writing a command or data, the "Input Buffer Empty" status bit (64h, bit <1>) should also be checked to ensure space is available.

#### I/O Port 60h

I/O port 60h is used for accessing the input and output buffers. This register is used to send and receive data from the keyboard and the pointing device. This register is also used to send the second byte of multi-byte commands to the 8042 and to receive responses from the 8042 for commands that require a response.

A read of 60h by the CPU yields the byte held in the output buffer. The output buffer holds data that has been received from the keyboard and is to be transferred to the system.

A CPU write to 60h places a data byte in the input byte buffer and sets the CMD/ DATA bit of the Status register to DATA. The input buffer is used for transferring data from the system to the keyboard. All data written to this port by the CPU will be transferred to the keyboard **except** bytes that follow a multibyte command that was written to 64h

#### I/O Port 64h

I/O port 64h is used for reading the status register and for writing commands. A read of 64h by the CPU will yield the status byte defined as follows:

| Bit | Function |
|---|---|
| 7..4 | General Purpose Flags. |
| 3 | CMD/DATA Flag (reflects the state of A2 during a CPU write).<br>0 = Data<br>1 = Command |
| 2 | General Purpose Flag. |
| 1 | Input Buffer Full. Set (to 1) upon a CPU write. Cleared by IN A, DBB instruction. |
| 0 | Output Buffer Full (if set). Cleared by a CPU read of the buffer. |

A CPU write to I/O port 64h places a command value into the input buffer and sets the CMD/DATA bit of the status register (bit <3>) to CMD.

Table 5-13 lists the commands that can be sent to the 8042 by the CPU. The 8042 uses IRQ1 for gaining the attention of the CPU.

**Table 5-13.**
CPU Commands To The 8042

| Value | Command Description |
|---|---|
| 20h | Put current command byte in port 60h. |
| 60h | Load new command byte. This is a two-byte operation described as follows:<br>1. Write 60h to port 64h.<br>2. Write the command byte to port 60h as follows:<br>Bit <7> Reserved<br><6> Keyboard Code Conversion<br>0 = Do not convert codes<br>1 = Convert codes to 9-bit 8088/8086-compatible format<br>Bit <5> Pointing Device Enable<br>0 = Enable pointing device<br>1 = Disable pointing device<br>Bit <4> Keyboard Enable<br>0 = Enable keyboard<br>1 = Disable keyboard<br>Bit <3> Reserved<br>Bit <2> System Flag<br>0 = Cold boot<br>1 = CPU reset (exit from protected mode)<br>Bit <1> Pointing Device Interrupt Enable<br>0 = Disable interrupt<br>1 = Enable interrupt<br>Bit <0> Keyboard Interrupt Enable<br>0 = Disable interrupt<br>1 = Enable interrupt |
| A4h | Test password installed. Tests whether or not a password is installed in the 8042:<br>If FAh is returned, password is installed.<br>If F1h is returned, no password is installed. |
| A5h | Load password. This multi-byte operation places a password in the 8042 using the following manner:<br>1. Write A5h to port 64h.<br>2. Write each character of the password in 9-bit scan code (translated) format to port 60h.<br>3. Write 00h to port 60h. |
| A6h | Enable security. This command places the 8042 in password lock mode following the A5h command. The correct password must then be entered before further communication with the 8042 is allowed. |
| A7h | Disable pointing device. This command sets bit <5> of the 8042 command byte, pulling the clock line of the pointing device interface low. |
| A8h | Enable pointing device. This command clears bit <5> of the 8042 command byte, activating the clock line of the pointing device interface. |
| A9h | Test the clock and data lines of the pointing device interface and place test results in the output buffer.<br>00h = No error detected<br>01h = Clock line stuck low<br>02h = Clock line stuck high<br>03h = Data line stuck low<br>04h = Data line stuck high |
| AAh | Initialization. This command causes the 8042 to inhibit the keyboard and pointing device and places 55h into the output buffer. |
| ABh | Test the clock and data lines of the keyboard interface and place test results in the output buffer.<br>00h = No error detected<br>01h = Clock line stuck low<br>02h = Clock line stuck high<br>03h = Data line stuck low<br>04h = Data line stuck high |
| ADh | Disable keyboard command (sets bit <4> of the 8042 command byte). |
| AEh | Enable keyboard command (clears bit <4> of the 8042 command byte). |

*Continued*

**Table 5-13.** CPU Commands To The 8042 *(Continued)*

| Value | Command Description |
|---|---|
| C0h | Read input port of the 8042. This command directs the 8042 to transfer the contents of the input port to the output buffer so that they can be read at port 60h. The contents are as follows:<br>Bit <7> Password Enable:<br>0 = Disabled<br>1 = Enabled<br>Bit <6> External Boot Enable:<br>0 = Enabled<br>1 = Disabled<br>Bit <5> Setup Enable:<br>0 = Enabled<br>1 = Disabled<br>Bit <4> VGA Enable:<br>0 = Enabled<br>1 = Disabled<br>Bit <3> Diskette Writes:<br>0 = Disabled<br>1 = Enabled<br>Bit <2> Reserved<br>Bit <1> Pointing Device Data Input Line<br>Bit <0> Keyboard Data Input Line |
| C2h | Poll Input Port High. This command directs the 8042 to place bits <7..4> of the input port into the upper half of the status byte on a continous basis until another command is received. |
| C3h | Poll Input Port Low. This command directs the 8042 to place bits <3..0> of the input port into the lower half of the status byte on a continous basis until another command is received. |
| D0h | Read output port. This command directs the 8042 to transfer the contents of the output port to the output buffer so that they can be read at port 60h. The contents are as follows:<br>Bit <7> Keyboard data stream<br>Bit <6> Keyboard clock<br>Bit <5> IRQ12 (pointing device interrupt)<br>Bit <4> IRQ1 (keyboard interrupt)<br>Bit <3> Pointing device clock<br>Bit <2> Pointing device data<br>Bit <1> A20 Control:<br>0 = Hold A20 low<br>1 = Enable A20<br>Bit <0> Reset Line Status;<br>0 = Inactive<br>1 = Active |
| D1h | Write output port. This command directs the 8042 to place the next byte written to port 60h into the output port (only bit <1> can be changed). |
| D2h | Echo keyboard data. Directs the 8042 to send back to the CPU the next byte written to port 60h as if it originated from the keyboard. No 11-to-9 bit translation takes place but an interrupt (IRQ1) is generated if enabled. |
| D3h | Echo pointing device data. Directs the 8042 to send back to the CPU the next byte written to port 60h as if it originated from the pointing device. An interrupt (IRQ12) is generated if enabled. |
| D4h | Write to pointing device. Directs the 8042 to send the next byte written to 60h to the pointing device. |
| E0h | Read test inputs. Directs the 8042 to transfer the test bits 1 and 0 into bits <1,0> of the output buffer. |
| F0h-FFh | Pulse output port. Controls the pulsing of bits <3..0> of the output port (0 = pulse, 1 = don't pulse). Note that pulsing bit <0> will reset the system. |

## 5.6.4 KEYBOARD/POINTING DEVICE INTERFACE CONNECTOR

The legacy-light model provides separate PS/2 connectors for the keyboard and pointing device. Both connectors are identical both physically and electrically. Figure 5-7 and Table 5-14 show the connector and pinout of the keyboard/pointing device interface connectors.

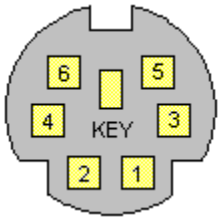



**Figure 5-7.** Keyboard or Pointing Device Interface Connector (as viewed from rear of chassis)

**Table 5-17.**
Keyboard/Pointing Device Connector Pinout

| Pin | Signal | Description | Pin | Signal | Description |
|---|---|---|---|---|---|
| 1 | DATA | Data | 4 | + 5 VDC | Power |
| 2 | NC | Not Connected | 5 | CLK | Clock |
| 3 | GND | Ground | 6 | NC | Not Connected |

## 5.7 UNIVERSAL SERIAL BUS INTERFACE

The Universal Serial Bus (USB) interface provides asynchronous/isochronous data transfers of up to 12 Mb/s with compatible peripherals such as keyboards, printers, or modems. This high-speed interface supports hot-plugging of compatible devices, making possible system configuration changes without powering down or even rebooting systems.

> **NOTE:** It is recommended to run the Windows 98 (or later) operating system when using USB peripherals, **especially a USB keyboard and USB mouse**. Problems may be encountered when using USB devices with a system running Windows 95, although some peripherals (such as a modem and/or a camera) may operate satisfactorily.

As shown in Figure 5-8, the USB interface is provided by the 82801 ICH component and a USB hub component. All models provide two front-panel accessible series-A USB ports. The legacy-free system provides three additional series-A USB ports on the rear panel.

> **NOTE:** For more information on the USB interface refer to the following web site:
> http://www.usb.org

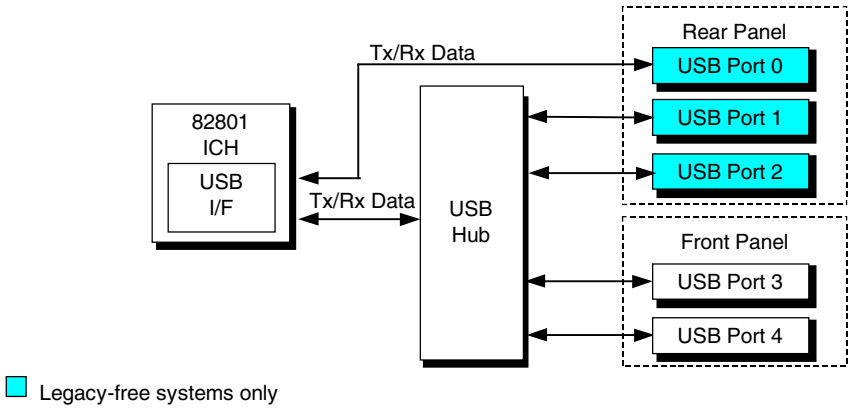



**Figure 5-8.** USB I/F, Block Diagram

### 5.7.1 USB DATA FORMATS

The USB I/F uses non-return-to-zero inverted (NRZI) encoding for data transmissions, in which a 1 is represented by no change (between bit times) in signal level and a 0 is represented by a change in signal level. Bit stuffing is employed prior to NRZ1 encoding so that in the event a string of 1's is transmitted (normally resulting in a steady signal level) a 0 is inserted after every six consecutive 1's to ensure adequate signal transitions in the data stream.

The USB transmissions consist of packets using one of four types of formats (Figure 5-9) that include two or more of seven field types.

- Sync Field – 8-bit field that starts every packet and is used by the receiver to align the incoming signal with the local clock.
- Packet Identifier (PID) Field – 8-bit field sent with every packet to identify the attributes (in. out, start-of-frame (SOF), setup, data, acknowledge, stall, preamble) and the degree of error correction to be applied.
- Address and Endpint Fields – 7- and 4-bit fields (respectively) that provide source/destination information required in token packets.
- Frame Field – 11-bit field sent in Start-of-Frame (SOF) packets that are incremented by the host and sent only at the start of each frame.
- Data Field – 0-1023-byte field of data.
- Cyclic Redundancy Check (CRC) Field – 5- or 16-bit field used to check transmission integrity.

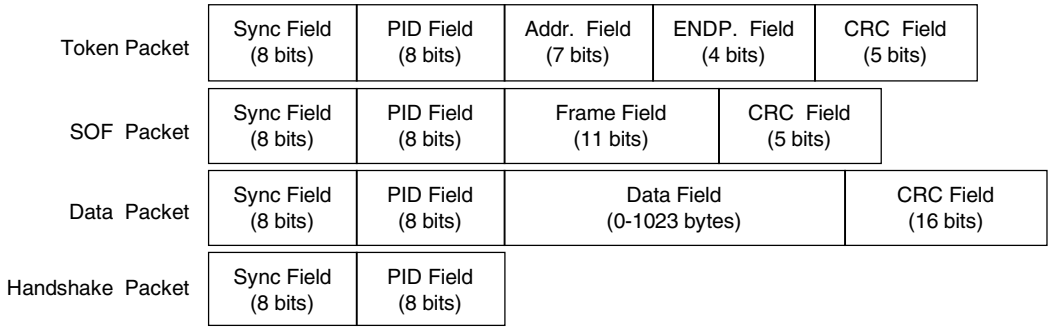



**Figure 5-9.** USB Packet Formats

Data is transferred LSb first. A cyclic redundancy check (CRC) is applied to all packets (except a handshake packet). A packet causing a CRC error is generally completely ignored by the receiver.

## 5.7.2 USB PROGRAMMING

Programming the USB interface consists of configuration, which typically occurs during POST, and control, which occurs at runtime.

### 5.7.2.1 USB Configuration

The USB interface functions as a PCI device (31) within the 82801 component (function 2) and is configured using PCI Configuration Registers as listed in Table 5-15.

**Table 5-15.**
USB Interface Configuration Registers

| PCI Config. Addr. | Register | Reset Value | PCI Config. Addr. | Register | Reset Value |
|---|---|---|---|---|---|
| 00, 01h | Vender ID | 8086h | 0Dh | Latency Timer | 00h |
| 02, 03h | Device ID | 2412h | 0Eh | Header Type | 00h |
| 04, 05h | PCI Command | 0000h | 20-23h | I/O Space Base Address | 1h |
| 06, 07h | PCI Status | 0280h | 3Ch | Interrupt Line | 00h |
| 08h | Revision ID | 00h | 3Dh | Interrupt Pin | 04h |
| 09h | Programming I/F | 00h | 60h | Miscellaneous Control 1 | 10h |
| 0Ah | Sub Class Code | 03h | C0, C1h | Miscellaneous Control 2 | 2000h |
| 0Bh | Base Class Code | 0Ch | C4h | USB Resume Enable | 00h |

### 5.7.2.2 USB Control

The USB is controlled through I/O registers as listed in table 5-16.

**Table 5-16.**
USB Control Registers

| I/O Addr. | Register | Default Value |
|---|---|---|
| 00, 01h | Command | 0000h |
| 02, 03h | Status | 0000h |
| 04, 05h | Interupt Enable | 0000h |
| 06, 07 | Frame Number | 0000h |
| 08, 0B | Frame List Base Address | 0000h |
| 0Ch | Start of Frame Modify | 40h |
| 10, 11h | Port 1 Status/Control | 0080h |
| 12, 13h | Port 2 Status/Control | 0080h |
| 18h | Test Data | 00h |

## 5.7.3 USB CONNECTOR

The USB interface provides two series-A connectors on the front panel and, on legacy-free models, three series-A USB connectors on the rear panel.

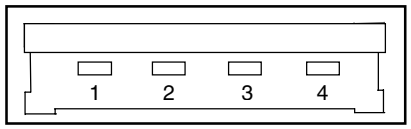



**Figure 5-10.** Universal Serial Bus Connector

**Table 5-17.**
USB Connector Pinout

| Pin | Signal | Description | Pin | Signal | Description |
|---|---|---|---|---|---|
| 1 | Vcc | +5 VDC | 3 | USB+ | Data (plus) |
| 2 | USB- | Data (minus) | 4 | GND | Ground |

## 5.7.4 USB CABLE DATA

The recommended cable length between the host and the USB device should be no longer than sixteen feet for full-channel (12 MB/s) operation, depending on cable specification (see following table).

**Table 5-18.**
USB Cable Length Data

| Conductor Size | Resistance | Maximum Length |
|---|---|---|
| 20 AWG | 0.036 Ω | 16.4 ft (5.00 m) |
| 22 AWG | 0.057 Ω | 9.94 ft (3.03 m) |
| 24 AWG | 0.091 Ω | 6.82 ft (2.08 m) |
| 26 AWG | 0.145 Ω | 4.30 ft (1.31 m) |
| 28 AWG | 0.232 Ω | 2.66 ft (0.81 m) |

NOTE:
For sub-channel (1.5 MB/s) operation and/or when using sub-standard cable shorter lengths may be allowable and/or necessary.

The shield, chassis ground, and power ground should be tied together at the host end but left unconnected at the device end to avoid ground loops.

Color code:

| Signal | Insulation color |
|---|---|
| Data + | Green |
| Data - | White |
| Vcc | Red |
| Ground | Black |

## 5.8 AUDIO SUBSYSTEM

A PCI audio subsystem is integrated onto the system board of the Compaq iPAQ. Implementing AC'97 design guidelines, the audio subsystem is designed to provide optimum sound. Key features of the audio subsystem include:

- AC'97 ver. 2.1 compliance
- Multiple audio channel streaming
- Soft CD, DVD/AC-3 processing
- Wavetable synthesis utilizing system memory
- Acoustic echo cancellation
- 16-bit stereo PCM input and output w/ up to 48 KHz sampling

### 5.8.1 FUNCTIONAL ANALYSIS

A block diagram of the audio subsystem is shown in Figure 5-11. The architecture uses the AC'97 Audio Controller of the 82801 ICH component to access and control an Analog Devices AD1881 Audio Codec, which provides the analog-to-digital (ADC) and digital-to-analog (DAC) conversions as well as the mixing functions.

All control functions such as volume, audio source selection, and sampling rate are controlled through software over the PCI bus through the AC97 Audio Controller of the 82801 ICH. Control data and digital audio streams (record and playback) are transferred between the Audio Controller and the Audio Codec over the AC97 Link Bus. Playback audio from the Audio Codec is routed to a 5-watt low-distortion amplifier (TDA7056A) that drives a long-excursion large-magnet speaker for optimum sound.

The analog interfaces allowing connection to external audio devices are discussed in the following paragraphs.

**Mic In** - This front panel-accessible input uses a three-conductor (stereo) mini-jack that is specifically designed for connection of a condenser microphone with an impedance of 10-K ohms. This is the default recording input after a system reset.

**Line In** - This input uses a three-conductor (stereo) mini-jack that is specifically designed for connection of a high-impedance (10k-ohm) audio source such as a tape deck.

**Headphones Out** - This front panel-accessible input uses a three-conductor (stereo) mini-jack that is specifically designed for connecting a set of 16-ohm (nom.) stereo headphones. Plugging into the Headphones jack mutes the signal to the internal speaker and the Line Out jack.

**Line Out** - This output uses a three-conductor (stereo) mini-jack for connecting left and right channel line-level signals (20-K ohm impedance). A typical connection would be to a tape recorder's Line In (Record In) jacks, an amplifier's Line In jacks, or to "powered" speakers that contain amplifiers. Plugging into the Line Out mutes the internal speaker.

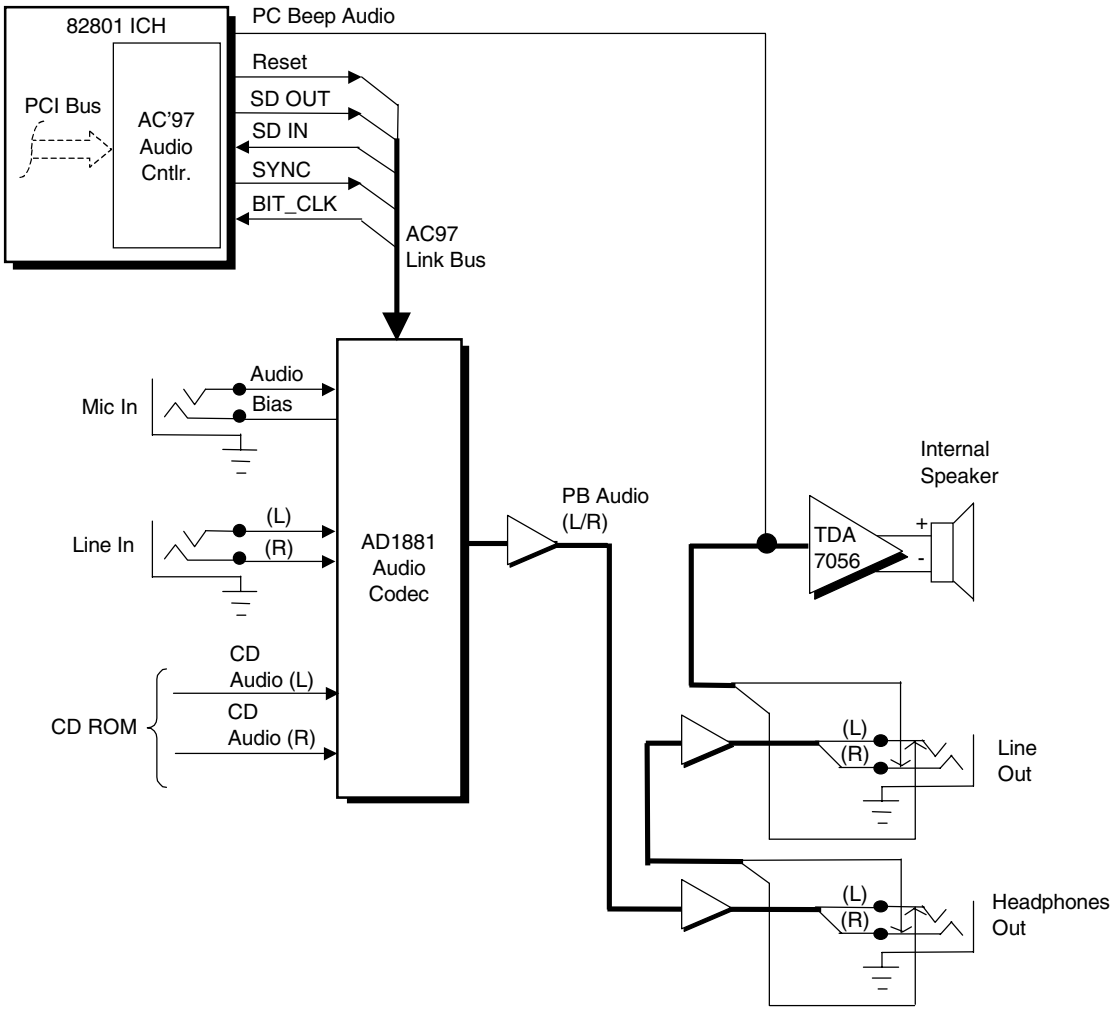



**Figure 5-11.** Audio Subsystem Functional Block Diagram

Legacy beep audio originates from the 82801 ICH and is applied to the output amplifier, bypassing the audio codec so that basic support of beep codes produced during POST is maintained.

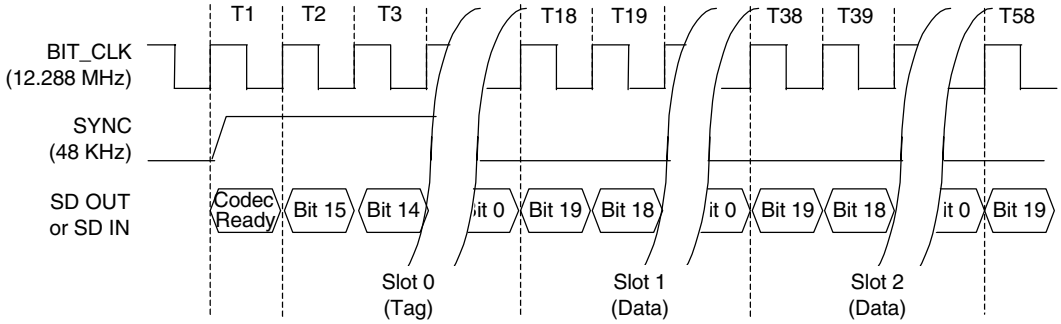
## 5.8.2 AC97 AUDIO CONTROLLER

The AC97 Audio Controller is a PCI device (device 31/function 5) that is integrated into the 82801 ICH component and supports the following functions:

- Read/write access to audio codec registers
- 16-bit stereo PCM output @ up to 48 KHz sampling
- 16-bit stereo PCM input @ up to 48 KHz sampling
- Acoustic echo correction for microphone
- AC'97 Link Bus
- ACPI power management

## 5.8.3 AC97 LINK BUS

The audio controller and the audio codec communicate over a five-signal AC97 Link Bus (Figure 5-12). The AC97 Link Bus includes two serial data lines (SD OUT/SD IN) that transfer control and PCM audio data serially to and from the audio codec using a time-division multiplexed (TDM) protocol. The data lines are qualified by a 12.288 MHz BIT_CLK signal driven by the audio codec. Data is transferred in frames synchronized by the 48-KHz SYNC signal, which is derived from the clock signal and driven by the audio controller. The SYNC signal is high during the frame's tag phase then falls during T17and remains low during the data phase. A frame consists of one 16-bit tag slot followed by twelve 20-bit data slots. When asserted (typically during a power cycle), the RESET- signal (not shown) will reset all audio registers to their default values.




| Slot | Description |
|---|---|
| 0 | Bit 15: Frame valid bit<br>Bits 14-3: Slots 1-12 valid bits<br>Bits 2-0: Codec ID |
| 1 | Command address: Bit 19, R/W; Bits 18..12, reg. Index; Bits 11..0, reserved. |
| 2 | Command data |
| 3 | Bits 19-4: PCM audio data, left channel (SD OUT, playback; SD IN, record)<br>Bits 3-0 all zeros |
| 4 | Bits 19-4: PCM audio data, right channel (SD OUT, playback; SD IN, record)<br>Bits 3-0 all zeros |
| 5 | Modem codec data (not used in this system) |
| 6-11 | Reserved |
| 12 | I/O control |

**Figure 5-12.** AC'97 Link Bus Protocol

## 5.8.4 AUDIO CODEC

The audio codec provides pulse code modulation (PCM) coding and decoding of audio information as well as the selection and/or mixing of analog channels. As shown in Figure 5-13, analog audio from a microphone, tape, or CD can be selected and, if to be recorded (saved) onto a disk drive, routed through an analog-to-digital converter (ADC). The resulting left and right PCM record data are muxed into a time-division-multiplexed (TDM) data stream (SD IN signal) that is routed to the audio controller. Playback (PB) audio takes the reverse path from the audio controller to the audio codec as SD OUT data and is decoded and processed by the digital-to-analog converter (DAC). The codec supports simultaneous record and playback of stereo (left and right) audio. The Sample Rate Generator may be set for sampling frequencies up to 48 KHz.

Analog audio may then be routed through 3D stereo enhancement processor or bypassed to the output selector (SEL). The integrated analog mixer provides the computer control-console functionality handling multiple audio inputs.

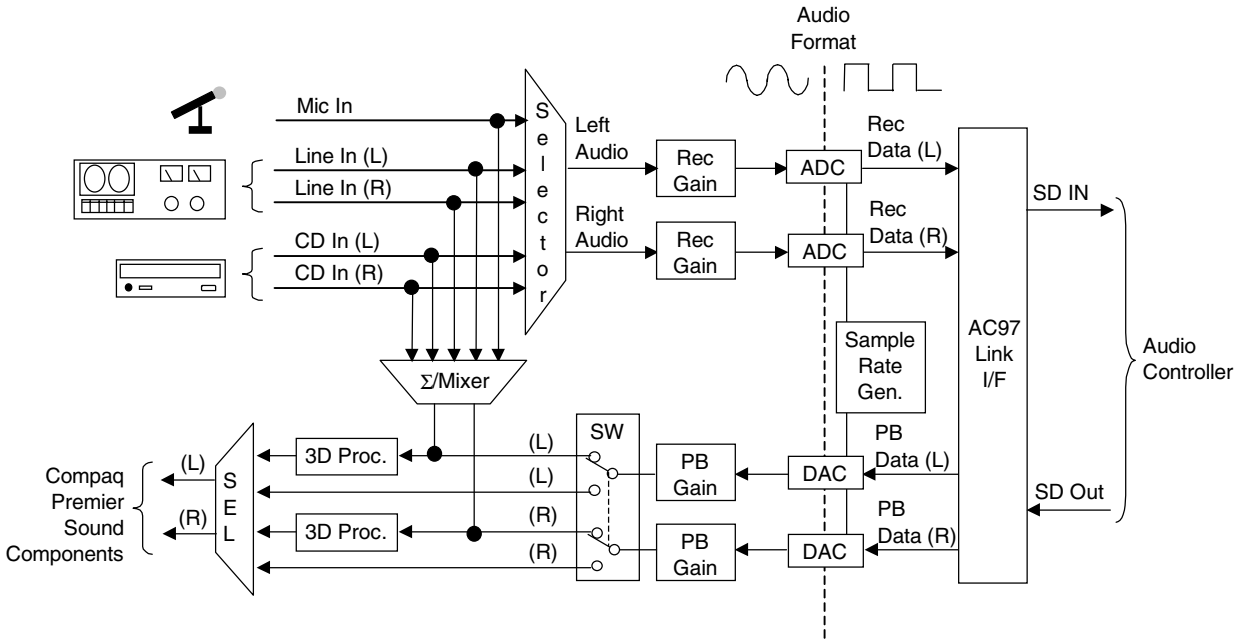



**Figure 5-13.** AD1881 Audio Codec Functional Block Diagram

All inputs and outputs are two-channel stereo except for the microphone input, which is inputted as a single-channel but mixed internally onto both left and right channels. The microphone input is the default active input. All block functions are controlled through index-addressed registers of the codec.

## 5.8.5 AUDIO PROGRAMMING

Audio subsystem programming consists configuration, typically accomplished during POST, and control, which occurs during runtime. The register maps are described in the following subsections.

### 5.8.5.1 Audio Configuration

The audio subsystem is configured according to PCI protocol through the AC'97 audio controller function of the 82801 ICH. Table 5-19 lists the PCI configuration registers of the audio subsystem.

**Table 5-19.**
AC'97 Audio Controller
PCI Configuration Registers (82801 Device 31/Function 5)

| PCI Conf. Addr. | Register | Value on Reset | PCI Conf. Addr. | Register | Value on Reset |
|---|---|---|---|---|---|
| 00-01h | Vender ID | 8086h | 14-17h | Native Audio Bus Mstr. Addr. | 1h |
| 02-03h | Device ID | 2415h | 18-1Bh | Reserved | 1h |
| 04-05h | PCI Command | 0000h | 1C-2Bh | Reserved | 1h |
| 06-07h | PCI Status | 0280h | 2C-2Dh | Subsystem Vender ID | 0000h |
| 08h | Revision ID | xxh | 2E-2Fh | Subsystem ID | 0000h |
| 09h | Programming | 01h | 30-3Bh | Reserved | 0's |
| 0Ah | Sub-Class | 01h | 3Ch | Interrupt Line | 00h |
| 0Bh | Base Class Code | 04h | 3Dh | Interrupt Pin | 03h |
| 0Eh | Header Type | 00h | 3E-FFh | Reserved | 0's |
| 10-13h | Native Audio Mixer Base Addr. | 1h | -- | -- | -- |

### 5.8.5.2 Audio Control

The audio subsystem is controlled through a set of indexed registers that physically reside in the audio codec . The register addresses are decoded by the audio controller and forwarded to the audio codec over the AC97 Link Bus previously described. The audio codec's control registers (Table 5-20) are mapped into 64 kilobytes of variable I/O space.

**Table 5-20.**
AC'97 Audio Codec Control Registers

| Offset Addr. / Register | Value On Reset | Offset Addr. / Register | Value On Reset | Offset Addr. / Register | Value On Reset |
|---|---|---|---|---|---|
| 00h Reset | 0100h | 14h Video Vol. | 8808h | 28h Ext. Audio ID. | 0001h |
| 02h Master Vol. | 8000h | 16h Aux Vol. | 8808h | 2Ah Ext. Audio Ctrl/Sts | 0000h |
| 04h Reserved | X | 18h PCM Out Vol. | 8808h | 2Ch PCM DAC SRate | BB80h |
| 06h Mono Mstr. Vol. | 8000h | 1Ah Record Sel. | 0000h | 32h PCM ADC SRate | BB80h |
| 08h Reserved | X | 1Ch Record Gain | 8000h | 34h Reserved | X |
| 0Ah PC Beep Vol. | 8000h | 1Eh Reserved | X | 72h Reserved | X |
| 0Ch Phone In Vol. | 8008h | 20h Gen. Purpose | 0000h | 74h Serial Config. | 7x0xh |
| 0Eh Mic Vol. | 8008h | 22h 3D Control | 0000h | 76h Misc. Control Bits | 0404h |
| 10h Line In Vol. | 8808h | 24h Reserved | X | 7Ch Vender ID1 | 4144h |
| 12h CD Vol. | 8808h | 26h Pwr Mgnt. | 000xh | 7Eh Vender ID2 | 5340h |

## 5.8.6 AUDIO SPECIFICATIONS

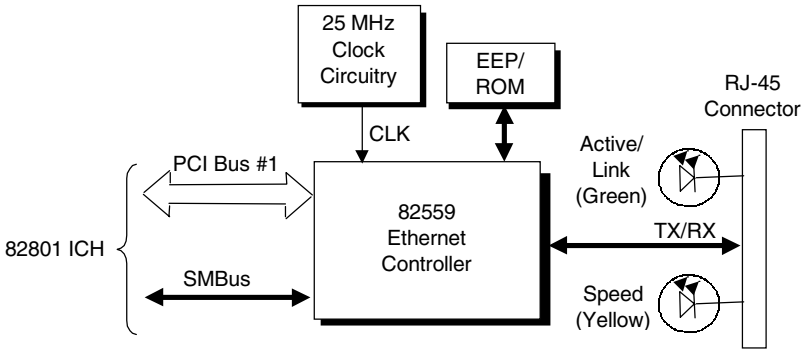
The specifications of the audio subsystem are listed in Table 5-21.

**Table 5-21.**
Audio Subsystem Specifications

| Paramemter | Measurement |
|---|---|
| Sampling Rate | 5.51 KHz to 44 KHz |
| Resolution | 16 bit |
| Nominal Input Voltage: | |
| Mic In (w/+20 db gain | .283 Vp-p |
| Line In | 2.83 Vp-p |
| Impedance: | |
| Mic In | 1 K ohms (nom) |
| Line In | 10 K ohms (min) |
| Line Out | 800 ohms |
| Signal-to-Noise Ratio (input to Line Out) | 90 db (nom) |
| Max. Power Output (into 8 ohms) | 5.2 watts |
| Total Harmonic Distortion (THD) (to int. spkr): | |
| @ 0.5 watts | 1 % |
| @ max. power output | 10 % |
| Headphone Output Power (into 32 ohms) | 60 mW |
| Input Gain Attenuation Range | 46.5 db |
| Master Volume Range | -94.5 db |
| Frequency Response: | |
| Codec | 20-20 KHz |
| Speaker | 450 - 4000 Hz |

## 5.9 NETWORK INTERFACE CONTROLLER

The Compaq iPAQ includes a network interface controller (NIC) resident on the system board. The NIC (Figure 5-14) includes the 82559 controller, two LED indicators, and support firmware. The support firmware is contained in the system (BIOS) ROM. The NIC can operate in half- or full-duplex modes, and provides auto-negotiation of both mode and speed. Half-duplex operation features an Intel-proprietary collision reduction mechanism while full-duplex operation follows the IEEE 802.3x flow control specification. Transmit and receive FIFOs of 3 kilobytes each reduce the chance of overrun while waiting for bus access.




| LED | Function |
|---|---|
| Green | Activity/Link: Indicates network activity and link pulse reception. |
| Yellow | Speed: Indicates link detection in 100 MB/s mode (always on if 100Base-Tx is forced). |

**Figure 5-14.** 10/100 TX Network Interface Controller Block Diagram

The Intel 82559 Fast Ethernet Controller includes the following features:

- Intel 82559 Fast Ethernet controller with 32-bit architecture and 3-KB TX/RX buffers.
- Dual-mode support with auto-switching between 10BASE-T and 100BASE-TX.
- Power down and Wake up support in both APM and ACPI environments (PME- and WOL).
- Alert-on-LAN (AOL v1.0) support.
- Dual control (PCI and SM bus interfaces).
- Link and Activity LED indicator drivers

The 82559 controller features high and low priority queues and provides priority-packet processing for networks that can support that feature. The controller's micro-machine processes transmit and receive frames independently and concurrently. Receive runt (under-sized) frames are not passed on as faulty data but discarded by the controller, which also directly handles such errors as collision detection or data under-run. An EEPROM, accessed by the 82559 controller over a serial interface, is used to store identification, configuration and connection parameters.

The NIC uses 3.3 VDC auxiliary power, which allows the 82559 controller to support Wake-On-LAN (WOL) and Alert-On-LAN (AOL) functions while the main system is powered down.

△ **NOTE:** For the WOL and AOL features to function as described in the following paragraphs, the system unit must be plugged into a live AC outlet. Controlling unit power through a switchable power strip will, with the strip turned off, disable WOL and AOL functionality.

### 5.9.1 WAKE ON LAN

The 82559 NIC supports the Wired-for-Management (WfM) standard of Wake-On-LAN (WOL) that allows the system to be booted up from a powered down condition upon the detection of special packets received over a network. The NIC component receives 3.3 VDC auxiliary power while the system unit is powered down in order to process special packets. The detection of a Magic Packet by the 82559 NIC results in the PME- signal on the PCI bus to be asserted, initiating system wake-up from an ACPI S1 or S3 state.

### 5.9.2 ALERT ON LAN

Alert-On-LAN (AOL) support allows the NIC to communicate the occurrence of certain events over a network even while the system unit is powered off. In a system-off (powered down) condition the 82801 ICH and the 82559 NIC components receive auxiliary +3.3 VDC power (derived from the +5 VDC auxiliary power from the power supply assembly). Certain events (listed in Table 5-22) detected by the 82801 ICH will result in the ICH generating an alert message over the SMBus to the 82559 NIC. Upon receiving the alert message from the ICH the NIC transmits the appropriate pre-constructed message over the network to a system management console.

Reportable AOL events are listed in the following table:

**Table 5-22.**
AOL Events

| Event | Description |
|---|---|
| BIOS Failure | System fails to boot successfully. |
| OS Problem | System fails to load operating system after POST. |
| Missing/Faulty Processor | Processor fails to fetch first instruction. |
| Thermal Condition | Thermal ASIC reports high temperature. |
| Heartbeat | Indication of system's network presence (sent approximately every 30 seconds in normal operation). |

The AOL implementation requirements are as follows:

1. Intel PRO/100+ Management Adapter driver 3.1x or later (available from Compaq).
2. Client-side utility agent software (available from Compaq).
3. Management console running one of the following:
   a. HP OpenView Network Node Manager 6.x
   b. Intel LANDesk Client Manager
   c. Compaq Insight Manager

### 5.9.3 POWER MANAGEMENT SUPPORT

The 82559 controller features Wired-for-Management (WfM) support providing system wake up from network events (WOL) as well as generating system status messages (AOL) and supports both APM and ACPI power management environments. The controller receives 3.3 VDC (auxiliary) power as long as the system is plugged into a live AC receptacle, allowing support of wake-up events occuring over a network while the system is powered down or in a low-power state.

#### 5.9.3.1 APM Environment

The Advanced Power Management (APM) functionality of system wake up is implemented through the system's APM-compliant BIOS and the controller's Magic Packet-compliant hardware. This environment bypasses operating system (OS) intervention allowing a plugged in unit to be turned on remotely over the network (i.e., "remote wake up"). In APM mode the controller, will respond upon receiving a Magic Packet, which is a packet where the node's address is repeated 16 times. Upon Magic packet detection, the controller intitiates the boot sequence.

#### 5.9.3.2 ACPI Environment

The Advanced Configuration and Power Interface (ACPI) functionality of system wake up is implemented through an ACPI-compliant OS **and is the default power management mode**. The following wakeup events may be individually enabled/disabled through the supplied software driver:

- Magic Packet – Packet with node address repeated 16 times in data portion

  **NOTE**: The following functions are supported in NDIS5 drivers but implemented through remote management software applications (such as LanDesk).

- Individual address match – Packet with matching user-defined byte mask
- Multicast address match – Packet with matching user-defined sample frame
- ARP (address resolution protocol) packet
- Flexible packet filtering – Packets that match defined CRC signature

## 5.9.4 NIC PROGRAMMING

Programming the 82559 NIC controller consists of configuration, which occurs during POST, and control, which occurs at runtime.

### 5.9.4.1 Configuration

The 82559 controller is a PCI device and configured though PCI configuration space registers using PCI protocol described in chapter 4. The PCI configuration registers are listed in the following table:

**Table 5-23.**
NIC Controller PCI Configuration Registers (82559 Device 2/Function 0)

| PCI Conf. Addr. | Register | Value on Reset | PCI Conf. Addr. | Register | Value on Reset |
|---|---|---|---|---|---|
| 00-01h | Vender ID | 8086h | 10-13h | Cntrl. Reg. Base Addr. (Mem) | 0000h |
| 02-03h | Device ID | 1229h | 14-17h | Cntrl. Reg. Base Addr. (I/O) | 00h |
| 04-05h | PCI Command | 0000h | 18-1Bh | Flash Mem. Base Addr. | 00h |
| 06-07h | PCI Status | 0280h | 2C-2Dh | Subsystem Vender ID | |
| 08h | Revision ID | xxh | 2E-2Fh | Subsystem ID | |
| 09-0Bh | Class Code | 01h | 30-33h | Expansion ROM Base Addr. | |
| 0Ch | Cache Line Size | 01h | 34h | Cap-Ptr | |
| 0Dh | Latency Timer | 04h | 3C-3D | Interrupt Line/Pin | |
| 0Eh | Header Type | 00h | 3E-3Fh | Min Gnt/Max Lat | |
| 0Fh | BIST | 00h | DC-E3h | Power Mgmt. Functions | |

NOTE:
Assume unmarked gaps are reserved and/or not used.

### 5.9.4.2 Control

The 82559 controller is controlled though registers that may be mapped in system memory space or variable I/O space. The registers are listed in the following table:

**Table 5-24.**
NIC Control Registers

| Offset Addr. / Register | No. of Bytes | Offset Addr. / Register | No. of Bytes |
|---|---|---|---|
| 00h SCB Status | 2 | 19h Flow Control Register | 2 |
| 02h SCB Command | 2 | 1Bh PMDR | 1 |
| 04h SCB General Pointer | 4 | 1Ch General Control | 1 |
| 08h PORT | 4 | 1Dh General Status | 1 |
| 0Ch Flash Control Reg. | 2 | 1E-2Fh Reserved | 10 |
| 0Eh EEPROM Control Reg. | 2 | 30h Function Event Register | 4 |
| 10h Mgmt. Data I/F Cntrl. Reg. | 4 | 34h Function Event Mask Register | 4 |
| 14h Rx Direct Mem. Access Byte Cnt. | 4 | 38h Function Present State Register | 4 |
| 18h Early Receive Interrupt | 1 | 20h Force Event Register | 4 |

Not implemented in these systems (CardBus registers).

### 5.9.4.3 RJ-45 Connector

Figure 5-15 shows the RJ-45 connector used for the NIC interface. This connector includes the two status LEDs as part of the connector assembly.

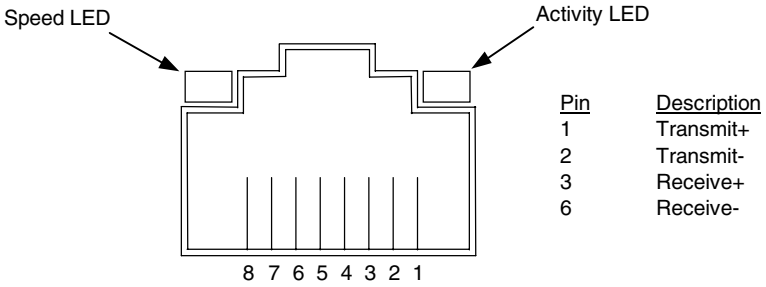



**Figure 5-15.** Ethernet TPE Connector (RJ-45, viewed from card edge)

### 5.9.4.4 82559 NIC Specifications

**Table 5-25.**
82559 NIC Specifications

| Parameter | |
|---|---|
| Modes Supported | 10BASE-T half duplex @ 10 MB/s<br>10Base-T full duplex @ 20 MB/s<br>100BASE-TX half duplex @ 100 MB/s<br>100Base-TX full duplex @ 200 MB/s |
| Standards Compliance | IEEE VLAN (802.1A)<br>IEEE 802.2<br>IEEE 802.3 & 802.3u<br>IEEE Intel priority packet (801.1p) |
| OS Driver Support | MS Windows 95,98, and 2000 beta<br>MS Windows NT 3.51 & 4.0<br>Novell Netware 3.11, 3.12, & 4.1x; 5 Server<br>Sunsoft Solaris<br>SCO UnixWare<br>Open Desktop<br>OpenServer |
| Boot ROM Support | Intel PRO/100 Boot Agent (PXE 2.0, RPL) |
| F12 BIOS Support | Yes |
| Bus Inteface | PCI 2.2 |
| Power Management Support | APM, ACPI, PCI Power Management Spec. |

# Chapter 6
# GRAPHICS SUBSYSTEM

## 6.1 INTRODUCTION

This chapter describes the graphics subsystem of the Compaq iPAQ Internet Device. The 82810e/DC-100 GMCH component integrates the equivalent of the Intel i740 graphics controller, which employs the AGP interface allowing the use of system memory to provide efficient, economical 2D and 3D performance.

This chapter covers the following subjects:

## 6.2 FUNCTIONAL DESCRIPTION

The Intel 810e chipset integrates the equivalent of an Intel i740 graphics controller into the GMCH component (Figure 6-1).

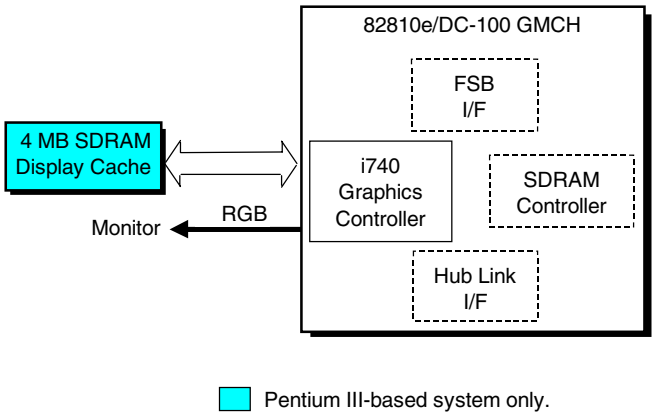



**Figure 6-1.** Graphics Subsystem Block diagram

The Intel graphics controller (Figure 6-2) integrated into the GMCH component includes 2D and 3D accelerator engines working with a deeply-pipelined pre-processor. The controller supports perspective-correct texture mapping, bilinear and anisotropic Mip-mapping, Alpha blending, Gouraud shading, and fogging.

The controller uses the AGP 2X interface and supports Type 1, Type 2, and Type 3 sideband cycles for a peak transfer rate of 533 MB/s. The AGP interface also allows the Intel graphics controller to use a portion of system memory for instructions, textures, and frame (display) buffering. Either a 32- or 64-MB block of system memory may be configured for use by the graphics controller for graphics use. Another 512-KB block (fixed) is used for memory-mapped control and status registers.

In Pentium III-based systems the controller also uses four megabytes of SDRAM (soldered down) as a display cache especially suited for 3D operation. This additional display cache allows the graphics controller to simultaneously render graphics to the Z-buffer (in the display cache) while processing textures in a portion of system memory. The 4-MB SDRAM Display Cache is accessed through a 32-bit 100-MHz interface.

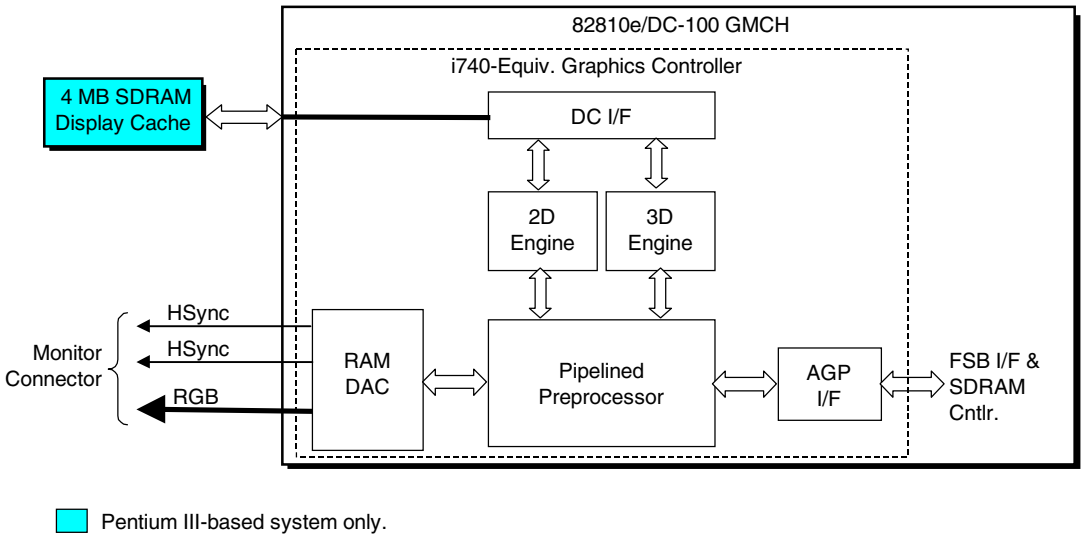



**Figure 6-2.** 82810e/DC-100 Integrated Graphics Controller

The Intel graphics controller includes special enhancements for 2D operations. Motion compensation logic is included to improve performance during software decoding of MPEG2 video. Hardware cursor and overlay engines relieve software processing and provide independent gamma correction, saturation, and brightness control.

The 230-MHz RAMDAC can support a variable-scan rate monitor up to a maximum resolution of 1600 x 1200 with 256 colors. Video BIOS for the controller is held in the system BIOS ROM and copied into systems memory at runtime for maximum performance.

### 6.2.1 FEATURE SUMMARY

- Accelerated driver support for Windows 3.1/95/98/2000, Windows NT 4.0, OS/2
- MS ActiveMovie and Media Player support for Win95
- Direct 3D support
- MS Direct Draw 5/6 support
- AGP 2X interface
- DDC2B compliant
- Accelerator engine support for:
  - 3-ROP BitBLT
  - Line Draw
  - Color expansion
  - Video color conversion/scaling
  - Motion video
  - Triangle setup

## 6.3 DISPLAY MODES

The Intel graphics controller supports the following 2D display modes:

**Table 6-1.**
Intel 2D Graphics Display Modes

| Resolution | Bits per pixel | Color Depth | Refresh Rate |
|---|---|---|---|
| 640 x 480 | 8 | 256 | 60, 70, 72, 75, 85 |
| 640 x 480 | 16 | 65K | 60, 70, 72, 75, 85 |
| 640 x 480 | 24 | 16.7M | 60, 70, 72, 75, 85 |
| 720 x 480 | 8 | 256 | 75, 85 |
| 720 x 480 | 16 | 65K | 75, 85 |
| 720 x 480 | 24 | 16.7M | 75, 85 |
| 720 x 576 | 8 | 256 | 60, 75, 85 |
| 720 x 576 | 16 | 65K | 60, 75, 85 |
| 720 x 576 | 24 | 16.7M | 60, 75, 85 |
| 800 x 600 | 8 | 256 | 60, 70, 72, 75, 85 |
| 800 x 600 | 16 | 65K | 60, 70, 72, 75, 85 |
| 800 x 600 | 24 | 16.7M | 60, 70, 72, 75, 85 |
| 1024 x 768 | 8 | 256 | 60, 70, 72, 75, 85 |
| 1024 x 768 | 16 | 65K | 60, 70, 72, 75, 85 |
| 1024 x 768 | 24 | 16.7M | 60, 70, 72, 75, 85 |
| 1152 x 864 | 8 | 256 | 60, 70, 72, 75, 85 |
| 1152 x 864 | 16 | 65K | 60, 70, 72, 75, 85 |
| 1152 x 864 | 24 | 16.7M | 60, 70, 72, 75, 85 |
| 1280 x 720 | 8 | 256 | 60, 75, 85 |
| 1280 x 720 | 16 | 65K | 60, 75, 85 |
| 1280 x 720 | 24 | 16.7M | 60, 75, 85 |
| 1280 x 960 | 8 | 256 | 60, 75, 85 |
| 1280 x 960 | 16 | 65K | 60, 75, 85 |
| 1280 x 960 | 24 | 16.7M | 60, 75, 85 |
| 1280 x 1024 | 8 | 256 | 60, 70, 72, 75, 85 |
| 1280 x 1024 | 16 | 65K | 60, 70, 72, 75, 85 |
| 1280 x 1024 | 24 | 16.7M | 60, 70, 75, 85 |
| 1600 x 900 | 8 | 256 | 60, 75, 85 |
| 1600 x 900 | 16 | 65K | 60, 75, 85 |
| 1600 x 1200 | 8 | 256 | 60, 70, 72, 75, 85 |

## 6.4 UPGRADING

The graphics controller is not upgradable.

## 6.5 PROGRAMMING

### 6.5.1 CONFIGURATION

The graphics subsystem works off the AGP bus and is configured through PCI configuration space registers using PCI protocol. These registers (Table 6-3) are configured by BIOS during POST.

**Table 6-3.**
PCI Configuration Space Registers

| PCI Config. Address | Function | PCI Config. Address | Function |
|---|---|---|---|
| 00h | Vender ID/Device ID | 14h | Relocateable I/O Base Address |
| 04h | PCI Command | 30h | Expansion ROM Base Address |
| 08h | Status | 3Ch | Interrupt Line / Interrupt Pin |
| 10h | Display Memory Base Address | -- | -- |

For a discussion of accessing PCI configuration space registers refer to chapter 4. For a detailed description of registers refer to applicable ATI Technologies, Inc. documentation.

### 6.5.2 CONTROL

#### 6.5.2.1 Standard VGA Modes

Table 6-4 list the control registers used for operating in standard VGA mode. No special drivers are required for VGA, EGA, and CGA modes. For a detailed description of the registers refer to applicable ATI Technologies, Inc. documentation.

**Table 6-4.**
Standard VGA Mode I/O Mapping

| I/O Address | Function | I/O Address | Function |
|---|---|---|---|
| 3B5.00..26h* | CRT Controller (mono) | 3C6h..3C9h | RAMDAC |
| 3BAh | VSYNC Control, Display Status | 3CAh | Read VSYNC Status |
| 3C1.00..14h* | Attribute Controller | 3CCh | Misc. Control, Read |
| 3C2h | Misc. Control / Status | 3CF.00..08h | Graphics Controller |
| 3C5h.00..04h* | Sequencer | 3D5.00..26h* | CRT Controller (color) |
| -- | -- | 3DAh | VSYNC Control, Display Status (color) |

* Index at base minus 1 (i.e., if base is 3B5h, index is at 3B4h.

#### 6.5.2.2 Extended VGA Modes

Extended modes use the video BIOS (contained in the system flash ROM) and the supplied driver.

## 6.6 MONITOR POWER MANAGEMENT CONTROL

This controller provides monitor power control for monitors that conform to the VESA display power management signaling (DPMS) protocol. This protocol defines different power consumption conditions and uses the HSYNC and VSYNC signals to select a monitor's power condition. Table 6-5 lists the monitor power conditions.

**Table 6-5.**
Monitor Power Management Conditions

| HSYNC | VSYNC | Power Mode | Description |
|---|---|---|---|
| Active | Active | On | Monitor is completely powered up. If activated, the inactivity counter counts down during system inactivity and if allowed to tiemout, generates an SMI to initiate the Suspend mode. |
| Active | Inactive | Suspend | Monitor's high voltage section is turned off and CRT heater (filament) voltage is reduced from 6.6 to 4.4 VDC. The Off mode inactivity timer counts down from the preset value and if allowed to timeout, another SMI is generated and serviced, resulting in the monitor being placed into the Off mode. Wake up from Suspend mode is typically a few seconds. |
| Inactive | Inactive | Off | Monitor's high voltage section and heater circuitry is turned off. Wake up from Off mode is a little longer than from Suspend. |

## 6.7 MONITOR CONNECTOR

The Deskpro EN SFF models provide a DB-15 connector on the rear chassis panel for connection to an analog monitor. The pinout for this connector is shown in Figure 6-3 and Table 6-6.

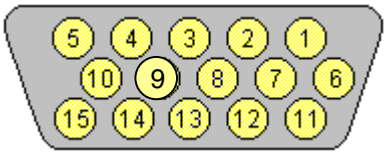



**Figure 6-3.** VGA Monitor Connector, (Female DB-15, as viewed from rear).

**Table 6-6.**
DB-15 Monitor Connector Pinout

| Pin | Signal | Description | Pin | Signal | Description |
|---|---|---|---|---|---|
| 1 | R | Red Analog | 9 | PWR | +5 VDC (fused) [1] |
| 2 | G | Blue Analog | 10 | GND | Ground |
| 3 | B | Green Analog | 11 | NC | Not Connected |
| 4 | NC | Not Connected | 12 | SDA | DDC2-B Data |
| 5 | GND | Ground | 13 | HSync | Horizontal Sync |
| 6 | R GND | Red Analog Ground | 14 | VSync | Vertical Sync |
| 7 | G GND | Blue Analog Ground | 15 | SCL | DDC2-B Clock |
| 8 | B GND | Green Analog Ground | -- | -- | -- |

NOTES:
[1] Fuse automatically resets when excessive load is removed.

# Chapter 7
# POWER and SIGNAL DISTRIBUTION

## 7.1 INTRODUCTION

This chapter describes the power supply and method of general power and signal distribution. Topics covered in this chapter include:



## 7.2 POWER SUPPLY ASSEMBLY/CONTROL

This system features a power supply assembly that is controlled through programmable logic (Figure 7-1).

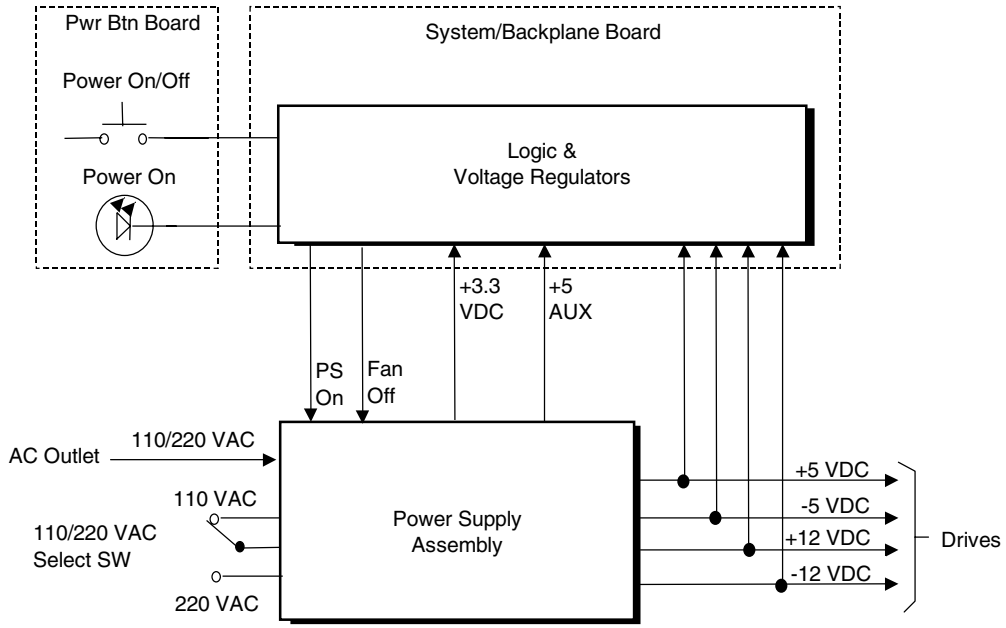



**Figure 7–1.** Power Distribution and Control, Block Diagram

## 7.2.1 POWER SUPPLY ASSEMBLY

The power supply assembly is contained in a single unit that features a selectable input voltage: 90-132 VAC and 180-264 VAC. The system uses a 90-watt supply with specifications listed in Table 7-1.

**Table 7-1.**
90-Watt Power Supply Assembly Specifications (P/N 159447)

| | Range/ Tolerance | Min. Current Loading [1] | Max. Current | Surge Current [2] | Max. Ripple |
|---|---|---|---|---|---|
| Input Line Voltage: | | | | | |
| 110 VAC Setting | 90 - 132 VAC | -- | -- | -- | -- |
| 220 VAC Setting | 180-264 VAC | -- | -- | -- | -- |
| Line Frequency | 47 - 63 Hz | -- | -- | -- | -- |
| Steady State Input (VAC) Current | -- | -- | 3.0 A | -- | -- |
| +3.3 VDC Output | +/- 5% | 0.50 A | 6.00 A | 6.00 A | 50 mV |
| +5 VDC Output | +/- 5 % | 0.70 A | 10.0 A | 12.0 A | 50 mV |
| +5 AUX Output | +/- 4 % | 0.00 A | 2.50 A | 2.50 A | 50 mV |
| +12 VDC Output | +/- 5 % | 0.05 A | 1.50 A | 3.50 A | 120 mV |
| -12 VDC Output | +/- 10 % | 0.00 A | 0.30 A | 0.30 A | 200 mV |

NOTES:

[1] Minimum loading requirements must be met at all times to ensure normal operation and specification compliance.

[2] Surge duration no longer than 10 seconds and +12 tolerance +/- 10%.

The power supply assembly features power line surge protection, withstanding brief surges of up to 2000 VAC without damage.

## 7.2.2 POWER CONTROL

The power supply assembly is controlled digitally by the PS On signal (Figure 7-1). When PS On is asserted, the Power Supply Assembly is activated and all voltage outputs are produced. When PS On is de-asserted, the Power Supply Assembly is off and no voltages (except +5 AUX) are generated. **Note that the +5 AUX voltage is always produced as long as the system is connected to a live AC source.**

The PS On signal can be controlled either by the Power Button or by the operating system (OS).

### 7.2.2.1 Power Button Control

The PS On signal is typically controlled through the Power Button which, when pressed and released, applies a negative (grounding) pulse to the power control logic. The resultant action of pressing the power button depends on the state and mode of the system at that time and is described as follows:

| System State | Pressed Power Button Results In: |
|---|---|
| Off | Negative pulse, of which the falling edge results in power control logic asserting PS On signal to Power Supply Assembly, which then initializes. ACPI four-second counter is not active. |
| On, ACPI Disabled | Negative pulse, of which the falling edge causes power control logic to de-assert the PS On signal. ACPI four-second counter is not active. |
| Full On, ACPI Enabled | (Pressed and Released in Under Four Seconds):<br>Negative pulse, of which the falling edge causes power control logic to generate SMI-, set a bit in the SMI source register, set a bit for button status, and start four-second counter. Software should clear the button status bit within four seconds and the Suspend state is entered. If the status bit is not cleared by software in four seconds PS On is de-asserted and the power supply assembly shuts down (this operation is meant as a guard if the OS is hung).<br><br>(Pressed and Held At least Four Seconds Before Release):<br>PS On is negated, de-activating the power supply. |
| Suspend, ACPI Enabled | (Pressed and Released in Under Four Seconds):<br>System wakes up to Full On.<br>(Pressed and Held At least Four Seconds Before Release):<br>System powers off. |

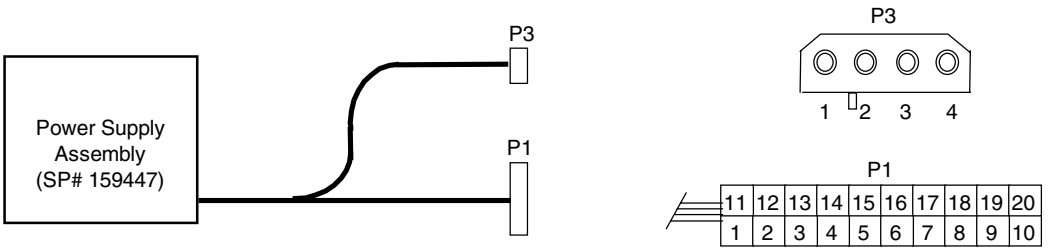
### 7.2.2.2 OS Power Control

The PS On signal can be de-asserted by the ACPI-compliant operating system such as Windows 95. This system uses ACPI mode as the default power management mode, allowing the operating system to shut off the system (once the user has selected that decision) without further user intervention.

## 7.3 POWER DISTRIBUTION

### 7.3.1 3.3/5/12 VDC DISTRIBUTION

The power supply assembly includes a multi-connector cable assembly that routes +3.3 VDC, +5 VDC, -5 VDC, +12 VC, and -12 VDC to the system board as well as to the individual drive assemblies. Figure 7-2 shows the power supply cabling.




| Conn. # | Pin 1 | Pin 2 | Pin 3 | Pin 4 | Pin 5 | Pin 6 | Pin 7 | Pin 8 | Pin 9 | Pin 10 |
|---|---|---|---|---|---|---|---|---|---|---|
| P1 | +3.3 | +3.3 | RTN | +5 | RTN | +5 | RTN | PwrGd | +5 Aux | +12 |
| P1 [1] | +3.3 | -12 | RTN | PS On | RTN | RTN | RTN | FO | +5 | +5 |
| P3 | +5 | GND | GND | +12 | | | | | | |

NOTES:

[1] This row represents pins 11-20 of connector P1.
All + and - values are VDC.
RTN = Return (signal ground)
GND = Power ground
PwrGd = Power Good
FO = Fan off

**Figure 7–2**. Power Cable Diagram

### 7.3.2 LOW VOLTAGE DISTRIBUTION

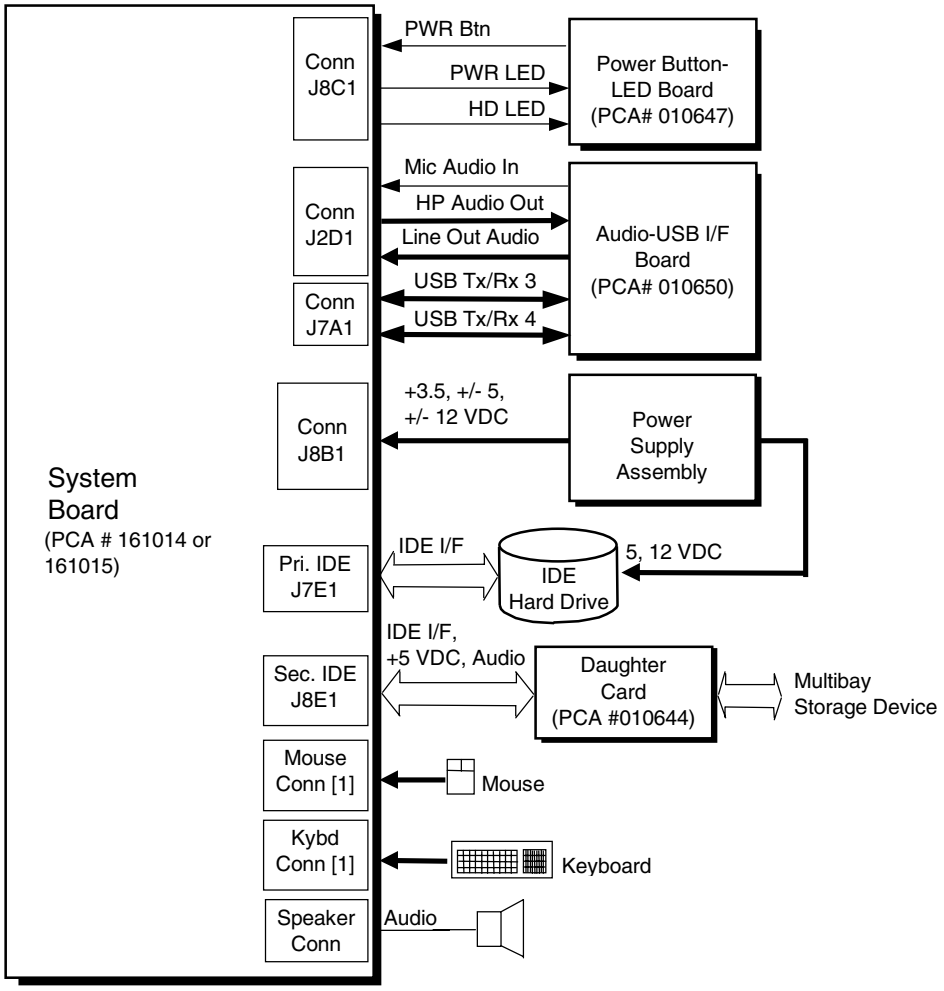
Voltages less than 3.3 VDC (including processor core (VccP) voltage) are produced through regulator circuitry on the system board.

An on-board regulator produces the VccP (processor core) voltage according to the strapping of signals VID3..0 by the processor. The possible voltages available are listed as follows:

| VID 3..0 | VccP | VID 3..0 | VccP |
|---|---|---|---|
| 0000 | 2.05 VDC | 1000 | 1.65 VDC |
| 0001 | 2.00 VDC | 1001 | 1.60 VDC |
| 0010 | 1.95 VDC | 1010 | 1.55 VDC |
| 0011 | 1.90 VDC | 1011 | 1.50 VDC |
| 0100 | 1.85 VDC | 1100 | 1.45 VDC |
| 0101 | 1.80 VDC | 1101 | 1.40 VDC |
| 0110 | 1.75 VDC | 1110 | 1.35 VDC |
| 0111 | 1.70 VDC | 1111 | 1.30 VDC |

## 7.4 SIGNAL DISTRIBUTION

Figures 7-4 shows general signal distribution between the main subassemblies of the system unit.




NOTE:

[1] On legacy-light models, PS/2-type connector. On legacy-free models, USB connector.

**Figure 7–3**. Signal Distribution Diagram

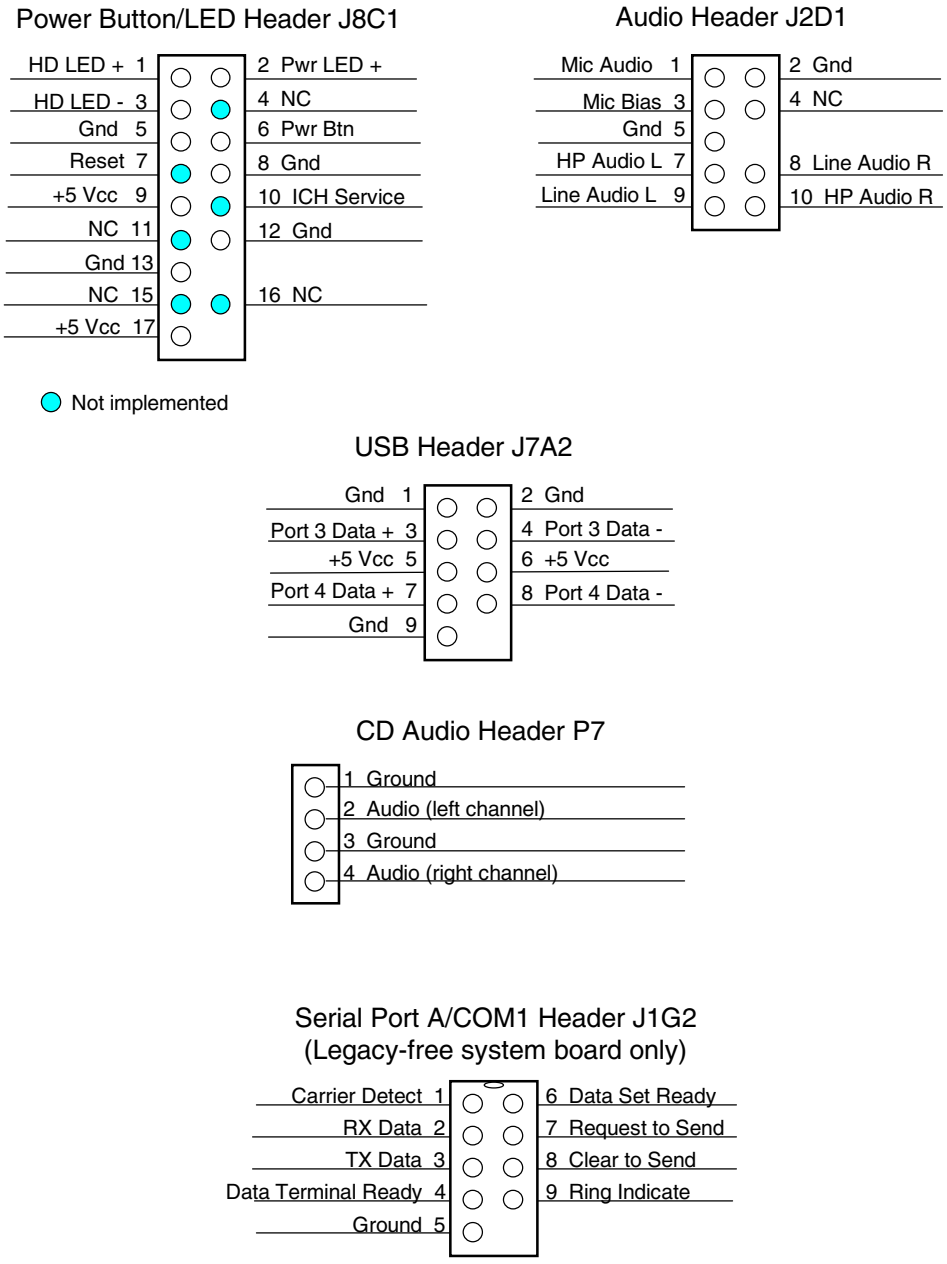



**Figure 7–4**. Header Pinouts

# Chapter 8
# BIOS ROM

## 8.1 INTRODUCTION

The Compaq iPAQ Internet Device uses Compaq BIOS firmware loaded into the 82802 FWH component. The BIOS ROM includes such functions as Power-On Self Test (POST), PCI device initialization, Plug 'n Play support, power management activities, and Setup. This chapter includes the following topics:



The firmware contained in the BIOS ROM supports the following operating systems and specifications:

- DOS 6.2
- Windows for Workgroups 3.11
- Windows 95
- Windows 98
- Windows NT 3.5 and 4.0
- OS/2 ver 2.1
- OS/2 Warp
- SCO Unix
- DMI 2.1
- Intel Wired for Management (WfM) ver. 2.2
- SMBIOS 2.3.1
- Alert-On-LAN (AOL)
- Wake-On-LAN (WOL)
- ACPI/WHIIG and OnNow
- APM 1.2
- Phoenix PMM
- PC98/99 and NetPC

The microprocessor accesses the BIOS ROM as a 128-KB block from E0000h to FFFFFh. The BIOS data is shadowed in a 64-KB block in the upper memory area. The BIOS segments are dynamically paged in and out of the 64-KB block as they are needed.

> **NOTE:** This chapter describes BIOS in general and focuses only on aspects of BIOS unique to this particular system..

## 8.2 DESKTOP MANAGEMENT SUPPORT

Desktop Management deals with issues of security, identification, and system management functions. Desktop Management is provided by BIOS INT 15 functions listed Table 8-1.

**Table 8-1.**
Desktop Management Functions (INT15)

| AX | Function | Mode |
|---|---|---|
| E800h | Get system ID | Real, 16-, & 32-bit Prot. |
| E807h | Get System Information Table | Real, 16-, & 32-bit Prot. |
| E813h | Get monitor information | Real, 16-, & 32-bit Prot. |
| E814h | Get system revision | Real, 16-, & 32-bit Prot. |
| E816h | Get temperature status | Real, 16-, & 32-bit Prot. |
| E817h | Get drive attribute | Real |
| E818h | Get drive off-line test | Real |
| E819h | Get chassis serial number | Real, 16-, & 32-bit Prot. |
| E81Ah | Write chassis serial number | Real |
| E81Bh | Get drive threshold | Real |
| E81Eh | Get drive ID | Real |
| E820h | System Memory Map | Real |
| E822h | Flash ROM/Sys. Admin. Fnc. | Real, 16-, & 32-bit Prot. |
| E827h | DIMM EEPROM Access | Real, 16-, & 32-bit Prot. |
| E828h | Inhibit power button | Real, 16-, & 32-bit Prot. |
| E845h | Access CMOS Feature Bits | Real, 16-, & 32-bit Prot. |
| E846h | Security Functions | Real, 16-, & 32-bit Prot. |

All 32-bit protected mode calls are accessed by using the industry-standard BIOS32 Service Directory. Using the service directory involves three steps:

1. Locating the service directory.
2. Using the service directory to obtain the entry point for the client management functions.
3. Calling the client management service to perform the desired function.

The BIOS32 Service Directory is a 16-byte block that begins on a 16-byte boundary between the physical address range of 0E0000h-0FFFFFh. The format is as follows:

| Offset | No. Bytes | Description |
|---|---|---|
| 00h | 4 | Service identifier (four ASCII characters) |
| 04h | 4 | Entry point for the BIOS32 Service Directory |
| 08h | 1 | Revision level |
| 09h | 1 | Length of data structure (no. of 16-byte units) |
| 0Ah | 1 | Checksum (should add up to 00h) |
| 0Bh | 5 | Reserved (all 0s) |

To support Windows NT an additional table to the BIOS32 table has been defined to contain 32-bit pointers for the DDC and SIT locations. The Windows NT extension table is as follows:

```
; Extension to BIOS SERVICE directory table (next paragraph)

        db      "32OS"          ; sig
        db      2               ; number of entries in table
        db      "$DDC"          ; DDC POST buffer sig
        dd      ?               ; 32-bit pointer
        dw      ?               ; byte size
        db      "$SIT"          ; SIT sig
        dd      ?               ; 32-bit pointer
        dw      ?               ; byte size
        db      "$ERB"          ; ESCD sig
        dd      ?               ; 32-bit pointer
        dw      ?               ; bytes size
```

The service identifier for Desktop Management functions is "$CLM." Once the service identifier is found and the checksum verified, a FAR call is invoked using the value specified at offset 04h to retrieve the CM services entry point. The following entry conditions are used for calling the Desktop Management service directory:

```
INPUT:
        EAX             = Service Identifier [$CLM]
        EBX (31..8)     = Reserved
        EBX (7..0)      = Must be set to 00h
        CS              = Code selector set to encompass the physical page holding
                          entry point as well as the immediately following physical page.
                          It must have the same base. CS is execute/read.
        DS              = Data selector set to encompass the physical page holding
                          entry point as well as the immediately following physical page.
                          It must have the same base. DS is read only.
        SS              = Stack selector must provide at least 1K of stack space and be 32-bit.
        (I/O permissions must be provided so that the BIOS can support as necessary)

OUTPUT:
        AL              = Return code:
                          00h, requested service is present
                          80h, requested service is not present
                          81h, un-implemented function specified in BL
                          86h and CF=1, function not supported
        EBX             = Physical address to use as the selector BASE for the service
        ECX             = Value to use as the selector LIMIT for the service
        EDX             = Entry point for the service relative to the BASE returned in EBX
```

### 8.2.1 SYSTEM ID

The INT 15, AX=E800h BIOS function can be used to identify the type of system. This function will return the system ID in the BX register.

| System | ROM Type | PnP ID | System ID |
|---|---|---|---|
| Compaq iPAQ | 686J1 | CPQB1A0 | 0630h |

### 8.2.2 SYSTEM INFORMATION TABLE

The System Information Table (SIT) is a comprehensive list of fixed configuration information arranged into records. The INT 15 AX=E807h BIOS function accesses the SIT by returning a pointer in ES:BX to indicate the location of the SIT. This system includes the following SIT records:

| Record # | Function |
|---|---|
| 01h | Power conservation |
| 02h | System standby |
| 03h | Display screensave |
| 04h | Hard drive timeout counter |
| 05h | Security features |
| 06h | Processor, memory, cache attributes |
| 07h | General peripheral & input device information |
| 08h | Memory module information |
| 09h | Timeout default value |
| 0Ah | CMOS information |
| 0Eh | Extended disks information |
| 0Fh | System information |
| 10h | Product name header |
| 12h | Processor micro-code patch data |

The SIT records are used by Compaq applications such as Diagnostics, Inspect, and Insight Manager. Other applications may use SMBIOS firmware to obtain system data.

### 8.2.3 EDID RETRIEVE

The BIOS function INT 15, AX=E813h is a tri-modal call that retrieves the VESA extended display identification data (EDID). Two subfunctions are provided: AX=E813h BH=00h retrieves the EDID information while AX=E813h BX=01h determines the level of DDC support.

Input:

AX = E813h
BH = 00 Get EDID .
BH = 01 Get DDC support level

If BH = 00 then
DS:(E)SI = Pointer to a buffer (128 bytes) where ROM will return block
If 32-bit protected mode then
DS:(E)SI = Pointer to $DDC location

Output:
(Successful)

If BH = 0:
DS:SI=Buffer with EDID file.
CX = Number of bytes written
CF = 0
AH =00h Completion of command

If BH = 1:
BH = System DDC support
<0>=1 DDC1 support
<1>=1 DDC2 support
BL = Monitor DDC support
<0>=1 DDC1 support
<1>=1 DDC2 support
<2>=1 Screen blanked during transfer

(Failure)

CF = 1
AH = 86h or 87h

### 8.2.4 DRIVE FAULT PREDICTION

The Compaq BIOS provides direct Drive Fault Prediction support for IDE-type hard drives. This feature is provided through two BIOS calls. Function INT 15, AX=E817h is used to retrieve a 512-byte block of drive attribute data while the INT 15, AX=E81Bh is used to retrieve the drive's warranty threshold data. If data is returned indicating possible failure then the following message is displayed:

"1720-Intellisafe Hard Drive detects imminent failure"

### 8.2.5 SYSTEM MAP RETRIEVAL

The BIOS function INT 15, AX=E820h will return base memory and ISA/PCI memory contiguous with base memory as normal memory ranges. This real mode call will indicate chipset-defined address holes that are not in use, motherboard memory-mapped devices, and all occurrences of the system BIOS as reserved. Standard PC address ranges will not be reported.

Input:

EBX = continuation value or 00000000h to start at beginning of map
ECX = number of bytes to copy (>=20)
EDX = 534D4150h ('SMAP')
ES:DI = buffer for result (see below)

| Offset | Size | Description |
|---|---|---|
| 00h | QWORD | base address |
| 08h | QWORD | length in bytes |
| 10h | DWORD | type of address range |

01h memory, available to OS
02h reserved, not available (e.g. system ROM, memory-mapped device)
other: not defined

Output:
If CF=0 (success)

EAX = 534D4150h ('SMAP')
EBX = next offset from which to copy or 00000000h if finished
ECX = actual length returned in bytes
ES:DI buffer filled

If CF=1 (failure)

AH = Error Code (86h)

In order to determine the entire memory map, multiple calls must be made.
For example, the first call would be:

Input:

EDX = 534D4150h
EBX = 00h
ECX = 14h
ES:DI = some buffer to store information.

Output:

EAX = 534D4150h
EBX = 01h
ECX = 14h
ES:DI = 00 00 00 00 00 00 00 00 00 FC 09 00 00 00 00 00 01 00 00 00
(indicates 0-639k is available to the OS)

Consecutive calls would continue until EBX returns with 0, indicating that the memory map is complete.

### 8.2.6 FLASH ROM FUNCTIONS

The system BIOS may be upgraded by flashing the ROM using the INT 15, AX=E822h BIOS interface, which includes the necessary subfunctions. An upgrade utility is provided on a ROMPAQ diskette.

### 8.2.7 POWER BUTTON FUNCTIONS

The BIOS includes an interface for controlling the system unit's power button. The power button can be disabled and enabled.

The INT 15, AX=E822h, BL=08h function can be invoked to disable the power button, preventing a user from inadvertently powering down the system. This tri-modal function is typically used in the ROM flashing procedure to reduce the chance of an accidental power down while the BIOS is being upgraded.

Entry:
AX = E822h
BL = 08h

Return:
(Successful)
CF = 0
AH = 00

(Failure)
CF = 1
AH = 86, not supported

**NOTE:** With the Disable function invoked the system can **still** be powered down by holding the power button in for four seconds or more.

The INT 15, AX=E822h, BL=09h function is used to restore the power button to the state it was in prior to invoking the Disable (BL=08h) function.

Entry:
AX = E822h
BL = 09h

Return:
(Successful)
CF = 0
AH = 00

(Failure)
CF = 1
AH = 86, call not supported

### 8.2.8 ACCESSING CMOS

Configuration memory data can be retrieved with the BIOS call INT 15, AX=E823h. This tri-modal function retrieves a specific byte from the CMOS map described in Chapter 4. The function is described as follows:

INPUT:

| | |
|---|---|
| EAX | = E823h |
| BH | = 0, Read |
| | = 1, Write |
| BL | = Value to write (if a write is specified) |
| CX | = Bytes number (zero-based) |

OUTPUT:
(Successful)

| | |
|---|---|
| CF | = 0 |
| AH | = 00h |
| AL | = Byte value (on a read) |

(Failure)

| | |
|---|---|
| CF | = 1 |
| AH | = 86h, Function not supported |
| | = FFh, byte does not exist |

### 8.2.9 ACCESSING CMOS FEATURE BITS

The BIOS function INT 15, AX=E845h is a tri-modal call for accessing areas in non-volatile memory (CMOS) used for storing variables for various features. Note that this function differs from the previously discussed call since data blocks of varying lengths are retrieved.

INPUT:

| | |
|---|---|
| EAX | = E845h |
| BL | = 0, Read |
| | = 1, Write |
| BH | = Value Read/to Write |
| CX | = Feature Bits Number (refer to Table 8-2) |
| DS:SI | = Pointer to buffer passing multiple byte features |

OUTPUT:
(Successful)

| | |
|---|---|
| CF | = 0 |
| EAX | = Reserved |
| BH | = Value read (on a read) |

(Failure)

| | |
|---|---|
| CF | = 1 |
| AH | = 86h, Function not supported |

**Table 8-2.**
CMOS Feature Bits

| CX | Function | Default Value | Default Setting | CX | Function | Default Value | Default Setting |
|---|---|---|---|---|---|---|---|
| 0000h | PCI 2.1 Mode Enable | 01h | Yes | 0025h | Asset Tag | [1] | [1] |
| 0001h | Erase Eaze Kybd | 03h | Ign. | 0026h | Bck-to-bck I/O Delay | 00h | Norm |
| 0002h | COM/IR Port Select | 00h | COM | 0027h | CMOS 10-2Fh BU | [1] | [1] |
| 0003h | PnP Rejects SET | 00h | Yes | 0028h | QuickLock after Stby | 00h | No |
| 0004h | PCI VGA Snoop | 00h | No | 0029h | Audio Chip Enable | 01h | Yes |
| 0005h | PCI Bus Mastering | 00h | Yes | 002Ah | Audio IRQ | 01h | IRQ5 |
| 0006h | Auto Prompt Setup | 00h | Yes | 002Bh | Audio DMA | 02h | DMA1 |
| 0007h | Mode 2 Config. Enable | 01h | Yes | 002Ch | Audio Addr. | 00h | 22xh |
| 0008h | Sec. IDE Cntlr, En. | 01h | Yes | 002Dh | ECP DMA Config. | 03h | DMA3 |
| 0009h | Sec. IDE Cntlr. IRQ | 03h | IRQ15 | 002Eh | COM1 Base Addr. | 3Fh | 3F8h |
| 000Ah | Custom Drive Type 1 | 00h | [1] | 002Fh | COM1 IRQ | 00h | Rsrvd |
| 000Bh | Custom Drive Type 2 | 00h | [1] | 0030h | COM2 Base Addr. | 1Fh | 2F8h |
| 000Ch | Custom Drive Type 3 | 00h | [1] | 0031h | COM2 IRQ | 00h | Rsrvd |
| 000Dh | Custom Drive Type 4 | 00h | [1] | 0032h | UDMA33 Enable | 0Fh | Yes |
| 000Eh | POST Verbose/Terse | 01h | Terse | 0033h | Net Server Md En. | 00h | No |
| 000Fh | Translate SCSI Drive | 00h | Yes | 0034h | CIA BOM No. Bytes | [1] | [1] |
| 0010h | Mfg. Process no. | [1] | [1] | 0035h | Copy Std. CMOS | [1] | [1] |
| 0011h | Admin. Password | [1] | [1] | 0036h | AGP Adapter Srch. | 01h | Yes |
| 0012h | Pwr-On Password | [1] | [1] | 0037h | APM Fan Throttle | 00h | Auto |
| 0013h | Ownership Tag | [1] | [1] | 0038h | Mfg. Diags. Enable | 00h | No |
| 0014h | Warm Boot Pswrd En. | 00h | Yes | 0039h | RIPL ROM Boot En. | 01h | Yes |
| 0015h | Hood Lock Enable | 00h | Yes | 003Ah | Exit CleanBoot Scrn. | [1] | [1] |
| 0016h | Hood Removal En. | 00h | No | 003Bh | Ethernet Speed Sel. | 00h | Auto |
| 0017h | USB Security Enable | 01h | Yes | 003Ch | Ethernet Mode Sel. | 00h | Auto |
| 0018h | Power Supply Mode | 01h | ACPI | 003Dh | Ethernet Conn. Type | 01h | UTP |
| 0019h | QuickBoot Mode | 1Fh | Fast | 003Eh | ACPI Enable | 01h | Yes |
| 001Ah | Onbd NIC Enable | 01h | Yes | 003Fh | S/W BOM S/N | | |
| 001Bh | Onbd. SCSI Enable | 01h | Yes | 0040h | ECP Mode Selected | 01h | Yes |
| 001Ch | Onbd. Pri. IDE Enable | 01h | Yes | 0041h | NT Shutdown Dvr. | 00h | No |
| 001Dh | Ultra SCSI Md. Enable | 00h | No | 0042h | Em. SCSI Priority | 00h | Lowest |
| 001Eh | QuickLock Enable | 00h | No | 0043h | Factor Boot Sel. | 00h | |
| 001Fh | QuickBlank Enable | 00h | No | 0044h | Product Name | 00h | [1] |
| 0020h | Serial I/F 1 Security [2] | 01h | No | 0045h | UUID | 00h | [1] |
| 0021h | Serial I/F 2 Security | 01h | No | 0046h | Processor # Enable | 01h | Yes |
| 0022h | Printer I/F Security [2] | 01h | No | 0047h | After G3 State | 00h | Off |
| 0023h | CD/Diskette Boot | 00h | Yes | 0048h | UUID Enable | 01h | Yes |
| 0024h | CD/Diskette Write | 00h | Yes | -- | -- | -- | -- |

NOTE:

Not applicable to these systems.

[1] Default Value will be pointer to buffer DS:SI (16-bit mode) or DS:(E)SI (32-bit mode) where actual data is held. Default Setting will be unique for each system.

[2] Legacy-light system only.

## 8.2.10 SECURITY FUNCTIONS

The INT 15 AX=E846h BIOS function is used to control various security features of the system. This function may be issued by a remote system (over a network). The issuing driver must build a request buffer for each security feature prior to making the call. This system supports the following security features:

- QuickLock
- IDE controller disable
- Serial port disable (legacy-light only)
- Parallel port disable (legacy-light only)
- Change administrator password
- QuickLock on suspend
- Ownership tag
- USB disable (legacy-light only)

The write-protect function that determines diskette write control is extended to cover all drives that use removable read/write media (i.e., if diskette write protect is invoked, then any diskette drive, power drive (SCSI and/or ATAPI), and floptical drive installed will be inaccessible for (protected from) writes). Client management software should check the following bytes of SIT record 07h for the location and access method for this bit:

**System Information Table, Peripheral and Input Device Record (07h) (partial listing)**

| Byte | Bit | Function |
|---|---|---|
| 1Fh | 7-0 | Removable Read/Write Media Write Protect Enable Byte Offset (0-255) |
| 20h | | Removable Read/Write Media Write Protect Enable Bit Location: |
| | 7..4 | CMOS Type:<br>0000 = CMOS<br>0001 = High CMOS<br>0010 = NVRAM<br>0011 = Flat model NVRAM |
| | 3..0 | Bit Location:<br>0000 = Bit 0 0100 = Bit 4<br>0001 = Bit 1 0101 = Bit 5<br>0010 = Bit 2 0110 = Bit 6<br>0011 = Bit 3 0111 = Bit 7 |

## 8.3 MEMORY DETECTION AND CONFIGURATION

This system uses the Serial Presence Detect (SPD) method of determining the installed DIMM configuration. The BIOS communicates with an EEPROM on each DIMM through an $I^2C$-type bus to obtain data on the following DIMM parameters:

- Presence
- Size
- Type
- Timing/CAS latency

**NOTE:** Refer to Chapter 3, "Processor/Memory Subsystem" for the SPD format and DIMM data specific to this system.

The BIOS performs memory detection and configuration with the following steps:

1. Set Memory Buffer Strength – The memory controller must be configured for correct buffer drive strength. The BIOS provides this function by reading the number of module banks, ECC enable/disable status, and SDRAM width data from the DIMMs and transferring that data to the memory controller. SPD bytes checked: 5, 11, 13
2. Determine DIMM Presence/Type – The BIOS checks each memory socket for DIMM presence. If present, the DIMM type and CAS latency is determined. SPD bytes checked: 2, 9, 10, 18, 23, 24.
   Check Sequence:
   a. SPD byte 2 is read for all slots first. A failed read or returned value of other than 02h (EDO) or 04h (SDRAM) results in the slot marked as empty. If mixed types are detected then only SDRAMs are used (see chapter 3 for details).
   b. SPD byte 18 is read for maximum CAS latency, followed by reads of bytes 9 and 10 for bus speed compatibility. A DIMM detected as too-slow results in an error.
   c. If the DIMM can handle the memory bus speed at maximum CAS latency then bytes 23 and 24 are checked to see if the DIMM can work maximum CAS latency minus 1. Once all slots are checked, the greatest CAS latency (2 or 3) is used. A DIMM detected as incompatible will result in a bit in CMOS being set and the Num Lock LED on the keyboard will blink for a short time. Depending on the progress of the BIOS routine a POST message may be displayed before the system locks up.
3. Initialize SDRAM – If SDRAM are installed then each row containing SDRAM will be initialized. This step includes pre-charging all banks, sending a CAS-before-RAS command, sending a Mode-Register-Set-Enable command, reading DIMM location/CAS latency data, and sending a Normal Op command.
4. Memory Sizing – The SPD bytes 3, 4, and 17 are checked for number of row and column addresses and (for SDRAM) the number of internal banks.
5. Memory Timing – For SDRAM, the memory controller requires the RAS pre-charge time and the RAS-to-CAS delay time. SPD bytes checked: 27and 29.

## 8.4 PNP SUPPORT

The BIOS includes Plug 'n Play (PnP) support for PnP version 1.0A.

> **NOTE**: For full PnP functionality to be realized, all peripherals used in the system must be designed as "PnP ready." Any installed ISA peripherals that are not "PnP ready" can still be used in the system, although configuration parameters may need to be considered (and require intervention) by the user.

Table 8-2 shows the PnP functions supported (for detailed PnP information refer to the Compaq BIOS Technical Reference Guide):

**Table 8-2.**
PnP BIOS Functions

| Function | Register |
|---|---|
| 00h | Get number of system device nodes |
| 01h | Get system device node |
| 02h | Set system device node |
| 03h | Get event |
| 04h | Send message |
| 40h | Get ISA configuration [1] |
| 50h | Get SMBIOS Structure Information |
| 51h | Get Specific SMBIOS Structure |

NOTE:
[1] Since no ISA slots are present, this function will return 0 for the max. CSN.

The BIOS call INT 15, AX=E841h, BH=01h can be used by an application to retrieve the default settings of PnP devices for the user. The application should use the following steps for the display function:

1. Call PnP function 01(get System Device Node) for each devnode with bit 1 of the control flag set (get static configuration) and save the results.
2. Call INT 15, AX=E841h, BH=01h.
3. Call PnP "Get Static Configuration" for each devnode and display the defaults.
4. If the user chooses to save the configuration, no further action is required. The system board devices will be configured at the next boot. If the user wants to abandon the changes, then the application must call PnP function 02 (Set System Device Node) for each devnode (with bit 1 of the control flag set for static configuration) with the results from the calls made prior to invoking this function.

### 8.4.1 SMBIOS

This system supports System Management BIOS (SMBIOS) version 2.3.1, which is compliant with the Desktop Management Interface (DMI) specification. The PnP functions 50h and 51h are used to retrieve the SMBIOS data, which is stored using management information format (MIF) structures. Function 50h retrieves the number of structures, size of the largest structure, and SMBIOS version. Function 51h retrieves a specific structure. This system the following structure types:

| Type | Data |
|---|---|
| 0 | BIOS Information |
| 1 | System Information |
| 3 | System Enclosure or Chassis |
| 4 | Processor Information |
| 5 | Memory Controller Information |
| 6 | Memory Module Information |
| 7 | Cache Information |
| 8 | Port Connector Information |
| 9 | System Slots |
| 10 | On Board Device Information |
| 12 | System Configuration Options |
| 13 | BIOS Language Information |
| 16 | Physical Memory Array |
| 17 | Memory Devices |
| 18 | Memory Error Information |
| 19 | Memory Array Mapped Addresses |
| 20 | Memory Device Mapped Addresses |

## 8.5 POWER MANAGEMENT FUNCTIONS

The BIOS provides three types of power management support: independent PM support; ACPI support, and APM support. These power management interfaces share a common goal of reducing energy consumption during periods of system inactivity. The following table compares and describes the different system states identified by the various power management interfaces.

| Global State | Sleep State | System Condition | Power Consumption | OS Restart Required |
|---|---|---|---|---|
| G0 | -- | Fully on. OS and application software is running, all devices are active, responsive, and maintaining context. | Maximum | No |
| G1 | S1 | On, with CPU executing and data held in memory, but peripheral devices (display output, some I/O) may be disabled/low power. | Low | No |
| | S2/S3 | On, but CPU not executing and cache context lost. Memory is maintained. Display and I/O devices disabled or under low power. | Low | No |
| | S4 | Off. CPU and most other devices powered off. No data held in RAM, but memory image from lower state has been saved to disk for recall upon wake up. | Low | Yes |
| G2 | S5 | Soft Off. OS has completed shutdown. Some devices may be powered to allow for "wake up" to occur resulting in a full boot sequence. | Minimum | Yes |
| G3 | -- | Mechanical off. Power to unit has been switched off (or unit has been unplugged). Only internal RTC battery power is being consumed. Unit may be disassembled/serviced safely. | None | Yes |

### 8.5.1 INDEPENDENT PM SUPPORT

The BIOS ROM can provide power management of the system independently from any software (OS or application) that is running on the system. In this mode the BIOS uses a timer to determine when to switch the system to a different power state. State switching is not reported to the OS and occurs as follows:

**On** – The computer is running normally and is drawing full power.

**Standby** – The computer is in a low power state. In this state the processor and chipset are still running and the VSYNC signal to the monitor is turned off. Returning to the On state requires very little time and will be initiated by any of the following actions:

a. key stroke
b. mouse movement

**Off** – The computer is not running and drawing practically no power at all.

### 8.5.2 ACPI SUPPORT

This system meets the hardware and firmware requirements for being ACPI compliant. The BIOS function INT 15 AX=E845h can be used to check or set the ACPI enable/disable status of the system, which defaults to the "ACPI enabled" state. The setup option for ACPI should be disabled if APM/PnP is to be used with Windows 98 or when disabling power management and PnP support for NT5.0. A hardware redetection should be made with Windows 98 and a reinstall of Windows NT5.0 should be performed when an ACPI switch is made. This system supports the following ACPI functions:

- PM timer
- Power button
- Power button override
- RTC alarm
- Sleep/Wake logic (S1, S4 (NT), S5
- Legacy/ACPI select
- C1 state (Halt)
- C2 state (STOPGRANT)
- C3 state (no clock)
- PCI PME

### 8.5.3 APM 1.2 SUPPORT

Advanced Power Management (APM) BIOS support provides interaction between the BIOS ROM and the operating system (OS). The BIOS advises the OS when a power state transition should occur. The OS then notifies the appropriate driver(s) and reports back to the BIOS. For maximum energy-conservation benefit, APM functionality should be implemented using the following three layers:

- BIOS layer (APM BIOS (ver. 1.2, 1.1, 1.0))
- Operating system (OS) layer (APM driver)
- Application layer (APM-aware application or device driver)

The process starts with the OS or driver making a connection with the BIOS through an APM BIOS call. In a DOS environment POWER.EXE makes a Real mode connection. In Windows 3.1 and in Windows 95, a 32-bit connection is made. Currently Windows NT does not make an APM connection. With power management enabled, inactivity timers are monitored.

When an inactivity timer times out, an SMI is sent to the microprocessor to invoke the SMI handler. The SMI handler works with the APM driver and APM BIOS to take appropriate action based on which inactivity timer timed out.

Three power states are defined under power management:

**On** - The computer is running, all subsystems are on and drawing full power. Any activity in the following subsystems will reset the activity timer, which has a default setting of 15 minutes before Standby entered:

a. Keyboard (PS/2 only)
b. Mouse (PS/2 only)
c. Serial port
d. Hard drive

**Standby** - The computer is in a low power state: video is off, some subsystems may be drawing less power, and the microprocessor is halted except for servicing interrupts. Video graphics controller is under driver control and/or VSYNC is off and the power supply fan is turned off. Any of the following activities will generate a wake-up SMI and return the system to On:

a. Keyboard (PS/2 only)
b. Mouse (PS/2 only)
c. Serial port
d. Hard drive
e. RTC Alarm
f. Power Button

If no APM connection is present, the BIOS will set an APM timer to 45 minutes, at which time the Suspend will be entered if no activity has occurred. This function can be defeated (so that Suspend will **not** be achieved). If an APM connection is present, the BIOS APM timer is not used and Suspend is entered only by user request either through an icon in Windows 95 or by pressing and releasing the power button under 4 seconds.

**Suspend** - The computer is in a low power state: video graphics controller is under driver control and/or HSYNC and VSYNC are off, some subsystems may be drawing less power, and the microprocessor is halted except for servicing interrupts. Any of the following activities will generate a wake-up SMI and return the system to On:

a. Keyboard (PS/2 only)
b. Mouse (PS/2 only)
c. Serial port
d. Diskette drive
e. Hard drive
f. RTC Alarm
g. Network interface controller

The APM BIOS for this system supports APM 1.2 as well as previous versions 1.1 and 1.0. The APM BIOS functions are listed in Table 8-3.

**Table 8-3.**
APM BIOS Functions (INT15)

| AX | Function |
|---|---|
| 5300h | APM Installation Check |
| 5301h | APM Connect (Real Mode) |
| 5302h | APM Connect (16-bit Protected Mode) |
| 5303h | APM Connect (32-bit Protected Mode) |
| 5304h | Interface Disconnect |
| 5305h | CPU Idle |
| 5306h | CPU Busy |
| 5307h | Set Power State [1] |
| 5308h | Enable/Disable Power Management |
| 5309h | Restore Power On Defaults |
| 530Ah | Get Power Status |
| 530Bh | Get PM Event |
| 530Ch | Get Power State |
| 530Dh | Enable/Disable Device Power Management |
| 530Eh | APM Driver Version |
| 530Fh | Engage/Disengage Power Management |
| 5380h | OEM (Compaq) Specific APM Function |

## 8.6 USB LEGACY SUPPORT

The BIOS ROM checks the USB port, during POST, for the presence of a USB keyboard. This allows a system with only a USB keyboard to be used during ROM-based setup and also on a system with an OS that does not include a USB driver.

On such a system a keystroke will generate an SMI and the SMI handler will retrieve the data from the device and convert it to PS/2 data. The data will be passed to the keyboard controller and processed as in the PS/2 interface. Changing the delay and/or typematic rate of a USB keyboard though BIOS function INT 16 is not supported.

The system does not support hot-plugging of a USB keyboard, nor is a keyboard attached to a USB hub supported. A PS/2 keyboard and a USB keyboard can, however, be connected and used simultaneously.

## 8.7 BIOS UPGRADING

The flash ROM device can be re-written with updated BIOS code if necessary. The flashing procedure is as follows:

1. Create a system (bootable) diskette using the FORMAT A: /S command in DOS.
2. Download the appropriate BIOS firmware from the Compaq web site.
3. Copy the downloaded BIOS file and the flash utility file onto the boot diskette.
4. Unzip the BIOS and flash utility files, which should result in an .exe file and a .bin file.
5. Place the boot diskette into drive A: and reboot the system.
6. At the A: prompt, type in "*filename*.exe *filename*.bin" (there is a space between the file names) and press **Enter.**
7. At the Flash Memory Write menu, to the question "Do you want to save BIOS?" select Y. If you want to save the current BIOS then type the current BIOS name and the extension after "File name to save" (example: type in 613j900.bin). Alternately, select N if you do not want to save the current BIOS.
8. To the question "Are you sure to program?" select Y.
9. Wait until the message "Power Off or Reset the system," indicating the BIOS has been loaded successfully. Then remove the boot diskette. **Should power be lost or the system reset during this time (before the message is displayed) the BIOS code in ROM will likely be corrupted and the procedure will have to be repeated (starting at step 5).**
10. Turn off (power down) the system.
11. While holding the **End** key down, turn on (power up) the system, making sure the **End** key is held down until the Setup utility is entered.
12. Complete the Setup utility as appropriate.
13. Re-boot the system.

# Appendix A
# ERROR MESSAGES AND CODES

## A.1 INTRODUCTION

This appendix lists the error codes and a brief description of the probable cause of the error**. Note that not all errors listed in this appendix may be applicable to a particular system depending on the model and/or configuration**.

## A.2 POWER-ON MESSAGES

**Table A-1.**
Power-On Messages

| Message | Beeps | Probable Cause |
|---|---|---|
| CMOS Time and Date Not Set | (None) | Invalid time or date |
| (none) | 2 short | Power-On successful |
| Run Setup | (None) | Any failure |

## A.3 BEEP/KEYBOARD LED CODES

**Table A-2.**
Beep/Keyboard LED Codes

| Beeps | LED [1] | Probable Cause |
|---|---|---|
| 1 short, 2 long | NUM lock blinking | Base memory failure. |
| 1 long, 2 short | CAP lock blinking | Video/graphics controller failure. |
| 2 long, 1 short | Scroll lock blinking | System failure (prior to video initialization). |
| None | All three blink in sequence | Keyboard locked in network mode. |
| None | NUM lock steady on | ROMPAQ diskette not present, bad, or drive not ready. |
| None | CAP lock steady on | Password prompt. |
| None | All three blink together | ROM flash failed. |
| None | All three steady on | Successful ROM flash. |

NOTE:

[1] PS/2 keyboard only.

## A.4 POWER-ON SELF TEST (POST) MESSAGES

**Table A-3.**
Power-On Self Test (POST) Messages

| Error Message | Probable Cause |
|---|---|
| Bad PnP Serial ID Checksum | Serial ID checksum of PnP card was invalid. |
| Address Lines Short! | Error in address decoding circuitry on system board. |
| Cache Memory Failure, Do Not Enable Cache! | Defective cache memory, CPU has failed. |
| CMOS Battery Failed | Low RTC/CMOS battery |
| CMOS Checksum Invalid | Previous and current checksum value mismatch. |
| CMOS System Options Not Set | Corrupt or non-existant CMOS values. |
| CMOS Display Type Mismatch | Graphics/video type in CMOS does not match type detected by BIOS. |
| CMOS Memory Size Mismatch | Memory amount detected does not match value stored in CMOS. |
| CMOS Time and Date Not Set | Time and date are invalid. |
| Diskette Boot Failure | Boot disk in drive A: is corrupt. |
| DMA Bus Timeout | Bus driven by device for more than 7.8 us |
| DMA Controller Error | Error in one or both DMA controllers. |
| Drive Not Ready Error | BIOS cannot access the diskette drive. |
| Diskette Drive Controller Failure | BIOS cannot communicate with diskette drive controller. |
| Diskette Drive Controller Resource Conflict | Diskette drive controller has requested a resource already in use. |
| Diskette Drive A: Failure | BIOS cannot access drive A:. |
| Diskette Drive B: Failure | BIOS cannot access drive B: |
| Gate A20 Failure | Gate A20 of keyboard controller not working. |
| Invalid Boot Diskette | BIOS can read but cannot boot system from drive A:. |
| Keyboard Controller Error | Keyboard controller failure. |
| Keyboard is Locked…Please Unlock It | Locked keyboard. |
| Keyboard Stuck Key Detected | Key pressed down. |
| Master DMA Controller Error | Error exists in master DMA controller. |
| Master Interrupt Controller Error | Master interrupt controller failure. |
| Memory Size Decreased | Amount of memory detected is less than stated value in CMOS. |
| NVRAM Checksum Error, NVRAM Cleared | ESCD data was re-initialized due to NVRAM checksum error. |
| NVRAM Cleared By Jumper | NVRAM has been cleared by removal of jumper. |
| NVRAM Data Invalid, NVRAM Cleared | Invalid entry in ESCD. |
| Off Board Parity Error Addr. (HEX) = X | Parity error occurred in expansion memory, x= address of error. |
| Parallel Port Resource Conflict | Parallel port has requested a resource already in use. |
| PCI Error Log is Full | PCI conflict error limit (15) has been reached. |
| PCI I/O Port Conflict | Two devices requested the same resource. |
| PCI Memory Conflict | Two devices requested the same resource. |
| Primary Boot Device Not Found | Designated primary boot device could not be found. |
| Primary IDE Cntrl. Resource Conflict | Primary IDE controller requested a resource already in use. |
| Primary Input Device Not Found | Designated primary input device could not be found. |
| Secondary IDE Controller Resource | Secondary IDE controller has requested a resource already in use. |
| Serial Port 1 Resource Conflict | Serial port 1 requested a resource already in use. |
| Serial Port 2 Resource Conflict | Serial port 2 requested a resource already in use. |
| Slave DMA Controller Error | Error exists in slave DMA controller. |
| Slave Interrupt Controller Error | Slave interrupt controller failure. |
| Static Device Resource Conflict | A non-PnP ISA card has requested a resource already in use. |
| System Board Device Resource Conflict | A non-PnP ISA card has requested a resource already in use. |
| System Memory Size Mismatch | Amount of memory detected on system board is different from amount indicated in CMOS. |

NOTE:
PCI and PnP messages are displayed with bus, device, and function information.

## A.5 PROCESSOR ERROR MESSAGES (1xx-xx)

**Table A-4.**
System Error Messages

| Message | Probable Cause | Message | Probable Cause |
|---|---|---|---|
| 101 | Option ROM error | 110-01 | Programmable timer load data test failed |
| 102 | System board failure (see note) | 110-02 | Programmable timer dynamic test failed |
| 103 | System board failure | 110-03 | Program timer 2 load data test failed |
| 104-01 | Master int. cntlr. test fialed | 111-01 | Refresh detect test failed |
| 104-02 | Slave int. cntlr. test failed | 112-01 | Speed test Slow mode out of range |
| 104-03 | Int. cntlr. SW RTC inoperative | 112-02 | Speed test Mixed mode out of range |
| 105-01 | Port 61 bit <6> not at zero | 112-03 | Speed test Fast mode out of range |
| 105-02 | Port 61 bit <5> not at zero | 112-04 | Speed test unable to enter Slow mode |
| 105-03 | Port 61 bit <3> not at zero | 112-05 | Speed test unable to enter Mixed mode |
| 105-04 | Port 61 bit <1> not at zero | 112-06 | Speed test unable to enter Fast mode |
| 105-05 | Port 61 bit <0> not at zero | 112-07 | Speed test system error |
| 105-06 | Port 61 bit <5> not at one | 112-08 | Unable to enter Auto mode in speed test |
| 105-07 | Port 61 bit <3> not at one | 112-09 | Unable to enter High mode in speed test |
| 105-08 | Port 61 bit <1> not at one | 112-10 | Speed test High mode out of range |
| 105-09 | Port 61 bit <0> not at one | 112-11 | Speed test Auto mode out of range |
| 105-10 | Port 61 I/O test failed | 112-12 | Speed test variable speed mode inop. |
| 105-11 | Port 61 bit <7> not at zero | 113-01 | Protected mode test failed |
| 105-12 | Port 61 bit <2> not at zero | 114-01 | Speaker test failed |
| 105-13 | No int. generated by failsafe timer | 116-xx | Way 0 read/write test failed |
| 105-14 | NMI not triggered by failsafe timer | 162-xx | Sys. options failed (mismatch in drive type) |
| 106-01 | Keyboard controller test failed | 163-xx | Time and date not set |
| 107-01 | CMOS RAM test failed | 164-xx | Memory size |
| 108-02 | CMOS interrupt test failed | 199-00 | Installed devices test failed |
| 108-03 | CMOS not properly initialized (int.test) | | |
| 109-01 | CMOS clock load data test failed | | |
| 109-02 | CMOS clock rollover test failed | | |
| 109-03 | CMOS not properly initialized (clk test) | | |

**NOTE:** A 102 message code may be caused by one of a variety of processor-related problems that may be solved by replacing the processor, although system board replacement may be needed.

## A.6 MEMORY ERROR MESSAGES (2xx-xx)

**Table A-5.**
Memory Error Messages

| Message | Probable Cause |
|---|---|
| 200-04 | Real memory size changed |
| 200-05 | Extended memory size changed |
| 200-06 | Invalid memory configuration |
| 200-07 | Extended memory size changed |
| 200-08 | CLIM memory size changed |
| 201-01 | Memory machine ID test failed |
| 202-01 | Memory system ROM checksum failed |
| 202-02 | Failed RAM/ROM map test |
| 202-03 | Failed RAM/ROM protect test |
| 203-01 | Memory read/write test failed |
| 203-02 | Error while saving block in read/write test |
| 203-03 | Error while restoring block in read/write test |
| 204-01 | Memory address test failed |
| 204-02 | Error while saving block in address test |
| 204-03 | Error while restoring block in address test |
| 204-04 | A20 address test failed |
| 204-05 | Page hit address test failed |
| 205-01 | Walking I/O test failed |
| 205-02 | Error while saving block in walking I/O test |
| 205-03 | Error while restoring block in walking I/O test |
| 206-xx | Increment pattern test failed |
| 207-xx | ECC failure |
| 210-01 | Memory increment pattern test |
| 210-02 | Error while saving memory during increment pattern test |
| 210-03 | Error while restoring memory during increment pattern test |
| 211-01 | Memory random pattern test |
| 211-02 | Error while saving memory during random memory pattern test |
| 211-03 | Error while restoring memory during random memory pattern test |
| 213-xx | Incompatible DIMM in slot x |
| 214-xx | Noise test failed |
| 215-xx | Random address test |

## A.7 KEYBOARD ERROR MESSAGES (30x-xx)

**Table A-6.**
Keyboard Error Messages

| Message | Probable Cause | Message | Probable Cause |
|---|---|---|---|
| 300-xx | Failed ID test | 303-05 | LED test, LED command test failed |
| 301-01 | Kybd short test, 8042 self-test failed | 303-06 | LED test, LED command test failed |
| 301-02 | Kybd short test, interface test failed | 303-07 | LED test, LED command test failed |
| 301-03 | Kybd short test, echo test failed | 303-08 | LED test, command byte restore test failed |
| 301-04 | Kybd short test, kybd reset failed | 303-09 | LED test, LEDs failed to light |
| 301-05 | Kybd short test, kybd reset failed | 304-01 | Keyboard repeat key test failed |
| 302-xx | Failed individual key test | 304-02 | Unable to enter mode 3 |
| 302-01 | Kybd long test failed | 304-03 | Incorrect scan code from keyboard |
| 303-01 | LED test, 8042 self-test failed | 304-04 | No Make code observed |
| 303-02 | LED test, reset test failed | 304-05 | Cannot /disable repeat key feature |
| 303-03 | LED test, reset failed | 304-06 | Unable to return to Normal mode |
| 303-04 | LED test, LED command test failed | -- | -- |

## A.8 PRINTER ERROR MESSAGES (4xx-xx)

**Table A-7.**
Printer Error Messages

| Message | Probable Cause | Message | Probable Cause |
|---|---|---|---|
| 401-01 | Printer failed or not connected | 402-11 | Interrupt test, data/cntrl. reg. failed |
| 402-01 | Printer data register failed | 402-12 | Interrupt test and loopback test failed |
| 402-02 | Printer control register failed | 402-13 | Int. test, LpBk. test., and data register failed |
| 402-03 | Data and control registers failed | 402-14 | Int. test, LpBk. test., and cntrl. register failed |
| 402-04 | Loopback test failed | 402-15 | Int. test, LpBk. test., and data/cntrl. reg. failed |
| 402-05 | Loopback test and data reg. failed | 402-16 | Unexpected interrupt received |
| 402-06 | Loopback test and cntrl. reg. failed | 402-01 | Printer pattern test failed |
| 402-07 | Loopback tst, data/cntrl. reg. failed | 403-xx | Printer pattern test failed |
| 402-08 | Interrupt test failed | 404-xx | Parallel port address conflict |
| 402-09 | Interrupt test and data reg. failed | 498-00 | Printer failed or not connected |
| 402-10 | Interrupt test and control reg. failed | -- | -- |

## A.9 VIDEO (GRAPHICS) ERROR MESSAGES (5xx-xx)

**Table A-8.**
Video (Graphics) Error Messages

| Message | Probable Cause | Message | Probable Cause |
|---|---|---|---|
| 501-01 | Video controller test failed | 508-01 | 320x200 mode, color set 0 test failed |
| 502-01 | Video memory test failed | 509-01 | 320x200 mode, color set 1 test failed |
| 503-01 | Video attribute test failed | 510-01 | 640x200 mode test failed |
| 504-01 | Video character set test failed | 511-01 | Screen memory page test failed |
| 505-01 | 80x25 mode, 9x14 cell test failed | 512-01 | Gray scale test failed |
| 506-01 | 80x25 mode, 8x8 cell test failed | 514-01 | White screen test failed |
| 507-01 | 40x25 mode test failed | 516-01 | Noise pattern test failed |

See Table A-14 for additional graphics messages.

## A.10 DISKETTE DRIVE ERROR MESSAGES (6xx-xx)

**Table A-9.**
Diskette Drive Error Messages

| Message | Probable Cause | Message | Probable Cause |
|---|---|---|---|
| 6xx-01 | Exceeded maximum soft error limit | 6xx-20 | Failed to get drive type |
| 6xx-02 | Exceeded maximum hard error limit | 6xx-21 | Failed to get change line status |
| 6xx-03 | Previously exceeded max soft limit | 6xx-22 | Failed to clear change line status |
| 6xx-04 | Previously exceeded max hard limit | 6xx-23 | Failed to set drive type in ID media |
| 6xx-05 | Failed to reset controller | 6xx-24 | Failed to read diskette media |
| 6xx-06 | Fatal error while reading | 6xx-25 | Failed to verify diskette media |
| 6xx-07 | Fatal error while writing | 6xx-26 | Failed to read media in speed test |
| 6xx-08 | Failed compare of R/W buffers | 6xx-27 | Failed speed limits |
| 6xx-09 | Failed to format a tract | 6xx-28 | Failed write-protect test |
| 6xx-10 | Failed sector wrap test | -- | -- |

600-xx = Diskette drive ID test
601-xx = Diskette drive format
602-xx = Diskette read test
603-xx = Diskette drive R/W compare test
604-xx = Diskette drive random seek test
605-xx = Diskette drive ID media
606-xx = Diskette drive speed test
607-xx = Diskette drive wrap test
608-xx = Diskette drive write-protect test
609-xx = Diskette drive reset controller test
610-xx = Diskette drive change line test
611-xx = Pri. diskette drive port addr. conflict
612-xx = Sec. diskette drive port addr. conflict
694-00 = Pin 34 not cut on 360-KB drive
697-00 = Diskette type error
698-00 = Drive speed not within limits
699-00 = Drive/media ID error (run Setup)

## A.11 SERIAL INTERFACE ERROR MESSAGES (11xx-xx)

**Table A-10.**
Serial Interface Error Messages

| Message | Probable Cause | Message | Probable Cause |
|---|---|---|---|
| 1101-01 | UART DLAB bit failure | 1101-13 | UART cntrl. signal interrupt failure |
| 1101-02 | Line input or UART fault | 1101-14 | DRVR/RCVR data failure |
| 1101-03 | Address line fault | 1109-01 | Clock register initialization failure |
| 1101-04 | Data line fault | 1109-02 | Clock register rollover failure |
| 1101-05 | UART cntrl. signal failure | 1109-03 | Clock reset failure |
| 1101-06 | UART THRE bit failure | 1109-04 | Input line or clock failure |
| 1101-07 | UART Data RDY bit failure | 1109-05 | Address line fault |
| 1101-08 | UART TX/RX buffer failure | 1109-06 | Data line fault |
| 1101-09 | Interrupt circuit failure | 1150-xx | Comm port setup error (run Setup) |
| 1101-10 | COM1 set to invalid INT | 1151-xx | COM1 address conflict |
| 1101-11 | COM2 set to invalid INT | 1152-xx | COM2 address conflict |
| 1101-12 | DRVR/RCVR cntrl. signal failure | 1155-xx | COM port address conflict |

## A.12 MODEM COMMUNICATIONS ERROR MESSAGES (12xx-xx)

**Table A-11.**
Serial Interface Error Messages

| Message | Probable Cause | Message | Probable Cause |
|---|---|---|---|
| 1201-XX | Modem internal loopback test | 1204-03 | Data block retry limit reached [4] |
| 1201-01 | UART DLAB bit failure | 1204-04 | RX exceeded carrier lost limit |
| 1201-02 | Line input or UART failure | 1204-05 | TX exceeded carrier lost limit |
| 1201-03 | Address line failure | 1204-06 | Time-out waiting for dial tone |
| 1201-04 | Data line fault | 1204-07 | Dial number string too long |
| 1201-05 | UART control signal failure | 1204-08 | Modem time-out waiting for remote response |
| 1201-06 | UART THRE bit failure | 1204-09 | Modem exceeded maximum redial limit |
| 1201-07 | UART DATA READY bit failure | 1204-10 | Line quality prevented remote response |
| 1201-08 | UART TX/RX buffer failure | 1204-11 | Modem time-out waiting for remote connection |
| 1201-09 | Interrupt circuit failure | 1205-XX | Modem auto answer test |
| 1201-10 | COM1 set to invalid inturrupt | 1205-01 | Time-out waiting for SYNC [5] |
| 1201-11 | COM2 set to invalid | 1205-02 | Time-out waiting for response [5] |
| 1201-12 | DRVR/RCVR control signal failure | 1205-03 | Data block retry limit reached [5] |
| 1201-13 | UART control signal interrupt failure | 1205-04 | RX exceeded carrier lost limit |
| 1201-14 | DRVR/RCVR data failure | 1205-05 | TX exceeded carrier lost limit |
| 1201-15 | Modem detection failure | 1205-06 | Time-out waiting for dial tone |
| 1201-16 | Modem ROM, checksum failure | 1205-07 | Dial number string too long |
| 1201-17 | Tone detect failure | 1205-08 | Modem time-out waiting for remote response |
| 1202-XX | Modem internal test | 1205-09 | Modem exceeded maximum redial limit |
| 1202-01 | Time-out waiting for SYNC [1] | 1205-10 | Line quality prevented remote response |
| 1202-02 | Time-out waiting for response [1] | 1205-11 | Modem time-out waiting for remote connection |
| 1202-03 | Data block retry limit reached [1] | 1206-XX | Dial multi-frequency tone test |
| 1202-11 | Time-out waiting for SYNC [2] | 1206-17 | Tone detection failure |
| 1202-12 | Time-out waiting for response [2] | 1210-XX | Modem direct connect test |
| 1202-13 | Data block retry limit reached [2] | 1210-01 | Time-out waiting for SYNC [6] |
| 1202-21 | Time-out waiting for SYNC [3] | 1210-02 | Time-out waiting for response [6] |
| 1202-22 | Time-out waiting for response [3] | 1210-03 | Data block retry limit reached [6] |
| 1202-23 | Data block retry limit reached [3] | 1210-04 | RX exceeded carrier lost limit |
| 1203-XX | Modem external termination test | 1210-05 | TX exceeded carrier lost limit |
| 1203-01 | Modem external TIP/RING failure | 1210-06 | Time-out waiting for dial tone |
| 1203-02 | Modem external data TIP/RING fail | 1210-07 | Dial number string too long |
| 1203-03 | Modem line termination failure | 1210-08 | Modem time-out waiting for remote response |
| 1204-XX | Modem auto originate test | 1210-09 | Modem exceeded maximum redial limit |
| 1204-01 | Time-out waiting for SYNC [4] | 1210-10 | Line quality prevented remote response |
| 1204-02 | Time-out waiting for response [4] | 1210-11 | Modem time-out waiting for remote connection |

NOTES:

[1] Local loopback mode
[2] Analog loopback originate mode
[3] Analog loopback answer mode
[4] Modem auto originate test
[5] Modem auto answer test
[6] Modem direct connect test

## A.13 SYSTEM STATUS ERROR MESSAGES (16xx-xx)

**Table A-12.**
System Status Error Messages

| Message | Probable Cause |
|---|---|
| 1601-xx | Temperature violation |
| 1611-xx | Fan failure |

See Table A-18 for additional messages.

## A.14 HARD DRIVE ERROR MESSAGES (17xx-xx)

**Table A-13.**
Hard Drive Error Messages

| Message | Probable Cause | Message | Probable Cause |
|---|---|---|---|
| 17xx-01 | Exceeded max. soft error limit | 17xx-51 | Failed I/O read test |
| 17xx-02 | Exceeded max. Hard error limit | 17xx-52 | Failed file I/O compare test |
| 17xx-03 | Previously exceeded max. soft error limit | 17xx-53 | Failed drive/head register test |
| 17xx-04 | Previously exceeded max.hard error limit | 17xx-54 | Failed digital input register test |
| 17xx-05 | Failed to reset controller | 17xx-55 | Cylinder 1 error |
| 17xx-06 | Fatal error while reading | 17xx-56 | Failed controller RAM diagnostics |
| 17xx-07 | Fatal error while writing | 17xx-57 | Failed controller-to-drive diagnostics |
| 17xx-08 | Failed compare of R/W buffers | 17xx-58 | Failed to write sector buffer |
| 17xx-09 | Failed to format a track | 17xx-59 | Failed to read sector buffer |
| 17xx-10 | Failed diskette sector wrap during read | 17xx-60 | Failed uncorrectable ECC error |
| 17xx-19 | Cntlr. failed to deallocate bad sectors | 17xx-62 | Failed correctable ECC error |
| 17xx-40 | Cylinder 0 error | 17xx-63 | Failed soft error rate |
| 17xx-41 | Drive not ready | 17xx-65 | Exceeded max. bad sectors per track |
| 17xx-42 | Failed to recalibrate drive | 17xx-66 | Failed to initialize drive parameter |
| 17xx-43 | Failed to format a bad track | 17xx-67 | Failed to write long |
| 17xx-44 | Failed controller diagnostics | 17xx-68 | Failed to read long |
| 17xx-45 | Failed to get drive parameters from ROM | 17xx-69 | Failed to read drive size |
| 17xx-46 | Invalid drive parameters from ROM | 17xx-70 | Failed translate mode |
| 17xx-47 | Failed to park heads | 17xx-71 | Failed non-translate mode |
| 17xx-48 | Failed to move hard drive table to RAM | 17xx-72 | Bad track limit exceeded |
| 17xx-49 | Failed to read media in file write test | 17xx-73 | Previously exceeded bad track limit |
| 17xx-50 | Failed I/O write test | -- | -- |

1700-xx = Hard drive ID test
1701-xx = Hard drive format test
1702-xx = Hard drive read test
1703-xx = Hard drive read/write compare test
1704-xx = Hard drive random seek test
1705-xx = Hard drive controller test
1706-xx = Hard drive ready test
1707-xx = Hard drive recalibrate test
1708-xx = Hard drive format bad track test
1709-xx = Hard drive reset controller test
1710-xx = Hard drive park head test
1714-xx = Hard drive file write test
1715-xx = Hard drive head select test
1716-xx = Hard drive conditional format test
1717-xx = Hard drive ECC test
1719-xx = Hard drive power mode test
1720-xx = SMART drive detects imminent failure
1721-xx = SCSI hard drive imminent failure
1724-xx = Net work preparation test
1736-xx = Drive monitoring test
1771-xx = Pri. IDE controller address conflict
1772-xx = Sec. IDE controller address conflict
1780-xx = Disk 0 failure
1781-xx = Disk 1 failure
1782-xx = Pri. IDE controller failure
1790-xx = Disk 0 failure
1791-xx = Disk 1 failure
1792-xx = Se. controller failure
1793-xx = Sec. Controller or disk failure
1799-xx = Invalid hard drive type

## A.15 HARD DRIVE ERROR MESSAGES (19xx-xx)

**Table A-14.**
Hard Drive Error Messages

| Message | Probable Cause | Message | Probable Cause |
|---|---|---|---|
| 19xx-01 | Drive not installed | 19xx-21 | Got servo pulses second time but not first |
| 19xx-02 | Cartridge not installed | 19xx-22 | Never got to EOT after servo check |
| 19xx-03 | Tape motion error | 19xx-23 | Change line unset |
| 19xx-04 | Drive busy erro | 19xx-24 | Write-protect error |
| 19xx-05 | Track seek error | 19xx-25 | Unable to erase cartridge |
| 19xx-06 | Tape write-protect error | 19xx-26 | Cannot identify drive |
| 19xx-07 | Tape already Servo Written | 19xx-27 | Drive not compatible with controller |
| 19xx-08 | Unable to Servo Write | 19xx-28 | Format gap error |
| 19xx-09 | Unable to format | 19xx-30 | Exception bit not set |
| 19xx-10 | Format mode error | 19xx-31 | Unexpected drive status |
| 19xx-11 | Drive recalibration error | 19xx-32 | Device fault |
| 19xx-12 | Tape not Servo Written | 19xx-33 | Illegal command |
| 19xx-13 | Tape not formatted | 19xx-34 | No data detected |
| 19xx-14 | Drive time-out error | 19xx-35 | Power-on reset occurred |
| 19xx-15 | Sensor error flag | 19xx-36 | Failed to set FLEX format mode |
| 19xx-16 | Block locate (block ID) error | 19xx-37 | Failed to reset FLEX format mode |
| 19xx-17 | Soft error limit exceeded | 19xx-38 | Data mismatch on directory track |
| 19xx-18 | Hard error limit exceeded | 19xx-39 | Data mismatch on track 0 |
| 19xx-19 | Write (probably ID ) error | 19xx-40 | Failed self-test |
| 19xx-20 | NEC fatal error | 19xx-91 | Power lost during test |

1900-xx = Tape ID test failed
1901-xx = Tape servo write failed
1902-xx = Tape format failed
1903-xx = Tape drive sensor test failed
1904-xx = Tape BOT/EOT test failed
1905-xx = Tape read test failed
1906-xx = Tape R/W compare test failed
1907-xx = Tape write-protect failed

## A.16 VIDEO (GRAPHICS) ERROR MESSAGES (24xx-xx)

**Table A-15.**
Video (Graphics) Error Messages

| Message | Probable Cause | Message | Probable Cause |
|---|---|---|---|
| 2402-01 | Video memory test failed | 2418-02 | EGA shadow RAM test failed |
| 2403-01 | Video attribute test failed | 2419-01 | EGA ROM checksum test failed |
| 2404-01 | Video character set test failed | 2420-01 | EGA attribute test failed |
| 2405-01 | 80x25 mode, 9x14 cell test failed | 2421-01 | 640x200 mode test failed |
| 2406-01 | 80x25 mode, 8x8 cell test failed | 2422-01 | 640x350 16-color set test failed |
| 2407-01 | 40x25 mode test failed | 2423-01 | 640x350 64-color set test failed |
| 2408-01 | 320x200 mode color set 0 test failed | 2424-01 | EGA Mono. text mode test failed |
| 2409-01 | 320x200 mode color set 1 test failed | 2425-01 | EGA Mono. graphics mode test failed |
| 2410-01 | 640x200 mode test failed | 2431-01 | 640x480 graphics mode test failed |
| 2411-01 | Screen memory page test failed | 2432-01 | 320x200 256-color set test failed |
| 2412-01 | Gray scale test failed | 2448-01 | Advanced VGA controller test failed |
| 2414-01 | White screen test failed | 2451-01 | 132-column AVGA test failed |
| 2416-01 | Noise pattern test failed | 2456-01 | AVGA 256-color test failed |
| 2417-01 | Lightpen text test failed, no response | 2458-xx | AVGA BitBLT test failed |
| 2417-02 | Lightpen text test failed, invalid response | 2468-xx | AVGA DAC test failed |
| 2417-03 | Lightpen graphics test failed, no resp. | 2477-xx | AVGA data path test failed |
| 2417-04 | Lightpen graphics test failed, invalid resp. | 2478-xx | AVGA BitBLT test failed |
| 2418-01 | EGA memory test failed | 2480-xx | AVGA linedraw test failed |

## A.17 AUDIO ERROR MESSAGES (3206-xx)

**Table A-16.**
Audio Error Message

| Message | Probable Cause |
|---|---|
| 3206-xx | Audio subsystem internal error |

## A.18 DVD/CD-ROM ERROR MESSAGES (33xx-xx)

**Table A-17.**
DVD/CD-ROM Drive Error Messages

| Message | Probable Cause |
|---|---|
| 3301-xx | Drive test failed |
| 3305-XX | Seek test failed |

See Table A-18 for additional messages.

## A.19 NETWORK INTERFACE ERROR MESSAGES (60xx-xx)

**Table A-18.**
Network Interface Error Messages

| Message | Probable Cause | Message | Probable Cause |
|---|---|---|---|
| 6000-xx | Pointing device interface error | 6054-xx | Token ring configuration test failed |
| 6014-xx | Ethernet configuration test failed | 6056-xx | Token ring reset test failed |
| 6016-xx | Ethernet reset test failed | 6068-xx | Token ring int. loopback test failed |
| 6028-xx | Ethernet int. loopback test failed | 6069-xx | Token ring ext. loopback test failed |
| 6029-xx | Ethernet ext. loopback test failed | 6089-xx | Token ring open |

## A.20 SCSI INTERFACE ERROR MESSAGES (65xx-xx, 66xx-xx, 67xx-xx)

**Table A-19.**
SCSI Interface Error Messages

| Message | Probable Cause | Message | Probable Cause |
|---|---|---|---|
| 6nyy-02 | Drive not installed | 6nyy-33 | Illegal controller command |
| 6nyy-03 | Media not installed | 6nyy-34 | Invalid SCSI bus phase |
| 6nyy-05 | Seek failure | 6nyy-35 | Invalid SCSI bus phase |
| 6nyy-06 | Drive timed out | 6nyy-36 | Invalid SCSI bus phase |
| 6nyy-07 | Drive busy | 6nyy-39 | Error status from drive |
| 6nyy-08 | Drive already reserved | 6nyy-40 | Drive timed out |
| 6nyy-09 | Reserved | 6nyy-41 | SSI bus stayed busy |
| 6nyy-10 | Reserved | 6nyy-42 | ACK/REQ lines bad |
| 6nyy-11 | Media soft error | 6nyy-43 | ACK did not deassert |
| 6nyy-12 | Drive not ready | 6nyy-44 | Parity error |
| 6nyy-13 | Media error | 6nyy-50 | Data pins bad |
| 6nyy-14 | Drive hardware error | 6nyy-51 | Data line 7 bad |
| 6nyy-15 | Illegal drive command | 6nyy-52 | MSG, C/D, or I/O lines bad |
| 6nyy-16 | Media was changed | 6nyy-53 | BSY never went busy |
| 6nyy-17 | Tape write-protected | 6nyy-54 | BSY stayed busy |
| 6nyy-18 | No data detected | 6nyy-60 | Controller CONFIG-1 register fault |
| 6nyy-21 | Drive command aborted | 6nyy-61 | Controller CONFIG-2 register fault |
| 6nyy-24 | Media hard error | 6nyy-65 | Media not unloaded |
| 6nyy-25 | Reserved | 6nyy-90 | Fan failure |
| 6nyy-30 | Controller timed out | 6nyy-91 | Over temperature condition |
| 6nyy-31 | Unrecoverable error | 6nyy-92 | Side panel not installed |
| 6nyy-32 | Controller/drive not connected | 6nyy-99 | Autoloader reported tape not loaded properly |

n = 5, Hard drive
= 6, CD-ROM drive
= 7, Tape drive.

yy = 00, ID
= 03, Power check
= 05, Read
= 06, SA/Media
= 08, Controller
= 23, Random read
= 28, Media load/unload

## A.21 POINTING DEVICE INTERFACE ERROR MESSAGES (8601-xx)

**Table A-20.**
Pointing Device Interface Error Messages

| Message | Probable Cause | Message | Probable Cause |
|---|---|---|---|
| 8601-01 | Mouse ID fails | 8601-07 | Right block not selected |
| 8601-02 | Left mouse button is inoperative | 8601-08 | Timeout occurred |
| 8601-03 | Left mouse button is stuck closed | 8601-09 | Mouse loopback test failed |
| 8601-04 | Right mouse button is inoperative | 8601-10 | Pointing device is inoperative |
| 8601-05 | Right mouse button is stuck closed | 8602-xx | I/F test failed |
| 8601-06 | Left block not selected | -- | -- |

## A.22 CEMM PRIVILEDGED OPS ERROR MESSAGES

**Table A-21.**
CEMM Privileged Ops Error Messages

| Message | Probable Cause | Message | Probable Cause |
|---|---|---|---|
| 00 | LGDT instruction | 04 | LL3 instruction |
| 01 | LIDT instruction | 05 | MOV CRx instruction |
| 02 | LMSW instruction | 06 | MOV DRx instruction |
| 03 | LL2 instruction | 07 | MOV TRx instruction |

## A.23 CEMM EXCEPTION ERROR MESSAGES

**Table A-22.**
CEMM Exception Error Messages

| Message | Probable Cause | Message | Probable Cause |
|---|---|---|---|
| 00 | Divide | 10 | Invalid TSS |
| 01 | Debug | 11 | Segment not present |
| 02 | NMI or parity | 12 | Stack full |
| 03 | INT 0 (arithmetic overflow) | 13 | General protection fault |
| 04 | INT 3 | 14 | Page fault |
| 05 | Array bounds check | 16 | Coprocessor |
| 06 | Invalid opcode | 32 | Attempt to write to protected area |
| 07 | Coprocessor device not available | 33 | Reserved |
| 08 | Double fault | 34 | Invalid software interrupt |
| 09 | Coprocessor segment overrun | -- | -- |

# Appendix B
# ASCII CHARACTER SET

## B.1 INTRODUCTION

This appendix lists, in Table B-1, the 256-character ASCII code set including the decimal and hexadecimal values. All ASCII symbols may be called while in DOS or using standard text-mode editors by using the combination keystroke of holding the **Alt** key and using the Numeric Keypad to enter the decimal value of the symbol. The extended ASCII characters (decimals 128-255) can only be called using the **Alt** + Numeric Keypad keys.

**NOTE:** Regarding keystrokes, refer to notes at the end of the table. Applications may interpret multiple keystroke accesses differently or ignore them completely.

**Table B-1.**
ASCII Character Set

| Dec | Hex | Symbol | Dec | Hex | Symbol | Dec | Hex | Symbol | Dec | Hex | Symbol |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 00 | Blank | 32 | 20 | Space | 64 | 40 | @ | 96 | 60 | ‘ |
| 1 | 01 | ☺ | 33 | 21 | ! | 65 | 41 | A | 97 | 61 | a |
| 2 | 02 | ☻ | 34 | 22 | “ | 66 | 42 | B | 98 | 62 | b |
| 3 | 03 | ♥ | 35 | 23 | # | 67 | 43 | C | 99 | 63 | c |
| 4 | 04 | ♦ | 36 | 24 | $ | 68 | 44 | D | 100 | 64 | d |
| 5 | 05 | ♣ | 37 | 25 | % | 69 | 45 | E | 101 | 65 | e |
| 6 | 06 | ♠ | 38 | 26 | & | 70 | 46 | F | 102 | 66 | f |
| 7 | 07 | • | 39 | 27 | ‘ | 71 | 47 | G | 103 | 67 | g |
| 8 | 08 | ◘ | 40 | 28 | ( | 72 | 48 | H | 104 | 68 | h |
| 9 | 09 | ○ | 41 | 29 | ) | 73 | 49 | I | 105 | 69 | I |
| 10 | 0A | ◙ | 42 | 2A | * | 74 | 4A | J | 106 | 6A | j |
| 11 | 0B | ♂ | 43 | 2B | + | 75 | 4B | K | 107 | 6B | k |
| 12 | 0C | ♀ | 44 | 2C | ` | 76 | 4C | L | 108 | 6C | l |
| 13 | 0D | ♪ | 45 | 2D | - | 77 | 4D | M | 109 | 6D | m |
| 14 | 0E | ♫ | 46 | 2E | . | 78 | 4E | N | 110 | 6E | n |
| 15 | 0F | ☼ | 47 | 2F | / | 79 | 4F | O | 111 | 6F | o |
| 16 | 10 | ► | 48 | 30 | 0 | 80 | 50 | P | 112 | 70 | p |
| 17 | 11 | ◄ | 49 | 31 | 1 | 81 | 51 | Q | 113 | 71 | q |
| 18 | 12 | ↕ | 50 | 32 | 2 | 82 | 52 | R | 114 | 72 | r |
| 19 | 13 | ‼ | 51 | 33 | 3 | 83 | 53 | S | 115 | 73 | s |
| 20 | 14 | ¶ | 52 | 34 | 4 | 84 | 54 | T | 116 | 74 | t |
| 21 | 15 | § | 53 | 35 | 5 | 85 | 55 | U | 117 | 75 | u |
| 22 | 16 | ▬ | 54 | 36 | 6 | 86 | 56 | V | 118 | 76 | v |
| 23 | 17 | ↨ | 55 | 37 | 7 | 87 | 57 | W | 119 | 77 | w |
| 24 | 18 | ↑ | 56 | 38 | 8 | 88 | 58 | X | 120 | 78 | x |
| 25 | 19 | ↓ | 57 | 39 | 9 | 89 | 59 | Y | 121 | 79 | y |
| 26 | 1A | → | 58 | 3A | : | 90 | 5A | Z | 122 | 7A | z |
| 27 | 1B | ← | 59 | 3B | ; | 91 | 5B | [ | 123 | 7B | { |
| 28 | 1C | ∟ | 60 | 3C | < | 92 | 5C | \ | 124 | 7C | l |
| 29 | 1D | ↔ | 61 | 3D | = | 93 | 5D | ] | 125 | 7D | } |
| 30 | 1E | ▲ | 62 | 3E | > | 94 | 5E | ^ | 126 | 7E | ~ |
| 31 | 1F | ▼ | 63 | 3F | ? | 95 | 5F | _ | 127 | 7F | △ [1] |

*Continued*

**Table B-1.** ASCII Code Set *(Continued)*

| Dec | Hex | Symbol | Dec | Hex | Symbol | Dec | Hex | Symbol | Dec | Hex | Symbol |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 128 | 80 | Ç | 160 | A0 | á | 192 | C0 | └ | 224 | E0 | α |
| 129 | 81 | ü | 161 | A1 | í | 193 | C1 | ┴ | 225 | E1 | ß |
| 130 | 82 | é | 162 | A2 | ó | 194 | C2 | ┬ | 226 | E2 | Γ |
| 131 | 83 | â | 163 | A3 | ú | 195 | C3 | ├ | 227 | E3 | π |
| 132 | 84 | ä | 164 | A4 | ñ | 196 | C4 | ─ | 228 | E4 | Σ |
| 133 | 85 | à | 165 | A5 | Ñ | 197 | C5 | ┼ | 229 | E5 | σ |
| 134 | 86 | å | 166 | A6 | ª | 198 | C6 | ╞ | 230 | E6 | µ |
| 135 | 87 | ç | 167 | A7 | º | 199 | C7 | ╟ | 231 | E7 | τ |
| 136 | 88 | ê | 168 | A8 | ¿ | 200 | C8 | ╚ | 232 | E8 | Φ |
| 137 | 89 | ë | 169 | A9 | ⌐ | 201 | C9 | ╔ | 233 | E9 | Θ |
| 138 | 8A | è | 170 | AA | ¬ | 202 | CA | ╩ | 234 | EA | Ω |
| 139 | 8B | ï | 171 | AB | ½ | 203 | CB | ╦ | 235 | EB | δ |
| 140 | 8C | î | 172 | AC | ¼ | 204 | CC | ╠ | 236 | EC | ∞ |
| 141 | 8D | ì | 173 | AD | ¡ | 205 | CD | ═ | 237 | ED | φ |
| 142 | 8E | Ä | 174 | AE | « | 206 | CE | ╬ | 238 | EE | ε |
| 143 | 8F | Å | 175 | AF | » | 207 | CF | ╧ | 239 | EF | ∩ |
| 144 | 90 | É | 176 | B0 | ░ | 208 | D0 | ╨ | 240 | F0 | ≡ |
| 145 | 91 | æ | 177 | B1 | ▒ | 209 | D1 | ╤ | 241 | F1 | ± |
| 146 | 92 | Æ | 178 | B2 | ▓ | 210 | D2 | ╥ | 242 | F2 | ≥ |
| 147 | 93 | ô | 179 | B3 | │ | 211 | D3 | ╙ | 243 | F3 | ≤ |
| 148 | 94 | ö | 180 | B4 | ┤ | 212 | D4 | ╘ | 244 | F4 | ⌠ |
| 149 | 95 | ò | 181 | B5 | ╡ | 213 | D5 | ╒ | 245 | F5 | ⌡ |
| 150 | 96 | û | 182 | B6 | ╢ | 214 | D6 | ╓ | 246 | F6 | ÷ |
| 151 | 97 | ù | 183 | B7 | ╖ | 215 | D7 | ╫ | 247 | F7 | ≈ |
| 152 | 98 | ÿ | 184 | B8 | ╕ | 216 | D8 | ╪ | 248 | F8 | ° |
| 153 | 99 | Ö | 185 | B9 | ╣ | 217 | D9 | ┘ | 249 | F9 | ∙ |
| 154 | 9A | Ü | 186 | BA | ║ | 218 | DA | ┌ | 250 | FA | · |
| 155 | 9B | ¢ | 187 | BB | ╗ | 219 | DB | █ | 251 | FB | √ |
| 156 | 9C | £ | 188 | BC | ╝ | 220 | DC | ▄ | 252 | FC | ⁿ |
| 157 | 9D | ¥ | 189 | BD | ╜ | 221 | DD | ▌ | 253 | FD | ² |
| 158 | 9E | ₧ | 190 | BE | ╛ | 222 | DE | ▐ | 254 | FE | ■ |
| 159 | 9F | ƒ | 191 | BF | ┐ | 223 | DF | ▀ | 255 | FF | Blank |

NOTES:

[1] Symbol not displayed.

Keystroke Guide:

| Dec # | Keystroke(s) |
|---|---|
| 0 | Ctrl 2 |
| 1-26 | Ctrl A thru Z respectively |
| 27 | Ctrl [ |
| 28 | Ctrl |
| 29 | Ctrl ] |
| 30 | Ctrl 6 |
| 31 | Ctrl - |
| 32 | Space Bar |
| 33-43 | Shift and key w/corresponding symbol |
| 44-47 | Key w/corresponding symbol |
| 48-57 | Key w/corresponding symbol, numerical keypad w/Num Lock active |
| 58 | Shift and key w/corresponding symbol |
| 59 | Key w/corresponding symbol |
| 60 | Shift and key w/corresponding symbol |
| 61 | Key w/corresponding symbol |
| 62-64 | Shift and key w/corresponding symbol |
| 65-90 | Shift and key w/corresponding symbol or key w/corresponding symbol and Caps Lock active |
| 91-93 | Key w/corresponding symbol |
| 94, 95 | Shift and key w/corresponding symbol |
| 96 | Key w/corresponding symbol |
| 97-126 | Key w/corresponding symbol or Shift and key w/corresponding symbol and Caps Lock active |
| 127 | Ctrl - |
| 128-255 | Alt and decimal digit(s) of desired character |

# Appendix C
# KEYBOARD

## C.1 INTRODUCTION

This appendix describes the Compaq keyboard that is included as standard with the system unit. The keyboard complies with the industry-standard classification of an "enhanced keyboard" and includes a separate cursor control key cluster, twelve "function" keys, and enhanced programmability for additional functions.
This appendix covers the following keyboard types:

- Standard enhanced keyboard.
- Space-Saver Windows-version keyboard featuring additional keys for specific support of the Windows operating system.
- Easy Access keyboard with additional buttons for internet accessibility functions.

Only one type of keyboard is supplied with each system. Other types may be available as an option.

> **NOTE:** This appendix discusses only the keyboard unit. The keyboard interface is a function of the system unit and is discussed in Chapter 5, Input/Output Interfaces.

Topics covered in this appendix include the following:

## C.2 KEYSTROKE PROCESSING

A functional block diagram of the keystroke processing elements is shown in Figure C-1. Power (+5 VDC) is obtained from the system through the PS/2-type interface. The keyboard uses a Z86C14 (or equivalent) microprocessor. The Z86C14 scans the key matrix drivers every 10 ms for pressed keys while at the same time monitoring communications with the keyboard interface of the system unit. When a key is pressed, a Make code is generated. A Break code is generated when the key is released. The Make and Break codes are collectively referred to as scan codes. All keys generate Make and Break codes with the exception of the Pause key, which generates a Make code only.

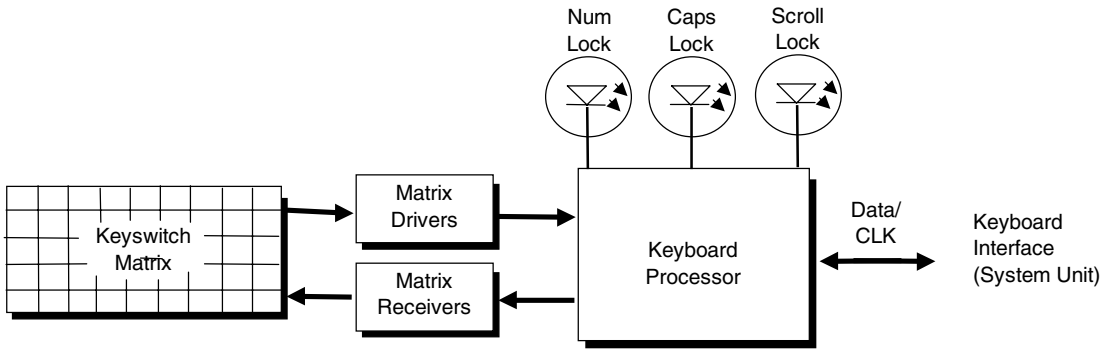



**Figure C–1.** Keystroke Processing Elements, Block Diagram

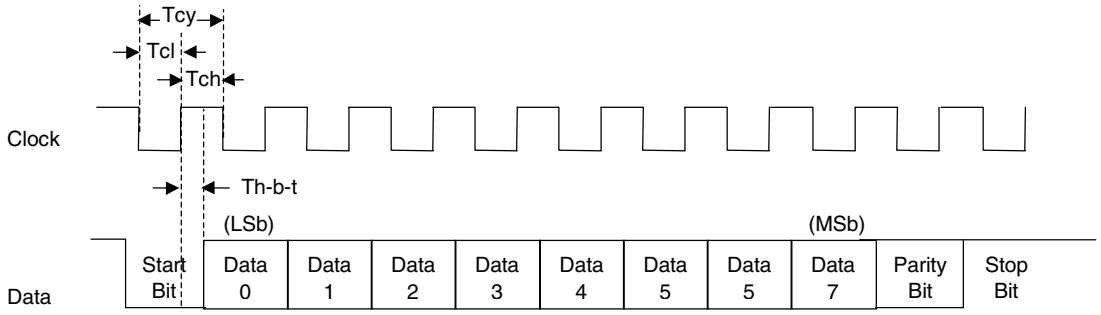
When the system is turned on, the keyboard processor generates a Power-On Reset (POR) signal after a period of 150 ms to 2 seconds. The keyboard undergoes a Basic Assurance Test (BAT) that checks for shorted keys and basic operation of the keyboard processor. The BAT takes from 300 to 500 ms to complete.

If the keyboard fails the BAT, an error code is sent to the CPU and the keyboard is disabled until an input command is received. After successful completion of the POR and BAT, a completion code (AAh) is sent to the CPU and the scanning process begins.

The keyboard processor includes a 16-byte FIFO buffer for holding scan codes until the system is ready to receive them. Response and typematic codes are not buffered. If the buffer is full (16 bytes held) a 17$^{th}$ byte of a successive scan code results in an overrun condition and the overrun code replaces the scan code byte and any additional scan code data (and the respective key strokes) are lost. Multi-byte sequences must fit entirely into the buffer before the respective keystroke can be registered.

## C.2.1 PS/2-TYPE KEYBOARD TRANSMISSIONS

The PS/2-type keyboard sends two main types of data to the system; commands (or responses to system commands) and keystroke scan codes. Before the keyboard sends data to the system (specifically, to the 8042-type logic within the system), the keyboard verifies the clock and data lines to the system. If the clock signal is low (0), the keyboard recognizes the inhibited state and loads the data into a buffer. Once the inhibited state is removed, the data is sent to the system. Keyboard-to-system transfers (in the default mode) consist of 11 bits as shown in Figure C-2.




| Parameter | Minimum | Nominal | Maximum |
|---|---|---|---|
| Tcy (clock cycle) | 60 us | -- | 80 us |
| Tcl (clock low) | 30 us | 41 us | 50 us |
| Tch (clock high) | 30 us | -- | 40 us |
| Th-t-t (high-before-transmit) | -- | 20 us | -- |

**Figure C–2.** PS/2 Keyboard-To-System Transmission, Timing Diagram

The system can halt keyboard transmission by setting the clock signal low. The keyboard checks the clock line every 60 us to verify the state of the signal. If a low is detected, the keyboard will finish the current transmission **if** the rising edge of the clock pulse for the parity bit has not occurred. The system uses the same timing relationships during reads (typically with slightly reduced time periods).

The enhanced keyboard has three operating modes:

- Mode 1 - PC-XT compatible
- Mode 2 - PC-AT compatible (default)
- Mode 3 - Select mode (keys are programmable as to make-only, break-only, typematic)

Modes can be selected by the user or set by the system. Mode 2 is the default mode. Each mode produces a different set of scan codes. When a key is pressed, the keyboard processor sends that key's make code to the 8042 logic of the system unit. The When the key is released, a release code is transmitted as well (except for the Pause key, which produces only a make code). The 8042-type logic of the system unit responds to scan code reception by asserting IRQ1, which is processed by the interrupt logic and serviced by the CPU with an interrupt service routine. The service routine takes the appropriate action based on which key was pressed.

## C.2.2 USB-TYPE KEYBOARD TRANSMISSIONS

The USB-type keyboard sends essentially the same information to the system that the PS/2 keyboard does, except that the data receives additional NRZI encoding and formatting (prior to leaving the keyboard) to comply with the USB I/F specification (discussed in chapter 5 of this guide).

Packets received at the system's USB I/F and decoded as originating from the keyboard result in an SMI being generated. An SMI handler routine is invoked that decodes the data and transfers the information to the 8042 keyboard controller where normal (legacy) keyboard processing takes place.

## C.2.3 KEYBOARD LAYOUTS

Figures C-3 through C-8 show the key layouts for keyboards shipped with Compaq systems. Actual styling details including location of the Compaq logo as well as the numbers lock, caps lock, and scroll lock LEDs may vary.

### C.2.3.1 Standard Enhanced Keyboards

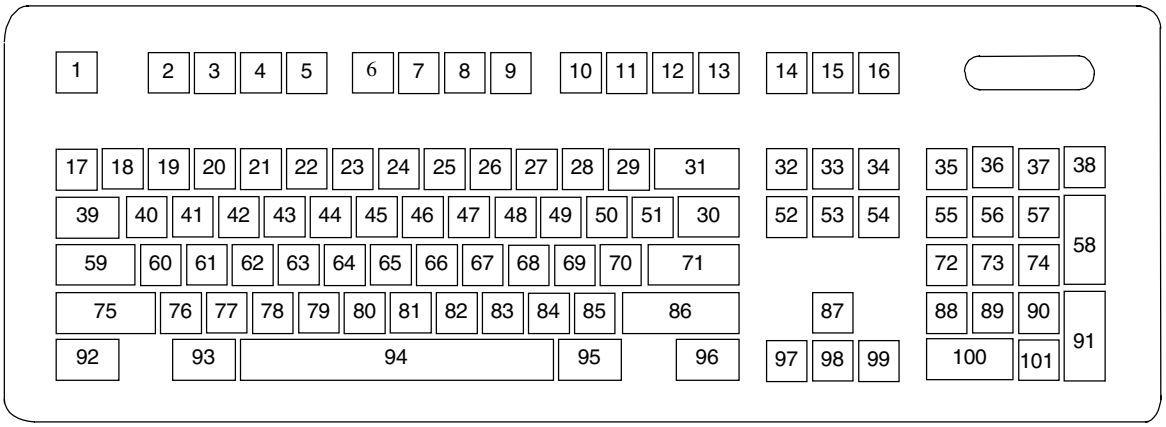



**Figure C–3.** U.S. English (101-Key) Keyboard Key Positions

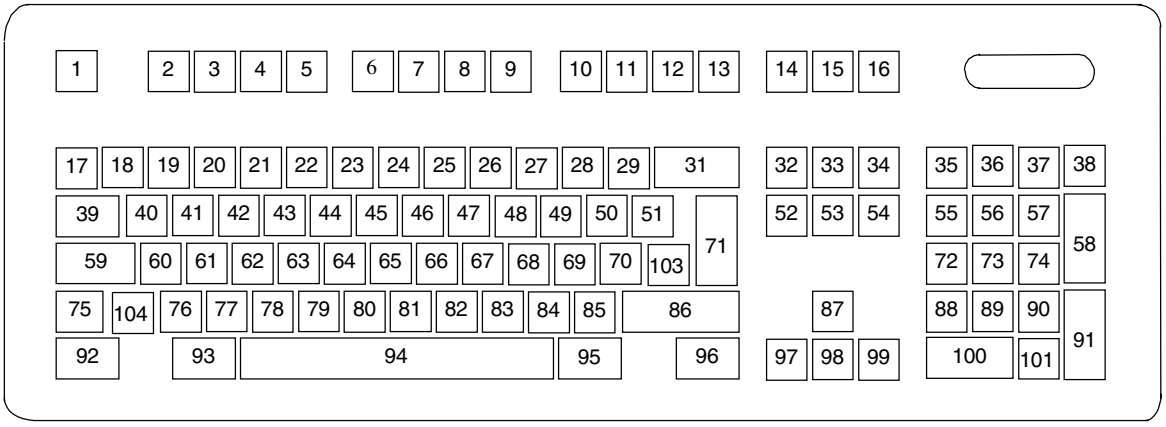



**Figure C–4.** National (102-Key) Keyboard Key Positions

### C.2.3.2 Windows Enhanced Keyboards

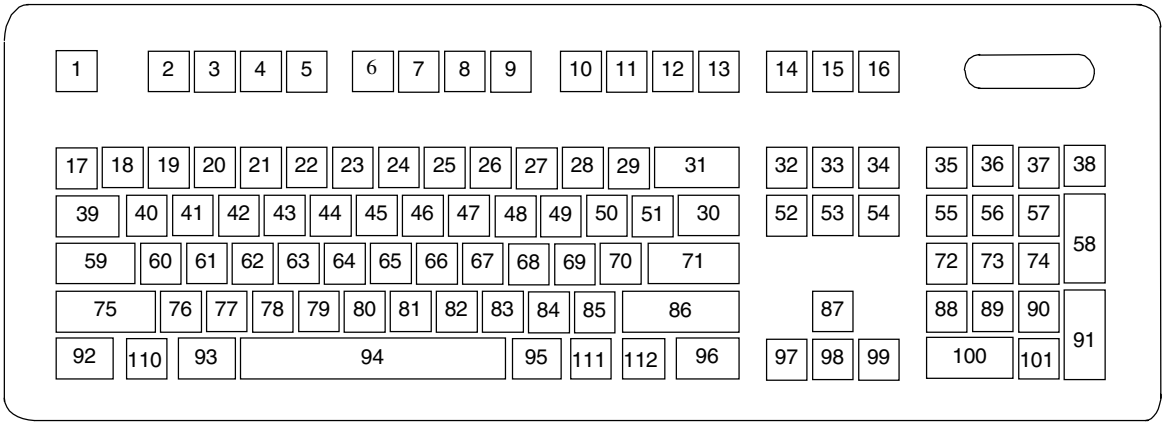



**Figure C–5.** U.S. English Windows (101W-Key) Keyboard Key Positions

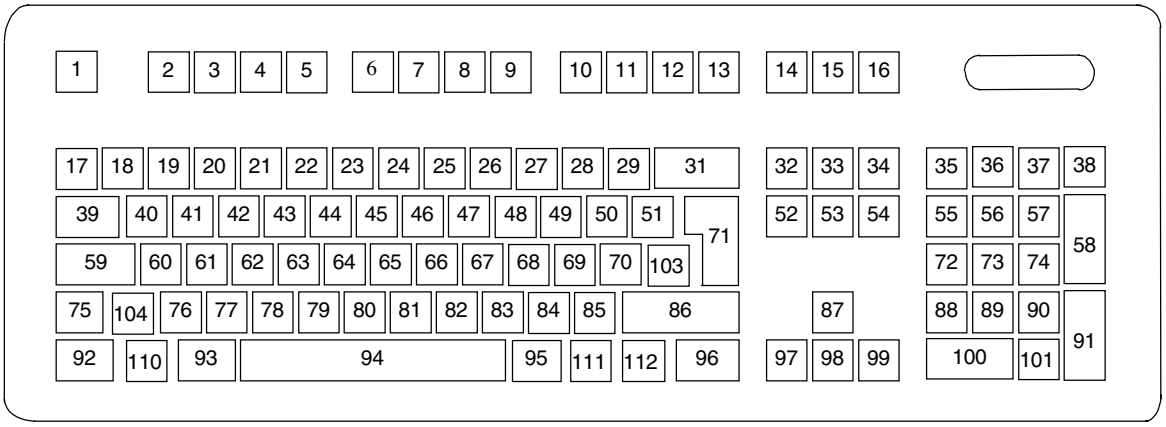
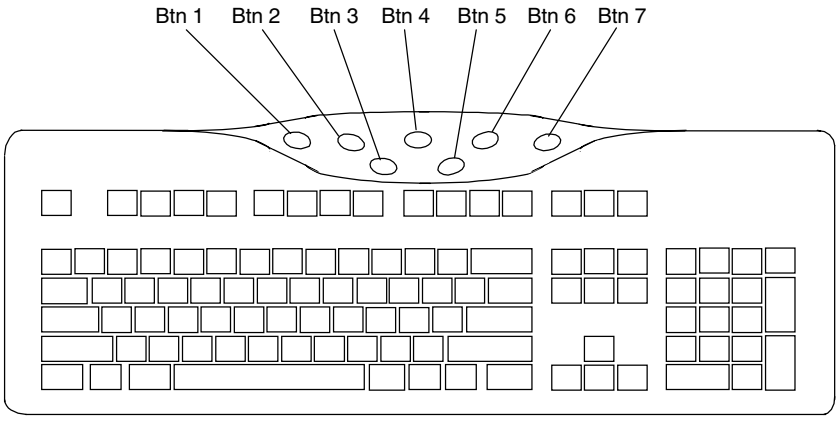



**Figure C–6.** National Windows (102W-Key) Keyboard Key Positions

### C.2.3.3 Easy Access Keyboards

The Easy Access keyboard, such as that shipped with the Compaq iPaq system, is a Windows Enhanced-type keyboard that includes special buttons (Figure C-7) allowing quick internet navigation. Depending on the system, either a legacy PS/2-type keyboard or a Universal Serial Bus (USB) type keyboard may be employed. Either type uses the layout shown in the following figure.




NOTE:
Main key positions same as Windows Enhanced (Figures C-5 or C-6).

**Figure C–7.** Easy Access Key Positions

## C.2.4 KEYS

All keys generate a make code (when pressed) and a break code (when released) with the exception of the **Pause** key (pos. 16), which produces a make code only. All keys with the exception of the **Pause** and Easy Access keys are also typematic, although the typematic action of the **Shift**, **Ctrl**, **Alt**, **Num Lock**, **Scroll Lock**, **Caps Lock**, and **Ins** keys is suppressed by the BIOS. Typematic keys, when held down longer than 500 ms, send the make code repetitively at a 10-12 Hz rate until the key is released. If more than one key is held down, the last key pressed will be typematic.

### C.2.4.1 Special Single-Keystroke Functions

The following keys provide the intended function in most applications and environments.

**Caps Lock** - The **Caps Lock** key (pos. 59), when pressed and released, invokes a BIOS routine that turns on the caps lock LED and shifts into upper case key positions 40-49, 60-68, and 76-82. When pressed and released again, these keys revert to the lower case state and the LED is turned off. Use of the **Shift** key will reverse which state these keys are in based on the **Caps Lock** key.

**Num Lock** - The **Num Lock** key (pos. 32), when pressed and released, invokes a BIOS routine that turns on the num lock LED and shifts into upper case key positions 55-57, 72-74, 88-90, 100, and 101. When pressed and released again, these keys revert to the lower case state and the LED is turned off.

The following keys provide special functions that require specific support by the application.

**Print Scrn** - The **Print Scrn** (pos. 14) key can, when pressed, generate an interrupt that initiates a print routine. This function may be inhibited by the application.

**Scroll Lock** - The **Scroll Lock** key (pos. 15) when pressed and released, , invokes a BIOS routine that turns on the scroll lock LED and inhibits movement of the cursor. When pressed and released again, the LED is turned off and the function is removed. This keystroke is always serviced by the BIOS (as indicated by the LED) but may be inhibited or ignored by the application.

**Pause** - The **Pause** (pos. 16) key, when pressed, can be used to cause the keyboard interrupt to loop, i.e., wait for another key to be pressed. This can be used to momentarily suspend an operation. The key that is pressed to resume operation is discarded. This function may be ignored by the application.

The **Esc**, **Fn** (function), **Insert**, **Home**, **Page Up**/**Down**, **Delete**, and **End** keys operate at the discretion of the application software.

### C.2.4.2 Multi-Keystroke Functions

**Shift** - The **Shift** key (pos. 75/86), when held down, produces a shift state (upper case) for keys in positions 17-29, 30, 39-51, 60-70, and 76-85 as long as the **Caps Lock** key (pos. 59) is toggled off. If the **Caps Lock** key is toggled on, then a held **Shift** key produces the lower (normal) case for the identified pressed keys. The **Shift** key also reverses the **Num Lock** state of key positions 55-57, 72, 74, 88-90, 100, and 101.

**Ctrl** - The **Ctrl** keys (pos. 92/96) can be used in conjunction with keys in positions 1-13, 16, 17-34, 39-54, 60-71, and 76-84. The application determines the actual function. Both **Ctrl** key positions provide identical functionality. The pressed combination of **Ctrl** and **Break** (pos. 16) results in the generation of BIOS function INT 1Bh. This software interrupt provides a method of exiting an application and generally halts execution of the current program.

**Alt** - The **Alt** keys (pos. 93/95) can be used in conjunction with the same keys available for use with the **Ctrl** keys with the exception that position 14 (**SysRq**) is available instead of position 16 (**Break**). The **Alt** key can also be used in conjunction with the numeric keypad keys (pos. 55-57, 72-74, and 88-90) to enter the decimal value of an ASCII character code from 1-255. The application determines the actual function of the keystrokes. Both **Alt** key positions provide identical functionality. The combination keystroke of **Alt** and **SysRq** results in software interrupt 15h, AX=8500h being executed. It is up to the application to use or not use this BIOS function.

The **Ctrl** and **Alt** keys can be used together in conjunction with keys in positions 1-13, 17-34, 39-54, 60-71, and 76-84. The **Ctrl** and **Alt** key positions used and the sequence in which they are pressed make no difference as long as they are held down at the time the third key is pressed. The **Ctrl**, **Alt,** and **Delete** keystroke combination (required twice if in the Windows environment) initiates a system reset (warm boot) that is handled by the BIOS.

### C.2.4.3 Windows Keystrokes

Windows-enhanced keyboards include three additional key positions. Key positions 110 and 111 (marked with the Windows logo  ) have the same functionality and are used by themselves or in combination with other keys to perform specific "hot-key" type functions for the Windows operating system. The defined functions of the Windows logo keys are listed as follows:

| Keystroke | Function |
|---|---|
| Window Logo | Open Start menu |
| Window Logo + F1 | Display pop-up menu for the selected object |
| Window Logo + TAB | Activate next task bar button |
| Window Logo + E | Explore my computer |
| Window Logo + F | Find document |
| Window Logo + CTRL + F | Find computer |
| Window Logo + M | Minimize all |
| Shift + Window Logo + M | Undo minimize all |
| Window Logo + R | Display Run dialog box |
| Window Logo + PAUSE | Perform system function |
| Window Logo + 0-9 | Reserved for OEM use (see following text) |

The combination keystroke of the Window Logo + 1-0 keys are reserved for OEM use for auxiliary functions (speaker volume, monitor brightness, password, etc.).

Key position 112 (marked with an application window icon  ) is used in combination with other keys for invoking Windows application functions.

### C.2.4.4 Easy Access Keystrokes

The Easy Access keyboard (Figure C-7) includes additional keys (also referred to as buttons) used to streamline internet navigation.

These buttons have the default functionality described below:

| Button # | Description | Default Function |
|---|---|---|
| 1 | Check email | Email |
| 2 | Go to community | Emoney |
| 3 | Extra web site | Compaq web site |
| 4 | Go to favorite web site | AltaVista web site |
| 5 | Internet search | Search |
| 6 | Instant answer | Travel expenses |
| 7 | E-commerce | Shopping |

All buttons may be re-programmed by the user through the Easy Access utility.

## C.2.5 KEYBOARD COMMANDS

Table C-1 lists the commands that the keyboard can send to the system (specifically, to the 8042-type logic).

**Table C-1.**
Keyboard-to-System Commands

| Command | Value | Description |
|---|---|---|
| Key Detection Error/Over/run | 00h [1]<br>FFh [2] | Indicates to the system that a switch closure couldn't be identified. |
| BAT Completion | AAh | Indicates to the system that the BAT has been successful. |
| BAT Failure | FCh | Indicates failure of the BAT by the keyboard. |
| Echo | EEh | Indicates that the Echo command was received by the keyboard. |
| Acknowledge (ACK) | FAh | Issued by the keyboard as a response to valid system inputs (except the Echo and Resend commands). |
| Resend | FEh | Issued by the keyboard following an invalid input. |
| Keyboard ID | 83ABh | Upon receipt of the Read ID command from the system, the keyboard issues the ACK command followed by the two IDS bytes. |

Note:
[1] Modes 2 and 3.
[2] Mode 1 only.

## C.2.6 SCAN CODES

The scan codes generated by the keyboard processor are determined by the mode the keyboard is operating in.

- Mode 1: In Mode 1 operation, the keyboard generates scan codes compatible with 8088-/8086-based systems. To enter Mode 1, the scan code translation function of the keyboard controller must be disabled. Since translation is not performed, the scan codes generated in Mode 1 are identical to the codes required by BIOS. Mode 1 is initiated by sending command F0h with the 01h option byte. Applications can obtain system codes and status information by using BIOS function INT 16h with AH=00h, 01h, and 02h.

- Mode 2: Mode 2 is the default mode for keyboard operation. In this mode, the 8042 logic translates the make codes from the keyboard processor into the codes required by the BIOS. This mode was made necessary with the development of the Enhanced III keyboard, which includes additional functions over earlier standard keyboards. Applications should use BIOS function INT 16h, with AH=10h, 11h, and 12h for obtaining codes and status data. In Mode 2, the keyboard generates the Break code, a two-byte sequence that consists of a Make code immediately preceded by F0h (i.e., Break code for 0Eh is "F0h 0Eh").

- Mode 3: Mode 3 generates a different scan code set from Modes 1 and 2. Code translation must be disabled since translation for this mode cannot be done.

**Table C-2.**
Keyboard Scan Codes

| Key Pos. | Legend | Make / Break Codes (Hex) Mode 1 | Mode 2 | Mode 3 |
|---|---|---|---|---|
| 1 | Esc | 01/81 | 76/F0 76 | 08/na |
| 2 | F1 | 3B/BB | 05/F0 05 | 07/na |
| 3 | F2 | 3C/BC | 06/F0 06 | 0F/na |
| 4 | F3 | 3D/BD | 04/F0 04 | 17/na |
| 5 | F4 | 3E/BE | 0C/F0 0C | 1F/na |
| 6 | F5 | 3F/BF | 03/F0 03 | 27/na |
| 7 | F6 | 40/C0 | 0B/F0 0B | 2F/na |
| 8 | F7 | 41/C1 | 83/F0 83 | 37/na |
| 9 | F8 | 42/C2 | 0A/F0 0A | 3F/na |
| 10 | F9 | 43/C3 | 01/FO 01 | 47/na |
| 11 | F10 | 44/C4 | 09/F0 09 | 4F/na |
| 12 | F11 | 57/D7 | 78/F0 78 | 56/na |
| 13 | F12 | 58/D8 | 07/F0 07 | 5E/na |
| 14 | Print Scrn | E0 2A E0 37/E0 B7 E0 AA<br>E0 37/E0 B7 [1] [2]<br>54/84 [3] | E0 2A E0 7C/E0 F0 7C E0 F0 12<br>E0 7C/E0 F0 7C [1] [2]<br>84/F0 84 [3] | 57/na |
| 15 | Scroll Lock | 46/C6 | 7E/F0 7E | 5F/na |
| 16 | Pause | E1 1D 45 E1 9D C5/na<br>E0 46 E0 C6/na [3] | E1 14 77 E1 F0 14 F0 77/na<br>E0 7E E0 F0 7E/na [3] | 62/na |
| 17 | ` | 29/A9 | 0E/F0 E0 | 0E/F0 0E |
| 18 | 1 | 02/82 | 16/F0 16 | 46/F0 46 |
| 19 | 2 | 03/83 | 1E/F0 1E | 1E/F0 1E |
| 20 | 3 | 04/84 | 26/F0 26 | 26/F0 26 |
| 21 | 4 | 05/85 | 25/F0 25 | 25/F0 25 |
| 22 | 5 | 06/86 | 2E/F0 2E | 2E/F0 2E |
| 23 | 6 | 07/87 | 36/F0 36 | 36/F0 36 |
| 24 | 7 | 08/88 | 3D/F0 3D | 3D/F0 3D |
| 25 | 8 | 09/89 | 3E/F0 3E | 3E/F0 3E |
| 26 | 9 | 0A/8A | 46/F0 46 | 46/F0 46 |
| 27 | 0 | 0B/8B | 45/F0 45 | 45/F0 45 |
| 28 | - | 0C/8C | 4E/F0 4E | 4E/F0 4E |
| 29 | = | 0D/8D | 55/F0 55 | 55/F0 55 |
| 30 | \ | 2B/AB | 5D/F0 5D | 5C/F0 5C |
| 31 | Backspace | 0E/8E | 66/F0 66 | 66/F0 66 |
| 32 | Insert | E0 52/E0 D2<br>E0 AA E0 52/E0 D2 E0 2A [4]<br>E0 2A E0 52/E0 D2 E0 AA [6] | E0 70/E0 F0 70<br>E0 F0 12 E0 70/E0 F0 70 E0 12 [5]<br>E0 12 E0 70/E0 F0 70 E0 F0 12 [6] | 67/na |
| 33 | Home | E0 47/E0 D2<br>E0 AA E0 52/E0 D2 E0 2A [4]<br>E0 2A E0 47/E0 C7 E0 AA [6] | E0 6C/E0 F0 6C<br>E0 F0 12 E0 6C/E0 F0 6C E0 12 [5]<br>E0 12 E0 6C/E0 F0 6C E0 F0 12 [6] | 6E/na |
| 34 | Page Up | E0 49/E0 C7<br>E0 AA E0 49/E0 C9 E0 2A [4]<br>E0 2A E0 49/E0 C9 E0 AA [6] | E0 7D/E0 F0 7D<br>E0 F0 12 E0 7D/E0 F0 7D E0 12 [5]<br>E0 12 E0 7D/E0 F0 7D E0 F0 12 [6] | 6F/na |
| 35 | Num Lock | 45/C5 | 77/F0 77 | 76/na |
| 36 | / | E0 35/E0 B5<br>E0 AA E0 35/E0 B5 E0 2A [1] | E0 4A/E0 F0 4A<br>E0 F0 12 E0 4A/E0 F0 4A E0 12 [1] | 77/na |
| 37 | * | 37/B7 | 7C/F0 7C | 7E/na |
| 38 | - | 4A/CA | 7B/F0 7B | 84/na |
| 39 | Tab | 0F/8F | 0D/F0 0D | 0D/na |
| 40 | Q | 10/90 | 15/F0 15 | 15/na |

*Continued*

([x] Notes listed at end of table.)

**Table C-2**. Keyboard Scan Codes *(Continued)*

| Key Pos | Legend | Make / Break Codes (Hex) Mode 1 | Mode 2 | Mode 3 |
|---|---|---|---|---|
| 41 | W | 11/91 | 1D/F0 1D | 1D/F0 1D |
| 42 | E | 12/92 | 24/F0 24 | 24/F0 24 |
| 43 | R | 13/93 | 2D/F0 2D | 2D/F0 2D |
| 44 | T | 14/94 | 2C/F0 2C | 2C/F0 2C |
| 45 | Y | 15/95 | 35/F0 35 | 35/F0 35 |
| 46 | U | 16/96 | 3C/F0 3C | 3C/F0 3C |
| 47 | I | 17/97 | 43/F0 43 | 43/F0 43 |
| 48 | O | 18/98 | 44/F0 44 | 44/F0 44 |
| 49 | P | 19/99 | 4D/F0 4D | 4D/F0 4D |
| 50 | [ | 1A/9A | 54/F0 54 | 54/F0 54 |
| 51 | ] | 1B/9B | 5B/F0 5B | 5B/F0 5B |
| 52 | Delete | E0 53/E0 D3<br>E0 AA E0 53/E0 D3 E0 2A [4]<br>E0 2A E0 53/E0 D3 E0 AA [6] | E0 71/E0 F0 71<br>E0 F0 12 E0 71/E0 F0 71 E0 12 [5]<br>E0 12 E0 71/E0 F0 71 E0 F0 12 [6] | 64/F0 64 |
| 53 | End | E0 4F/E0 CF<br>E0 AA E0 4F/E0 CF E0 2A [4]<br>E0 2A E0 4F/E0 CF E0 AA [6] | E0 69/E0 F0 69<br>E0 F0 12 E0 69/E0 F0 69 E0 12 [5]<br>E0 12 E0 69/E0 F0 69 E0 F0 12 [6] | 65/F0 65 |
| 54 | Page Down | E0 51/E0 D1<br>E0 AA E0 51/E0 D1 E0 2A [4]<br>E0 @a E0 51/E0 D1 E0 AA [6] | E0 7A/E0 F0 7A<br>E0 F0 12 E0 7A/E0 F0 7A E0 12 [5]<br>E0 12 E0 7A/E0 F0 7A E0 F0 12 [6] | 6D/F0 6D |
| 55 | 7 | 47/C7 [6] | 6C/F0 6C [6] | 6C/na [6] |
| 56 | 8 | 48/C8 [6] | 75/F0 75 [6] | 75/na [6] |
| 57 | 9 | 49/C9 [6] | 7D/F0 7D [6] | 7D/na [6] |
| 58 | + | 4E/CE [6] | 79/F0 79 [6] | 7C/F0 7C |
| 59 | Caps Lock | 3A/BA | 58/F0 58 | 14/F0 14 |
| 60 | A | 1E/9E | 1C/F0 1C | 1C/F0 1C |
| 61 | S | 1F/9F | 1B/F0 1B | 1B/F0 1B |
| 62 | D | 20/A0 | 23/F0 23 | 23/F0 23 |
| 63 | F | 21/A1 | 2B/F0 2B | 2B/F0 2B |
| 64 | G | 22/A2 | 34/F0 34 | 34/F0 34 |
| 65 | H | 23/A3 | 33/F0 33 | 33/F0 33 |
| 66 | J | 24/A4 | 3B/F0 3B | 3B/F0 3B |
| 67 | K | 25/A5 | 42/F0 42 | 42/F0 42 |
| 68 | L | 26/A6 | 4B/F0 4B | 4B/F0 4B |
| 69 | ; | 27/A7 | 4C/F0 4C | 4C/F0 4C |
| 70 | ‘ | 28/A8 | 52/F0 52 | 52/F0 52 |
| 71 | Enter | 1C/9C | 5A/F0 5A | 5A/F0 5A |
| 72 | 4 | 4B/CB [6] | 6B/F0 6B [6] | 6B/na [6] |
| 73 | 5 | 4C/CC [6] | 73/F0 73 [6] | 73/na [6] |
| 74 | 6 | 4D/CD [6] | 74/F0 74 [6] | 74/na [6] |
| 75 | Shift (left) | 2A/AA | 12/F0 12 | 12/F0 12 |
| 76 | Z | 2C/AC | 1A/F0 1A | 1A/F0 1A |
| 77 | X | 2D/AD | 22/F0 22 | 22/F0 22 |
| 78 | C | 2E/AE | 21/F0 21 | 21/F0 21 |
| 79 | V | 2F/AF | 2A/F0 2A | 2A/F0 2A |
| 80 | B | 30/B0 | 32/F0 32 | 32/F0 32 |

*Continued*

([x] Notes listed at end of table.)

**Table C-2**. Keyboard Scan Codes *(Continued)*

| Key Pos. | Legend | Make / Break Codes (Hex) Mode 1 | Mode 2 | Mode 3 |
|---|---|---|---|---|
| 81 | N | 31/B1 | 31/F0 31 | 31/F0 31 |
| 82 | M | 32/B2 | 3A/F0 3A | 3A/F0 3A |
| 83 | , | 33/B3 | 41/F0 41 | 41/F0 41 |
| 84 | . | 34/B4 | 49/F0 49 | 49/F0 49 |
| 85 | / | 35/B5 | 4A/F0 4A | 4A/F0 4A |
| 86 | Shift (right) | 36/B6 | 59/F0 59 | 59/F0 59 |
| 87 | ↑ | E0 48/E0 C8<br>E0 AA E0 48/E0 C8 E0 2A [4]<br>E0 2A E0 48/E0 C8 E0 AA [6] | E0 75/E0 F0 75<br>E0 F0 12 E0 75/E0 F0 75 E0 12 [5]<br>E0 12 E0 75/E0 F0 75 E0 F0 12 [6] | 63/F0 63 |
| 88 | 1 | 4F/CF [6] | 69/F0 69 [6] | 69/na [6] |
| 89 | 2 | 50/D0 [6] | 72/F0 72 [6] | 72/na [6] |
| 90 | 3 | 51/D1 [6] | 7A/F0 7A [6] | 7A/na [6] |
| 91 | Enter | E0 1C/E0 9C | E0 5A/F0 E0 5A | 79/F0 79[6] |
| 92 | Ctrl (left) | 1D/9D | 14/F0 14 | 11/F0 11 |
| 93 | Alt (left) | 38/B8 | 11/F0 11 | 19/F0 19 |
| 94 | (Space) | 39/B9 | 29/F0 29 | 29/F0 29 |
| 95 | Alt (right) | E0 38/E0 B8 | E0 11/F0 E0 11 | 39/na |
| 96 | Ctrl (right) | E0 1D/E0 9D | E0 14/F0 E0 14 | 58/na |
| 97 | ← | E0 4B/E0 CB<br>E0 AA E0 4B/E0 CB E0 2A [4]<br>E0 2A E0 4B/E0 CB E0 AA [6] | E0 6B/Eo F0 6B<br>E0 F0 12 E0 6B/E0 F0 6B E0 12[5]<br>E0 12 E0 6B/E0 F0 6B E0 F0 12[6] | 61/F0 61 |
| 98 | ↓ | E0 50/E0 D0<br>E0 AA E0 50/E0 D0 E0 2A [4]<br>E0 2A E0 50/E0 D0 E0 AA [6] | E0 72/E0 F0 72<br>E0 F0 12 E0 72/E0 F0 72 E0 12[5]<br>E0 12 E0 72/E0 F0 72 E0 F0 12[6] | 60/F0 60 |
| 99 | → | E0 4D/E0 CD<br>E0 AA E0 4D/E0 CD E0 2A [4]<br>E0 2A E0 4D/E0 CD E0 AA [6] | E0 74/E0 F0 74<br>E0 F0 12 E0 74/E0 F0 74 E0 12[5]<br>E0 12 E0 74/E0 F0 74 E0 F0 12[6] | 6A/F0 6A |
| 100 | 0 | 52/D2 [6] | 70/F0 70 [6] | 70/na [6] |
| 101 | . | 53/D3 [6] | 71/F0 71 [6] | 71/na [6] |
| 102 | na | 7E/FE | 6D/F0 6D | 7B/F0 7B |
| 103 | na | 2B/AB | 5D/F0 5D | 53/F0 53 |
| 104 | na | 36/D6 | 61/F0 61 | 13/F0 13 |
| 110 | (Win95) [7] | E0 5B/E0 DB<br>E0 AA E0 5B/E0 DB E0 2A [4]<br>E0 2A E0 5B/E0 DB E0 AA [6] | E0 1F/E0 F0 1F<br>E0 F0 12 E0 1F/E0 F0 1F E0 12 [5]<br>E0 12 E0 1F/E0 F0 1F E0 F0 12 [6] | 8B/F0 8B |
| 111 | (Win95) [7] | E0 5C/E0 DC<br>E0 AA E0 5C/E0 DC E0 2A [4]<br>E0 2A E0 5C/E0 DC E0 AA [6] | E0 2F/E0 F0 27<br>E0 F0 12 E0 27/E0 F0 27 E0 12 [5]<br>E0 12 E0 27/E0 F0 27 E0 F0 12 [6] | 8C/F0 8C |
| 112 | (Win Apps) [7] | E0 5D/E0 DD<br>E0 AA E0 5D/E0 DD E0 2A [4]<br>E0 2A E0 5D E0 DD E0 AA [6] | E0 2F/E0 F0 2F<br>E0 F0 12 E0 2F/E0 F0 2F E0 12 [5]<br>E0 12 E0 2F/E0 F0 2F E0 F0 12 [6 | 8D/F0 8D |
| Btn 1 | [8] | E0 1E/E0 9E | E0 1C/E0 F0 1C | 95/F0 95 |
| Btn 2 | [8] | E0 26/E0 A6 | E0 4B/E0 F0 4B | 9C/F0 9C |
| Btn 3 | [8] | E0 25/E0 A5 | E0 42/E0 F0 42 | 9D/F0 9D |
| Btn 4 | [8] | E0 23/E0 A3 | E0 33/E0 F0 33 | 9A/F0 9A |
| Btn 5 | [8] | E0 21/E0 A1 | E0 2B/E0 F0 2B | 99/F0 99 |
| Btn 6 | [8] | E0 12/E0 92 | E0 24/E0 F0 24 | 96/F0 96 |
| Btn 7 | [8] | E0 32/E0 B2 | E0 3A/E0 F0 3A | 97/F0 97 |

NOTES:

All codes assume Shift, Ctrl, and Alt keys inactive unless otherwise noted.
NA = Not applicable
[1] Shift (left) key active.
[2] Ctrl key active.
[3] Alt key active.
[4] Left Shift key active. For active right Shift key, substitute AA/2A make/break codes for B6/36 codes.
[5] Left Shift key active. For active right Shift key, substitute F0 12/12 make/break codes for F0 59/59 codes.
[6] Num Lock key active.
[7] Windows keyboards only.
[8] Easy Access keyboards only.

## C.3 CONNECTORS

Two types of keyboard interfaces are used in Compaq systems: PS/2-type and USB-type. Systems that provide a PS/2 connector will ship with a PS/2-type keyboard but may also support simultaneous connection of a USB keyboard. Systems that do not provide a PS/2 interface will ship with a USB keyboard. For a detailed description of the PS/2 and USB interfaces refer to the Input/Output chapter of this guide. The keyboard cable connectors and their pinouts are described in the following figures:

| Pin | Function |
|---|---|
| 1 | Data |
| 2 | Not connected |
| 3 | Ground |
| 4 | +5 VDC |
| 5 | Clock |
| 6 | Not connected |

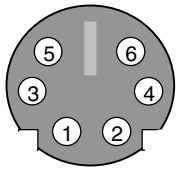



**Figure C–8.** PS/2 Keyboard Cable Connector (Male)

| Pin | Function |
|---|---|
| 1 | +5 VDC |
| 2 | Data (+) |
| 3 | Data (-) |
| 4 | Ground |

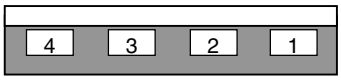



**Figure C–9.** USB Keyboard Cable Connector (Male)

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