COMPAQ

Technical Reference Guide

for

Compaq Deskpro 4000N and 4000S Personal Computers

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Deskpro 4000N and 4000S Personal Computers ***TRG***

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Technical Reference Guide for
Compaq Deskpro 4000N and 4000S Personal Computers
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Chapter 1
INTRODUCTION

1.1 ABOUT THIS GUIDE

This guide provides technical information about the Compaq Deskpro 4000N and 4000S Personal Computers. This document includes information regarding system design, function, and features that can be used by programmers, engineers, technicians, and system administrators.

1.1.1 USING THIS GUIDE

This guide consists of chapters and appendices. The chapters primarily describe the hardware and firmware elements contained within the chassis and specifically deal with the system board and the power supply assembly. The appendices contain general information about standard peripheral devices such as the keyboard as well as separate audio or other interface cards, as well as other general information in tabular format.

1.1.2 ADDITIONAL INFORMATION SOURCES

This guide does not describe in detail other manufacturer's components used in the product covered. For more information on individual commercial-off-the-shelf (COTS) components refer to the indicated manufacturers' documentation. The products covered by this guide use architecture based on industry-standard specifications that can be referenced for detailed information.

Hardcopy documentation sources:

- The Lotus/Intel/Microsoft Expanded Memory Specification, Ver. 4.0
- PCI Local Bus Specification Revision 2.1
- Extended Industry Standard Architecture Expansion Bus Technical Reference Guide, p/n 130584, Second Edition, Compaq Computer Corporation
- Compaq Basic Input/Out System (BIOS) Technical Reference Guide
  Doc.# 074A/0693, Fourth Edition, Compaq Computer Corporation

Online information sources:

- Compaq Computer Corporation: http://www.compaq.com
- Intel Corporation: http://www.intel.com
- VIA Technologies Incorporated: http://www.via.com
- National Semiconductor: http://www.national.com
- S3 Incorporated: http://www.S3.com

1.2 NOTATIONAL CONVENTIONS

1.2.1 VALUES

Hexadecimal values are indicated by the letter “h” following an alpha-numerical value. Binary values are indicated by the letter “b” following a value of ones and zeros. Memory addresses expressed as “SSSS:OOOO” (SSSS = 16-bit segment, OOOO = 16-bit offset) can be assumed as a hexadecimal value. Values that have no succeeding letter can be assumed to be decimal.

1.2.2 RANGES

Ranges or limits for a parameter are shown as a pair of values separated by two dots:

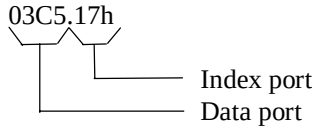
Example: Bits <7..4> = bits 7, 6, 5, and 4.

1.2.3 SIGNAL LABELS

Signal names are indicated using abbreviations, acronyms, or, if possible, the full signal name in all capital letters. Signals that are meant to be active low are indicated with a dash immediately following the name.

1.2.4 REGISTER NOTATION AND USAGE

This guide uses standard Intel naming conventions in discussing the microprocessor’s (CPU) internal registers. Registers that are accessed through programmable I/O using an indexing scheme are indicated using the following format:



In the example above, register 03C5.17h is accessed by writing the index port value 17h to the index address (03C4h), followed by a write to or a read from port 03C5h.

1.2.5 BIT NOTATION

Bit values are labeled with bit <0> representing the least-significant bit (LSb) and bit <7> representing the most-significant bit (MSb) of a byte. Bytes, words, double words, and quad words are typically shown with most-significant portions on the left or top and the least-significant portions on the right or bottom respectively.

1.3 COMMON ACRONYMS AND ABBREVIATIONS

Table 1-1 lists the acronyms and abbreviations used in this guide.

Table 1-1.
Acronyms and Abbreviations

Acronym/Abbreviation	Description
A	ampere
AC	alternating current
ACPI	Advanced Configuration and Power Interface
A/D	analog-to-digital
AGP	advanced graphics port
API	application programming interface
APM	advanced power management
ASIC	application-specific integrated circuit
AT	1. attention (commands) 2. 286-based PC architecture
ATA	AT attachment (mode)
AVI	audio-video interleaved
AVGA	Advanced VGA
BCD	binary-coded decimal
BIOS	basic input/output system
bis	second/new revision
BitBLT	bit block transfer
BNC	Bayonet Neill-Concelman (connector)
bps or b/s	bits per second
BSP	Bootstrap processor
CAS	column address strobe
CD	compact disk
CD-ROM	compact disk read-only memory
CDS	compct disk system
CF	carry flag
CGA	color graphics adapter
Ch	channel
CLUT	color look-up table (pallete)
cm	centimeter
CMC	cache/memory controller
CMOS	complimentary metal-oxide semiconductor (configuration memory)
Cntlr	controller
codec	compressor/decompressor
CPQ	Compaq
CPU	central processing unit
CRT	cathode ray tube
CSM	Compaq system management / Compaq server management
DAA	direct access arrangement
DAC	digital-to-analog converter
db	decibel
DC	direct current
DCH	DOS compatibility hole
DDC	Display Data Channel
DF	direction flag

Continued

Table 1-1. Acronyms and Abbreviations *Continued*

Acronym/Abbreviation	Description
DIMM	dual inline memory module
DIN	Deutche IndustriNorm (connector standard)
DIP	dual inline package
DMA	direct memory access
dpi	dots per inch
DRAM	dynamic random access memory
DRQ	data request
EDID	extended display identification data
EDO	extended data out (RAM type)
EEPROM	electrically eraseable PROM
EGA	enhanced graphics adapter
EIA	Electronic Industry Association
EISA	extended ISA
EPP	enhanced parallel port
EIDE	enhanced IDE
ESCD	Extended System Configuration Data (format)
EV	Environmental Variable (data)
ExCA	Exchangeable Card Architecture
FIFO	first in / first out
FL	flag (register)
FM	frequency modulation
FPM	fast page mode (RAM type)
FPU	Floating point unit (numeric or math coprocessor)
ft	foot
GB	gigabyte
GND	ground
GPIO	general purpose I/O
GPOC	general purpose open-collector
GUI	graphics user interface
h	hexadecimal
HW	hardware
hex	hexadecimal
Hz	hertz
IDE	integrated drive element
IEEE	Institute of Electrical and Electronic Engineers
IF	interrupt flag
I/F	interface
in	inch
INT	interrupt
I/O	input/output
IPL	initial program loader
IrDA	InfraRed Data Association
IRQ	interrupt request
ISA	industry standard architecture
JEDEC	Joint Electron Device Engineering Council
Kb / KB	kilobits / kilobytes (x 1024 bits / x 1024 bytes)
Kb/s	kilobits per second
kg	kilogram
KHz	kilohertz
kv	kilovolt

Continued

Table 1-1. Acronyms and Abbreviations *Continued*

Acronym/Abbreviation	Description
lb	pound
LCD	liquid crystal display
LED	light-emitting diode
LIF	low insertion force (socket)
LSI	large scale integration
LSb / LSB	least significant bit / least significant byte
LUN	logical unit (SCSI)
MMX	multimedia extensions
MPEG	Motion Picture Experts Group
MOSFET	Metal oxide silicon field effect transistor
ms	millisecond
MSb / MSB	most significant bit / most significant byte
mux	multiplex
MVA	motion video acceleration
MVW	motion video window
n	variable parameter/value
NIC	network interface card/controller
NiCad	nickel cadmium
NiMH	nickel-metal hydride
NMI	non-maskable interrupt
ns	nanosecond
NT	nested task flag
NTSC	National Television Standards Committee
NVRAM	non-volatile random access memory
OEM	original equipment manufacturer
OS	operating system
PAL	1. programmable array logic 2. phase altering line
PC	personal computer
PCI	peripheral component interconnect
PCM	pulse code modulation
PCMCIA	Personal Computer Memory Card International Association
PF	parity flag
PIN	personal identification number
POST	power-on self test
PROM	programmable read-only memory
PTR	pointer
RAM	random access memory
RAS	row address strobe
rcvr	receiver
RF	resume flag
RGB	red/green/blue
RH	Relative humidity
RMS	root mean square
ROM	read-only memory
RPM	revolutions per minute
RTC	real time clock
R/W	read/write

Continued

Table 1-1. Acronyms and Abbreviations *Continued*

Acronym/Abbreviation	Description
SCSI	small computer system interface
SDRAM	Synchronous Dynamic RAM
SEC	Single Edge-Connector
SECAM	sequential colour avec memoire (sequential color with memory)
SF	sign flag
SGRAM	Synchronous Graphics RAM
SIMM	single in-line memory module
SIT	system information table
SMI	system management interrupt
SMM	system management mode
SMRAM	system management RAM
SPD	serial presence detect
SPP	standard parallel port
SRAM	static RAM
STN	super twist pneumatic
SVGA	super VGA
SW	software
TAD	telephone answering device
TAM	telephone answering machine
TCP	tape carrier package
TF	trap flag
TFT	thin-film transistor
TIA	Telecommunications Information Administration
TPE	twisted pair ethernet
TPI	track per inch
TTl	transistor-transistor logic
TV	television
TX	transmit
UART	universal asynchronous receiver/transmitter
us / µs	microsecond
USB	Universal Serial Bus
UTP	unshielded twisted pair
V	volt
VESA	Video Electronic Standards Association
VGA	video graphics adapter
vib	vibrato
VLSI	very large scale integration
VRAM	Video RAM
W	watt
WRAM	Windows RAM
ZF	zero flag
ZIF	zero insertion force (socket)

Chapter 2
SYSTEM OVERVIEW

2.1 INTRODUCTION

The Compaq Deskpro 4000N and 4000S Personal Computers are based on Pentium microprocessors featuring MMX technology and designed with an emphasis on speed, storage capacity, and multimedia compatibility to meet the requirements of the business environment. These models feature architectures incorporating the PCI and ISA buses. All models are easily upgradeable and expandable to keep pace with the needs of the office or home.

Figure 2–1. Compaq Deskpro 4000S Personal Computer with Monitor

2.2 FEATURES

This section describes the standard and distinguishing features.

2.2.1 STANDARD FEATURES

The following standard features are included on all models:

- Pentium microprocessor with MMX technology
- 256-KB second-level cache
- 16 or 32 megabytes of SDRAM, with support for ECC and SDP memory
- Integrated S3 Trio64V2/GX graphics controller with 2-MB frame
- Enhanced IDE controller supporting Ultra ATA (UDMA) modes 0-2
- Hard drive fault prediction
- PCI connector
- Two serial interfaces
- Parallel interface
- Two universal serial bus ports
- Integrated network interface controller (RJ-45/AUI ports)
- Compaq Space Saver keyboard w/Windows support
- Compaq PS/2-type mouse
- APM 1.2 power management support
- Plug 'n Play compatible (with ESCD support)
- Energy Star compliant
- 76-watt, surge-tolerant power supply

The Deskpro 4000N and 4000S support the Intelligent Manageability features listed below:

Configuration Management	**Asset Management**	**Fault Management**	**Security Management**
Remote ROM Flash	RAM Type Data	ECC RAM Fault Prediction	Memory Change Alert
Remote Security	DMI BIOS	SMART II Hard Drive	Ownership Tag
Remote Wakeup	Asset Tag	Monitor Fault Diag.	Config. Cntrl. Hardware
Remote Shutdown	Sys. Serial #	UDMA Integrity Log.	Setup Password
Replicated Setup	Sys. Manuf./Model	Proactive Backup	Power-On Password
ACPI-Ready	Sys. Board Rev. Level	Thermal Sensor	QuickLock/QuickBlank
Dual-State Power Sw.	ROM rev.		Diskette Boot Cntrl.
Failsafe Boot Block ROM	Hard Drive Type Data		Diskette Write Cntrl.
	Monitor Type Data		I/O Port En/Dis. Cntrl.
	Compaq Insight Edition		Cable Lock Provision

The Intelligent Manageability features provide support for DMI 2.0, Compaq Insight Manager, and Management Solutions Partners.

2.2.2 MODEL DIFFERENCES

	Deskpro 4000N	**Deskpro 4000S**
PCI connector:	1	1 (shared slot)
ISA connector:	none	1 (shared slot)
OS installed:	Windows NT 4.0	Windows 95
Remote boot support:	Yes	No
Diskette drive installed:	No	Yes
Hard drive size:	1.6 or 2.1 GB	2.1 GB
CD-ROM support:	No	Yes

2.2.3 OPTIONS

Options that are specific to the Compaq Deskpro 4000N and 4000S Series Personal Computers include:

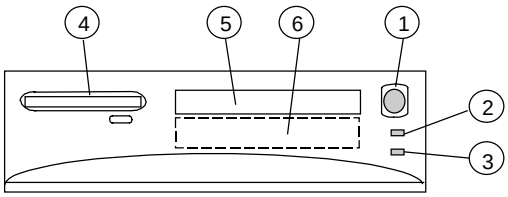
- System Memory: 8-MB DIMM
  16-MB DIMM
  32-MB DIMM
  64-MB DIMM
  128-MB DIMM

Compaq Deskpro Computers are easily upgraded and enhanced with peripheral devices designed to meet PCI and ISA standards. The Compaq Deskpro Personal Computers are compatible with peripherals design for Plug ’n Play operation.

2.3 MECHANICAL DESIGN

This section illustrates the layout used by the formfactor. In addition, this section includes the layout of the system board.

2.3.1 CABINET LAYOUT

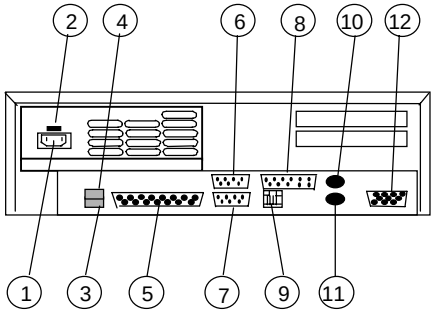


Item	Function
1	Power Switch
2	Power-On Light
3	Hard Drive Activity Light
4	1.44 MB Diskette Drive (3.5” Drive) [1]
5	1/3 Height Drive Bay (3.5” or 5.25” Drive) [2]
6	1/3 Height Drive Bay (3.5” or 5.25” Drive)

NOTES:

[1] Deskpro 4000S only
[2] Front panel access on 4000S only.

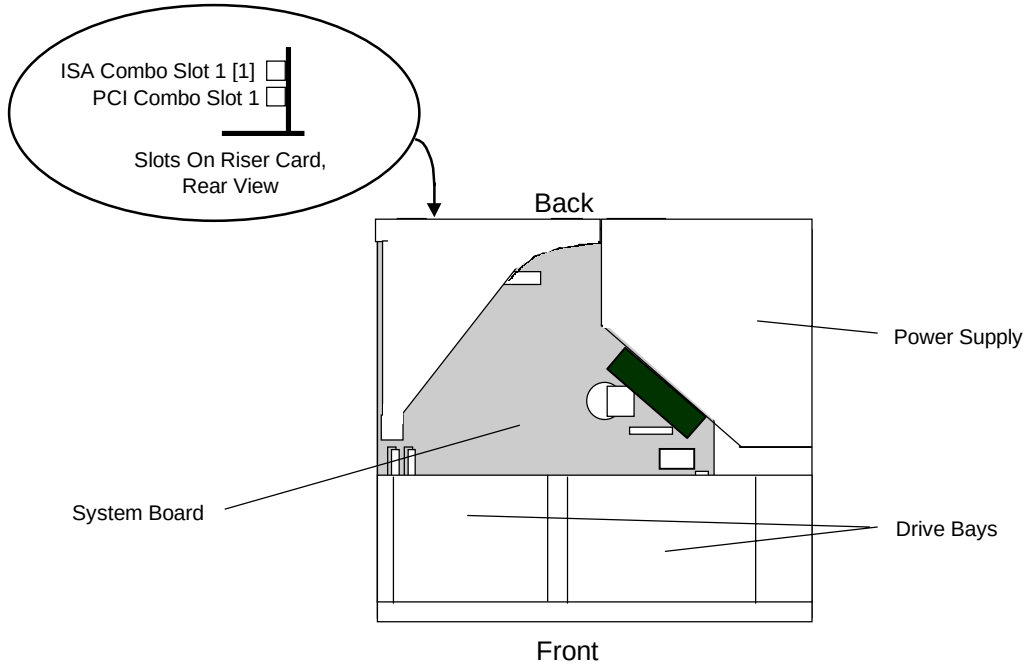
Figure 2–2. Cabinet Layout, Front View



Item	Function
1	AC Line In Connector
2	Line Voltage Select Switch
3	Universal Serial Bus Interface port 1
4	Universal Serial Bus Interface port 2
5	Parallel Interface Connector
6	Serial Interface Connector B
7	Serial Interface Connector A
8	Network Interface AUI Connector
9	Network Interface RJ-45 Connector
10	Mouse Connector
11	Keyboard Connector
12	Monitor Interface

Figure 2–3. Cabinet Layout, Rear View

2.3.2 CHASSIS LAYOUT

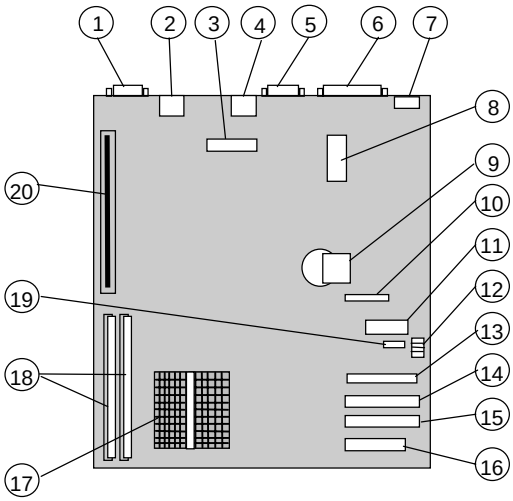


NOTES:

[1] Deskpro 4000S only

Figure 2–4. Chassis Layout, Top View

2.3.3 SYSTEM BOARD LAYOUT



System Board
p/n 006582-xxx (4000S)
or
p/n 007602-xxx (4000N)

Item	Function
1	Graphics monitor connector (J2)
2	Top, Mouse interface connector; Bottom, keyboard connector (J9)
3	NIC AUI connector header (P15)
4	NIC RJ-45 connector (J5)
5	Serial interface connector (P24)
6	Parallel interface connector (J3)
7	Universal serial bus connectors (J6)
8	Power supply connector (P17)
9	RTC/CMOS Battery
10	RTC/CMOS battery replacement header (P14)
11	Power switch, PWR/HD LED cable connector (P16)
12	Processing frequency configuration switch (SW1)
13	CD-ROM connector (P25)
14	Secondary IDE connector (P21)
15	Primary IDE connector (P20)
16	Diskette drive connector (J1)
17	Microprocessor (in type 7 socket)
18	DIMM sockets (J7, J8)
19	CD-ROM drive connector P25 audio out (J11)
20	Riser card connector (J4)

Figure 2–5. System Board Layout, Component Side

2.4 SYSTEM ARCHITECTURE

The Compaq Deskpro 4000N and 4000S Personal Computers featuring MMX technology are based on a Pentium MXX microprocessor matched with a support chipset that is complimentary in design. Both the "N" and "S" systems share the same basic architecture (Figure 2-7), which utilizes three main buses: the Host bus, the Peripheral Component Interconnect (PCI) bus, and the Industry Standard Architecture (ISA) bus.

The Host bus provides high performance support for CPU, cache and system memory accesses, and on these systems is set to operate at 66 MHz. The 32-bit PCI bus provides support for the graphics subsystem, the EIDE controllers, and expansion devices designed for high performance. The PCI bus operates at 33 MHz. The ISA bus provides a standard 8-MHz interface for the input/output (I/O) devices such as the keyboard, diskette drive, serial and parallel interfaces, as well as the addition of 16- or 8-bit expansion devices.

The CPU/PCI and PCI/ISA bridge functions are handled by the specific support chipset matched with the microprocessor employed. The support chipset also provides memory controller and data buffering functions as well as bus control and arbitration functions.

The I/O port functions and diskette drive controller are integrated into the PC87307 I/O Controller. This component also includes the real time clock and battery-backed configuration memory (CMOS).

Table 2-1 lists the architectural highlights.

Table 2-1.
Architectural Overview

	Type
Microprocessor	Pentium MMX
Support Chipset	VIA VP2
System Memory	
Standard installed:	16/32 MB [1]
Expandable to:	256 MB
Cache Memory	
L1:	32 KB [2]
L2:	256 KB
Graphics Subsystem	S3 TrioV2-based integrated on board

NOTES:
[1] Depending on model
[2] Integrated with the microprocessor

The following subsections provide a description of the key functions and subsystems.

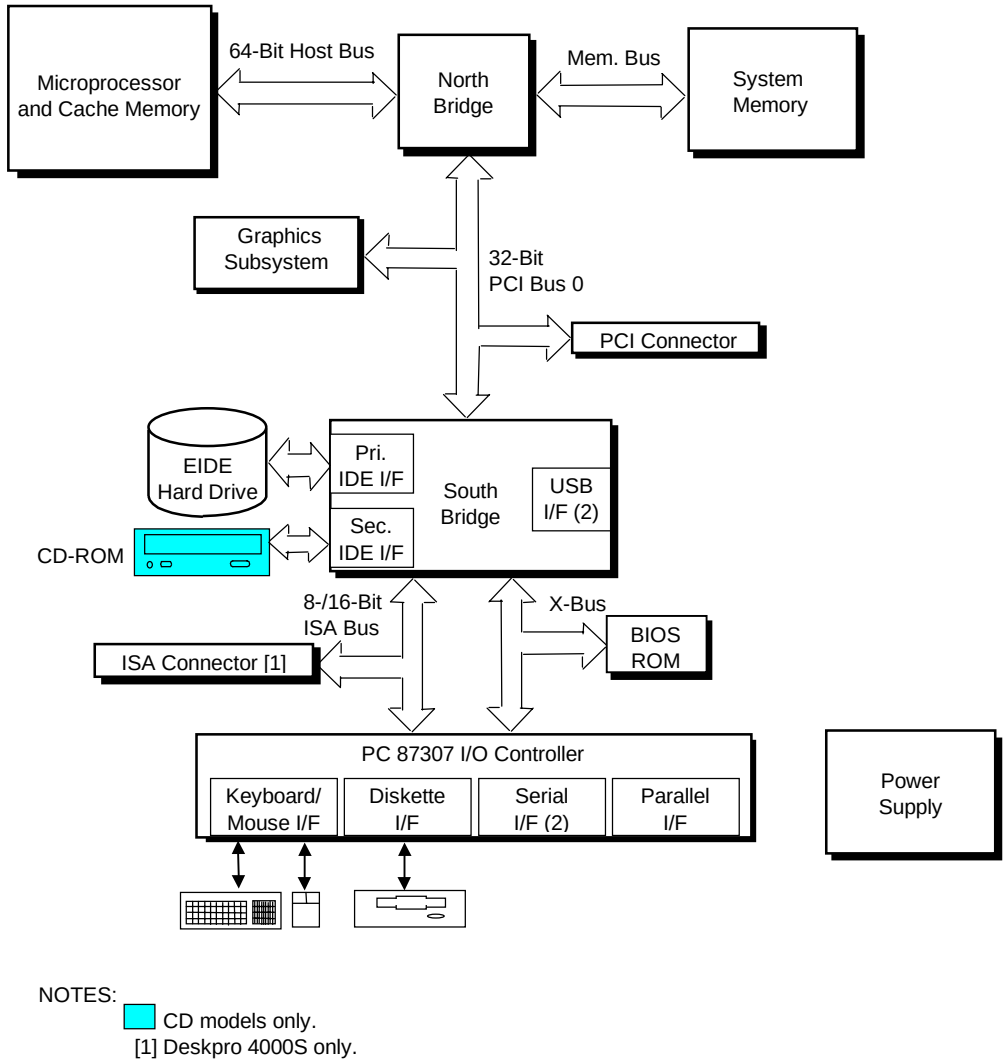


Figure 2–6. Compaq Deskpro 4000N and 4000S System Architecture, Block diagram

2.4.1 MICROPROCESSOR

The Compaq Deskpro 4000N and 4000S Personal Computers feature the Pentium MMX microprocessor that is backward-compatible with software written for x86-type processors. The Pentium MMX microprocessor includes a 32 KB L1 cache and extensions to the instruction set that provide higher performance for processing graphics and video code. The microprocessor is mounted in a ZIF type-7 socket that allows replacing and/or upgrading.

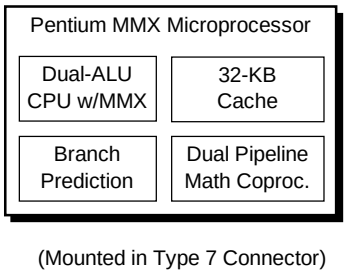


Figure 2–7. Microprocessor Architectural Diagram

2.4.2 MEMORY

This system includes 256 kilobytes of SRAM for secondary (L2) cache support of the microprocessor's primary (L1) cache. The L2 cache is arranged as direct-mapped, write-through using synchronous pipelined burst SRAMs.

For system memory two 168-pin DIMM sockets are provided with 16 or 32 megabytes of un-buffered SDRAM installed depending on model. System memory can be expanded up to 256 megabytes using 8-, 16-, 32-,64-, and 128-MB DIMMs. Both EDO and SDRAM DIMMs are supported (SDRAM DIMMs are recommended). The system supports the use of ECC memory as well.

The system ROM utilizes a flash ROM component that contains the BIOS and stores PCI, ESCD, and EV data. The BIOS is updateable by remote or local flashing of the ROM, which includes boot block ROM support.

2.4.3 SUPPORT CHIPSET

Table 2-2 shows the chipsets used for the Deskpro 4000N and 4000S systems.

Table 2-2.
Support Chipsets

Function	Component
Host/PCI (North) Bridge:	VT82C595
System Controller	"
Data Buffer	"
PCI/ISA (South) Bridge:	VT82C586
EIDE Controller	"
DMA Controller	"
Interrupt Controller	"
Timer/Counter	"
NMI Registers	"
Reset Control Reg.	"
USB I/F	"
I/O Controller:	87307
Keyboard I/F	"
Diskette I/F	"
Serial I/F	"
Parallel I/F	"
RTC/CMOS Mem.	"
GPIO Ports	"

2.4.4 MASS STORAGE

A 1.6- or 2.1-GB EIDE hard drive may be installed, depending on series/model. All models include a PCI bus mastering Enhanced IDE (EIDE) controller that provides two EIDE interfaces supporting two IDE devices. Master/slave drive selection is determined using the cable-select method, eliminating the need to move jumpers when re-configuring drives. The mass storage drive bay capacity is determined by the form factor (refer to Section 2.3, Mechanical Design). All Deskpro 4000S models include a 3.5 inch 1.44-MB diskette drive installed.

2.4.5 SERIAL AND PARALLEL INTERFACES

All models include two serial and one parallel port available at the rear of the unit chassis. The serial and parallel ports are integrated into a PC87307 I/O Controller component. The serial ports use 16550/16450-equivalent logic and are RS-232-C compatible and operate at baud rates up to 115,200. The parallel interface is Enhanced Parallel Port (EPP1.9) and Enhanced Capability Port (ECP) compatible, and supports bi-directional data transfers.

2.4.6 UNIVERSAL SERIAL BUS INTERFACE

Two Universal Serial Bus (USB) ports are included, each providing a high speed interface for future systems and/or peripherals. The USB interface operates at 12 Mbps and provides hot plugging/unplugging (Plug 'n Play) functionality.

2.4.7 GRAPHICS SUBSYSTEM

The graphics subsystem is integrated on the system board and operates off the PCI bus. The subsystem is based on the S3 Trio64 V2/GX controller and includes two megabytes of SGRAM. The subsystem provides a maximum resolution of 1280 x 1024 with 256 colors.

NOTE: The graphics subsystem is not upgradeable.

Table 2-3.
Graphics Subsystem Overview

Parameter	Type
Graphics Controller	S3 Trio64V2
Graphics Memory	2 MB SGRAM
Maximum Resolution	1280x1024 @ 256 colors

2.5 SPECIFICATIONS

This section includes the environmental, electrical, and physical specifications for the Compaq Deskpro 4000N and 4000S Series Personal Computers.

Table 2-4.
Environmental Specifications

Parameter	Operating	Nonoperating
Air Temperature	50° to 95° F (10° to 35° C)	-24° to 140° F (-30° to 60° C)
Shock	N/A	60.0 g for 2 ms half-sine pulse
Vibration	0.000215g^ 2/Hz, 10-300 Hz [1]	0.0005g^ 2/Hz, 10-500 Hz [1]
Humidity	80% RH @ 36° C (no hard drive)	95% RH @ 36° C
Maximum Altitude	10,000 ft (3048 m)	30,000 ft (9,144 m)

NOTE:
Values are subject to change without notice.
[1] 0.5 grms nominal.

Table 2-5.
Electrical Specifications

Parameter	Domestic	International
Input Line Voltage:		
Nominal:	100 - 120 VAC	200 - 240 VAC
Maximum:	90 - 132 VAC	180 - 264 VAC
Input Line Frequency Range:		
Nominal:	50 - 60 Hz	50 - 60 Hz
Maximum:	47 - 63 Hz	47 - 63 Hz
Power Supply		
Maximum Continuous Power:	75 watts	75 watts
Maximum Line Current Draw:	5.5 A	?? watts
		3.0 A

Table 2-6.
Physical Specifications

Dimension	Measurement
Height	3.56 in (9.00 cm)
Width	112.50 in (31.80 cm)
Depth	14.60 in (37.10 cm)
Weight	20 lb (9.08 kg)

NOTE:
Metric measurements shown in parenthesis.

Table 2-7.
Diskette Drive Specifications

Paramemter	Measurement
Media Type	3.5 in 1.44 MB/720 KB diskette
Height	1/3
Bytes per Sector	512
Sectors per Track:	
High Density	18
Low Density	9
Tracks per Side:	
High Density	80
Low Density	80
Read/Write Heads	2
Average Access Time:	
Track-to-Track (high/low)	3 ms/3 ms
Average (high/low)	94 ms/94ms
Settling Time	15 ms
Latency Average	100 ms

Table 2-8.
20x CD-ROM Drive Specifications

Paramemter	Measurement
Media Type	Mode 1,2, Mixed Mode, CD-DA, Photo CD, Cdi, CD-XA
Center Hole Diameter	15 mm
Disc Diameter	8/12 cm
Disc Thickness	1.2 mm
Track Pitch	1.6 um
Laser	
Beam Divergence	53.5 +/- 1.5 °
Output Power	53.6 0.14 mW
Typr	GaAs
Wave Length	790 +/- 25 nm
Average Access Time:	
Random	150 ms
Full Stroke	600 ms
Audio Output Level	0.7 Vrms
Cache Buffer	128 KB (min)
Data Transfer Time	
Sustained	3000 KB/s
Startup Time	7 secs (nom)

Table 2-9.
Hard Drive Specifications

Parameter	**1.6 GB**	**2.1 GB**
Interface:	EIDE	EIDE
Drive Type:	65	65
Drive Size:	5.25 in	5.25 in
Transfer Rate		
Heads:	94.0 Mb/s	27.2-55 Mb/s
Interface:	16.7 MB/s	16.7 MB/s
Seek Time (w/settling)		
Single Track:	2.0 ms	2.0 ms
Average:	11.0 ms	12.0 ms
Full Stroke:	25.0 ms	22.0 ms
Disk RPM:	4500	4500
EDMA Support:	Mode 2	Mode 2
PIO Support:	Mode 4	Mode 4
Power Mode Command Support:	Yes	Yes
Drive Fault Prediction:	SMART II	SMART II

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Chapter 3
PROCESSOR/ MEMORY SUBSYSTEM

3.1 INTRODUCTION

This chapter describes the processor/cache memory subsystem of the Compaq Deskpro 4000N and 4000S Series of Personal Computers.

This chapter includes the following topics:

Table 3-1 lists the highlights of the processor/memory architecture.

Table 3-1.
Processor/Memory
Architectural Highlights

Feature	Type/Amount
Support Chipset	VT82C595
System Memory	
Standard installed:	16 or 32 MB SDRAM
Expandable to:	256 MB
Cache Memory	
L1:	32 KB [1]
L2:	256 KB

NOTES:
[1] Integrated into the microprocessor

3.2 PENTIUM MMX-BASED PROCESSOR/MEMORY SUBSYSTEM

The processor/memory subsystem is based on the Pentium MMX microprocessor, a 512-KB or 1-MB secondary cache, and a VT82C595 system controller (Figure 3-1).

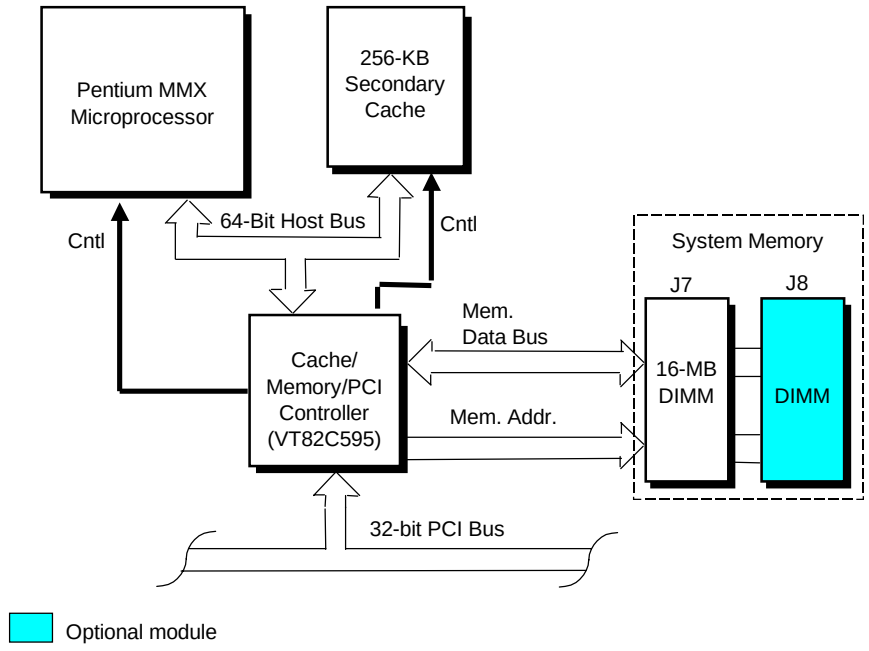


Figure 3–1. Processor/Memory Subsystem Architecture

The microprocessor is mounted in a ZIF type 7 socket that facilitates easy changing/upgrading. The system supports both 2.8V and 3.3V core processors. Replacing the microprocessor may require reconfiguring a DIP switch to select the correct bus frequency/core frequency combination. Frequency selection is described in detail later in this section.

The VT82C595 system controller provides the Host/PCI bridge functions and controls transfers with the 64-bit memory data bus. The system includes 256 kilobytes of SRAM controlled by the system controller as a direct-mapped, write-through L2 cache to the L1 cache integrated into the microprocessor. The system supports synchronous, pipelined burst SRAM/DRAM for the L2 cache, providing 3-1-1-1 read/write cycles at 60 and 66 MHz on a cache hit.

The standard system memory configuration consists of 16 or 32 megabytes of SDRAM system memory. The system memory can be expanded to 256 megabytes.

3.2.1 PENTIUM MMX MICROPROCESSOR

The Pentium MMX microprocessor is software-compatible with earlier generation x86 microprocessors but provides significantly higher performance due to both higher processing speed and enhanced design (Figure 3-2.).

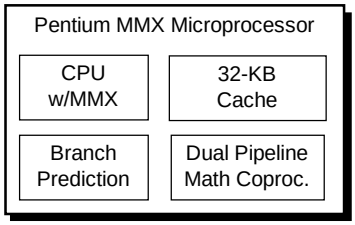


Figure 3–2. Pentium MMX Microprocessor Internal Architecture

The Pentium MMX microprocessor contains a dual-ALU CPU, branch prediction logic, dual-pipeline math coprocessor, and a 32-KB cache that is split into two 16-KB 4-way, set-associative caches for handling code and data separately. The microprocessor is mounted in a ZIF type 7 socket for easy changing/upgrading of the microprocessor. Replacing the microprocessor may require reconfiguring the settings of DIP switch SW1 to properly set the speed of the Host bus and the core (processing) frequencies.

3.2.1.1 MMX Technology

The CPU of the Pentium MMX supports 57 additional instructions specifically designed for accelerating multimedia and communications applications. Such applications often involve compute-intensive loops that can take up as much as 90 percent of CPU execution time. The MMX logic, using a parallel processing technique called Single Instruction-Multiple Data (SIMD), operates on 64 bits at a time. The MMX instructions are designed to take advantage of the dual-pipeline CPU as well as help the programmer in avoiding branches in code. Specific applications that benefit from MMX technology include 2D/3D graphics, audio, speech recognition, video codecs, and data compression .

> **NOTE:** MMX operations utilize a portion of the floating point registers of the integrated math coprocessor. Programmers should take note that mixing MMX code with that of floating point operations can result in reduced performance and should therefore be avoided.

.

3.2.2 BUS/PROCESSING SPEED SELECT

The Pentium MMX-based system board includes a four-position DIP switch (SW1) that is used to select the Host bus frequency and the processing frequency of the system. The SW1 positions 2 and 3 control the Bus Fraction (BF0, BF1) signals to the CPU, which determines the bus-to-core speed ratio. Position 5 of SW1 determines the bus frequency generated by the clock generator (refer to Chapter 4, "System Support" for more information on clock frequency generation). Table 3-2 shows the switch configurations to be used with a particular microprocessor.

Table 3-2.
Pentium MMX Microprocessor
Bus/Core Speed Switch (SW1) Settings

DIP SW1 Settings [1]			Microprocessor
2	3	5	Bus/Core Speed (in MHz)
Off	Off	Off	60/210
Off	Off	On	66/233
Off	On	Off	60/180
Off	On	On	66/200
On	Off	Off	60/120
On	Off	On	66/133
On	On	Off	60/150
On	On	On	66/166

NOTES:
Shipping configurations are unshaded

NOTE:
SW1 should be set to match the specified core speed of the microprocessor. Configuring for a core speed lower or higher than that for which the CPU is designed can result in unstable or possibly destructive operation.

The status of SW1-2, -3, and -5 is readable through general-purpose I/O (GPIO) port 78h bits <2..0>, allowing BIOS and/or diagnostic software to check an installed microprocessor with the switch configuration. Table 3-3 shows the switch position-to-GPIO-to-I/O port 78h input wiring.

Table 3-3.
SW1 Bus/Core Speed Positions
to GPIO Assignments

Switch Position	Signal Name	GPIO Number	I/O Port 78h
SW1-2	BF0	10	bit <0>
SW1-3	BF1	11	bit <1>
SW1-5	SPD66-	12	bit <2>

SPD = Bus frequency select BF = Bus/core fraction

3.2.3 SECONDARY (L2) CACHE MEMORY

The system board comes with 256 kilobytes of SRAM implemented as the secondary (L2) cache to the integrated L1 cache of the Pentium MMX microprocessor. This L2 cache uses two 32K x 32 synchronous pipelined burst SRAMs (with one 32K x 8 TAG RAM) arranged as a direct-mapped, write-back. The L2 cache provides a typical cycle time (in Host clocks) of 3-1-1-1 for burst reads (cache hit) and writes (write back). The L2 controller allows the full system memory range to be cached.

3.2.4 SYSTEM MEMORY

The system board contains two 168-pin DIMM sockets for system memory. This system is designed for using SDRAM DIMMs. As shipped from the factory the standard configuration may be 16 or 32 megabytes installed. The addition of 16-, or 32-, 64-, or 128-MB DIMMs allows the expansion of system memory up to a maximum of 256 megabytes. Single or double-sided DIMMs may be used. It is strongly recommended to use DIMMs with gold-plated contacts.

The system memory uses the following RAS line assignments:

RAS#0	DIMM 1, Bank A
RAS#1	DIMM 1, Bank B
RAS#2	DIMM 2, Bank A
RAS#3	DIMM 2, Bank B

This system does not use parity but does support ECC, and the memory is unbuffered. The performance times of the SDRAM is listed as follows:

Table 3-4.
SDRAM Performance Times

Parameter	CAS Latency = 2 CLKs
Burst Read Page Hit:	6-1-1-
Read Row Miss	8-1-1-1
Read Page Miss	10-1-1-1
Bk-to-Bk Burst Reads (Pg Hit)	6-1-1-1, 3-1-1-1
Write Page Hit	3
Write Row Miss	6
Write Page Miss	9
Posted Write	3-1-1-1

In addition to the supplied (and recommended) SDRAM, the system supports EDO and ECC RAM, with error logging/alerting supported. The RAM type (as well as other information) is detected during power-up by the system BIOS using the serial presence detect (SPD) method, which reads the EEPROM on each DIMM to obtain identification data such as the type and operating parameters. The supported format complies to the JEDEC specification for 128-byte EEPROMs. This system also provides support for 256-byte EEPROMs to include additional Compaq-added features such as the part number, serial number, and error logging. The SPD format as supported in this system is shown in Table 3-5.

Table 3-5.
SPD Address Map (SDRAM DIMM)

Byte	Description	Notes	Byte	Description	Notes
0	No. of Bytes Written Into EEPROM	[1]	62	SPD Revision	[7]
1	Total Bytes (#) In EEPROM	[2]	63	Checksum Bytes 0-62	
2	Memory Type		64-71	JEP-106E ID Code	[8]
3	No. of Row Addresses On DIMM	[3]	72	DIMM OEM Location	[8]
4	No. of Column Addresses On DIMM		73-90	OEM's Part Number	[8]
5	No. of Module Banks On DIMM		91, 92	OEM's Rev. Code	[8]
6, 7	Data Width of Module		93, 94	Manufacture Date	[8]
8	Voltage Interface Standard of DIMM		95-98	OEM's Assembly S/N	[8]
9	Cycletime @ Max CAS Latency (CL)	[4]	99-125	OEM Specific Data	[8]
10	Access From Clock	[4]	126, 127	Reserved	
11	Config. Type (Parity, Nonparity, etc.)		128-135	Sys. Integrator's ID	[9]
12	Refresh Rate/Type	[4] [5]	136-150	Sys. Integrator's P/N	[9]
13	Width, Primary DRAM		151-152	Sys. Integrator's D/C	[9]
14	Error Checking Data Width		153-165	Sys. Integrator's S/N	[9]
15	Min. Clock Delay	[6]	166	Chksm Bytes 128-165	[9]
16	Burst Lengths Supported		167-189	Top Level Sys. S/N	[9]
17	No. of Banks For Each Mem. Device	[4]	190-221	Avaiable for use	[9]
18	CAS Latencies Supported	[4]	222	Chksm Bytes 167-221	[9]
19	CS# Latency	[4]	223-253	Available for use	[9]
20	Write Latency	[4]	254	Chksm Bytes 223-253	[9]
21	DIMM Attributes		255	Chksm Byes 0-128	[9]
22	Memory Device Attributes				
23	Min. Clock Cycle Time at CL X-1	[7]			
24	Max. Acc. Time From CLK at CL X-1	[7]			
25	Min. Clock Cycle Time at CL X-2	[7]			
26	Max. Acc. Time From CLK at CL X-2	[7]			
27	Min. Row Precharge Time	[7]			
28	Min. Row Active To Row Active Delay	[7]			
29	Min. RAS to CAS Delay	[7]			
30, 31	Reserved				
32..61	Superset Data For Future Use				

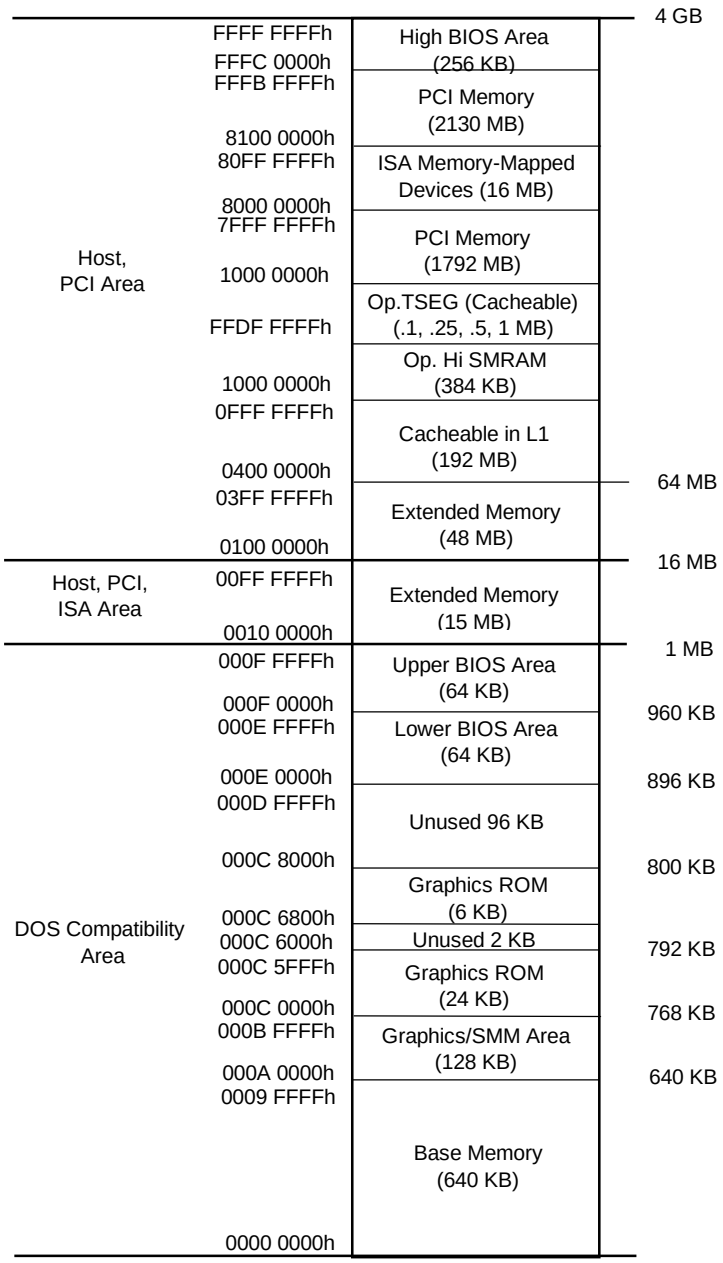
NOTES:

[1] Programmed as 128 bytes by the DIMM's OEM
[2] Must be programmed to 256 bytes.
[3] High order bit defines redundant addressing: if set (1), highest order RAS# address must be re-sent as highest order CAS# address.
[4] Refer to memory manufacturer's datasheet
[5] MSb is Self Refresh flag. If set (1), assembly supports self refresh.
[6] Back-to-back random column addresses.
[7] Field format proposed to JEDEC but not defined as standard at publication time.
[8] Field specified as optional by JEDEC but required by this system.
[9] Field format proposed to JEDEC. This system requires that the DIMM's EEPROM have this space available for reads/writes.

Access to the DIMM's EEPROM is through an I^2C-type bus interface using BIOS call INT 15, AX-E827h (discussed in Chapter 8, "BIOS ROM").

If the BIOS finds an installed module that is not supported then the memory controller is programmed to indicate empty rows as appropriate.

Figure 3-3 shows the system memory map.



NOTE: All locations in the 256 megabytes of system memory are cacheable in the L2 cache.

Figure 3–3. System Memory Map

3.2.5 SUBSYSTEM CONFIGURATION

The VT82C595 component provides the configuration function for the processor/memory subsystem. Table 3-6 lists the configuration registers used for setting and checking such parameters as cache (L2) control, system memory control, and PCI bus operation. These registers reside in the PCI Configuration Space and accessed using the methods described in Chapter 4, section 4.2.

Table 3-6.
Host/PCI Bridge Configuration Registers (VT82C595)

PCI Config. Addr.	Register	Reset Value	PCI Config. Addr.	Register	Reset Value
00, 01h	Vender ID	1106h	64h	DRAM Timing	ABh
02, 03h	Device ID	0595h	65h	DRAM Control Reg. 1	00h
04, 05h	Command	0007h	66h	DRAM Control Reg. 2	00h
06, 07h	Status		67h	DRAM Width	00h
08h	Revision ID		68h	UMA Control Reg. 1	00h
09-0Bh	Class Code		69h	UMA Control Reg. 2	00h
0Dh	Latency Timer	00h	6Ah	Refresh Control	00h
0Eh	Header Type	00h	6Bh	Misc. Cointrol	00h
0Fh	BIST (read only)		6Ch	SDRAM Control	
50h	Cache Control Reg. 1	00h	6Dh	DRAM Control Drive Strength	
51h	Cache Control Reg. 2	00h	6Eh	ECC Control Reg.	
52h	Non-Cacheable Control	02h	6Fh	ECC Status Reg.	
53h	Misc. Control	00h	70h	PCI Buffer Control	00h
54, 55h	Non-Cacheable Area 1	00h	71h	CPU-to-PCI Flow Cntl. Reg. 1	00h
56, 57h	Non-Cacheable Area 2	00h	72h	CPU-to-PCI Flow Cntl. Reg. 2	00h
58h	DRAM Configuration	40h	73h	PCI Master Control Reg.1	00h
59h	DRAM Configuration	05h	74h	PCI Master Control Reg. 2	00h
5A..5Fh	DRAM ROW End Addr.	01h	75h	PCI Arbitration	00h
60h	DRAM Type	00h	76h	Extension (PCI Arbitration)	00h
61..63h	Shadow RAM Control	00h	--	--	--

NOTE:
Refer to VIA Technologies, Inc. documentation for detailed description of registers.
Assume unmarked locations/gaps as reserved.

Chapter 4
SYSTEM SUPPORT

4.1 INTRODUCTION

This chapter covers subjects dealing with basic system architecture and covers the following topics:

This chapter covers functions provided by off-the-shelf chipsets and therefore describes only basic aspects of these functions as well as information unique to the Compaq Deskpro 4000 Personal Computers. For detailed information on specific components, refer to the applicable manufacturer's documentation.

4.2 PCI BUS OVERVIEW

NOTE: This section describes the PCI bus in general and highlights bus implementation in this particular system. For detailed information regarding PCI bus operation, refer to the *PCI Local Bus Specification Revision 2.1*.

This system implements a 32-bit Peripheral Component Interconnect (PCI) bus. The PCI bus uses a shared address/data bus design. On the first clock cycle of a PCI bus transaction the bus carries address information. On subsequent cycles, the bus carries data. PCI transactions occur synchronously with the Host bus at a rate of up to 33 MHz, depending on the speed of the microprocessor used. All I/O transactions involve the PCI bus. All ISA transactions involving the microprocessor, cache, and memory also involve the PCI bus. Memory cycles will involve the PCI if the access is initiated by a device or subsystem other than the microprocessor.

The PCI bus handles address/data transfers through the identification of devices and functions on the bus (Figure 4-1). A device is defined as a component or slot that resides on the PCI bus. A function is defined as the end source or target of the bus transaction. A device (component or slot) may contain one or more functions (i.e., in this system the PCI/ISA Bridge function, EIDE controller function, USB function, and ACPI function are contained within the South Bridge component).

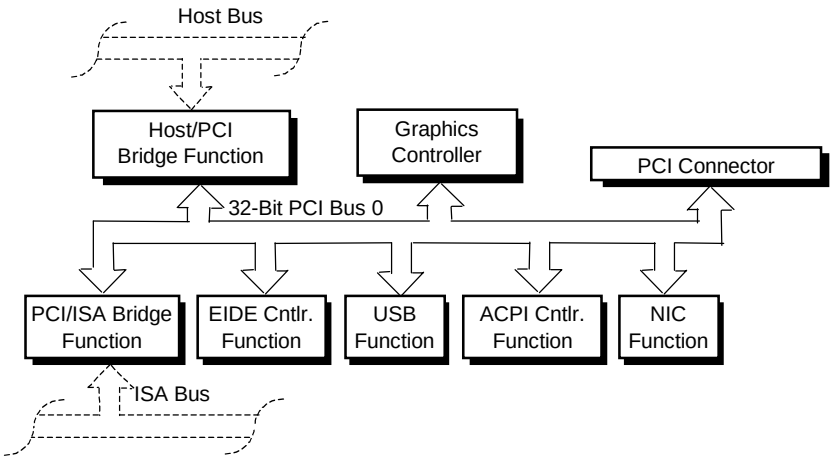
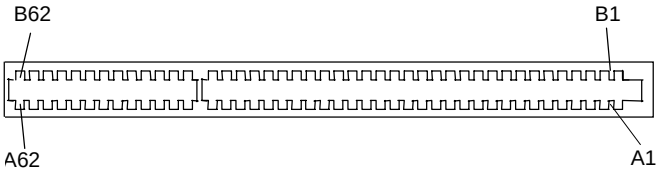


Figure 4–1. PCI Bus Devices and Functions

4.2.1 PCI CONNECTOR



NOTE: See caution below.

Figure 4–2. 32-Bit PCI Bus Connector (32-Bit Type)

Table 4-1.
PCI Bus Connector Pinout

Pin	B Signal	A Signal	Pin	B Signal	A Signal
01	-12 VDC	TRST-	32	AD17	AD16
02	TCK	+12 VDC	33	C/BE2-	+3.3 VDC
03	GND	TMS	34	GND	FRAME-
04	TDO	TDI	35	IRDY-	GND
05	+5 VDC	+5 VDC	36	+3.3 VDC	TRDY-
06	+5 VDC	INTA-	37	DEVSEL-	GND
07	INTB-	INTC-	38	GND	STOP-
08	INTD-	+5 VDC	39	LOCK-	+3.3 VDC
09	PRSNT1-	Reserved	40	PERR-	SDONE
10	RSVD	+5 VDC	41	+3.3 VDC	SBO-
11	PRSNT2-	Reserved	42	SERR-	GND
12	GND	GND	43	+3.3 VDC	PAR
13	GND	GND	44	C/BE1-	AD15
14	RSVD	Reserved	45	AD14	+3.3 VDC
15	GND	RST-	46	GND	AD13
16	CLK	+5 VDC	47	AD12	AD11
17	GND	GNT-	48	AD10	GND
18	REQ-	GND	49	GND	AD09
19	+5 VDC	Reserved	50	Key	Key
20	AD31	AD30	51	Key	Key
21	AD29	+3.3 VDC	52	AD08	C/BE0-
22	GND	AD28	53	AD07	+3.3 VDC
23	AD27	AD26	54	+3.3 VDC	AD06
24	AD25	GND	55	AD05	AD04
25	+3.3 VDC	AD24	56	AD03	GND
26	C/BE3-	IDSEL	57	GND	AD02
27	AD23	+3.3 VDC	58	AD01	AD00
28	GND	AD22	59	+5 VDC	+5 VDC
29	AD21	AD20	60	ACK64- [1]	REQ64- [1]
30	AD19	GND	61	+5 VDC	+5 VDC
31	+3.3 VDC	AD18	62	+5 VDC	+5 VDC
--	--	--	--	--	--

NOTE:

[1] The REQ64- and ACK64- signals are pulled high, allowing the use of 64-bit PCI cards in 32-bit mode.

CAUTION: The maximum length for an expansion card (PCI or ISA) installed in this system is 7 inches. Longer cards may be damaged or cause damage to the system.

4.2.2 PCI BUS MASTER ARBITRATION

The PCI bus supports a bus master/target arbitration scheme. A bus master is a device that has been granted control of the bus for the purpose of initiating a transaction. A target is a device that is the recipient of a transaction. Request (REQ), Grant (GNT), and FRAME signals are used by PCI bus masters for gaining access to the PCI bus. When a PCI device needs access to the PCI bus (and does not already own it), the PCI device asserts it's REQ*n* signal to the PCI bus arbiter (a function of the system controller component). If the bus is available, the arbiter asserts the GNT*n* signal to the requesting device, which then asserts FRAME and conducts the address phase of the transaction with a target. If the PCI device already owns the bus, a request is not needed and the device can simply assert FRAME and conduct the transaction. Table 4-1 shows the grant and request signals assignments for the devices on the PCI bus.

Table 4-2.
PCI Bus Mastering Devices

REQ/GNT Line	Device
REQ1/GNT1	PCI Connector
REQ2/GNT2	Graphics Controller
REQ3/GNT3	Network I/F Controller

PCI bus control is granted according to a Least Recently Used (LRU) algorithm. During times that the bus is not used or requested, bus control is given to the Host/PCI bridge. After a device has given up control of the bus or has not executed a transaction for 16 PCI clock cycles (PCICLKs) after gaining bus control, it loses access and is placed on the bottom of the priority list.

The PCI/ISA bridge is given special consideration. If the PCI/ISA bridge gains control of the PCI bus but does not execute a transaction after 16 PCICLKs, the PCI/ISA bridge retains ownership of the PCI bus until the current ISA bus master relinquishes the ISA bus. The PCI/ISA bridge is then placed on the bottom of the priority list.

PCI bus priority can be altered in two ways: by a master needing to perform a retry of a data cycle, or by the master locking the bus. When a master is retried, it releases the bus and negates its REQ*n*- line for a minimum of two PCICLKs and then requests the bus again. If the master is granted the bus before the condition that caused the retry is resolved, the master is retried again, which may result in bus "thrashing." Bus thrashing is minimized by masking the REQ*n*- line of a particular device that has had a transaction retried.

If a master locks the PCI bus, it retains top priority, allowing it to quickly finish a lock sequence. The PCI/ISA bridge cannot become master until the locking device unlocks the bus. Consequently, a master should not lock the bus for long periods of time or latency problems could occur.

4.2.3 PCI BUS TRANSACTIONS

The PCI bus consists of a 32-bit path (AD31-00 lines) that uses a multiplexed scheme for handling both address and data transfers. A bus transaction consists of an address cycle and one or more data cycles, with each cycle requiring a clock (PCICLK) cycle. High performance is realized during burst modes in which a transaction with contiguous memory locations requires that only one address cycle be conducted and subsequent data cycles are completed using auto-incremented addressing. Four types of address cycles can take place on the PCI bus; I/O, memory, configuration, and special. Address decoding is distributed (left up to each device on the PCI bus).

4.2.3.1 I/O and Memory Cycles

For I/O and memory cycles, a standard 32-bit address decode (AD31..0) for byte-level addressing is handled by the appropriate PCI device. For memory addressing, PCI devices decode the AD31..2 lines for dword-level addressing and check the AD1,0 lines for burst (linear-incrementing) mode. In burst mode, subsequent data phases are conducted a dword at a time with addressing assumed to increment accordingly (four bytes at a time).

4.2.3.2 Configuration Cycles

Devices on the PCI bus must comply with PCI protocol that allows configuration of that device by software. In this system, configuration mechanism #1 (as described in the PCI Local Bus specification Rev. 2.1) is employed. This method uses two 32-bit registers for initiating a configuration cycle for accessing the configuration space of a PCI device. The configuration address register (CONFIG_ADDRESS) at 0CF8h holds a value that specifies the PCI bus, PCI device, and specific register to be accessed. The configuration data register (CONFIG_DATA) at 0CFCh contains the configuration data.

PCI Configuration Address Register
I/O Port 0CF8h, R/W, (32-bit access only)

Bit	Function
31	Configuration Enable 0 = Disabled 1 = Enable
30..24	Reserved - read/write 0s
23..16	Bus Number. Selects PCI bus
15..11	PCI Device Number. Selects PCI device for access
10..8	Function Number. Selects function of selected PCI device.
7..2	Register Index. Specifies config. reg.
1,0	Configuration Cycle Type ID. 00 = Type 0 01 = Type 1

PCI Configuration Data Register
I/O Port 0CFCh, R/W, (8-, 16-, 32-bit access)

Bit	Function
31..0	Configuration Data.

Figure 4-3 shows how the loading of 0CF8h results in a Type 0 configuration cycle on the PCI bus. The Device Number (bits <15..11> determines which one of the AD31..11 lines is to be asserted high for the IDSEL signal, which acts as a "chip select" function for the PCI device to be configured.

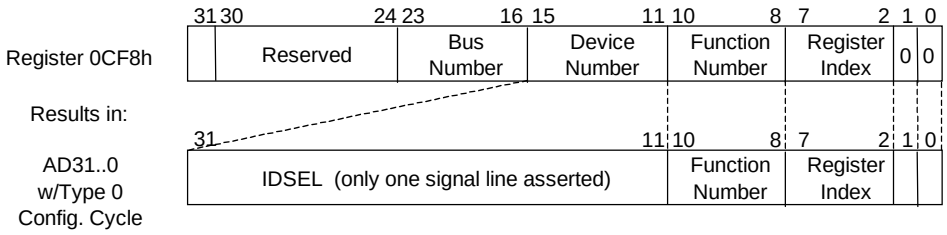


Figure 4–3. Type 0 Configuration Cycle

Type 0 configuration cycles are used for configuring devices on PCI bus # 0. Type 1 configuration cycles (reg. 0CF8h bits <1,0> = 01b) are passed on to PCI bus # 1 (if present). Table 4-3 shows the standard configuration of device numbers and IDSEL connections for components and slots residing on a PCI bus.

Table 4-3.
PCI Device Configuration Access

PCI Device	Device No. (CF8h <15..11>)	IDSEL Wired to:
North Bridge (82C595)	0	AD11
PCI Connector	2	AD13
South Bridge (82C586)	7	AD31
Graphics Controller	15	AD26
Network Interface Controller	16	AD27

The function number (CF8h, bits <10..8>) is used to select a particular function within a multifunction device as shown in Table 4-4.

Table 4-4.
PCI Function Configuration Access

PCI Function	Device No.	Function No.
Host/PCI Bridge	0	0
PCI/ISA Bridge	7	0
IDE Interface	7	1
USB Interface	7	2
ACPI Cntlr.	7	3
Graphics Controller	15	0
Network Interface Controller	16	0

The register index (CF8h, bits <7..2>)identifies the 32-bit location within the configuration space of the PCI device to be accessed. All PCI devices can contain up to 256 bytes of configuration data (see Figure 4-4), of which the first 64 bytes comprise the configuration space header.

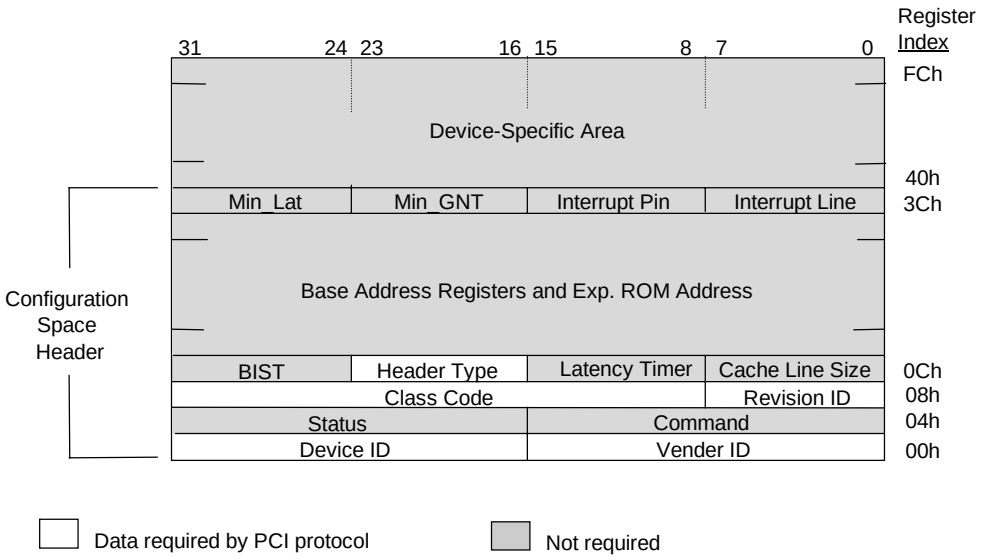


Figure 4–4. PCI Configuration Space Map

Each PCI device is identified with a vender ID (assigned to the vender by the PCI Special Interest Group) and a device ID (assigned by the vender). The device and vender IDs for the devices used in these systems are listed in Table 4-5.

Table 4-5.
PCI Device Identification

PCI Device	Vender ID	Device ID
VT82C595 (North Bridge)	1106h	0595h
VT82C586 (South Bridge):		
PCI/ISA Bridge (Function 0)	1106h	0586h
EIDE Controller (Function 1)	1106h	0571h
USB I/F (Function 2)	1106h	3038h
ACPI Cntlr (Function 3)	1106h	3040h
Network Interface Controller	0E11h	B011h
Graphics Controller	5333h	8901h

4.2.3.3 Special Cycles

There are two types of special cycles that may occur on the PCI bus. The first type is initiated by the host and is used to perform the following functions: Shutdown, Flush, Halt, Write Back, Flush Acknowledge, Branch Trace Message, and Stop/Grant. These cycles start like all other PCI cycles and terminate with a master abort.

The second type of special cycle is initiated by writing to 0CF8h, Bus # = all 0s, Device = all 1s, Function # all 1s, and Register = all 0s) and 0CFCh to generate a Type 0 configuration cycle. This type 0 cycle, however, does not assert any of the IDSEL lines and therefore results in a master abort with FFFFh returned to the microprocessor.

4.2.4 OPTION ROM MAPPING

During POST, the PCI bus is scanned for devices that contain their own specific firmware in ROM. Such option ROM data, if detected, is loaded into system memory's DOS compatibility area (refer to the system memory map shown in chapter 3).

4.2.5 PCI INTERRUPT MAPPING

The PCI bus provides for four interrupt signals; INTA-, INTB-, INTC-, and INTD-. These signals may be generated by on-board PCI devices or by devices installed in the PCI slots. In order to minimize latency, INTA-..INTD- signal routing from the PCI slot to the system board is distributed by the riser card (backplane) as shown below:

System Board	PCI Slot
INTA-	INTD-
INTB-	INTA- [1]
INTC-	INTB-
INTD-	INTC- [2]

NOTES:

[1] Shared with network interface controller

[2] Shared with graphic controller

Interrupts generated by PCI devices can be configured to share the standard AT (IRQn) interrupt lines. Two devices that share a single PCI interrupt must also share the corresponding AT interrupt. Example: If a PCI card is installed in slot 5 and wants to use INTA- then it must share INTA- as well as the corresponding AT interrupt with the on-board network interface controller.

Three PCI configuration registers of the 82C586 are used to route the INTA-..INTD- signals to the IRQn signal lines (refer to section 4.3.4.1 for information on IRQn routing). The power up (default) configuration has PCI interrupt redirection disabled.

PCI Configuration Register 55h, IRQ Routing Reg. 1

Default Value = 00h

Bit	Function
7..4	INTD- Routing: 0000 = Reserved 0001 = IRQ1 0010 = Reserved 0011 = IRQ3 0100 = IRQ4 0101 = IRQ5 0110 = IRQ6 0111 = IRQ7 1000 = Reserved 1001 = IRQ9 1010 = IRQ10 1011 = IRQ11 1100 = IRQ12 1101 = Reserved 1110 = IRQ14 1111 = IRQ15
3..0	MIRQ0- Routing (Same as PIRQD-)

PCI Configuration Register 56h, IRQ Routing Reg. 2

Default Value = 00h

Bit	Function
7..4	INTA- Routing: (Same as PIRQD-)
3..0	INTB- Routing (Same as PIRQD-)

PCI Configuration Register 57h, IRQ Routing Reg. 3

Default Value = 00h

Bit	Function
7..4	INTC- Routing: (Same as PIRQD-)
3..0	MIRQ1 Routing (Same as PIRQD-)

4.2.6 PCI CONFIGURATION

PCI bus operations, especially those that involve ISA bus interaction, require the configuration of certain parameters such as PCI IRQ routing, top of memory accessable by ISA, SMI generation, and clock throttling characteristics. These parameters are handled by the PCI/ISA bridge function (PCI function #0) of the South Bridge component and configured through the PCI configuration space registers listed in Table 4-6. Configuration is provided by BIOS at power-up but re-configurable by software .

Table 4-6.
PCI/ISA Bridge Configuration Registers
(VT82C586 Function 0)

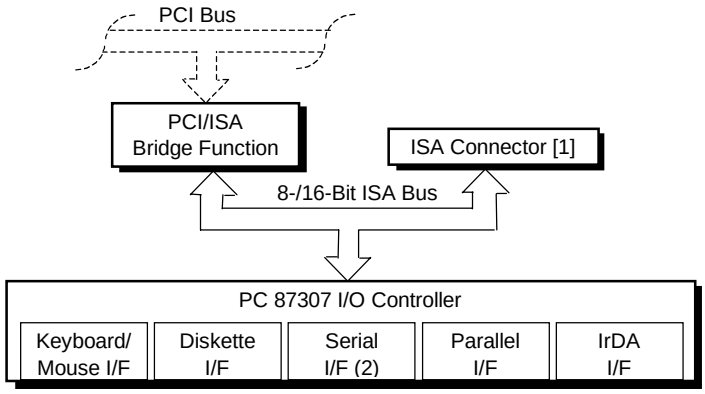
PCI Config. Addr.	Register	Reset Value	PCI Config. Addr.	Register	Reset Value
00, 01h	Vender ID	1106h	4C..4Eh	ISA DMA/Master Mem. Acc.	00h
02, 03h	Device ID	0586h	4Fh	ISA DMA/Master Mem. Acc.	03h
04, 05h	Command		50h	PnP DRQ Routing	24h
06, 07h	Status		54h	PCI Interrupt Polarity	00h
08h	Revision ID		55..57h	PCI Interrupt Routing	00h
09-0Bh	Class Code		80h	Primary Activity Detect En.	00h
0Eh	Header Type		82h	Primary Activity Detect Sts.	
40h	ISA Bus Control	00h	84, 85h	Reserved	
41h	Refresh & Port 92 Control	00h	86, 87h	Reserved	
42h	ISA Clock Control	00h	88..8Bh	Timer Control Registers	00h
43h	ROM Decoding Cntl.	00h	8Ch	Conserve Mode/Sec. Event	00h
44	Keyboard Controller Control	00h	8Dh	Miscellaneous Control	00h
45h	Type F DMA Control	00h	8Eh	STPCLK- Duty Cycle	00h
46, 47h	Misc. Control	00h	90..93h	ISA INT. As Primary Event	00h
48h	Misc. Control	01h	94h	Ext. SMI Pin Status	(RO)
4Ah	IDE Interrupt Routing	04h	95, 96h	Power-Up Strap Options	(RO)

NOTE: Assume unmarked locations/gaps as reserved.

4.3 ISA BUS OVERVIEW

NOTE: This section describes the ISA bus in general and highlights bus implementation in this particular system. For detailed information regarding ISA bus operation, refer to the *Compaq Extended Industry Standard Architecture (EISA) Technical Reference Guide*.

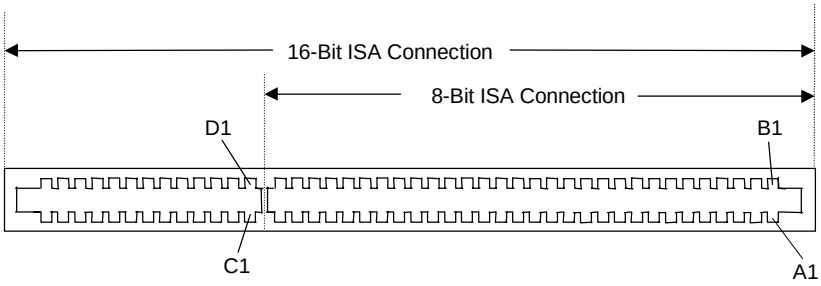
The industry standard architecture (ISA) bus provides an 8-/16-bit path for standard I/O peripherals as well as for an optional device that can be installed in the ISA expansion slot (if present). Figure 4-5 shows the key functions and devices that reside on the ISA bus.



NOTE:
[1] Deskpro 4000S only

Figure 4–5. ISA Bus Block Diagram

4.3.1 ISA CONNECTOR



NOTE: See caution below.

Figure 4–6. ISA Expansion Connector

Table 4-7.
ISA Expansion Connector Pinout

8-Bit ISA Interface				16-Bit ISA Interface			
Pin	**Signal**	**Pin**	**Signal**	**Pin**	**Signal**	**Pin**	**Signal**
B01	GND	A01	I/O CHK-	D01	M16-	C01	SBHE-
B02	RESDRV	A02	SD7	D02	I/O16-	C02	LA23
B03	+5 VDC	A03	SD6	D03	IRQ10	C03	LA22
B04	IRQ9	A04	SD5	D04	IRQ11	C04	LA21
B05	-5 VDC	A05	SD4	D05	IRQ12	C05	LA20
B06	DRQ2	A06	SD3	D06	IRQ15	C06	LA19
B07	-12 VDC	A07	SD2	D07	IRQ14	C07	LA18
B08	NOWS-	A08	SD1	D08	DAK0-	C08	LA17
B09	+12 VDC	A09	SD0	D09	DRQ0	C09	MRDC-
B10	GND	A10	BUSRDY	D10	DAK5-	C10	MWTC-
B11	SMWTC-	A11	DMA	D11	DRQ5	C11	SD8
B12	SMRDC-	A12	SA19	D12	DAK6-	C12	SD9
B13	IOWC-	A13	SA18	D13	DRQ6	C13	SD10
B14	IORC-	A14	SA17	D14	DAK7-	C14	SD11
B15	DAK3-	A15	SA16	D15	DRQ7	C15	SD12
B16	DRQ3	A16	SA15	D16	+5 VDC	C16	SD13
B17	DAK1	A17	SA14	D17	GRAB-	C17	SD14
B18	DRQ1	A18	SA13	D18	GND	C18	SD15
B19	REFRESH-	A19	SA12				
B20	BCLK	A20	SA11				
B21	IRQ7	A21	SA10				
B22	IRQ6	A22	SA9				
B23	IRQ5	A23	SA8				
B24	IRQ4	A24	SA7				
B25	IRQ3	A25	SA6				
B26	DAK2-	A26	SA5				
B27	T-C	A27	SA4				
B28	BALE	A28	SA3				
B29	+5 VDC	A29	SA2				
B30	OSC	A30	SA1				
B31	GND	A31	SA0				

CAUTION: The maximum length for an expansion card (PCI or ISA) installed in this system is 7 inches. Longer cards may be damaged or cause damage to the system.

4.3.2 ISA BUS TRANSACTIONS

The ISA bus supports 8- and 16-bit transfers at an 8-MHz rate. Devices limited to 8-bit transfers use the lower byte portion (data lines 7..0) while 16-bit transfers use the full bandwidth (data lines 15..0). Addressing is handled by two classifications of address signals: latched and latchable. Latched address signals (SA19..0) select the specific byte within the 1-MB section of memory defined by address lines LA23..17. Latchable address lines (LA23..17) provide a longer setup time for pre-chip selection or for pre-address decoding for high-speed memory and allow access to up to 16-MB of physical memory on the ISA bus. The SA19..17 signals have the same values as the LA19..17 signals for all memory cycles. The I/O cycles use only the SA15..0 signals.

The key control signals are described as follows:

- MRDC- (Memory Read Cycle): MRDC- is active on all ISA memory reads accessing memory from 000000h to FFFFFFh.
- SMEMR- (System Memory Read): SMEMR- is asserted by the PCI/ISA bridge to request an ISA memory device to drive data onto the data lines for accesses below one megabyte. SMEMR- is a delayed version of MRDC-.
- MWTC- (Memory Write Cycle): MWTC- is active on all ISA memory write cycles accessing memory from 000000h to FFFFFFh.
- SMEMW- (System Memory Write): SMEMW- is asserted by the PCI/ISA bridge to request an ISA memory device to accept data from the data lines for access below one megabyte. SMEMW- is a delayed version of MWTC-.
- IORC- (Input/Output Read Cycle): IORC- commands an ISA I/O device to drive data onto the data lines.
- IOWC- (Input/Output Write Cycle): IOWC- commands an ISA I/O device to accept data from the data lines.
- SBHE- (System Byte High Enable): SBHE- indicates that a byte is being transferred on the upper half (D15..8) of the data lines.
- SA0- (System Address Bit <0>): This bit is the complement of SBHE- and indicates that a byte is being transferred on the lower half (D7..0) of the data lines.
- M16- (16-bit Memory Cycle): M16- is asserted by 16-bit ISA devices to indicate 16-bit memory cycle capability.
- IO16- (16-bit I/O Cycle): IO16- is asserted by 16-bit ISA devices to indicate 16-bit I/O cycle transfer capability.

If the address on the SA lines is above one megabyte, SMRDC- and SMWTC- will not be active. The MRDC- and MWTC- signals are active for memory accesses up to 16 megabytes and can be used by any device that uses the full 16-bit ISA bus. To request a 16-bit transfer, a device asserts either the M16- (memory) or IO16- (I/O) signal when the device is addressed.

When another device (such as a DMA device or another bus master) takes control of the ISA, the Bus Address Latch Enable (BALE) signal is held active for the duration of the operation. As a result , signals LA23..17 are always enabled and must be held stable for the duration of each bus cycle.

When the address changes, devices on the bus may decode the latchable address (LA23..17) lines and then latch them. This arrangement allows devices to decode chip selects and M16- before the next cycle actually begins.

The following guidelines apply to optional ISA devices installed in the system:

- On bus lines that can be driven by a controller board, the driver should be able to sink a minimum of 20 ma at 0.5 VDC and source 2 ma at 3.75 VDC.
- On bus lines that are driven in the low direction only (open collector), the driver should be able to sink 20 ma at 0.5 VDC.
- The load on any logic line from a single bus slot should not exceed 2.0 ma in the low state (at 0.5 VDC) or 0.1 ma in the high state (at 3.75 VDC).
- The logic-high voltage at the bus ranges from 3.75 VDC to 5.5 VDC. The logic low voltage ranges from 0 VDC to 0.8 VDC.

4.3.3 DIRECT MEMORY ACCESS

Direct Memory Access (DMA) is a method by which an ISA device accesses system memory without involving the microprocessor. DMA is normally used to transfer blocks of data to or from an ISA I/O device. DMA reduces the amount of CPU interactions with memory, freeing the CPU for other processing tasks.

> **NOTE:** This section describes DMA in general. For detailed information regarding DMA operation, refer to the *Compaq Extended Industry Standard Architecture (EISA) Technical Reference Guide*. Note, however, that EISA enhancements as described in the referenced document are not supported in this (ISA only) system.

The South Bridge component includes the equivalent of two 8237 DMA controllers cascaded together to provide eight DMA channels. Table 4-8 lists the default configuration of the DMA channels.

Table 4-8.
Default DMA Channel Assignments

DMA Channel	Device ID
Controller 1 (byte transfers)	
0	Spare & ISA conn. pins D8, D9
1	Audio subsystem & ISA conn. pins B17, B18
2	Diskette drive & ISA conn. pins B6, B26
3	ECP LPT1 & ISA conn. pins B15, B16
Controller 2 (word transfers)	
4	Cascade for controller 1
5	Spare & ISA conn. pins D10, D11
6	Spare & ISA conn. pins D12, D13
7	Spare & ISA conn. pins. D14, D15

All channels in DMA controller 1 operate at a higher priority than those in controller 2. Note that channel 4 is not available for use other than its cascading function for controller 1. The DMA controller 2 can transfer words only on an even address boundary. The DMA controller and page register define a 24-bit address that allows data transfers within the address space of the CPU. The DMA controllers operate at 8 MHz.

The DMA logic is accessed through two types of I/O mapped registers; page registers and controller registers. The mapping is the same regardless of the support chipset used.

4.3.3.1 Page Registers

The DMA page register contains the eight most significant bits of the 24-bit address and works in conjunction with the DMA controllers to define the complete (24-bit)address for the DMA channels. Table 4-9 lists the page register port addresses.

Table 4-9.
DMA Page Register Addresses

DMA Channel	Page Register I/O Port
Controller 1 (byte transfers)	
Ch 0	087h
Ch 1	083h
Ch 2	081h
Ch 3	082h
Controller 2 (word transfers)	
Ch 4	n/a
Ch 5	08Bh
Ch 6	089h
Ch 7	08Ah
Refresh	08Fh [see note]

NOTE:
The DMA memory page register for the refresh channel must be programmed with 00h for proper operation.

The memory address is derived as follows:

24-Bit Address - Controller 1 (Byte Transfers)

8-Bit Page Register	8-Bit DMA Controller
A23..A16	A15..A00

24-Bit Address - Controller 2 (Word Transfers)

8-Bit Page Register	16-Bit DMA Controller
A23..A17	A16..A01, (A00 = 0)

Note that address line A16 from the DMA memory page register is disabled when DMA controller 2 is selected. Address line A00 is not connected to DMA controller 2 and is always 0 when word-length transfers are selected.

By not connecting A00, the following applies:

- The size of the the block of data that can be moved or addressed is measured in 16-bits (words) rather than 8-bits (bytes).
- The words must always be addressed on an even boundary.

DMA controller 1 can move up to 64 Kbytes of data per DMA transfer. DMA controller 2 can move up to 64 Kwords (128 Kbytes) of data per DMA transfer. Word DMA operations are only possible between 16-bit memory and 16-bit peripherals.

The RAM refresh is designed to perform a memory read cycle on each of the 512 row addresses in the DRAM memory space. Refresh operations are used to refresh memory on the 32-bit memory bus and the ISA bus. The refresh address is provided on lines SA00 through SA08. Address lines LA23..17, SA18,19 are driven low.

The remaining address lines are in an undefined state during the refresh cycle. The refresh operations are driven by a 69.799-KHz clock generated by Interval Timer 1, Counter 1. The refresh rate is 128 refresh cycles in 2.038 ms.

4.3.3.2 DMA Controller Registers

Table 4-10 lists the DMA Controller Registers and their I/O port addresses. Note that there is a set of registers for each DMA controller.

Table 4-10.
DMA Controller Registers

Register	Controller 1	Controller 2	R/W
Status	008h	0D0h	R
Command	008h	0D0h	W
Mode	00Bh	0D6h	W
Write Single Mask Bit	00Ah	0D4h	W
Write All Mask Bits	00Fh	0DEh	W
Software DRQx Request	009h	0D2h	W
Base and Current Address - Ch 0	000h	0C0h	W
Current Address - Ch 0	000h	0C0h	R
Base and Current Word Count - Ch 0	001h	0C2h	W
Current Word Count - Ch 0	001h	0C2h	R
Base and Current Address - Ch 1	002h	0C4h	W
Current Address - Ch 1	002h	0C4h	R
Base and Current Word Count - Ch 1	003h	0C6h	W
Current Word Count - Ch 1	003h	0C6h	R
Base and Current Address - Ch 2	004h	0C8h	W
Current Address - Ch 2	004h	0C8h	R
Base and Current Word Count - Ch 2	005h	0CAh	W
Current Word Count - Ch 2	005h	0CAh	R
Base and Current Address - Ch 3	006h	0CCh	W
Current Address - Ch 3	006h	0CCh	R
Base and Current Word Count - Ch 3	007h	0CEh	W
Current Word Count - Ch 3	007h	0CEh	R
Temporary (Command)	00Dh	0DAh	R
Reset Pointer Flip-Flop (Command)	00Ch	0D8h	W
Master Reset (Command)	00Dh	0DAh	W
Reset Mask Register (Command)	00Eh	0DCh	W

NOTE:
For a detailed description of the DMA registers, refer to the *Compaq EISA Technical Reference Guide*.

4.3.4 INTERRUPTS

The microprocessor uses two types of interrupts; maskable and nonmaskable. A maskable interrupt can be enabled or disabled within the microprocessor by the use of the STI and CLI instructions. A nonmaskable interrupt cannot be masked off within the microprocessor but may be inhibited by hardware or software means external to the microprocessor.

4.3.4.1 Maskable Interrupts

The maskable interrupt is a hardware-generated signal used by peripheral functions within the system to get the attention of the microprocessor. Peripheral functions produce a unique INTA-D (PCI) or IRQ0-15 (ISA) signal that is routed to interrupt processing logic that asserts the interrupt (INTR) input to the microprocessor. The microprocessor halts execution to determine the source of the interrupt and then services the peripheral as appropriate.

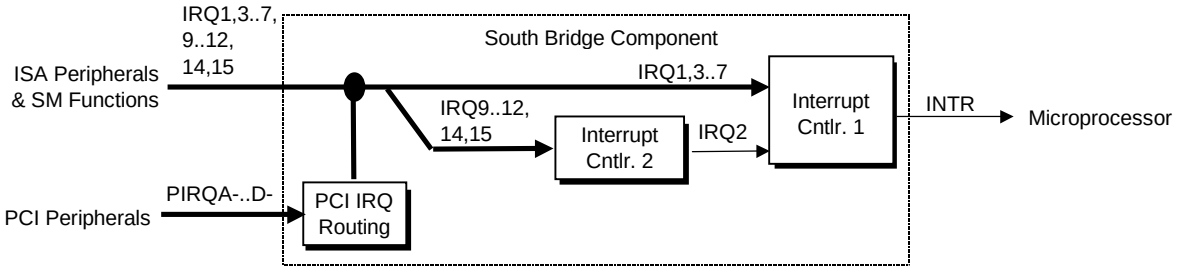


Figure 4–7. Maskable Interrupt Processing, Block Diagram

The South Bridge component, which includes the equivalent of two 8259 interrupt controllers cascaded together, handles the standard AT-type (ISA) interrupt signals (IRQn). The South Bridge also receives the PCI interrupt signals (PIRQA-..PIRQD-) from PCI devices. The PCI interrupts can be configured by PCI Configuration Registers 55h..57h to share the standard ISA interrupts (IRQn). The power-up default configuration has the PIRQn disabled. Table 4-11 lists the standard source configuration for maskable interrupts and their priorities. If more than one interrupt is pending, the highest priority (lowest number) is processed first.

Table 4-11.
Maskable Interrupt Priorities and Assignments

Priority	Signal Label	Source (Typical)	Notes
1	IRQ0	Interval timer 1, counter 0	
2	IRQ1	Keyboard	
3	IRQ8-	Real-time clock	
4	IRQ9	Spare and ISA connector pin B04	
5	IRQ10	Spare and ISA connector pin D03	
6	IRQ11	Spare and ISA connector pin D04	
7	IRQ12	Mouse and ISA connector pin D05	
8	IRQ13	Coprocessor (math)	
9	IRQ14	IDE primary I/F and ISA connector pin D07	
10	IRQ15	IDE secondary I/F and ISA connector pin D06	
11	IRQ3	Serial port (COM2) and ISA connector pin B25	
12	IRQ4	Serial port (COM1) and ISA connector pin B24	
13	IRQ5	Audio subsystem and ISA connector pin B23	
14	IRQ6	Diskette drive controller and ISA connector pin B22	
15	IRQ7	Parallel port (LPT1)	
--	IRQ2	NOT AVAILABLE (Cascade from interrupt controller 2)	

NOTE:

[3] Alternate available interrupts: IRQ5, 9,10,11,14, or 15

Interrupts generated by PCI devices can be configured to share the standard AT (IRQn) interrupt lines. Refer to section 4.2.5 “PCI Interrupt Mapping” for information on PCI interrupts.

Maskable Interrupt processing is controlled and monitored through standard AT-type I/O-mapped registers. These registers are listed in Table 4-12.

Table 4-12.
Maskable Interrupt Control Registers

I/O Port	Register
020h	Base Address, Int. Cntlr. 1
021h	Initialization Command Word 2-4, Int. Cntlr. 1
0A0h	Base Address, Int. Cntlr. 2
0A1h	Initialization Command Word 2-4, Int. Cntlr. 2

The initialization and operation of the interrupt control registers follows standard AT-type protocol.

4.3.4.2 Non-Maskable Interrupts

Non-maskble interrupts cannot be masked (inhibited) within the microprocessor itself but may be maskable by software using logic external to the microprocessor. There are two nonmaskable interrupt signals: the NMI- and the SMI-. These signals have service priority over all maskable interrupts, with the SMI- having top priority over all interrupts including the NMI-.

NMI- Generation

The Non-Maskable Interrupt (NMI-) signal can be generated by one of the following actions:

- Parity errors detected on the ISA bus (activating IOCHK-).
- Parity errors detected on a PCI bus (activating SERR- or PERR-).
- Microprocessor internal error (activating IERRA or IERRB)

The IOCHK-, SERR-, and PERR- signals are routed through the south bridge component, which in turn activates the NMI to the microprocessor.

The NMI Status Register at I/O port 061h contains NMI source and status data as follows:

NMI Status Register 61h

Bit	Function
7	NMI Status: 0 = No NMI from system board parity error. 1 = NMI requested, read only
6	IOCHK- NMI: 0 = No NMI from IOCHK- 1 = IOCHK- is active (low), NMI requested, read only
5	Interval Timer 1, Counter 2 (Speaker) Status
4	Refresh Indicator (toggles with every refresh)
3	IOCHK- NMI Enable/Disable: 0 = NMI from IOCHK- enabled 1 = NMI from IOCHK- disabled and cleared (R/W)
2	System Board Parity Error (PERR/SERR) NMI Enable: 0 = Parity error NMI enabled 1 = Parity error NMI disabled and cleared (R/W)
1	Speaker Data (R/W)
0	Inteval Timer 1, Counter 2 Gate Signal (R/W) 0 = Counter 2 disabled 1 = Counter 2 enabled

Functions not related to NMI activity.

After the active NMI has been processed, status bits <7> or <6> are cleared by pulsing bits <2> or <3> respectively.

The NMI Enable Register (070h, <7>) is used to enable/disable the NMI signal. Writing 80h to this register masks generation of the NMI-. Note that the lower six bits of register at I/O port 70h affect RTC operation and should be considered when changing NMI- generation status.

SMI- Generation

The SMI- (System Management Interrupt) is typically used for power management functions. When power management is enabled, inactivity timers are monitored. When a timer times out, SMI- is asserted and invokes the microprocessor's SMI handler. The SMI- handler works with the APM BIOS to service the SMI- according to the cause of the timeout.

Although the SMI- is primarily used for power managment the interrupt is also employed for the QuickLock/QuickBlank functions as well.

4.3.5 INTERVAL TIMER

The interval timer generates pulses at software (programmable) intervals. A 8254-compatible timer is integrated into the South Bridge chip. The timer function provides three counters, the functions of which are listed in Table 4-13.

Table 4-13.
Interval Timer Functions

Counter	Function	Gate	Clock In	Clock Out
0	System Clock	Always on	1.193 MHz	IRQ0
1	Refresh	Always on	1.193 MHz	Refresh Req.
2	Speaker Tone	Port 61, bit<0>	1.193 MHz	Speaker Input

The interval timer is controlled through the I/O mapped registers listed in Table 4-14.

Table 4-14.
Interval Timer Control Registers

I/O Port	Register
040h	Read or write value, counter 0
041h	Read or write value, counter 1
042h	Read or write value, counter 2
043h	Control Word

Interval timer operation follows standard AT-type protocol. For a detailed description of timer registers and operation, refer to the *Compaq Extended Industry Standard Architecture Expansion Bus Technical Reference Guide.*

4.3.6 ISA CONFIGURATION

The working relationship between the PCI and ISA buses requires that certain parameters be configured. The PC/ISA bridge function of the South Bridge component includes configuration registers to set parameters such as PCI IRQ routing and top-of-memory available to ISA/DMA devices. These parameters are programmed by BIOS during power-up, using registers listed previously in Table 4-6.

4.4 SYSTEM CLOCK DISTRIBUTION

The system uses an ICS9147-08 or compatible part for generation of most clock signals. Tables 4-15 lists the clock signals and to which components they are distributed.

Table 4-15.
Clock Generation and Distribution

Signal	Frequency	Source	Destination
CPUCLK	60/66 MHz [1]	ICS9147	CPU, VT82C595
CACHE_CLKn	CPUCLK	"	L2 SRAMs
DIMMn_CLKn	CPUCLK	"	DIMMs
PCICLK	CPUCLK/2	"	PCI slots
LRU_CLK	CPUCLK/2	"	Compaq ASIC
TLAN_CLK	CPUCLK/2	"	TLAN ASIC
PCI Bridge Clock	CPUCLK/2	"	VT82C595, VT82C586
SIO/USB CLK	48 MHz	"	87307, VT82C586
PHYCLK	25 MHz	Crystal	LXT970
TLAN	20 MHz	"	TLAN ASIC
Crystal CLK	14.318 MHz	Crystal	ICS9147
CLK_14	14 MHz	ICS9147 [2]	ISA bus, VT82C586, ESS1868
BCLK	PCICLK/4 [3]	VT82C586	ISA bus

NOTES:

[1] Depending on speed configuration (refer to Chapter 3, "Processor/Memory Subsystem").
[2] Routed through buffer before destination.
[3] 8.33 MHz if PCICLK = 33 MHz, 7.5 MHz if PCICLK = 30 MHz

4.5 REAL-TIME CLOCK AND CONFIGURATION MEMORY

The Real-time clock (RTC) and configuration memory functions are provided by the PC87307 I/O controller. The RTC uses the first 14 of 256 bytes of configuration memory and is MC146818-compatible. As shown in the following figure, the 87307 controller provides 256 bytes of configuration memory, divided into two 128-byte banks. The RTC/configuration memory can be accessed using conventional OUT and IN assembly language instructions using I/O ports 70h/71h, although the suggested method is to use the INT15 AX=E823h BIOS call.

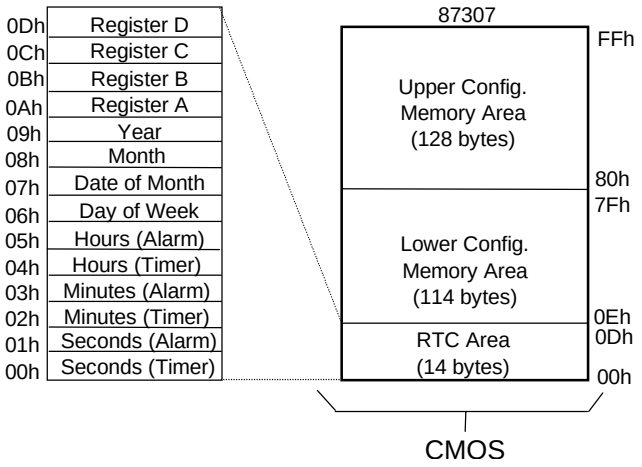


Figure 4–8. Configuration Memory Map

NOTE: Non-volatile (NVRAM) storage of PCI, ESCD, and Environmental Variable (EV) data is provided by portions of the 256-KB system BIOS ROM component.

A 3-VDC battery is used for maintaining the RTC and configuration memory while the system is powered down. This battery is soldered on the system board and is designed to last from 5-7 years. Once expired, the soldered battery is by-passed by connecting a replacement battery (Compaq p/n 160274-001 or equivalent 4.5 VDC @ 660 ma alkaline battery) to header P14 pins 9-12. On-board logic regulates the external battery voltage to 3 VDC.

The configuration memory (including the password) can be cleared by moving the jumper from P14 pins 1 and 2 to pins 2 and 3 for at least one minute while unit power ids off. The password can be disabled by switching DIP SW1-1 on.

4.5.1 CONFIGURATION MEMORY BYTE DEFINITIONS

Table 4-16 lists the mapping of the configuration memory.

Table 4-16.
Configuration Memory (CMOS) Map

Location	Function	Location	Function
00-0Dh	Real-rime clock	41h-44h	Hoof Removal Time Stamp
0Eh	Diagnostic status	45h	Keyboard snoop byte
0Fh	System reset code	46h	Diskette drive status
10h	Diskette drive type	47h	Last IPL device
11h	Reserved	48h-4Bh	IPL priority
12h	Hard drive type	4Ch-4Fh	BVC priority
13h	Security functions	51h	ECC DIMM status
14h	Equipment installed	52h	Board revision (from boot block)
15h	Base memory size, low byte/KB	53h	SWSMI command
16h	Base memory size, high byte/KB	54h	SWSMI data
17h	Extended memory, low byte/KB	55h	APM command
18h	Extended memory, high byte/KB	56h	Erase-Ease keyboard byte
19h	Hard drive 1, primary controller	57h-76H	Saved CMOS location 10h-2Fh
1Ah	Hard drive 2, primary controller	77h-7Fh	Administrator password
1Bh	Hard drive 1, secondary controller	80h	ECMOS diagnostic byte
1Ch	Hard drive 2, secondary controller	81h-82h	Total super ext. memory tested good
1Dh	Enhanced hard drive support	83h	Microprocessor chip ID
1Eh	Reserved	84h	Microprocessor chip revision
1Fh	Power management functions	85h	Hood removal status byte
24h	System board ID	86h	Fast boot date
25h	System architecture data	87h	Fast boot status byte
26h	Auxiliary peripheral configuration	8Dh-8Fh	POST error logging
27h	Speed control external drive	90h-91h	Total super extended memory configured
28h	Expanded/base mem. size, IRQ12	92h	Miscellaneous configuration byte
29h	Miscellaneous configuration	93h	Miscellaneous PCI features
2Ah	Hard drive timeout	94h	ROM flash/power button status
2Bh	System inactivity timeout	97h	Asset/test prompt byte
2Ch	Monitor timeout, Num Lock Cntrl	9Bh	Ultra-33 DMA enable byte
2Dh	Additional flags	9Ch	Mode-2 Configuration
2Eh-2Fh	Checksum of locations 10h-2Dh	9Dh	ESS audio configuration
30h-31h	Total extended memory tested	9Eh	ECP DMA configuration
32h	Century	9Fh-AFh	Serial number
33h	Miscellaneous flags set by BIOS	B0h-C3h	Custom drive types 65, 66, 68, 15
34h	International language	C7h	Serial port 1 address
35h	APM status flags	C8h	Serial port 2 address
36h	ECC POST test single bit	C9h	COM1/COM2 port configuration
37h-3Fh	Power-on password	DEh-DFh	Checksum of locations 90h to DDh
40h	Miscellaneous Disk Bits	E0h-FFh	Client Management error log

NOTE: Assume unmarked gaps are reserved.

Default values (where applicable) are given for a standard system as shipped from the factory. The contents of configuration memory can be cleared by the following jumper positioning:

RTC using internal battery:

Move jumper on header E50 from pins 1 and 2 to pins 2 and 3.

RTC using external battery:

Move jumper on header E50 from pins 2 and 3 to pins 1 and 2.

RTC Control Register A, Byte 0Ah

Bit	Function
7	Update in Progress. Read only. 0 = Time update will not occur before 2444 us 1 = Time update will occur within 2444 us
6..4	Divider Chain Control. R/W. 00x = Oscillator disabled. 010 = Normal operation (time base frequency = 32.768 KHz). 11x = Divider chain reset.
3..0	Periodic Interrupt Control. R/W. Specifies the periodic interrupt interval. 0000 = none 1000 = 3.90625 ms 0001 = 3.90625 ms 1001 = 7.8125 ms 0010 = 7.8125 ms 1010 = 15. 625 ms 0011 = 122.070 us 1011 = 31.25 ms 0100 = 244.141 us 1100 = 62.50 ms 0101 = 488.281 us 1101 = 125 ms 0110 = 976.562 us 1110 = 250 ms 0111 = 1.953125 ms 1111 = 500 ms

RTC Control Register B, Byte 0Bh

Bit	Function
7	Time Update Enable/disable 0 = Normal operation, 1 = Disable time updating for time set
6	Periodic Interrupt Enable/Disable. 0 = Disable, 1 = Enable interval specified by Register A
5	Alarm Interrupt Enable/disable 0 = Disabled, 1 = Enabled
4	End-of-Update Interrupt Enable/Disable 0 = Disabled, 1 = Enabled
3	Reserved (read 0)
2	Time/Date Format Select 0 = BCD format, 1 = Binary format
1	Time Mode 0 = 12-lhour mode, 1 = 24-hour mode
0	Automatic Daylight Savings Time Enable/Disable 0 = Disable 1 = Enable (Advance 1 hour on 1st Sunday in April, retreat 1 hour on last Sunday in October).

RTC Status Register C, Byte 0Ch

Bit	Function
7	If set, interrupt output signal active (read only)
6	If set, indicates periodic interrupt flag
5	If set, indicates alarm interrupt
4	If set, indicates end-of-update interrupt
3..0	Reserved

RTC Status Register D, Byte 0Dh

Bit	Function
7	RTC Power Status 0 = RTC has lost power 1 = RTC has not lost power
6..0	Reserved

Configuration Byte 0Eh, Diagnostic Status

Default Value = 00h

This byte contains diagnostic status data.

Configuration Byte 0Fh, System Reset Code

Default Value = 00h

This byte contains the system reset code.

Configuration Byte 10h, Diskette Drive Type

Bit	Function
7..4	Primary (Drive A) Diskette Drive Type
3..0	Secondary (Drive B) Diskette Drive Type

Valid values for bits <7..4> and bits <3..0>:

0000 = Not installed
0001 = 360-KB drive
0010 = 1.2-MB drive
0011 = 720-KB drive
0100 = 1.44-MB/1.25-MB drive
0110 = 2.88-MB drive
(all other values reserved)

Configuration Byte 12h, Hard Drive Type

Bit	Function
7..4	Primary Controller 1, Hard Drive 1 Type: 0000 = none 1000 = Type 8 0001 = Type 1 1001 = Type 9 0010 = Type 2 1010 = Type 10 0011 = Type 3 1011 = Type 11 0100 = Type 4 1100 = Type 12 0101 = Type 5 1101 = Type 13 0110 = Type 6 1110 = Type 14 0111 = Type 7 1111 = other (use bytes 19h)
3..0	Primary Controller 1, Hard Drive 2 Type: 0000 = none 1000 = Type 8 0001 = Type 1 1001 = Type 9 0010 = Type 2 1010 = Type 10 0011 = Type 3 1011 = Type 11 0100 = Type 4 1100 = Type 12 0101 = Type 5 1101 = Type 13 0110 = Type 6 1110 = Type 14 0111 = Type 7 1111 = other (use bytes 1Ah)

Configuration Byte 13h, Security Functions

Default Value = 00h

Bit	Function
7	Reserved
6	QuickBlank Enable After Standby: 0 = Disable 1 = Enable
5	Administrator Password: 0 = Not present 1 = Present
4	Reserved
3	Diskette Boot Enable: 0 = Enable 1 = Disable
2	QuickLock Enable: 0 = Disable 1 = Enable
1	Network Server Mode/Security Lock Override: 0 = Disable 1 = Enable
0	Password State (Set by BIOS at Power-up) 0 = Not set 1 = Set

Configuration Byte 14h, Equipment Installed

Default Value (standard configuration) = 03h

Bit	Function
7,6	No. of Diskette Drives Installed: 00 = 1 drive 10 = 3 drives 01 = 2 drives 11 = 4 drives
5..2	Reserved
1	Coprocessor Present 0 = Coprocessor not installed 1 = Coprocessor installed
0	Diskette Drives Present 0 = No diskette drives installed 1 = Diskette drive(s) installed

Configuration Bytes 15h and 16h, Base Memory Size

Default Value = 280h

Bytes 15h and 16h hold a 16-bit value that specifies the base memory size in increments of 1-KB (1024) bytes. Valid base memory sizes are 512-KB and 640-KB.

Configuration Bytes 17h and 18h, Extended Memory Size

Bytes 17h and 18h hold a 16-bit value that specifies the extended memory size in increments of 1-KB (1024) bytes.

Configuration Bytes 19h-1Ch, Hard Drive Types

Byte 19h contains the hard drive type for drive 1 of the primary controller if byte 12h bits <7..4> hold 1111b. Byte 1Ah contains the hard drive type for drive 2 of the primary controller if byte 12h bits <3..0> hold 1111b. Bytes1Bh and 1Ch contain the hard drive types for hard drives 1 and 2 of the secondary controller.

Configuration Byte 1Dh, Enhanced IDE Hard Drive Support

Default Value = F0h

Bit	Function
7	EIDE - Drive C (83h)
6	EIDE - Drive D (82h)
5	EIDE - Drive E (81h)
4	EIDE - Drive F (80h)
3..0	Reserved

Values for bits <7..4> :

0 = Disable

1 = Enable for auto-configure

Configuration Byte 1Fh, Power Management Functions

Default Value = 00h

Bit	Function
7..4	Reserved
3	Slow Processor Clock for Low Power Mode 0 = Processor runs at full speed 1 = Processor runs at slow speed
2	Reserved
1	Monitor Off Mode 0 = Turn monitor power off after 45 minutes in standby 1 = Leave monitor power on
0	Energy Saver Mode Indicator (Blinking LED) 0 = Disable 1 = Enable

Configuration Byte 24h, System Board Identification

Default Value = 7Eh

Configuration memory location 24h holds the system board ID.

Configuration Byte 25h, System Architecture Data

Default Value = 0Bh

Bit	Function
7..4	Reserved
3	Unmapping of ROM: 0 = Allowed 1 = Not allowed
2	Reserved
1,0	Diagnostic Status Byte Address 00 = Memory locations 80C00000h-80C00004h 01 = I/O ports 878h-87Ch 11 = neither place

Configuration Byte 26h, Auxiliary Peripheral Configuration

Default Value = 00h

Bit	Function
7,6	I/O Delay Select 00 = 420 ns (default) 01 = 300 ns 10 = 2600 ns 11 = 540 ns
5	Alternative A20 Switching 0 = Disable port 92 mode 1 = Enable port 92 mode
4	Bi-directional Print Port Mode 0 = Disabled 1 = Enabled
3	Graphics Type 0 = Color 1 = Monochrome
2	Hard Drive Primary/Secondary Address Select: 0 = Primary 1 = Secondary
1	Diskette I/O Port 0 = Primary 1 = Secondary
0	Diskette I/O Port Enable 0 = Primary 1 = Secondary

Configuration Byte 27h, Speed Control/External Drive

Default Value = 00h

Bit	Function
7	Boot Speed 0 = Max MHz 1 = Fast speed
6..0	Reserved

Configuration Byte 28h, Expanded and Base Memory, IRQ12 Select

Default Value = 00h

Bit	Function
7	IRQ12 Select 0 = Mouse 1 = Expansion bus
6,5	Base Memory Size: 00 = 640 KB 01 = 512 KB 10 = 256 KB 11 = Invalid
4..0	Internal Compaq Memory: 00000 = None 00001 = 512 KB 00010 = 1 MB 00011 = 1.5 MB . . 11111 = 15.5 MB

Configuration Byte 29h, Miscellaneous Configuration Data

Default Value = 00h

Bit	Function
7..5	Reserved
4	Primary Hard Drive Enable (Non-PCI IDE Controllers) 0 = Disable 1 = Enable
3..0	Reserved

Configuration Byte 2Ah, Hard Drive Timeout

Default Value = 02h

Bit	Function
7..5	Reserved
4..0	Hard Drive Timeout 00000 = Disabled 00001 = 1 minute 00010 = 2 minutes . . 10101 = 21 minutes

Configuration Byte 2Bh, System Inactivity Timeout

Default Value = 23h

Bit	Function
7	Reserved
6,5	Power Conservation Boot 00 = Reserved 01 = PC on 10 = PC off 11 = Reserved
4..0	System Inactive Timeout. (Index to SIT system timeout record) 00000 = Disabled

Configuration Byte 2Ch, ScreenSave and NUMLOCK Control

Default Value = 00h

Bit	Function
7	Reserved
6	Numlock Control 0 = Numlock off at power on 1 = Numlock on at power on
5	Screen Blank Control: 0 = No screen blank 1 = Screen blank w/QuickLock
4..0	ScreenSave Timeout. (Index to SIT monitor timeout record) 000000 = Disabled

Configuration Byte 2Dh, Additional Flags

Default Value = 00h

Bit	Function
7..5	Reserved
4	Memory Test 0 = Test memory on power up only 1 = Test memory on warm boot
3	POST Error Handling (BIOS Defined) 0 = Display “Press F1 to Continue” on error 1 = Skip F1 message
2..0	Reserved

Configuration Byte 2Eh, 2Fh, Checksum

These bytes hold the checksum of bytes 10h to 2Dh.

Configuration Byte 30h, 31h, Total Extended Memory Tested

This location holds the amount of system memory that checked good during the POST.

Configuration Byte 32h, Century

This location holds the Century value in a binary coded decimal (BCD) format.

Configuration Byte 33h, Miscellaneous Flags

Default Value = 80h

Bit	Function
7	Memory Above 640 KB 0 = No, 1 = Yes
6	Reserved
5	Weitek Numeric Coprocessor Present: 0 = Not installed, 1 = Installed
4	Standard Numeric Coprocessor Present: 0 = Not installed, 1 = Installed
3..0	Reserved

Configuration Byte 34h, International Language Support

Default Value = 00h

Configuration Byte 35h, APM Status Flags

Default Value = 11h

Bit	Function
7..6	Power Conservation State: 00 = Ready 01 = Standby 10 = Suspend 11 = Off
5,4	Reserved
3	32-bit Connection: 0 = Disconnected, 1 = Connected
2	16-bit Connection 0 = Disconnected, 1 = Connected
1	Real Mode Connection 0 = Disconnected, 1 = Connected
0	Power Management Enable: 0 = Disabled 1 = Enabled

Configuration Byte 36h, ECC POST Test Single Bit Errors

Default Value = 01h

Bit	Function
7	Row 7 Error Detect
6	Row 6 Error Detect
5	Row 5 Error Detect
4	Row 4 Error Detect
3	Row 3 Error Detect
2	Row 2 Error Detect
1	Row 1 Error Detect
0	Row 0 Error Detect

0 = No single bit error detected.
1 = Single bit error detected.

Configuration Byte 37h-3Fh, Power-On Password

These eight locations hold the power-on password.

Configuration Byte 40h, Miscellaneous Disk Data

Configuration Bytes 41h-44h, Hood Removal Time Stamp

These four bytes record the time at which the hood of the system was removed:
Byte 41h, month & day
Byte 42h, year and month
Byte 43h, minutes and seconds
Byte 44h, removal flag and minutes

Configuration Byte 45h, Keyboard Snoop Data

Default Value = xxh

Bit	Function
7	Cntrl/F10 Key Status: 0 = Cntrl & F10 keys not pressed 1 = Cntrl & F10 keys pressed
6	F10 Key Status: 0 = F10 key not pressed 1 = F10 key pressed
5..1	Reserved
0	Key Pressed Flag: 0 = Key not pressed 1 = Key pressed

Configuration Byte 46h, Diskette/Hard Drive Status

Default Value = xxh

Bit	Function
7,6	Reserved
5	Partition On HD: 0 = Not set, 1 = Set
4	Setup Disk: 0 = Not present, 1 = Present
3	ROMPAQ or DIAGS Diskette: 0 = Not present, 1 = Present
2	Boot Diskette in Drive A: 0 = No, 1 = Yes
1	Drive B: Present: 0 = Not present, 1 = Present
0	Drive A: Present: 0 = Not present, 1 = Present

Configuration Bytes 47h-4Fh, IPL Data

These bytes hold initial program load (IPL) data for boot purposes:
Byte 47h, last IPL device
Bytes 48h-4Bh, IPL priority
Byte 4Ch-4Fh, BCV priority

Configuration Byte 51h, ECC Status Byte

Default Value = xxh

Bit	Function
7	ECC Status for DIMM 3
6	ECC Status for DIMM 2
5	ECC Status for DIMM 1
4	ECC Status for DIMM 0
3..0	Reserved

Configuration Byte 52h, Board Revision

This byte holds the board revision as copied from the boot block sector.

Configuration Byte 53h, 54h, SW SMI Command/Data Bytes

Configuration Byte 55h, APM Command Byte

Configuration Byte 56h, Miscellaneous Flags Byte

Bit	Function
7	CAS Latency: 0 = 2, 1 = 3
6	IR Port Enable Flag: 0 = Disabled (COM2 config. for standard serial port) 1 = Enabled (COM2 config. for IrDA)
5	Warm Boot Enable Flag: 0 = Disable, 1 = Enable
4	POST Terse/Verbose Mode 0 = Verbose, 1 = Terse
3..1	Erase Ease Keyboard Mode: 000 = Backspace/Spacebar 001 = Spacebar/Backspace 010 = Spacebar/Spacebar 011-111 = Invalid
0	Configurable Power Supply: 0 = Power switch active 1 = Power switch inhibited

Configuration Byte 57h-76h, CMOS Copy

Configuration Bytes 77h-7Fh, Administrator Password

Configuration Byte 80h, CMOS Diagnostic Flags Byte

Default Value = 00h. Set bit indicates function is valid.

Bit	Function
7	CMOS Initialization (Set CMOS to Default)
6	Setup password locked
5	PnP should not reject SETs because Diags is active
4	Reserved
3	Manufacturing diagnostics diskette found
2	Invalid electronic serial number
1	Boot maintenance partition once
0	Invalid CMOS checksum

Configuration Byte 81h, 82h, Total Super Extended Memory Tested

This byte holds the value of the amount of extended system memory that tested good during POST. The amount is given in 64-KB increments.

Configuration Byte 83h, Microprocessor Identification

This byte holds the component ID and chip revision of the microprocessor.

Configuration Byte 84h, Microprocessor Revision

Configuration Byte 85h, Hood Lock/Administration Mode

Bit	Function
7,6	Reserved
5	ESCD Buffering: 0 = No buffering, 1 = ESCD buffered at F000h.
4	Hood Lock Enable: 0 = Disabled, 1 = Enabled
3	User Mode Flag
2	Administration Mode Flag
1	Level Support: 0 = Level 1, 1 = Level 2
0	Feature Support Bit 0 = Disabled, 1 = Enabled

Configuration Byte 86h, Fast Boot Date

Configuration Byte 87h, Fast Boot Select

Bit	Function
7..3	
2	
1	
0	

Configuration Byte 88h, Fast Boot Date (Year/Century)

Configuration Byte 89h, APM Resume Timer

Bit <7> indicates the timer status: 0 = disabled, 1 = timer set.

Configuration Byte 8Ah-8Fh, APM Resume Timer

These bytes hold the APM timer values:
Byte 8Ah, minutes
Byte 8Bh, hours
Byte 8Ch, day
Byte 8Dh, month
Byte 8Eh, year
Byte 8Fh, century

Configuration Byte 90h, 91h, Total Super Extended Memory Configured

This byte holds the value of the amount of extended system memory that is configured. The amount is given in 64-KB increments.

Configuration Byte 92h, Miscellaneous Configuration Byte

Default Value = 18h

Bit	Function
7..5	Reserved
4	Diskette Write Control: 0 = Disable 1 = Enable
3..1	Reserved
0	Diskette Drive Swap Control: 0 = Don't swap 1 = Swap drive A: and B:

Configuration Byte 93h, PCI Configuration Byte

Default Value = 00h

Bit	Function
7	Onboard SCSI Status: 0 = Hidden 1 = Active
6	Onboard NIC Status: 0 = Hidden 1 = Active
5	Onboard USB Status: 0 = Hidden 1 = Active
3	Reserved
2	ISA Passive Release: 0 = Enabled 1 = Disabled
1	PCI Bus Master Enable 0 = Enabled 1 = Disabled
0	PCI VGA Palette Snoop 0 = Disable 1 = Enable

If palette snooping is enabled, then a primary PCI graphics card may share a common palette with the ISA graphics card. Palette snooping should only be enabled if all of the following conditions are met:

- An ISA card connects to a PCI graphics card through the VESA connector.
- The ISA card is connected to a color monitor.
- The ISA card uses the RAMDAC on the PCI card
- The palette snooping feature (sometimes called "RAMDAC shadowing") on the PCI card is enabled and functioning properly.

Configuration Byte 94h, ROM Flash/Power Button Status

Default Value = 00h

Bit	Function
7..5	Reserved
4	ROM Flash In Progress (if set)
3	Reserved
2	Power Button Inhibited (ifset)
1	User-Forced Bootblock (if set)
0	ROM Flash In Progress (if set)

Configuration Byte 97h, Asset/Test Prompt Byte

Default Value = 00h

Bit	Function
7,6	Test Prompt: 01 = Fake F1 10 = Fake F2 11 = Fake F10
5..0	Asset Value

Configuration Byte 9Bh, Ultra-33 DMA Enable Byte

Default Value = 00h

Bit	Function
7..4	Reserved
3	Secondary Slave Enabled for U-33 if Set
2	Secondary Master Enabled for U-33 if Set
1	Primary Slave Enabled for U-33 if Set
0	Primary Master Enabled for U-33 if Set

Configuration Byte 9Ch, Mode-2 Configuration Byte

Default Value = 1Ch

Bit	Function
7,6	Reserved
5	Mode 2 Support 0 = Disable 1 = Enable
4	Secondary Hard Drive Controller 0 = Disable 1 = Enable
3,2	Secondary Hard Drive Controller IRQ 00 = IRQ10 01 = IRQ11 10 = IRQ12 11 = IRQ15
1,0	Reserved

Configuration Byte 9Dh, ESS Audio Configuration Byte

Default Value = 12h

Bit	Function
7	Reserved for Game Port Enable
6,5	Audio Address 00 = 22xh 01 = 23xh 10 = 24xh 11 = 25xh
4,3	DMA Channel 00 = Disabled 01 = DMA0 10 = DMA1 11 = DMA3
2,1	IRQ Select 00 = IRQ9 01 = IRQ5 10 = IRQ7 11 = IRQ10
0	ESS Audio Chip Enable 0 = Enabled 1 = Disabled

Configuration Byte 9Eh, ECP DMA Configuration Byte

Default Value = 03h

Bit	Function
7..4	Reserved
3	SafeStart Control: 0 = Disable 1 = Enable
2..0	ECP DMA Channel 000 = Invalid 100 = Disabled All other values (001-011, 101-111) refer to channel no.

Configuration Byte 9Fh-AFh, Asset Tag Serial Number

Configuration Bytes B0h-C3h; Custom Hard Drive Information

These bytes contain the number of cylinders, heads, and sectors per track for hard drives C, D, E, and F respectively. The mapping for each drive is as follows:

Drive 65 (C)	Drive 66 (D)	Drive 68 (E)	Drive 15 (F)	Function
B0h	B5h	BAh	BFh	No. of Cylinders, Low Byte
B1h	B6h	BBh	C0h	No. of Cylinders, High Byte
B2h	B7h	BCh	C1h	No. of Heads
B3h	B8h	BDh	C2h	Max ECC Bytes
B4h	B9h	BEh	C3h	No. of Sectors Per Track

Configuration Byte C7h, C8h, Serial Ports 1 and 2 (Respectively) Configuration Bytes

Default Value = FEh, 7Dh

Bit	Function
7..2	Base I/O Address (in packed format) (Algorithm: [Addr. - 200h] / 8) (i.e., 3Fh = 3F8h, 1Fh = 2F8h, 00 = 200h)
1..0	Reserved

4.6 I/O MAP AND REGISTER ACCESSING

This section describes the system I/O map and methods of accessing various system functions.

4.6.1 SYSTEM I/O MAP

Table 4-17.
System I/O Map

I/O Port	Function
0000..000Fh	DMA Controller 1
0020..0021h	Interrupt Controller 1
0040..0043h	Timer 1
0060h	Keyboard Controller Data Byte
0061h	NMI, Speaker Control
0064h	Keyboard Controller Command/Status Byte
0070h	NMI Enable, RTC Address
0071h	RTC Data
0078h..007Bh	General Purpose I/O Port 1
007Ch..007Fh	General Purpose I/O Port 2
0080..008Fh	DMA Page Registers
0092h	Port A, Fast A20/Reset
00A0..00A1h	Interrupt Controller 2
00B2h, 00B3h	APM Control/Status Ports
00C0..00DFh	DMA Controller 2
00F0h	Math Coprocessor Busy Clear
015C, 015Dh	87307 I/O Controller Configuration Registers (Index, Data)
0170..0177h	Hard Drive (IDE) Controller 2
01F0..01FFh	Hard Drive (IDE) Controller 1
0201..024Fh	Reserved.
0278..027Bh	Parallel Port (LPT2)
02F8..02FFh	Serial Port (COM2)
0371.. 0375h	Diskette Drive Controller Alternate Addresses
0376h	IDE Controller Alternate Address
0377h	IDE Controller Alternate Address, Diskette Drive Controller Alternate Address
0378..037Fh	Parallel Port (LPT1)
0388..038Bh	FM synthesizer (alias addresses)
03B0..03DFh	Graphics Controller
03E8..03EFh	Serial Port (COM3)
03F0..03F5h	Diskette Drive Controller Primary Addresses
03F6, 03F7h	Diskette Drive Controller Primary Addresses, Hard Drive Controller Primary Addresses
03F8..03FFh	Serial Port (COM1)
04D0, 04D1h	Master, Slave Edge/Level INTR Control Register
0C06, 0C07h	Reserved - Compaq proprietary use only
0C50, 0C51h	System Management Configuration Registers (Index, Data)
0C70..0C77h	ACPI
0C82h	Auto Rev Data (not used)
0CF8h	PCI Configuration Address (dword access)
0CFCh	PCI Configuration Data (byte, word, or dword access)
F800..F83Fh	ACPI & GPIOs

NOTE: Assume unmarked gaps are reserved/unused.

4.6.2 87307 I/O CONTROLLER CONFIGURATION

The 87307 I/O controller contains various functions such as the keyboard/mouse interfaces, diskette interface, serial interfaces, and parallel interface. Software control of these interfaces uses standard AT-type I/O addressing. Firmware configuration of these functions uses indexed ports unique to the 87307. In this system, hardware strapping selects I/O addresses 015Ch and 015Dh at reset as the Index/Data ports for accessing the configuration registers of the logical devices within the 87307. The hardware strapping also places the 87307 into PnP motherboard mode. Table 4-18 lists the PnP standard configuration registers for the devices within the 87307.

Table 4-18.
87307 I/O Controller PnP Standard Configuration Registers

Index	Function	Reset Value
00h	Set RD_DATA Port	00h
01h	Serial Isolation	
02h	Configuration Control	
03h	Wake (CSN)	00h
04h	Resource Data	
05h	Status	
06h	Card Select Number (CSN)	00h
07h	Logical Device Select: 00h = 8042 Controller (Keyboard I/F) 01h = 8042 Controller (Mouse I/F) 02h = RTC/APC Configuration 03h = Diskette Controller 04h = Parallel Port 05h = UART 2 (Serial Port B / IrDA) 06h = UART 1 (Serial Port A) 07h = GPIO Ports 08h = Power Management	00h
20h	Super I/O ID Register (SID)	A0h
21h	SIO Configuration 1 Register	D6h
22h	SIO Configuration 1 Register	02h
23h	Programmable Chip Select Configuration Index	00h
24h	Programmable Chip Select Configuration Data	00h
30h	Logical Device Activate	--
31h	Logical Device I/O Range Check	--
60,61h	Logical Device Data Base Address	--
62,63h	Logical Device Command Base Address	--
70h	Logical Device Interrupt Select	--
71h	Logical Device Interrupt Type	--
74,75h	Logical Device DMA Assignment	--
F0h	Logical Device Configuration	--
F1h	Drive ID (Logical Device 03 only)	--

The configuration registers are accessed by writing the appropriate logical device's number to index 07h and writing the desired offset to the index register. The data is then either written to or read from the data register.

The 87307 I/O Controller provides 11 general purpose pins that can be individually configured as either inputs or outputs. These pins are mapped as two general purpose ports and software-accessable through the registers shown below.

GPIO Port 1 Data, I/O Addr. 078h, (87307 I/O Controller)

Bit	Function
7..4	GPIO17..GPIO14: Not used.
3	GPIO13 (config. as input). Bus Fraction (BF2)
2	GPIO12 (config. as input): CPU Bus Speed Read 0, 60 MHz Read 1, 66 MHz
1,0	GPIO11,10 (config. as inputs): Bus Fraction (ratio) BF1,0 Read 00, 2/5 bus/core speed ratio Read 10, 1/3 bus/core speed ratio Read 01, ½ bus/core speed ratio Read 11, 2/7 bus/core speed ratio

GPIO Port 1 Direction, I/O Addr. 079h, (87307 I/O Controller)

GPIO Port 1 Output Type, I/O Addr. 07Ah, (87307 I/O Controller)

GPIO Port 1 Pullup Control, I/O Addr. 07Bh, (87307 I/O Controller)

GPIO Port 2 Data, I/O Addr. 07Ch, (87307 I/O Controller)

Bit	Function
7..4	GPIO27..24 (config. as I/O): X bus bits <5..2>
3	GPIO23 (config. as input): Ring Wake Up (Serial Modem) Read 0, Ring indicate active Read 1, Ring indicate inactive
2	GPIO22 (config. as output): NIC I/F Enable. Write 0 to enable. Write 1 to disable.
1,0	GPIO21 Not used.

GPIO Port 2 Direction, I/O Addr. 07Dh, (87307 I/O Controller)

GPIO Port 2 Output Type, I/O Addr. 07Eh, (87307 I/O Controller)

GPIO Port 2 Pullup Control, I/O Addr. 07Fh, (87307 I/O Controller)

4.7 SYSTEM MANAGEMENT SUPPORT

This section describes the hardware support of functions involving security, safety, identification, and power consumption of the system. System management functions are handled largely through a Compaq-proprietary ASIC. Most functions are controlled through registers (Table 4-19) accessed using the indexed method through I/O ports 0C50h (index) and 0C51h (Data).

Table 4-19.
System Management Control Registers

Index	Function
00h	Identification
02h	Temperature Status / Clear
03h	Temperature Interrupt / SMI Enable
05h	Power On LED Blink Control
12h	General Purpose Open Collector (GPOC) Bits
13h	Secured GPOC Bits
20h	Power Button Control
21h	SMI / SCI Source
22h	SMI / SCI Mapping
30h	REQ/GNT Control
80h-89h	Reserved

NOTE: System management functions are handled by BIOS and the Setup utility. The information in the following subsections is intended only for clarification of system operations.

4.7.1 FLASH ROM WRITE PROTECT

The system BIOS firmware is contained in a flash ROM device that can be re-written with updated code if necessary. The ROM is write-protected with a Black Box* security feature. The Black Box feature uses the Administrator password to protect against unauthorized writes to the flash ROM. During the boot sequence, the BIOS checks for the presence of the ROMPAQ diskette. If ROMPAQ is detected and the password is locked into the Black Box with the Protect Resources command, an Access Resources command followed by Administrator password entry must occur before the ROM can be flashed. If the Permanently Lock Resources command has been invoked, the power must be cycled before the ROM can be flashed. The system ROM is write-protected as follows:

Start Addr.	End Addr.	Data Type	Protection
C0000h	EFFFFh	Option ROM	Password write-protected
F0000h	F7FFFh	System BIOS	Password write-protected
F8000h	F9FFFh	ESCD	Never write-protected
FA000h	FFFFFh	Boot Block	Always write-protected

The flashing functions are handled using the INT15 AX-E822h BIOS interface.

* Black Box logic Compaq-proprietary and controlled exclusively through firmware in the BIOS ROM.

4.7.2 PASSWORD PROTECTION

When enabled, the user is prompted to enter the power-on password during POST. If an incorrect entry is made, the system halts and does not boot. The Power-On password is stored in eight bytes at configuration memory locations 37h-3Fh. These locations are physically located within the 87307. At the time a new password is written into 37h-3Fh, the password is also written into Black Box* logic. The Black Box logic is used for power-on password protection support instead of the port 92 sequence used on other systems. The Black Box logic prevents inadvertent or unauthorized access to the password bytes of the 87307 by monitoring I/O ports 70/71h for access to the 37h-3Fh CMOS range and inhibiting the AEN signal to the 87307 if such access is detected. Slot 1 of the Black Box logic can be written to at runtime, allowing the user to change the power on password without cycling power and going through the F10 method. The Black Box password cannot be read.

The power-on password function can be disabled by setting DIP SW1 position 1 to on (closed).

The administrator password is stored in eight bytes at configuration memory locations 77h-7Fh. If the administrator password function is enabled, the user is prompted to enter the password before running F10-Setup or before booting from a ROMPAQ diskette. If an incorrect entry is made, the system boots although system administration functions are inhibited. The administrator password is also stored in the Black Box* logic. Black Box logic acting as the sentry for the administrator password by preventing inadvertent or unauthorized writing to the Flash ROM.

* Black Box logic is Compaq-proprietary and controlled exclusively through firmware in BIOS ROM.

4.7.3 I/O SECURITY

The 87307 I/O controller allows various I/O functions to be disabled through configuration registers. In addition, the configuration registers of the 87307 are further protected by Client Management (CM) logic, which can be set (using BIOS call INT 15 AX=E829h) to block access to the 87307 configuration registers of the following functions:

- Diskette drive
- Serial port
- Parallel port

In blocking 87307 functions, the CM logic monitors ISA I/O cycles and can detect, through index address-matching, when an attempt is made to access a function provided by the 87307. If the CM logic has been set to block access, then ISA bus signal AEN or IOWC-, both which the CM logic provides to the 87307, is disabled, effectively inhibiting the I/O access.

The NIC controller can also be blocked from access by the CM logic. In this case the CM logic can be set to block the routing of the IDSEL signal to the NIC controller, thereby disabling the interface.

4.7.4 USER SECURITY

The QuickLock feature allows, if enabled in F10-Setup through CMOS location 13h bit <2>, the user to lock the keyboard and mouse by invoking the **Ctrl-Alt-L** keystrokes. This initiates an SMI and the SMI handler then takes the action required to lock the keyboard. If the QuickBlank feature is enabled at that time then the screen will be blanked as well. The user then must enter the power-on password to re-activate the keyboard and/or display .

> **NOTE:** Although the SMI is used for initiating QuickLock/QuickBlank functions, these functions are not considered power management features.

4.7.5 TEMPERATURE SENSING

Two components (one programmable LM75 and one TC623) are used in monitoring the internal temperature of the system. The LM75 sensor is mounted in the cavity of the microprocessor socket to detect microprocessor temperature. The LM75 is programmed for two temperature levels:

a. Tos - Overtemperature shutdown value (level at which the LM75's output becomes active)
b. Thyst - Hysterious value (level at which the LM75's output is negated)

In the standard configuration the BIOS programs Tos for 60°C and Thyst for 58°C. Detection by the LM75 sensor results in a warning being issued to the user and/or the power supply fan being turned on. Note that upgrading to particular microprocessor step with unique operating temperature characteristics may require that the BIOS be upgraded as well in order to set the LM75 to the proper detection levels.

The following two indexed registers are used by BIOS and available to software for controlling the temperature sense function.

I/O Port C51.02h, Temperature Status/Clear Register

Bit	Function
7..2	Reserved
1	Temperature Deadly (RO) 0 = Normal 1 = Critical temperature detected
0	Temperature Caution for Processor 1 (RO) 0 = Normal 1 = High temperature detected at P1

NOTE: Bits 2..0 are cleared when read but will be instantly reset if condition remains.

I/O Port C51.03h, Temperature Interrupt/SMI Enable Register

Bit	Function
7..3	Reserved
2	Temperature Deadly Shutdown Disable: 0 = Initiate shutdown w/deadly condition. 1 = Do not initiate shutdown.
1	Temperature SMI Enable: 0 = Do not generate SMI- w/caution condition. 1 = Generate SMI- upon caution condition.
0	Temperature IRQ Enable: 0 = Do not generate IRQ w/ caution condition. 1 = Generate IRQ w/caution condition.

A second sensor (TC623) is used to detect a deadly temperature condition. This sensor, which is non-programmable (fixed), activates a signal that disables the ICS9147 clock generator, effectively shutting down the system.

4.7.6 POWER MANAGEMENT

This system includes hardware support of Advanced Power Management (APM ver. 1.2) firmware and software and is Energy Star-compliant.

4.7.6.1 HARD DRIVE SPINDOWN CONTROL

The timeout parameter stored in the SIT record 04h and indexed through CMOS location 2Ah (bits <4..0>) represents the period of hard drive inactivity required to elapse before the hard drive is allowed to spin down. The timeout value is downloaded from CMOS to a timer on the hard drive. The timeout period can be set in incremental values of 0 (timeout disabled), 10, 15 (default), 20, 30, and 60 minutes. A timed-out and spun-down hard drive will automatically spin back up upon the next drive access. It is normal for the user to detect a certain amount of access latency in this situation.

4.7.6.2 DISPLAY MONITOR POWER MANAGEMENT CONTROL

This system supports monitor power control for graphics controllers and display monitors that conform to the VESA display power management signaling (DPMS) protocol. This protocol defines different power consumption conditions and uses the HSYNC and VSYNC signals to select a monitor's power condition This operation is described in chapter 6, "Graphics Subsystem."

The timeout parameter set in the SIT record 03h and indexed at CMOS location 2Ch (bits <4..0>) represents the period of system I/O inactivity required to elapse before the monitor is placed into Suspend mode.

A separate timer function (enabled through CMOS location 1Fh, bit <1>) can be enabled to place the monitor into the Off mode after 45 minutes of being in Suspend mode.

Chapter 5
INPUT/OUTPUT INTERFACES

5.1 INTRODUCTION

This chapter describes the system's interfaces that provide input and output (I/O) porting of data and specifically discusses interfaces that are controlled through I/O-mapped registers. The I/O interfaces are integrated functions of the support chipset and the 87307 I/O controller. The following I/O interfaces are covered in this chapter:

5.2 ENHANCED IDE INTERFACE

The enhanced IDE (EIDE) interface consists of primary and secondary interfaces that can support two IDE devices each. Devices that may connect to an IDE interface include hard drives, CD-ROM drives, power (writeable CD-ROM) drives, and 120-MB floptical drives.

Two 40-pin keyed IDE data connectors and one 50-pin keyed connector are provided on the system board. Each 40-pin connector can support two devices* and can be configured independently for PIO or bus master (DMA) operation. In the standard configuration the hard drive is attached to the primary connector and the CD-ROM (if installed) is attached to the 50-pin secondary connector.

The system ROM supports PIO modes 1-4 and Ultra ATA (UATA) modes 0-2, although the type of drive connected will determine the final transfer speed.

> **NOTE:** For UATA mode 2 operation an 80-conductor cable must be used. A 40-conductor cable will result in the BIOS limiting IDE operation to a maximum transfer of 25 MB/s (UATA mode 1).

5.2.1 IDE PROGRAMMING

The IDE interface is configured as a PCI device and controlled through standard I/O mapped registers.

* Refer to chapter 2 for possible physical limitations on drive accommodations.

5.2.1.1 IDE Configuration Registers

The IDE interface is handled by the 82586 component and configured as a PCI device with bus mastering capability. The PCI configuration registers for the IDE controller function (PCI device #20, function #1) are listed in Table 5-1.

Table 5-1.
EIDE PCI Configuration Registers (82586, Function 1)

PCI Conf. Addr.	Register	Value on Reset	PCI Conf. Addr.	Register	Value on Reset
00-01h	Vender ID	1106h	40h	Chip Enable reg.	
02-03h	Device ID	0586h	41h	IDE Configuration	00h
04-05h	PCI Command	0000h	42h	Miscellaneous Control	
06-07h	PCI Status	0000h	43h	FIFO Configuration	
08h	Revision ID	0Ah	44h	Miscellaneous Control	
09h	Programming	xxxxh	45h	Miscellaneous Control	
0Ah	Sub-Class	01h	46h	Miscellaneous Control	C0h
0Bh	Base Class Code	01h	48h	Sec. IDE Drv.1 Timing Cntrl.	A8h
0Dh	Master Latency Timer	0000h	49h	Sec. IDE Drv.0 Timing Cntrl	A8h
0Eh	Header Type	80h	4Ah	Pri. IDE Drv.1 Timing Cntrl.	A8h
10-13h	Pri. Data/Cmd Base Addr.	1F0h	4Bh	Pri. IDE Drv.0 Timing Cntrl	A8h
14-17h	Pri. Cntrl./Sts. Base Addr.	3F4h	4Ch	Address Setup Time	
18-1Bh	Sec. Data/Cmd Base Addr.	170h	4E, 4Fh	Non-1F0h Port Drive Timing	00FFh
1C-1Fh	Sec. Cntrl./Sts. Base Addr.	374h	50h	Sec. Drive 1 Ext. Timing	00h
20-23h	Bus Mstr. Cntrl. Reg. Base Addr.		51h	Sec. Drive 0 Ext. Timing	00h
24-27h	Mem. Base Addr. for MM I/O		52h	Pri. Drive 1 Ext. Timing	00h
3Ch	Interrupt Line	0Eh	53h	Pri. Drive 0 Ext. Timing	00h
3Dh	Interrupt Pin		54-5Fh	Reserved	
3Eh	Min_GNT		60, 61h,	Sector Size for Pri. IDE	200h
3Fh	Min_LAT		68, 69h	Sector Size for Sec. IDE	200h

NOTE:
Assume unmarked gaps are reserved and/or not used.

5.2.1.2 IDE Bus Master Control Registers

The IDE interface can perform PCI bus master operations using the I/O mapped control registers listed in Table 5-2.

Table 5-2.
IDE Bus Master Control Registers

I/O Addr. Offset	Size (Bytes)	Register	Default Value
00h	2	Bus Master IDE Command (Primary)	00h
02h	2	Bus Master IDE Status (Primary)	00h
04h	4	Bus Master IDE Descriptor Ptr (Pri.)	0000 0000h
08h	2	Bus Master IDE Command (Secondary)	00h
0Ah	2	Bus Master IDE Status (Secondary)	00h
0Ch	4	Bus Master IDE Descriptor Ptr (Sec.)	0000 0000h

5.2.1.3 IDE ATA Control Registers

The IDE controller of the 82586 decodes the addressing of the standard AT attachment (ATA) registers for the connected drive, which is where the ATA control registers actually reside. The primary and secondary interface connectors are mapped as shown in Table 5-3.

Table 5-3.
IDE ATA Control Registers

Primary I/O Addr.	Secondary I/O Addr.	Register	R/W
1F0h	170h	Data	R/W
1F1h	171h	Error	R
1F1h	171h	Features	W
1F2h	172h	Sector Count	R/W
1F3h	173h	Sector Number	R/W
1F4h	174h	Cylinder Low	R/W
1F5h	175h	Cylinder High	R/W
1F6h	176h	Drive/Head	R/W
1F7h	177h	Status	R
1F7h	177h	Command	W
3F6h	376h	Alternate Status	R
3F6h	376h	Drive Control	W
3F7h	377h	Drive Address	R
3F7h	377h	n/a for hard drive	W

The following paragraphs describe the IDE ATA control registers.

Data Register, I/O Port 1F0h/170h

This register is used for transferring all data to and from the hard drive controller. This register is also used for transferring the sector table during format commands. All transfers are high-speed 16-bit I/O operation except for Error Correction Code (ECC) bytes during Read/Write Long commands.

Error Register, I/O Port 1F1h/171h (Read Only)

The Error register contains error status from the last command executed by the hard drive controller. The contents of this register are valid when the following conditions exist:

- Error bit is set in the Status register
- Hard drive controller has completed execution of its internal diagnostics

The contents of the Error register are interpreted as a diagnostic status byte after the execution of a diagnostic command or when the system is initialized.

Bit	Function
7	Bad Block Mark Detected in Requested Sector ID Field (if set)
6	Non-correctable Data Error (if set)
5	Reserved
4	Requested Sector ID Field Not Found (if set)
3	Reserved
2	Requested Command Aborted Due To Invalid Hard Drive Status or Invalid Command Code (if set)
1	Track 0 Not Found During Re-calibration Command (if set)
0	Data Address Mark Not Found After Correct ID Field (if set)

Set Features Register, I/O Port 1F1h/171h (Write Only)

This register is command-specific and may be used to enable and disable features of the interface.

Sector Count Register, I/O Port 1F2h/172h

This register defines either:

- the number of sectors of data to be read or written

or

- the number of sectors per track for format commands

If the value in this register is zero, a count of 256 sectors is specified. The sector count is decremented as each sector is accessed, so that the value indicates the number of sectors left to access when an error occurs in a multi-sector operation. During the Initialize Drive Parameters command, this register contains the number of sectors per track.

Sector Number Register, I/O Port 1F3h/173h

The Sector Number register contains the starting sector number for a hard drive access.

Cylinder Low, Cylinder High Registers, I/O Port 1F4h, 1F5h/174h, 175h

These registers contain the starting cylinder number for each hard drive access. The three most-significant bits of the value are held in byte address 1F5h (bits <2..0>) while the remaining bits are held in location 1F4h.

Drive Select/Head Register, I/O Port 1F6h/176h

Bit	Function
7	Reserved
6,5	Sector Size: 00 = Reserved 01 = 512 bytes/sector 10, 11 = Reserved
4	Drive Select: 0 = Drive 1 1 = Drive 2
3..0	Head Select Number: 0000 = 0 1000 = 8 0001 = 1 1001 = 9 0010 = 2 1010 = 10 0011 = 3 1011 = 11 0100 = 4 1100 = 12 0101 = 5 1101 = 13 0110 = 6 1110 = 14 0111 = 7 1111 = 15

NOTE:

Setting bit <4> to 1 when Drive 2 is not present may cause remaining controller registers to not respond until Drive 1 is selected again.

Status Register, I/O Port 1F7h/177h (Read Only)

The contents of this register are updated at the completion of each command. If the Busy bit is set, no other bits are valid. Reading this register clears the IRQ14 interrupt.

Bit	Function
7	Controller Busy. If set, controller is executing a command.
6	READY- Signal Active (if set).
5	WRITE FAULT- Signal Active (if set).
4	SEEK COMPLETE- Signal Active (if set)
3	Data Request. If set, the controller is ready for a byte or word-length data transfer. Bit should be verified before each transfer.
2	Correctable Data Error Flag. If set, data error has occurred and has been corrected.
1	INDEX- Signal Active (if set).
0	Error Detected. When set, indicates error has occurred. O.ther bits in register should be checked to determine error source.

NOTE:

Register status of an error condition does not change until register is read.

The alternate Status register at location 3F6h holds the same status data as location 1F7h but does not clear hardware conditions when read.

Command Register, I/O Port 1F7h/177h (Write Only)

The IDE controller commands are written to this register. The command write action should be prefaced with the loading of data into the appropriate registers. Execution begins when the command is written to 1F7h/177h. Table 5-4 lists the standard IDE commands.

Table 5-4.
IDE Controller Commands

Command	Value
Initialize Drive Parameters	91h
Seek	7xh
Recalibrate	1xh
Read Sectors with Retries	20h*
Read Long with Retries	22h*
Write Sectors with Retries	30h*
Write Long with Retries	32h*
Verify Sectors with Retries	40h
Format Track	50h
Execute Controller Diagnostic	90h
Idle	97h, E3h
Idle Immediate	95h, E1h
Enter Low Power and Enable/Disable Timeout	96h
Enter Idle and Enable/Disable Timeout	97h
Check Status	98h
Identify	ECh
Read Buffer	E4h
Write Buffer	E8h
NOP	00h
Read DMA with Retry	C8h
Read DMA without Retry	C9h
Read Multiple	C4h
Set Features	EFh
Set Multiple Mode	C6h
Sleep	99h, E6h
Standby	96h, E2h
Standby Immediate	94h, E0h
Write DMA with Retry	CAh
Write DMA without Retry	CBh
Write Multiple	C5h
Write Same	E9h
Write Verify	3Ch

* Without retries, add one to the value.

Alternate Status Register, I/O Port 3F6h/376h (Read Only)

The alternate Status register at location 3F6h holds the same status data as location 1F7h but does not clear hardware conditions when read.

Drive Control Register, I/O Port 3F6h/376h (Write Only)

Bit	Function
7..3	Reserved
2	Controller Control: 0 = Re-enable 1 = Reset
1	Interrupt Enable/Disable 0 = Disable interrupts 1 = Enable interrupts
0	Reserved

Drive Access Register, I/O Port 3F7h/377h (Read Only)

Bit	Function
7	Reserved
6	WRITE GATE- Signal Active (if set)
5..2	Head Select: 0000 = 15 1000 = 7 0001 = 14 1001 = 6 0010 = 13 1010 = 5 0011 = 12 1011 = 4 0100 = 11 1100 = 3 0101 = 10 1101 = 2 0110 = 9 1110 = 1 0111 = 8 1111 = 0
1,0	Drive Select: 00 = Disabled 01 = Drive 1 selected 10 = Drive 0 selected 11 = Invalid

5.2.2 IDE CONNECTORS

This system includes two standard 40-pin connectors and one 50-pin connector for IDE devices. Devices attached to the 40-pin connectors obtain power through a separate connector. The 40-pin connector is shown in the illustration below followed by the connector's pinout.

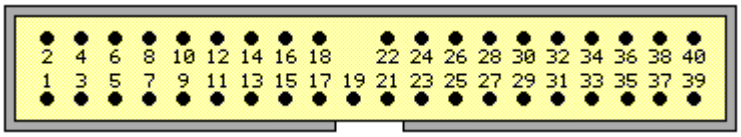


Figure 5–1. 40-Pin IDE Connector.

Table 5-5.
40-Pin IDE Connector Pinout

Pin	Signal	Description	Pin	Signal	Description
1	RESET-	Reset	21	DRQ	DMA Request
2	GND	Ground	22	GND	Ground
3	DD7	Data Bit <7>	23	IOW-	I/O Write
4	DD8	Data Bit <8>	24	GND	Ground
5	DD6	Data Bit <6>	25	IOR-	I/O Read
6	DD9	Data Bit <9>	26	GND	Ground
7	DD5	Data Bit <5>	27	IORDY	I/O Channel Ready
8	DD10	Data Bit <10>	28	CSEL	Cable Select
9	DD4	Data Bit <4>	29	DAK-	DMA Acknowledge
10	DD11	Data Bit <11>	30	GND	Ground
11	DD3	Data Bit <3>	31	IRQn	Interrupt Request [1]
12	DD12	Data Bit <12>	32	IO16-	16-bit I/O
13	DD2	Data Bit <2>	33	DA1	Address 1
14	DD13	Data Bit <13>	34	DSKPDIAG	Pass Diagnostics
15	DD1	Data Bit <1>	35	DA0	Address 0
16	DD14	Data Bit <14>	36	DA2	Address 2
17	DD0	Data Bit <0>	37	CS0-	Chip Select
18	DD15	Data Bit <15>	38	CS1-	Chip Select
19	GND	Ground	39	HDACTIVE-	Drive Active (front panel LED) [2]
20	--	Key	40	GND	Ground

NOTES:

[1] Primary connector wired to IRQ14, secondary connector wired to IRQ15.

[2] Pin 39 is used for spindle sync and drive activity (becomes SPSYNC/DACT-) when synchronous drive are connected.

The 50-pin connector is intended for a CD-ROM drive that operates as a slave on the secondary IDE interface. This interface includes power and audio signals. The 50-pin connector is illustrated below followed by the pinout.

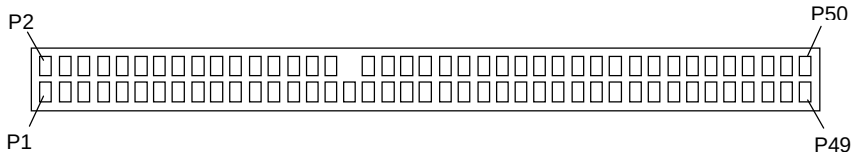


Figure 5–1. 50-Pin IDE Connector.

Table 5-5.
50-Pin IDE Connector Pinout

Pin	Signal	Description	Pin	Signal	Description
1	RESDRV-	Reset	26	GND	Ground
2	GND	Ground	27	CHRDY	I/O Channel Ready
3	SHD07	Data Bit <7>	28	ALE	Cable Select [1]
4	SHD08	Data Bit <8>	29	DAK-	DMA Acknowledge
5	SHD06	Data Bit <6>	30	GND	Ground
6	SHD09	Data Bit <9>	31	IRQ	Interrupt Request [1]
7	SHD05	Data Bit <5>	32	IO16-	16-bit I/O
8	SHD10	Data Bit <10>	33	A1	Address 1
9	SHD04	Data Bit <4>	34	PDIAG-	Pass Diagnostics
10	SHD11	Data Bit <11>	35	A0	Address 0
11	SHD03	Data Bit <3>	36	A2	Address 2
12	SHD12	Data Bit <12>	37	CS1FX-	Chip Select
13	SHD02	Data Bit <2>	38	CS3FX-	Chip Select
14	SHD13	Data Bit <13>	39	DASF-	Drive Active
15	SHD01	Data Bit <1>	40	GND	Ground
16	SHD14	Data Bit <14>	41	AUD L	Left Channel Audio
17	SHD00	Data Bit <0>	42	AUD R	Right Channel Audio
18	SHD15	Data Bit <15>	43	AUD R RTN	Right Channel Audio Return
19	GND	Ground	44	AUD L RTN	Left Channel Audio Return
20	--	(Key Space)	45	+5 VDC	Motor Power
21	DRQ	DMA Request	46	+5 VDC	Motor Power
22	GND	Ground	47	+5 VDC	Motor Power
23	IOW-	I/O Write	48	+5 VDC	Motor Power
24	GND	Ground	49	+5 VDC	Log Power
25	IOR-	I/O Read	50	+5 VDC	Log Power

NOTES:

[1] Pin is left floating to make CD-ROM always slave.

5.3 DISKETTE DRIVE INTERFACE

The diskette drive interface supports up to two diskette drives through a standard 34-pin diskette drive connector. All Deskpro 4000S models include a 3.5 inch 1.44-MB diskette drive installed as drive A. There is no physical provision for a second drive (B).

The diskette drive interface function is integrated into the 87307 I/O controller component. The internal logic of the I/O controller is software-compatible with standard 82077-type logic. The diskette drive controller has three operational phases in the following order:

- Command phase - The controller receives the command from the system.
- Execution phase - The controller carries out the command.
- Results phase - Status and results data is read back from the controller to the system.

The Command phase consists of several bytes written in series from the CPU to the data register (3F5h/375h). The first byte identifies the command and the remaining bytes define the parameters of the command. The Main Status register (3F4h/374h) provides data flow control for the diskette drive controller and must be polled between each byte transfer during the Command phase.

The Execution phase starts as soon as the last byte of the Command phase is received. An Execution phase may involve the transfer of data to and from the diskette drive, a mechnical control function of the drive, or an operation that remains internal to the diskette drive controller. Data transfers (writes or reads) with the diskette drive controller are by DMA, using the DRQ2 and DACK2- signals for control.

The Results phase consists of the CPU reading a series of status bytes (from the data register (3F5h/375h)) that indicate the results of the command. Note that some commands do not have a Result phase, in which case the Execution phase can be followed by a Command phase.

During periods of inactivity, the diskette drive controller is in a non-operation mode known as the Idle phase.

5.3.1 DISKETTE DRIVE PROGRAMMING

5.3.1.1 Diskette Drive Interface Configuration

The diskette drive controller must be configured for a specific address and also must be enabled before it can be used. Address selection and enabling of the diskette drive interface are affected by firmware through the PnP configuration registers of the 87307 I/O controller.

The PnP configuration registers are accessed through I/O registers 15Ch (index) and 15Dh (data). The diskette drive I/F is initiated by firmware selecting logical device 3 of the 87307. This is accomplished by the following sequence:

1. Write 07h to I/O register 15Ch.
2. Write 03h to I/O register 15Dh (this selects the diskette drive I/F).
3. Write 30h to I/O register 15Ch.
4. Write 01h to I/O register 15Dh (this activates the interface).

The diskette drive I/F configuration registers are listed in the following table:

Table 5-6.
Diskette Drive Interface Configuration Registers

Index Address	Function	R/W	Reset Value
30h	Activate	R/W	01h
31h	I/O Range Check	R/W	00h
60h	Base Address MSB	R/W	03h
61h	Base Address LSB	R/W	F0h
70h	Interrupt Select	R/W	06h
71h	Interrupt Type	R/W	03h
74h	DMA Channel Select	R/W	02h
75h	Report DMA Assignment	RO	04h
F0h	Configuration Data	R/W	--
F1h	Drive ID	R/W	--

5.3.1.2 Diskette Drive Interface Control

The BIOS function INT 13 provides basic control of the diskette drive interface. The diskette drive interface can be controlled by software through I/O-mapped registers listed in Table 5-7.

Table 5-7.
Diskette Drive Interface Control Registers

Primary Address	Alternate Address	Register	R/W
3F1h	371h	Media ID	R
3F2h	372h	Drive Control	W
3F4h	374h	Main Status	R
3F5h	375h	Data	R/W
3F7h	377h	Drive Status	R
		Data Transfer Rate	W

The base address (3F1h or 371h) and enabling of the diskette drive controller is selected through the Function Enable Register (FER, addr. 399.00h) of the 87307 I/O controller. Address selection and enabling is automatically done by the BIOS during POST but can also be accomplished with the Setup utility and other software.

The following paragraphs describe the diskette drive interface control registers.

Media ID Register, I/O Port 3F1h/371h (Read Only)

Bit	Function
7..5	Media Type: xx1 = Invalid 000 = 5.25 inch drive 010 = 2.88 MB (3.5 inch drive) 100 = 1.44 MB (3.5 inch drive) 110 = 720 KB (3.5 inch drive)
4..2	Reserved
1,0	Tape Select: 00 = None 10 = Drive 2 01 = Drive 1 11 = Drive 3

Drive Control Register, I/O Port 3F2h/372h (Write Only)

Bit	Function
7,6	Reserved
5	Drive 2 Motor 0 = Off, 1 = On
4	Drive 1 Motor 0 = Off, 1 = On
3	Interrupt / DMA Enable 0 = Disabled, 1 = Enabled
2	Controller Enable 0 = Reset controller, 1 = Enable controller
1,0	Drive Select 00 = Drive 1 01 = Drive 2 10 = Reserved 11 = Tape drive

Main Status Register, I/O Port 3F4h/374h (Read Only)

Bit	Function
7	Request for Master. When set, indicates the controller is ready to send or receive data from the CPU. Cleared immediately after a byte transfer. Indicates interrupt pin status during non-DMA phase.
6	Data I/O Direction. 0 = Expecting a write 1 = Expecting a read
5	Non-DMA Execution. When set, indicates controller is in the execution phase of a byte transfer in non-DMA mode.
4	Command In Progress. When set, indicates that first byte of command phase has been received. Cleared when last byte in result phase is read.
3..0	Drive Busy Indicators. Bit is set after the last byte of the command phase of a seek or recalibrate command is given by the corresponding drive: <3>, Drive 3 <2>, Drive 2 <1>, Drive 1 <0>, Drive 0

Data Register, I/O Port 3F5h/375h

Data commands are written to, and data and status bytes are read from this register.

Data Transfer Rate Register, I/O Port 3F7h/377h (Write Only)

Bit	Function
7	Software Reset
6	Low Power Mode (if set)
5	Reserved
4..2	Write Precompensation Delay 000 = Default values for selected data rate (default)
1,0	Data Rate Select: 00 = 500 Kb/s 01 = 300 Kb/s 10 = 250 Kb/s 11 = 1 or 2 Mb/s (depending on TUP reg. Bit <1>)

5.3.2 DISKETTE DRIVE CONNECTOR

This system uses a standard 34-pin connector (refer to Figure 5-2 and Table 5-8 for the pinout) for diskette drives. Drive power is supplied through a separate connector.

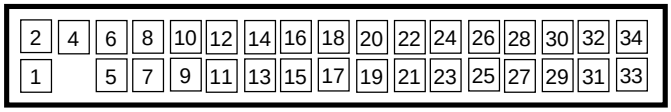


Figure 5–2. 34-Pin Diskette Drive Connector.

Table 5-8.
34-Pin Diskette Drive Connector Pinout

Pin	Signal	Description	Pin	Signal	Description
1	GND	Ground	18	DIR-	Drive head direction control
2	LOW DEN-	Low density select	19	GND	Ground
3	---	(KEY)	20	STEP-	Drive head track step control
4	MEDIA ID-	Media identification	21	GND	Ground
5	GND	Ground	22	WR DATA-	Write data
6	DRV 4 SEL-	Drive 4 select	23	GND	Ground
7	GND	Ground	24	WR ENABLE-	Enable for WR DATA-
8	INDEX-	Media index is detected	25	GND	Ground
9	GND	Ground	26	TRK 00-	Heads at track 00 indicator
10	MTR 1 ON-	Activates drive motor	27	GND	Ground
11	GND	Ground	28	WR PRTK-	Media write protect status
12	DRV 2 SEL-	Drive 2 select	29	GND	Ground
13	GND	Ground	30	RD DATA-	Data and clock read off disk
14	DRV 1 SEL-	Drive 1 select	31	GND	Ground
15	GND	Ground	32	SIDE SEL-	Head select (side 0 or 1)
16	MTR 2 ON-	Activates drive motor	33	GND	Ground
17	GND	Ground	34	DSK CHG-	Drive door opened indicator

5.4 SERIAL INTERFACES

The serial interfaces transmit and receive asynchronous serial data with external devices. The serial interface function is provided by the 87307 I/O controller component, which integrates two 16550/16450-compatible UARTs. One UART(1) is dedicated to support DB-9 connector (A) on the rear of the chassis while the second UART(2) can be configured to support the second DB-9 connector (B).

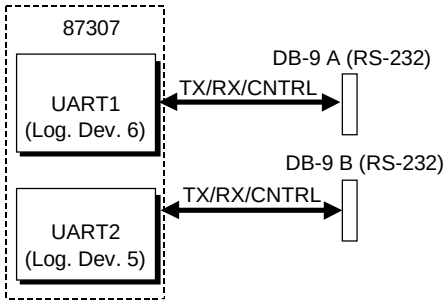


Figure 5–3. Serial Interfaces Block Diagram

5.4.1 RS-232 INTERFACE

The DB-9 connector-based interface complies with EIA standard RS-232-C, which includes modem control signals and supports baud rates up to 115.2 Kbps. The DB-9 connector is shown in the following figure and the pinout of the connector is listed in Table 5-9.

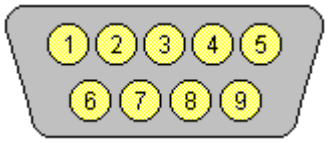


Figure 5–4. Serial Interface Connector (Male DB-9 as viewed from rear of chassis)

Table 5-9.
DB-9 Serial Connector Pinout

Pin	Signal	Description	Pin	Signal	Description
1	CD	Carrier Detect	6	DSR	Data Set Ready
2	RX Data	Receive Data	7	RTS	Request To Send
3	TX Data	Transmit Data	8	CTS	Clear To Send
4	DTR	Data Terminal Ready	9	RI	Ring Indicator
5	GND	Ground	--	--	--

Each DB-9 port is independently configurable as to it's COMn (address) designation.

5.4.2 SERIAL INTERFACE PROGRAMMING

5.4.2.1 Serial Interface Configuration

The serial interfaces must be configured for a specific address range (COM1, COM2, etc.) and also must be activated before it can be used. Address selection and activation of the serial interface are affected through the PnP configuration registers of the 87307 I/O controller.

The PnP configuration registers are accessed through I/O registers 15Ch (index) and 15Dh (data). Each serial interface is initiated by firmware selecting logical device 5 or 6 of the 87307. This is accomplished by the following sequence:

1. Write 07h to I/O register 15Ch.
2. Write 05h or 06h to I/O register 15Dh (for selecting UART2 or UART1).
3. Write 30h to I/O register 15Ch.
4. Write 01h to I/O register 15Dh (this activates the interface).

The serial interface configuration registers are listed in the following table:

Table 5-11.
Serial Interface Configuration Registers

Index Address	Function	R/W	Reset Value [1]
30h	Activate	R/W	00h / 00h
31h	I/O Range Check	R/W	00h / 00h
60h	Base Address MSB	R/W	02h / 03h
61h	Base Address LSB	R/W	F8h / F8h
70h	Interrupt Select	R/W	03h / 04h
71h	Interrupt Type	R/W	03h / 03h
74h	DMA Channel Select	R/W	04h / 04h
75h	Report DMA Assignment	RO	04h / 04h
F0h	Configuration Data	R/W	--

NOTES:
[1] Device 5 (UART2) / Device 6 (UART1)

5.4.2.2 Serial Interface Control

The BIOS function INT 14 provides basic control of the serial interface. The serial interface can be controlled by software through the registers listed in Table 5-12.

Table 5-12.
Serial Interface Control Registers

Address	Register	R/W
Base	Receive Buffer / Transmit Holding [1]	R/W
Base, Base + 1	Baud Rate Divisor Latch [2]	R/W
Base + 1	Interrupt Enable	R/W
Base + 2	Interrupt ID	RO
Base + 3	Line Control	R/W
Base + 4	Modem Control	R/W
Base + 5	Line Status	RO
Base + 6	Modem Status	RO
Base + 7	Scratch Pad	R/W

NOTES:

Base Address:

COM1 = 3F8h
COM2 = 2F8h

[1] This register holds receive data when read from and transmit data when written to.
[2] When bit <7> of the Line Control register is set (1), writing to 3F8h and 3F9h programs the divisor rate for the baud rate generator.

Receive Buffer / Transmit Holding Register, I/O Port 3F8h/2F8h

When read by the CPU, this byte contains receive data. When written to by the CPU, the byte contains data to be transmitted.

Baud Rate Divisor Latch Register, I/O Port 3F8h, 3F9h/2F8, 2F9h

When bit <7> of the Line Control register is set (1), a write to this pair of locations loads the decimal value used to divide the 1.8462-MHz clock to create the desired baud rate for serial transmission. The possible baud rates are shown as follows:

Baud Rate	Decimal Divisor	Baud Rate	Decimal Divisor
50	2304	2400	48
75	1536	3600	32
110	1047	4800	24
134.5	857	7200	16
150	768	9600	12
300	384	19200	6
600	192	38400	3
1200	96	57600	2
1800	64	115200	1
2000	58		

Divisor = 1846200 / (Desired baud rate X 16)

Interrupt Enable Register, I/O Port 3F9h/2F9h

Bits <3..0> of this register are used for enabling interrupt sources. A set bit enables interrupt generation by the associated source.

Bit	Function
7..4	Reserved
3	Modem Status Interrupt Enable (if set) (CTS, DSR, RI, CD)
2	Receiver Line Status Interrupt Enable (if set) (Overrun error, parity error, framing error, break)
1	Transmitter Holding Register Empty Interrupt Enable (if set)
0	Baud Rate Divisor Interrupt Enable (if set)

Interrupt ID Register, I/O Port 3FAh/2FAh (Read Only)

This read-only register indicates the serial controller as the source of the interrupt (bit <0>) as well as the reason (bits <3..1>) for the interrupt. Reading this register clears the interrupt and sets bit <0>.

Bit	Function
7,6	FIFO Enable/Disable 0 = Disabled 1 = Enabled
5,4	Reserved
3..1	Interrupt Source: 000 = Modem status (lowest priority) 001 = Transmitter holding reg. Empty 010 = Received data available 011 = Receiver line status reg. 100,101 = Reserved 110 = Character time-out (highest priority) 111 = Reserved
0	Interrupt Pending (if cleared)

FIFO Control Register, I/O Port 3FAh/2FAh (Write Only)

This write-only register enables and clears the FIFOs and set the trigger level and DMA mode.

Bit	Function
7,6	Receiver Trigger Level 00 = 1 byte 10 = 8 bytes 01 = 4 bytes 11 = 14 bytes
5..3	Reserved
2	Transmit FIFO Reset (if set)
1	Receive FIFO Reset (if set)
0	FIFOs Enable/Disable 0 = Disable TX/RX FIFOs, 1 = Enable TX/RX FIFOs

Line Control Register, I/O Port 3FBh/2FBh

This register specifies the data transmission format.

Bit	Function
7	RX Buffer / TX Holding Reg. And Divisor Rate Reg. Access 0 = RX buffer, TX holding reg., and Interrupt En. Reg. Are accessable. 1 = Divisor Latch reg. is accessable.
6	Break Control (forces SOUT signal low if set)
5	Stick Parity. If set, even parity bit is logic 0, odd parity bit is logic 1
4	Parity Type 0 = Odd, 1 = Even
3	Parity Enable: 0 = Disabled, 1 = Enabled
2	Stop Bit: 0 = 1 stop bit, 1 = 2 stop bits
1,0	Word Size: 00 = 5 bits 10 = 7 bits 01 = 6 bits 11 = 8 bits

Modem Control Register, I/O Port 3FCh/2FCh

This register controls the modem signal lines

Bit	Function
7..5	Reserved
4	Internal Loopback Enabled (if set)
3	Serial Interface Interrupts Enabled (if set)
2	Reserved
1	RTS Signal Active (if set)
0	DTR Signal Active (if set)

Line Status Register, I/O Port 3FDh/2FDh (Read Only)

This register contains the status of the current data transfer. Bits <2..0> are cleared when read.

Bit	Function
7	Parity Error, Framing Error, or Break Cond. Exists (if set)
6	TX Holding Reg. and Transmitter Shift Reg. Are Empty (if set)
5	TX Holding Reg. Is Empty (if set)
4	Break Interrupt Has Occurred (if set)
3	Framing Error Has Occurred (if set
2	Parity Error Has Occurred (if set)
1	Overrun Error Has Occurred (if set)
0	Data Register Ready To Be Read (if set)

Modem Status Register, I/O Port 3FEh/2FEh (Read Only)

This register contains the status of the modem signal lines. A set bit indicates that the associated signal is active.

Bit	Function
7	DCD- Active
6	RI- Active
5	DSR Active
4	CTS Active
3	DCD- Changed Since Last Read
2	RI- Changed From Low to High Since Last Read
1	DSR- Has Changed State Since Last Read
0	CTS- Has Changed State Since Last Read

Scratch Pad Register, I/O Port 3FFh/2FFh

This register is not used in this system.

5.5 PARALLEL INTERFACE

The parallel interface provides connection to a peripheral device that has a compatible interface, the most common being a printer. The parallel interface function is integrated into the 87307 I/O controller component and provides bi-directional 8-bit parallel data transfers with a peripheral device. The parallel interface supports three modes of operation:

- Standard Parallel Port (SPP) mode
- Enhanced Parallel Port (EPP) mode
- Extended Capabilities Port (ECP) mode

These three modes provide complete support as specified for an IEEE 1284 parallel port.

5.5.1 STANDARD PARALLEL PORT MODE

The Standard Parallel Port (SPP) mode uses software-based protocol and includes two sub-modes of operation, compatible and extended, both of which can provide data transfers up to 150 KB/s. In the compatible mode, CPU write data is simply presented on the eight data lines. A CPU read of the parallel port yields the last data byte that was written.

The following steps define the standard procedure for communicating with a printing device:

1. The system checks the Printer Status register. If the Busy, Paper Out, or Printer Fault signals are indicated as being active, the system either waits for a status change or generates an error message.
2. The system sends a byte of data to the Printer Data register, then pulses the printer STROBE signal (through the Printer Control register) for at least 500 ns.
3. The system then monitors the Printer Status register for acknowledgment of the data byte before sending the next byte.

In extended mode, a direction control bit (CTR 37Ah, bit <5>) controls the latching of output data while allowing a CPU read to fetch data present on the data lines, thereby providing bi-directional parallel transfers to occur.

The SPP mode uses three registers for operation: the Data register (DTR), the Status register (STR) and the Control register (CTR). Address decoding in SPP mode includes address lines A0 and A1.

5.5.2 ENHANCED PARALLEL PORT MODE

In Enhanced Parallel Port (EPP) mode, increased data transfers are possible (up to 2 MB/s) due to a hardware protocol that provides automatic address and strobe generation. EPP revisions 1.7 and 1.9 are both supported. For the parallel interface to be initialized for EPP mode, a negotiation phase is entered to detect whether or not the connected peripheral is compatible with EPP mode. If compatible, then EPP mode can be used. In EPP mode, system timing is closely coupled to EPP timing. A watchdog timer is used to prevent system lockup.

Five additional registers are available in EPP mode to handle 16- and 32-bit CPU accesses with the parallel interface. Address decoding includes address lines A0, A1, and A2.

5.5.3 EXTENDED CAPABILITIES PORT MODE

The Extended Capabilities Port (ECP) mode, like EPP, also uses a hardware protocol-based design that supports transfers up to 2 MB/s. Automatic generation of addresses and strobes as well as Run Length Encoding (RLE) decompression is supported by ECP mode. The ECP mode includes a bi-directional FIFO buffer that can be accessed by the CPU using DMA or programmed I/O. For the parallel interface to be initialized for ECP mode, a negotiation phase is entered to detect whether or not the connected peripheral is compatible with ECP mode. If compatible, then ECP mode can be used.

Ten control registers are available in ECP mode to handle transfer operations. In accessing the control registers, the base address is determined by address lines A2-A9, with lines A0, A1, and A10 defining the offset address of the control register. Registers used for FIFO operations are accessed at their base address + 400h (i.e., if configured for LPT1, then 378h + 400h = 778h).

The ECP mode includes several sub-modes as determined by the Extended Control register. Two submodes of ECP allow the parallel port to be controlled by software. In these modes, the FIFO is cleared and not used, and DMA and RLE are inhibited.

5.5.4 PARALLEL INTERFACE PROGRAMMING

5.5.4.1 Parallel Interface Configuration

The parallel interface must be configured for a specific address range (LPT1, LPT2, etc.) and also must be enabled before it can be used. When configured for EPP or ECP mode, additional considerations must be taken into account. Address selection, enabling, and EPP/ECP mode parameters of the parallel interface are affected through the PnP configuration registers of the 87307 I/O controller. Address selection and enabling are automatically done by the BIOS during POST but can also be accomplished with the Setup utility and other software.

The PnP configuration registers are accessed through I/O registers 15Ch (index) and 15Dh (data). The parallel interface is initiated by firmware selecting logical device 4 of the 87307. This is accomplished by the following sequence:

1. Write 07h to I/O register 15Ch.
2. Write 04h to I/O register 15Dh (for selecting the parallel interface).
3. Write 30h to I/O register 15Ch.
4. Write 01h to I/O register 15Dh (this activates the interface).

The parallel interface configuration registers are listed in the following table:

Table 5-13.
Parallel Interface Configuration Registers

Index Address	Function	R/W	Reset Value
30h	Activate	R/W	01h
31h	I/O Range Check	R/W	00h
60h	Base Address MSB	R/W	02h
61h	Base Address LSB	R/W	78h
70h	Interrupt Select	R/W	07h
71h	Interrupt Type	R/W	00h
74h	DMA Channel Select	R/W	04h
75h	Report DMA Assignment	RO	04h
F0h	Configuration Data	R/W	--

5.5.4.2 Parallel Interface Control

The BIOS function INT 17 provides simplified control of the parallel interface. Basic functions such as initialization, character printing, and printer status are provide by subfunctions of INT 17. The parallel interface is controllable by software through a set of I/O mapped registers. The number and type of registers available depends on the mode used (SPP, EPP, or ECP). Table 5-14 lists the parallel registers and associated functions based on mode.

Table 5-14.
Parallel Interface Control Registers

Register	I/O Address	SPP Mode Ports	EPP Mode Ports	ECP Mode Ports
Data	Base	LPT1,2,3	LPT1,2	LPT1,2,3
Status	Base + 1h	LPT1,2,3	LPT1,2	LPT1,2,3
Control	Base + 2h	LPT1,2,3	LPT1,2	LPT1,2,3
Address	Base + 3h	--	LPT1,2	--
Data Port 0	Base + 4h	--	LPT1,2	--
Data Port 1	Base + 5h	--	LPT1,2	--
Data Port 2	Base + 6h	--	LPT1,2	--
Data Port 3	Base + 7h	--	LPT1,2	--
Parallel Data FIFO	Base + 400h	--	--	LPT1,2,3
ECP Data FIFO	Base + 400h	--	--	LPT1,2,3
Test FIFO	Base + 400h	--	--	LPT1,2,3
Configuration Register A	Base + 400h	--	--	LPT1,2,3
Configuration Register B	Base + 401h	--	--	LPT1,2,3
Extended Control Register	Base + 402h	--	--	LPT1,2,3

Base Address:
LPT1 = 378h
LPT2 = 278h
LPT3 = 3BCh

The following paragraphs describe the individual registers. Note that only the LPT1-based addresses are given in these descriptions.

Data Register, I/O Port 378h

Data written to this register is presented to the data lines D0-D7. A read of this register when in SPP-compatible mode yields the last byte written. A read while in SPP-extended or ECP mode yields the status of data lines D0-D7 (i.e., receive data).

In ECP mode in the forward (output) direction, a write to this location places a tagged command byte into the FIFO and reads have no effect.

Status Register, I/O Port 379h, Read Only

This register contains the current printer status. Reading this register clears the interrupt condition of the parallel port.

Bit	Function
7	Printer Busy (if 0)
6	Printer Acknowledgment Of Data Byte (if 0)
5	Printer Out Of Paper (if 1)
4	Printer Selected/Online (if 1)
3	Printer Error (if 0)
2	Reserved
1	EPP Interrupt Occurred (if set while in EPP mode)
0	EPP Timeout Occurred (if set while in EPP mode)

Control Register, I/O Port 37Ah

This register provides the printer control functions.

Bit	Function
7,6	Reserved
5	Direction Control for PS/2 and ECP Modes: 0 = Forward. Drivers enabled. Port writes to peripheral (default) 1 = Backward. Tristates drivers and data is read from peripheral
4	Acknowledge Interrupt Enable 0 = Disable ACK interrupt 1 = Enable interrupt on rising edge of ACK
3	Printer Select (if 0)
2	Printer Initialize (if 1)
1	Printer Auto Line Feed (if 0)
0	Printer Strobe (if 0)

Address Register, I/O Port 37Bh (EPP Mode Only)

This register is used for selecting the EPP register to be accessed.

Data Port Registers 0-3, I/O Ports 37C-Fh (EPP Mode Only)

These registers are used for reading/writing data. Port 0 is used for all transfers. Ports 1-3 are used for transferring the additional bytes of 16- or 32-bit transfers through port 0.

FIFO Register, I/O Port 7F8h (ECP Mode Only)

While in ECP/forward mode, this location is used for filling the 16-byte FIFO with data bytes. Reads have no effect (except when used in Test mode). While in ECP/backward mode, reads yield data bytes from the FIFO.

Configuration Register A, I/O Port 7F8h (ECP Mode Only)

A read of this location yields 10h, while writes have no effect.

Configuration Register B, I/O Port 7F9h (ECP Mode, Read Only)

A read of this location yields the status defined as follows:

Bit	Function
7	Reserved (always 0)
6	Status of Selected IRQ*n*.
5,4	Selected IRQ Indicator: 00 = IRQ7 11 = IRQ5 All other values invalid.
3	Reserved (always 1)
2..0	Reserved (always 000)

Extended Control Register B, I/O Port 7FAh (ECP ModeOnly)

This register defines the ECP mode functions.

Bit	Function
7..5	ECP Submode Select: 000 = Standard forward mode (37Ah <5> forced to 0). Writes are controlled by software and FIFO is reset. 001 = PS/2 mode. Reads and writes are software controlled and FIFO is reset. 010 = Parallel Port FIFO forward mode (37Ah <5> forced to 0). Writes are hardware controlled. 011 = ECP FIFO mode. Direction determined by 37Ah, <5>. Reads and writes are hardware controlled.
4	ECP Interrupt Mask: 0 = Interrupt is generated on ERR- assertion. 1 = Interrupt is inhibited.
3	ECP DMA Enable/Disable. 0 = Disabled 1 = Enabled
2	ECP Interrupt Generation with DMA 0 = Enabled 1 = Disabled
1	FIFO Full Status (Read Only) 0 = Not full (at least 1 empty byte 1 = Full
0	FIFO Empty Status (Read Only) 0 = Not empty (contains at least 1 byte) 1 = Empty

5.5.5 PARALLEL INTERFACE CONNECTOR

Figure 5-4 and Table 5-15 show the connector and pinout of the parallel inrteface connector.

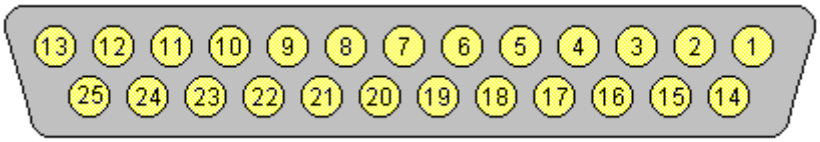


Figure 5–5. Parallel Interface Connector (Female DB-25 as viewed from rear of chassis)

Table 5-15.
DB-25 Parallel Connector Pinout

Pin	Signal	Description	Pin	Signal	Description
1	STB-	Strobe	14	LF-	Line Feed
2	D0	Data 0	15	ERR-	Error
3	D1	Data 1	16	INIT-	Initialize Paper
4	D2	Data 2	17	SLCTIN-	Select In
5	D3	Data 3	18	GND	Ground
6	D4	Data 4	19	GND	Ground
7	D5	Data 5	20	GND	Ground
8	D6	Data 6	21	GND	Ground
9	D7	Data 7	22	GND	Ground
10	ACK-	Acknowledge	23	GND	Ground
11	BSY	Busy	24	GND	Ground
12	PE	Paper End	25	GND	Ground
13	SLCT	Select	--	--	--

5.6 KEYBOARD/POINTING DEVICE INTERFACE

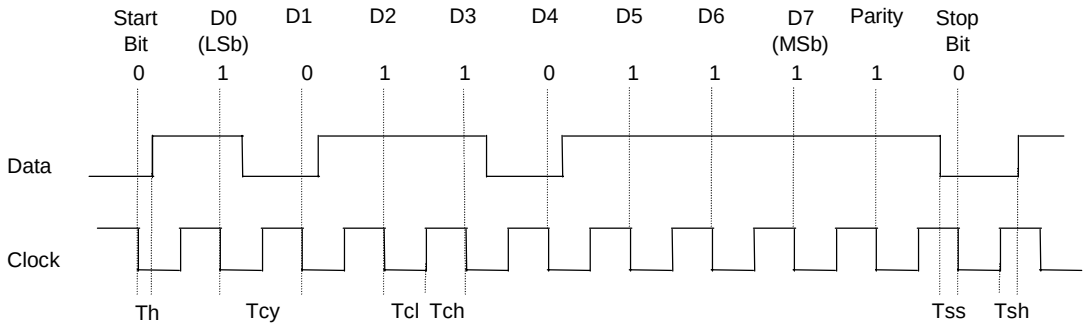
The keyboard/pointing device interface provides the connection of an enhanced keyboard and a mouse using PS/2-type connections. The keyboard/pointing device interface function is provided by the 87307 I/O controller component, which integrates 8042-compatible keyboard controller logic (hereafter referred to as simply the "8042") to communicate with the keyboard and pointing device using bi-directional serial data transfers. The 8042 handles scan code translation and password lock protection for the keyboard as well as communications with the pointing device. This section describes the interface itself. The keyboard is discussed in the Appendix C.

5.6.1 KEYBOARD INTERFACE OPERATION

The data/clock link between the 8042 and the keyboard is uni-directional for Keyboard Mode 1 and bi-directional for Keyboard Modes 2 and 3. (These modes are discussed in detail in Appendix C). This section describes Mode 2 (the default) mode of operation.

Communication between the keyboard and the 8042 consists of commands (originated by either the keyboard or the 8042) and scan codes from the keyboard. A command can request an action or indicate status. The keyboard interface uses IRQ1 to get the attention of the CPU.

The 8042 can send a command to the keyboard at any time. When the 8042 wants to send a command, the 8042 clamps the clock signal from the keyboard for a minimum of 60 us. If the keyboard is transmitting data at that time, the transmission is allowed to finish. When the 8042 is ready to transmit to the keyboard, the 8042 pulls the data line low, causing the keyboard to respond by pulling the clock line low as well, allowing the start bit to be clocked out of the 8042. The data is then transferred serially, LSb first, to the keyboard (Figure 5-5). An odd parity bit is sent following the eighth data bit. After the parity bit is received, the keyboard pulls the data line low and clocks this condition to the 8042. When the keyboard receives the stop bit, the clock line is pulled low to inhibit the keyboard and allow it to process the data.



Parameter	Minimum	Maximum
Tcy (Cycle Time)	0 us	80 us
Tcl (Clock Low)	25 us	35 us
Tch (clock High)	25 us	45 us
Th (Data Hold)	0 us	25 us
Tss (Stop Bit Setup)	8 us	20 us
Tsh (Stop Bit Hold)	15 us	25 us

Figure 5–6. 8042-To-Keyboard Transmission of Code EDh, Timing Diagram

Control of the data and clock signals is shared by the 8042and the keyboard depending on the originator of the transferred data. Note that the clock signal is always generated by the keyboard. After the keyboard receives a command from the 8042, the keyboard returns an ACK code. If a parity error or timeout occurs, a Resend command is sent to the 8042.

Table 5-16 lists and describes commands that can be issued by the 8042 to the keyboard.

Table 5-16.
8042-To-Keyboard Commands

Command	Value	Description
Set/Reset Status Indicators	EDh	Enables LED indicators. Value EDh is followed by an option byte that specifies the indicator as follows: Bits <7..3> not used Bit <2>, Caps Lock (0 = off, 1 = on) Bit <1>, NUM Lock (0 = off, 1 = on) Bit <0>, Scroll Lock (0 = off, 1 = on)
Echo	EEh	Keyboard returns EEh when previously enabled.
Invalid Command	EFh/F1h	These commands are not acknowledged.
Select Alternate Scan Codes	F0h	Instructs the keyboard to select another set of scan codes and sends an option byte after ACK is received: 01h = Mode 1 02h = Mode 2 03h = Mode 3
Read ID	F2h	Instructs the keyboard to stop scanning and return two keyboard ID bytes.
Set Typematic Rate/Display	F3h	Instructs the keyboard to change typematic rate and delay to specified values: Bit <7>, Reserved - 0 Bits <6,5>, Delay Time 00 = 250 ms 01 = 500 ms 10 = 750 ms 11 = 1000 ms Bits <4..0>, Transmission Rate: 00000 = 30.0 ms 00001 = 26.6 ms 00010 = 24.0 ms 00011 = 21.8 ms : 11111 = 2.0 ms
Enable	F4h	Instructs keyboard to clear output buffer and last typematic key and begin key scanning.
Default Disable	F5h	Resets keyboard to power-on default state and halts scanning pending next 8042 command.
Set Default	F6h	Resets keyboard to power-on default state and enable scanning.
Set Keys - Typematic	F7h	Clears keyboard buffer and sets default scan code set. [1]
Set Keys - Make/Brake	F8h	Clears keyboard buffer and sets default scan code set. [1]
Set Keys - Make	F9h	Clears keyboard buffer and sets default scan code set. [1]
Set Keys - Typematic/Make/Brake	FAh	Clears keyboard buffer and sets default scan code set. [1]
Set Type Key - Typematic	FBh	Clears keyboard buffer and prepare to receive key ID. [1]
Set Type Key - Make/Brake	FCh	Clears keyboard buffer and prepare to receive key ID. [1]
Set Type Key - Make	FDh	Clears keyboard buffer and prepare to receive key ID. [1]
Resend	FEh	8042 detected error in keyboard transmission.
Reset	FFh	Resets program, runs keyboard BAT, defaults to Mode 2.

Note:
[1] Used in Mode 3 only.

5.6.2 POINTING DEVICE INTERFACE OPERATION

The pointing device (typically a mouse) connects to a 6-pin DIN-type connector that is identical to the keyboard connector both physically and electrically. The operation of the interface (clock and data signal control) is the same as for the keyboard. The pointing device interface uses the IRQ12 interrupt.

5.6.3 KEYBOARD/POINTING DEVICE INTERFACE PROGRAMMING

5.6.3.1 8042 Configuration

The keyboard/pointing device interface must be enabled and configured for a particular speed before it can be used. Enabling and speed parameters of the 8042 logic are affected through the PnP configuration registers of the 87307 I/O controller. Enabling and speed control are automatically set by the BIOS during POST but can also be accomplished with the Setup utility and other software.

The PnP configuration registers are accessed through I/O registers 15Ch (index) and 15Dh (data). The keyboard and mouse interfaces are initiated by firmware selecting logical device 0 or 1 of the 87307. This is accomplished by the following sequence:

1. Write 07h to I/O register 15Ch.
2. Write 00h or 01h to I/O register 15Dh (for selecting the keyboard or mouse interface).
3. Write 30h to I/O register 15Ch.
4. Write 01h to I/O register 15Dh (this activates the interface).

The parallel interface configuration registers are listed in the following table:

Table 5-17.
Keyboard/Mouse Interface Configuration Registers

Index Address	Function	R/W	Reset Value [2]
30h	Activate	R/W	01h / 00h
31h	I/O Range Check [1]	R/W	00h / na
60h	Base Address MSB [1]	R/W	02h / na
61h	Base Address LSB [1]	R/W	78h / na
62h	Command Base Address MSB [1]	R/W	00h / na
63h	Command Base Address LSB [1]	R/W	00h / na
70h	Interrupt Select	R/W	01h / 0Ch
71h	Interrupt Type	R/W	01h / 01h
74h	DMA Channel Select	R/W	04h / 04h
75h	Report DMA Assignment	RO	04h / 04h
F0h	Configuration Data [1]	R/W	-- / na

NOTES:
[1] Keyboard I/F only.
[2] Keyboard I/F / Mouse I/F

5.6.3.2 8042 Control

The BIOS function INT 16 is typically used for controlling interaction with the keyboard. Sub-functions of INT 16 conduct the basic routines of handling keyboard data (i.e., translating the keyboard's scan codes into ASCII codes). The keyboard/pointing device interface is accessed by the CPU through I/O mapped ports 60h and 64h, which provide the following functions:

- Output buffer reads
- Input buffer writes
- Status reads
- Command writes

Ports 60h and 64h can be accessed using the IN instruction for a read and the OUT instruction for a write. Prior to reading data from port 60h, the "Output Buffer Full" status bit (64h, bit <0>) should be checked to ensure data is available. Likewise, before writing a command or data, the "Input Buffer Empty" status bit (64h, bit <1>) should also be checked to ensure space is available.

I/O Port 60h

I/O port 60h is used for accessing the input and output buffers. This register is used to send and receive data from the keyboard and the pointing device. This register is also used to send the second byte of multi-byte commands to the 8042 and to receive responses from the 8042 for commands that require a response.

A read of 60h by the CPU yields the byte held in the output buffer. The output buffer holds data that has been received from the keyboard and is to be transferred to the system.

A CPU write to 60h places a data byte in the input byte buffer and sets the CMD/ DATA bit of the Status register to DATA. The input buffer is used for transferring data from the system to the keyboard. All data written to this port by the CPU will be transferred to the keyboard **except** bytes that follow a multibyte command that was written to 64h

I/O Port 64h

I/O port 64h is used for reading the status register and for writing commands. A read of 64h by the CPU will yield the status byte defined as follows:

Bit	Function
7..4	General Purpose Flags.
3	CMD/DATA Flag (reflects the state of A2 during a CPU write). 0 = Data 1 = Command
2	General Purpose Flag.
1	Input Buffer Full. Set (to 1) upon a CPU write. Cleared by IN A, DBB instruction.
0	Output Buffer Full (if set). Cleared by a CPU read of the buffer.

A CPU write to I/O port 64h places a command value into the input buffer and sets the CMD/DATA bit of the status register (bit <3>) to CMD.

Table 5-18 lists the commands that can be sent to the 8042 by the CPU. The 8042 uses IRQ1 for gaining the attention of the CPU.

Table 5-18.
CPU Commands To The 8042

Value	Command Description
20h	Put current command byte in port 60h.
60h	Load new command byte. This is a two-byte operation described as follows: 1. Write 60h to port 64h. 2. Write the command byte to port 60h as follows: Bit <7> Reserved <6> Keyboard Code Conversion 0 = Do not convert codes 1 = Convert codes to 9-bit 8088/8086-compatible format Bit <5> Pointing Device Enable 0 = Enable pointing device 1 = Disable pointing device Bit <4> Keyboard Enable 0 = Enable keyboard 1 = Disable keyboard Bit <3> Reserved Bit <2> System Flag 0 = Cold boot 1 = CPU reset (exit from protected mode) Bit <1> Pointing Device Interrupt Enable 0 = Disable interrupt 1 = Enable interrupt Bit <0> Keyboard Interrupt Enable 0 = Disable interrupt 1 = Enable interrupt
A4h	Test password installed. Tests whether or not a password is installed in the 8042: If FAh is returned, password is installed. If F1h is returned, no password is installed.
A5h	Load password. This multi-byte operation places a password in the 8042 using the following manner: 1. Write A5h to port 64h. 2. Write each character of the password in 9-bit scan code (translated) format to port 60h. 3. Write 00h to port 60h.
A6h	Enable security. This command places the 8042 in password lock mode following the A5h command. The correct password must then be entered before further communication with the 8042 is allowed.
A7h	Disable pointing device. This command sets bit <5> of the 8042 command byte, pulling the clock line of the pointing device interface low.
A8h	Enable pointing device. This command clears bit <5> of the 8042 command byte, activating the clock line of the pointing device interface.
A9h	Test the clock and data lines of the pointing device interface and place test results in the output buffer. 00h = No error detected 01h = Clock line stuck low 02h = Clock line stuck high 03h = Data line stuck low 04h = Data line stuck high
AAh	Initialization. This command causes the 8042 to inhibit the keyboard and pointing device and places 55h into the output buffer.
ABh	Test the clock and data lines of the keyboard interface and place test results in the output buffer. 00h = No error detected 01h = Clock line stuck low 02h = Clock line stuck high 03h = Data line stuck low 04h = Data line stuck high
ADh	Disable keyboard command (sets bit <4> of the 8042 command byte).
AEh	Enable keyboard command (clears bit <4> of the 8042 command byte).

Continued

Table 5-18. CPU Commands To The 8042 *(Continued)*

Value	Command Description
C0h	Read input port of the 8042. This command directs the 8042 to transfer the contents of the input port to the output buffer so that they can be read at port 60h. The contents are as follows: Bit <7> Password Enable: 0 = Disabled 1 = Enabled Bit <6> External Boot Enable: 0 = Enabled 1 = Disabled Bit <5> Setup Enable: 0 = Enabled 1 = Disabled Bit <4> VGA Enable: 0 = Enabled 1 = Disabled Bit <3> Diskette Writes: 0 = Disabled 1 = Enabled Bit <2> Reserved Bit <1> Pointing Device Data Input Line Bit <0> Keyboard Data Input Line
C2h	Poll Input Port High. This command directs the 8042 to place bits <7..4> of the input port into the upper half of the status byte on a continous basis until another command is received.
C3h	Poll Input Port Low. This command directs the 8042 to place bits <3..0> of the input port into the lower half of the status byte on a continous basis until another command is received.
D0h	Read output port. This command directs the 8042 to transfer the contents of the output port to the output buffer so that they can be read at port 60h. The contents are as follows: Bit <7> Keyboard data stream Bit <6> Keyboard clock Bit <5> IRQ12 (pointing device interrupt) Bit <4> IRQ1 (keyboard interrupt) Bit <3> Pointing device clock Bit <2> Pointing device data Bit <1> A20 Control: 0 = Hold A20 low 1 = Enable A20 Bit <0> Reset Line Status; 0 = Inactive 1 = Active
D1h	Write output port. This command directs the 8042 to place the next byte written to port 60h into the output port (only bit <1> can be changed).
D2h	Echo keyboard data. Directs the 8042 to send back to the CPU the next byte written to port 60h as if it originated from the keyboard. No 11-to-9 bit translation takes place but an interrupt (IRQ1) is generated if enabled.
D3h	Echo pointing device data. Directs the 8042 to send back to the CPU the next byte written to port 60h as if it originated from the pointing device. An interrupt (IRQ12) is generated if enabled.
D4h	Write to pointing device. Directs the 8042 to send the next byte written to 60h to the pointing device.
E0h	Read test inputs. Directs the 8042 to transfer the test bits 1 and 0 into bits <1,0> of the output buffer.
F0h-FFh	Pulse output port. Controls the pulsing of bits <3..0> of the output port (0 = pulse, 1 = don't pulse). Note that pulsing bit <0> will reset the system.

5.6.4 KEYBOARD/POINTING DEVICE INTERFACE CONNECTOR

There are separate connectors for the keyboard and pointing device. Both connectors are identical both physically and electrically. Figure 5-6 and Table 5-19 show the connector and pinout of the keyboard/pointing device interface connectors.

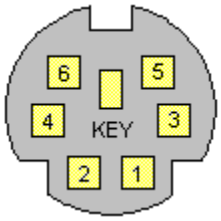


Figure 5–7. Keyboard or Pointing Device Interface Connector (as viewed from rear of chassis)

Table 5-19.
Keyboard/Pointing Device Connector Pinout

Pin	Signal	Description	Pin	Signal	Description
1	DATA	Data	4	+ 5 VDC	Power
2	NC	Not Connected	5	CLK	Clock
3	GND	Ground	6	NC	Not Connected

5.7 ETHERNET INTERFACE

The system board integrates an Ethernet interface that supports both 10 and 100 Mbps Ethernet communications using IEEE 802.3 (ISO 8802-3) protocol. Two connection options are available; an RJ-45 jack for twisted-pair Ethernet (TPE) systems (10BaseT and 100BaseTX) and an AUI connector for a direct 10BaseT connection or to a 10Base2 connection through and AUI-to-BNC adapter. The Ethernet interface (Figure 5-9) is based on the Texas Instruments TLAN3.1 component, which operates off the PCI bus and features auto-switching between 10 and 100 Mb/s interfaces.

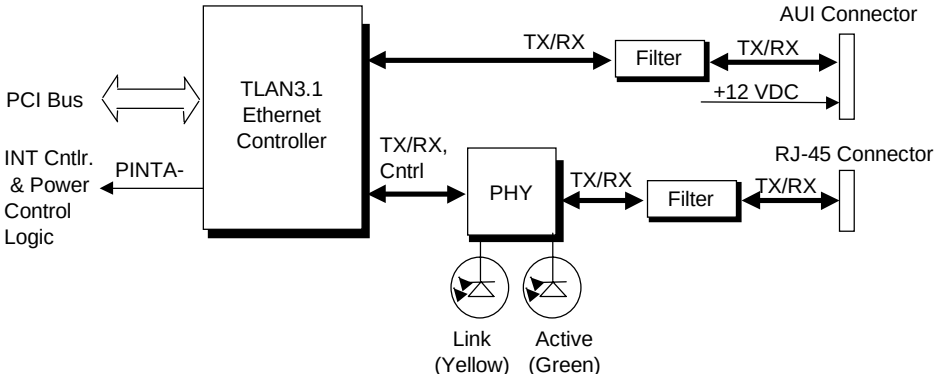


Figure 5–8. Ethernet Interface Block Diagram

The RJ-45 connctor is the default port, which is the required connection if Remote Wakeup operation or 10/100 autosensing is desired. Note also that the LED indicators are operational only for the RJ-45 interface. The LEDs provide the following indications:

Link LED (yellow) - Indicates reception of link pulses in 10 Mbs mode, indicates scrambler lock and valid idle code reception during 100 Mbs mode.

Active LED (green) - Indicates network activity.

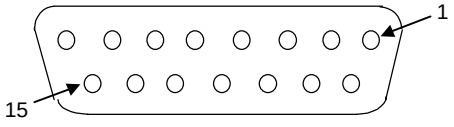
The network interface controller supports Remote Wakeup using the Magic Packet method of waking up a system unit that is powered down (the NIC logic is powered by +5 AUX, which is active as long as the system is receiving AC line voltage). With Remote Wakeup feature enabled, a received Magic Packet results in the PINTA- signal being asserted (low) and routed to power control logic, which in turn activates the power supply (refer to Chapter 7, “Power and Signal Distribution” for a discussion of the power control logic).

5.7.1 NIC CONFIGURATION/CONTROL

The NIC is a PCI device and configured through PCI configuration space registers. The NIC is controlled through I/O registers mapped in the 300h-30Fh range.

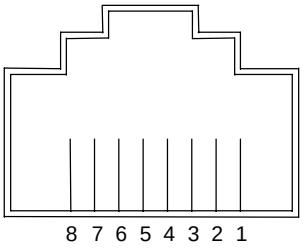
5.7.2 NIC CONNECTORS

The network interface provides two choices of connection to a LAN system as shown in the following figures.



Pin	Description	Pin	Description
1	Ground	9	Control In RTN
2	Control In	10	TX Data RTN
3	TX Data	11	Ground
4	Ground	12	RX Data RTN
5	RX Data	13	+12 VDC
6	Ground	14	Ground
7	n/c	15	n/c
8	Ground		

Figure 5–9. Ethernet AUI Connector (DB-15, viewed from rear)



Pin	Description
1	Transmit
2	Transmit Low
3	Receive
6	Receive Low

Figure 5–10. Ethernet RJ-45 Connector

5.8 UNIVERSAL SERIAL BUS INTERFACE

The Universal Serial Bus (USB) interface provides up to 12 Mb/s data transfers between the host system and peripherals designed with a compatible USB interface. This high speed interface supports hot-plugging of compatible devices, making possible system configuration changes without powering down or even rebooting systems. The USB interface supports both isochronous and asynchronous communications, and integrates a 5 VDC power bus that can eliminate the need for external powering of small remote peripherals.

5.8.1 USB CONFIGURATION

The USB interface functions as a PCI device (20) within the 82586 component (function 2) and is configured using PCI Configuration Registers as listed in Table 5-20.

Table 5-20.
USB PCI Configuration Registers (82586, Function 2)

PCI Config. Addr.	Register	Reset Value
00h-01h	Vender ID	1106h
02h-03h	Device ID	3038h
04h-05h	PCI Command	0000h
06h-07h	PCI Status	0280h
08h	Revision ID	00h
09h	Programming I/F	00h
0Ah	Sub Class Code	03h
0Bh	Base Class Code	0Ch
0Dh	Latency Timer	00h
0Eh	Header Type	80h
24h-27h	I/O Space Base Address	All 0's
3Ch	Interrupt Line	00h
3Dh	Interrupt Pin	04h
40h	Miscellaneous Control 1	
41h	Miscellaneous Control 2	
60h	Serial Base Release Number	00h
C0-C1h	Legacy Support Reg. (compliant w/UHCI v1.1)	2000h

5.8.2 USB CONTROL

The USB is controlled through I/O registers as listed in table 5-21.

Table 5-21.
USB Control Registers

I/O Addr.	Register
00, 01h	Command
02, 03h	Status
04, 05h	Interupt Enable
06, 07	Frame No.
08, 0B	Frame List Base Address
0Ch	Start of Frame Modify
10, 11h	Port 1 Status/Control
12, 13h	Port 2 Status/Control

5.8.3 USB CONNECTOR

The USB interface provides two connectors.

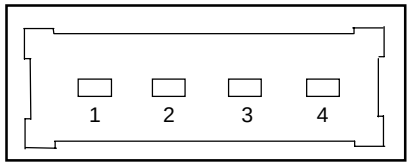


Figure 5–11. Universal Serial Bus Connector (one of two as viewed from rear of chassis)

Table 5-22.
USB Connector Pinout

Pin	Signal	Description	Pin	Signal	Description
1	Vcc	+5 VDC	3	USB+	Data (plus)
2	USB-	Data (minus)	4	GND	Ground

Chapter 6
GRAPHICS SUBSYSTEM

6.1 INTRODUCTION

This chapter describes the graphics subsystem. The graphics subsystem is integrated onto the system board and operates as a PCI peripheral device. Topics covered in this chapter include:

Table 6-1 provides an overview of the graphics subsystem.

Table 6-1.
Graphics Subsystem Overview

Graphics Controller:	S3 Trio64 V2-GX
Graphics Memory:	2 MB SGRAM
Maximum Resolution:	1280x1024 w/256 colors @ 85 Hz

The standard graphics controller used in the Deskpro 4000N/4000S Series is a PCI peripheral that can be identified by software reading the "Vendor ID" and "Device ID" words in PCI configuration address space locations 00h and 02h respectively. The values are as follows:

Vendor ID	Device ID	Graphics ASIC	System
5333h	8901h	S3 Trio64V2-GX	Pentium MMX-based

6.2 SUBSYSTEM DESCRIPTION

The graphics subsystem consists of the S3 Trio64V2/GX graphics controller and two megabytes of SGRAM for the frame buffer memory. The graphics BIOS code is included in the system BIOS ROM. This subsystem provides full multimedia support (with software MPEG acceleration) for a maximum resolution of 1024x768 with 256 colors @ 85 Hz, non-interlaced.

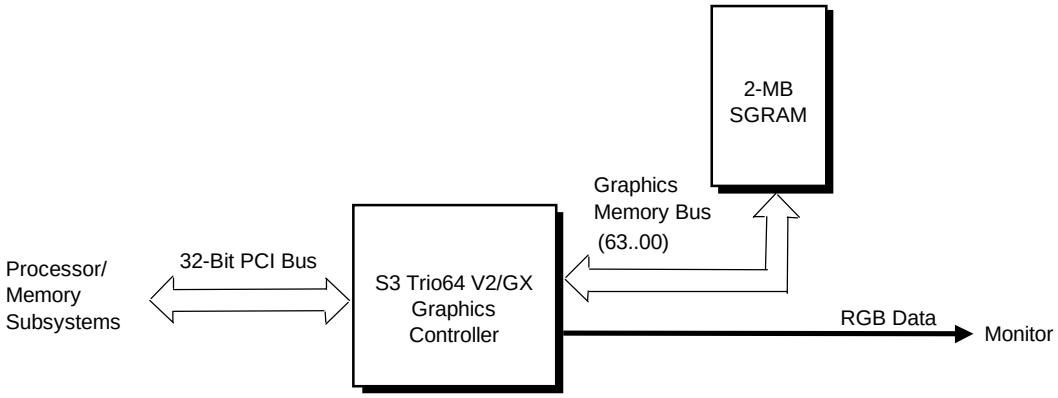


Figure 6–1. S3 Trio64V2/GX-Based Graphics Subsystem, Block diagram

6.2.1 S3 TRIO64V2/GX GRAPHICS CONTROLLER

The S3 Trio64V2/GX graphics controller provides most of the functionality of the integrated graphics subsystem and contains the features listed below:

- Quick Draw support
- DCI and DirectX video support
- MS DirectDraw support
- Horizontal and vertical interpolation
- On-the-fly stretching/blending of video streams
- Double-buffering for seamless video
- 170-MHz 24-bit (true color) RAMDAC
- Designed for SGRAM operation
- VESA DDC1 and DDC2B support

6.2.2 S3 TRIO64V2/GX GRAPHICS CONFIGURATIONS

The Trio64V2/GX-based graphics subsystem directly supports standard CGA, EGA, and VGA modes. Using the supplied drivers, the controller with this system supports the extended VGA modes listed in the table below. All modes are supported by the Win NT3.51 and 4.0, Win 3.1 and 95, and OS/2 operating systems unless otherwise noted.

Table 6-2.
S3 Trio64V2/GX-Based Subsystem
Extended VGA Display Modes

Pixel Resolutiun	Bits Per Pixel	Color Depth	Notes
640 x 480	8	256	
640 x 480	16	65 K	
640 x 480	24	16.7 M	[1]
640 x 480	32	16.7 M	
800 x 600	8	256	
800 x 600	16	65 K	
800 x 600	32	16.7 M	[1]
1024 x 768	8	256	
1024 x 768	16	65 K	
1152 x 864	8	256	[1] [2]
1280 x 1024	8	256	[2]

NOTES:

Operation is non-Interleaved for all modes with a refresh rate of up to 85 Hz.
[1] Mode not supported by OS/2.
[2] Mode not supported by Win 3.1.

6.2.3 S3 TRIO64V2/GX GRAPHICS SUBSYSTEM PROGRAMMING

The S3 Trio64V2/GX is compatible with software written for VGA, EGA, and CGA modes. Drivers are supplied for control of graphics (GUI) accelerator engines used in extended VGA modes.

6.2.3.1 Subsystem Configuration

The graphics subsystem works off the PCI bus and is configured through the Trio64V2's PCI configuration space registers (listed in Table 6-3) using PCI protocol. These registers are configured by BIOS during POST to the default configuration.

Table 6-3.
S3 Trio64V2/GX PCI Configuration Space Registers

PCI Config. Address	Function	PCI Config. Address	Function
00h-03h	Vender ID (5333h)/Device ID (8901h)	10h-13h	I/O Base Address
04h, 05h	PCI Command	30h, 31h	Expansion ROM Base Address
08h, 09h	Status	3Ch, 3Dh	Interrupt Line / Interrupt Pin

For a discussion of accessing PCI configuration space registers refer to chapter 4. For a detailed description of registers refer to the *S3 Trio64V2-GX Manual*.

6.2.3.2 Subsystem Control

Tables 6-4 and 6-5 list the control registers of the S3 Trio64V2/GX. For a detailed discription of the control registers refer to appropriate S3 documentation.

Table 6-4.
Standard VGA Mode I/O Mapping

I/O Address	Function	I/O Address	Function
3B5.00..26h*	CRT Controller (mono)	3C6h..3C9h	RAMDAC
3BAh	VSYNC Control, Display Status	3CAh	Read VSYNC Status
3C1.00..14h*	Attribute Controller	3CCh	Misc. Control, Read
3C2h	Misc. Control / Status	3CF.00..08h	Graphics Controller
3C5h.00..04h*	Sequencer	3D5.00..26h*	CRT Controller (color)
--	--	3DAh	VSYNC Control, Display Status (color)

* Index at base minus 1 (i.e., if base is 3B5h, index is at 3B4h.

Table 6-5.
S3-Specific Control Register Mapping

I/O Address	Function	I/O Address	Function
3x5.2D..3Ch [1]	Extended VGA Registers	42E8h, 4AE8h	Enhanced Command Registers
3x5.40..4Fh [1]	Control Registers	8180h-81FCh	Streams Processor Registers
3x5.50..6Fh [1]	Extension Registers	82E8h-E2EAh	Enhanced Command Registers [2]
--	--	FF00h-FF40h	Local Peripheral Bus Registers

x = B, Monochrome
x = C, Color
[1] Index at 3x4h
[2] Addresses not contiguously used through range.

6.2.4 MONITOR POWER CONTROL

This system provides monitor power control for monitors that conform to the VESA display power management signaling protocol. This protocol defines different power consumption conditions and uses the HSYNC and VSYNC signals to select a monitor's power condition. Table 6-6 lists the monitor power conditions.

Table 6-6.
Monitor Power Management Conditions

HSYNC	VSYNC	Power Mode	Description
Active	Active	On	Monitor is completely powered up. If activated, the inactivity counter counts down during system inactivity and if allowed to tiemout, generates an SMI to initiate the Suspend mode.
Active	Inactive	Suspend	Monitor's high voltage section is turned off and CRT heater (filament) voltage is reduced from 6.6 to 4.4 VDC. The Off mode inactivity timer counts down from the preset value and if allowed to timeout, another SMI is generated and serviced, resulting in the monitor being placed into the Off mode. Wake up from Suspend mode is typically a few seconds.
Inactive	Inactive	Off	Monitor's high voltage section and heater circuitry is turned off. Wake up from Off mode is a little longer than from Suspend.

The timeout parameter set in the SIT record 03h and indexed at CMOS location 2Ch (bits <4..0>) represents the period of system I/O inactivity required to elapse before the monitor is placed into Suspend mode.

A separate timer function (enabled through CMOS location 1Fh, bit <1>) can be enabled to place the monitor into the Off mode after 45 minutes of being in Suspend mode.

6.2.5 CONNECTORS

The graphics subsystem provides a VGA monitor connector described in the following figure and table.

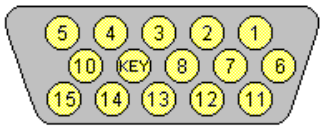


Figure 6–2. VGA Monitor Connector, (Female DB-15, as viewed from the rear of chassis).

Table 6-7.
DB-15 Monitor Connector Pinout

Pin	Signal	Description	Pin	Signal	Description
1	R	Red Analog	9	NC	Not Connected
2	G	Blue Analog	10	GND	Ground
3	B	Green Analog	11	Mon. ID	Monitor Identification
4	Mon ID	Monitor Identification	12	SDA	DDC2-B Data
5	GND	Ground	13	HSync	Horizontal Sync
6	R GND	Red Analog Ground	14	VSync	Vertical Sync
7	G GND	Blue Analog Ground	15	SCL	DDC2-B Clock
8	B GND	Green Analog Ground	--	--	--

Chapter 7
POWER and SIGNAL DISTRIBUTION

7.1 INTRODUCTION

This chapter describes the power supply and method of general power and signal distribution in the Compaq Deskpro 4000N and 4000S Personal Computers. All models use a 76-watt power supply assembly. Power distribution is basically similar in all models. Topics covered in this chapter include:

7.2 POWER SUPPLY ASSEMBLY/CONTROL

This system features a power supply that is controlled through programmable logic (Figure 7-1). This allows several options for how and when the system can be powered up.

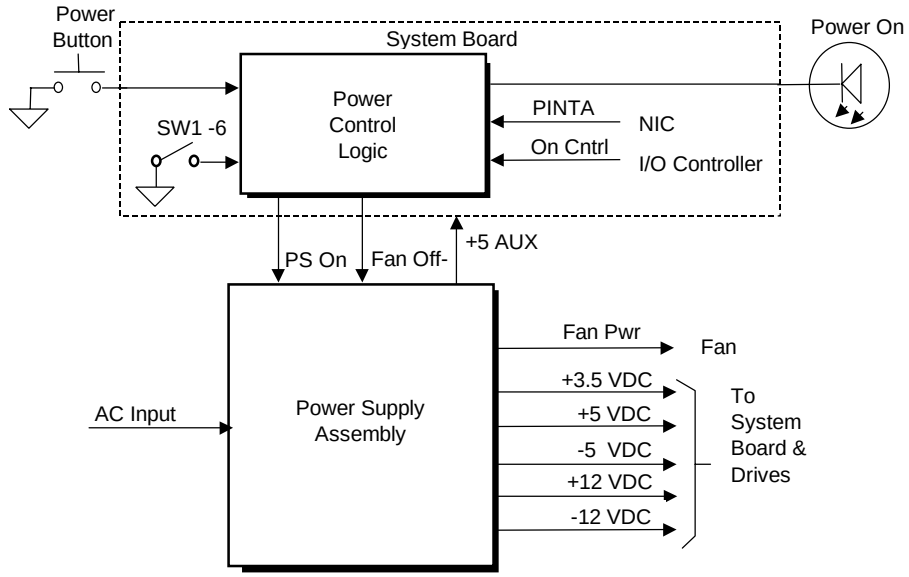


Figure 7–1. Power Supply Assembly, Block Diagram

7.2.1 POWER SUPPLY ASSEMBLY

The 76-watt power supply assembly is contained in a single unit that features a selectable input voltage of 90-132 VAC and 180-264 VAC. The power supply assembly provides +3.5 VDC, +5 VDC, -5 VDC, +12 VDC, and -12 VDC potentials for the system board, expansion board(s), and installed drives. These voltages are controlled by the PS On signal from the Power Control Logic.

A fault-detection circuit automatically shuts down the power supply when certain faults are detected. Faults that can trigger the protection circuitry include:

- Overvoltage - The +5 VDC output will activate the overvoltage crowbar circuit that triggers the protection circuit when the output exceeds +5.60 VDC to +6.80 VDC. The +3.5 VDC output will activate the overvoltage crowbar circuit when the output is sensed to be in the +3.7 VDC to +5.0 VDC range.
- Short Circuit - The protection circuit triggers if any power supply output is shorted to ground or to another output. This function reduces shock or fire hazard

In addition to the previously mentioned voltages, auxiliary +5 VDC (+5 AUX) is produced by the power supply assembly as long as the unit is plugged into a live AC outlet. The +5 AUX voltage is used by power control logic and the network interface controller.

Table 7-1 shows the specifications for the power supply.

Table 7-1.
Power Supply Assembly Specifications

Parameter	Tolerance/ Range	Min. Current Loading [1]	Max. Current	Surge Current [2]	Max. Ripple
Input Line Voltage:					
110 VAC Setting:	90 - 132 VAC	--	--	--	--
220 VAC Setting:	180-264 VAC	--	--	--	--
Line Frequency	47 - 63 Hz	--	--	--	--
Steady State Input (VAC) Current:	--	--	5.5 A	--	--
+3.5 VDC Output	+/- 1%	0.6 A	7.0 A	7.0 A	50 mV
+5 VDC Output	+/- 5 %	0.5 A	5.0 A	5.0 A	50 mV
+5 AUX Output	+/- 5 %	0.1 A	1.2 A	1.2 A	80 mV
+12 VDC Output	+/- 5 %	0.0 A	1.5 A	3.0 A	120 mV
-12 VDC Output	+/- 10 %	0.0 A	0.2 A	0.2 A	200 mV

NOTES:

[1] Minimum loading requirements must be met at all times to ensure normal operation and specification compliance.

[2] Surge duration no longer than 10 seconds and +12 tolerance +/- 10%.

The system fan is physically attached to and driven by the power supply. Fan speed is adjusted in a linear fashion (5.5-13.6 VDC) by the power supply. The power control logic also controls fan operation through an LM75 temperature sensor. This sensor controls the FAN OFF signal that indicates to the power supply to shut off the fan. A temperature sensor within the power supply can cause the power supply to override the FAN OFF signal if the ambient temperature of the power supply is too warm.

7.2.2 POWER CONTROL

The power supply assembly is controlled digitally by the PS On signal (Figure 7-1). When PS On is asserted (high), the Power Supply Assembly is activated. When PS On is de-asserted, the Power Supply Assembly (and the rest of the system) is off. The PS On signal is typically controlled through the Power Button, which can be set by software (Windows 95) to operate as either a standard On/Off button or as a Suspend button. The resultant action of pressing the power button depends on the programmed state of the power button.at that time and is described as follows:

System State	Pressed Power Button Results In:
Off	Negative pulse, of which the falling edge results in power control logic asserting PS On signal to Power Supply Assembly, which then initializes. Four-second counter is not active.
On, Advd. Power Disabled	Negative pulse, of which the rising edge causes power control logic to de-assert the PS On signal. Four-second counter is not active.
On, Advd. Power Enabled	Pressed and Released Under Four Seconds: Negative pulse, of which the falling edge causes power control logic to generate SMI-, set a bit in the SMI source register, set a bit for button status, and start four-second counter. Software should clear the button status bit within four seconds and the Suspend state is entered. If the status bit is not cleared by software in four seconds PS On is de-asserted and the power supply assembly shuts down (this condition is meant as a guard in case the OS is hung). Pressed and Held At least Four Seconds Before Release: If the button is held in for at least four seconds and then released, PS On is negated, de-activating the power supply.

The PS On signal can also be activated with a power “wake-up” of the system due to the following events:

Magic Packet - If the network interface controller is enabled for remote wake-up, reception of a “Magic Packet” results in the NIC component asserting the PINTA- signal to the power control logic, which in turn asserts the PS On signal and turns on the power supply assembly.

RTC Alarm/Modem Ring - These events (within the 87307 I/O controller) are programmable for power wake-up and can affect the assertion of the PS On signal through the power control logic.

> **NOTE:** The PS On signal can be configured to be asserted whenever the power supply assembly is connected to live AC by setting DIP SW1 position 6 to the “On” (closed or grounding) position. This condition overrides all other settings.

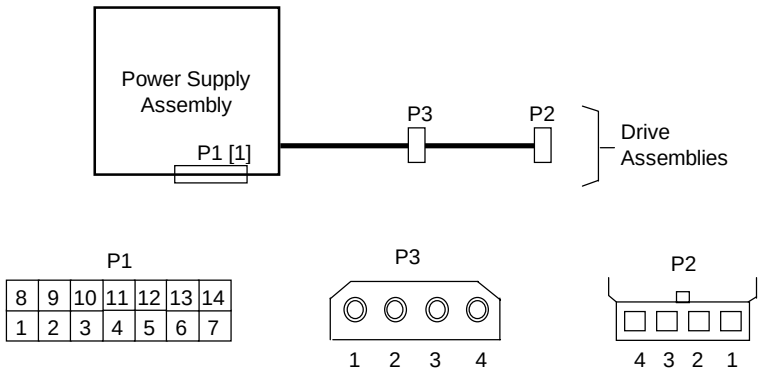
The power LED is normally on in a steady state with the system on. When the system is in a low power (suspend) condition the power LED is pulsed, causing it to blink at approximately a rate of 1-Hz. The blinking is affected through the power control logic

The power button can be inhibited by invoking BIOS call INT 15, AX=E828h, which is discussed in Chapter 8, “BIOS ROM.”

7.3 POWER DISTRIBUTION

7.3.1 3.5/5/12 VDC DISTRIBUTION

The power supply assembly includes a connector (P1) that mates directly with the system board connector (P17) when the assembly is installed. The power supply assembly also includes a cable assembly that routes +3.5 VDC, +5 VDC, -5 VDC, +12 VC, and -12 VDC to the individual drive assemblies.



Connector	Pin 1	Pin 2	Pin 3	Pin 4	Pin 5	Pin 6	Pin 7	Pin 8	Pin 9	Pin 10
P1	+3.5	+3.5RS	RTN	+5	RTN	+5	RTN	+3.5	-12	FO
P1 [2]	PS On	+5AUX	RS rtn	+12						
P2	+5	GND	GND	+12						
P3	+12	GND	GND	+5						

NOTES:

[1] Connector P1 mates directly with connector P17 on the system board.
[2] This row represents pins 11-14 of connector P1.
All + and - values are VDC.
RTN = Return (signal ground)
GND = Power ground
RS = Remote sense
FO = Fan off

Figure 7–2. Power Cable Diagram

7.3.2 LOW VOLTAGE DISTRIBUTION

The system board includes a provision for producing 2.5 VDC for microprocessors that require such a level for core power. The low voltage circuitry (Figure 7-3) consists of a power MOSFET and regulator components that produce 2.8 VDC, plus or minus 3.57%.

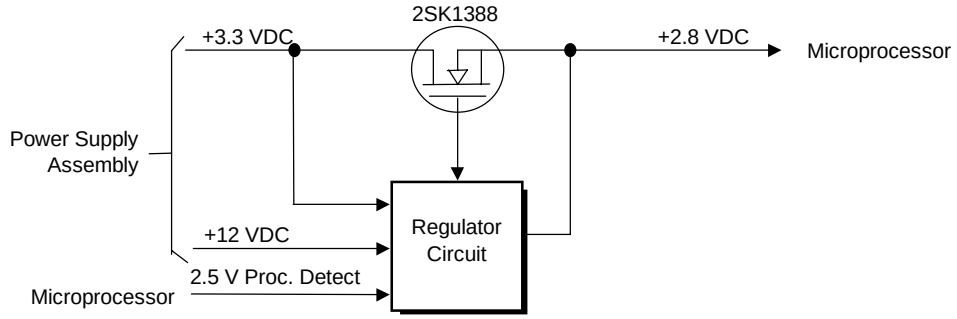
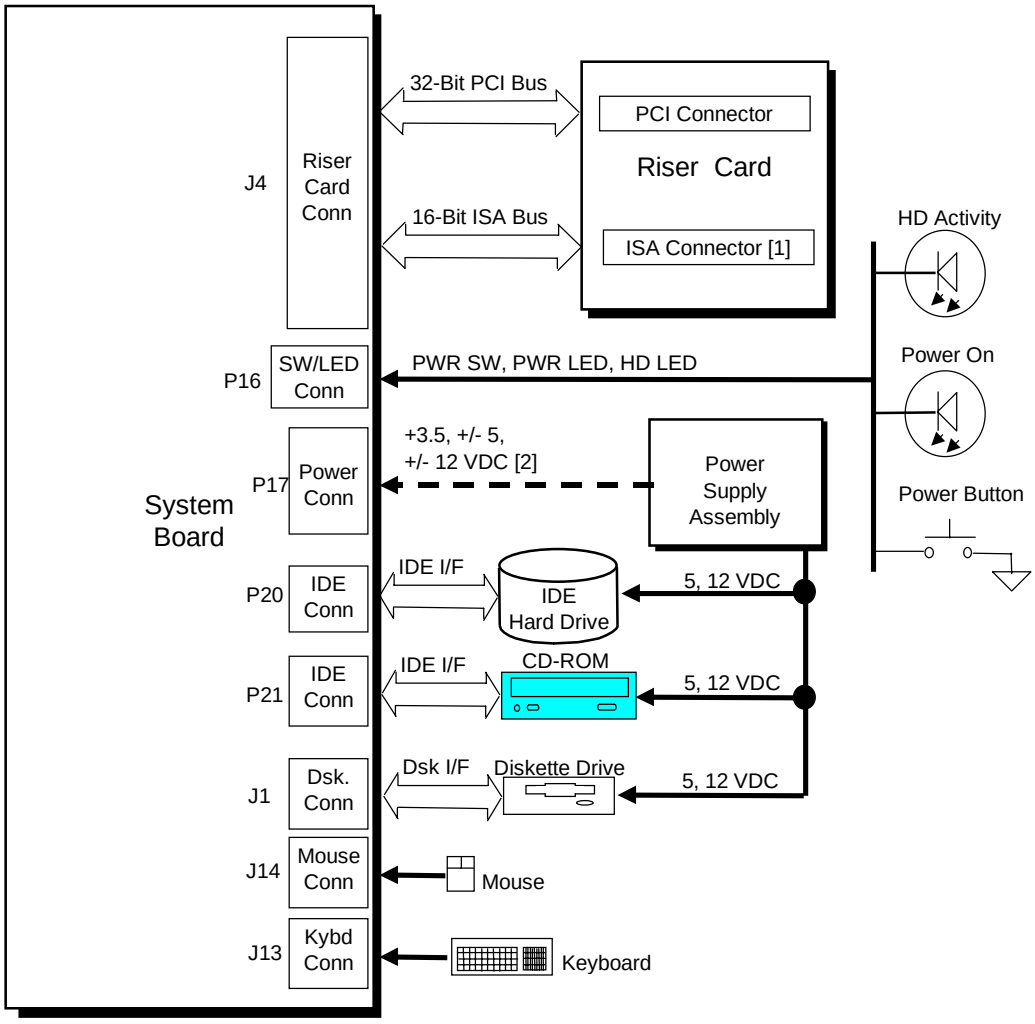


Figure 7–3. Low Voltage Supply, Block Diagram

7.4 SIGNAL DISTRIBUTION

Figure 7-4 shows general signal distribution between the main subassemblies of the system unit.



NOTES:

[1] Deskpro 4000S only

[2] No cable used for interface; direct connection between PS assembly and system board.

CD Models only. An audio card must be added by the user if audio is desired.

Figure 7–4. Signal Distribution Diagram

Chapter 8
BIOS ROM

8.1 INTRODUCTION

The Basic Input/Output System (BIOS) of the computer is a collection of machine language programs stored as firmware in read-only memory (ROM). The BIOS ROM includes such functions as Power-On Self Test (POST), PCI device initialization, Plug ‘n Play support, power management activities, and Setup. This chapter includes the following topics:

The firmware contained in the BIOS ROM supports the following operating systems:

- DOS 6.2
- Windows 3.1
- Windows for Workgroups 3.11
- Windows 95
- Windows NT 3.5
- OS/2 ver 2.1
- OS/2 Warp
- SCO Unix

The microprocessor accesses the BIOS ROM as a 128-KB block from E0000h to FFFFFh. The BIOS data is shadowed in a 64-KB block in the upper memory area. The BIOS segments are dynamically paged in and out of the 64-KB block as they are needed.

> **NOTE:** This chapter describes BIOS in general and focuses on aspects of BIOS unique to this particular system. For detailed information regarding the BIOS, refer to the *Compaq Basic Input/Output System Technical Reference Guide.*

8.2 BOOT FUNCTIONS

The system supports new system boot functions to support remote ROM flashing and PC97 requirements. This system also supports the EL Torito specification for bootable CDs.

> **NOTE:** This system will not boot CDs intended for use in Compaq ProLiant and ProSignia products.

8.2.1 BOOT BLOCK

This system includes 24 KB of boot block ROM that provides a way to recover from a failed remote flashing of the system BIOS ROM. Early during the boot process, the boot block code checks the system ROM. If validated, the system BIOS continues the boot sequence. If the system ROM fails the check, the boot block code provides the minimum amount of support necessary to allow booting the system from the diskette drive (bypassing the security measures) and re-flash the system ROM with a ROMPAQ diskette. Since video is not available during the initial boot sequence the boot block routine uses the keyboard LEDs to communicate status as follows:

Num Lock LED	Caps Lock LED	Scroll Lock LED	Meaning
Off	On	Off	Administrator password required.
On	Off	Off	Boot failed. Reset required for retry.
Off	Off	On	Flash failed (set by ROMPAQ).
On	On	On	Flash complete (set by ROMPAQ).

The boot block area of ROM is always write-protected.

8.2.2 QUICKBOOT

The QuickBoot mode (programmable through the INT 15, AX=E845h call) skips certain portions of the POST (such as the memory count) during the boot process **unless** the hood has been detected as being removed. The QuickBoot mode is programmable as to be invoked always, never (default) or every x-number of days.

8.2.3 SILENTBOOT

When in the SilentBoot mode, the boot process skips certain audio and visual aspects of POST (such as the speed beeps and screen messages). Error messages are still displayed. The QuickBoot mode is programmable (through the INT 15, AX=E845h call) as to either TERSE (default) or VERBOSE mode.

8.3 ACCESSING CONFIGURATION MEMORY

Configuration memory (CMOS and NVRAM) should be accessed using the appropriate BIOS function. The following subsections describe several BIOS functions available to applications for accessing the system's non-volatile memory.

8.3.1 ACCESSING CMOS

For accessing CMOS bytes, the calling application should use INT 15 AX=E823h, which is described as follows:

INPUT:

EAX	= E823h
BH	= 0, read
	= 1, write
BL	= Value to write (if a write is specified)
CX	= Byte number (zero-based)

OUTPUT:

(Successful)

CF	= 0
AH	= 00h
AL	= Byte Value (if a read was specified)

(Failure)

CF	= 1
AH	= 86h, Function not supported
	= FFh, Byte does not exist

8.3.2 SETTING DEFAULT PARAMETERS

The BIOS function INT 15, AX=E841h is used for setting various system parameters to the default settings on the next system boot. This function is intended for Plug 'n Play (PnP) support (refer to section 8.5 "Plug 'n Play" for more information. Two variances of the function are available and described as follows:

8.3.2.1 INT 15, AX=E841h, BL=00h - Set CMOS Defaults

This function sets a bit in NVRAM that instructs the BIOS to load NVRAM with default values during the next system boot. The user will not be prompted when the default values are set. Note that the ESCD area of NVRAM is not affected by this function. Any required changes to the ESCD area must be made by the calling application invoking PnP BIOS functions.

INPUT:
EAX = E841h
BH = 00h

OUTPUT:
(Successful)
CF = 0
AH = 00h
(Failure)
CF = 1
AH = 86h, Function not supported

8.3.2.2 INT 15, AX=E841h, BL=01h - Set System Board Device Defaults

This function performs a PnP Set System Device Node call for all system board “devnnodes.” On the next boot following execution of this function, each device is configured with the factory default settings. In addition to this call, an application may choose to also remove non-system board devices from ESCD area. The function is described as follows:

INPUT:
EAX = E841h
BH = 00h

OUTPUT:
(Successful)
CF = 0
AH = 00h
(Failure)
CF = 1
AH = 86h, Function not supported

8.3.3 ACCESSING CMOS FEATURE BITS

The BIOS function INT 15, AX=E845h is used for accessing areas in non-volatile memory used to store variables for various features. This is a Client Management function and is described in section 8.4.

8.4 CLIENT MANAGEMENT SUPPORT

Client Management deals with issues of security, identification, and system management functions. A group of BIOS INT 15 functions are provided to support Client Management. These functions are listed Table 8-2.

Table 8-2.
Client Management Functions (INT15)

AX	Function	Mode
E800h	Get system ID	Real, 16-, & 32-bit Prot.
E807h	Get System Information Table	Real, 16-, & 32-bit Prot.
E813h	Get monitor information	Real, 16-, & 32-bit Prot.
E814h	Get system revision	Real, 16-, & 32-bit Prot.
E816h	Get temperature status	Real, 16-, & 32-bit Prot.
E817h	Get drive attribute	Real
E818h	Get drive off-line test	Real
E819h	Get chassis serial number	Real, 16-, & 32-bit Prot.
E81Ah	Write chassis serial number	Real
E81Bh	Get drive threshold	Real
E81Ch	Write network error log	Real, 16-, & 32-bit Prot.
E81Dh	Read network error log	Real, 16-, & 32-bit Prot.
E81Eh	Get drive ID	Real
E822h	Flash ROM/Sys. Admin. Fnc.	Real, 16-, & 32-bit Prot.
E827h	DIMM EEPROM Access	Real, 16-, & 32-bit Prot.
E828h	Inhibit power button	Real, 16-, & 32-bit Prot.
E829h	Remote Security Functions	Real, 16-, & 32-bit Prot.
E845h	Access CMOS Feature Bits	Real, 16-, & 32-bit Prot.

All 32-bit protected mode calls are accessed by using the industry-standard BIOS32 Service Directory. Using the service directory involves three steps:

1. Locating the service directory.
2. Using the service directory to obtain the entry point for the client management functions.
3. Calling the client management service to perform the desired function.

The BIOS32 Service Directory is a 16-byte block that begins on a 16-byte boundary between the physical address range of 0E0000h-0FFFFFh. The format is as follows:

Offset	No. Bytes	Description
00h	4	Service identifier (four ASCII characters)
04h	4	Entry point for the BIOS32 Service Directory
08h	1	Revision level
09h	1	Length of data structure (no. of 16-byte units)
0Ah	1	Checksum (should add up to 00h)
0Bh	5	Reserved (all 0s)

To support Windows NT an additional table to the BIOS32 table has been defined to contain 32-bit pointers for the DDC and SIT locations. The Windows NT extension table is as follows:

```
; Extension to BIOS SERVICE directory table (next paragraph)

        db      "32OS"          ; sig
        db      2               ; number of entries in table
        db      "$DDC"          ; DDC POST buffer sig
        dd      ?               ; 32-bit pointer
        dw      ?               ; byte size
        db      "$SIT"          ; SIT sig
        dd      ?               ; 32-bit pointer
        dw      ?               ; byte size
        db      "$ERB"          ; ESCD sig
        dd      ?               ; 32-bit pointer
        dw      ?               ; bytes size
```

The service identifier for Client Management functions is "$CLM." Once the service identifier is found and the checksum verified, a FAR call is invoked using the value specified at offset 04h to retrieve the CM services entry point. The following entry conditions are used for calling the Client Management service directory:

```
INPUT:
        EAX             = Service Identifier [$CLM]
        EBX (31..8)     = Reserved
        EBX (7..0)      = Must be set to 00h
        CS              = Code selector set to encompass the physical page holding
                          entry point as well as the immediately following physical page.
                          It must have the same base. CS is execute/read.
        DS              = Data selector set to encompass the physical page holding
                          entry point as well as the immediately following physical page.
                          It must have the same base. DS is read only.
        SS              = Stack selector must provide at least 1K of stack space and be 32-bit.
        (I/O permissions must be provided so that the BIOS can support as necessary)

OUTPUT:
        AL              = Return code:
                          00h, requested service is present
                          80h, requested service is not present
                          81h, un-implemented function specified in BL
                          86h and CF=1, function not supported
        EBX             = Physical address to use as the selector BASE for the service
        ECX             = Value to use as the selector LIMIT for the service
        EDX             = Entry point for the service relative to the BASE returned in EBX
```

The following subsections describe aspects of Client Management **unique to this system**. For a general description of these BIOS functions refer to the *Compaq BIOS Technical Reference Guide*.

8.4.1 SYSTEM ID

The INT 15, AX=E800h BIOS function can be used by software to identify the system. The system ID will be returned in the BX register as follows:

Series	System ID
Deskpro 4000N	03D8h
Deskpro 4000S	038Ch

8.4.2 SYSTEM INFORMATION TABLE

The System Information Table (SIT) is a comprehensive list of fixed configuration information arranged into records. The INT 15 AX=E807h BIOS function accesses the SIT by returning a pointer in ES:BX to indicate the location of the SIT. This section lists the default values that should be read from the SIT. For specific bit descriptions and more detailed information on the SIT refer to the *Compaq Basic Input/Output System (BIOS) Technical Reference Guide*.

Power Conservation Record, SIT Record 01h

Byte	Function	Default Value
00h	Record ID	01h
01h	No. of Data Bytes in Record	0Bh
02h	Volume, CPU Speed, Screensave, PWR Consv. Mode	07h
03h	LED Blink, Popup, APM, PC Level, MAXBRIGHT Control	C4h
04h	SW Power Cntrl., Screensave/Hard Drive Timeouts, PWR	10h
05h	Magic Packet Flag, SMI, Modem Installed	[1]
06h-0Bh	Popup Location	[2]
0Ch	Qick Energy Save, Magic Packet PWR, Suspend, CPU Sp.	1Ch

NOTES:

[1] Will be determined at runtime

[2] Unsupported function - read all 0s.

Timeout Counter Record (System Standby), SIT Record 02h

Byte	Function	Default Value
00h	Record ID for System Standby Timeout	02h
01h	No. of Data Bytes in Record	08h
02h	First Value	0
03h		15
04h		20
05h		30
06h		40
07h		45
08h		60
09h	Last Value	75

Timeout Counter Record (Video Screensave), SIT Record 03h

Byte [1]	Function	Default Value
0Ah	Record ID for Video Screensave Timeout	03h
0Bh	No. of Data Bytes in Record	09h
0Ch	First Value	0
0Dh		5
0Eh		10
0Fh		15
10h		20
11h		30
12h		40
13h		50
14H	Last Value	60

NOTE:

[1] Offset from byte 00h of timeout record 02h.

Timeout Counter Record (Hard Drive), SIT Record 04h

Byte [1]	Function	Default Value
15h	Record ID for Hard Drive Timeout	04h
16h	No. of Data Bytes in Record	06h
17h	First Value	0
18h		10
19h		15
1Ah		20
1Bh		30
1Ch	Last Value	60

NOTE:

[1] Offset from byte 00h of timeout record 02h.

Security Record, SIT Record 05h

Byte	Function	Default Value
00h	Record ID	05h
01h	No. of Data Bytes in Record	04h
02h	NVRAM/HD Lock, QuickLock/QuickBlank, FD Boot, PWR Pwd	7Fh
03h	Virus Detect, Serial/Parallel Cntrl., FD Drive Cntl., Stby Cntrl.	1Eh
04h	Diskette Drive Fnct., Password Functions	7Ah
05h	Password Locking, Ownership Tag Length	[1]

NOTE:

[1] Determined by system at runtime.

Processor/Memory/Cache Record, SIT Record 06h

Byte	Function	Default Value
00h	Record ID	06h
01h	No. of Data Bytes in Record	0Eh
02h, 03h	Installed Microprocessor Speed	[1]
04h	Cache Configuration	07h
05h	L2 Cache Size	20h
06h	L2 Cache Speed	00h
07h	Total Memory Amount Adjustment	06h
08h, 09h	Total Soldered Memory	0000h
0Ah, 0Bh	Maximum Memory Installable	0100h
0Ch, 0Dh	Reserved	0000h
0Eh	Processor Designer	00h
0Fh	System Cache Error Correction	01h

NOTE: [1] Determined by system at runtime.

Peripheral and Input Device Record, SIT Record 07h

Byte	Function	Default Value
00h	Record ID	07h
01h	No. of Data Bytes in Record	34h
02h	DMA Functions, SCSI Support, Flashable ROM, Setup Partition, 101 Keyboard	07h
03h	Erase-Eaze Kybd. Support in ROM, El Torito CD Boot Support, QuickBoot, ROM Functions	53h
04h	Formfactor	04h, DT 05h, MT
05h	Softdrive 1 & 2 Data	FFh
06h	Softdrive 3 & 4 Data	FFh
07h-0Ah	Softdrive 1-4 Starting Address	all 0s
0Bh	Panel ID	00h
0Ch	Integrated Monitor, ROM Socket, No. of Prog. Serial Ports	12h
0Dh	Parallel Port Mode, Modem Type	00h
0Eh	Drive Fault Prediction Support for Drives 0-3	F1h
0Fh, 10h	PCI Bus Master CMOS Data	0000h
11h, 12h	VGA Palette Snoop Function	0000h
13h	Misc. PCI Information	01h
14h, 15h	I/O Address for I^2C Device	00h
16h	I^2C Information Byte	00h
17h	ATAPI Device Information (Logical Devices 1 & 2)	00h
18h	ATAPI Device Information (Logical Devices 3 & 4)	00h
19h	3-D Audio Support	00h
1Ah	BIOS Supported Features	00h
1Bh	Misc. Features (Power Inhibit Support)	01h
1Ch, 1Dh	Back-to-Back I/O Delay Index 0	0420h
1Eh, 1Fh	Back-to-Back I/O Delay Index 1	0300h
20h, 21h	Back-to-Back I/O Delay Index 2	0660h
22h, 23h	Back-to-Back I/O Delay Index 3	0780h
24h	Back-to-Back I/O Delay NVRAM Location	n/a
25h	Bit Mask for Byte 24h	n/a
26h	O/S Boot NVRAM Location	n/a
27h	Bit Mask for Byte 26h	n/a
28h-2Bh	IDE Drive 0-3 Max DMA/PIO Mode	n/a
2Ch-2Dh	Offset Address in EBDA for Bezel Button	n/a
2Eh	Processor Upgrade Mounting	01h
2Fh	Parallel Port Connector Type/Pinout	41h
30h	Serial Port Connector Type	01h
31h	Serial Port Maximum Speed	16h
32h	Serial Port Maximum Speed	E3h
33h	Serial Port Maximum Speed	60h
34h	DMA Burst Mode Support	0Bh
35h	Keyboard Connector Type	13h

Memory Module Information Record, SIT Record 08h

Byte	Function	Default Value
00h	Record ID	08h
01h	No. of Data Bytes in Record	0Dh
02h	No. of Sockets	03h
03h	Memory Socket Location 0	00h
04h	Memory Installed In Location 0	[1]
05h	Memory Speed In Location 0	[1]
06h	Memory Form Factor 0	03h
07h	Memory Socket Location 1	01h
08h	Memory Installed In Location 1	[1]
09h	Memory Speed In Location 1	[1]
0Ah	Memory Form Factor 1	03h
0Bh	Memory Socket Location 2	02h
0Ch	Memory Installed In Location 2	[1]
0Dh	Memory Speed In Location 2	[1]
0Eh	Memory Form Factor 2	03h

NOTE: [1] Determined at runtime.

Timeout Default Record, SIT Record 09h

Byte	Function	Default Value
00h	Record ID	09h
01h	No. of Data Bytes in Record	0Ah
02h	High Power - Standby	15 min
03h	High Power - Hard Drive/System Idle	15 min
04h	High Power - Screensave	15 min
05h	High Power - Maximum Brightness	100 min
06h	High Power - Processor Speed	100 min
07h	Medium Power - Standby	15 min
08h	Medium Power - Hard Drive/System Idle	15 min
09h	Medium Power - Screensave	15 min
0Ah	Medium Power - Maximum Brightness	100 min
0Bh	Medium Power - Processor Speed	100 min

CMOS/NVRAM Information Record, SIT Record 0Ah

Byte	Function	Default Value
00h	Record ID	0Ah
01h	No. of Data Bytes in Record	0Ah
02h	Size of EISA NVRAM or Extended CMOS (Low Byte)	00h
03h	Size of EISA NVRAM or Extended CMOS (High Byte)	00h
04h	Size of High CMOS (Low Byte)	00h
05h	Size of High CMOS (High Byte)	00h
06h	NVRAM Storage Device Access Type	00h

Automatic Server Recovery Record, SIT Record 0Bh (Not Used)

Memory Banks Information Record, SIT Record 0Ch (Not Used)

Multiprocessor Feature Information Record, SIT Record 0Dh (Not Used)

Extended Disk Support Record, SIT Record 0Eh

Byte	Function	Default Value
00h	Record ID	0Eh
01h	No. of Data Bytes in Record	02h
02h	Pointer To Extended Disk table (High Byte)	[1]
03h	Pointer To Extended Disk table (Low Byte)	[1]

NOTE: [1] Determined at runtime.

System Record, SIT Record 0Fh (Not Used)

Product Name Header Record, SIT Record 10h

Byte	Function	Default Value
00h	Record ID	10h
01h	No. of Data Bytes in Record	14h
02h-14	Product Name	“Compaq Deskpro 4000”
15h	Terminator Byte	00h

DC-DC Converter Record, SIT Record 11h (Not Used)

8.4.3 TEMPERATURE SENSOR

A temperature sensor component is mounted in the cavity of the microprocessor socket. This sensor component detects when the microprocessor has reached a programmed temperature level and initiates appropriate action. The sensor is programmed by BIOS for two temperature levels; a level for initiating a caution to the user and another level to initiate a system shutdown. Detection of a temperature level results in asserting an IRQ and/or the SMI- for initiating action.

The sensing feature is set up by BIOS during POST. A particular microprocessor step will have peculiar operating temperature optimums so that a processor upgrade may require that the BIOS be upgraded as well. The status of the temperature condition (caution, critical) may be retrieved using the INT 15, AX=E816h call.

8.4.4 DRIVE FAULT PREDICTION

The Compaq BIOS provides direct Drive Fault Prediction support for IDE-type hard drives. This feature is provided through two BIOS calls. Function INT 15, AX=E817h is used to retrieve a 512-byte block of drive attribute data while the INT 15, AX=E81Bh is used to retrieve the drive's warranty threshold data. If data is returned indicating possible failure then the following message is displayed:

"1720-Intellisafe Hard Drive detects imminent failure"

8.4.5 DIMM SUPPORT

The BIOS includes DIMM support consisting of the following:

- Access control with the serial (I^2C) EEPROM of the DIMM
- Runtime information on ECC-correctable single bit errors
- POST message if ECC-correctable errors are detectable during POST memory test

DIMMs with 128 bytes of EEPROM can be used although 256-byte EEPROM DIMMs are recommended for full support of Compaq intelligent manageability features. The following BIOS functions have been added to provide specific support of DIMMs:

INT 15h AX=E827h, BH=00h; Read DIMM EEPROM

ENTRY: AX = E827h
BH = 00h
BL = DIMM No. (0-3)
CX = Number of bytes to read
DX = Offset of first byte to read
DS: (E) SI = Address of data buffer to receive data

RETURN: CX = No. of bytes read
CF = 0 (Success)
AH = 0
1 (Failure)
AH = Error Code:
01h, No DIMM EEPROM or socket empty
02h, Boundary error (offset or no. of bytes to read exc. cap)
86h, Not supported

INT 15h AX=E827h, BH=01h; Write DIMM EEPROM

ENTRY: AX = E827h
BH = 01h
BL = DIMM No. (0-3)
CX = Number of bytes to be written
DX = Offset of first byte to be written
DS: (E) SI = Address of data buffer holding write data

RETURN: CX = No. of bytes written
CF = 0 (Success)
AH = 0
1 (Failure)
AH = Error Code:
01h, No DIMM EEPROM or socket empty
02h, Boundary error (offset or no. of bytes to read exc. cap)
86h, Not supported

INT 15h AX=E827h, BH=02h; Get ECC-Corrected Single Bit Error Status

ENTRY:	AX =	E827h
	BH =	02h
RETURN:	CF =	0 (Success) AH = 0
	BX =	0000h (if no single bit ECC corrected error has occurred) bit <0>, Error occurred on DIMM/SIMM pair 0 bit <1>, Error occurred on DIMM/SIMM pair 1 bit <2>, Error occurred on DIMM/SIMM pair 2 bit <3>, Error occurred on DIMM/SIMM pair 3
	CF =	1 (Failure) AH = 86h (Not supported)

The POST memory test checks for ECC-corrected single bit errors after each 64K of memory tested in a similar fashion as is done with parity. The errors are counted on a per DIMM basis and notify the user at the end of the test in the following format:

"207-ECC Corrected Single Bit Errors in DIMM/SIMM Pair(s) x,x…"

x = DIMM/SIMM pair numbers 0 through 3.

8.4.6 SECURITY FUNCTIONS

The INT 15 AX=E829h BIOS function is used to control various security features of the system. This function may be issued remotely (over a network) by a driver. A request buffer must be built (by the driver) for each security feature prior to making the call. This system supports the following security features:

- QuickLock
- QuickBlank
- Diskette drive boot disable
- Diskette drive write disable
- IDE controller disable
- Serial ports disable
- Parallel port disable
- Change administrator password
- Hood removal sensor
- Ownership tag
- Asset tag
- USB disable

The write-protect function that determines diskette write control is extended to cover all drives that use removable read/write media (i.e., if diskette write protect is invoked, then any diskette drive, power drive (SCSI and/or ATAPI), and floptical drive installed will be inaccessible for (protected from) writes). Client management software should check the following bytes of SIT record 07h for the location and access method for this bit:

System Information Table, Peripheral and Input Device Record (07h) (partial listing)

Byte	Bit	Function
1Fh	7-0	Removable Read/Write Media Write Protect Enable Byte Offset (0-255)
20h		Removable Read/Write Media Write Protect Enable Bit Location:
	7..4	CMOS Type: 0000 = CMOS 0001 = High CMOS 0010 = NVRAM 0011 = Flat model NVRAM
	3..0	Bit Location: 0000 = Bit 0 0100 = Bit 4 0001 = Bit 1 0101 = Bit 5 0010 = Bit 2 0110 = Bit 6 0011 = Bit 3 0111 = Bit 7

8.4.7 ACCESSING CMOS FEATURE BITS

The BIOS function INT 15, AX=E845h is a tri-modal call for accessing areas in non-volatile memory used to store variables for various features.

INPUT:

EAX = E845h
BL = 0, Read
= 1, Write
BH = Value Read/to Write
CX = Feature Bits Number (refer to description box below)
DS:SI = Pointer to buffer passing multiple byte features

OUTPUT:

(Successful)

CF = 0
EAX = Reserved
BH = Value read (if a read was specified)

(Failure)

CF = 1
AH = 86h, Function not supported

CX	Function	Default Value
0000h	PCI 2.1 Mode (Enabled)	1b
0001h	Erase Eaze Keyboard (off)	00b
0002h	Comm/IR Port Designation (Comm port)	0b
0003h	No Rejection of SETs By PnP (reject SETs)	0b
0004h	PCI VGA Snoop (snoop disabled)	0b
0005h	PCI Bus Mastering BIOS Support (disabled)	0b
0006h	Auto Prompt for Auto Setup (prompt for F1, F2, F10)	00b
0007h	Mode 2 Configuration Support (enabled)	1b
0008h	Secondary Hard Drive Controller Enabled (enabled)	1b
0009h	Secondary Hard Drive Controller IRQ (IRQ15)	11b
000Ah	Custom Drive Type #1	40 bits, all 0s
000Bh	Custom Drive Type #2	40 bits, all 0s
000Ch	Custom Drive Type #3	40 bits, all 0s
000Dh	Custom Drive Type #4	40 bits, all 0s
000Eh	POST Verbose/Terse or “Silent Boot” Mode (Terse)	1b
000Fh	Drive Translation Mode (translate)	0b
0010h	Mfg. Process Number Bytes	30 bits, [1]
0011h	Administrator Password	72 bits, [1]
0012h	Power-On Password	32 bits, [1]
0013h	Ownership Tag	640 bits, [1]
0014h	Warm Boot Password Mode (disabled)	0b
0015h	Hood Lock (enabled)	1b
0016h	Hood Removal (disabled)	00b
0017h	USB Security (disabled)	0b
0018h	Configurable Power Supply (legacy mode)	0b
0019h	QuickBoot Mode (full boot always)	00000b
001Ah	BBS IPL Order	76543210h

NOTE:

For full bit definitions refer to the *Compaq BIOS Technical Reference Guide.*
[1] Determined at runtime.

8.5 PNP SUPPORT

The BIOS includes Plug 'n Play (PnP) support for PnP version 1.0A.

> **NOTE**: For full PnP functionality to be realized, all peripherals used in the system must be designed as "PnP ready." Any installed ISA peripherals that are not "PnP ready" can still be used in the system, although configuration parameters may need to be considered (and require intervention) by the user.

Table 8-1 shows the PnP functions supported (for detailed PnP information refer to the Compaq BIOS Technical Reference Guide):

Table 8-1.
PnP BIOS Functions

Function	Register
00h	Get number of system device nodes
01h	Get system device node
02h	Set system device node
03h	Get event
04h	Send message

The BIOS call INT 15, AX=E841h, BH=01h (described earlier in section 8.3) can be used by an application to retrieve the default settings of PnP devices for the user. The application should use the following steps for the display function:

1. Call PnP function 01(get System Device Node) for each devnode with bit 1 of the control flag set (get static configuration) and save the results.
2. Call INT 15, AX=E841h, BH=01h.
3. Call PnP "Get Static Configuration" for each devnode and display the defaults.
4. If the user chooses to save the configuration, no further action is required. The system board devices will be configured at the next boot. If the user wants to abandon the changes, then the application must call PnP function 02 (Set System Device Node) for each devnode (with bit 1 of the control flag set for static configuration) with the results from the calls made prior to invoking this function.

8.6 POWER MANAGEMENT SUPPORT

The Compaq Deskpro 2000 system includes Advanced Power Management (APM) BIOS support that provides, if so configured, for the automatic shutdown of certain areas within a system after a specified time of inactivity has elapsed. When activity is detected, APM brings the system back up to full power to provide complete user support.

For maximum energy-conservation benefit, APM functionality should be implemented using the following three layers:

- BIOS layer (APM BIOS (ver. 1.2, 1.1, 1.0))
- Operating system (OS) layer (APM driver)
- Application layer (APM-aware application or device driver)

The BIOS layer informs the OS or driver when hardware events occur (or don't occur) so that a transition to another power state should take place. The process starts with the OS or driver making a connection with the BIOS through an APM BIOS call. In a DOS environment POWER.EXE makes a Real mode connection. In Windows 3.1 and in Windows 95, a 32-bit connection is made. Currently Windows NT does not make an APM connection.

With power management enabled, inactivity timers are monitored. When an inactivity timer times out, an SMI is sent to the microprocessor to invoke the SMI handler. The SMI handler works with the APM driver and APM BIOS to take appropriate action based on which inactivity timer timed out.

Two I/O ports are used for APM communication with the SMI handler:

Port Address	Name
0B2h	APM Control
0B3h	APM Status

Three power states are defined under power management:

On - The computer is running, all subsystems are on and drawing full power. Any activity in the following subsystems will reset the activity timer, which has a default setting of 15 minutes before Standby entered:

a. Keyboard
b. Mouse
c. Serial port
d. Diskette drive
e. Hard drive

Standby - The computer is in a low power state: video is off, some subsystems may be drawing less power, and the microprocessor is halted except for servicing interrupts. Video graphics controller is under driver control and/or VSYNC is off and the power supply fan is turned off. Any of the following activities will generate a wake-up SMI and return the system to On:

a. Keyboard
b. Mouse
c. Serial port
d. Diskette drive
e. Hard drive
f. RTC Alarm

If no APM connection is present, the BIOS will set an APM timer to 45 minutes, at which time the Suspend will be entered if no activity has occurred. This function can be defeated (so that Suspend will **not** be achieved). If an APM connection is present, the BIOS APM timer is not used and Suspend is entered only by user request either through an icon in Windows 95 or by pressing and releasing the power button under 4 seconds.

Suspend - The computer is in a low power state: video graphics controller is under driver control and/or HSYNC and VSYNC are off, some subsystems may be drawing less power, and the microprocessor is halted except for servicing interrupts. Any of the following activities will generate a wake-up SMI and return the system to On:

a. Keyboard
b. Mouse
c. Serial port
d. Diskette drive
e. Hard drive
f. RTC Alarm
g. Network interface controller

The APM BIOS for this system supports APM 1.2 as well as previous versions 1.1 and 1.0. The APM BIOS functions are listed in Table 8-3.

Table 8-3.
APM BIOS Functions (INT15)

AX	Function
5300h	APM Installation Check
5301h	APM Connect (Real Mode)
5302h	APM Connect (16-bit Protected Mode)
5303h	APM Connect (32-bit Protected Mode)
5304h	Interface Disconnect
5305h	CPU Idle
5306h	CPU Busy
5307h	Set Power State [1]
5308h	Enable/Disable Power Management
5309h	Restore Power On Defaults
530Ah	Get Power Status
530Bh	Get PM Event
530Ch	Get Power State
530Dh	Enable/Disable Device Power Management
530Eh	APM Driver Version
530Fh	Engage/Disengage Power Management
5380h	OEM (Compaq) Specific APM Function

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Appendix A
ERROR MESSAGES AND CODES

A.1 INTRODUCTION

This appendix lists the error codes and a brief description of the probable cause of the error. Note that not all errors listed in this appendix may be applicable to a particular system depending on the model and/or configuration.

A.2 POWER-ON MESSAGES

Table A-1.
Power-On Messages

Message	Beeps	Probable Cause
CMOS Time and Date Not Set	(None)	Invalid time or date
(none)	2 short	Power-On successful
Run Setup	(None)	Any failure

A.3 BEEP CODE MESSAGES

Table A-2.
Beep Code Messages

Beeps	Error	Probable Cause
1	Refresh Failure	Faulty memory refresh circuitry.
3	Base 64-KB Memory Failure	Memory failure in first 64-KB.
4	Timer Not Operational	Same as above or timer 1 not functioning.
5	Processor Error	CPU-generated error.
6	8042 Gate A20 Failure	Keyboard controller faulty, BIOS cannot switch to protected mode.
7	Processor Exception Interrupt Error	CPU-generated exception interrupt.
8	Display Memory R/W Error	Missing graphics/video adapter or faulty video memory (system still boots).
9	ROM Checksum Error	Checksum value does not match value in BIOS.
10	CMOS Shutdown Register R/W Error	CMOS RAM shutdown register failure.
11	Cache Error	Faulty cache.

A.4 POWER-ON SELF TEST (POST) MESSAGES

Table A-3.
Power-On Self Test (POST) Messages

Error Message	Probable Cause
Bad PnP Serial ID Checksum	Serial ID checksum of PnP card was invalid.
Address Lines Short!	Error in address decoding circuitry on system board.
Cache Memory Failure, Do Not Enable Cache!	Defective cache memory, CPU has failed.
CMOS Battery Failed	Low RTC/CMOS battery
CMOS Checksum Invalid	Previous and current checksum value mismatch.
CMOS System Options Not Set	Corrupt or non-existant CMOS values.
CMOS Display Type Mismatch	Graphics/video type in CMOS does not match type detected by BIOS.
CMOS Memory Size Mismatch	Memory amount detected does not match value stored in CMOS.
CMOS Time and Date Not Set	Time and date are invalid.
Diskette Boot Failure	Boot disk in drive A: is corrupt.
DMA Bus Timeout	Bus driven by device for more than 7.8 us
DMA Controller Error	Error in one or both DMA controllers.
Drive Not Ready Error	BIOS cannot access the diskette drive.
Diskette Drive Controller Failure	BIOS cannot communicate with diskette drive controller.
Diskette Drive Controller Resource Conflict	Diskette drive controller has requested a resource already in use.
Diskette Drive A: Failure	BIOS cannot access drive A:.
Diskette Drive B: Failure	BIOS cannot access drive B:
Gate A20 Failure	Gate A20 of keyboard controller not working.
Invalid Boot Diskette	BIOS can read but cannot boot system from drive A:.
Keyboard Controller Error	Keyboard controller failure.
Keyboard is Locked…Please Unlock It	Locked keyboard.
Keyboard Stuck Key Detected	Key pressed down.
Master DMA Controller Error	Error exists in master DMA controller.
Master Interrupt Controller Error	Master interrupt controller failure.
Memory Size Decreased	Amount of memory detected is less than stated value in CMOS.
NVRAM Checksum Error, NVRAM Cleared	ESCD data was re-initialized due to NVRAM checksum error.
NVRAM Cleared By Jumper	NVRAM has been cleared by removal of jumper.
NVRAM Data Invalid, NVRAM Cleared	Invalid entry in ESCD.
Off Board Parity Error Addr. (HEX) = X	Parity error occurred in expansion memory, x= address of error.
Parallel Port Resource Conflict	Parallel port has requested a resource already in use.
PCI Error Log is Full	PCI conflict error limit (15) has been reached.
PCI I/O Port Conflict	Two devices requested the same resource.
PCI Memory Conflict	Two devices requested the same resource.
Primary Boot Device Not Found	Designated primary boot device could not be found.
Primary IDE Cntrl. Resource Conflict	Primary IDE controller requested a resource already in use.
Primary Input Device Not Found	Designated primary input device could not be found.
Secondary IDE Controller Resource	Secondary IDE controller has requested a resource already in use.
Serial Port 1 Resource Conflict	Serial port 1 requested a resource already in use.
Serial Port 2 Resource Conflict	Serial port 2 requested a resource already in use.
Slave DMA Controller Error	Error exists in slave DMA controller.
Slave Interrupt Controller Error	Slave interrupt controller failure.
Static Device Resource Conflict	A non-PnP ISA card has requested a resource already in use.
System Board Device Resource Conflict	A non-PnP ISA card has requested a resource already in use.
System Memory Size Mismatch	Amount of memory detected on system board is different from amount indicated in CMOS.

NOTE:
PCI and PnP messages are displayed with bus, device, and function information.

A.5 PROCESSOR ERROR MESSAGES (1xx-xx)

Table A-4.
Processor Error Messages

Message	Probable Cause	Message	Probable Cause
101-01	CPU test failed	105-08	Port 61 bit <1> not at one
101-02	32-bit CPU test failed	105-09	Port 61 bit <0> not at one
101-91..94	Multiplication test failed	105-10	Port 61 I/O test failed
102-01	FPU initial sts. word incorrect	105-11	Port 61 bit <7> not at zero
102-02	FPU initial cntrl. Word incorrect	105-12	Port 61 bit <2> not at zero
102-03	FPU tag word not all ones	105-13	No interrupt generated by failsafe timer
102-04	FPU tag word not all zeros	105-14	NMI not triggered by failsafe timer
102-05	FPU exchange command failed	106-01	Keyboard controller test failed
102-06	FPU masked exception error	107-01	CMOS RAM test failed
102-07	FPU unmasked exception error	108-02	CMOS interrupt test failed
102-08	FPU wrong mask status bit set	108-03	CMOS not properly initialized (interrupt test)
102-09	FPU unable to store real number	109-01	CMOS clock load data test failed
102-10	FPU real number calc test failed	109-02	CMOS clock rollover test failed
102-11	FPU speed test failed	109-03	CMOS not properly initialized (clock test)
102-12	FPU pattern test failed	110-01	Programmable timer load data test failed
102-15	FPU is inoperative or not present	110-02	Programmable timer dynamic test failed
102-16	Weitek not responding	110-03	Program timer 2 load data test failed
102-17	Weitek failed register trnsfr. Test	111-01	Refresh detect test failed
102-18	Weitek failed arithemetic ops test	112-01	Speed test Slow mode out of range
102-19	Weitek failed data conv. Test	112-02	Speed test Mixed mode out of range
102-20	Weitek failed interrupt test	112-03	Speed test Fast mode out of range
102-21	Weitek failed speed test	112-04	Speed test unable to enter Slow mode
103-01	DMA page registers test failed	112-05	Speed test unable to enter Mixed mode
103-02	DMA byte controller test failed	112-06	Speed test unable to enter Fast mode
103-03	DMA word controller test failed	112-07	Speed test system error
104-01	Master int. cntlr. test fialed	112-08	Unable to enter Auto mode in speed test
104-02	Slave int. cntlr. test failed	112-09	Unable to enter High mode in speed test
104-03	Int. cntlr. SW RTC inoperative	112-10	Speed test High mode out of range
105-01	Port 61 bit <6> not at zero	112-11	Speed test Auto mode out of range
105-02	Port 61 bit <5> not at zero	112-12	Speed test variable speed mode inoperative
105-03	Port 61 bit <3> not at zero	113-01	Protected mode test failed
105-04	Port 61 bit <1> not at zero	114-01	Speaker test failed
105-05	Port 61 bit <0> not at zero	116-xx	Way 0 read/write test failed
105-06	Port 61 bit <5> not at one	199-00	Installed devices test failed
105-07	Port 61 bit <3> not at one	--	--

A.6 MEMORY ERROR MESSAGES (2xx-xx)

Table A-5.
Memory Error Messages

Message	Probable Cause
200-04	Real memory size changed
200-05	Extended memory size changed
200-06	Invalid memory configuration
200-07	Extended memory size changed
200-08	CLIM memory size changed
201-01	Memory machine ID test failed
202-01	Memory system ROM checksum failed
202-02	Failed RAM/ROM map test
202-03	Failed RAM/ROM protect test
203-01	Memory read/write test failed
203-02	Error while saving block in read/write test
203-03	Error while restoring block in read/write test
204-01	Memory address test failed
204-02	Error while saving block in address test
204-03	Error while restoring block in address test
204-04	A20 address test failed
204-05	Page hit address test failed
205-01	Walking I/O test failed
205-02	Error while saving block in walking I/O test
205-03	Error while restoring block in walking I/O test
206-xx	Increment pattern test failed
210-01	Memory increment pattern test
210-02	Error while saving memory during increment pattern test
210-03	Error while restoring memory during increment pattern test
211-01	Memory random pattern test
211-02	Error while saving memory during random memory pattern test
211-03	Error while restoring memory during random memory pattern test
213-xx	Incompatible DIMM in slot x
214-xx	Noise test failed
215-xx	Random address test

A.7 KEYBOARD ERROR MESSAGES (30x-xx)

Table A-6.
Keyboard Error Messages

Message	Probable Cause	Message	Probable Cause
300-xx	Failed ID test	303-05	LED test, LED command test failed
301-01	Kybd short test, 8042 self-test failed	303-06	LED test, LED command test failed
301-02	Kybd short test, interface test failed	303-07	LED test, LED command test failed
301-03	Kybd short test, echo test failed	303-08	LED test, command byte restore test failed
301-04	Kybd short test, kybd reset failed	303-09	LED test, LEDs failed to light
301-05	Kybd short test, kybd reset failed	304-01	Keyboard repeat key test failed
302-xx	Failed individual key test	304-02	Unable to enter mode 3
302-01	Kybd long test failed	304-03	Incorrect scan code from keyboard
303-01	LED test, 8042 self-test failed	304-04	No Make code observed
303-02	LED test, reset test failed	304-05	Cannot /disable repeat key feature
303-03	LED test, reset failed	304-06	Unable to return to Normal mode
303-04	LED test, LED command test failed	--	--

A.8 PRINTER ERROR MESSAGES (4xx-xx)

Table A-7.
Printer Error Messages

Message	Probable Cause	Message	Probable Cause
401-01	Printer failed or not connected	402-10	Interrupt test and control reg. failed
402-01	Printer data register failed	402-11	Interrupt test, data/cntrl. reg. failed
402-02	Printer control register failed	402-12	Interrupt test and loopback test failed
402-03	Data and control registers failed	402-13	Int. test, LpBk. test., and data register failed
402-04	Loopback test failed	402-14	Int. test, LpBk. test., and cntrl. register failed
402-05	Loopback test and data reg. failed	402-15	Int. test, LpBk. test., and data/cntrl. reg. failed
402-06	Loopback test and cntrl. reg. failed	402-16	Unexpected interrupt received
402-07	Loopback tst, data/cntrl. reg. failed	402-01	Printer pattern test failed
402-08	Interrupt test failed	498-00	Printer failed or not connected
402-09	Interrupt test and data reg. failed	--	--

A.9 VIDEO (GRAPHICS) ERROR MESSAGES (5xx-xx)

Table A-8.
Video (Graphics) Error Messages

Message	Probable Cause	Message	Probable Cause
501-01	Video controller test failed	508-01	320x200 mode, color set 0 test failed
502-01	Video memory test failed	509-01	320x200 mode, color set 1 test failed
503-01	Video attribute test failed	510-01	640x200 mode test failed
504-01	Video character set test failed	511-01	Screen memory page test failed
505-01	80x25 mode, 9x14 cell test failed	512-01	Gray scale test failed
506-01	80x25 mode, 8x8 cell test failed	514-01	White screen test failed
507-01	40x25 mode test failed	516-01	Noise pattern test failed

A.10 DISKETTE DRIVE ERROR MESSAGES (6xx-xx)

Table A-9.
Diskette Drive Error Messages

Message	Probable Cause	Message	Probable Cause
6xx-01	Exceeded maximum soft error limit	6xx-20	Failed to get drive type
6xx-02	Exceeded maximum hard error limit	6xx-21	Failed to get change line status
6xx-03	Previously exceeded max soft limit	6xx-22	Failed to clear change line status
6xx-04	Previously exceeded max hard limit	6xx-23	Failed to set drive type in ID media
6xx-05	Failed to reset controller	6xx-24	Failed to read diskette media
6xx-06	Fatal error while reading	6xx-25	Failed to verify diskette media
6xx-07	Fatal error while writing	6xx-26	Failed to read media in speed test
6xx-08	Failed compare of R/W buffers	6xx-27	Failed speed limits
6xx-09	Failed to format a tract	6xx-28	Failed write-protect test
6xx-10	Failed sector wrap test	--	--

600-xx = Diskette drive ID test
601-xx = Diskette drive format
602-xx = Diskette read test
603-xx = Diskette drive R/W compare test
604-xx = Diskette drive random seek test
605-xx = Diskette drive ID media
606-xx = Diskette drive speed test
607-xx = Diskette drive wrap test
608-xx = Diskette drive write-protect test
609-xx = Diskette drive reset controller test
610-xx = Diskette drive change line test
694-00 = Pin 34 not cut on 360-KB drive
697-00 = Diskette type error
698-00 = Drive speed not within limits
699-00 = Drive/media ID error (run Setup)

A.11 SERIAL INTERFACE ERROR MESSAGES (11xx-xx)

Table A-10.
Serial Interface Error Messages

Message	Probable Cause	Message	Probable Cause
1101-01	Port test, UART DLAB bit failure	1101-12	Port test, DRVR/RCVR cntrl. signal failure
1101-02	Port test, line input or UART fault	1101-13	Port test, UART cntrl. signal interrupt failure
1101-03	Port test, address line fault	1101-14	Port test, DRVR/RCVR data failure
1101-04	Port test, data line fault	1109-01	Clock register initialization failure
1101-05	Port test, UART cntrl. signal failure	1109-02	Clock register rollover failure
1101-06	Port test, UART THRE bit failure	1109-03	Clock reset failure
1101-07	Port test, UART Dta RDY bit failure	1109-04	Input line or clock failure
1101-08	Port test, UART TX/RX buffer failure	1109-05	Address line fault
1101-09	Port test, interrupt circuit failure	1109-06	Data line fault
1101-10	Port test, COM1 set to invalid INT	1150-xx	Comm port setup error (run Setup)
1101-11	Port test, COM2 set to invalid INT	--	--

A.12 MODEM COMMUNICATIONS ERROR MESSAGES (12xx-xx)

Table A-11.
Serial Interface Error Messages

Message	Probable Cause	Message	Probable Cause
1201-XX	Modem internal loopback test	1204-03	Data block retry limit reached [4]
1201-01	UART DLAB bit failure	1204-04	RX exceeded carrier lost limit
1201-02	Line input or UART failure	1204-05	TX exceeded carrier lost limit
1201-03	Address line failure	1204-06	Time-out waiting for dial tone
1201-04	Data line fault	1204-07	Dial number string too long
1201-05	UART control signal failure	1204-08	Modem time-out waiting for remote response
1201-06	UART THRE bit failure	1204-09	Modem exceeded maximum redial limit
1201-07	UART DATA READY bit failure	1204-10	Line quality prevented remote response
1201-08	UART TX/RX buffer failure	1204-11	Modem time-out waiting for remote connection
1201-09	Interrupt circuit failure	1205-XX	Modem auto answer test
1201-10	COM1 set to invalid inturrupt	1205-01	Time-out waiting for SYNC [5]
1201-11	COM2 set to invalid	1205-02	Time-out waiting for response [5]
1201-12	DRVR/RCVR control signal failure	1205-03	Data block retry limit reached [5]
1201-13	UART control signal interrupt failure	1205-04	RX exceeded carrier lost limit
1201-14	DRVR/RCVR data failure	1205-05	TX exceeded carrier lost limit
1201-15	Modem detection failure	1205-06	Time-out waiting for dial tone
1201-16	Modem ROM, checksum failure	1205-07	Dial number string too long
1201-17	Tone detect failure	1205-08	Modem time-out waiting for remote response
1202-XX	Modem internal test	1205-09	Modem exceeded maximum redial limit
1202-01	Time-out waiting for SYNC [1]	1205-10	Line quality prevented remote response
1202-02	Time-out waiting for response [1]	1205-11	Modem time-out waiting for remote connection
1202-03	Data block retry limit reached [1]	1206-XX	Dial multi-frequency tone test
1202-11	Time-out waiting for SYNC [2]	1206-17	Tone detection failure
1202-12	Time-out waiting for response [2]	1210-XX	Modem direct connect test
1202-13	Data block retry limit reached [2]	1210-01	Time-out waiting for SYNC [6]
1202-21	Time-out waiting for SYNC [3]	1210-02	Time-out waiting for response [6]
1202-22	Time-out waiting for response [3]	1210-03	Data block retry limit reached [6]
1202-23	Data block retry limit reached [3]	1210-04	RX exceeded carrier lost limit
1203-XX	Modem external termination test	1210-05	TX exceeded carrier lost limit
1203-01	Modem external TIP/RING failure	1210-06	Time-out waiting for dial tone
1203-02	Modem external data TIP/RING fail	1210-07	Dial number string too long
1203-03	Modem line termination failure	1210-08	Modem time-out waiting for remote response
1204-XX	Modem auto originate test	1210-09	Modem exceeded maximum redial limit
1204-01	Time-out waiting for SYNC [4]	1210-10	Line quality prevented remote response
1204-02	Time-out waiting for response [4]	1210-11	Modem time-out waiting for remote connection

NOTES:

[1] Local loopback mode
[2] Analog loopback originate mode
[3] Analog loopback answer mode
[4] Modem auto originate test
[5] Modem auto answer test
[6] Modem direct connect test

A.13 HARD DRIVE ERROR MESSAGES (17xx-xx)

Table A-12.
Hard Drive Error Messages

Message	Probable Cause	Message	Probable Cause
17xx-01	Exceeded max. soft error limit	17xx-51	Failed I/O read test
17xx-02	Exceeded max. Hard error limit	17xx-52	Failed file I/O compare test
17xx-03	Previously exceeded max. soft error limit	17xx-53	Failed drive/head register test
17xx-04	Previously exceeded max.hard error limit	17xx-54	Failed digital input register test
17xx-05	Failed to reset controller	17xx-55	Cylinder 1 error
17xx-06	Fatal error while reading	17xx-56	Failed controller RAM diagnostics
17xx-07	Fatal error while writing	17xx-57	Failed controller-to-drive diagnostics
17xx-08	Failed compare of R/W buffers	17xx-58	Failed to write sector buffer
17xx-09	Failed to format a track	17xx-59	Failed to read sector buffer
17xx-10	Failed diskette sector wrap during read	17xx-60	Failed uncorrectable ECC error
17xx-19	Cntlr. failed to deallocate bad sectors	17xx-62	Failed correctable ECC error
17xx-40	Cylinder 0 error	17xx-63	Failed soft error rate
17xx-41	Drive not ready	17xx-65	Exceeded max. bad sectors per track
17xx-42	Failed to recalibrate drive	17xx-66	Failed to initialize drive parameter
17xx-43	Failed to format a bad track	17xx-67	Failed to write long
17xx-44	Failed controller diagnostics	17xx-68	Failed to read long
17xx-45	Failed to get drive parameters from ROM	17xx-69	Failed to read drive size
17xx-46	Invalid drive parameters from ROM	17xx-70	Failed translate mode
17xx-47	Failed to park heads	17xx-71	Failed non-translate mode
17xx-48	Failed to move hard drive table to RAM	17xx-72	Bad track limit exceeded
17xx-49	Failed to read media in file write test	17xx-73	Previously exceeded bad track limit
17xx-50	Failed I/O write test	--	--

1700-xx = Hard drive ID test
1701-xx = Hard drive format test
1702-xx = Hard drive read test
1703-xx = Hard drive read/write compare test
1704-xx = Hard drive random seek test
1705-xx = Hard drive controller test
1706-xx = Hard drive ready test
1707-xx = Hard drive recalibrate test
1708-xx = Hard drive format bad track test
1709-xx = Hard drive reset controller test
1710-xx = Hard drive park head test
1714-xx = Hard drive file write test
1715-xx = Hard drive head select test
1716-xx = Hard drive conditional format test
1717-xx = Hard drive ECC test
1719-xx = Hard drive power mode test
1721-xx = SCSI hard drive imminent failure
1724-xx = Net work preparation test
1736-xx = Drive monitoring test
1799-xx = Invalid hard drive type

A.14 HARD DRIVE ERROR MESSAGES (19xx-xx)

Table A-13.
Hard Drive Error Messages

Message	Probable Cause	Message	Probable Cause
19xx-01	Drive not installed	19xx-21	Got servo pulses second time but not first
19xx-02	Cartridge not installed	19xx-22	Never got to EOT after servo check
19xx-03	Tape motion error	19xx-23	Change line unset
19xx-04	Drive busy erro	19xx-24	Write-protect error
19xx-05	Track seek error	19xx-25	Unable to erase cartridge
19xx-06	Tape write-protect error	19xx-26	Cannot identify drive
19xx-07	Tape already Servo Written	19xx-27	Drive not compatible with controller
19xx-08	Unable to Servo Write	19xx-28	Format gap error
19xx-09	Unable to format	19xx-30	Exception bit not set
19xx-10	Format mode error	19xx-31	Unexpected drive status
19xx-11	Drive recalibration error	19xx-32	Device fault
19xx-12	Tape not Servo Written	19xx-33	Illegal command
19xx-13	Tape not formatted	19xx-34	No data detected
19xx-14	Drive time-out error	19xx-35	Power-on reset occurred
19xx-15	Sensor error flag	19xx-36	Failed to set FLEX format mode
19xx-16	Block locate (block ID) error	19xx-37	Failed to reset FLEX format mode
19xx-17	Soft error limit exceeded	19xx-38	Data mismatch on directory track
19xx-18	Hard error limit exceeded	19xx-39	Data mismatch on track 0
19xx-19	Write (probably ID) error	19xx-40	Failed self-test
19xx-20	NEC fatal error	19xx-91	Power lost during test

1900-xx = Tape ID test failed
1901-xx = Tape servo write failed
1902-xx = Tape format failed
1903-xx = Tape drive sensor test failed
1904-xx = Tape BOT/EOT test failed
1905-xx = Tape read test failed
1906-xx = Tape R/W compare test failed
1907-xx = Tape write-protect failed

A.15 VIDEO (GRAPHICS) ERROR MESSAGES (24xx-xx)

Table A-14.
Hard Drive Error Messages

Message	Probable Cause	Message	Probable Cause
2402-01	Video memory test failed	2418-02	EGA shadow RAM test failed
2403-01	Video attribute test failed	2419-01	EGA ROM checksum test failed
2404-01	Video character set test failed	2420-01	EGA attribute test failed
2405-01	80x25 mode, 9x14 cell test failed	2421-01	640x200 mode test failed
2406-01	80x25 mode, 8x8 cell test failed	2422-01	640x350 16-color set test failed
2407-01	40x25 mode test failed	2423-01	640x350 64-color set test failed
2408-01	320x200 mode color set 0 test failed	2424-01	EGA Mono. text mode test failed
2409-01	320x200 mode color set 1 test failed	2425-01	EGA Mono. graphics mode test failed
2410-01	640x200 mode test failed	2431-01	640x480 graphics mode test failed
2411-01	Screen memory page test failed	2432-01	320x200 256-color set test failed
2412-01	Gray scale test failed	2448-01	Advanced VGA controller test failed
2414-01	White screen test failed	2451-01	132-column AVGA test failed
2416-01	Noise pattern test failed	2456-01	AVGA 256-color test failed
2417-01	Lightpen text test failed, no response	2458-xx	AVGA BitBLT test failed
2417-02	Lightpen text test failed, invalid response	2468-xx	AVGA DAC test failed
2417-03	Lightpen graphics test failed, no resp.	2477-xx	AVGA data path test failed
2417-04	Lightpen graphics test failed, invalid resp.	2478-xx	AVGA BitBLT test failed
2418-01	EGA memory test failed	2480-xx	AVGA linedraw test failed

A.16 AUDIO ERROR MESSAGES (3206-xx)

Table A-15.
Audio Error Message

Message	Probable Cause
3206-xx	Audio subsystem internal error

A.17 NETWORK INTERFACE ERROR MESSAGES (60xx-xx)

Table A-16.
Network Interface Error Messages

Message	Probable Cause	Message	Probable Cause
6000-xx	Pointing device interface error	6054-xx	Token ring configuration test failed
6014-xx	Ethernet configuration test failed	6056-xx	Token ring reset test failed
6016-xx	Ethernet reset test failed	6068-xx	Token ring int. loopback test failed
6028-xx	Ethernet int. loopback test failed	6069-xx	Token ring ext. loopback test failed
6029-xx	Ethernet ext. loopback test failed	6089-xx	Token ring open

A.18 SCSI INTERFACE ERROR MESSAGES (65xx-xx, 66xx-xx, 67xx-xx)

Table A-17.
SCSI Interface Error Messages

Message	Probable Cause	Message	Probable Cause
6nyy-02	Drive not installed	6nyy-33	Illegal controller command
6nyy-03	Media not installed	6nyy-34	Invalid SCSI bus phase
6nyy-05	Seek failure	6nyy-35	Invalid SCSI bus phase
6nyy-06	Drive timed out	6nyy-36	Invalid SCSI bus phase
6nyy-07	Drive busy	6nyy-39	Error status from drive
6nyy-08	Drive already reserved	6nyy-40	Drive timed out
6nyy-09	Reserved	6nyy-41	SSI bus stayed busy
6nyy-10	Reserved	6nyy-42	ACK/REQ lines bad
6nyy-11	Media soft error	6nyy-43	ACK did not deassert
6nyy-12	Drive not ready	6nyy-44	Parity error
6nyy-13	Media error	6nyy-50	Data pins bad
6nyy-14	Drive hardware error	6nyy-51	Data line 7 bad
6nyy-15	Illegal drive command	6nyy-52	MSG, C/D, or I/O lines bad
6nyy-16	Media was changed	6nyy-53	BSY never went busy
6nyy-17	Tape write-protected	6nyy-54	BSY stayed busy
6nyy-18	No data detected	6nyy-60	Controller CONFIG-1 register fault
6nyy-21	Drive command aborted	6nyy-61	Controller CONFIG-2 register fault
6nyy-24	Media hard error	6nyy-65	Media not unloaded
6nyy-25	Reserved	6nyy-90	Fan failure
6nyy-30	Controller timed out	6nyy-91	Over temperature condition
6nyy-31	Unrecoverable error	6nyy-92	Side panel not installed
6nyy-32	Controller/drive not connected	6nyy-99	Autoloader reported tape not loaded properly

n = 5, Hard drive
= 6, CD-ROM drive
= 7, Tape drive.

yy = 00, ID
= 03, Power check
= 05, Read
= 06, SA/Media
= 08, Controller;
= 23, Random read
= 28, Media load/unload

A.19 POINTING DEVICE INTERFACE ERROR MESSAGES (8601-xx)

Table A-18.
Pointing Device Interface Error Messages

Message	Probable Cause	Message	Probable Cause
8601-01	Mouse ID fails	8601-06	Left block not selected
8601-02	Left mouse button is inoperative	8601-07	Right block not selected
8601-03	Left mouse button is stuck closed	8601-08	Timeout occurred
8601-04	Right mouse button is inoperative	8601-09	Mouse loopback test failed
8601-05	Right mouse button is stuck closed	8601-10	Pointing device is inoperative

A.20 CEMM PRIVILEDGED OPS ERROR MESSAGES

Table A-19.
CEMM Privileged Ops Error Messages

Message	Probable Cause	Message	Probable Cause
00	LGDT instruction	04	LL3 instruction
01	LIDT instruction	05	MOV CRx instruction
02	LMSW instruction	06	MOV DRx instruction
03	LL2 instruction	07	MOV TRx instruction

A.21 CEMM EXCEPTION ERROR MESSAGES

Table A-20.
CEMM Exception Error Messages

Message	Probable Cause	Message	Probable Cause
00	Divide	10	Invalid TSS
01	Debug	11	Segment not present
02	NMI or parity	12	Stack full
03	INT 0 (arithmetic overflow)	13	General protection fault
04	INT 3	14	Page fault
05	Array bounds check	16	Coprocessor
06	Invalid opcode	32	Attempt to write to protected area
07	Coprocessor device not available	33	Reserved
08	Double fault	34	Invalid software interrupt
09	Coprocessor segment overrun	--	--

Appendix B
ASCII CHARACTER SET

B.1 INTRODUCTION

This appendix lists, in Table B-1, the 256-character ASCII code set including the decimal and hexadecimal values. All ASCII symbols may be called while in DOS or using standard text-mode editors by using the combination keystroke of holding the **Alt** key and using the Numeric Keypad to enter the decimal value of the symbol. The extended ASCII characters (decimals 128-255) can only be called using the **Alt** + Numeric Keypad keys.

NOTE: Regarding keystrokes, refer to notes at the end of the table. Applications may interpret multiple keystroke accesses differently or ignore them completely.

Table B-1.
ASCII Character Set

Dec	Hex	Symbol	Dec	Hex	Symbol	Dec	Hex	Symbol	Dec	Hex	Symbol
0	00	Blank	32	20	Space	64	40	@	96	60	‘
1	01	☺	33	21	!	65	41	A	97	61	a
2	02	☻	34	22	“	66	42	B	98	62	b
3	03	♥	35	23	#	67	43	C	99	63	c
4	04	♦	36	24	$	68	44	D	100	64	d
5	05	♣	37	25	%	69	45	E	101	65	e
6	06	♠	38	26	&	70	46	F	102	66	f
7	07	•	39	27	‘	71	47	G	103	67	g
8	08	◘	40	28	(	72	48	H	104	68	h
9	09	○	41	29	)	73	49	I	105	69	I
10	0A	◙	42	2A	*	74	4A	J	106	6A	j
11	0B	♂	43	2B	+	75	4B	K	107	6B	k
12	0C	♀	44	2C	`	76	4C	L	108	6C	l
13	0D	♪	45	2D	-	77	4D	M	109	6D	m
14	0E	♫	46	2E	.	78	4E	N	110	6E	n
15	0F	☼	47	2F	/	79	4F	O	111	6F	o
16	10	►	48	30	0	80	50	P	112	70	p
17	11	◄	49	31	1	81	51	Q	113	71	q
18	12	↕	50	32	2	82	52	R	114	72	r
19	13	‼	51	33	3	83	53	S	115	73	s
20	14	¶	52	34	4	84	54	T	116	74	t
21	15	§	53	35	5	85	55	U	117	75	u
22	16	▬	54	36	6	86	56	V	118	76	v
23	17	↨	55	37	7	87	57	W	119	77	w
24	18	↑	56	38	8	88	58	X	120	78	x
25	19	↓	57	39	9	89	59	Y	121	79	y
26	1A	→	58	3A	:	90	5A	Z	122	7A	z
27	1B	←	59	3B	;	91	5B	[	123	7B	{
28	1C	∟	60	3C	<	92	5C	\	124	7C	|
29	1D	↔	61	3D	=	93	5D	]	125	7D	}
30	1E	▲	62	3E	>	94	5E	^	126	7E	~
31	1F	▼	63	3F	?	95	5F	_	127	7F	△ [1]

Continued

Table B-1. ASCII Code Set *(Continued)*

Dec	Hex	Symbol	Dec	Hex	Symbol	Dec	Hex	Symbol	Dec	Hex	Symbol
128	80	Ç	160	A0	á	192	C0	•	224	E0	•
129	81	ü	161	A1	í	193	C1	•	225	E1	ß
130	82	é	162	A2	ó	194	C2	•	226	E2	•
131	83	â	163	A3	ú	195	C3	•	227	E3	•
132	84	ä	164	A4	ñ	196	C4	•	228	E4	•
133	85	à	165	A5	Ñ	197	C5	•	229	E5	•
134	86	å	166	A6	ª	198	C6	•	230	E6	µ
135	87	ç	167	A7	º	199	C7	•	231	E7	•
136	88	ê	168	A8	¿	200	C8	•	232	E8	•
137	89	ë	169	A9	•	201	C9	•	233	E9	•
138	8A	è	170	AA	¬	202	CA	•	234	EA	•
139	8B	ï	171	AB	½	203	CB	•	235	EB	•
140	8C	î	172	AC	¼	204	CC	•	236	EC	•
141	8D	ì	173	AD	¡	205	CD	•	237	ED	•
142	8E	Ä	174	AE	«	206	CE	•	238	EE	•
143	8F	Å	175	AF	»	207	CF	•	239	EF	•
144	90	É	176	B0	•	208	D0	•	240	F0	•
145	91	æ	177	B1	•	209	D1	•	241	F1	±
146	92	Æ	178	B2	•	210	D2	•	242	F2	•
147	93	ô	179	B3	•	211	D3	•	243	F3	•
148	94	ö	180	B4	•	212	D4	•	244	F4	•
149	95	ò	181	B5	•	213	D5	•	245	F5	•
150	96	û	182	B6	•	214	D6	•	246	F6	÷
151	97	ù	183	B7	•	215	D7	•	247	F7	•
152	98	ÿ	184	B8	•	216	D8	•	248	F8	°
153	99	Ö	185	B9	•	217	D9	•	249	F9	·
154	9A	Ü	186	BA	•	218	DA	•	250	FA	·
155	9B	¢	187	BB	•	219	DB	•	251	FB	•
156	9C	£	188	BC	•	220	DC	•	252	FC	•
157	9D	¥	189	BD	•	221	DD	•	253	FD	²
158	9E	•	190	BE	•	222	DE	•	254	FE	•
159	9F	*f*	191	BF	•	223	DF	•	255	FF	Blank

NOTES:

[1] Symbol not displayed.

Keystroke Guide:

Dec #	Keystroke(s)
0	Ctrl 2
1-26	Ctrl A thru Z respectively
27	Ctrl [
28	Ctrl
29	Ctrl]
30	Ctrl 6
31	Ctrl -
32	Space Bar
33-43	Shift and key w/corresponding symbol
44-47	Key w/corresponding symbol
48-57	Key w/corresponding symbol, numerical keypad w/Num Lock active
58	Shift and key w/corresponding symbol
59	Key w/corresponding symbol
60	Shift and key w/corresponding symbol
61	Key w/corresponding symbol
62-64	Shift and key w/corresponding symbol
65-90	Shift and key w/corresponding symbol or key w/corresponding symbol and Caps Lock active
91-93	Key w/corresponding symbol
94, 95	Shift and key w/corresponding symbol
96	Key w/corresponding symbol
97-126	Key w/corresponding symbol or Shift and key w/corresponding symbol and Caps Lock active
127	Ctrl -
128-255	Alt and decimal digit(s) of desired character

Appendix C
KEYBOARD

C.1 INTRODUCTION

This appendix describes the Compaq keyboard that is included as standard with the system unit. The keyboard complies with the industry-standard classification of an “enhanced keyboard” and includes a separate cursor control key cluster, twelve “function” keys, and enhanced programmability for additional functions.

This appendix covers the following keyboard types (some of which may be available only as an option):

- The Windows-version keyboard includes three additional keys for specific support of the Windows operating system.
- The Erase-Ease keyboard features a split spacebar that can be user-programmed to provide easy access to the backspace function or set to operate as the normal spacebar.
- The scanner keyboard includes a built-in document scanner for scanning loose-leaf hardcopy.

> **NOTE:** This appendix discusses only the keyboard unit. The keyboard interface is a function of the system unit and is discussed in Chapter 5, Input/Output Interfaces.

Topics covered in this appendix include the following:

C.2 KEYSTROKE PROCESSING

A functional block diagram of the keystroke processing elements is shown in Figure C-1. Power (+5 VDC) is obtained from the system through the PS/2-type interface. The keyboard uses a Z86C14 (or equivalent) microprocessor. The Z86C14 scans the key matrix drivers every 10 ms for pressed keys while at the same time monitoring communications with the keyboard interface of the system unit. When a key is pressed, a Make code is generated. A Break code is generated when the key is released. The Make and Break codes are collectively referred to as scan codes. All keys generate Make and Break codes with the exception of the Pause key, which generates a Make code only.

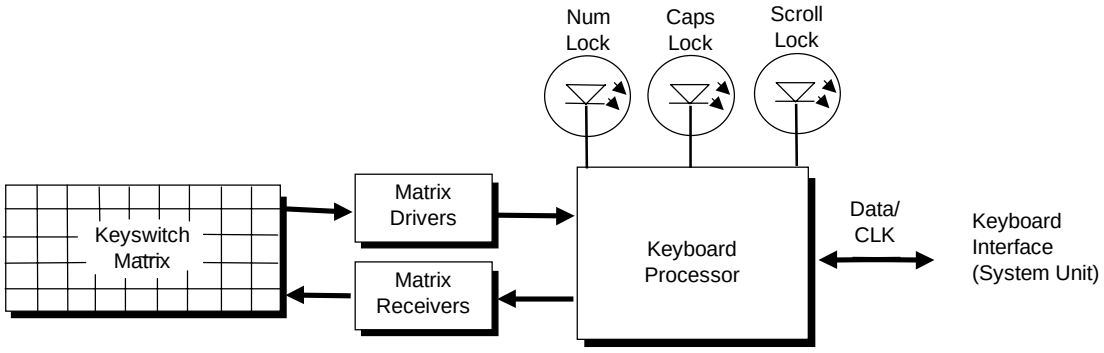


Figure C–1. Keystroke Processing Elements, Block Diagram

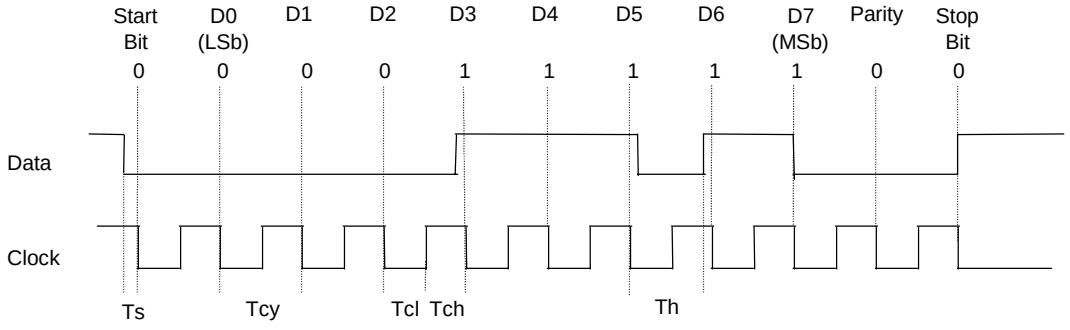
When the system is turned on, the keyboard processor generates a Power-On Reset (POR) signal after a period of 150 ms to 2 seconds. The keyboard undergoes a Basic Assurance Test (BAT) that checks for shorted keys and basic operation of the keyboard processor. The BAT takes from 300 to 500 ms to complete.

If the keyboard fails the BAT, an error code is sent to the CPU and the keyboard is disabled until an input command is received. After successful completion of the POR and BAT, a completion code (AAh) is sent to the CPU and the scanning process begins.

The keyboard processor includes a 16-byte FIFO buffer for holding scan codes until the system is ready to receive them. Response and typematic codes are not buffered. If the buffer is full (16 bytes held) a 17th byte of a successive scan code results in an overrun condition and the overrun code replaces the scan code byte and any additional scan code data (and the respective key strokes) are lost. Multi-byte sequences must fit entirely into the buffer before the respective keystroke can be registered.

C.2.1 TRANSMISSIONS TO THE SYSTEM

The keyboard processor sends two main types of data to the system; commands (or responses to system commands) and keystroke scan codes. Before the keyboard sends data to the system (specifically, to the 8042-type logic within the system), the keyboard verifies the clock and data lines to the system. If the clock signal is low (0), the keyboard recognizes the inhibited state and loads the data into a buffer. Once the inhibited state is removed, the data is sent to the system. Keyboard-to-system transfers consist of 11 bits as shown in Figure C-2.



Parameter	Minimum	Maximum
Tcy (Cycle Time)	60 us	80 us
Tcl (Clock Low)	30 us	35 us
Tch (clock High)	30 us	45 us
Th (Data Hold)	45 us	62 us
Ts (Data Setup)	8 us	14 us

Figure C–2. Keyboard-To-System Transmission of Code 58h, Timing Diagram

The system can halt keyboard transmission by setting the clock signal low. The keyboard checks the clock line every 60 us to verify the signal state. If a low is detected, the keyboard will finish the current transmission **if** the rising edge of the clock pulse for the parity bit has not occurred.

The enhanced keyboard has three operating modes:

- Mode 1 - PC-XT compatible
- Mode 2 - PC-AT compatible (default)
- Mode 3 - Select mode (keys are programmable as to make-only, break-only, typematic)

Modes can be selected by the user or set by the system. Mode 2 is the default mode. Each mode produces a different set of scan codes. When a key is pressed, the keyboard processor sends that key's make code to the 8042 logic of the system unit. The When the key is released, a release code is transmitted as well (except for the Pause key, which produces only a make code). The 8042-type logic of the system unit responds to scan code reception by asserting IRQ1, which is processed by the interrupt logic and serviced by the CPU with an interrupt service routine. The service routine takes the appropriate action based on which key was pressed.

C.2.2 KEYBOARD LAYOUTS

C.2.2.1 Standard Enhanced Keyboards

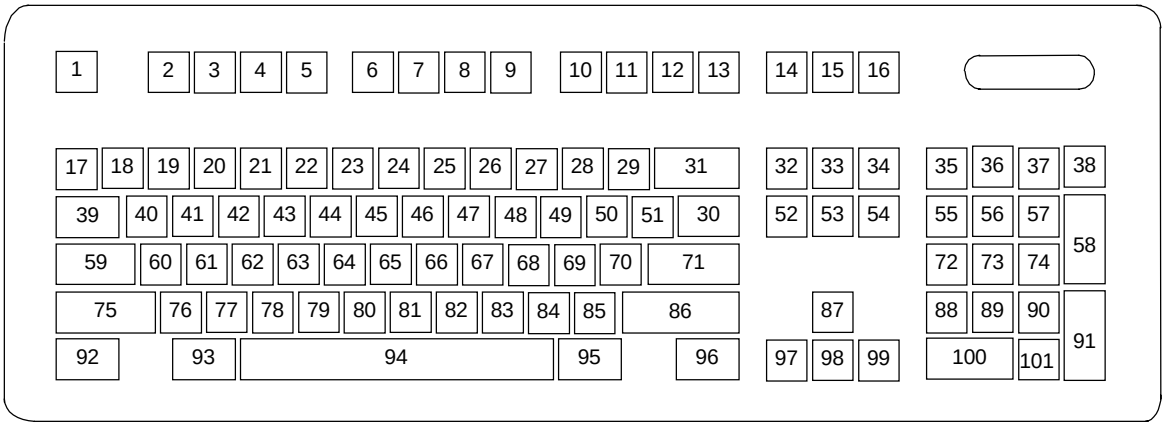


Figure C–3. U.S. English (101-Key) Keyboard Key Positions

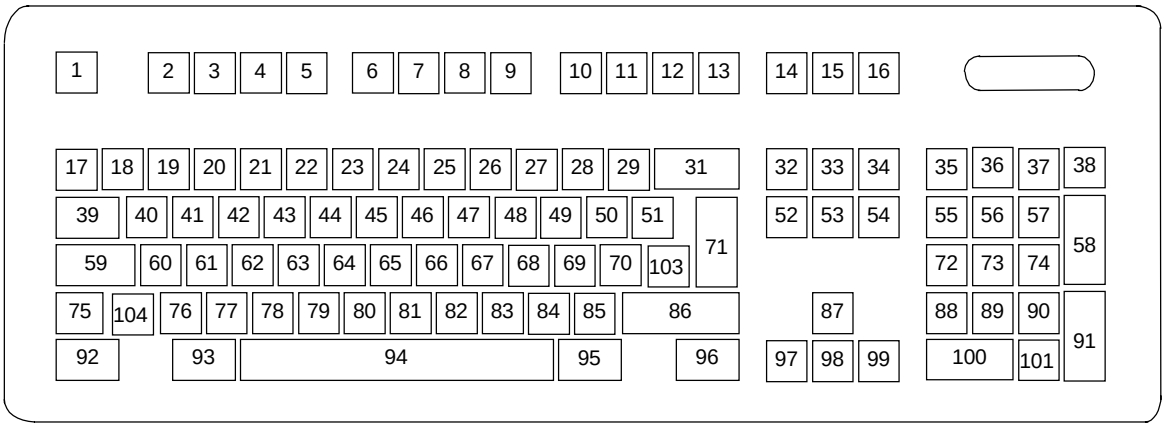


Figure C–4. National (102-Key) Keyboard Key Positions

C.2.2.2 Windows Enhanced Keyboards

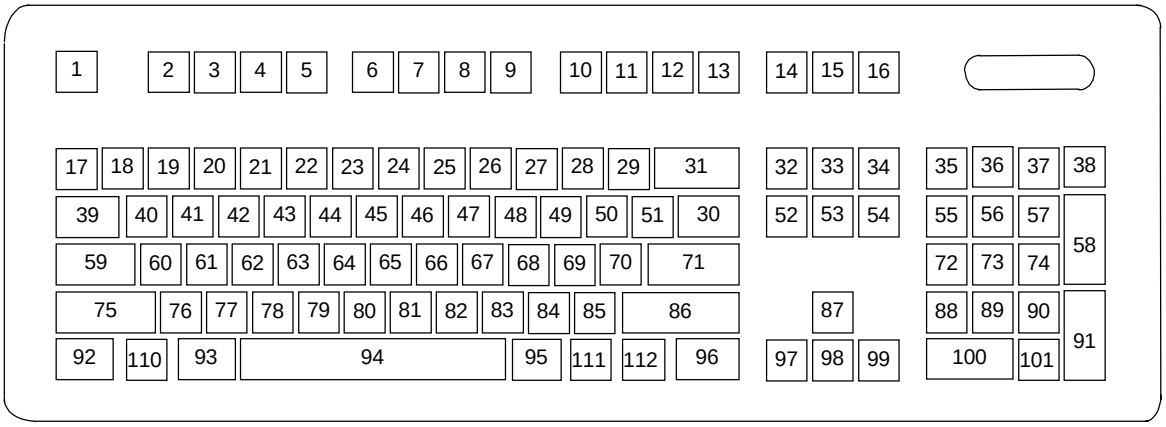


Figure C–5. U.S. English Windows (101W-Key) Keyboard Key Positions

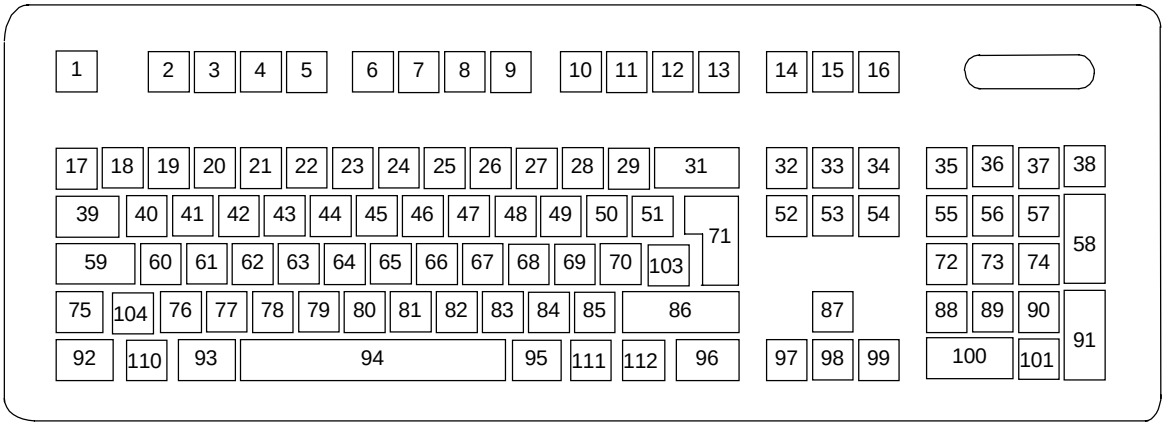


Figure C–6. National Windows (102W-Key) Keyboard Key Positions

C.2.2.3 Windows Enhanced Keyboards w/Erase-Ease

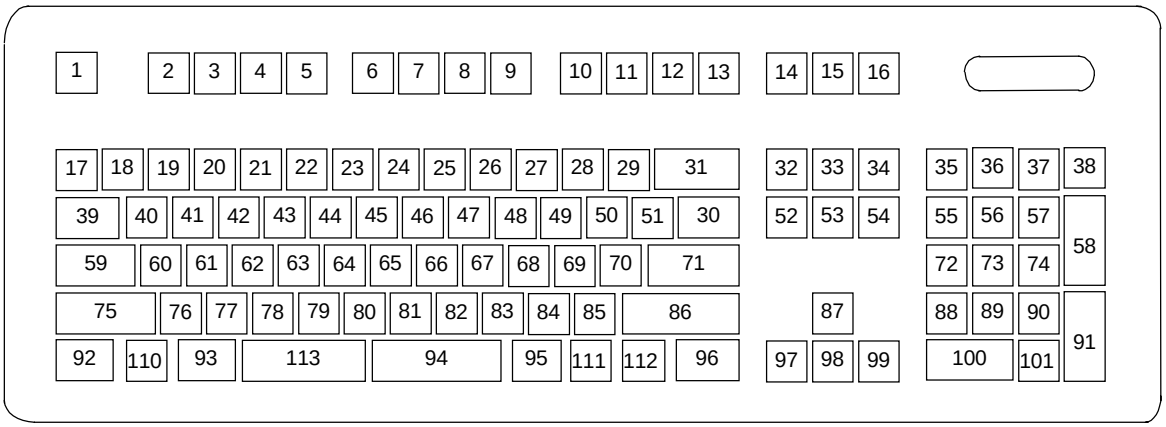


Figure C–7. U.S. English Windows (101WE-Key) Keyboard Key Positions

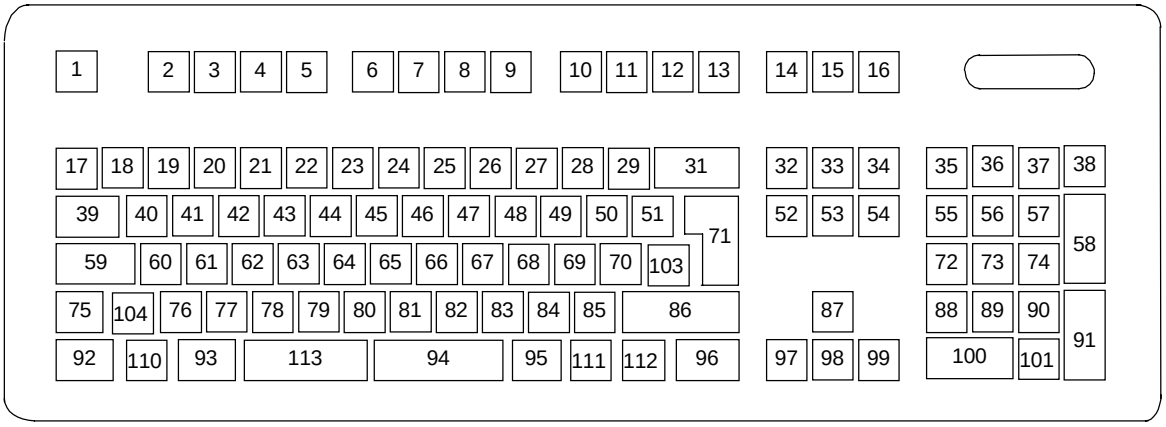


Figure C–8. National Windows (102WE-Key) Keyboard Key Positions

C.2.3 KEYS

All keys generate a make code (when pressed) and a break code (when released) with the exception of the **Pause** key (pos. 16), which produces a make code only. All keys, again, with the exception of the **Pause** key, are also typematic, although the typematic action of the **Shift**, **Ctrl**, **Alt**, **Num Lock**, **Scroll Lock**, **Caps Lock**, and **Ins** keys is suppressed by the BIOS. Typematic keys, when held down, send the make code repetitively at a predetermined rate until the key is released. If two keys are held down, the last key pressed will be typematic.

C.2.3.1 Special Single-Keystroke Functions

The following keys provide the intended function in most applications and environments.

Caps Lock - The **Caps Lock** key (pos. 59), when pressed and released, invokes a BIOS routine that turns on the caps lock LED and shifts into upper case key positions 40-49, 60-68, and 76-82. When pressed and released again, these keys revert to the lower case state and the LED is turned off. Use of the **Shift** key will reverse which state these keys are in based on the **Caps Lock** key.

Num Lock - The **Num Lock** key (pos. 32), when pressed and released, invokes a BIOS routine that turns on the num lock LED and shifts into upper case key positions 55-57, 72-74, 88-90, 100, and 101. When pressed and released again, these keys revert to the lower case state and the LED is turned off.

The following keys provide special functions that require specific support by the application.

Print Scrn - The **Print Scrn** (pos. 14) key can, when pressed, generate an interrupt that initiates a print routine. This function may be inhibited by the application.

Scroll Lock - The **Scroll Lock** key (pos. 15) when pressed and released, , invokes a BIOS routine that turns on the scroll lock LED and inhibits movement of the cursor. When pressed and released again, the LED is turned off and the function is removed. This keystroke is always serviced by the BIOS (as indicated by the LED) but may be inhibited or ignored by the application.

Pause - The **Pause** (pos. 16) key, when pressed, can be used to cause the keyboard interrupt to loop, i.e., wait for another key to be pressed. This can be used to momentarily suspend an operation. The key that is pressed to resume operation is discarded. This function may be ignored by the application.

The **Esc**, **Fn** (function), **Insert**, **Home**, **Page Up**/**Down**, **Delete**, and **End** keys operate at the discretion of the application software.

C.2.3.2 Multi-Keystroke Functions

Shift - The **Shift** key (pos. 75/86), when held down, produces a shift state (upper case) for keys in positions 17-29, 30, 39-51, 60-70, and 76-85 as long as the **Caps Lock** key (pos. 59) is toggled off. If the **Caps Lock** key is toggled on, then a held **Shift** key produces the lower (normal) case for the identified pressed keys. The **Shift** key also reverses the **Num Lock** state of key positions 55-57, 72, 74, 88-90, 100, and 101.

Ctrl - The **Ctrl** keys (pos. 92/96) can be used in conjunction with keys in positions 1-13, 16, 17-34, 39-54, 60-71, and 76-84. The application determines the actual function. Both **Ctrl** key positions provide identical functionality. The pressed combination of **Ctrl** and **Break** (pos. 16) results in the generation of BIOS function INT 1Bh. This software interrupt provides a method of exiting an application and generally halts execution of the current program.

Alt - The **Alt** keys (pos. 93/95) can be used in conjunction with the same keys available for use with the **Ctrl** keys with the exception that position 14 (**SysRq**) is available instead of position 16 (**Break**). The **Alt** key can also be used in conjunction with the numeric keypad keys (pos. 55-57, 72-74, and 88-90) to enter the decimal value of an ASCII character code from 1-255. The application determines the actual function of the keystrokes. Both **Alt** key positions provide identical functionality.

The combination keystroke of **Alt** and **SysRq** results in software interrupt 15h, AX=8500h being executed. It is up to the application to use or not use this BIOS function.

The **Ctrl** and **Alt** keys can be used together in conjunction with keys in positions 1-13, 17-34, 39-54, 60-71, and 76-84. The **Ctrl** and **Alt** key positions used and the sequence in which they are pressed make no difference as long as they are held down at the time the third key is pressed. The **Ctrl**, **Alt,** and **Delete** keystroke combination (required twice if in the Windows environment) initiates a system reset (warm boot) that is handled by the BIOS.

C.2.3.3 Windows Keystrokes

Windows-enhanced keyboards include three additional key positions. Key positions 110 and 111 (marked with the Windows logo) have the same functionality and are used by themselves or in combination with other keys to perform specific "hot-key" type functions for the Windows operating system. The defined functions of the Windows logo keys are listed as follows:

Keystroke	Function
Window Logo	Open Start menu
Window Logo + F1	Display pop-up menu for the selected object
Window Logo + TAB	Activate next task bar button
Window Logo + E	Explore my computer
Window Logo + F	Find document
Window Logo + CTRL + F	Find computer
Window Logo + M	Minimize all
Shift + Window Logo + M	Undo minimize all
Window Logo + R	Display Run dialog box
Window Logo + PAUSE	Perform system function
Window Logo + 1-0	Reserved for OEM use (see following text)

The combination keystroke of the Window Logo + 1-0 keys are reserved for OEM use for auxiliary functions (speaker volume, monitor brightness, password, etc.).

Key position 112 (marked with an application window icon) is used in combination with other keys for invoking Windows application functions.

C.2.3.4 Erase-Ease Keystrokes

The Erase-Ease keyboards feature a split space-bar key that operates as two separate keys (positions 113 and 94). The two keys can be configured for one of three modes:

Mode A:
(Power-on default)

113	94
Backspace	Spacebar

Mode B:

113	94
Spacebar	Backspace

Mode C:

113	94
Spacebar	Spacebar

To switch between modes the user holds down the left **ALT**, left **CTRL**, and left **Shift** keys while pressing the Erase-Ease (pos. 113) key once.

C.2.4 KEYBOARD COMMANDS

Table C-1 lists the commands that the keyboard can send to the system (specifically, to the 8042-type logic).

Table C-1.
Keyboard-to-System Commands

Command	Value	Description
Key Detection Error/Over/run	00h [1] FFh [2]	Indicates to the system that a switch closure couldn't be identified.
BAT Completion	AAh	Indicates to the system that the BAT has been successful.
BAT Failure	FCh	Indicates failure of the BAT by the keyboard.
Echo	EEh	Indicates that the Echo command was received by the keyboard.
Acknowledge (ACK)	FAh	Issued by the keyboard as a response to valid system inputs (except the Echo and Resend commands).
Resend	FEh	Issued by the keyboard following an invalid input.
Keyboard ID	83ABh	Upon receipt of the Read ID command from the system, the keyboard issues the ACK command followed by the two IDS bytes.

Note:
[1] Modes 2 and 3.
[2] Mode 1 only.

C.2.5 SCAN CODES

The scan codes generated by the keyboard processor are determined by the mode the keyboard is operating in.

- Mode 1: In Mode 1 operation, the keyboard generates scan codes compatible with 8088-/8086-based systems. To enter Mode 1, the scan code translation function of the keyboard controller must be disabled. Since translation is not performed, the scan codes generated in Mode 1 are identical to the codes required by BIOS. Mode 1 is initiated by sending command F0h with the 01h option byte. Applications can obtain system codes and status information by using BIOS function INT 16h with AH=00h, 01h, and 02h.

- Mode 2: Mode 2 is the default mode for keyboard operation. In this mode, the 8042 logic translates the make codes from the keyboard processor into the codes required by the BIOS. This mode was made necessary with the development of the Enhanced III keyboard, which includes additional functions over earlier standard keyboards. Applications should use BIOS function INT 16h, with AH=10h, 11h, and 12h for obtaining codes and status data. In Mode 2, the keyboard generates the Break code, a two-byte sequence that consists of a Make code immediately preceded by F0h (i.e., Break code for 0Eh is "F0h 0Eh").

- Mode 3: Mode 3 generates a different scan code set from Modes 1 and 2. Code translation must be disabled since translation for this mode cannot be done.

Table C-2.
Keyboard Scan Codes

Key Pos.	Legend	Make / Break Codes (Hex) Mode 1	Mode 2	Mode 3
1	Esc	01/81	76/F0 76	08/na
2	F1	3B/BB	05/F0 05	07/na
3	F2	3C/BC	06/F0 06	0F/na
4	F3	3D/BD	04/F0 04	17/na
5	F4	3E/BE	0C/F0 0C	1F/na
6	F5	3F/BF	03/F0 03	27/na
7	F6	40/C0	0B/F0 0B	2F/na
8	F7	41/C1	83/F0 83	37/na
9	F8	42/C2	0A/F0 0A	3F/na
10	F9	43/C3	01/FO 01	47/na
11	F10	44/C4	09/F0 09	4F/na
12	F11	57/D7	78/F0 78	56/na
13	F12	58/D8	07/F0 07	5E/na
14	Print Scrn	E0 2A E0 37/E0 B7 E0 AA E0 37/E0 B7 [1] [2] 54/84 [3]	E0 2A E0 7C/E0 F0 7C E0 F0 12 E0 7C/E0 F0 7C [1] [2] 84/F0 84 [3]	57/na
15	Scroll Lock	46/C6	7E/F0 7E	5F/na
16	Pause	E1 1D 45 E1 9D C5/na E0 46 E0 C6/na [3]	E1 14 77 E1 F0 14 F0 77/na E0 7E E0 F0 7E/na [3]	62/na
17	`	29/A9	0E/F0 E0	0E/F0 0E
18	1	02/82	16/F0 16	46/F0 46
19	2	03/83	1E/F0 1E	1E/F0 1E
20	3	04/84	26/F0 26	26/F0 26
21	4	05/85	25/F0 25	25/F0 25
22	5	06/86	2E/F0 2E	2E/F0 2E
23	6	07/87	36/F0 36	36/F0 36
24	7	08/88	3D/F0 3D	3D/F0 3D
25	8	09/89	3E/F0 3E	3E/F0 3E
26	9	0A/8A	46/F0 46	46/F0 46
27	0	0B/8B	45/F0 45	45/F0 45
28	-	0C/8C	4E/F0 4E	4E/F0 4E
29	=	0D/8D	55/F0 55	55/F0 55
30	\	2B/AB	5D/F0 5D	5C/F0 5C
31	Backspace	0E/8E	66/F0 66	66/F0 66
32	Insert	E0 52/E0 D2 E0 AA E0 52/E0 D2 E0 2A [4] E0 2A E0 52/E0 D2 E0 AA [6]	E0 70/E0 F0 70 E0 F0 12 E0 70/E0 F0 70 E0 12 [5] E0 12 E0 70/E0 F0 70 E0 F0 12 [6]	67/na
33	Home	E0 47/E0 C7 E0 AA E0 52/E0 C7 E0 2A [4] E0 2A E0 47/E0 C7 E0 AA [6]	E0 6C/E0 F0 6C E0 F0 12 E0 6C/E0 F0 6C E0 12 [5] E0 12 E0 6C/E0 F0 6C E0 F0 12 [6]	6E/na
34	Page Up	E0 49/E0 C9 E0 AA E0 49/E0 C9 E0 2A [4] E0 2A E0 49/E0 C9 E0 AA [6]	E0 7D/E0 F0 7D E0 F0 12 E0 7D/E0 F0 7D E0 12 [5] E0 12 E0 7D/E0 F0 7D E0 F0 12 [6]	6F/na
35	Num Lock	45/C5	77/F0 77	76/na
36	/	E0 35/E0 B5 E0 AA E0 35/E0 B5 E0 2A [1]	E0 4A/E0 F0 4A E0 F0 12 E0 4A/E0 F0 4A E0 12 [1]	77/na
37	*	37/B7	7C/F0 7C	7E/na
38	-	4A/CA	7B/F0 7B	84/na
39	Tab	0F/8F	0D/F0 0D	0D/na
40	Q	10/90	15/F0 15	15/na

Continued

([x] Notes listed at end of table.)

Table C-2. Keyboard Scan Codes *(Continued)*

Key Pos	Legend	Make / Break Codes (Hex) Mode 1	Mode 2	Mode 3
41	W	11/91	1D/F0 1D	1D/F0 1D
42	E	12/92	24/F0 24	24/F0 24
43	R	13/93	2D/F0 2D	2D/F0 2D
44	T	14/94	2C/F0 2C	2C/F0 2C
45	Y	15/95	35/F0 35	35/F0 35
46	U	16/96	3C/F0 3C	3C/F0 3C
47	I	17/97	43/F0 43	43/F0 43
48	O	18/98	44/F0 44	44/F0 44
49	P	19/99	4D/F0 4D	4D/F0 4D
50	[	1A/9A	54/F0 54	54/F0 54
51	]	1B/9B	5B/F0 5B	5B/F0 5B
52	Delete	E0 53/E0 D3 E0 AA E0 53/E0 D3 E0 2A [4] E0 2A E0 53/E0 D3 E0 AA [6]	E0 71/E0 F0 71 E0 F0 12 E0 71/E0 F0 71 E0 12 [5] E0 12 E0 71/E0 F0 71 E0 F0 12 [6]	64/F0 64
53	End	E0 4F/E0 CF E0 AA E0 4F/E0 CF E0 2A [4] E0 2A E0 4F/E0 CF E0 AA [6]	E0 69/E0 F0 69 E0 F0 12 E0 69/E0 F0 69 E0 12 [5] E0 12 E0 69/E0 F0 69 E0 F0 12 [6]	65/F0 65
54	Page Down	E0 51/E0 D1 E0 AA E0 51/E0 D1 E0 2A [4] E0 @a E0 51/E0 D1 E0 AA [6]	E0 7A/E0 F0 7A E0 F0 12 E0 7A/E0 F0 7A E0 12 [5] E0 12 E0 7A/E0 F0 7A E0 F0 12 [6]	6D/F0 6D
55	7	47/C7 [6]	6C/F0 6C [6]	6C/na [6]
56	8	48/C8 [6]	75/F0 75 [6]	75/na [6]
57	9	49/C9 [6]	7D/F0 7D [6]	7D/na [6]
58	+	4E/CE [6]	79/F0 79 [6]	7C/F0 7C
59	Caps Lock	3A/BA	58/F0 58	14/F0 14
60	A	1E/9E	1C/F0 1C	1C/F0 1C
61	S	1F/9F	1B/F0 1B	1B/F0 1B
62	D	20/A0	23/F0 23	23/F0 23
63	F	21/A1	2B/F0 2B	2B/F0 2B
64	G	22/A2	34/F0 34	34/F0 34
65	H	23/A3	33/F0 33	33/F0 33
66	J	24/A4	3B/F0 3B	3B/F0 3B
67	K	25/A5	42/F0 42	42/F0 42
68	L	26/A6	4B/F0 4B	4B/F0 4B
69	;	27/A7	4C/F0 4C	4C/F0 4C
70	‘	28/A8	52/F0 52	52/F0 52
71	Enter	1C/9C	5A/F0 5A	5A/F0 5A
72	4	4B/CB [6]	6B/F0 6B [6]	6B/na [6]
73	5	4C/CC [6]	73/F0 73 [6]	73/na [6]
74	6	4D/CD [6]	74/F0 74 [6]	74/na [6]
75	Shift (left)	2A/AA	12/F0 12	12/F0 12
76	Z	2C/AC	1A/F0 1A	1A/F0 1A
77	X	2D/AD	22/F0 22	22/F0 22
78	C	2E/AE	21/F0 21	21/F0 21
79	V	2F/AF	2A/F0 2A	2A/F0 2A
80	B	30/B0	32/F0 32	32/F0 32

Continued

([x] Notes listed at end of table.)

Table C-2. Keyboard Scan Codes *(Continued)*

Key Pos.	Legend	Make / Break Codes (Hex) Mode 1	Mode 2	Mode 3
81	N	31/B1	31/F0 31	31/F0 31
82	M	32/B2	3A/F0 3A	3A/F0 3A
83	,	33/B3	41/F0 41	41/F0 41
84	.	34/B4	49/F0 49	49/F0 49
85	/	35/B5	4A/F0 4A	4A/F0 4A
86	Shift (right)	36/B6	59/F0 59	59/F0 59
87	↑	E0 48/E0 C8 E0 AA E0 48/E0 C8 E0 2A [4] E0 2A E0 48/E0 C8 E0 AA [6]	E0 75/E0 F0 75 E0 F0 12 E0 75/E0 F0 75 E0 12 [5] E0 12 E0 75/E0 F0 75 E0 F0 12 [6]	63/F0 63
88	1	4F/CF [6]	69/F0 69 [6]	69/na [6]
89	2	50/D0 [6]	72/F0 72 [6]	72/na [6]
90	3	51/D1 [6]	7A/F0 7A [6]	7A/na [6]
91	Enter	E0 1C/E0 9C	E0 5A/F0 E0 5A	79/F0 79[6]
92	Ctrl (left)	1D/9D	14/F0 14	11/F0 11
93	Alt (left)	38/B8	11/F0 11	19/F0 19
94	(Space)	39/B9	29/F0 29	29/F0 29
95	Alt (right)	E0 38/E0 B8	E0 11/F0 E0 11	39/na
96	Ctrl (right)	E0 1D/E0 9D	E0 14/F0 E0 14	58/na
97	←	E0 4B/E0 CB E0 AA E0 4B/E0 CB E0 2A [4] E0 2A E0 4B/E0 CB E0 AA [6]	E0 6B/Eo F0 6B E0 F0 12 E0 6B/E0 F0 6B E0 12[5] E0 12 E0 6B/E0 F0 6B E0 F0 12[6]	61/F0 61
98	↓	E0 50/E0 D0 E0 AA E0 50/E0 D0 E0 2A [4] E0 2A E0 50/E0 D0 E0 AA [6]	E0 72/E0 F0 72 E0 F0 12 E0 72/E0 F0 72 E0 12[5] E0 12 E0 72/E0 F0 72 E0 F0 12[6]	60/F0 60
99	→	E0 4D/E0 CD E0 AA E0 4D/E0 CD E0 2A [4] E0 2A E0 4D/E0 CD E0 AA [6]	E0 74/E0 F0 74 E0 F0 12 E0 74/E0 F0 74 E0 12[5] E0 12 E0 74/E0 F0 74 E0 F0 12[6]	6A/F0 6A
100	0	52/D2 [6]	70/F0 70 [6]	70/na [6]
101	.	53/D3 [6]	71/F0 71 [6]	71/na [6]
102	na	7E/FE	6D/F0 6D	7B/F0 7B
103	na	2B/AB	5D/F0 5D	53/F0 53
104	na	36/D6	61/F0 61	13/F0 13
110	(Win95) [7]	E0 5B/E0 DB E0 AA E0 5B/E0 DB E0 2A [4] E0 2A E0 5B/E0 DB E0 AA [6]	E0 1F/E0 F0 1F E0 F0 12 E0 1F/E0 F0 1F E0 12 [5] E0 12 E0 1F/E0 F0 1F E0 F0 12 [6]	8B/F0 8B
111	(Win95) [7]	E0 5C/E0 DC E0 AA E0 5C/E0 DC E0 2A [4] E0 2A E0 5C/E0 DC E0 AA [6]	E0 2F/E0 F0 27 E0 F0 12 E0 27/E0 F0 27 E0 12 [5] E0 12 E0 27/E0 F0 27 E0 F0 12 [6]	8C/F0 8C
112	(Win Apps) [7]	E0 5D/E0 DD E0 AA E0 5D/E0 DD E0 2A [4] E0 2A E0 5D E0 DD E0 AA [6]	E0 2F/E0 F0 2F E0 F0 12 E0 2F/E0 F0 2F E0 12 [5] E0 12 E0 2F/E0 F0 2F E0 F0 12 [6	8D/F0 8D
113	(Erase-Ease) [8]	0E/8E	66/F0 66	66/na

NOTES:

All codes assume Shift, Ctrl, and Alt keys inactive unless otherwise noted.
NA = Not applicable
[1] Shift (left) key active.
[2] Ctrl key active.
[3] Alt key active.
[4] Left Shift key active. For active right Shift key, substitute AA/2A make/break codes for B6/36 codes.
[5] Left Shift key active. For active right Shift key, substitute F0 12/12 make/break codes for F0 59/59 codes.
[6] Num Lock key active.
[7] Windows keyboards only
[8] Erase-Ease keyboards only

C.3 SCANNER DESCRIPTION

The scanner keyboard, available as an option, integrates a scanner with a SpaceSaver Windows ’95 keyboard, providing the ability to scan hardcopy looseleaf documents for faxing or electronic storage. The scanner provides resolutions up to 400 dpi and 256 shades of gray and outputs through a standard serial interface to the system unit. Using optical character recognition (OCR) support software, printed textual data can be converted into editable files.

Operation of the scanner starts automatically when a sheet is inserted into the Contact Image Sensor (CIS). A button on the left side of the keyboard allows then operator to open a menu, halt scanning in progress, or invoke a serial port test. Figure C-9 shows a block diagram of the key scanner elements.

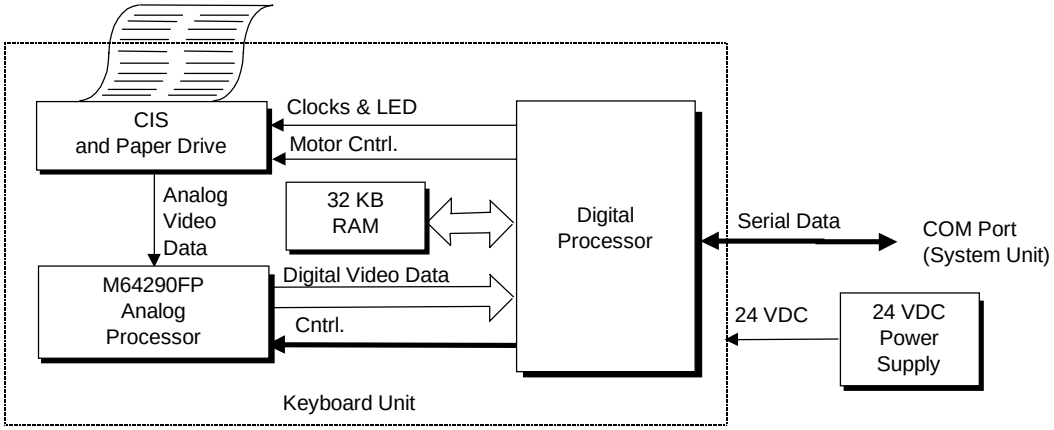


Figure C–9. Scanner Elements, Block Diagram

The Contact Image Sensor (CIS) and paper drive unit handles the hardcopy input. As each sheet is placed into the input slot, the sheet activates the mechanism and is drawn through and scanned by an LED illumination/photodiode sensor array. The drive motor provides 96 steps per revolution (3.75 degress per step) and is geared for 0.005 inch document movement per step for a resolution of 200 dpi. Half-stepping provides 400 dpi vertical resolution.

An analog video data stream is developed and routed to the Digital-to-Analog (D/A) Processor for conversion to digital video data that is routed to the Digital Processor. The Digital Processor provides most of the control of the scanner operation. A 32-KB RAM provides storage of executable code, pixel-to-pixel correction values, image processing line/diffusion data, and transmission data buffering.

The scanner elements are powered from an external 24 VDC power supply. Internal components use +5, +9, and -12 VDC.

C.3.1 SCANNER OPERATION

The scanner requires minimum user interface for normal operation. Insertion of a sheet of hardcopy activates the scanner. Operating parameters such as resolution, brightness, and motor speed are programmable for optimum performance. Other characteristics such as gamma correction, modulation transfer function (MTF), image compression, and pixel normalization are optimized through the use of pre-computed tables that are downloaded for image correction and adjustments when necessary.

The user interface is provided through a button located to the left of the sheet insertion tray. This normally-open switch provides the following functions depending on when pressed:

When Pressed	Function
During Power-Up	Scanner enters communications loopback mode. Mode remains in effect until the next power cycle (cold boot).
Scanner at idle	Actives a menu for changing/viewing parameters.
During a scan	Aborts the scan and reverses the motor, backing the document out of the scanner.

An inserted document activates one or more of five sensing fingers mounted on a shaft. The shaft begins rotation, turning an opaque flag that breaks an opto-interrupter beam between an LED and a phototransistor. The paper sensor signal goes active high, initiating the Digital Processor to begin the scanning process.

An LED/phototransistor assembly similar to the paper sensor is used for skew control. Sensing fingers on each side of the paper path check for misalignment (skew) of the document as it is pulled through the scan area. If the document comes in contact with one of the sensor fingers, an opaque flag is engaged to rotate, blocking an opto-interrupter beam and initiating an abort sequence. The skew LEDs , along with the LEDs used for scanning, are only powered up during the scan operation (i.e., while a document is in the scanner).

A flow chart of the scanning operation is shown in Figure C-10. Photo-Response Non-Uniformity (PRNU) refers to the fact that not every photosensor in the CIS has the same sensitivity. The PRNU correction stage adjusts for each photosensor's sensistivity level by applying a unique offset and gain value for it. A calibration procedure (initially done at the factory) is used to determine the compensation values for the photo array of the CIS. This data is stored in the CALIBRAT.DAT file on the installation disk and copied to the system unit's hard drive. The data is downloaded to the scanner after power up.

The modulation transfer function (MTF) of the optical system and document motion is corrected by downloading the MTF compensation parameters from the system unit to improve the quality of the scanned image.

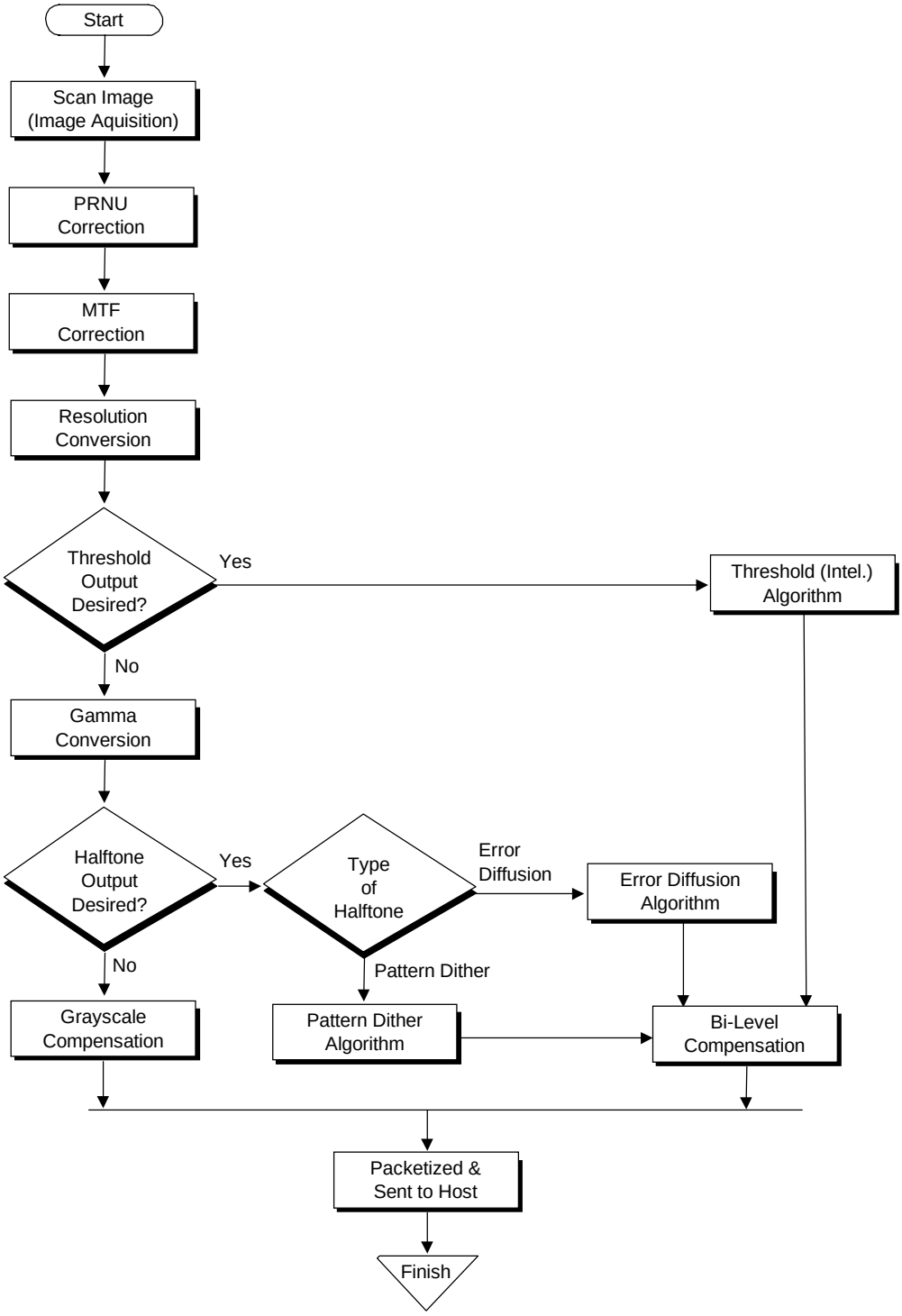


Figure C–10. Scanner operation Flow Chart

C.3.1.1 Resolution/Shade Depth

The drive motor mechanism of the CIS supports a vertical resolution of 400 dpi. The CIS provides a maximum horizontal resolution of 200 dpi. These factors provide true spatial resolutions of 100 and 200 dpi. Using horizontal interpolation, pseudo 300 and 400 dpi spatial resolutions are possible. Shade depth is determined by the number of bits used to control each pixel. The bits per pixel (bpp) parameter can be set to one (for black and white), two, four, or eight (for 256 shades of gray).

The selected resolution/shade depth determines the scanning time of a given sheet. Table C-3 lists the approximate scanning times for a standard 11 inch sheet using specified resolution/shade depths based on the line integration time of 2.5 ms.

Table C-3.
Scanner Performance Chart

		Scan Time for 11" Page		
X / Y	**DPI**	**1 bpp**	**4 bpp**	**8 bpp**
100 / 100	100	7 sec	11 sec	14 sec
200 / 200	200	7 sec	27 sec	36 sec
200 / 300	300 (Pseudo)	12 sec	60 sec	60 sec
200 / 400	400 (Pseudo)	17 sec	62 sec	80 sec

NOTE:
Scan times measured on a Pentium/90-based system with 16 MB RAM.

C.3.1.2 Image Quality

Brightness is fully programmable and independently adjustable using either normal or intelligent methods. The normal method slices each gray scale pixel into either black or white depending on the threshold value selected. The intelligent method automatically adjusts the pixel to the background for the best detail.

The grayscale transfer function can be tailored by gamma correction values that are downloaded from the system. This function can be disabled if desired.

Compensation for the Modulation Transfer Function (MTF) of the optical system and document motion is provided for improving image quality. The MTF parameters are /downloaded from the host if (if enabled).

Image compression is provided through a table-driven compressor. Compression values are loadable from the host and used by one of two types of algorithms: Huffman DPCM for 2- to 8-bit grayscale images, and a proprietary 1-bit compression.

C.3.2 SCANNER INTERFACE

The scanner communicates with the system unit (host) using a serial port as the primary choice of connection. The scanner interface is adaptable to several types of host connections as shown in Table C-4 (unshaded portion describes standard scanner interface with Compaq system unit).

Table C-4.
Scanner I/F Signals

Scanner Signals		Serial Port (PC)			Parallel Port		Serial Port (MacIntosh)	
Pnyb Mode	Mser Mode	RS232 Signal	DB9 Pin	DB25 Pin	Signal	DB25 Pin	Signal	DIN8 Pin
P0	SCLK	CTS	8	5	Select	13	HSKIn	2
P1		DSR	6	6	Paper Out	12	--	--
P2		RI	9	22	Ack	10	--	--
P3		DCD	1	8	Busy	11	--	--
PCLK	DTR	DTR	4	20	Strobe	1	HSKOut	1
SOUT	TXD	RTS	7	4	Init	16	TXD	6
GND	--	GND	5	7	GND	18	GND/RXD+	4/8
PnP	RXD	--	2	3	--	--	RXD-	5

Optional interface configuration.

The scanner uses one of two communication modes; Pnyb and Mser. The scanner selects the mode based on the idle status of the DTR/PCLK signal. If detected in a low state, the scanner uses the Pnyb mode. If PCLK is detected in a high state at idle, then the Mser mode is used.

Switching between the Pnyb and Mser modes is automatic and transparent to the operating system and application. This allows the scanner to be configured through an A/B box to two systems using different interfaces. The system unit (host) must drive the DTR signal at the appropriate level for at least 20 us before transmitting data packets.

A packet consists of an exchange of one or more bytes between the scanner and the host. A session is an exchange of packets between the scanner and the host. A session begins with a single-byte packet called a wakeup code and ends with the transfer of an acknowledgment (ACK) of the last packet received. Either the scanner or the host can initiate a session, and a session can be ended or cancelled by the scanner or the host, regardless of which initiated the session. A session is restricted to the action specified in the wakeup code.

C.3.2.1 Pnyb Mode

In the parallel nibble or "Pnyb" mode, the scanner transfers scanned information to the system unit (host) four bits (a nibble) at a time using the P3..P0 signals, which conform to RS-232 voltage and timing specifications. The P3..P0 signals are mapped to bits <7..4> respectively of the Modem Status Register (primary address 3FEh). The nibbles are clocked into the host with each transition of the PCLK signal. PCLK transitions from low to high clock in a high nibble, which transitions from high to low clock in a low nibble. The host can assume a nibble from the scanner is ready to be read 3.3 us after the PCLK transition requesting it. At the end of a scanner-to-host packet transfer, the host toggles the PCLK signal an extra time (0-to-1-to-0). This extra toggle indicates to the scanner that the last nibble has been read and sets the P3..P0 lines signals to a waiting state.

Data from the system unit (host) is transferred serially (bit-by-bit) as the SO signal along with the PCLK signal. A data bit is clocked with each transition of the PCLK signal so that a byte is transferred with four PCLK cycles. These signals also conform to RS-232 voltage and timing specifications and are mapped at bits <1,0> of the Modem Control Register (primary address 3FCh). The scanner can read data as long as the setup time is at least 1 us and the hold time is at least 3.3 us. The host must allow an additional 50 us after sending the LSb of each of the first five bytes of a multi-byte packet to the scanner. During host-to-scanner transfers, the scanner uses the P3..P0 lines for indicating transmission status to the host.

In the Pnyb mode, the host must insure that the high state of the first PCLK cycle of a session completes in less than 10 us so that the scanner does not interpret a Mser mode transfer.

C.3.2.2 Mser Mode (MacIntosh Connection Only)

The MacIntosh Serial or "Mser" mode uses bit-serial transfers for both scanner-to-host (RXD signal) as well as host-to-scanner (TXD signal) transfers. Transfers are accomplished using 10-bit frames that consist of a start bit, a data byte (LSb first), and a stop bit. The clock (SCLK) signal is provided by the scanner. The Mser mode is similar to isochronous transmission.

C.3.3 SCANNER SPECIFICATIONS/REQUIREMENTS

Table C-5.
Scanner Specifications

Parameter	Specification [1]
Dimensions (Complete keyboard unit):	
Width	20.5 in (52.07 cm)
Height	2.5 in (6.35 cm)
Depth	9 in (22.86 cm)
Weight (Complete keyvoard unit)	10.1 lb (4.58 kg)
Scanner Paper Sizes:	
Minimum	2.0 x 3.0 in (5.1 x 7.6 cm)
Maximum	8.5 x 30 in 21.6 x 76.2 cm)
Maximum Scanned Resolution (input)	2400 x 2400 dpi
Maximum Scanning Resolution (output)	400 dpi
Maximum Scan Time (8.5 x 11" sheet)	6 seconds [2]
Power Requirements (Scanner only):	
Input Voltage	24 VDC
Maximum Current Drain (scanning)	990 ma
Environmental Conditions:	
Tempurature, operating	50°-104° F (10°-40° C)
Tempurature, non-operating	-4°-140° F (-20°-60° C)
Humidity, operating	20-80% RH
Humidity, non-operating	5-95% RH

NOTE:
[1] Metric numbers shown in parenthesis.
[2] Based on Pentium/90-based system w/16 MB RAM

The scanner imposes the following requirements on the host system:

- 486 or better microprocessor
- Serial port
- Windows 3.1, Windows for Workgroups 3.11, or Windows 95 or later
- 4 megabytes of RAM (8 megabytes recommended)
- 50 megabytes free disk space

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