High Speed Converter Evaluation Platform

HSC-ADC-EVALC

FEATURES

Xilinx Virtex-4 FPGA-based buffer memory board
Used for capturing digital data from high speed ADC evaluation boards to simplify evaluation
64 kB FIFO depth
Parallel input at 644 MSPS SDR and 800 MSPS DDR
Supports 1.8 V, 2.5 V, and 3.3 V CMOS and LVDS interfaces
Supports multiple ADC channels up to 18 bits
Measures performance with VisualAnalog
Real-time FFT and time domain analysis
Analyzes SNR, SINAD, SFDR, and harmonics
Simple USB port interface (2.0)
Supports ADCs with serial port interfaces (SPI)
FPGA reconfigurable via JTAG, on-board EPROM, or USB
On-board regulator circuit speeds setup
5 V, 3 A switching power supply included
Compatible with Windows 98 (2nd edition), Windows 2000, Windows ME, and Windows XP

EQUIPMENT NEEDED

Analog signal source and antialiasing filter
Low jitter clock source
High speed ADC evaluation board and ADC data sheet
PC running Windows 98 (2nd edition), Windows 2000, Windows ME, or Windows XP
Latest version of VisualAnalog
USB 2.0 port recommended (USB 1.1 compatible)

PRODUCT HIGHLIGHTS

1. Easy to Set Up. Connect the included power supply along with the CLK and AIN signal sources to the two evaluation boards. Then connect to the PC via the USB port and evaluate the performance instantly.
2. USB Port Connection to PC. PC interface is via a USB 2.0 connection (1.1 compatible) to the PC. A USB cable is provided in the kit.
3. 64 kB FIFO. The on-board FPGA contains an integrated FIFO to store data captured from the ADC for subsequent processing.
4. Up to 644 MSPS SDR/800 MSPS DDR Encode Rates on Each Channel. Multichannel ADCs with encode rates up to 644 MSPS SDR and 800 MSPS DDR can be used with the ADC capture board.
5. Supports ADCs with Serial Port Interface or SPI. Some ADCs include a feature set that can be changed via the SPI. The ADC capture board supports these SPI-driven features through the existing USB connection to the computer without additional cabling needed.
6. VisualAnalog™. VisualAnalog supports the HSC-ADC-EVALC hardware platform as well as enabling virtual ADC evaluation using ADIsimADC™, Analog Devices proprietary behavioral modeling technology. This allows rapid comparison between multiple ADCs, with or without hardware evaluation boards. For more information, see AN-737 at www.analog.com/VisualAnalog.

FUNCTIONAL BLOCK DIAGRAM

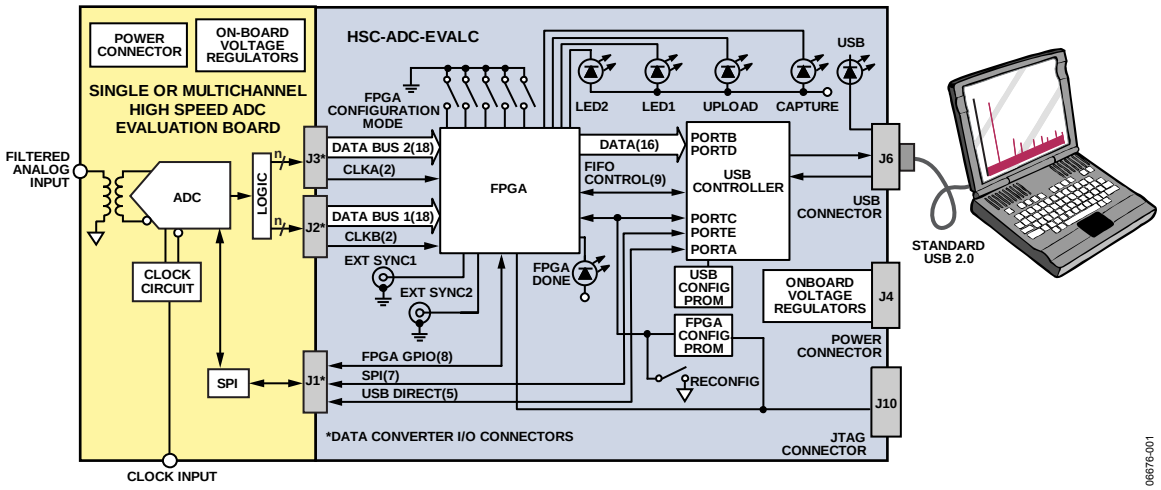

Figure 1.

Rev. 0

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REVISION HISTORY

4/07—Revision 0: Initial Version

PRODUCT DESCRIPTION

The Analog Devices, Inc. high speed converter evaluation platform (HSC-ADC-EVALC) includes the latest version of VisualAnalog and an FPGA-based buffer memory board to capture blocks of digital data from the Analog Devices high speed analog-to-digital converter (ADC) evaluation boards. The ADC capture board is connected to the PC through a USB port and is used with VisualAnalog to quickly evaluate the performance of high speed ADCs. Users can view an FFT for a specific analog input and encode rate to analyze SNR, SINAD, SFDR, and harmonic information.

The ADC capture board is easy to set up. Additional equipment needed includes an Analog Devices high speed ADC evaluation board, a signal source, and a clock source. Once the kit is connected and powered, the evaluation is enabled instantly on the PC.

The ADC capture board enables numerous expansion and evaluation possibilities by virtue of its powerful reconfigurable FPGA core.

The system can acquire digital data at speeds up to 644 MSPS single data rate (SDR) and 800 MSPS double data rate (DDR).

The FPGA contains an integrated FIFO memory that allows capture of data record lengths up to a total of 64 kB. A USB 2.0 microcontroller communicating with VisualAnalog allows for easy interfacing to newer computers using the USB 2.0 (USB 1.1 compatible) interface.

EVALUATION BOARD DESCRIPTION

The ADC capture board provides all of the support circuitry required to accept two 18-bit channels from an ADC's parallel CMOS or LVDS outputs. Various functions such as FPGA configuration load options and I/O logic levels can be selected by proper connection of various jumpers or switches (see Table 1). When using the HSC-ADC-EVALC in conjunction with an ADC evaluation board, it is critical that the signal sources used for the ADC board's analog input and clock have very low phase noise (<1 ps rms jitter) to achieve the ultimate performance of the converter.

Proper filtering of the analog input signal to remove harmonics and lower the integrated or broadband noise at the input is also necessary to achieve the specified noise performance.

See Figure 5 to Figure 20 for complete schematics and layout plots.

EVALUATION BOARD HARDWARE

HSC-ADC-EVALC ADC CAPTURE BOARD EASY START

Requirements

- HSC-ADC-EVALC ADC capture board, VisualAnalog, 5 V wall transformer, and USB cable
- High speed ADC evaluation board and ADC data sheet
- Power supply for ADC evaluation board
- Analog signal source and appropriate filtering
- Low jitter clock source applicable for specific ADC evaluation, typically <1 ps rms jitter
- PC running Windows® 98 (2nd edition), Windows 2000, Windows ME, or Windows XP
- PC with a USB 2.0 port recommended (USB 1.1 compatible)

Easy Start Steps

Important Note

Administrative rights for the Windows operating systems are needed during the entire easy start procedure.

Completion of every step before reverting to a normal user mode is recommended.

1. Install VisualAnalog from the CD provided in the ADC capture board kit or download the latest version from the Web. For the latest updates to the software, check the Analog Devices website at www.analog.com/FIFO.
2. Connect the ADC capture board to the ADC evaluation board. If an adapter is required, insert the adapter between the ADC evaluation board and the ADC capture board.
3. Connect the provided USB cable to the ADC capture board and to an available USB port on the computer.
4. Refer to Table 1 for setting the ADC capture board's I/O logic level to match the level coming from the ADC evaluation board. 1.8 V is default; 2.5 V and 3.3 V are jumper selectable. Most evaluation boards can be used with the default settings.
5. The ADC capture board is supplied with a wall mount switching power supply. Connect the supply end to an ac wall outlet rated for 100 Vac to 240 Vac at 47 Hz to 63 Hz. The other end is a 2.1 mm inner diameter jack that connects to the PCB at J4.
6. Once the USB cable is connected to both the computer and the HSC-ADC-EVALC board, and power is applied, the USB driver starts to install. The **Found New Hardware Wizard** opens and prompts you through the automated install process.
7. (Optional) Verify in the Windows device manager that **Analog Devices ADC-HSC-EVALC** is listed under the USB hardware.
8. Refer to the instructions included in the respective ADC data sheet found at www.analog.com/FIFO for more information about connecting the ADC evaluation board's power supply and other requirements. After verification of power supply connections, apply power to the ADC evaluation board and check the voltage levels on the ADC board to make sure they are correct.
9. Make sure the evaluation boards are powered on before connecting the analog input and clock. Connect the appropriate analog input (which should be filtered with a band-pass filter) and low jitter clock signal.
10. Refer to the *VisualAnalog User Manual* at www.analog.com/FIFO for detailed software operating instructions.

POWER SUPPLIES

The ADC capture board is supplied with a wall mount switching power supply that provides a 5 V, 3 A maximum output. Connect the supply to the rated 100 Vac to 240 Vac wall outlet at 47 Hz to 63 Hz. The other end is a 2.1 mm inner diameter jack that connects to the PCB at J4. On the PC board, the supply is fused and conditioned before connecting to the regulators that supply the proper bias to the entire ADC capture board.

CONNECTION AND SETUP

The ADC capture board has two 40-pin connectors (J2 and J3) that accept two 18-bit channels of parallel CMOS or LVDS inputs from the ADC (see Figure *2*). The third 40-pin connector (J1) is used to pass SPI and other USB/FPGA control signals across to adjacent ADC evaluation boards that support these features.

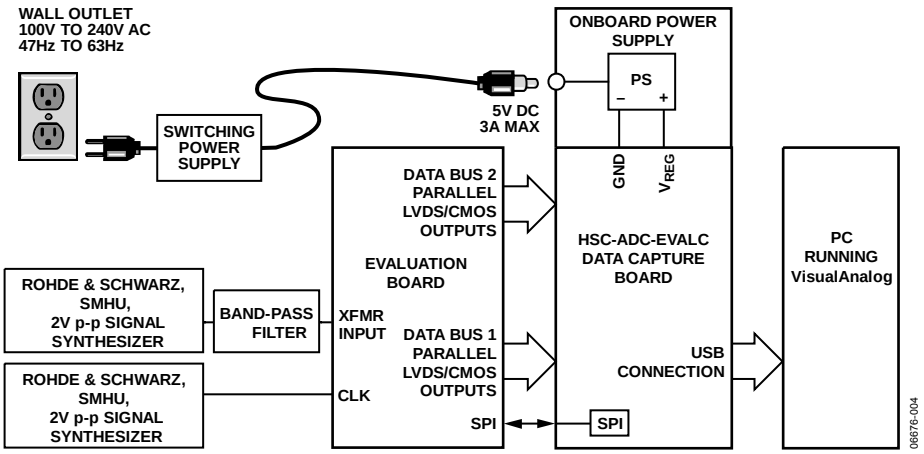


Figure 2. Example Setup Using ADC Evaluation Board and HSC-ADC-EVALC ADC Capture Board

JUMPERS

Default Settings

Table 1 lists the default settings for the HSC-ADC-EVALC evaluation kit.

Table 1. Jumper Configurations

Jumper Number	Description
J9, Pin 1 to Pin 2 (1.8 V)	Default. Sets FPGA I/O voltage to 1.8 V logic (hardwired, do not remove).
J9, Pin 3 to Pin 4 (2.5 V)	Install single jumper here to set FPGA I/O voltage to 2.5 V logic.
J9, Pin 5 to Pin 6 (3.3 V)	Install single jumper here to set FPGA I/O voltage to 3.3 V logic.

Table 2. FPGA Configuration Mode

U4 DIP Switch Setting	M0	M1	M2	M3	M4
FPGA Configured via EEPROM	On	On	On	Reserved	Reserved
FPGA Configured via USB (Default)	On	Off	Off	Reserved	Reserved

HSC-ADC-EVALC ADC CAPTURE BOARD FEATURES

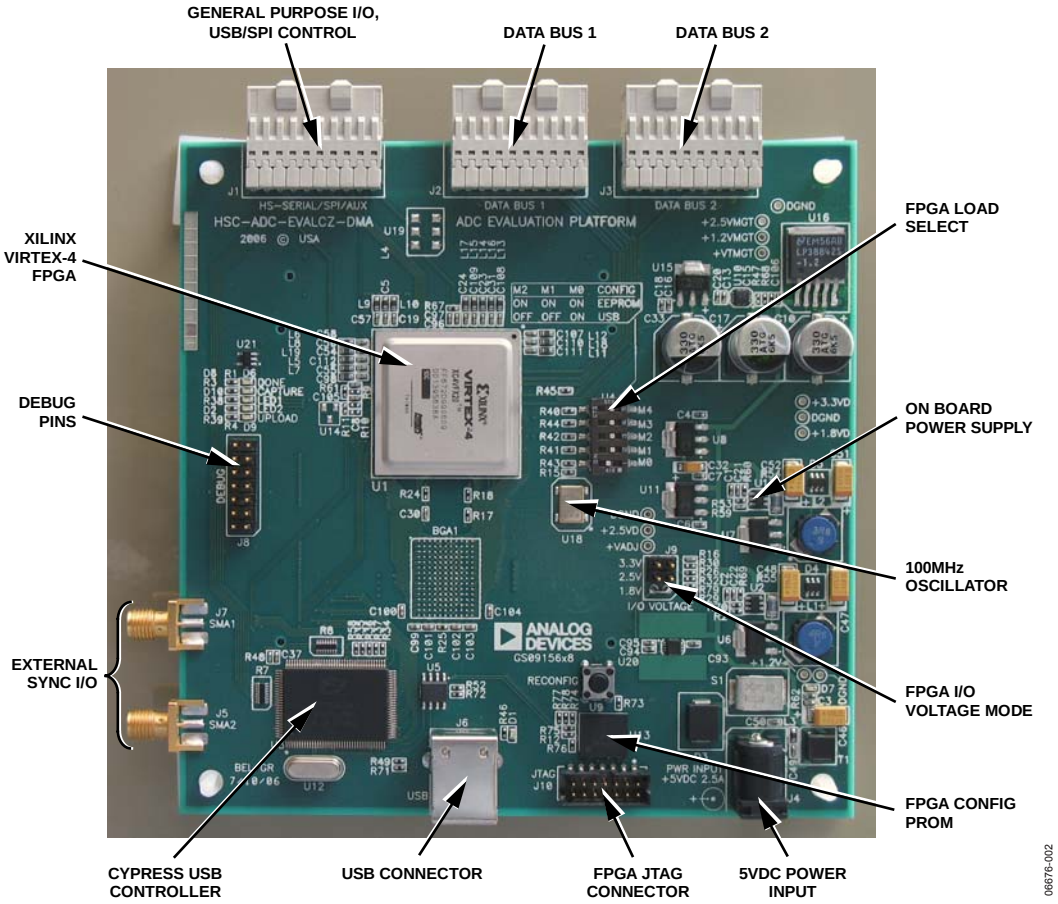


Figure 3. HSC-ADC-EVALC Components (Top View)

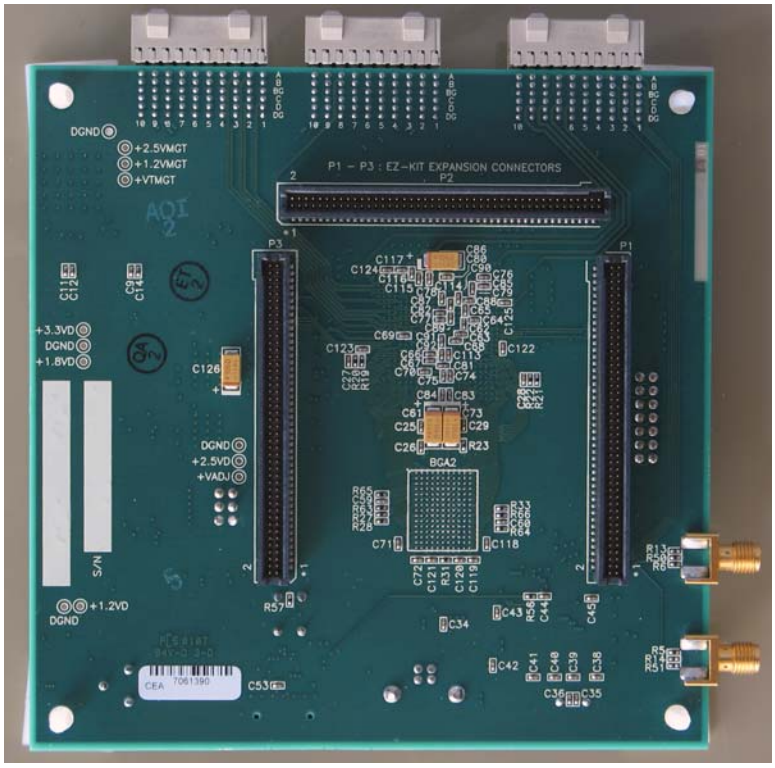


Figure 4. HSC-ADC-EVALC Components (Bottom View)

HSC-ADC-EVALC SUPPORTED ADC EVALUATION BOARDS

Refer to the Analog Devices ADC capture board product page at www.analog.com/FIFO for a list of HSC-ADC-EVALC-compatible ADC evaluation boards. Some legacy ADC boards may require interposer cards to facilitate proper pin mapping to the ADC capture board. If needed, the interposer part number is noted in the compatibility table at www.analog.com/FIFO for the respective data converter.

THEORY OF OPERATION

The HSC-ADC-EVALC evaluation platform is based around the Virtex-4 FPGA (XC4VFX20-10FFG672C) from Xilinx®, which can be programmed through VisualAnalog to operate with a variety of data converters. Another key component, the Cypress USB device (U3), communicates with a host PC and provides the SPI interface used for configuration.

CONFIGURATION

Some converter devices require programming for mode or feature selection, which the SPI controller accomplishes using SPI-accessible register maps. U3 drives the 4-wire SPI (SCLK, SDI, SDO, CSB[1]) signals to the converter board via connector (J1). For more information on serial port interface (SPI) functions, consult the user manual titled *Interfacing to High Speed ADCs via SPI* at www.analog.com/FIFO.

The SPI interface designed on the Cypress IC can communicate with up to five different SPI-enabled devices including the FPGA. The CLK and SDI/SDO data lines are common to all SPI devices. The desired SPI-enabled device is selected for control by using one of the five active low chip select (CS) pins. This functionality is controlled by selecting a SPI channel in the SPI Controller software.

At power-up, VisualAnalog attempts to autodetect the converter that is attached to the ADC capture board using the SPI interface. If a recognized device is found, VisualAnalog selects the appropriate FPGA configuration; otherwise, the user is prompted to make the device selection. In either case, VisualAnalog then programs the FPGA using the SPI interface of U3. The configurations typically program a FIFO data capture function within the FPGA.

INPUT CIRCUITRY

The parallel data input pins of the FPGA, which interface to the converter, are configurable. They can operate with 1.8 V, 2.5 V, or 3.3 V logic levels and can accept LVDS or CMOS inputs. Each channel of the ADC capture board requires a clock signal to capture data. These clock signals are normally provided by the attached ADC evaluation board and are passed along with the data through one or more pins on Connector J2 and/or Connector J3. Refer to the HSC-ADC-EVALC I/O connector pin mappings shown in Figure 21 and Figure 22.

DATA CAPTURE

The process of filling the FIFO and reading the data back requires several steps.

1. VisualAnalog initiates the FIFO fill process by resetting the FIFOs.
2. The 48 MHz USB read clock (RCLK) is then suspended to ensure that it does not add noise to the ADC input.
3. VisualAnalog waits approximately 30 ms to allow for data capture before beginning the readback process. This wait time is an adjustable parameter in VisualAnalog.
4. VisualAnalog reads the data from the FIFO through the USB interface to the PC.

CODE DESCRIPTION

FPGA configuration files are provided by ADI for all ADCs supported by the HSC-ADC-EVALC evaluation platform. These files are designed and tested to facilitate quick performance evaluations of Analog Devices data converters. No additional FPGA programming is required from the user for typical operation.

FPGA CONFIGURATION AND CUSTOMIZATION

Users can manually customize or update the FPGA code through a JTAG connector (J10) provided on the ADC capture board, as shown in Figure 17. However, Analog Devices provides no support or guarantee of performance if the provided code is customized by the user.

The HSC-ADC-EVALC hardware platform may contain additional circuit functions to support future developments and capabilities. These functions are not supported beyond the scope of this data sheet and the Analog Devices supplied data-capture FPGA routines at this time.

Additional FPGA programming support may be available through the user's local Xilinx representative or distributor.

[1] Note that CSB1 is the default CSB line used.

EVALUATION BOARD SCHEMATICS AND ARTWORK

HSC-ADC-EVALC SCHEMATICS

TYCO AND DSP EZ–KIT CONNECTOR TO FPGA

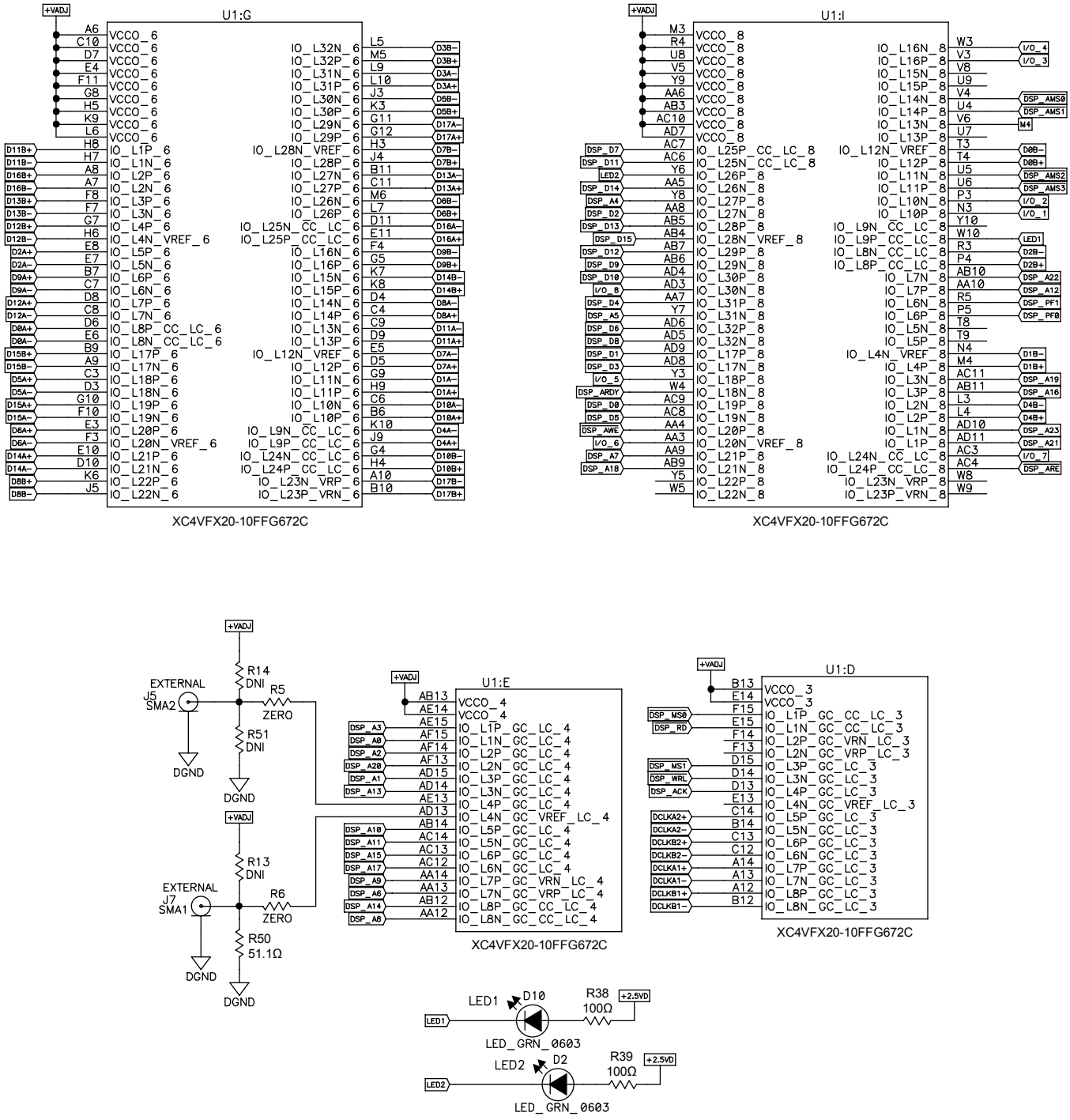


Figure 5.

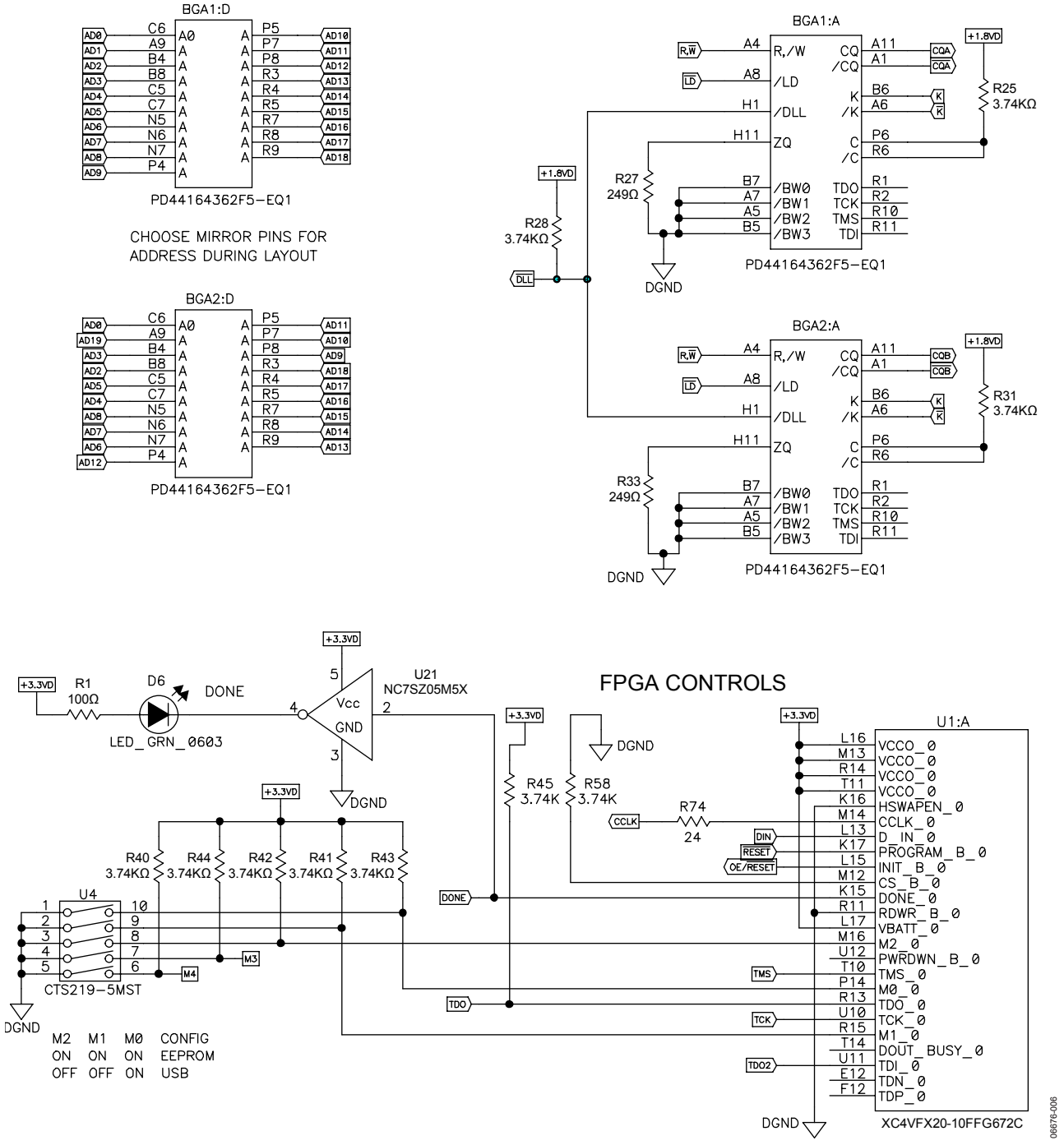


Figure 6.

FPGA TO SRAM DATA

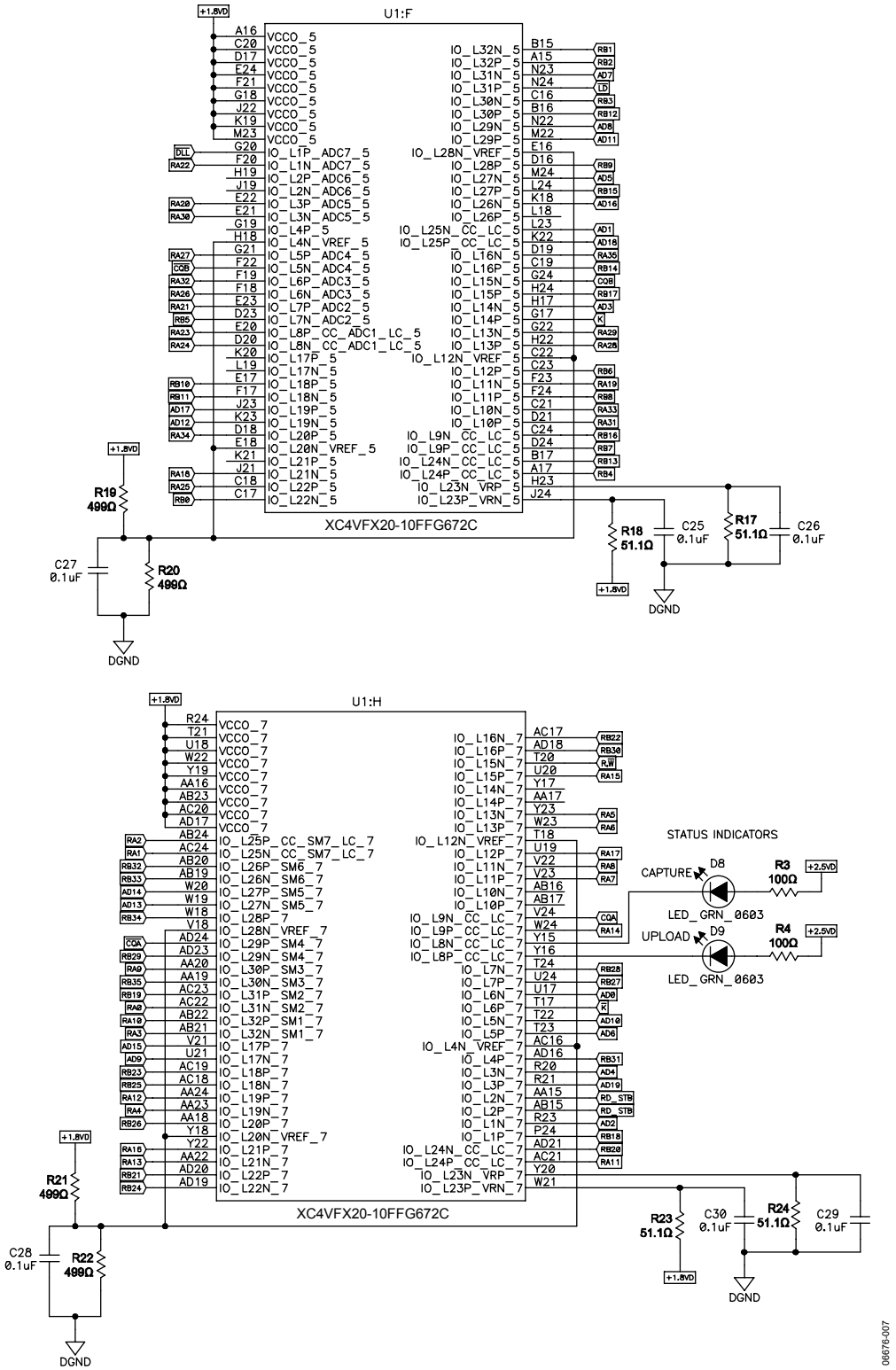


Figure 7.

AD19 TO BE USED WITH HIGHER
DENSITY SRAM DEVICES

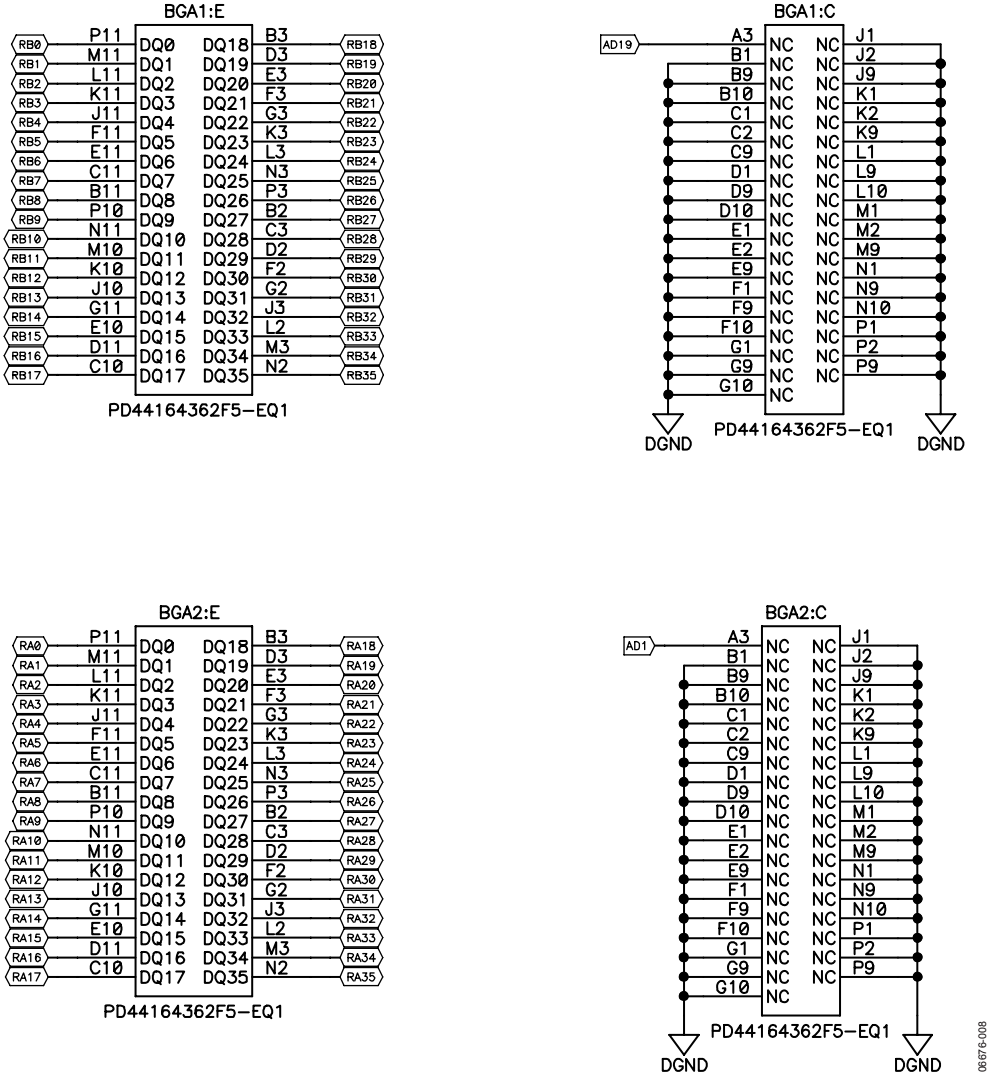


Figure 8.

SRAM AND FPGA POWER

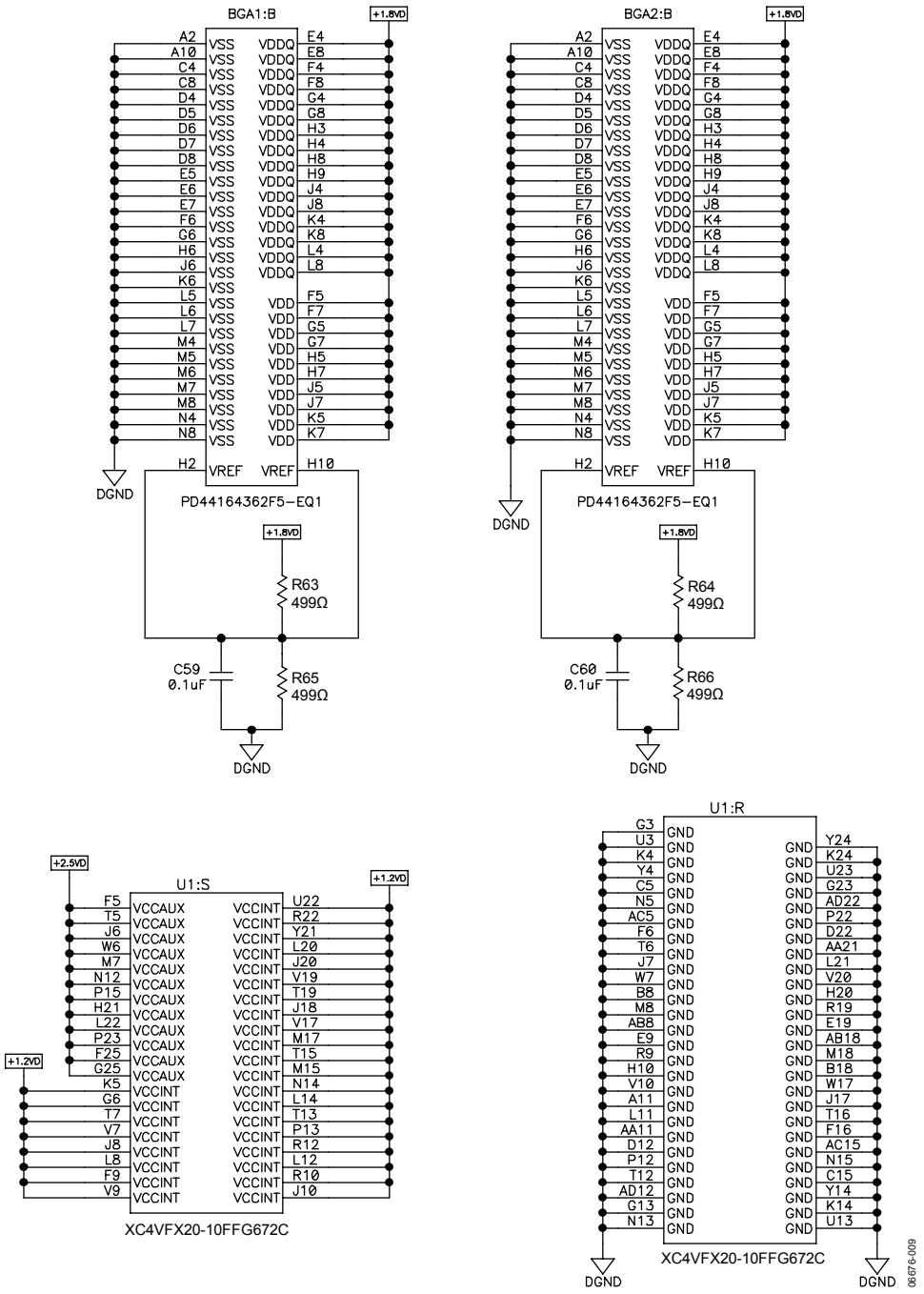


Figure 9.

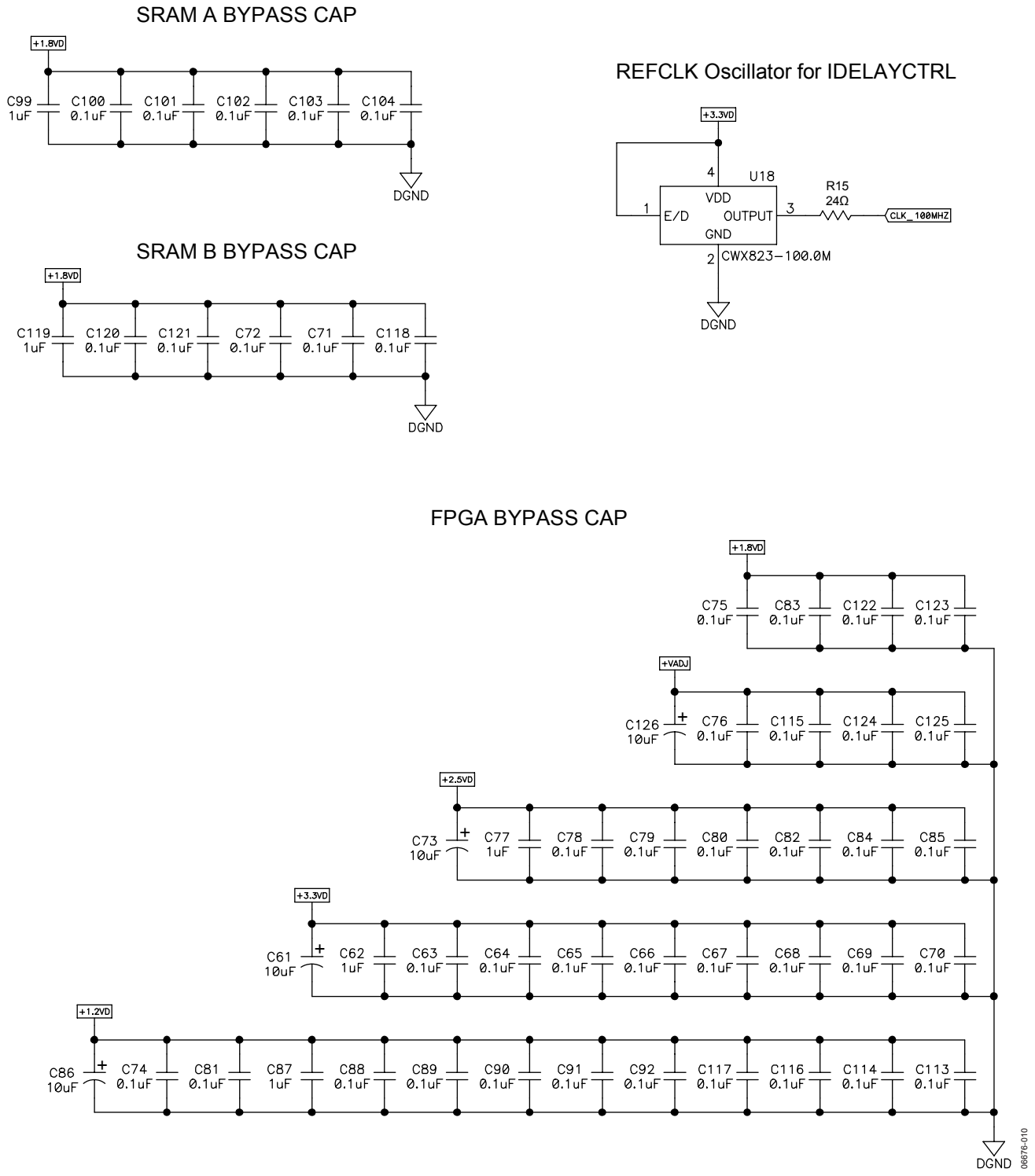
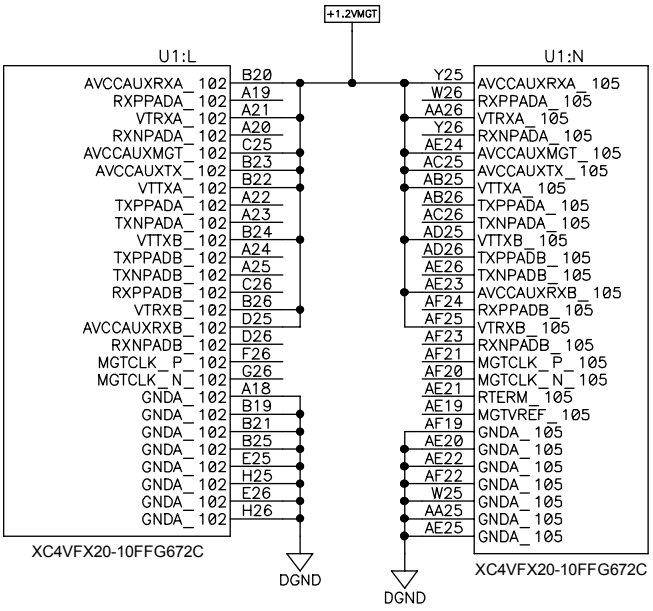


Figure 10.

UNUSED ROCKET I/0 CONNECTIONS



DEBUG PINS

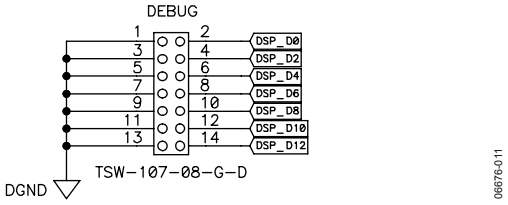


Figure 11.

ROCKET I/0 CONNECTIONS

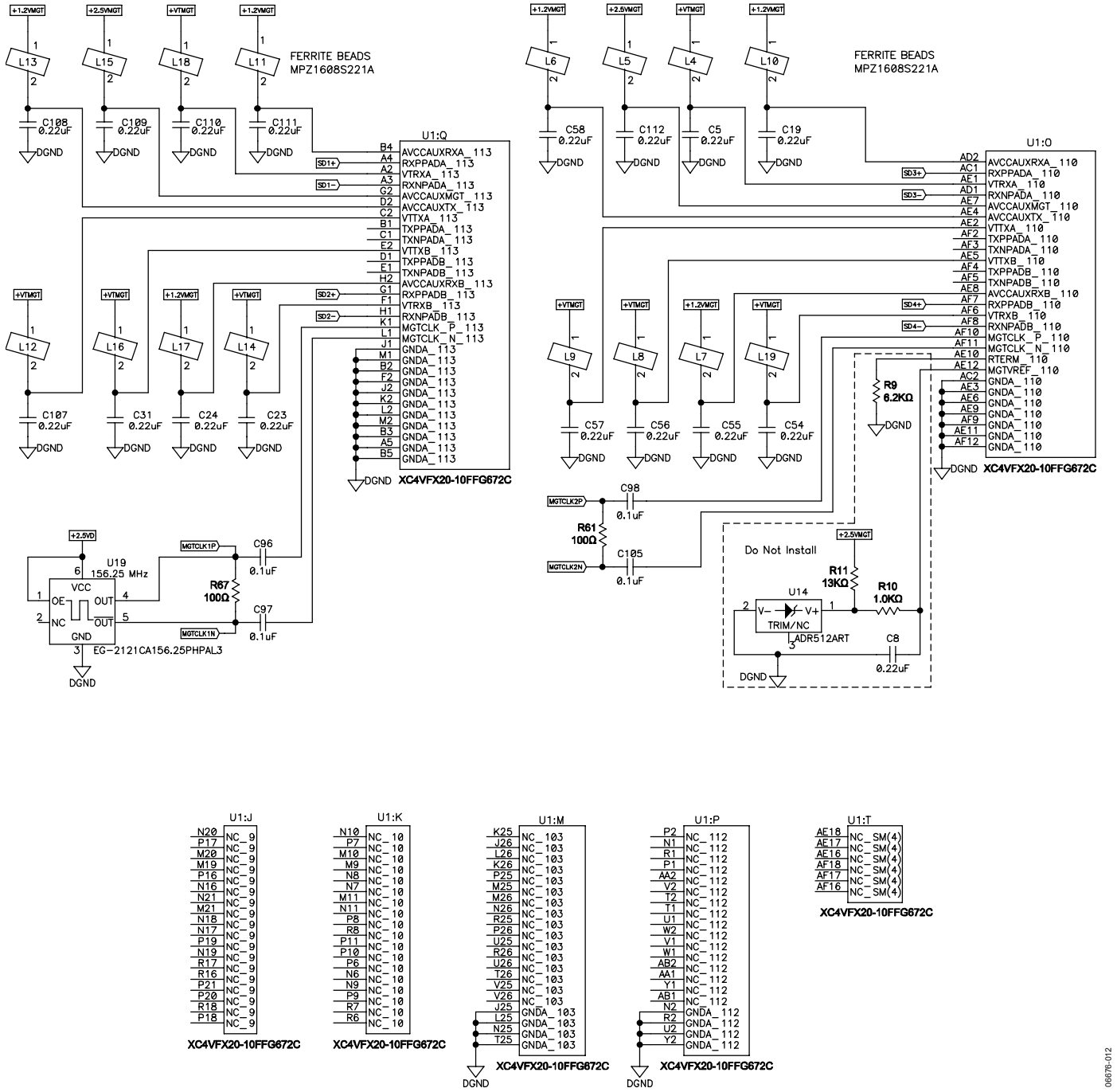


Figure 12.

USB CONNECTIONS

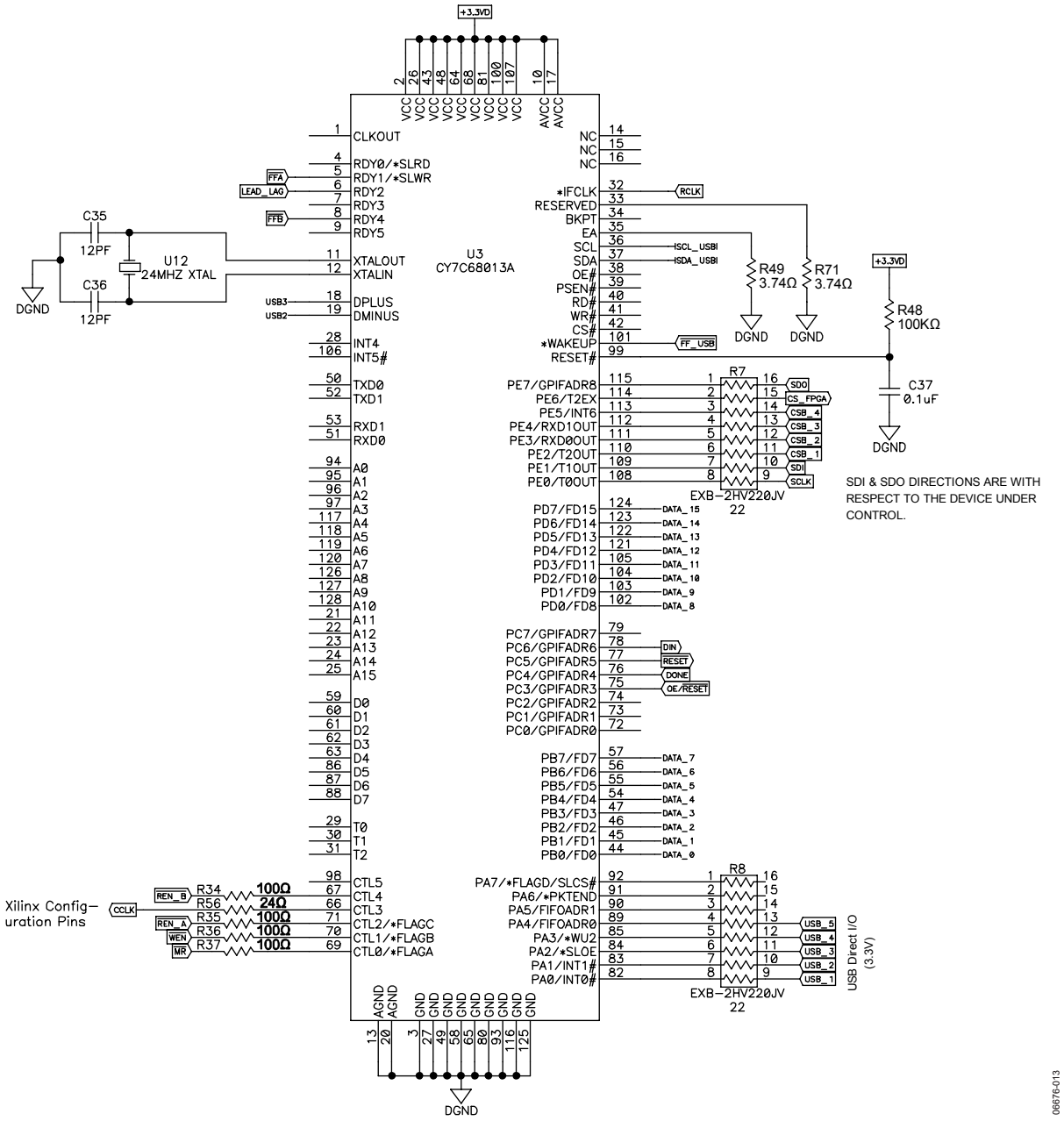
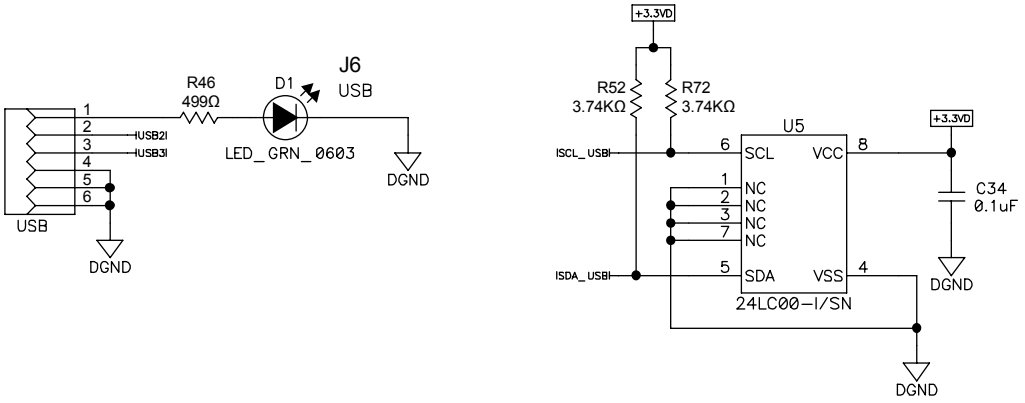
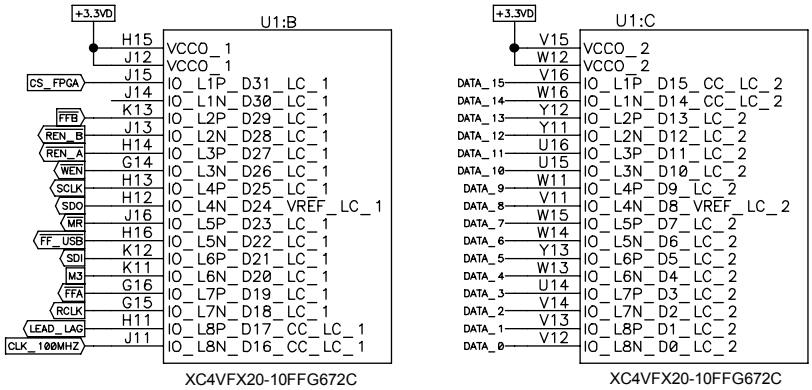


Figure 13.

USB CONNECTIONS (CONTINUED)





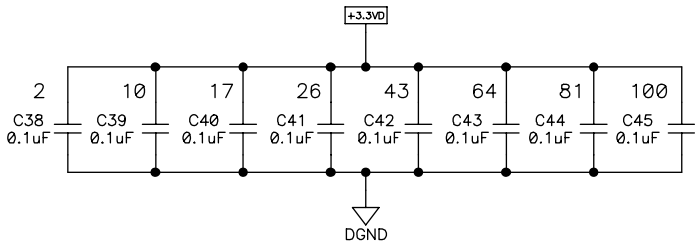


Figure 14.

EZ–KIT EXPANSION INTERFACE – FOR DSPs

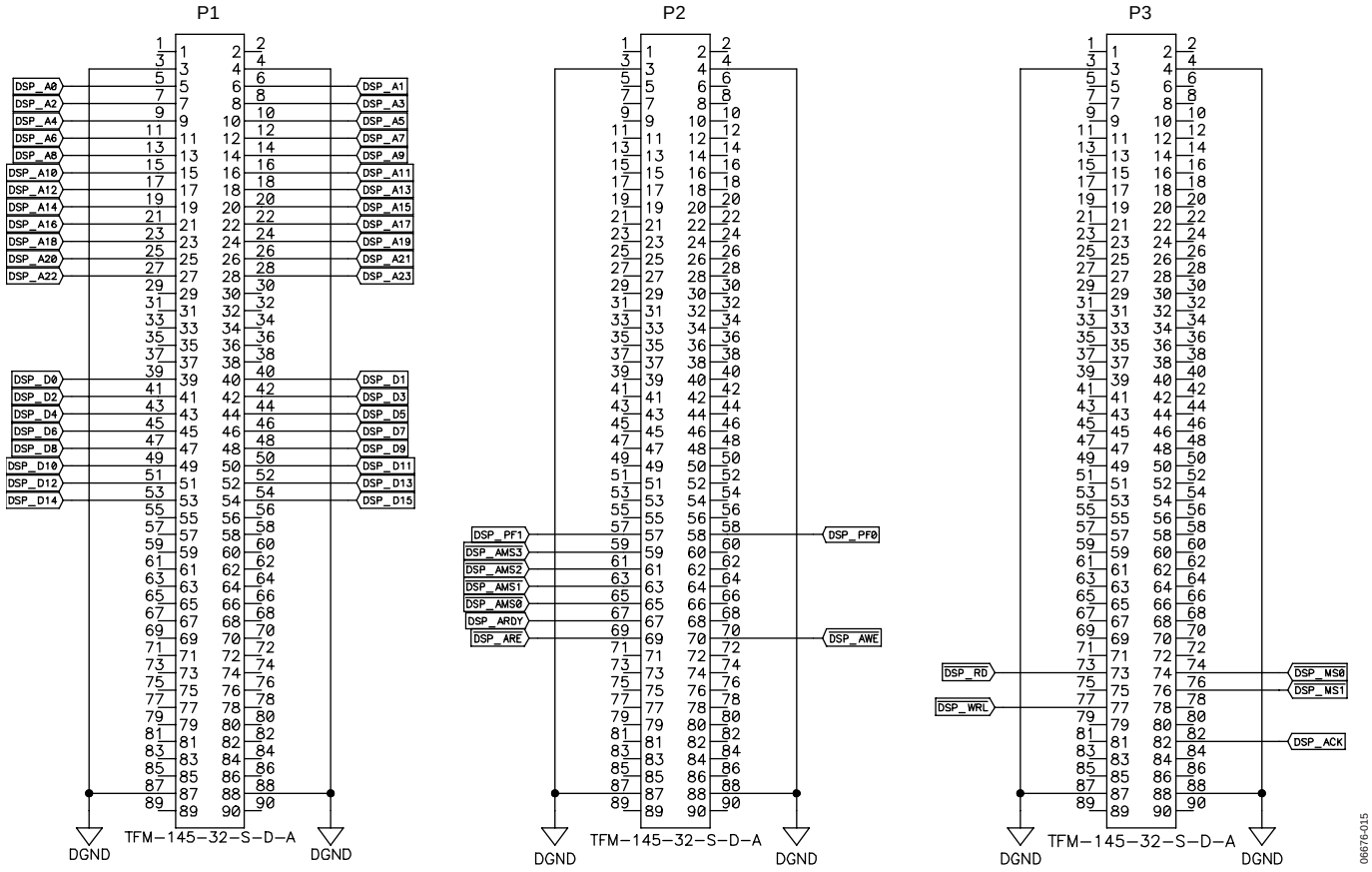


Figure 15.

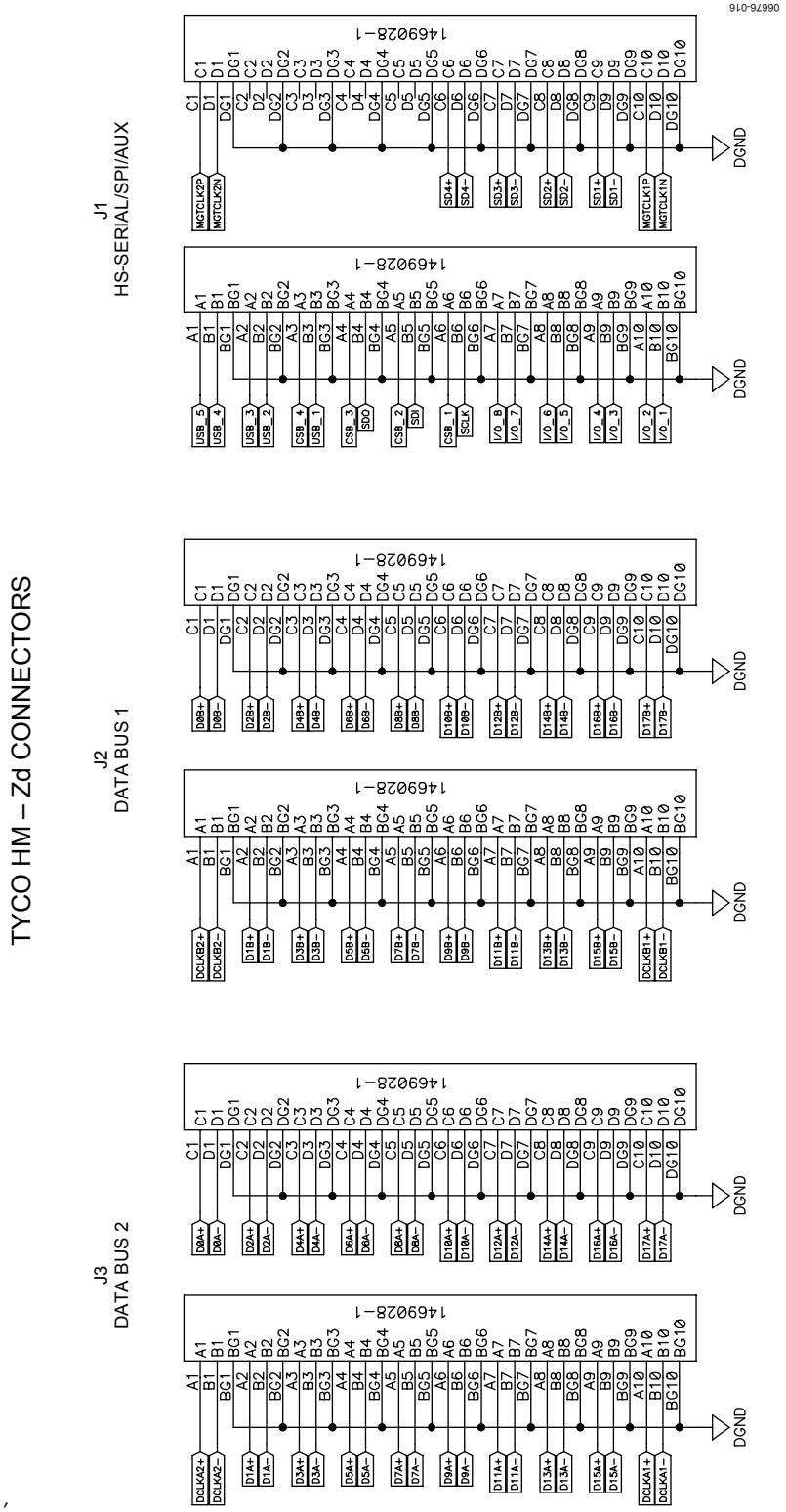
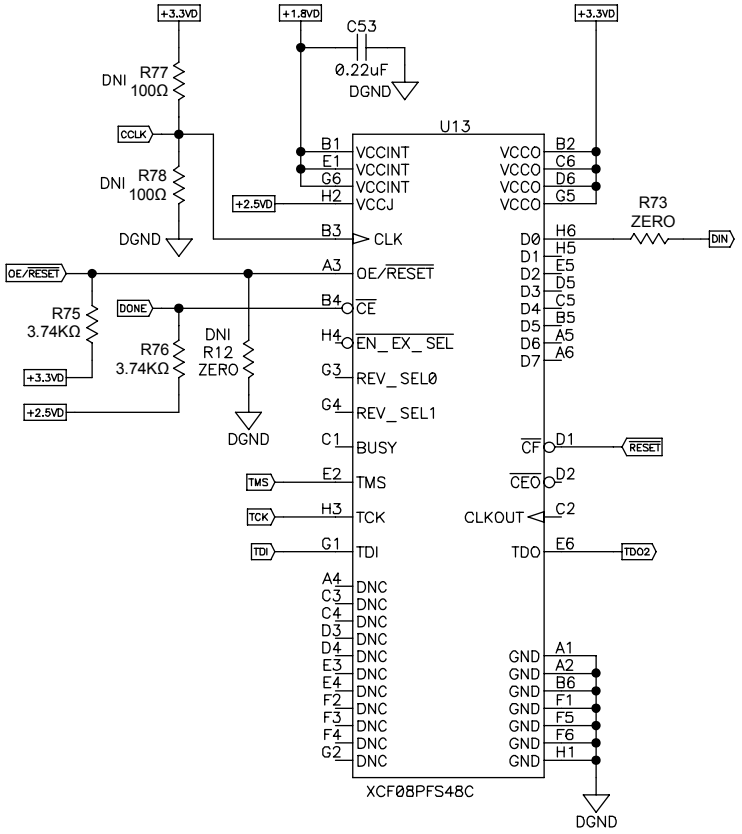
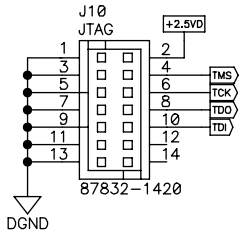


Figure 16.

CONFIGURATION EEPROM



JTAG CONNECTOR



EEPROM HARDWARE RECONFIGURATION PUSHBUTTON

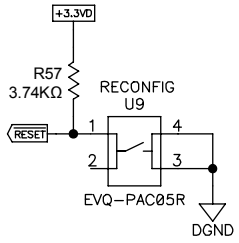


Figure 17.

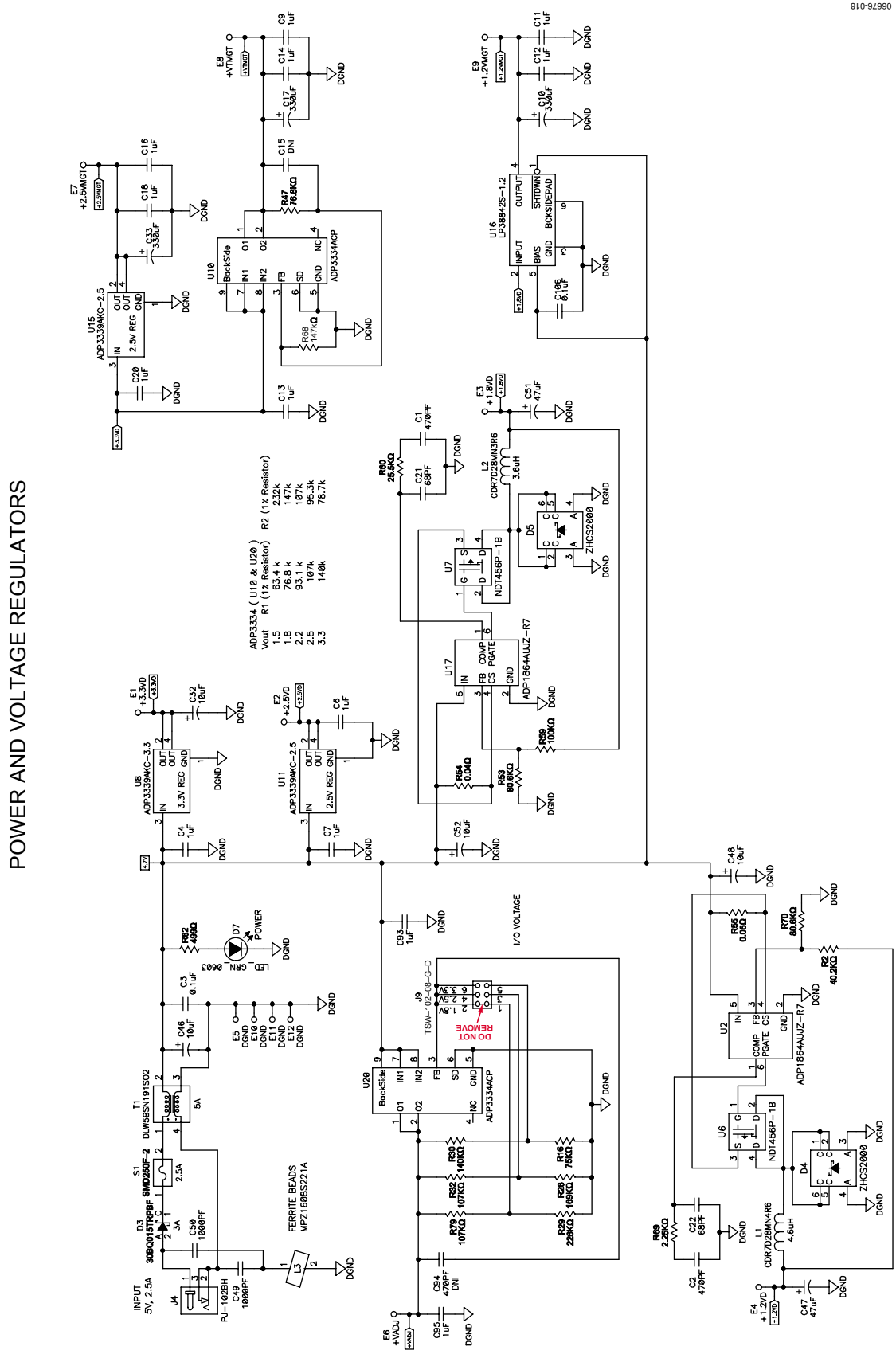


Figure 18.

PCB LAYOUT

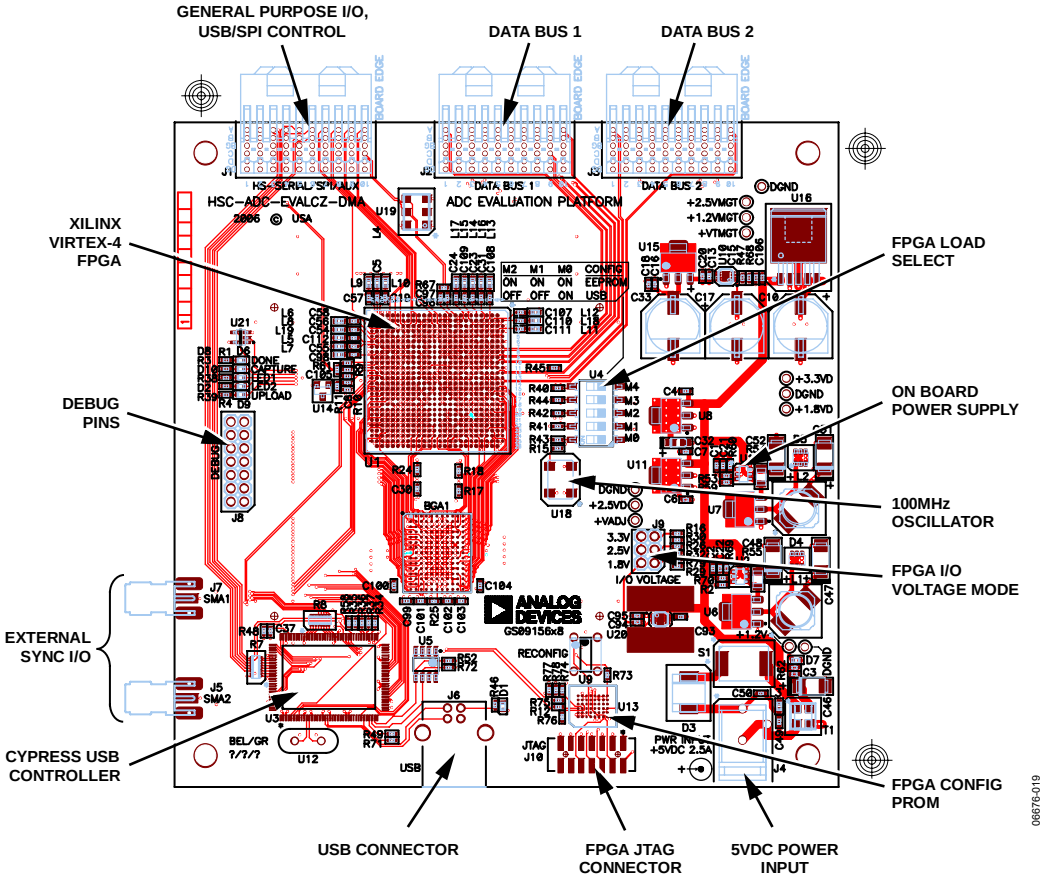


Figure 19. Top Silkscreen

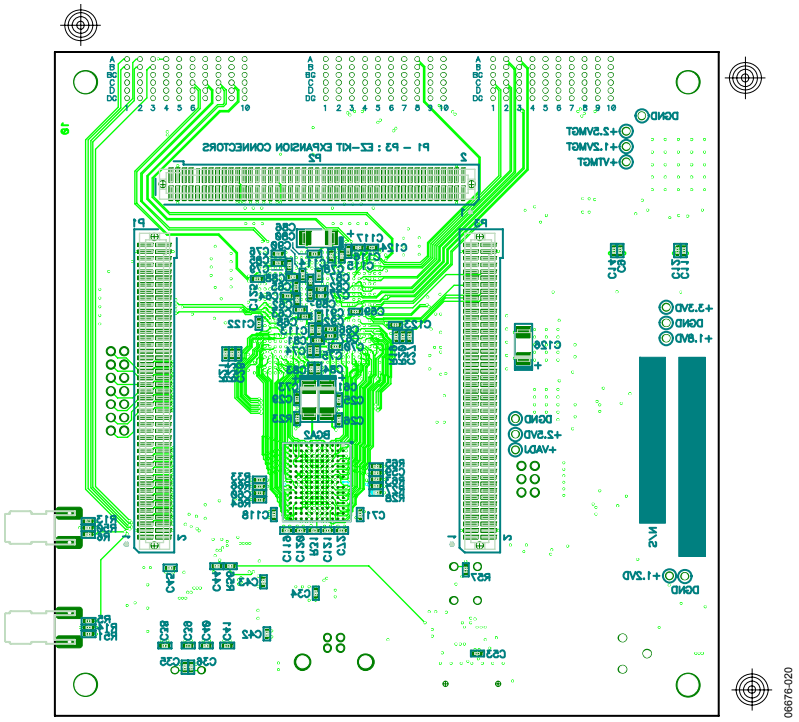


Figure 20. Bottom Silkscreen

I/O CONNECTOR—J1, J2, AND J3 PIN MAPPING

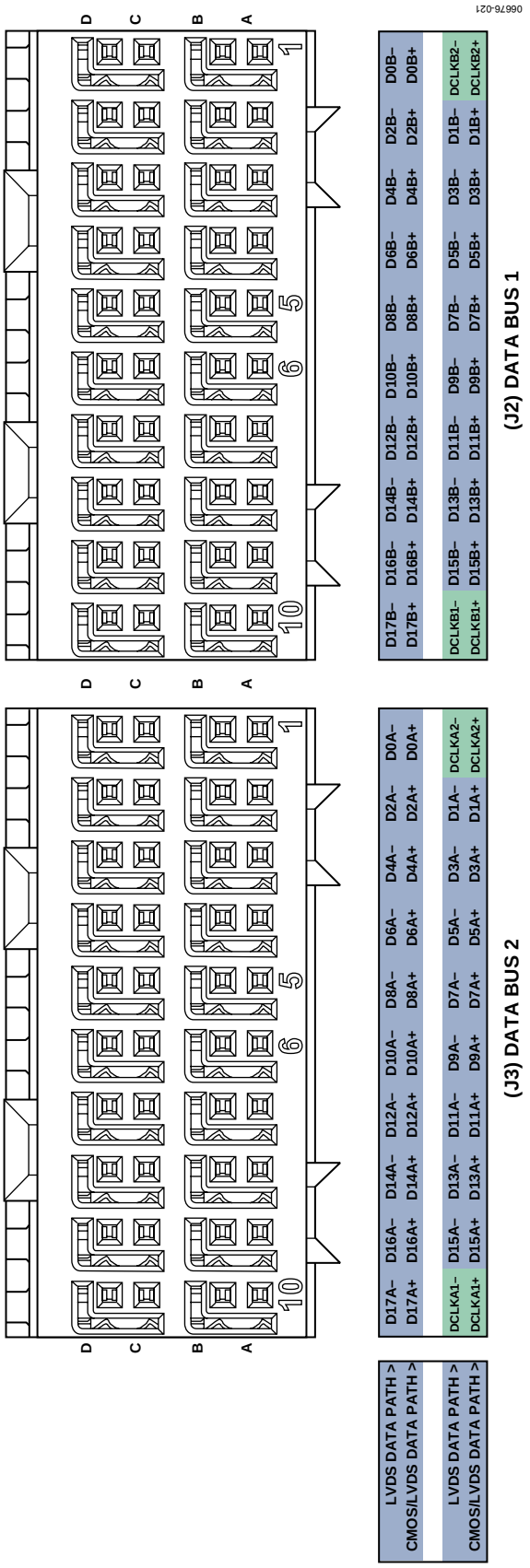


Figure 21. J2 and J3 Pin Mapping

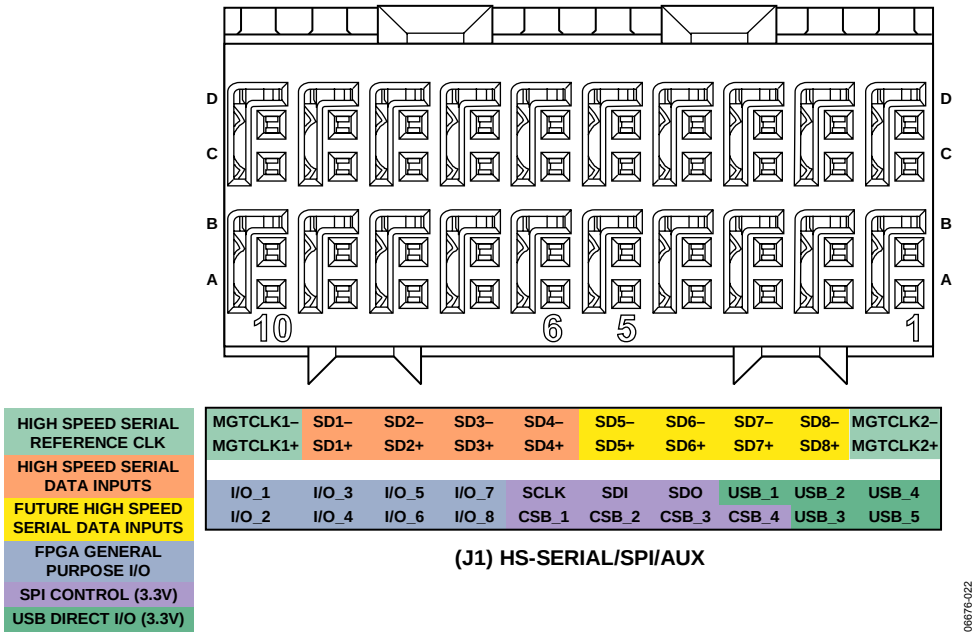


Figure 22. J1 Pin Mapping

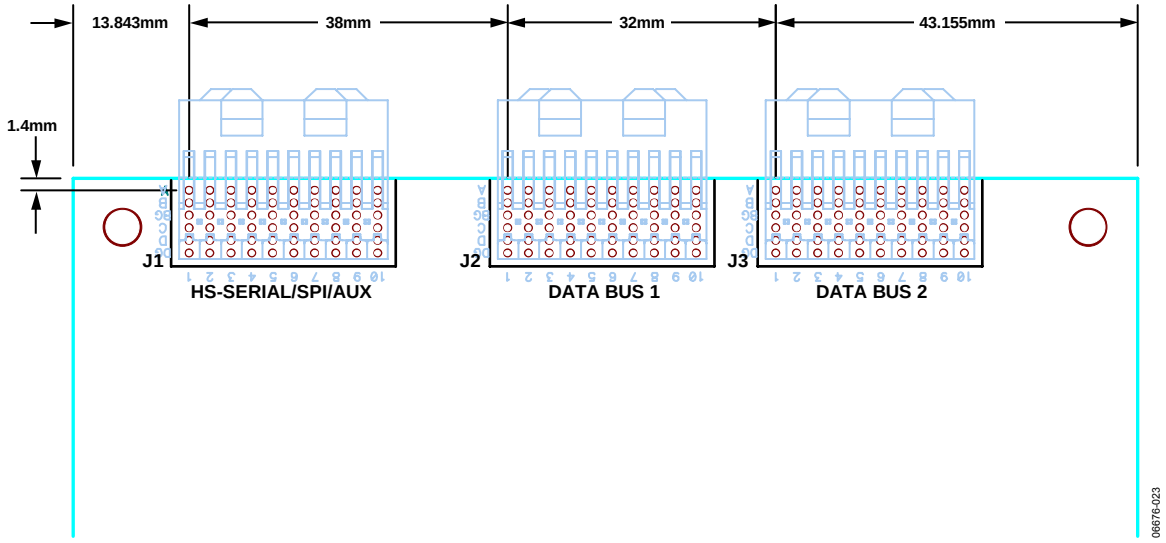


Figure 23. Data Converter I/O Connector Placement (Top View)

Table 3. HSC-ADC-EVALC J1 I/O Connections to FPGA (U1)

Connector J1 (HS-Serial, SPI, AUX)	Schematic Net Name	FPGA Pin
A1	USB_5	none
B1	USB_4	none
C1	MGTCLK2+	AF10
D1	MGTCLK2–	AF11
A2	USB_3	none
B2	USB_2	none
C2	none	none
D2	none	none
A3	CSB_4	none
B3	USB_1	none
C3	none	none
D3	none	none
A4	CSB_3	none
B4	SDO	H12
C4	none	none
D4	none	none
A5	CSB_2	none
B5	SDI	K12
C5	none	none
D5	none	none
A6	CSB_1	none
B6	SCLK	H13
C6	SD4+	AF7
D6	SD4–	AF8
A7	I/O_8	AD3
B7	I/O_7	AC3
C7	SD3+	AC1
D7	SD3–	AD1
A8	I/O_6	AA3
B8	I/O_5	Y3
C8	SD2+	G1
D8	SD2–	H1
A9	I/O_4	W3
B9	I/O_3	V3
C9	SD1+	A4
D9	SD1–	A3
A10	I/O_2	P3
B10	I/O_1	N3
C10	MGTCLK1+	K1
D10	MGTCLK1–	L1

Table 4. HSC-ADC-EVALC J2 I/O Connections to FPGA (U1)

Connector J2 (DATA BUS 1)	Schematic Net Name	FPGA Pin
A1	DCLKB2+	C13
B1	DCLKB2–	C12
C1	D0B+	T4
D1	D0B–	T3
A2	D1B+	M4
B2	D1B–	N4
C2	D2B+	P4
D2	D2B–	R3
A3	D3B+	M5
B3	D3B–	L5
C3	D4B+	L4
D3	D4B–	L3
A4	D5B+	K3
B4	D5B–	J3
C4	D6B+	L7
D4	D6B–	M6
A5	D7B+	J4
B5	D7B–	H3
C5	D8B+	K6
D5	D8B–	J5
A6	D9B+	G5
B6	D9B–	F4
C6	D10B+	H4
D6	D10B–	G4
A7	D11B+	H8
B7	D11B–	H7
C7	D12B+	G7
D7	D12B–	H6
A8	D13B+	F8
B8	D13B–	F7
C8	D14B+	K8
D8	D14B–	K7
A9	D15B+	B9
B9	D15B–	A9
C9	D16B+	A8
D9	D16B–	A7
A10	DCLKB1+	A12
B10	DCLKB1–	B12
C10	D17B+	B10
D10	D17B–	A10

Table 5. HSC-ADC-EVALC J3 I/O Connections to FPGA (U1)

Connector J3 (DATA BUS 2)	Schematic Net Name	FPGA Pin
A1	DCLKA2+	C14
B1	DCLKA2−	B14
C1	D0A+	D6
D1	D0A−	E6
A2	D1A+	H9
B2	D1A−	G9
C2	D2A+	E8
D2	D2A−	E7
A3	D3A+	L10
B3	D3A−	L9
C3	D4A+	J9
D3	D4A−	K10
A4	D5A+	C3
B4	D5A−	D3
C4	D6A+	E3
D4	D6A−	F3
A5	D7A+	D5
B5	D7A−	E5
C5	D8A+	C4
D5	D8A−	D4
A6	D9A+	B7
B6	D9A−	C7
C6	D10A+	B6
D6	D10A−	C6
A7	D11A+	D9
B7	D11A−	C9
C7	D12A+	D8
D7	D12A−	C8
A8	D13A+	C11
B8	D13A−	B11
C8	D14A+	E10
D8	D14A−	D10
A9	D15A+	G10
B9	D15A−	F10
C9	D16A+	E11
D9	D16A−	D11
A10	DCLKA1+	A14
B10	DCLKA1−	A13
C10	D17A+	G12
D10	D17A−	G11

ORDERING INFORMATION

BILL OF MATERIALS (RoHS COMPLIANT)

Table 6.

Qty	Reference Designator	Description	Manufacturer	Part Number
1	PCB	PCB, ADC evaluation platform	MOOG/PCSM	GS09156x8
0	BGA1, BGA2	IC, 18-bit DDRII SRAM 2-word burst operation (MOS integrated circuit), do not install	NEC	PD44164362F5-EQ1
2	C1, C2	Capacitor, 470 pF, 50 V ceramic X7R 0402	Panasonic/ECG	ECJ-0EB1H471K
3	C10, C17, C33	Capacitor, 330 µF, 10 V TG SMD	Panasonic/ECG	EEETG1A331P
2	C21, C22	Capacitor, 68 pF, 50 V, ceramic 0402 SMD	Panasonic/ECG	ECU-E1H680JCQ
67	C3, C25 to C30, C34, C37 to C45, C59, C60, C63 to C72, C74 to C76, C78 to C85, C88 to C92, C96 to C98, C100 to C106, C113 to C118, C120 to C125	Capacitor, 0.1 µF, 10 V, ceramic X5R 0402	Panasonic/ECG	ECJ-0EB1A104K
1	C32	Capacitor, 10 µF, 6.3 V, tantalum TE series	Kemet	T491A106M006AT
2	C35, C36	Capacitor, 12 pF, 50 V, ceramic 0402 SMD	Panasonic/ECG	ECJ-0EC1H120J
18	C4, C6, C7, C9, C11 to C14, C16, C18, C20, C62, C77, C87, C93, C95, C99, C119	Capacitor, 0402 chip, X5R, 6.3 V, 1 µF, ± 20%	Panasonic	ECJ-0EB0J105M
7	C46, C48, C52, C61, C73, C86, C126	Capacitor, 10 µF, 20 V, tantalum TEL SMD	AVX	TPSC106K025R0500
2	C47, C51	Capacitor, 47 µF, 10 V, tantalum TEL SMD	Epcos, Inc.	B45197A2476K309
2	C49, C50	Capacitor, 1000 pF, 50 V, ceramic Y5V 0402	Panasonic/ECG	ECJ-0EF1H102Z
17	C5, C19, C23, C24, C31, C53 to C58, C107 to C112	Capacitor, 0402 chip, X5R, 6.3 V, 0.22 µF, ±10%	Panasonic	ECJ-0EB0J224K
1	C94	Capacitor, 470 pF, 25 V, ceramic 0402 SMD	Panasonic/ECG	ECJ-0EB1E471K
7	D1, D2, D6 to D10	LED green, clear lens SMD	Panasonic	LNJ308G8TRA
1	D3	PolySwitch surface-mount (PTC devices)	International IRF Rectifiers	30BQ015TRPBF
2	D4, D5	40 V silicon high current Schottky barrier diode	Zetex Semiconductors	ZHCS2000
1	J1, J2, J3	Connector, 2-pair 10 column high speed HM-Zd PCB mount	Tyco	6469028-1
1	J10	Connector, 2 mm, 2 × 7 pin SMT vertical male, with shroud	Molex	87832-1420-TB32
1	J4	Connector, DC power jack	CUI Inc.	PJ-102AH
1	J6	Connector, USB Type B	Mill-Max	897-43-004-90-000000
2	J5,J7	Connector, end launch jack/PCB, 62 mil, gold	Emerson	142-0701-801
1	J8	Connector, 25 mil square postheader, 100 mil, 2 × 7	Samtec, Inc.	TSW-107-08-G-D
1	J9 (2.5 V and 3.3 V)	Connector, 2 × 2 header, 100 mil	Samtec, Inc.	TSW-102-08-G-D
1	J9 (Jumper Pin 1 to Jumper Pin 2)	Solder wire jumper (Pin 1 indicator to 1.8 V on silkscreen)		
1	L1	Inductor, 4.6 µH SMD, Code 0004	Sumida	CDR7D28MN4R6
1	L2	Inductor, 3.6 µH SMD, Code 0003	Sumida	CDR7D28MN3R6

Qty	Reference Designator	Description	Manufacturer	Part Number
17	L3 to L19	Ferrite chip, 220 Ω, 2 A, 0603, 100 MHz	TDK	MPZ1608S221A
3	P1 to P3	Connector, 0.050 in × 0.050 in, Samtec TFM series, 2R	Samtec, Inc.	TFM-145-32-S-D-A
13	R1, R3, R4, R34 to R39, R61, R67, R77, R78	Resistor, 100 Ω, 1/16 W, 1%, 0402 SMD	Panasonic/ECG	ERJ-2RKF1000X
3	R15, R56, R74	Resistor, 24 Ω, 1/16 W, 5%, 0402 SMD	Panasonic/ECG	ERJ-2GEJ240X
1	R16	Resistor, 75 kΩ, 1/16 W, 1%, 0402 SMD	Panasonic/ECG	ERJ-2RKF7502X
5	R17, R18, R23, R24, R50	Resistor, 51.1 Ω, 1/16 W, 1%, 0402 SMD	Panasonic/ECG	ERJ-2RKF51R1X
10	R19 to R22, R46, R62 to R66	Resistor, 499 Ω, 1/16 W, 1%, 0402 SMD	Panasonic/ECG	ERJ-2RKF4990X
1	R2	Resistor, 40.2 kΩ, 1/16 W, 1%, 0402 SMD	Panasonic/ECG	ERJ-2RKF4022X
17	R25, R28, R31, R40 to R45, R49, R52, R57, R58, R71, R72, R75, R76	Resistor, 3.74 kΩ, 1/16 W, 1%, 0402 SMD	Panasonic/ECG	ERJ-2RKF3741X
1	R26	Resistor, 169 kΩ, 1/16 W, 1%, 0402 SMD	Panasonic/ECG	ERJ-2RKF1693X
2	R27, R33	Resistor, 249 Ω, 1/16 W, 1%, 0402 SMD	Panasonic/ECG	ERJ-2RKF2490X
1	R68	Resistor, 147 kΩ, 1/16 W, 1%, 0402 SMD	Panasonic/ECG	ERJ-2RKF1473X
1	R29	Resistor, 226 kΩ, 1/16 W, 1%, 0402 SMD	Panasonic/ECG	ERJ-2RKF2263X
0	R30	Resistor, 140 kΩ, 1/16 W, 1%, 0402 SMD, do not install	Panasonic/ECG	ERJ-2RKF1403X
1	(R32), R79	Resistor, 107 kΩ, 1/16 W, 1%, 0402 SMD, do not install R32	Panasonic/ECG	ERJ-2RKF1073X
1	R47	Resistor, 76.8 kΩ, 1/16 W, 1%, 0402 SMD	Panasonic/ECG	ERJ-2RKF7682X
2	R48, R59	Resistor, 100 kΩ, 1/16 W, 1%, 0402 SMD	Panasonic/ECG	ERJ-2RKF1003X
3	R5, R6, R73	Resistor 0 Ω, 1/16 W, 5%, 0402 SMD	Panasonic/ECG	ERJ-2GE0R00X
2	R53, R70	Resistor 80.6 kΩ, 1/16 W, 1%, 0402 SMD	Panasonic/ECG	ERJ-2RKF8062X
1	R54	Resistor, low value, 1206 SMD, 0.04 Ω	TT Electronics	LRC-LR1206LF-01-R040-F
1	R55	Resistor, low value, 1206 SMD, 0.06 Ω	TT Electronics	LRC-LR1206LF-01-R060-F
2	R60, R69	Resistor, 25.5K Ω, 1/16 W, 1%, 0402 SMD	Panasonic/ECG	ERJ-2RKF2552X
2	R7, R8	Resistor array network, 8 Ω to 22 Ω chip	Panasonic	EXB-2HV220JV
1	S1	Fuse, PolySwitch SMT (PTC devices)	Tyco	SMD250F-2
1	T1	Choke, common-mode coils, wire-wound type for large current DLW5AH/DLW5BS series (2014/2020 Size)	Murata	DLW5BSN191SQ2
1	U1	Virtex-4 FPGA	Xilinx	XC4VFX20-10FFG672C
2	U10, U20	Voltage regulator, high accuracy, low IQ, adjustable	Analog Devices	ADP3334ACPZ-REEL7
2	U11, U15	Voltage regulator, high accuracy ultralow IQ, 1.5 A	Analog Devices	ADP3339AKCZ-2.5R7
1	U12	Crystal oscillator, 24 Mhz, 12 pF, SMD	ECS	ECS-240-12-4X
1	U13	1.8 V, 8 Mb, platform flash-in system	Xilinx	XCF08PFSG48C
1	U16	Voltage regulator, 1.5 A ultralow dropout linear regulator	National Semiconductor	LP38842S-1.2
1	U18	Crystal controlled oscillator (100 MHz fixed frequency oscillator)	Connor-Winfield Corp.	CWX823-100.0M
0	U19	156.25 MHz low jitter saw crystal oscillator, do not install	Epson Electronics America	EG-2121CA 156.2500M-PHPAL3
2	U2, U17	IC, constant frequency current-mode, step-down, dc-to-dc controller in TSOT	Analog Devices	ADP1864AUJZ-R7
1	U21	IC, single inverter buffer/driver with open-drain output	Fairchild Semiconductor	NC7SZ05M5X
1	U3	IC, EZ-USB FX2LP USB microcontroller	Cypress Semiconductor Corp.	CY7C68013A-128AXC
1	U4	Switch, 5-position, SMT, DIP	CTS	219-5MST
1	U5	IC, 128-bit I^2C bus serial EEPROM	Microchip	24LC00-I/SN

Qty	Reference Designator	Description	Manufacturer	Part Number
2	U6, U7	IC, P-channel enhancement mode field effect transistor	Fairchild Semiconductor	NDT456P
1	U8	Voltage regulator, high accuracy ultralow IQ, 1.5 A	Analog Devices	ADP3339AKCZ-3.3
1	U9	Switch, 6 mm light touch SW, N.O.	Alps	SKHHAKA010
4	H1, H2, H3, H4	Circuit board support on base	Richco, Inc.	CBSB-14-01
1	Packed with PCB	Transformer 5 V, 3 A switcher P5	CUI, Inc.	DPS050300U-P5P-TK
0	U14	1.2 V precision low noise shunt voltage references, SOT-23 (RT-3), do not install	Analog Devices	ADR512ART
0	R9	Resistor, 6.2 kΩ, 1/16 W, 5%, 0402 SMD, do not install	Panasonic/ECG	ERJ-2GEJ622X
0	R12, R13, R14, R51	Resistor, 0 Ω, 1/16 W, 5%, 0402 SMD, do not install	Panasonic/ECG	ERJ-2GE0R00X
0	R11	Resistor 13 k Ω, 1/16 W, 5%, 0402 SMD, do not install	Panasonic/ECG	ERJ-2GEJ133X
0	R10	Resistor 1.0 kΩ, 1/16 W, 5%, 0402 SMD, do not install	Panasonic/ECG	ERJ-2GEJ102X
0	C8	Capacitor, 0402 SMD, X5R, 6.3 V, 0.22 µF, ±10%, do not install	Panasonic	ECJ-0EB0J224K
0	C15	0402 chip capacitor, X5R, 6.3 V, 1 µF, ±20%, do not install	Panasonic	ECJ-0EB0J105M

ORDERING GUIDE

Model	Description
HSC-ADC-EVALC	Data Converter Evaluation Platform
HSC-ADC-EVALCZ[1]	Data Converter Evaluation Platform

[1]Z = RoHS Compliant Part.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

NOTES

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