ADVANCE

**CY14E102L, CY14E102N**

# 2-Mbit (256K x 8/128K x 16) nvSRAM

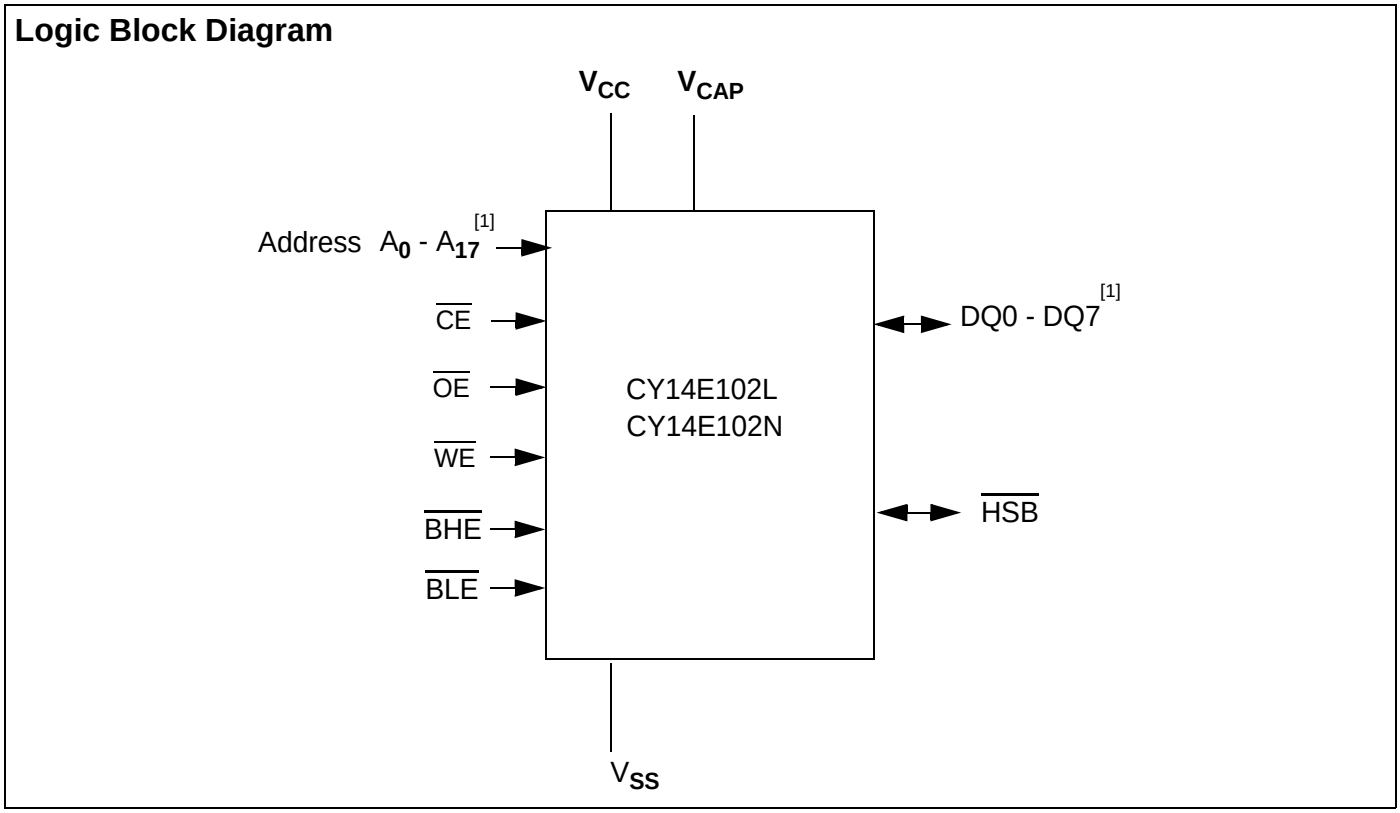
## Features

- 15 ns, 20 ns, 25 ns, and 45 ns access times
- Internally organized as 256K x 8 (CY14E102L) or 128K x 16 (CY14E102N)
- Hands off automatic STORE on power down with only a small capacitor
- STORE to QuantumTrap™ nonvolatile elements initiated by software, device pin, or AutoStore™ on power down
- RECALL to SRAM initiated by software or power up
- Infinite read, write, and recall cycles
- 200,000 STORE cycles to QuantumTrap
- 20 year data retention
- Single 5V ±10% operation
- Commercial and Industrial temperatures
- 48-pin FBGA, 44 and 54-pin TSOP II packages
- Pb-free and RoHS compliance

## Functional Description

The Cypress CY14E102L/CY14E102N is a fast static RAM, with a nonvolatile element in each memory cell. The memory is organized as 256K words of 8 bits each or 128K words of 16 bits each. The embedded nonvolatile elements incorporate QuantumTrap technology, producing the world's most reliable nonvolatile memory. The SRAM provides infinite read and write cycles, while independent nonvolatile data reside in the highly reliable QuantumTrap cell. Data transfers from the SRAM to the nonvolatile elements (the STORE operation) takes place automatically at power down. On power up, data is restored to the SRAM (the RECALL operation) from the nonvolatile memory. Both the STORE and RECALL operations are also available under software control.

## Logic Block Diagram




**Note**

1. Address $A_0$ - $A_{17}$ and Data DQ0 - DQ7 for x8 configuration, Address $A_0$ - $A_{16}$ and Data DQ0 - DQ15 for x16 configuration.

## Pinouts

**Figure 1. Pin Diagram - 48 FBGA (Top View)**

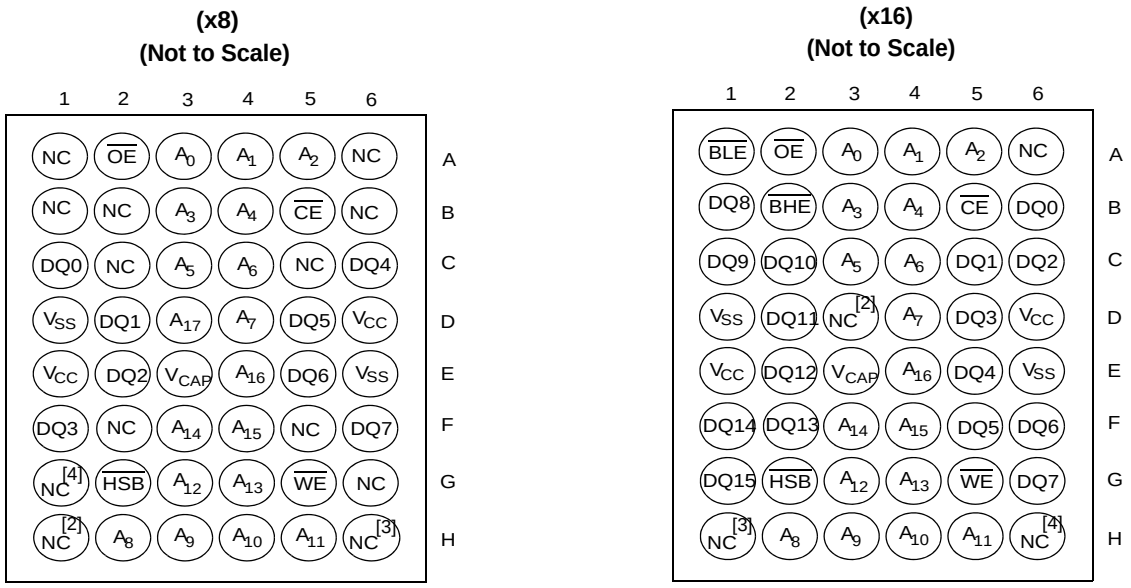
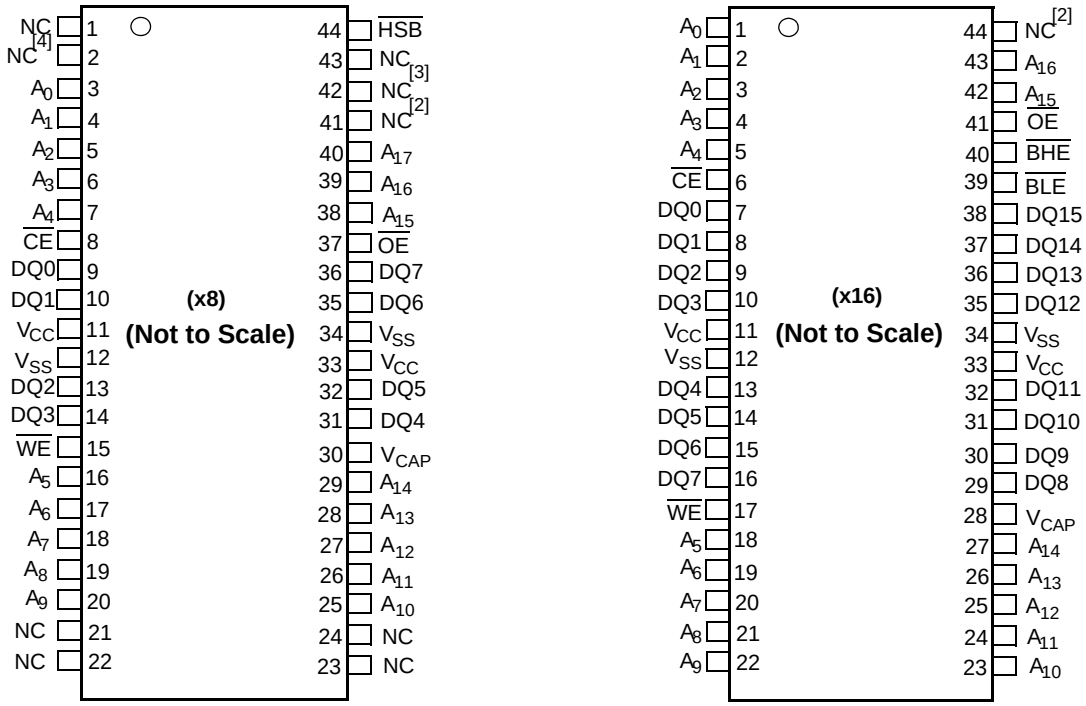


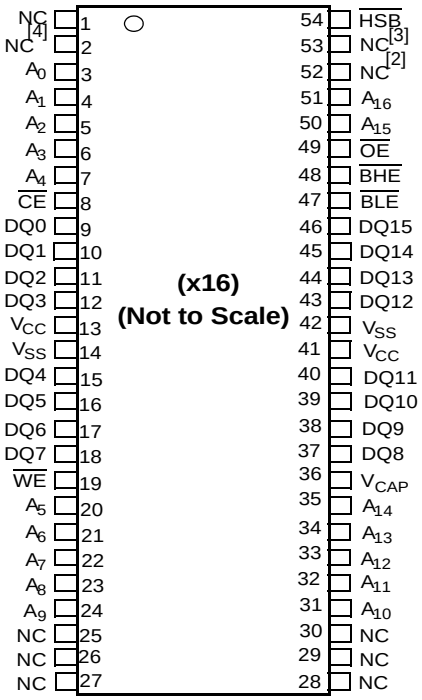

**Figure 2. Pin Diagram - 44 TSOP II (Top View)**




**Notes**
2. Address expansion for 4 Mbit. NC pin not connected to die.
3. Address expansion for 8 Mbit. NC pin not connected to die.
4. Address expansion for 16 Mbit. NC pin not connected to die.

## Pinouts (continued)

**Figure 3. Pin Diagram - 54 TSOP II (Top View)**




## Pin Definitions

| Pin Name | IO Type | Description |
|---|---|---|
| $A_0 – A_{17}$ | Input | **Address Inputs.** Used to select one of the 262, 144 bytes of the nvSRAM for x8 Configuration. |
| $A_0 – A_{16}$ | | **Address Inputs.** Used to select one of the 131, 072 bytes of the nvSRAM for x16 Configuration. |
| DQ0 – DQ7 | Input/Output | **Bidirectional Data IO Lines for x8 Configuration**. Used as input or output lines depending on operation. |
| DQ0 – DQ15 | | **Bidirectional Data IO Lines for x16 Configuration**. Used as input or output lines depending on operation. |
| $\overline{WE}$ | Input | **Write Enable Input, Active LOW**. When selected LOW, data on the IO pins is written to the address location latched by the falling edge of $\overline{CE}$. |
| $\overline{CE}$ | Input | **Chip Enable Input, Active LOW**. When LOW, selects the chip. When HIGH, deselects the chip. |
| $\overline{OE}$ | Input | **Output Enable, Active LOW**. The active LOW $\overline{OE}$ input enables the data output buffers during read cycles. IO pins are tri-stated on deasserting $\overline{OE}$ high. |
| $\overline{BHE}$ | Input | **Byte High Enable, Active LOW.** Controls DQ15 - DQ8. |
| $\overline{BLE}$ | Input | **Byte Low Enable, Active LOW.** Controls DQ7 - DQ0. |
| $V_{SS}$ | Ground | **Ground for the Device.** Must be connected to the ground of the system. |
| $V_{CC}$ | Power Supply | **Power Supply Inputs to the Device**. |
| $\overline{HSB}$ | Input/Output | **Hardware Store Busy ($\overline{HSB}$)**. When LOW this output indicates that a hardware store is in progress. When pulled LOW external to the chip it initiates a nonvolatile STORE operation. A weak internal pull up resistor keeps this pin HIGH if not connected (connection is optional). |
| $V_{CAP}$ | Power Supply | **AutoStore Capacitor**. Supplies power to the nvSRAM during power loss to store data from the SRAM to nonvolatile elements. |
| NC | No Connect | **No Connect**. Do not connect this pin to the die. |

## Device Operation

The CY14E102L/CY14E102N nvSRAM is made up of two functional components paired in the same physical cell. They are an SRAM memory cell and a nonvolatile QuantumTrap cell. The SRAM memory cell operates as a standard fast static RAM. Data in the SRAM is transferred to the nonvolatile cell (the STORE operation), or from the nonvolatile cell to the SRAM (the RECALL operation). Using this unique architecture all cells are stored and recalled in parallel. During the STORE and RECALL operations SRAM read and write operations are inhibited. The CY14E102L/CY14E102N supports infinite reads and writes similar to a typical SRAM. In addition, it provides infinite RECALL operations from the nonvolatile cells and up to 200K STORE operations.

## SRAM Read

The CY14E102L/CY14E102N performs a READ cycle when $\overline{CE}$ and $\overline{OE}$ are LOW, and $\overline{WE}$ and $\overline{HSB}$ are HIGH. The address specified on pins $A_{0-17}$ or $A_{0-16}$ determines which of the 262, 144 data bytes or 131, 072 words of 16 bits each is accessed. When the read is initiated by an address transition, the outputs are valid after a delay of $t_{AA}$. If the read is initiated by $\overline{CE}$ or $\overline{OE}$, the outputs are valid at $t_{ACE}$ or at $t_{DOE}$, whichever is later. The data outputs repeatedly respond to address changes within the $t_{AA}$ access time without the need for transitions on any control input pins. This remains valid until another address change or until $\overline{CE}$ or $\overline{OE}$ is brought HIGH, or $\overline{WE}$ or $\overline{HSB}$ is brought LOW.

## SRAM Write

A WRITE cycle is performed whenever $\overline{CE}$ and $\overline{WE}$ are LOW and $\overline{HSB}$ is HIGH. The address inputs must be stable before entering the WRITE cycle and must remain stable until either $\overline{CE}$ or $\overline{WE}$ goes high at the end of the cycle. The data on the common IO pins $DQ_{0–15}$ are written into the memory if the data is valid $t_{SD}$ before the end of a $\overline{WE}$ controlled WRITE or before the end of an $\overline{CE}$ controlled WRITE. It is recommended that $\overline{OE}$ be kept HIGH during the entire WRITE cycle to avoid data bus contention on common IO lines. If $\overline{OE}$ is left LOW, internal circuitry turns off the output buffers $t_{HZWE}$ after $\overline{WE}$ goes LOW.

## AutoStore Operation

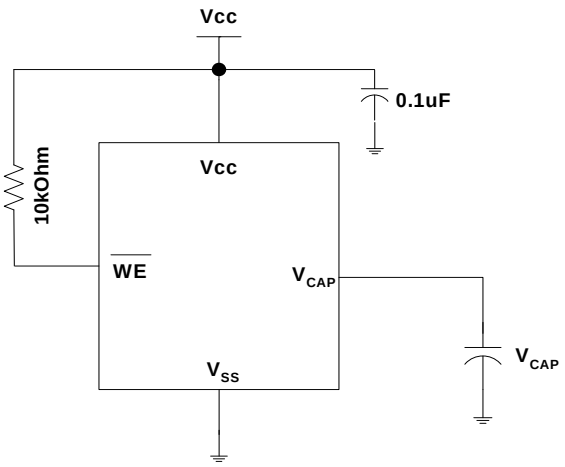
The CY14E102L/CY14E102N stores data to the nvSRAM using one of the following three storage operations: Hardware Store activated by $\overline{HSB}$, Software Store activated by an address sequence, and AutoStore on device power down. The AutoStore operation is a unique feature of QuantumTrap technology and is enabled by default on the CY14E102L/CY14E102N.

During a normal operation, the device draws current from $V_{CC}$ to charge a capacitor connected to the $V_{CAP}$ pin. This stored charge is used by the chip to perform a single STORE operation. If the voltage on the $V_{CC}$ pin drops below $V_{SWITCH}$, the part automatically disconnects the $V_{CAP}$ pin from $V_{CC}$. A STORE operation is initiated with power provided by the $V_{CAP}$ capacitor.

Figure 4 shows the proper connection of the storage capacitor ($V_{CAP}$) for automatic store operation. Refer to the section DC Electrical Characteristics on page 7 for the size of $V_{CAP}$ .

To reduce unnecessary nonvolatile stores, AutoStore and Hardware Store operations are ignored unless at least one WRITE operation has taken place since the most recent STORE or RECALL cycle. Software initiated STORE cycles are performed regardless of whether a WRITE operation has taken place. Monitor the $\overline{HSB}$ signal by the system to detect if an AutoStore cycle is in progress.

**Figure 4. AutoStore Mode**




## Hardware STORE Operation

The CY14E102L/CY14E102N provides the $\overline{HSB}$ pin for controlling and acknowledging the STORE operations. Use the $\overline{HSB}$ pin to request a hardware STORE cycle. When the $\overline{HSB}$ pin is driven LOW, the CY14E102L/CY14E102N conditionally initiates a STORE operation after $t_{DELAY}$. An actual STORE cycle only begins if a WRITE to the SRAM took place since the last STORE or RECALL cycle. The $\overline{HSB}$ pin also acts as an open drain driver that is internally driven LOW to indicate a busy condition while the STORE (initiated by any means) is in progress.

SRAM READ and WRITE operations that are in progress when $\overline{HSB}$ is driven LOW by any means are given time to complete before the STORE operation is initiated. After $\overline{HSB}$ goes LOW, the CY14E102LL/CY14E102N continues SRAM operations for $t_{DELAY}$. During $t_{DELAY}$, multiple SRAM READ operations may take place. If a WRITE is in progress when $\overline{HSB}$ is pulled low it is allowed a time, $t_{DELAY}$ to complete. However, any SRAM WRITE cycles requested after $\overline{HSB}$ goes LOW is inhibited until $\overline{HSB}$ returns HIGH.

During any STORE operation, regardless of how it was initiated, the CY14E102L/CY14E102N continues to drive the $\overline{HSB}$ pin LOW, releasing it only when the STORE is complete. Upon completion of the STORE operation, the CY14E102L/CY14E102N remains disabled until the $\overline{HSB}$ pin returns HIGH. Leave the $\overline{HSB}$ unconnected if it is not used.

## Hardware RECALL (Power Up)

During power up or after any low power condition ($V_{CC}$< $V_{SWITCH}$), an internal RECALL request is latched. When $V_{CC}$ again exceeds the sense voltage of $V_{SWITCH}$, a RECALL cycle is automatically initiated and takes $t_{HRECALL}$ to complete.

## Software STORE

Transfer data from the SRAM to the nonvolatile memory with a software address sequence. The CY14E102L/CY14E102N software STORE cycle is initiated by executing sequential CE-controlled READ cycles from six specific address locations in exact order. During the STORE cycle an erase of the previous nonvolatile data is first performed, followed by a program of the nonvolatile elements. After a STORE cycle is initiated, further input and output are disabled until the cycle is completed.

Because a sequence of READs from specific addresses is used for STORE initiation, it is important that no other READ or WRITE accesses intervene in the sequence. If there are intervening READ or WRITE accesses, the sequence is aborted and no STORE or RECALL takes place.

To initiate the software STORE cycle, the following READ sequence must be performed.

1. Read Address 0x4E38 Valid READ
2. Read Address 0xB1C7 Valid READ
3. Read Address 0x83E0 Valid READ
4. Read Address 0x7C1F Valid READ
5. Read Address 0x703F Valid READ
6. Read Address 0x8FC0 Initiate STORE Cycle

The software sequence may be clocked with $\overline{CE}$ controlled READs or $\overline{OE}$ controlled READs. After the sixth address in the sequence is entered, the STORE cycle commences and the chip is disabled. It is important to use READ cycles and not WRITE cycles in the sequence, although it is not necessary that $\overline{OE}$ be LOW for a valid sequence. After the $t_{STORE}$ cycle time is fulfilled, the SRAM is activated again for the READ and WRITE operation.

## Software RECALL

Transfer the data from the nonvolatile memory to the SRAM with a software address sequence. A software RECALL cycle is initiated with a sequence of READ operations in a manner similar to the software STORE initiation. To initiate the RECALL cycle, the following sequence of $\overline{CE}$ controlled READ operations must be performed:

1. Read Address 0x4E38 Valid READ
2. Read Address 0xB1C7 Valid READ
3. Read Address 0x83E0 Valid READ
4. Read Address 0x7C1F Valid READ
5. Read Address 0x703F Valid READ
6. Read Address 0x4C63 Initiate RECALL Cycle

Internally, RECALL is a two step procedure. First, the SRAM data is cleared and then, the nonvolatile information is transferred into the SRAM cells. After the $t_{RECALL}$ cycle time, the SRAM is again ready for READ and WRITE operations. The RECALL operation does not alter the data in the nonvolatile elements.

**Table 1. Mode Selection**

| $\overline{CE}$ | $\overline{WE}$ | $\overline{OE}$ | A15 - A0 | Mode | IO | Power |
|---|---|---|---|---|---|---|
| H | X | X | X | Not Selected | Output High Z | Standby |
| L | H | L | X | Read SRAM | Output Data | Active |
| L | L | X | X | Write SRAM | Input Data | Active |
| L | H | L | 0x4E38<br>0xB1C7<br>0x83E0<br>0x7C1F<br>0x703F<br>0x8B45 | Read SRAM<br>Read SRAM<br>Read SRAM<br>Read SRAM<br>Read SRAM<br>AutoStore Disable | Output Data<br>Output Data<br>Output Data<br>Output Data<br>Output Data<br>Output Data | Active[5,6,7] |
| L | H | L | 0x4E38<br>0xB1C7<br>0x83E0<br>0x7C1F<br>0x703F<br>0x4B46 | Read SRAM<br>Read SRAM<br>Read SRAM<br>Read SRAM<br>Read SRAM<br>AutoStore Enable | Output Data<br>Output Data<br>Output Data<br>Output Data<br>Output Data<br>Output Data | Active[5,6,7] |

**Notes**
5. The six consecutive address locations must be in the order listed. $\overline{WE}$ must be HIGH during all six cycles to enable a nonvolatile cycle.
6. While there are 18/17 address lines on the CY14E102L/CY14E102N, only the lower 16 lines are used to control software modes.
7. IO state depends on the state of $\overline{OE}$, $\overline{BHE}$, and $\overline{BLE}$. The IO table shown assumes $\overline{OE}$, $\overline{BHE}$, and $\overline{BLE}$ LOW.

**Table 1. Mode Selection** (continued)

| $\overline{CE}$ | $\overline{WE}$ | $\overline{OE}$ | A15 - A0 | Mode | IO | Power |
|---|---|---|---|---|---|---|
| L | H | L | 0x4E38<br>0xB1C7<br>0x83E0<br>0x7C1F<br>0x703F<br>0x8FC0 | Read SRAM<br>Read SRAM<br>Read SRAM<br>Read SRAM<br>Read SRAM<br>Nonvolatile Store | Output Data<br>Output Data<br>Output Data<br>Output Data<br>Output Data<br>Output High Z | Active $I_{CC2}$[5,6,7] |
| L | H | L | 0x4E38<br>0xB1C7<br>0x83E0<br>0x7C1F<br>0x703F<br>0x4C63 | Read SRAM<br>Read SRAM<br>Read SRAM<br>Read SRAM<br>Read SRAM<br>Nonvolatile Recall | Output Data<br>Output Data<br>Output Data<br>Output Data<br>Output Data<br>Output High Z | Active[5,6,7] |

## Preventing AutoStore

The AutoStore function is disabled by initiating an AutoStore disable sequence. A sequence of read operations is performed in a manner similar to the software STORE initiation. To initiate the AutoStore disable sequence, the following sequence of $\overline{CE}$ controlled read operations must be performed:

1. Read address 0x4E38 Valid READ
2. Read address 0xB1C7 Valid READ
3. Read address 0x83E0 Valid READ
4. Read address 0x7C1F Valid READ
5. Read address 0x703F Valid READ
6. Read address 0x8B45 AutoStore Disable

The AutoStore is re-enabled by initiating an AutoStore enable sequence. A sequence of read operations is performed in a manner similar to the software RECALL initiation. To initiate the AutoStore enable sequence, the following sequence of $\overline{CE}$ controlled read operations must be performed:

1. Read address 0x4E38 Valid READ
2. Read address 0xB1C7 Valid READ
3. Read address 0x83E0 Valid READ
4. Read address 0x7C1F Valid READ
5. Read address 0x703F Valid READ
6. Read address 0x4B46 AutoStore Enable

If the AutoStore function is disabled or re-enabled a manual STORE operation (hardware or software) must be issued to save the AutoStore state through subsequent power down cycles. The part comes from the factory with AutoStore enabled.

## Data Protection

The CY14E102L/CY14E102N protects data from corruption during low voltage conditions by inhibiting all externally initiated STORE and write operations. The low voltage condition is detected when $V_{CC} < V_{SWITCH}$. If the CY14E102L/CY14E102N is in a write mode (both $\overline{CE}$ and $\overline{WE}$ LOW) at power up, after a RECALL or STORE, the write is inhibited until a negative transition on $\overline{CE}$ or $\overline{WE}$ is detected. This protects against inadvertent writes during power up or brown out conditions.

## Noise Considerations

Refer CY Application Note AN1064.

## Maximum Ratings

Exceeding maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage Temperature ..... –65°C to +150°C

Ambient Temperature with Power Applied ..... –55°C to +150°C

Supply Voltage on $V_{CC}$ Relative to GND .....–0.5V to 7.0V

Voltage Applied to Outputs in High-Z State..... –0.5V to $V_{CC}$ + 0.5V

Input Voltage.....–0.5V to Vcc+0.5V

Transient Voltage (<20 ns) on Any Pin to Ground Potential ..... –2.0V to $V_{CC}$ + 2.0V

Package Power Dissipation Capability ($T_A$ = 25°C) ..... 1.0W

Surface Mount Pb Soldering Temperature (3 Seconds) ..... +260°C

Output Short Circuit Current [8]..... 15 mA

Static Discharge Voltage..... > 2001V (per MIL-STD-883, Method 3015)

Latch-Up Current..... > 200 mA

## Operating Range

| Range | Ambient Temperature | $V_{CC}$ |
|---|---|---|
| Commercial | 0°C to +70°C | 4.5V to 5.5V |
| Industrial | –40°C to +85°C | 4.5V to 5.5V |

## DC Electrical Characteristics

Over the Operating Range ($V_{CC}$ = 4.5V to 5.5V)[10]

| Parameter | Description | Test Conditions | | Min | Max | Unit |
|---|---|---|---|---|---|---|
| $I_{CC1}$ | Average $V_{CC}$ Current | $t_{RC}$ = 15 ns<br>$t_{RC}$ = 20 ns<br>$t_{RC}$ = 25 ns<br>$t_{RC}$ = 45 ns<br>Dependent on output loading and cycle rate.Values obtained without output loads.<br>$I_{OUT}$ = 0 mA | Commercial | | 70<br>65<br>65<br>50 | mA<br>mA<br>mA |
| | | | Industrial | | 75<br>70<br>70<br>52 | mA<br>mA<br>mA |
| $I_{CC2}$ | Average $V_{CC}$ Current during STORE | All Inputs Don't Care, $V_{CC}$ = Max<br>Average current for duration $t_{STORE}$ | | | 6 | mA |
| $I_{CC3}$[9] | Average $V_{CC}$ Current at $t_{RC}$= 200 ns, 5V, 25°C typical | $\overline{WE}$ > ($V_{CC}$ – 0.2). All other I/P cycling.<br>Dependent on output loading and cycle rate. Values obtained without output loads. | | | 35 | mA |
| $I_{CC4}$ | Average $V_{CAP}$ Current during AutoStore Cycle | All Inputs Don't Care, $V_{CC}$ = Max<br>Average current for duration $t_{STORE}$ | | | 6 | mA |
| $I_{SB}$ | $V_{CC}$ Standby Current | $\overline{CE}$ > ($V_{CC}$ – 0.2). All others $V_{IN}$ < 0.2V or > ($V_{CC}$ – 0.2V).<br>Standby current level after nonvolatile cycle is complete.<br>Inputs are static. f = 0 MHz. | | | 3 | mA |
| $I_{IX}$ | Input Leakage Current (except HSB) | $V_{CC}$ = Max, $V_{SS} \le V_{IN} \le V_{CC}$ | | –1 | +1 | µA |
| | Input Leakage Current (For HSB) | $V_{CC}$ = Max, $V_{SS} \le V_{IN} \le V_{CC}$ | | –100 | +1 | µA |
| $I_{OZ}$ | Off-State Output Leakage Current | $V_{CC}$ = Max, $V_{SS} \le V_{IN} \le V_{CC}$, $\overline{CE}$ or $\overline{OE}$ > $V_{IH}$ | | –1 | +1 | µA |
| $V_{IH}$ | Input HIGH Voltage | | | 2.0 | $V_{CC}$ + 0.5 | V |
| $V_{IL}$ | Input LOW Voltage | | | $V_{SS}$ – 0.5 | 0.8 | V |
| $V_{OH}$ | Output HIGH Voltage | $I_{OUT}$ = –2 mA | | 2.4 | | V |
| $V_{OL}$ | Output LOW Voltage | $I_{OUT}$ = 4 mA | | | 0.4 | V |
| $V_{CAP}$ | Storage Capacitor | Between $V_{CAP}$ pin and $V_{SS}$, 5V Rated | | 61 | 82 | µF |

**Notes**

8. Outputs shorted for no more than one second. No more than one output shorted at a time.
9. Typical conditions for the active current shown on the front page of the data sheet are average values at 25°C (room temperature), and $V_{CC}$ = 5V. Not 100% tested.
10. The $\overline{HSB}$ pin has $I_{OUT}$=-10 uA for $V_{OH}$ of 2.4V.This parameter is characterized but not tested.

## Capacitance

The following table lists the capacitance parameters.[11]

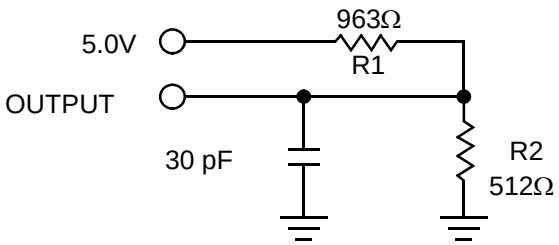
| Parameter | Description | Test Conditions | Max | Unit |
|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | $T_A$ = 25°C, f = 1 MHz, $V_{CC}$ = 0 to 3.0V | 7 | pF |
| $C_{OUT}$ | Output Capacitance | | 7 | pF |

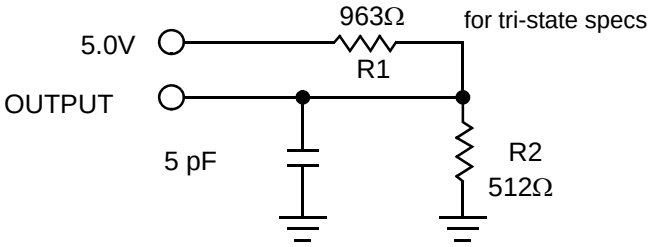
## Thermal Resistance

The following table lists the thermal resistance parameters. [11]

| Parameter | Description | Test Conditions | 48-FBGA | 44-TSOP II | 54-TSOP II | Unit |
|---|---|---|---|---|---|---|
| $\Theta_{JA}$ | Thermal Resistance (Junction to Ambient) | Test conditions follow standard test methods and procedures for measuring thermal impedance, in accordance with EIA/JESD51. | 28.82 | 31.11 | 30.73 | °C/W |
| $\Theta_{JC}$ | Thermal Resistance (Junction to Case) | | 7.84 | 5.56 | 6.08 | °C/W |

## AC Test Loads




## AC Test Conditions

Input Pulse Levels ..... 0V to 3V

Input Rise and Fall Times (10% - 90%) ..... <5 ns

Input and Output Timing Reference Levels ..... 1.5V

**Note**

11. These parameters are guaranteed but not tested.

## AC Switching Characteristics

The following table lists the AC switching characteristics.

| Parameters | | Description | 15 ns | | 20 ns | | 25 ns | | 45 ns | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Cypress Parameters | Alt Parameters | | Min | Max | Min | Max | Min | Max | Min | Max | |
| **SRAM Read Cycle** | | | | | | | | | | | |
| $t_{ACE}$ | $t_{ACS}$ | Chip Enable Access Time | | 15 | | 20 | | 25 | | 45 | ns |
| $t_{RC}$[12] | $t_{RC}$ | Read Cycle Time | 15 | | 20 | | 25 | | 45 | | ns |
| $t_{AA}$[13] | $t_{AA}$ | Address Access Time | | 15 | | 20 | | 25 | | 45 | ns |
| $t_{DOE}$ | $t_{OE}$ | Output Enable to Data Valid | | 10 | | 10 | | 12 | | 20 | ns |
| $t_{OHA}$ | $t_{OH}$ | Output Hold After Address Change | 3 | | 3 | | 3 | | 3 | | ns |
| $t_{LZCE}$[14] | $t_{LZ}$ | Chip Enable to Output Active | 3 | | 3 | | 3 | | 3 | | ns |
| $t_{HZCE}$[14] | $t_{HZ}$ | Chip Disable to Output Inactive | | 7 | | 8 | | 10 | | 15 | ns |
| $t_{LZOE}$[14] | $t_{OLZ}$ | Output Enable to Output Active | 0 | | 0 | | 0 | | 0 | | ns |
| $t_{HZOE}$[14] | $t_{OHZ}$ | Output Disable to Output Inactive | | 7 | | 8 | | 10 | | 15 | ns |
| $t_{PU}$[11] | $t_{PA}$ | Chip Enable to Power Active | 0 | | 0 | | 0 | | 0 | | ns |
| $t_{PD}$[11] | $t_{PS}$ | Chip Disable to Power Standby | | 15 | | 20 | | 25 | | 45 | ns |
| $t_{DBE}$ | - | Byte Enable to Data Valid | | 10 | | 10 | | 12 | | 20 | ns |
| $t_{LZBE}$ | - | Byte Enable to Output Active | 0 | | 0 | | 0 | | 0 | | ns |
| $t_{HZBE}$ | - | Byte Disable to Output Inactive | | 7 | | 8 | | 10 | | 15 | ns |
| **SRAM Write Cycle** | | | | | | | | | | | |
| $t_{WC}$ | $t_{WC}$ | Write Cycle Time | 15 | | 20 | | 25 | | 45 | | ns |
| $t_{PWE}$ | $t_{WP}$ | Write Pulse Width | 10 | | 15 | | 20 | | 30 | | ns |
| $t_{SCE}$ | $t_{CW}$ | Chip Enable To End of Write | 15 | | 15 | | 20 | | 30 | | ns |
| $t_{SD}$ | $t_{DW}$ | Data Setup to End of Write | 5 | | 8 | | 10 | | 15 | | ns |
| $t_{HD}$ | $t_{DH}$ | Data Hold After End of Write | 0 | | 0 | | 0 | | 0 | | ns |
| $t_{AW}$ | $t_{AW}$ | Address Setup to End of Write | 10 | | 15 | | 20 | | 30 | | ns |
| $t_{SA}$ | $t_{AS}$ | Address Setup to Start of Write | 0 | | 0 | | 0 | | 0 | | ns |
| $t_{HA}$ | $t_{WR}$ | Address Hold After End of Write | 0 | | 0 | | 0 | | 0 | | ns |
| $t_{HZWE}$[14,15] | $t_{WZ}$ | Write Enable to Output Disable | | 7 | | 8 | | 10 | | 15 | ns |
| $t_{LZWE}$[14] | $t_{OW}$ | Output Active after End of Write | 3 | | 3 | | 3 | | 3 | | ns |
| $t_{BW}$ | - | Byte Enable to End of Write | 15 | | 15 | | 20 | | 30 | | ns |

**Notes**
12. $\overline{WE}$ must be HIGH during SRAM read cycles.
13. Device is continuously selected with $\overline{CE}$ and $\overline{OE}$ both LOW.
14. Measured ±200 mV from steady state output voltage.
15. If $\overline{WE}$ is LOW when $\overline{CE}$ goes LOW, the output goes into high impedance state.

## AutoStore and Power Up RECALL

| Parameters | Description | CY14E102L/CY14E102N | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| $t_{HRECALL}$ [16] | Power Up RECALL Duration | | 20 | ms |
| $t_{STORE}$ [17] | STORE Cycle Duration | | 15 | ms |
| $V_{SWITCH}$ | Low Voltage Trigger Level | | 4.4 | V |
| $t_{VCCRISE}$ | VCC Rise Time | 150 | | µs |

## Software Controlled STORE and RECALL Cycle

The following table lists the software controlled STORE and RECALL cycle parameters.[18, 19]

| Parameters | Description | 15ns | | 20 ns | | 25ns | | 45ns | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | Min | Max | |
| $t_{RC}$ | STORE and RECALL Initiation Cycle Time | 15 | | 20 | | 25 | | 45 | | ns |
| $t_{AS}$ | Address Setup Time | 0 | | 0 | | 0 | | 0 | | ns |
| $t_{CW}$ | Clock Pulse Width | 12 | | 15 | | 20 | | 30 | | ns |
| $t_{GHAX}$ | Address Hold Time | 1 | | 1 | | 1 | | 1 | | ns |
| $t_{RECALL}$ | RECALL Duration | | 200 | | 200 | | 200 | | 200 | µs |
| $t_{SS}$ [20, 21] | Soft Sequence Processing Time | | 70 | | 70 | | 70 | | 70 | µs |

## Hardware STORE Cycle

| Parameters | Description | CY14E102L/CY14E102N | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| $t_{DELAY}$ [22] | Time allowed to complete SRAM cycle | 1 | 70 | µs |
| $t_{HLHX}$ | Hardware STORE pulse width | 15 | | ns |

**Notes**

16. $t_{HRECALL}$ starts from the time $V_{CC}$ rises above $V_{SWITCH}$.
17. If an SRAM Write has not taken place since the last nonvolatile cycle, no STORE takes place.
18. The software sequence is clocked with $\overline{CE}$ controlled or $\overline{OE}$ controlled reads.
19. The six consecutive addresses must be read in the order listed in the mode selection table. $\overline{WE}$ must be HIGH during all six consecutive cycles.
20. This is the amount of time it takes to take action on a soft sequence command.Vcc power must remain HIGH to effectively register command.
21. Commands such as STORE and RECALL lock out IO until operation is complete which further increases this time. See the specific command.
22. On a hardware STORE initiation, SRAM operation continues to be enabled for time $t_{DELAY}$ to allow read and write cycles to complete.

## Switching Waveforms

**Figure 5. SRAM Read Cycle #1: Address Controlled**[12, 13, 23]

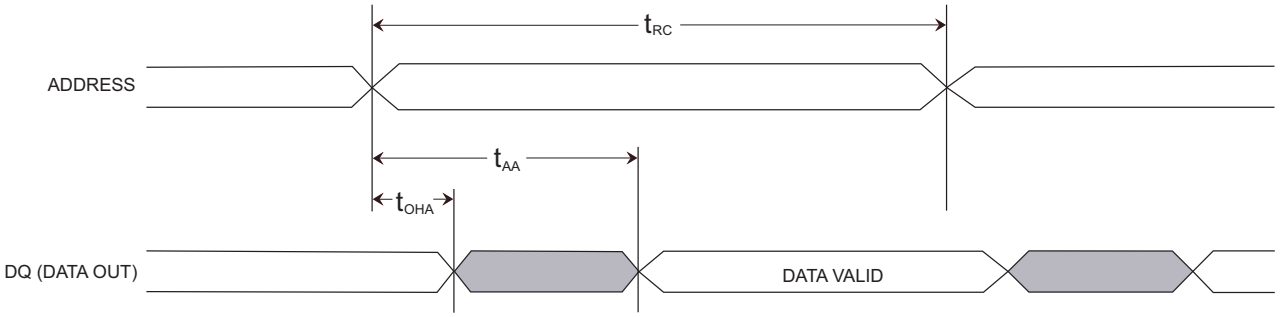
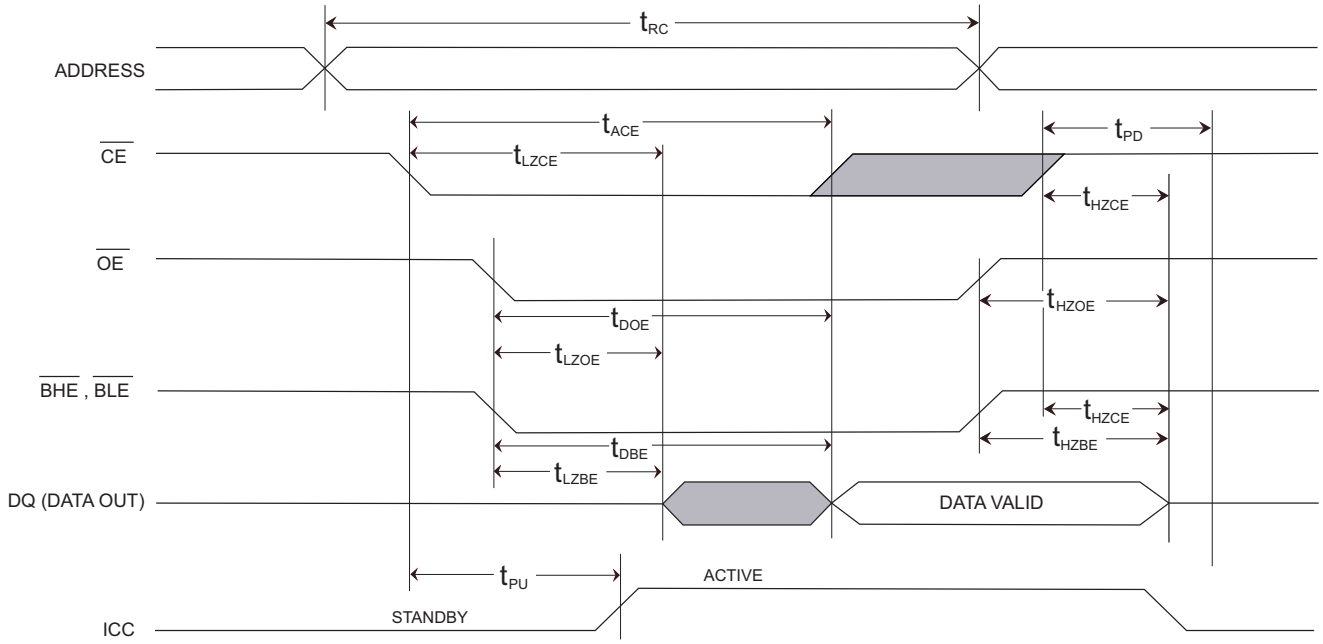



**Figure 6. SRAM Read Cycle #2: $\overline{CE}$ and $\overline{OE}$ Controlled**[12, 23, 25]




**Notes**
23. $\overline{HSB}$ must remain HIGH during READ and WRITE cycles.
24. $\overline{CE}$ or $\overline{WE}$ must be $\geq V_{IH}$ during address transitions.
25. $\overline{BHE}$ and $\overline{BLE}$ are applicable for x16 configuration only.

## Switching Waveforms (continued)

**Figure 7. SRAM Write Cycle #1: $\overline{WE}$ Controlled**[13, 21, 22, 23]

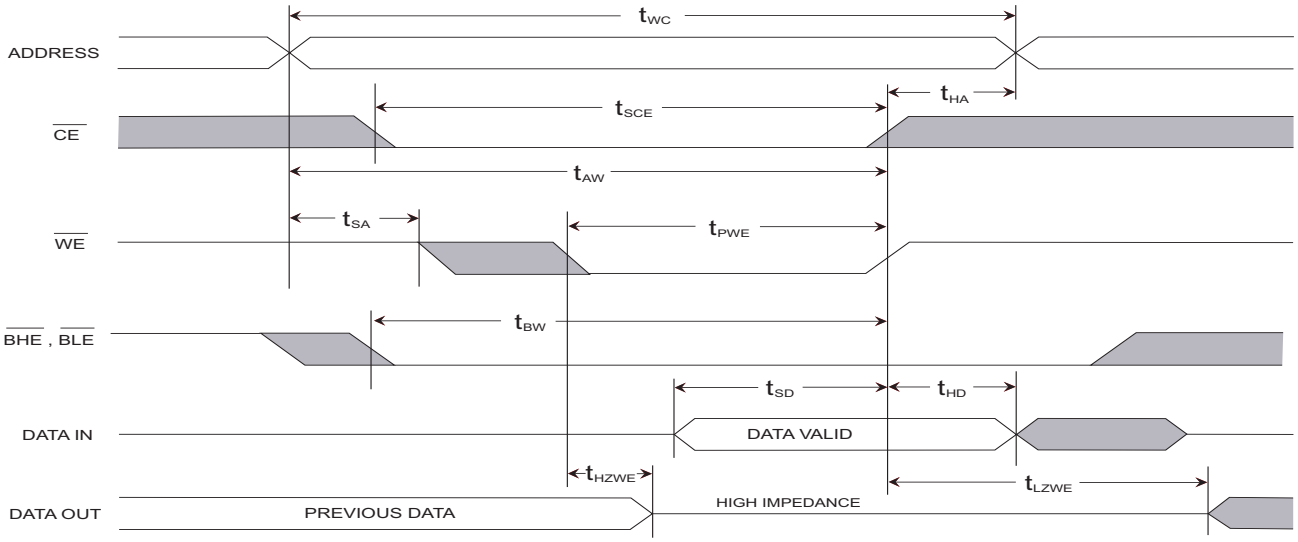
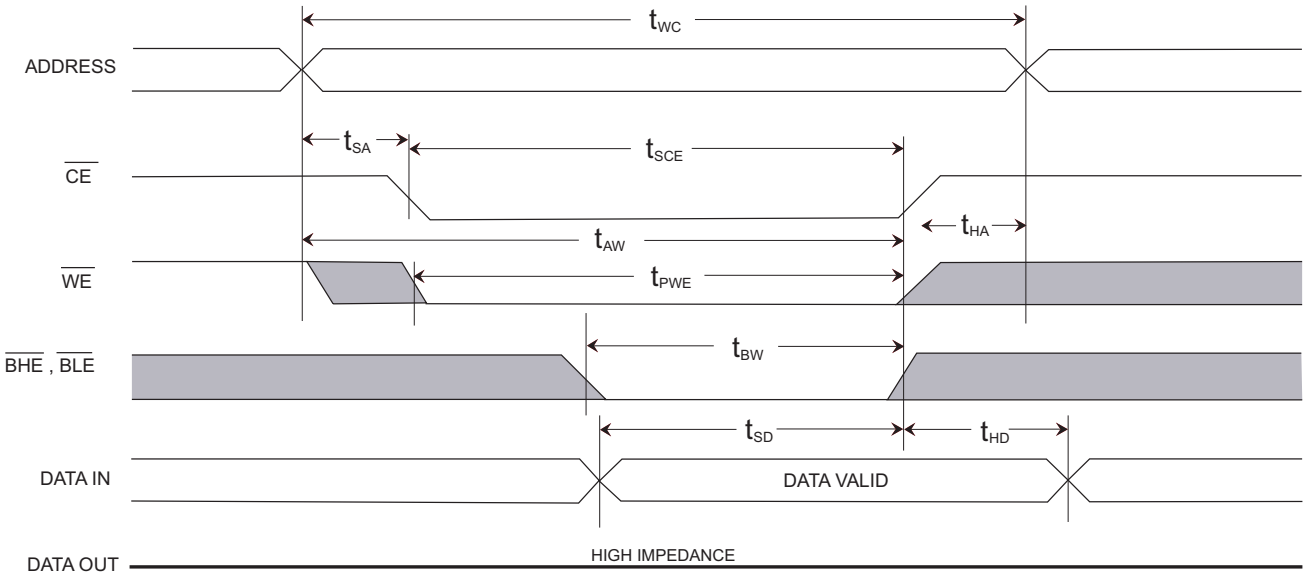



**Figure 8. SRAM Write Cycle #2: $\overline{CE}$ Controlled**[13, 21, 22, 23]



## Switching Waveforms (continued)

**Figure 9. AutoStore or Power Up RECALL[26]**

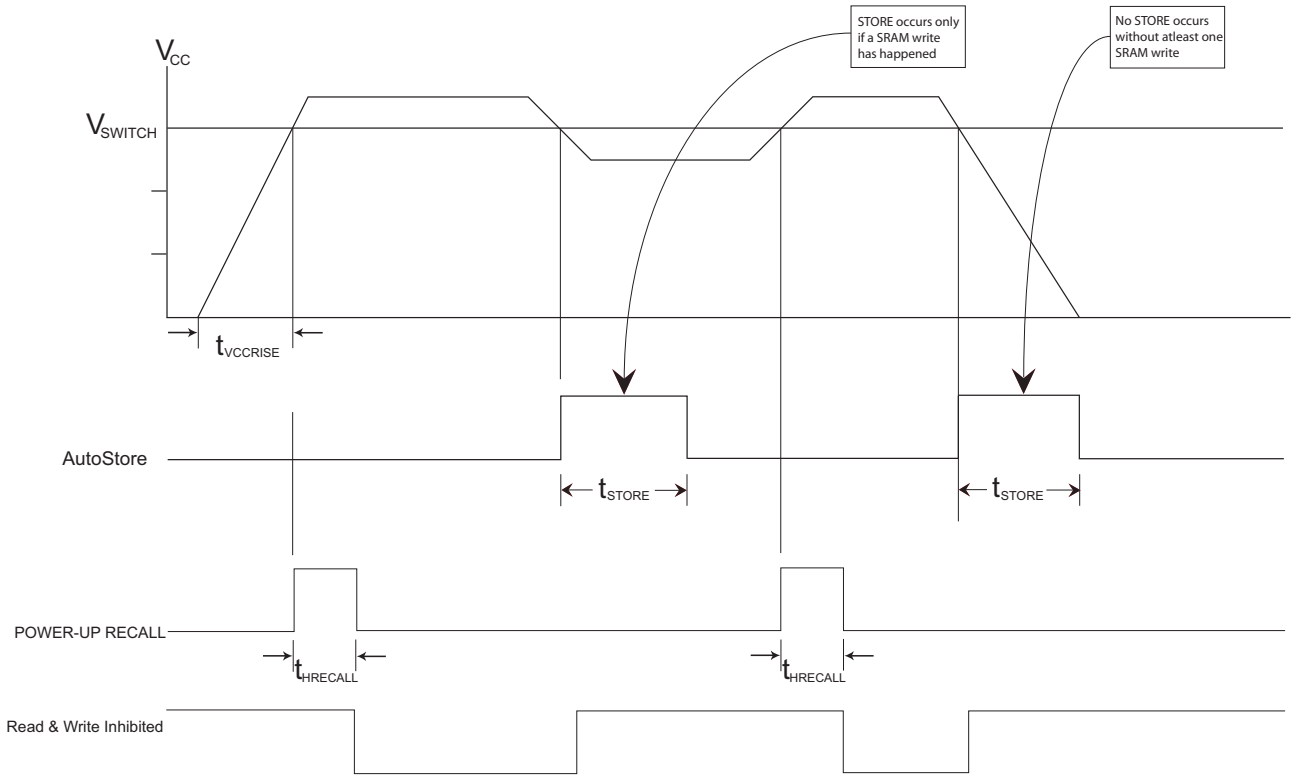
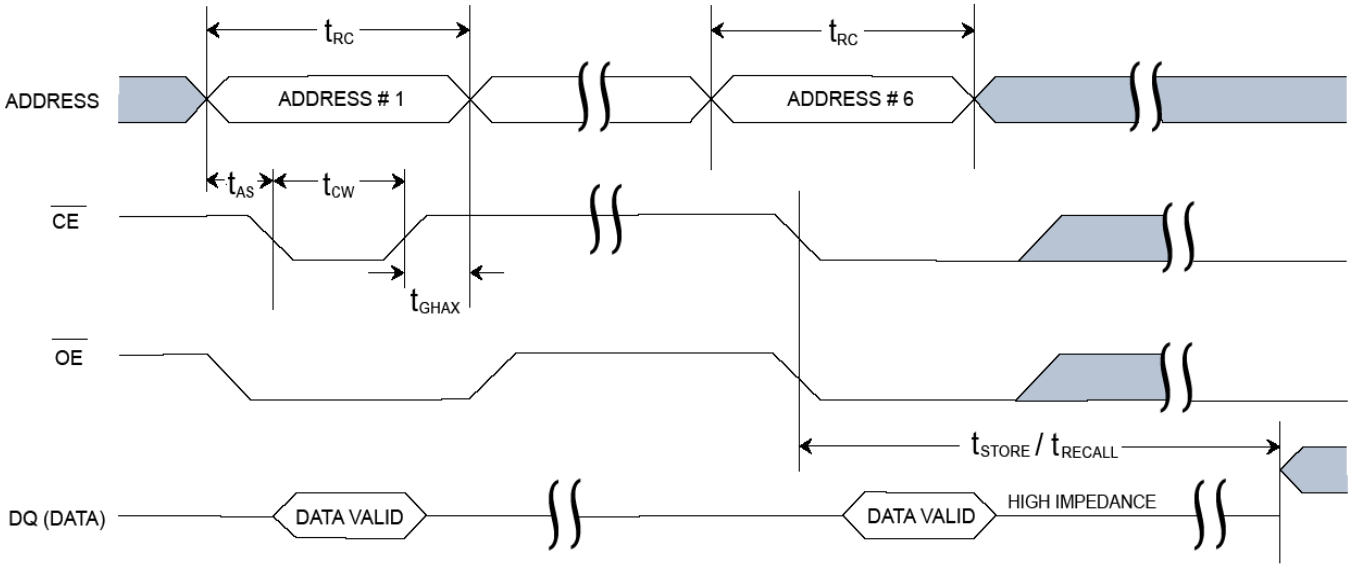



**Figure 10. $\overline{CE}$ Controlled Software STORE/RECALL Cycle[19]**




**Note**
26. Read and Write cycles are ignored during STORE, RECALL, and while VCC is below $V_{SWITCH}$.

## Switching Waveforms (continued)

**Figure 11. $\overline{OE}$ Controlled Software STORE/RECALL Cycle[19]**

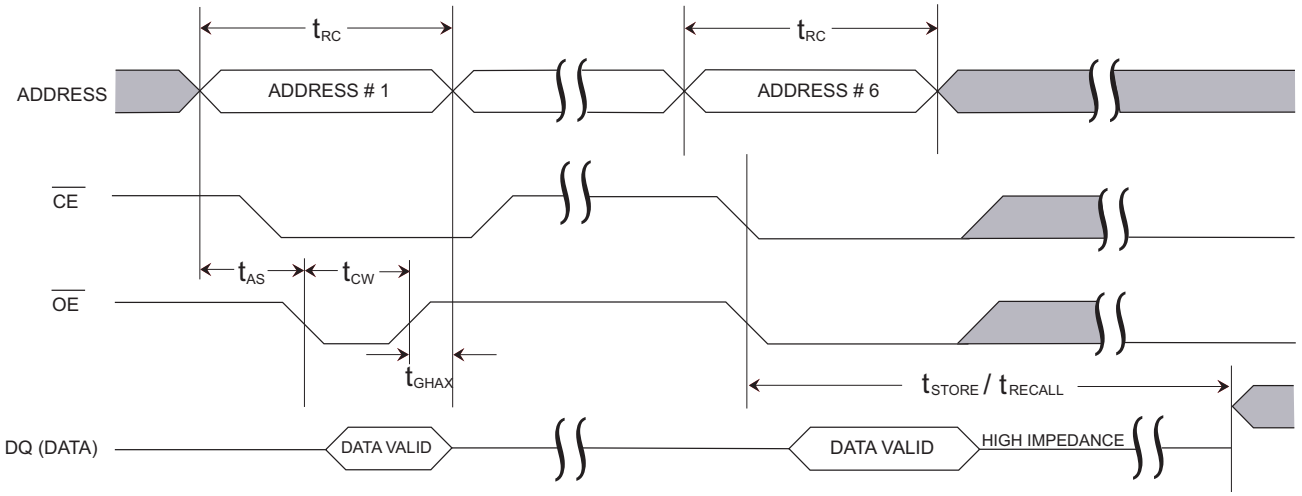



**Figure 12. Hardware STORE Cycle[22]**

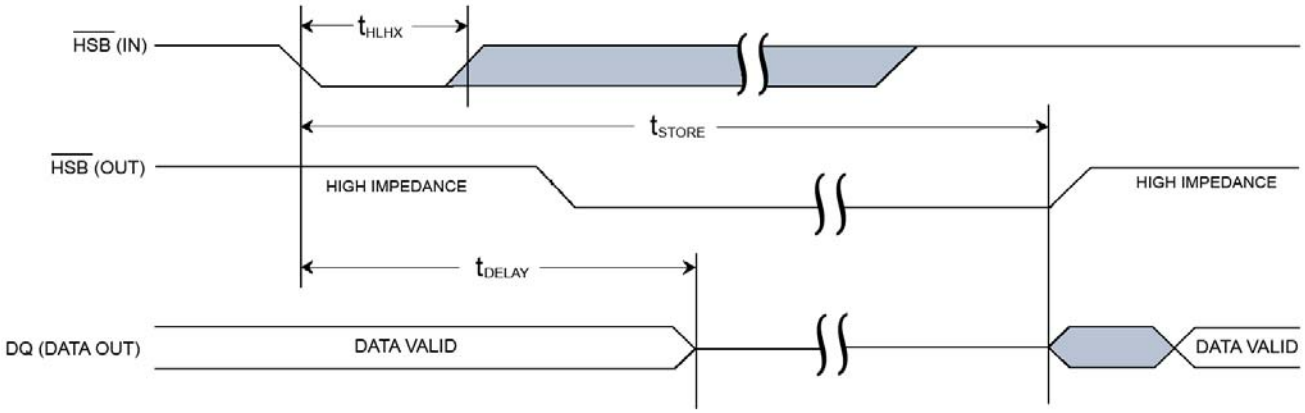
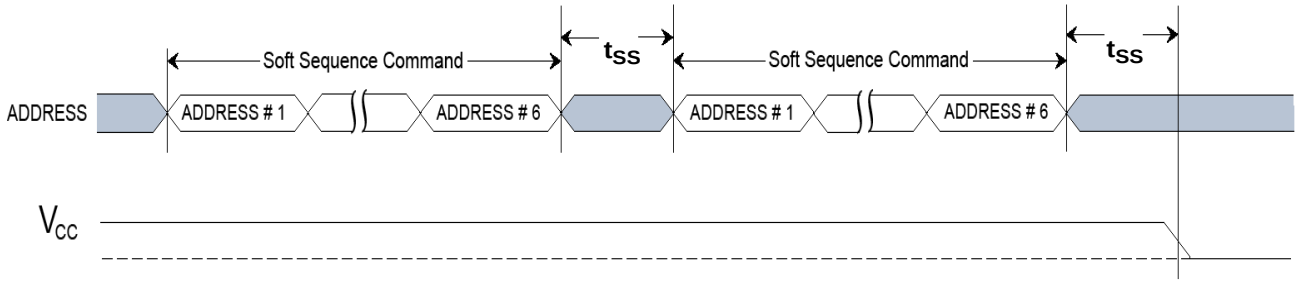



**Figure 13. Soft Sequence Processing[20, 21]**



## Ordering Information

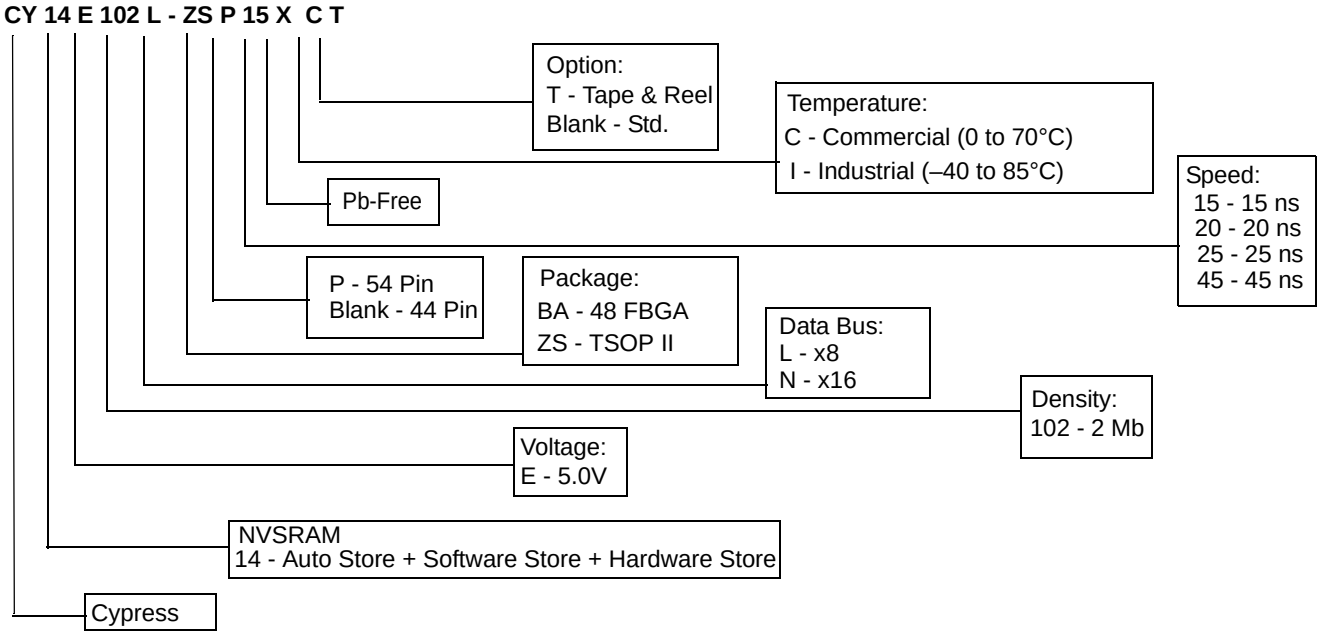
| Speed (ns) | Ordering Code | Package Diagram | Package Type | Operating Range |
|---|---|---|---|---|
| 15 | CY14B102L-ZS15XCT | 51-85087 | 44-pin TSOP II | Commercial |
| | CY14E102L-ZS15XIT | 51-85087 | 44-pin TSOP II | Industrial |
| | CY14E102L-ZS15XI | 51-85087 | 44-pin TSOP II | |
| | CY14E102L-BA15XCT | 51-85128 | 48-ball FBGA | Commercial |
| | CY14E102L-BA15XIT | 51-85128 | 48-ball FBGA | Industrial |
| | CY14E102L-BA15XI | 51-85128 | 48-ball FBGA | |
| | CY14E102L-ZSP15XCT | 51-85160 | 54-pin TSOP II | Commercial |
| | CY14E102L-ZSP15XIT | 51-85160 | 54-pin TSOP II | Industrial |
| | CY14E102L-ZSP15XI | 51-85160 | 54-pin TSOP II | |
| | CY14E102N-BA115XCT | 51-85128 | 48-ball FBGA | Commercial |
| | CY14E102N-BA15XIT | 51-85128 | 48-ball FBGA | Industrial |
| | CY14E102N-BA15XI | 51-85128 | 48-ball FBGA | |
| | CY14E102N-ZSP15XCT | 51-85160 | 54-pin TSOP II | Commercial |
| | CY14E102N-ZSP15XIT | 51-85160 | 54-pin TSOP II | Industrial |
| | CY14E102N-ZSP15XI | 51-85160 | 54-pin TSOP II | |
| 20 | CY14B102L-ZS20XCT | 51-85087 | 44-pin TSOP II | Commercial |
| | CY14E102L-ZS20XIT | 51-85087 | 44-pin TSOP II | Industrial |
| | CY14E102L-ZS20XI | 51-85087 | 44-pin TSOP II | |
| | CY14E102L-BA20XCT | 51-85128 | 48-ball FBGA | Commercial |
| | CY14E102L-BA20XIT | 51-85128 | 48-ball FBGA | Industrial |
| | CY14E102L-BA20XI | 51-85128 | 48-ball FBGA | |
| | CY14E102L-ZSP20XCT | 51-85160 | 54-pin TSOP II | Commercial |
| | CY14E102L-ZSP20XIT | 51-85160 | 54-pin TSOP II | Industrial |
| | CY14E102L-ZSP20XI | 51-85160 | 54-pin TSOP II | |
| | CY14E102N-BA20XCT | 51-85128 | 48-ball FBGA | Commercial |
| | CY14E102N-BA20XIT | 51-85128 | 48-ball FBGA | Industrial |
| | CY14E102N-BA20XI | 51-85128 | 48-ball FBGA | |
| | CY14E102N-ZSP20XCT | 51-85160 | 54-pin TSOP II | Commercial |
| | CY14E102N-ZSP20XIT | 51-85160 | 54-pin TSOP II | Industrial |
| | CY14E102N-ZSP20XI | 51-85160 | 54-pin TSOP II | |

## Ordering Information (continued)

| Speed (ns) | Ordering Code | Package Diagram | Package Type | Operating Range |
|---|---|---|---|---|
| 25 | CY14E102L-ZS25XCT | 51-85087 | 44-pin TSOP II | Commercial |
| | CY14E102L-ZS25XIT | 51-85087 | 44-pin TSOP II | Industrial |
| | CY14E102L-ZS25XI | 51-85087 | 44-pin TSOP II | |
| | CY14E102N-BA25XCT | 51-85128 | 48-ball FBGA | Commercial |
| | CY14E102L-BA25XIT | 51-85128 | 48-ball FBGA | Industrial |
| | CY14E102L-BA25XI | 51-85128 | 48-ball FBGA | |
| | CY14E102L-ZSP25XCT | 51-85160 | 54-pin TSOP II | Commercial |
| | CY14E102L-ZSP25XIT | 51-85160 | 54-pin TSOP II | Industrial |
| | CY14E102L-ZSP25XI | 51-85160 | 54-pin TSOP II | |
| | CY14E102N-BA25XCT | 51-85128 | 48-ball FBGA | Commercial |
| | CY14E102N-BA25XIT | 51-85128 | 48-ball FBGA | Industrial |
| | CY14E102N-BA25XI | 51-85128 | 48-ball FBGA | |
| | CY14E102N-ZSP25XCT | 51-85160 | 54-pin TSOP II | Commercial |
| | CY14E102N-ZSP25XIT | 51-85160 | 54-pin TSOP II | Industrial |
| | CY14E102N-ZSP25XI | 51-85160 | 54-pin TSOP II | |
| 45 | CY14E102L-ZS45XCT | 51-85087 | 44-pin TSOP II | Commercial |
| | CY14E102L-ZS45XIT | 51-85087 | 44-pin TSOP II | Industrial |
| | CY14E102L-ZS45XI | 51-85087 | 44-pin TSOP II | |
| | CY14E102L-BA45XCT | 51-85128 | 48-ball FBGA | Commercial |
| | CY14E102L-BA45XIT | 51-85128 | 48-ball FBGA | Industrial |
| | CY14E102L-BA45XI | 51-85128 | 48-ball FBGA | |
| | CY14E102L-ZSP45XCT | 51-85160 | 54-pin TSOP II | Commercial |
| | CY14E102L-ZSP45XIT | 51-85160 | 54-pin TSOP II | Industrial |
| | CY14E102L-ZSP45XI | 51-85160 | 54-pin TSOP II | |
| | CY14E102N-BA45XCT | 51-85128 | 48-ball FBGA | Commercial |
| | CY14E102N-BA45XIT | 51-85128 | 48-ball FBGA | Industrial |
| | CY14E102N-BA45XI | 51-85128 | 48-ball FBGA | |
| | CY14E102N-ZSP45XCT | 51-85160 | 54-pin TSOP II | Commercial |
| | CY14E102N-ZSP45XIT | 51-85160 | 54-pin TSOP II | Industrial |
| | CY14E102N-ZSP45XI | 51-85160 | 54-pin TSOP II | |

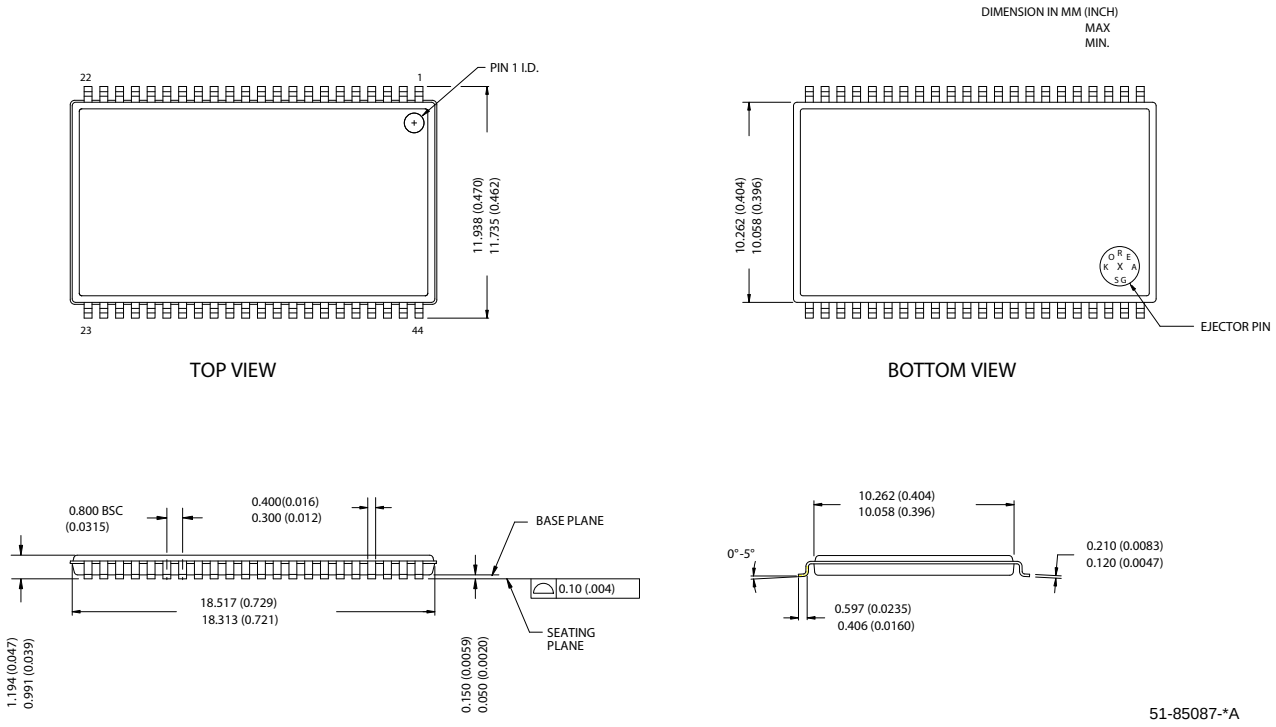
All parts are Pb-free. The above table contains Advance information. Please contact your local Cypress sales representative for availability of these parts.

## Part Numbering Nomenclature



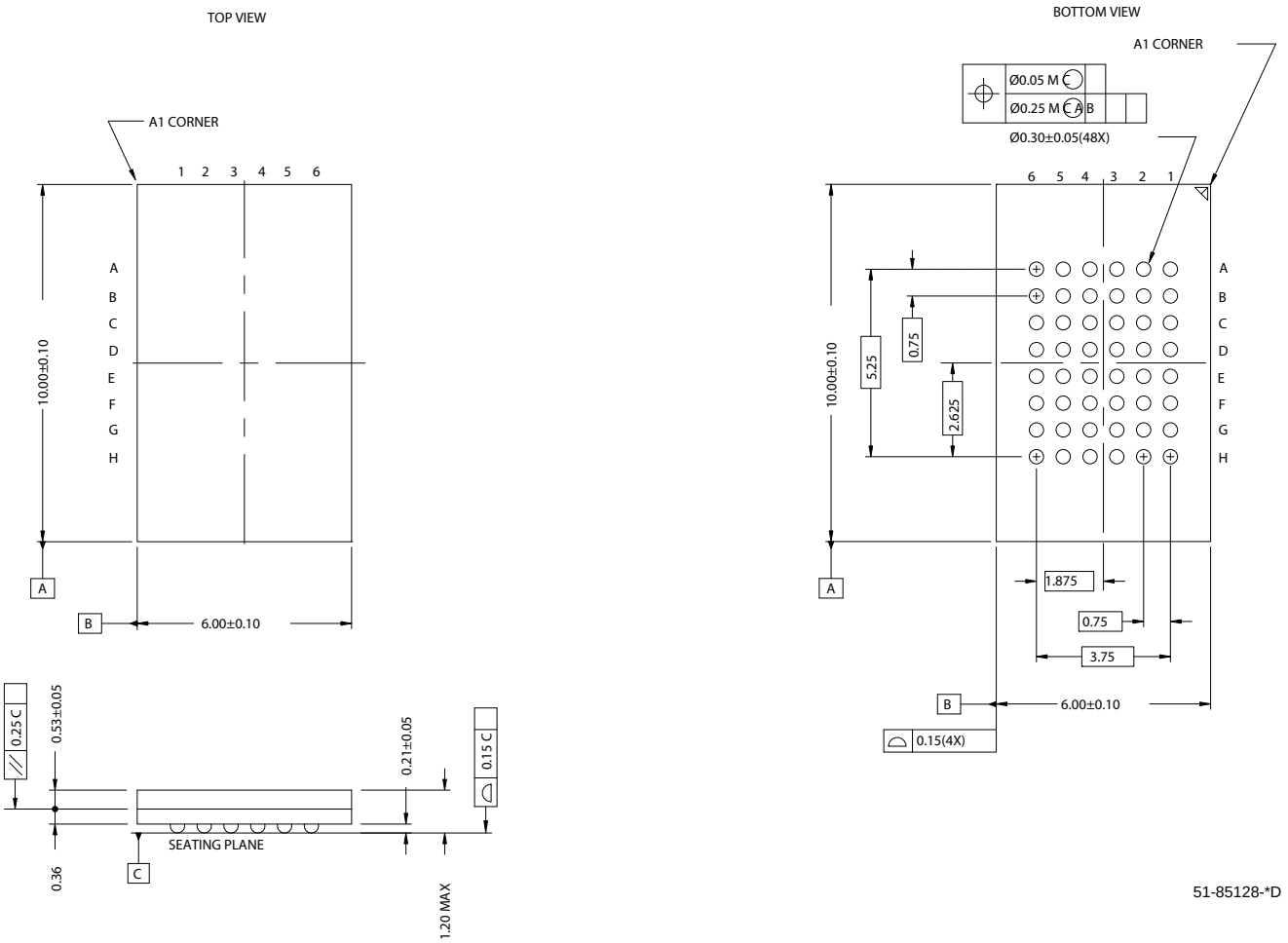
## Package Diagrams

**Figure 14. 44-Pin TSOP II**



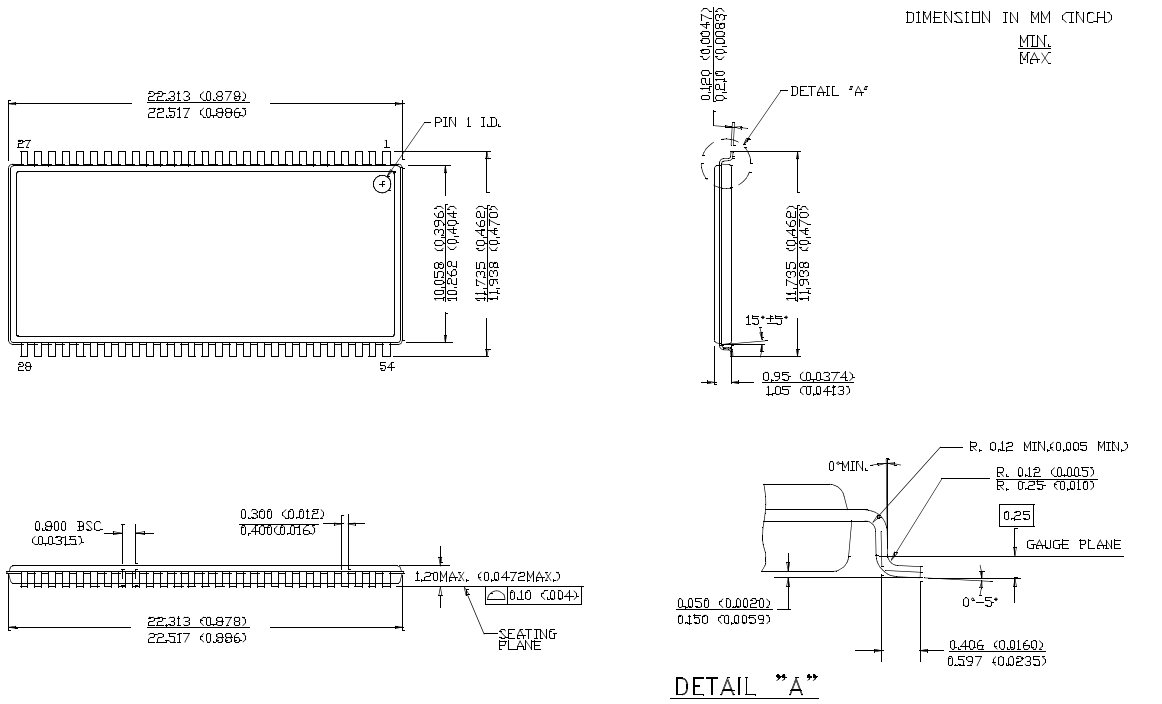
## Package Diagrams (continued)

**Figure 15. 48-Ball FBGA - 6 mm x 10 mm x 1.2 mm**



## Package Diagrams (continued)

**Figure 16. 54-Pin TSOP II**



## Document History Page

| Document Title: CY14E102L/CY14E102N 2-Mbit (256K x 8/128K x 16) nvSRAM<br>Document Number: 001- 45755 | | | | |
|---|---|---|---|---|
| **REV.** | **ECN NO.** | **Orig. of Change** | **Submission Date** | **Description of Change** |
| ** | 2470086 | GVCH | | New Data Sheet |
| *A | 2522209 | GVCH/ AESA | 06/27/2008 | Added 20 ns access speed information in “Features”.<br>Added $I_{CC1}$ for $t_{RC}$=20 ns for both industrial and Commercial temperature Grade.<br>Updated Thermal resistance values for 48-FBGA, 44-TSOP II and 54-TSOP II Packages.<br>Added AC Switching Characteristics specs for 20 ns access speed.<br>Added software controlled STORE/RECALL cycle specs for 20 ns access speed.<br>Updated ordering information and part numbering nomenclature.<br>Updated data sheet template. |

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