

# MoBL<sup>®</sup>,CY62126EV30

# 1-Mbit (64K x 16) Static RAM

### Features

- High speed: 45 ns
- Temperature ranges
  □ Industrial: -40°C to +85°C
  □ Automotive: -40°C to +125°C
- Wide voltage range: 2.2V to 3.6V
- Pin compatible with CY62126DV30
- Ultra low standby power
  Typical standby current: 1 μA
  Maximum standby current: 4 μA
- Ultra low active power
  Typical active current: 1.3 mA at f = 1 MHz
- Easy memory expansion with CE and OE features
- Automatic power down when deselected
- CMOS for optimum speed and power
- Offered in Pb-free 48-ball VFBGA and 44-pin TSOP II packages

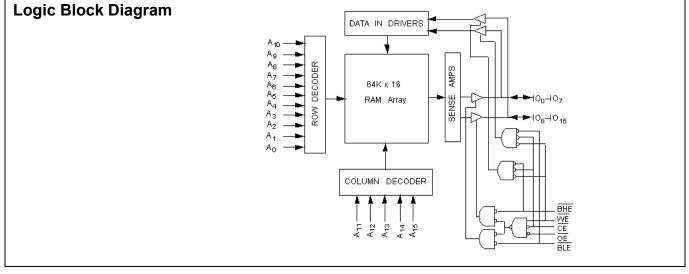
### **Functional Description**

The CY62126EV30 is a high performance CMOS static RAM organized as 64K words by 16 bits<sup>[1]</sup>. This device features advanced circuit design to provide ultra low active current. This is ideal for providing More Battery Life<sup>TM</sup> (MoBL<sup>®</sup>) in portable applications such as cellular telephones. The device also has an automatic power down feature that significantly reduces power consumption when addresses are not toggling. Placing the device in standby mode reduces power consumption by more than 99 percent when deselected (CE HIGH). The input and output pins (IO<sub>0</sub> through IO<sub>15</sub>) are placed in a high impedance state when:

- Deselected (CE HIGH)
- Outputs are disabled (OE HIGH)
- <u>Both</u> B<u>yte</u> High Enable and Byte Low Enable are disabled (BHE, BLE HIGH)
- Write operation is active (CE LOW and WE LOW)

To write to the device, take Chip Enable  $\overline{(CE)}$  and Write Enable  $\overline{(WE)}$  inputs LOW. If Byte Low Enable (BLE) is LOW, then data from IO pins (IO<sub>0</sub> through IO<sub>7</sub>) is written into the location specified on the address pins (A<sub>0</sub> through A<sub>15</sub>). If Byte High Enable (BHE) is LOW, then data from IO pins (IO<sub>8</sub> through IO<sub>15</sub>) is written into the location specified on the address pins (A<sub>0</sub> through A<sub>15</sub>).

To read <u>from</u> the device, take Chip Enable (CE) and Output Enable (OE) LOW while forcing the Write Enable (WE) HIGH. If Byte Low Enable (BLE) is LOW, then data from the memory location specified by the address pins appear on  $IO_0$  to  $IO_7$ . If Byte High Enable (BHE) is LOW, then data from memory appears on  $IO_8$  to  $IO_{15}$ . See the "Truth Table" on page 9 for a complete description of read and write modes.



#### Note

1. For best practice recommendations, refer to the Cypress application note AN1064, SRAM System Guidelines.

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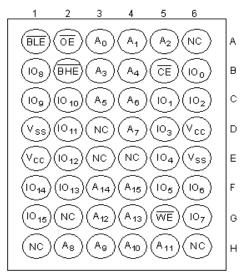
San Jose, CA 95134-1709

9 • 408-943-2600 Revised January 5, 2009



### **Pin Configurations**

### Figure 1. 44-Ball VFBGA (Top View)



### Figure 2. 44-Pin TSOP II (Top View)<sup>[2]</sup>

$\begin{array}{c} A_4 & \square \\ A_3 & \square \\ A_2 & \square \\ A_2 & \square \\ A_1 & \square \\ B_2 & \square \\$	44   A <sub>5</sub> 43   A <sub>6</sub> 42   OE 41   OE 39   BLE 39   IO15 37   IO14 36   IO12 34   Vss 33   IO10 30   IO3 31   IO10 30   IO9 29   NC 27   A <sub>8</sub> 26   A <sub>10</sub> 24   NC
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### Table 1. Product Portfolio

								Power	Dissipa	tion		
Product	Range	V	<sub>CC</sub> Range ('	V)	Speed Operating, I <sub>CC</sub> (mA)				A)	Standby, I <sub>SB2</sub> (μΑ)		
Floudet	Kalige				(ns)	f = 1 MHz		MHz f = f <sub>max</sub>		Stanuby	(μA)	
		Min	<b>Typ</b> <sup>[3]</sup>	Max		<b>Typ</b> <sup>[3]</sup>	Мах	<b>Typ</b> <sup>[3]</sup>	Max	<b>Typ</b> <sup>[3]</sup>	Max	
CY62126EV30LL	Industrial	2.2	3.0	3.6	45	1.3	2	11	16	1	4	
CY62126EV30LL	Automotive	2.2	3.0	3.6	55	1.3	4	11	35	1	30	

#### Notes

NC pins are not connected on the die.
 Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V<sub>CC</sub> = V<sub>CC(typ)</sub>, T<sub>A</sub> = 25°C.



### **Maximum Ratings**

Exceeding maximum ratings may shorten the battery life of the device. These user guidelines are not tested.

Storage Temperature65°C to +150°C
Ambient Temperature with Power Applied55°C to +125°C
Supply Voltage to Ground Potential0.3V to 3.6V (V <sub>CCmax</sub> + 0.3V)
DC Voltage Applied to Outputs in High-Z State <sup>[4, 5]</sup> –0.3V to 3.6V ( $V_{CCmax}$ + 0.3V)

DC Input Voltage <sup>[4, 5]</sup> –0.3V to 3.6V (V <sub>CCmax</sub>	+ 0.3V)
Output Current into Outputs (LOW)	20 mA
Static Discharge Voltage> (MIL-STD-883, Method 3015)	2001V
Latch up Current > 2	200 mA

## **Operating Range**

Device	Range	Ambient Temperature	<b>V</b> <sub>CC</sub> <sup>[6]</sup>
CY62126EV30LL	Industrial	–40°C to +85°C	2.2V to
	Automotive	–40°C to +125°C	3.6V

### Electrical Characteristics (Over the Operating Range)

Baramatar Description		Test Canditions	45	ns (Ind	ustrial)	55 ns (Automotive)			11
Parameter	Description	Test Conditions	Min	<b>Typ</b> <sup>[1]</sup>	Max	Min	<b>Typ</b> <sup>[1]</sup>	Max	Unit
V <sub>OH</sub>	Output HIGH Voltage	I <sub>OH</sub> = –0.1 mA	2.0			2.0			V
		I <sub>OH</sub> = −1.0 mA, V <sub>CC</sub> ≥ 2.70V	2.4			2.4			V
V <sub>OL</sub>	Output LOW Voltage	I <sub>OL</sub> = 0.1 mA			0.4			0.4	V
		I <sub>OL</sub> = 2.1mA, V <sub>CC</sub> ≥ 2.70V			0.4			0.4	V
V <sub>IH</sub>	Input HIGH Voltage	V <sub>CC</sub> = 2.2V to 2.7V	1.8		V <sub>CC</sub> +0.3	1.8		V <sub>CC</sub> +0.3	V
		V <sub>CC</sub> = 2.7V to 3.6V	2.2		V <sub>CC</sub> +0.3	2.2		V <sub>CC</sub> +0.3	V
V <sub>IL</sub>	Input LOW	V <sub>CC</sub> = 2.2V to 2.7V	-0.3		0.6	-0.3		0.6	V
	Voltage	V <sub>CC</sub> = 2.7V to 3.6V	-0.3		0.8	-0.3		0.8	V
I <sub>IX</sub>	Input Leakage Current	$GND \leq V_I \leq V_{CC}$	-1		+1	-4		+4	μA
I <sub>OZ</sub>	Output Leakage Current	GND ≤ V <sub>O</sub> ≤ V <sub>CC</sub> , Output Disabled	-1		+1	-4		+4	μA
I <sub>CC</sub>	V <sub>CC</sub> Operating Supply	$f = f_{max} = 1/t_{RC}$ $V_{CC} = V_{CCmax}$		11	16		11	35	mA
	Current	f = 1 MHz I <sub>OUT</sub> = 0 mA CMOS levels		1.3	2.0		1.3	4.0	
I <sub>SB1</sub>	Automatic CE Power down Current —CMOS Inputs	$\label{eq:central_constraints} \begin{split} \overline{CE} &\geq V_{CC} - 0.2V, \\ V_{IN} &\geq V_{CC} - 0.2V, \ V_{IN} &\leq 0.2V) \\ f &= f_{max} (Address and Data Only) \\ f &= 0 (OE, \overline{BHE}, \overline{BLE} and \overline{WE}), \\ V_{CC} &= 3.60V \end{split}$	,	1	4		1	35	μΑ
I <sub>SB2</sub> <sup>[7]</sup>	down Current	$\label{eq:central_constraint} \begin{split} \overline{CE} &\geq V_{CC} - 0.2V, \\ V_{\text{IN}} &\geq V_{CC} - 0.2V \text{ or } V_{\text{IN}} \leq 0.2V, \\ f &= 0, \ V_{CC} = 3.60V \end{split}$		1	4		1	30	μΑ

### Capacitance

For all packages. Tested initially and after any design or process changes that may affect these parameters.

Parameter	Description	Test Conditions	Max	Unit
C <sub>IN</sub>	Input Capacitance	$T_A = 25^{\circ}C$ , f = 1 MHz, $V_{CC} = V_{CC(typ)}$	10	pF
C <sub>OUT</sub>	Output Capacitance		10	pF

### Notes

V<sub>IL(min)</sub> = -2.0V for pulse durations less than 20 ns.
 V<sub>IL(min)</sub> = V<sub>CC</sub>+0.75V for pulse durations less than 20 ns.
 V<sub>IH(max)</sub> = V<sub>CC</sub>+0.75V for pulse durations less than 20 ns.
 Full device AC operation assumes a 100 μs ramp time from 0 to V<sub>cc</sub>(min) and 200 μs wait time after V<sub>cc</sub> stabilization.
 Only chip enable (CE) and byte enables (BHE and BLE) need to be tied to CMOS levels to meet the I<sub>SB2</sub> / I<sub>CCDR</sub> spec. Other inputs can be left floating.

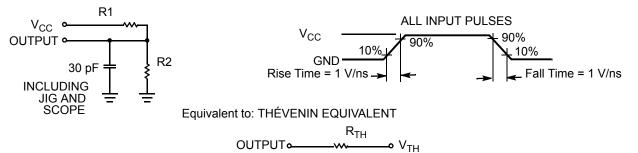


### **Thermal Resistance**

Tested initially and after any design or process changes that may affect these parameters.

Parameter	Description	Test Conditions	VFBGA Package	TSOP II Package	Unit
$\Theta_{JA}$		Still Air, soldered on a 4.25 x 1.125 inch, two-layer printed circuit board	58.85	28.2	°C/W
Θ <sub>JC</sub>	Thermal Resistance (Junction to Case)		17.01	3.4	°C/W

### Figure 3. AC Test Loads and Waveforms



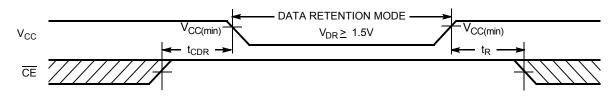
Parameters	2.2V - 2.7V	2.7V - 3.6V	Unit
R1	16600	1103	Ohms
R2	15400	1554	Ohms
R <sub>TH</sub>	8000	645	Ohms
V <sub>TH</sub>	1.2	1.75	Volts

# **Data Retention Characteristics**

Over the Operating Range

Parameter	Description	Conditions	Min	<b>Typ</b> <sup>[1]</sup>	Max	Unit	
V <sub>DR</sub>	V <sub>CC</sub> for Data Retention			1.5			V
I <sub>CCDR</sub> <sup>[7]</sup>	Data Retention Current	$V_{CC} = V_{DR}, \overline{CE} \ge V_{CC} - 0.2V,$ $V_{IN} \ge V_{CC} - 0.2V \text{ or } V_{IN} \le 0.2V$	Industrial			3	μA
		$V_{IN} \ge V_{CC} - 0.2V \text{ or } V_{IN} \le 0.2V$	Automotive			30	μA
t <sub>CDR</sub> <sup>[8]</sup>	Chip Deselect to Data Retention Time			0			ns
t <sub>R</sub> <sup>[9]</sup>	Operation Recovery Time			t <sub>RC</sub>			ns

### Figure 4. Data Retention Waveform



#### Notes

8. Tested initially and after any design or process changes that may affect these parameters.

9. Full device AC operation requires linear V<sub>CC</sub> ramp from V<sub>DR</sub> to V<sub>CC(min)</sub> > 100  $\mu$ s.

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### **Switching Characteristics**

Over the Operating Range [10, 11]

Demonstern	Description	45 ns (li	ndustrial)	55 ns (Au	utomotive)	11
Parameter	Description	Min	Max	Min	Max	Unit
Read Cycle	·	•	•			
t <sub>RC</sub>	Read Cycle Time	45		55		ns
t <sub>AA</sub>	Address to Data Valid		45		55	ns
t <sub>OHA</sub>	Data Hold from Address Change	10		10		ns
t <sub>ACE</sub>	CE LOW to Data Valid		45		55	ns
t <sub>DOE</sub>	OE LOW to Data Valid		22		25	ns
t <sub>LZOE</sub>	OE LOW to Low Z <sup>[12]</sup>	5		5		ns
t <sub>HZOE</sub>	OE HIGH to High Z <sup>[12, 13]</sup>		18		20	ns
t <sub>LZCE</sub>	CE LOW to Low Z <sup>[12]</sup>	10		10		ns
t <sub>HZCE</sub>	CE HIGH to High Z <sup>[12, 13]</sup>		18		20	ns
t <sub>PU</sub>	CE LOW to Power Up	0		0		ns
t <sub>PD</sub>	CE HIGH to Power Down		45		55	ns
t <sub>DBE</sub>	BHE / BLE LOW to Data Valid		22		25	ns
t <sub>LZBE</sub>	BHE / BLE LOW to Low Z <sup>[12]</sup>	5		5		ns
t <sub>HZBE</sub>	BHE / BLE HIGH to High Z [12, 13]		18		20	ns
Write Cycle [14]	· ·					
t <sub>WC</sub>	Write Cycle Time	45		55		ns
t <sub>SCE</sub>	CE LOW to Write End	35		40		ns
t <sub>AW</sub>	Address Setup to Write End	35		40		ns
t <sub>HA</sub>	Address Hold from Write End	0		0		ns
t <sub>SA</sub>	Address Setup to Write Start	0		0		ns
t <sub>PWE</sub>	WE Pulse Width	35		40		ns
t <sub>BW</sub>	BHE / BLE Pulse Width	35		40		ns
t <sub>SD</sub>	Data Setup to Write End	25		25		ns
t <sub>HD</sub>	Data Hold from Write End	0		0		ns
t <sub>HZWE</sub>	WE LOW to High Z <sup>[12, 13]</sup>		18		20	ns
t <sub>LZWE</sub>	WE HIGH to Low Z <sup>[12]</sup>	10		10		ns

Notes

10. Test conditions assume signal transition time of 3 ns or less, timing reference levels of V<sub>CC(typ</sub>)/2, input pulse levels of 0 to V<sub>CC(typ</sub>), and output loading of the specified I<sub>OL</sub>/I<sub>OH</sub> and 30-pF load capacitance.

11. AC timing parameters are subject to byte enable signals (BHE or BLE) not switching when chip is disabled. See application note AN13842 for further clarification.

12. At any temperature and voltage condition, t<sub>HZCE</sub> is less than t<sub>LZCE</sub>, t<sub>HZBE</sub> is less than t<sub>LZDE</sub>, t<sub>HZCE</sub> is less than t<sub>LZDE</sub>, and t<sub>HZWE</sub> transitions are measured when the <u>outputs</u> enter a high impedance state.
 13. t<sub>HZOE</sub>, t<sub>HZCE</sub>, t<sub>HZDE</sub>, and t<sub>HZWE</sub> transitions are measured when the <u>outputs</u> enter a high impedance state.
 14. The internal write time of the memory is defined by the overlap of WE, CE = V<sub>IL</sub>, BHE, BLE or both = V<sub>IL</sub>. All signals must be active to initiate a write and any of these signals can terminate a write by going inactive. The data input setup and hold timing must refer to the edge of signal that terminates write.



### **Switching Waveforms**

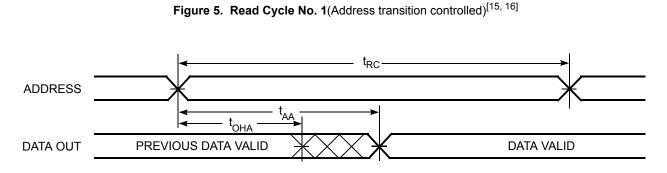
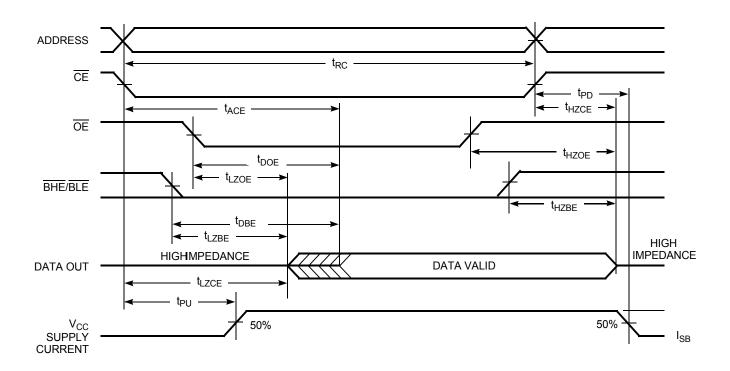


Figure 6. Read Cycle No. 2 (OE controlled)<sup>[16, 17]</sup>



#### Notes

15. The device is continuously selected.  $\overline{OE}$ ,  $\overline{CE} = V_{IL}$ ,  $\overline{BHE}$ ,  $\overline{BLE}$ , or both =  $V_{IL}$ . 16.  $\overline{WE}$  is HIGH for read cycle.

17. Address valid before or similar to  $\overline{CE}$  and  $\overline{BHE}$ ,  $\overline{BLE}$  transition LOW.



### Switching Waveforms (continued)

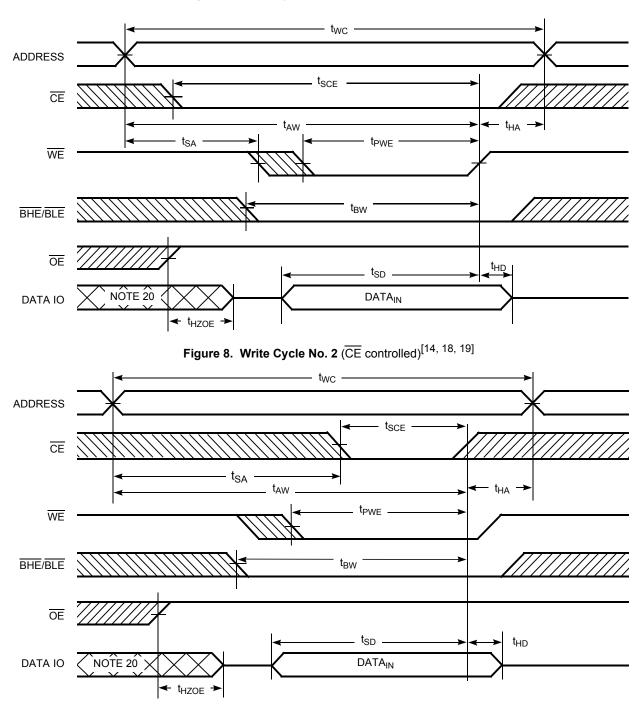


Figure 7. Write Cycle No. 1 (WE controlled)<sup>[14, 18, 19]</sup>

#### Notes

18. Data IO is high impedance if  $\overline{OE} = V_{|H|}$ . 19. If  $\overline{CE}$  goes HIGH simultaneously with WE =  $V_{|H|}$ , the output remains in a high impedance state. 20. During this period, the IOs are in output state. Do not apply input signals.



# Switching Waveforms (continued)

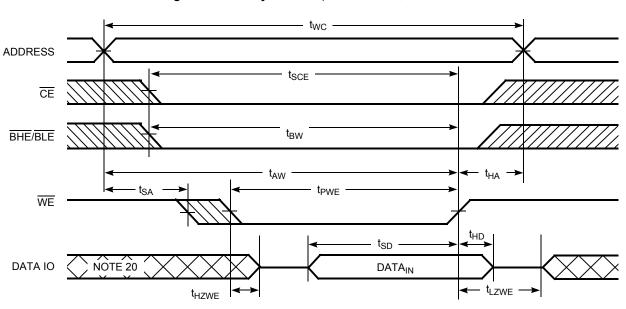
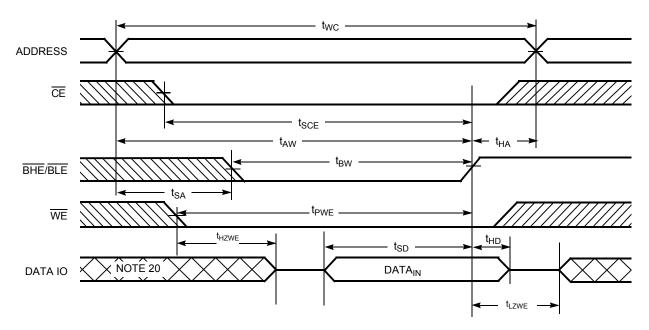


Figure 9. Write Cycle No. 3 ( $\overline{\text{WE}}$  controlled,  $\overline{\text{OE}}$  LOW <sup>[19]</sup>

Figure 10. Write Cycle No. 4  $(\overline{\text{BHE/BLE}} \text{ controlled}, \overline{\text{OE}} \text{ LOW})^{[19]}$ 







### **Truth Table**

CE	WE	OE	BHE	BLE	Inputs/Outputs	Mode	Power
Н	Х	Х	Х	Х	High Z	h Z Deselect/Power Down	
L	Х	Х	Н	Н	High Z	Output Disabled	Active (I <sub>CC</sub> )
L	Н	L	L	L	Data Out (IO <sub>0</sub> –IO <sub>15</sub> )	Read	Active (I <sub>CC</sub> )
L	Н	L	Н	L	Data Out (IO <sub>0</sub> –IO <sub>7</sub> ); IO <sub>8</sub> –IO <sub>15</sub> in High Z	Read	Active (I <sub>CC</sub> )
L	Н	L	L	Н	Data Out (IO <sub>8</sub> –IO <sub>15</sub> ); IO <sub>0</sub> –IO <sub>7</sub> in High Z	Read	Active (I <sub>CC</sub> )
L	Н	Н	L	L	High Z	Output Disabled	Active (I <sub>CC</sub> )
L	Н	Н	Н	L	High Z	Output Disabled	Active (I <sub>CC</sub> )
L	Н	Н	L	Н	High Z	Output Disabled	Active (I <sub>CC</sub> )
L	L	Х	L	L	Data In (IO <sub>0</sub> –IO <sub>15</sub> )	Write	Active (I <sub>CC</sub> )
L	L	Х	Н	L	Data In (IO <sub>0</sub> –IO <sub>7</sub> ); IO <sub>8</sub> –IO <sub>15</sub> in High Z	Write	Active (I <sub>CC</sub> )
L	L	Х	L	Н	Data In (IO <sub>8</sub> –IO <sub>15</sub> ); IO <sub>0</sub> –IO <sub>7</sub> in High Z	Write	Active (I <sub>CC</sub> )

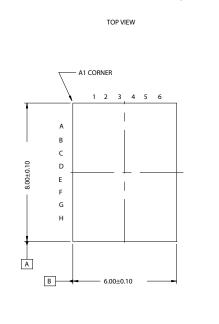
# **Ordering Information**

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
45	CY62126EV30LL-45BVXI	51-85150	48-ball Very Fine Pitch Ball Grid Array (Pb-free)	Industrial
	CY62126EV30LL-45ZSXI	51-85087	44-pin Thin Small Outline Package II (Pb-free)	
55	CY62126EV30LL-55BVXE	51-85150	48-ball Very Fine Pitch Ball Grid Array (Pb-free)	Automotive
	CY62126EV30LL-55ZSXE	51-85087	44-pin Thin Small Outline Package II (Pb-free)	

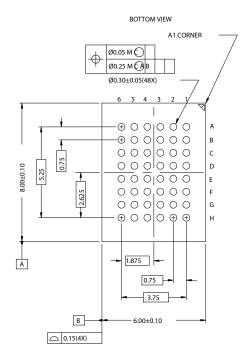
Contact your local Cypress sales representative for availability of other parts.

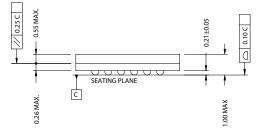


# Package Diagrams







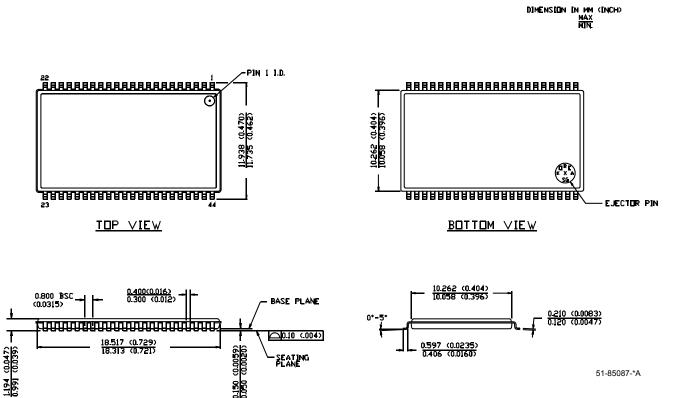


51-85150-\*D



### Package Diagrams (continued)

Figure 12. 44-Pin TSOP II (51-85087)



51-85087-\*A





# **Document History Page**

Rev.	ECN No.	Submission Date	Orig. of Change	Description of Change	
**	202760	See ECN	AJU	New data sheet	
*A	300835	See ECN	SYT	Converted from Advance Information to Preliminary Specified Typical standby power in the Features Section Changed E3 ball from DNU to NC in the Pin Configuration for the FBGA Package and removed the footnote associated with it on page #2 Changed $t_{OHA}$ from 6 ns to 10 ns for both 35- and 45-ns speed bins, respectively Changed $t_{DOE}$ , $t_{SD}$ from 15 to 18 ns for 35-ns speed bin Changed $t_{HZOE}$ , $t_{HZBE}$ , $t_{HZWE}$ from 12 and 15 ns to 15 and 18 ns for the 35- and 45-ns speed bins, respectively Changed $t_{HZCE}$ from 12 and 15 ns to 18 and 22 ns for the 35- and 45-ns speed bins, respectively Changed $t_{SCE}$ , $t_{BW}$ from 25 and 40 ns to 30 and 35 ns for the 35- and 45-ns speed bins, respectively Changed $t_{SCE}$ , $t_{BW}$ from 25 to 30 ns and 40 to 35 ns for 35 and 45-ns speed bins respectively Changed $t_{DBE}$ from 35 and 45 ns to 18 and 22 ns for the 35- and 45-ns speed bins, respectively Changed $t_{DBE}$ from 35 and 45 ns to 18 and 22 ns for the 35 and 45 ns speed bins respectively Changed $t_{DBE}$ from 35 and 45 ns to 18 and 22 ns for the 35 and 45 ns speed bins respectively Removed footnote that read "BHE.BLE is the AND of both BHE and BLE. Chip car be deselected by either disabling the chip enable signals or by disabling both BHE and BLE" on page # 4 Removed footnote that read "If both BHE and BLE are toggled together, then $t_{LZB}$ is 10 ns" on page # 5 Added Pb-free package information	
*В	461631	See ECN	NXR	Converted from Preliminary to Final Removed 35 ns Speed Bin Removed "L" version of CY62126EV30 Changed $I_{CC (Typ)}$ from 8 mA to 11 mA and $I_{CC (max)}$ from 12 mA to 16 mA for f = f <sub>ma</sub> Changed $I_{CC (max)}$ from 1.5 mA to 2.0 mA for f = 1 MHz Changed $I_{SB1}$ , $I_{SB2 (max)}$ from 1 $\mu$ A to 4 $\mu$ A Changed $I_{SB1}$ , $I_{SB2 (Typ)}$ from 0.5 $\mu$ A to 1 $\mu$ A Changed $I_{CCDR (max)}$ from 1.5 $\mu$ A to 3 $\mu$ A Changed the AC Test load Capacitance value from 50 pF to 30 pF Changed t <sub>LZCE</sub> from 3 to 5 ns Changed $I_{LZCE}$ from 6 to 10 ns Changed $I_{LZEE}$ from 6 to 5 ns Changed $I_{EXE}$ from 6 to 5 ns Changed $I_{SD}$ from 22 to 25 ns Changed $I_{LZWE}$ from 6 to 10 ns Updated the Ordering Information table.	
*C	925501	See ECN	VKN	Added footnote #7 related to I <sub>SB2</sub> and I <sub>CCDR</sub> Added footnote #11 related AC timing parameters	
*D	1045260	See ECN	VKN	Added Automotive information Updated Ordering Information table	
*E	2631771	01/07/09	NXR/PYRS	Changed $\overline{CE}$ condition from X to L in Truth table for Output Disable mode Updated template	



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