DATA BRIEF **CY7C68003**

MoBL-USB™ TX2UL USB 2.0 ULPI Transceiver

Features

The Cypress MoBL-USB™ TX2UL is a low voltage high speed (HS) USB 2.0 ULPI Transceiver.

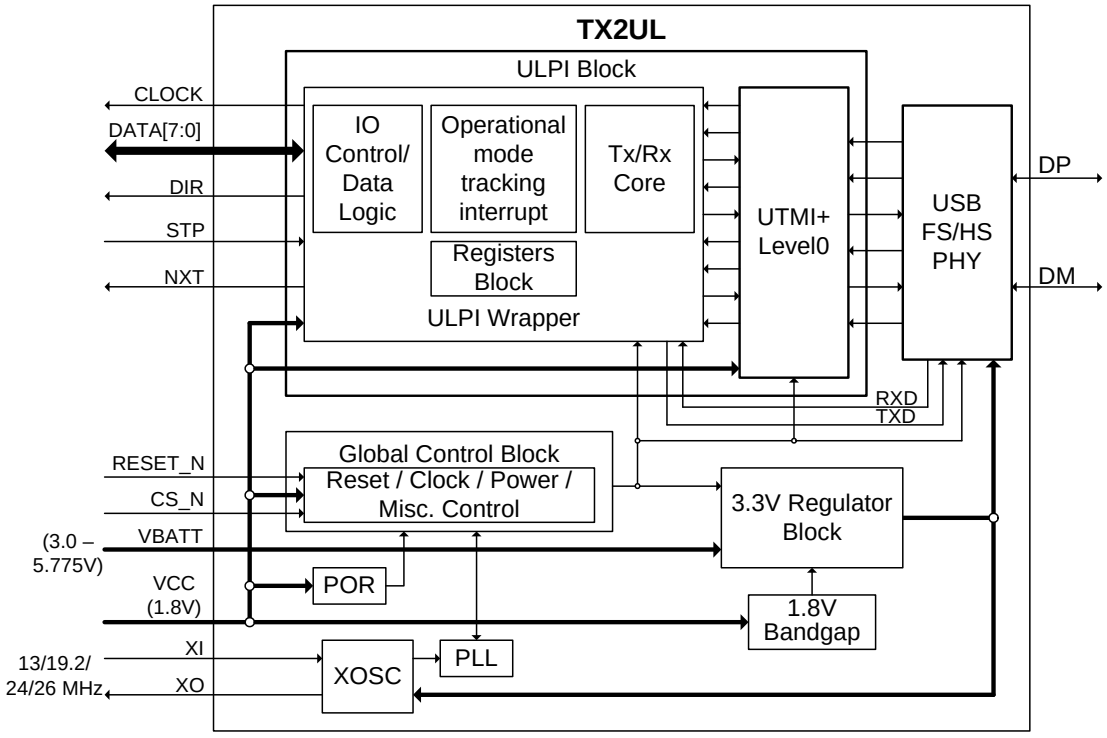
The TX2UL is specifically designed for mobile handset applications by offering tiny package options and low power consumption.

- USB 2.0 Full Speed and High Speed Compliant Transceiver
- Multi-Range (1.8V to 3.3V) IO Voltages
- Fully Compliant ULPI Link Interface
- 8-bit SDR ULPI Data Path
- UTMI+ Level 0 Support
- Integrated Oscillator
- Integrated PLL (13, 19.2, 24, or 26 MHz Reference)
- Integrated USB Pull Up and Termination Resistors
- 3.0V to 5.775V VBATT Input
- Chip Select Pin
- Single Ended Device RESET Input
- UART Pass Through Mode
- ESD Compliance:
  - JESD22-A114D 8 kV Contact Human Body Model (HBM) for DP, DM, and VSS Pins
  - IEC61000-4-2 8 kV Contact Discharge
  - IEC61000-4-2 15 kV Air Discharge
- Support for Industrial Temperature Range (-40°C to 85°C)
- Low Power Consumption for Mobile Applications:
  - 5 uA Nominal Sleep Mode
  - 30 mA Nominal Active HS Transfer
- Small Package for Mobile Applications:
  - 2.14 x 1.76 mm 20-pin WLCSP 0.4 mm Pitch
  - 4 x 4 mm 24-pin QFN

Applications

- Mobile Phones
- PDAs
- Portable Media Players (PMPs)
- DTV Applications
- Portable GPS Units

TX2UL Block Diagram



Functional Overview

UTMI+ Low Pin Interface (ULPI)

This block conforms to the ULPI Specification. It supports the 8-bit wide SDR data path. The primary IOs of this block support multi-range LVCMOS signaling from 1.8V to 3.3V (±5%). The level used is automatically selected by the voltage applied to Vccio and is set at any voltage between 1.8V and 3.3V.

Oscillator (OSC)

This block meets the requirements of both the on-chip PLL and the USB-IF requirements for clock parameters. It is a fundamental mode parallel resonant oscillator with a maximum ESR of 60 ohms. It supports the following:

- Integrated Crystal Oscillator - 13, 19.2, 24, or 26 MHz crystal
- 13, 19.2, 24, or 26 MHz LVCMOS single ended input clock on XI

Phase Locked Loop (PLL)

The PLL meets all clock stability requirements imposed by this device and the USB standard. It supports all requirements to make the device compliant to the USB 2.0 specifications. It also has a fractional multiplier that enables it to supply the correct frequency to the device when it is presented with a 13, 19.2, 24, or 26 MHz reference clock.

Power On Reset (POR)

This block provides a power on reset signal (internal) based on the input supply. An internal power on reset is generated when VCC input rises above VPOR(trip).

Reset (RESET_N)

The three major functions of RESET_N pin are as follows:

- Reset TX2UL
- Place TX2UL into Sleep Mode
- Place TX2UL into Configuration Mode

When the RESET_N pin is asserted (low) for tSTATE (tSTATE is specified in Table 21 on page 19), the TX2UL enters into either Sleep Mode or Configuration Mode depending on the CS_N state. When RESET_N is asserted while CS_N is asserted, TX2UL enters into Sleep Mode. When RESET_N is asserted for tSTATE while CS_N is deasserted, TX2UL enters into Configuration Mode. In these modes, all the pins in the ULPI interface are tri-stated. If the RESET_N pin is not used, it must be pulled high. For more information about different modes of configuration, see Table 5 on page 4.

DP and DM pins

The DP and DM pins are the differential pins for the USB. They must be connected to the corresponding DP and DM pins of the USB receptacle.

Chip Select (CS_N)

This signal pin is available only in 24-pin QFN package. The two major functions of CS_N are as follows:

- Tri-state the ULPI bus output pins
- Associate with RESET_N to place TX2UL in the Sleep mode

When the CS_N pin is deasserted (high), all the pins in the ULPI interface are tri-stated.

USB2 Transceiver Macrocell Interface (UTMI+)

This block conforms to the UTMI+ Level 0 standard. It performs all the UTMI to USB translation.

Global Control

This block is the digital control logic that ties the blocks of the device together. Functions performed include pull up control, over current protect control, and more.

Full Speed and High Speed USB Transceivers (FS/HS)

The FS and HS Transceivers comply fully with the USB 2.0 specifications.

USB Pull up and Intr Detect, Termination Resistors (Pull up / TERM)

These blocks contain the USB pull up and termination resistors as specified by the USB 2.0 specification.

UART Pass Through Mode

TX2UL supports Carkit UART Pass Through Mode. When the Carkit Mode bit in the Interface Control register is set, it enables the Link to communicate through the DP/DM to a remote system using UART signaling. By default, the clock is powered down when the TX2UL enters Carkit Mode. Entering and exiting the Carkit Mode is identical to the Serial Mode. Table 1, Table 2, and Figure 1 show the UART Signal Mapping between the DP/DM and DATA[1:0] at ULPI interface.

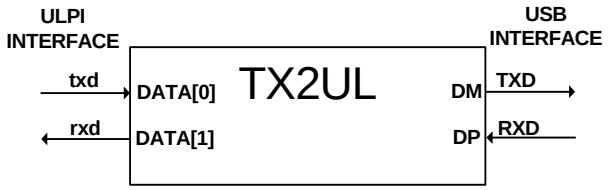
Table 1. UART Signal Mapping at ULPI Interface

Signal	Maps to	Direction	Description
txd	DATA[0]	IN	UART TXD signal routed to DM pin
rxd	DATA[1]	OUT	UART RXD signal routed to DP pin
Reserved	DATA[7:2]	-	Reserved

Table 2. UART Signal Mapping at USB Interface

Signal	Maps to	Direction	Description
TXD	DM	OUT	UART TXD signal
RXD	DP	INT	UART RXD signal

Figure 1. UART Signal Mapping in Pass Through Mode



Clocking

TX2UL supports external crystal and clock inputs at the 13, 19.2, 24, and 26 MHz frequencies. The internal PLL applies the proper clock multiply option depending on the input frequency. For applications that use an external clock source to drive XI, the XO pin (in 24-pin QFN package) is left floating. TX2UL has an on-chip oscillator circuit that uses an external 13, 19.2, 24, or 26 MHz (±100 ppm) crystal with the following characteristics:

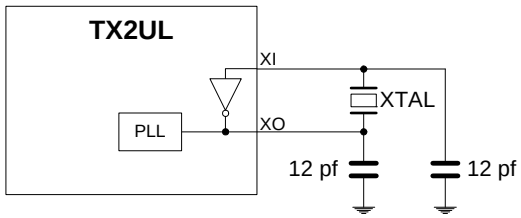
- Parallel Resonant
- Fundamental Mode
- 750 mW Drive Level
- 12 pF (5 percent tolerance) Load Capacitors
- 150 ppm

TX2UL operates on one of two primary clock sources:

- LVCMOS square wave clock input driven on the XI pin
- Crystal generated sine wave clock on the XI and XO pins

The selection between input clock source and frequency on the XI pin is determined by the *Chip Configuration* register loaded through the RESET_N during Configuration Mode. The external clock source requirements are shown in Figure 3 on page 4.

Figure 2. Crystal Configuration



* 12 pF capacitor values assumes a trace capacitance of 3 pF per side on a four layer FR4 PCA

Table 3. External Clock Requirements

Parameter	Description	Specification		Unit
		Min	Max	
Vn	Supply Voltage Noise at frequencies < 50 MHz		20	mV p-p
PN_100	Input Phase Noise at 100 Hz		–75	dBc/Hz
PN_1k	Input Phase Noise at 1 kHz offset		–104	dBc/Hz
PN_10k	Input Phase Noise at 10 kHz offset		–120	dBc/Hz
PN_100k	Input Phase Noise at 100 kHz offset		–128	dBc/Hz
PN_1M	Input Phase Noise at 1 MHz offset		–130	dBc/Hz
	Duty Cycle	30	70	%
	Maximum Frequency Deviation		150	ppm

Power Domains

The TX2UL has three power supply domains:

- VCC
- VIO
- VBATT

TX2UL has two grounds:

- VSS
- VSSBATT

VCC

This is the core 1.8V power supply for the TX2UL. It can range anywhere from 1.7V to 1.9V during actual operation.

VIO

This is the 1.8V to 3.3V multi range supply to the I/O ring. It can range anywhere from 1.7V to 3.6V during actual operation.

VBATT

This is the battery input supply that powers the 3.3V Regulator block. It can range anywhere from 3.0 to 5.775V during actual operation.

Voltage Regulator

The internal 3.3V regulator block regulates the VBATT supply to the internal 3.3V supply for the USBIO and XOSC blocks. If the supply voltage at VBATT is below 3.3V, the regulator block switches the VBATT supply directly for the USBIO and XOSC blocks.

Power Supply Sequence

TX2UL does not require power supply sequence. All power supplies are independently sequenced without damaging the part. All supplies are up and stable for the device to function properly. The analog block contains circuitry that senses the power supply to determine when all supplies are valid.

Operation Modes

There are six operation modes available in TX2UL. They are:

- Normal Operation Mode
- Configuration Mode
- ULPI Low Power Mode
- Sleep Mode
- Carkit UART Pass Through Mode
- Tri-state ULPI Interface Output Mode (only available in 24-pin QFN package)

When changing the operation modes, if the current and changing modes are not the Normal Operation Mode, TX2UL first changes to the Normal Operation Mode. For example, to change from ULPI Low power mode to Sleep mode, TX2UL changes to Normal operation mode first, and then changes to Sleep mode. The Mode Change State diagram in Figure 3 shows the mode change path of TX2UL. The entries of the six operations modes (20-pin CSP package has 5 operation modes) are listed in Table 4 and Table 5. There are three mode change transactions that require the RESET_N assert or deassert with tSTATE (see Table 21 on page 19 for tSTATE). These three mode change transactions are:

- Change from Normal Operation Mode to Configuration Mode – RESET_N is required to assert with tSTATE
- Change from Configuration Mode to Normal Operation Mode – RESET_N is required to de-assert with tSTATE
- Change from Normal Operation Mode to Sleep Mode – RESET_N is required to assert with tSTATE

Figure 3. Mode Change State Diagram

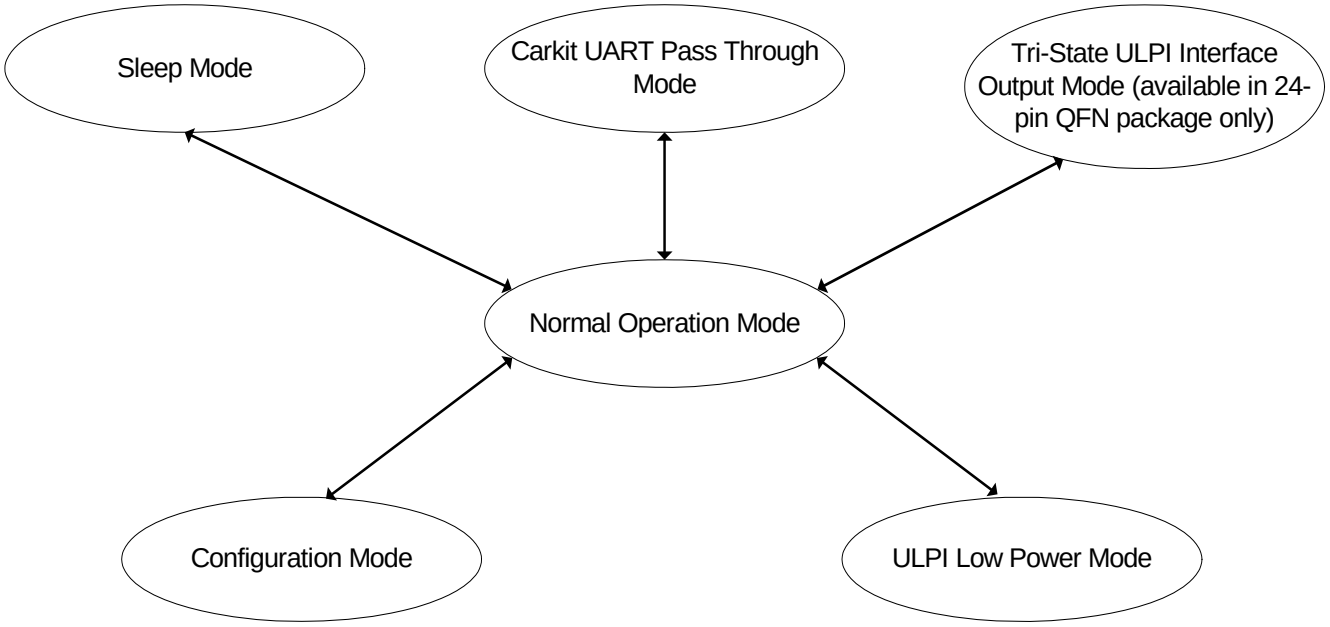


Table 4. TX2UL 20-Pin CPS Package Operation Modes

RESET_N	Mode
0 (Low)	Sleep Mode
1 (High)	Normal Operation Mode
1 (High)	Enter into ULPI Low Power Mode by setting SuspendM register bit (in Function Control Register) to 0 during the Normal Operation Mode.
1 (High)	Enter into Carkit UART Pass Through Mode by setting Carkit Mode register bit (in Interface Control Register) to 1 during the Normal Operation Mode.
0 (Low) when Power On (VCC On)	Enter into Configuration Mode

Table 5. TX2UL 24-Pin QFN Package Operation Modes

CS_N	RESET_N	Mode
0 (Low)	0 (Low)	Sleep Mode
0 (Low)	1 (High)	Normal Operation Mode
0 (Low)	1 (High)	Enter into ULPI Low Power Mode by setting SuspendM register bit (in Function Control Register) to 0 during the Normal Operation Mode.
0 (Low)	1 (High)	Enter into Carkit UART Pass Through Mode by setting Carkit Mode register bit (in Interface Control Register) to 1 during the Normal Operation Mode.
1 (High)	0 (Low)	Configuration Mode
1 (High)	1 (High)	Tri-state ULPI Interface output pins

The operation and configuration modes are described in Operation Modes on page 4 and Configuration Mode on page 14 respectively. The ULPI Low power mode and Sleep mode are described in the following sections:

ULPI Low Power Mode

In this mode, the link optionally places the TX2UL in low power mode when the USB is suspended. TX2UL powers down all the circuitry except for the interface pins and full speed receiver. To enter low power mode, the link must set SuspendM in the Function Control register to 0b. The TX2UL clock is stopped for a minimum of five cycles after TX2UL accepts the register write. To exit the low power mode, the link signals TX2UL to exit the mode by asynchronously asserting a signal, STP. The TX2UL wakes up its internal circuitry and when it meets the ULPI timing requirements it deasserts DIR. The SuspendM register is set to 1b.

Sleep Mode

Sleep mode is entered by asserting RESET_N during the Normal Operation Mode. When RESET_N is driven low for tSTATE (see Table 21 on page 19 for tSTATE requirement) while CS_N is low, TX2UL enters into Sleep Mode. VCC must remain supplied (ON) during the sleep mode. This mode powers down all internal circuitry except the RESET_N pin and the chip_config register. The ULPI interface bus is tri-stated.

During the Sleep Mode ensure that:

- The ULPI interface IOs is either floating or driven high by the link
- DP and DM are either floating or pull to 0V
- Deassert RESET_N to exit the Sleep Mode.

VID and PID

The VID and PID are hard coded into Product ID and Vendor ID registers (read only) as shown in Table 6.

Table 6. Immediate Register Values for VID and PID

Field Name	Size (bit)	Address (6 bits)				Value
		Rd	Wr	Set	Clr	
Vendor ID (VID) Low	8	00h	-	-	-	B4h
Vendor ID (VID) High	8	01h	-	-	-	04h
Product ID (PID) Low	8	02h	-	-	-	03h
Product ID (PID) High	8	03h	-	-	-	68h