

CY24713

Set-top Box Clock Generator with VCXO

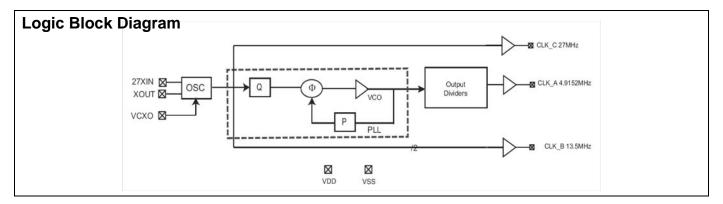
Features

- Integrated phase-locked loop (PLL)
- Low-jitter, high-accuracy outputs
- VCXO with analog adjust
- 3.3V Operation
- 8-pin SOIC

Benefits

- High-performance PLL tailored for Set Top Box applications
- Meets critical timing requirements in complex system designs
- Large ±150-ppm range, better linearity
- Meet industry standard voltage platforms
- Industry standard packaging saves on board space

Part Number	Outputs	Input Frequency Range	Output Frequencies
CY24713	3	27-MHz pullable crystal input per Cypress specification	4.9152 MHz, 13.5 MHz, 27 MHz



Pin Configuration

Figure 1. CY24713, 8-Pin SOIC

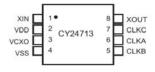


Table 1. Pin Definition

Name	Number	Description	
XIN	1	Reference Crystal Input	
VDD	2	3.3V Voltage Supply	
VCXO	3	Input Analog Control for VCXO	
VSS	4	Ground	
CLK_B	5	13.5-MHz Clock Output	
CLK_A	6	4.9152-MHz Clock Output	
CLK_C	7	27-MHz Clock Output	
XOUT ^[1]	8	Reference Crystal Output	

Note

1. Float X_{OUT} if X_{IN} is externally driven.

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San Jose, CA 95134-1709

• 408-943-2600 Revised May 22, 2008



Absolute Maximum Conditions

Parameter	Description	Min	Max	Unit
V _{DD}	Supply Voltage	-0.5	7.0	V
Τ _S	Storage Temperature ^[2]	-65	125	°C
TJ	Junction Temperature	-	125	°C
	Digital Inputs	V _{SS} – 0.3	V _{DD} + 0.3	V
	Digital Outputs referred to V _{DD}	V _{SS} – 0.3	V _{DD} + 0.3	V
	Electrostatic Discharge	-	2000	V
	Analog Input	-0.5	7.0	V

Pullable Crystal Specifications

Parameter	Description	Condition	Min	Тур.	Max	Unit
F _{NOM}	Nominal crystal frequency	Parallel resonance, funda- mental mode, AT cut	_	27	-	MHz
C _{LNOM}	Nominal load capacitance		-	14	-	pF
R ₁	Equivalent series resistance (ESR)	Fundamental mode	-	-	25	Ω
R ₃ /R ₁	Ratio of third overtone mode ESR to fundamen- tal mode ESR	Ratio used because typical R ₁ values are much less than the maximum spec.	3	-	-	
DL	Crystal drive level	No external series resistor as- sumed	_	0.5	2.0	mW
F _{3SEPHI}	Third overtone separation from 3*F _{NOM}	High side	300	-	-	ppm
F _{3SEPLO}	Third overtone separation from 3*F _{NOM}	Low side	-	-	-150	ppm
C ₀	Crystal shunt capacitance		-	-	7	pF
C ₀ /C ₁	Ratio of shunt to motional capacitance		180	-	250	
C ₁	Crystal motional capacitance		14.4	18	21.6	pF

Recommended Operating Conditions

Parameter	Description	Min	Тур.	Max	Unit
V _{DD}	Operating Voltage	3.135	3.3	3.465	V
T _A	Ambient Temperature	0	-	70	°C
C _{LOAD}	Max. Load Capacitance	-	-	15	pF
t _{PU}	Power up time for all VDDs to reach minimum specified voltage (power ramps must be monotonic)	0.05	_	500	ms

DC Electrical Characteristics

Parameter	Description	Conditions	Min	Тур.	Max	Unit
I _{ОН}	Output High Current	$V_{OH} = V_{DD} - 0.5, V_{DD} = 3.3V$	12	24	_	mA
I _{OL}	Output Low Current	V _{OL} = 0.5, V _{DD} = 3.3V	12	24	-	mA
C _{IN}	Input Capacitance		-	-	7	pF
I _{IZ}	Input Leakage Current		-	5	-	μA
f _{∆XO}	VCXO pullability range		±150	-	-	ppm
V _{VCXO}	VCXO input range		0	-	V _{DD}	V
I _{VDD}	Supply Current		_	25	30	mA

Note

2. Rated for 10 years



AC Electrical Characteristics (V_{DD} = 3.3V)

Parameter ^[3]	Description	Conditions	Min	Тур.	Max	Unit
DC	Output Duty Cycle	Duty Cycle is defined in Figure 3 50% of V _{DD}	45	50	55	%
ER ₀	Rising Edge Rate	Output Clock Edge Rate, Measured from 20% to 80% of V_{DD} , C_{LOAD} = 15 pF Figure 4.	0.8	1.4	-	V/ns
EF ₁	Falling Edge Rate	Output Clock Edge Rate, Measured from 80% to 20% of V_{DD} , C_{LOAD} = 15 pF Figure 4.	0.8	1.4	-	V/ns
t ₉	Clock Jitter	Peak-Peak period jitter maximum absolute jitter	-	200	250	ps
t ₁₀	PLL Lock Time		-	-	3	ms

Figure 2. Test Circuit

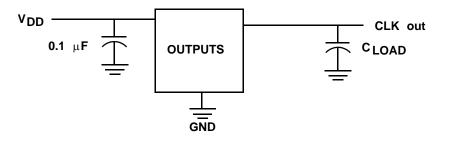


Figure 3. Duty Cycle Definition; DC = t2/t1

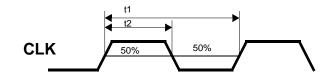
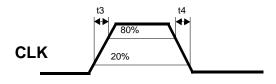


Figure 4. Rise and Fall Time Definitions: ER = 0.6 x V_{DD} /t3, EF = 0.6 x V_{DD} /t4



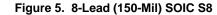
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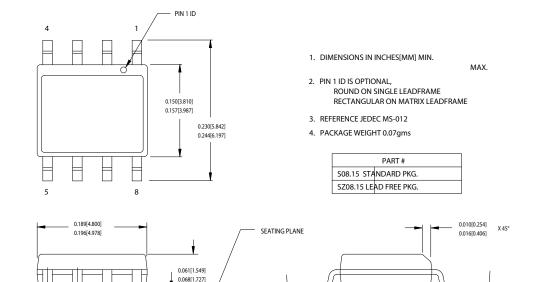


Ordering Information

Ordering Code	Package Type	Operating Range	Operating Voltage
CY24713SC ^[4]	8-pin SOIC	Commercial	3.3V
CY24713SCT ^[4]	8-pin SOIC	Commercial	3.3V
Pb-free			
CY24713SXC ^[4]	8-pin SOIC	Commercial	3.3V
CY24713SXCT ^[4]	8-pin SOIC-Tape and Reel	Commercial	3.3V
CY24713KSXC	8-pin SOIC	Commercial	3.3V
CY24713KSXCT	8-pin SOIC-Tape and Reel	Commercial	3.3V

Package Diagram





0.004[0.102]

0°~8°

0.016[0.406]

0.035[0.889]

51-85066 *C

0.004[0.102]

0.0098[0.249]

0.0138[0.350] 0.0192[0.487]

0.050[1.270]

BSC

0.0075[0.190]

0.0098[0.249]



Document History Page

Document Title: CY24713 Set-top Box Clock Generator with VCXO Document Number: 38-07396								
REV.	ECN No.	Orig. of Change	Submission Date	Description of Change				
**	333175	RGL	See ECN	New Data Sheet				
*A	2440886	AESA	See ECN	Updated template. Added Note "Not recommended for new designs." Added part number CY24713KSXC, and CY24713KSXCT in ordering infor- mation table. Replaced Lead-Free with Pb-Free.				

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