

## Product Specification

### 1000BASE-T Copper SFP Transceiver

#### FCLF-8520/8521-3

#### Product Features

- Up to 1.25Gb/s bi-directional data links
- Hot-pluggable SFP footprint
- Extended case temperature range (0°C to +85°C )
- Fully metallic enclosure for low EMI
- Low power dissipation (1.05 W typical)
- Compact RJ-45 connector assembly
- RoHS compliant and Lead Free
- Access to physical layer IC via 2-wire serial bus
- 10/100/1000 BASE-T operation in host systems with SGMII interface



#### Applications

- 1.25 Gigabit Ethernet over Cat 5 cable

Finisar's FCLF-8520/8521-3 1000BASE-T Copper Small Form Pluggable (SFP) transceivers are based on the SFP Multi Source Agreement (MSA)<sup>1</sup>. They are compatible with the Gigabit Ethernet and 1000BASE-T standards as specified in IEEE Std 802.3<sup>2</sup>. The 1000BASE-T physical layer IC (PHY) can be accessed via I2C, allowing access to all PHY settings and features.

The FCLF-8520-3 uses the SFP's RX\_LOS pin for link indication, and 1000BASE-X auto-negotiation should be disabled on the host system. The FCLF-8521-3 is compatible with 1000BASE-X auto-negotiation, but does not have a link indication feature (RX\_LOS is internally grounded). See AN-2036, "Frequently Asked Questions Regarding Finisar's 1000BASE-T SFPs", for a more complete explanation on the differences between the two models and details on applications issues for the products.

#### PRODUCT SELECTION

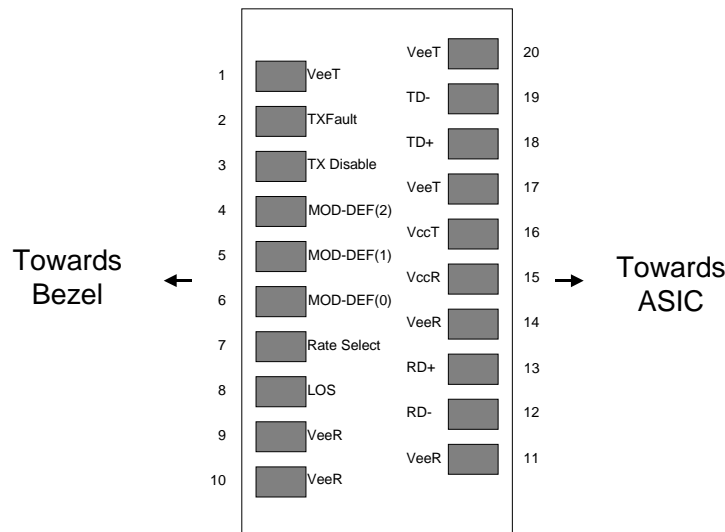
Part Number	Link Indicator on RX_LOS Pin	1000BASE-X auto-negotiation enabled by default
FCLF-8520-3	Yes	No
FCLF-8521-3	No	Yes

**I. SFP to Host Connector Pin Out**

Pin	Symbol	Name/Description	Note
1	V <sub>EET</sub>	Transmitter ground (common with receiver ground)	1
2	T <sub>FAULT</sub>	Transmitter Fault. Not supported	
3	T <sub>DIS</sub>	Transmitter Disable. PHY disabled on high or open	2
4	MOD_DEF(2)	Module Definition 2. Data line for serial ID	3
5	MOD_DEF(1)	Module Definition 1. Clock line for serial ID	3
6	MOD_DEF(0)	Module Definition 0. Grounded within the module	3
7	Rate Select	No connection required	
8	LOS	Loss of Signal indication.	4
9	V <sub>EER</sub>	Receiver ground (common with transmitter ground)	1
10	V <sub>EER</sub>	Receiver ground (common with transmitter ground)	1
11	V <sub>EER</sub>	Receiver ground (common with transmitter ground)	1
12	RD-	Receiver Inverted DATA out. AC coupled	
13	RD+	Receiver Non-inverted DATA out. AC coupled	
14	V <sub>EER</sub>	Receiver ground (common with transmitter ground)	1
15	V <sub>CCR</sub>	Receiver power supply	
16	V <sub>CCT</sub>	Transmitter power supply	
17	V <sub>EET</sub>	Transmitter ground (common with receiver ground)	1
18	TD+	Transmitter Non-Inverted DATA in. AC coupled	
19	TD-	Transmitter Inverted DATA in. AC coupled	
20	V <sub>EET</sub>	Transmitter ground (common with receiver ground)	1

- Notes:
1. Circuit ground is connected to chassis ground
  2. PHY disabled on T<sub>DIS</sub> > 2.0V or open, enabled on T<sub>DIS</sub> < 0.8V
  3. Should be pulled up with 4.7k – 10k Ohms on host board to a voltage between 2.0 V and 3.6 V. MOD\_DEF(0) pulls line low to indicate module is plugged in.
  4. LVTTTL compatible with a maximum voltage of 2.5V. Not supported on FCLF-8521-3.

**Table 1. SFP to host connector pin assignments and descriptions**



**Figure 1. Diagram of host board connector block pin numbers and names**

## II. +3.3V Volt Electrical Power Interface

The FCLF-8520/8521-3 has an input voltage range of 3.3 V +/- 5%. The 4 V maximum voltage is not allowed for continuous operation.

<b>+3.3 Volt Electrical Power Interface</b>						
<b>Parameter</b>	<b>Symbol</b>	<b>Min</b>	<b>Typ</b>	<b>Max</b>	<b>Units</b>	<b>Notes/Conditions</b>
Supply Current	$I_s$		320	375	mA	1.2W max power over full range of voltage and temperature. See caution note below
Input Voltage	$V_{cc}$	3.13	3.3	3.47	V	Referenced to GND
Maximum Voltage	$V_{max}$			4	V	
Surge Current	$I_{surge}$			30	mA	Hot plug above steady state current. See caution note below

Caution: Power consumption and surge current are higher than the specified values in the SFP MSA

**Table 2. +3.3 Volt electrical power interface**

## III. Low-Speed Signals

MOD\_DEF(1) (SCL) and MOD\_DEF(2) (SDA), are open drain CMOS signals (see section VII, "Serial Communication Protocol"). Both MOD\_DEF(1) and MOD\_DEF(2) must be pulled up to host\_Vcc.

<b>Low-Speed Signals, Electronic Characteristics</b>						
<b>Parameter</b>	<b>Symbol</b>	<b>Min</b>	<b>Max</b>	<b>Units</b>	<b>Notes/Conditions</b>	
SFP Output LOW	$V_{OL}$	0	0.5	V	4.7k to 10k pull-up to host_Vcc, measured at host side of connector	
SFP Output HIGH	$V_{OH}$	host_Vcc - 0.5	host_Vcc + 0.3	V	4.7k to 10k pull-up to host_Vcc, measured at host side of connector	
SFP Input LOW	$V_{IL}$	0	0.8	V	4.7k to 10k pull-up to Vcc, measured at SFP side of connector	
SFP Input HIGH	$V_{IH}$	2	Vcc + 0.3	V	4.7k to 10k pull-up to Vcc, measured at SFP side of connector	

**Table 3. Low-speed signals, electronic characteristics**

#### IV. High-Speed Electrical Interface

All high-speed signals are AC-coupled internally.

<b>High-Speed Electrical Interface, Transmission Line-SFP</b>						
<b>Parameter</b>	<b>Symbol</b>	<b>Min</b>	<b>Typ</b>	<b>Max</b>	<b>Units</b>	<b>Notes/Conditions</b>
Line Frequency	$f_L$		125		MHz	5-level encoding, per IEEE 802.3
Tx Output Impedance	$Z_{out,TX}$		100		Ohm	Differential, for all frequencies between 1MHz and 125MHz
Rx Input Impedance	$Z_{in,RX}$		100		Ohm	Differential, for all frequencies between 1MHz and 125MHz

**Table 4. High-speed electrical interface, transmission line-SFP**

<b>High-Speed Electrical Interface, Host-SFP</b>						
<b>Parameter</b>	<b>Symbol</b>	<b>Min</b>	<b>Typ</b>	<b>Max</b>	<b>Units</b>	<b>Notes/Conditions</b>
Single ended data input swing	$V_{insing}$	250		1200	mV	Single ended
Single ended data output swing	$V_{outsing}$	350		800	mV	Single ended
Rise/Fall Time	$T_r, T_f$		175		psec	20%-80%
Tx Input Impedance	$Z_{in}$		50		Ohm	Single ended
Rx Output Impedance	$Z_{out}$		50		Ohm	Single ended

**Table 5. High-speed electrical interface, host-SFP**

## V. General Specifications

General						
Parameter	Symbol	Min	Typ	Max	Units	Notes/Conditions
Data Rate	BR	10		1,000	Mb/sec	IEEE 802.3 compatible. See Notes 2 through 4 below
Cable Length	L			100	m	Category 5 UTP. BER <10 <sup>-12</sup>

Table 6. General specifications

### Notes:

1. Clock tolerance is +/- 50 ppm
2. By default, the FCLF-8520/8521-3 is a full duplex device in preferred master mode
3. Automatic crossover detection is enabled. External crossover cable is not required
4. 10/100/1000 BASE-T operation requires the host system to have an SGMII interface with no clocks, and the module PHY to be configured per Application Note AN-2036. With a SERDES that does not support SGMII, the module will operate at 1000BASE-T only.

## VI. Environmental Specifications

The FCLF-8520/8521-3 has an extended range from 0°C to +85°C case temperature as specified in Table 8.

Environmental Specifications						
Parameter	Symbol	Min	Typ	Max	Units	Notes/Conditions
Operating Temperature	T <sub>op</sub>	0		85	°C	Case temperature
Storage Temperature	T <sub>sto</sub>	-40		85	°C	Ambient temperature

Table 7. Environmental specifications

## VII. Serial Communication Protocol

All Finisar SFPs support the 2-wire serial communication protocol outlined in the SFP MSA<sup>1</sup>. These SFPs use an Atmel AT24C01A 128 byte E<sup>2</sup>PROM with an address of A0h. For details on interfacing with the E<sup>2</sup>PROM, see the Atmel data sheet titled "AT24C01A/02/04/08/16 2-Wire Serial CMOS E<sup>2</sup>PROM."<sup>3</sup>

The 1000BASE-T physical layer IC can also be accessed via the 2-wire serial bus at address ACh. For details interfacing with the PHY IC, see Marvell data sheet titled "Alaska Ultra 88E1111 Integrated Gigabit Ethernet Transceiver"<sup>4</sup> (Marvell document number MV-S100649-00).

Serial Bus Timing Requirements						
Parameter	Symbol	Min	Typ	Max	Units	Notes/Conditions
I <sup>2</sup> C Clock Rate		0		100,000	Hz	

Table 8. Serial bus timing requirements

### VIII. Mechanical Specifications

The host-side of the FCLF-8520/8521-3 conforms to the mechanical specifications outlined in the SFP MSA<sup>1</sup>. The front portion of the SFP (part extending beyond the face plate of the host) is larger to accommodate the RJ-45 connector. See Figure 2 below for details.

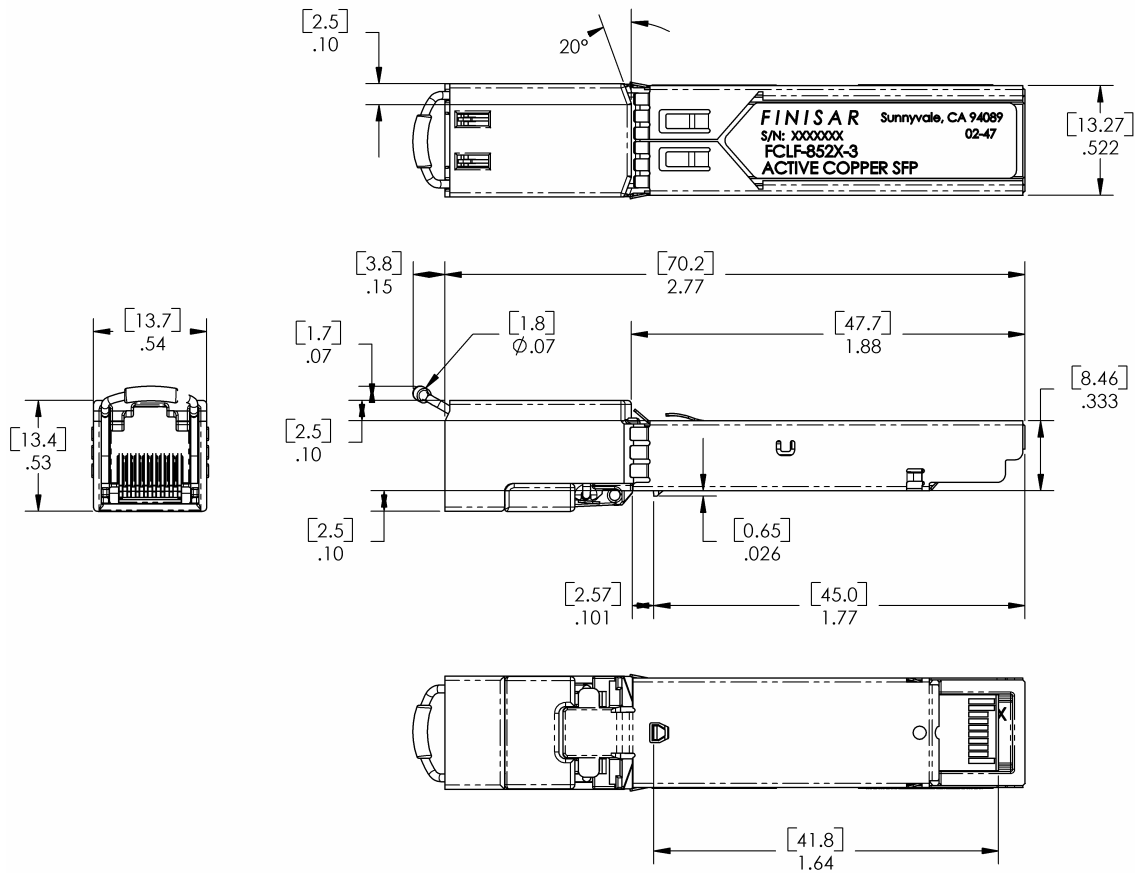


Figure 2. FCLF-8520/8521-3 mechanical dimensions

**IX. References**

1. Small Form Factor Pluggable (SFP) Transceiver Multi-Source Agreement (MSA), September 2000. Documentation is currently available at Finisar upon request.
2. IEEE Std 802.3, 2002 Edition. IEEE Standards Department, 2002.
4. “AT24C01A/02/04/08/16 2-Wire Serial CMOS E<sup>2</sup>PROM”, Atmel Corporation. [www.Atmel.com](http://www.Atmel.com)
5. “Alaska Ultra 88E1111 Integrated 10/100/1000 Gigabit Ethernet Transceiver”, Marvell Corporation. [www.marvell.com](http://www.marvell.com)

**X. For More Information**

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