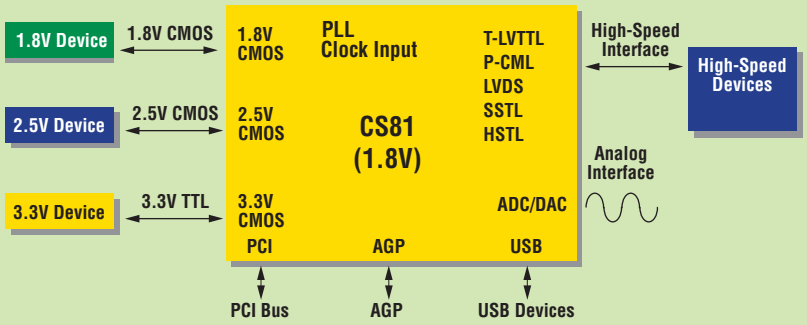
CS81 Series Standard Cell

0.18µm CMOS Technology

Features

- 0.13µm effective channel length
- 3 to 5 layers of metal interconnects
- Very high density: 110K raw gates/mm^2
- Up to 28 million gates
- Core power supply voltage: 1.8V to 1.1V
- 5 nW/gate/MHz power dissipation at 1.1V
- 11 ps gate delay at 1.8V and 1 fan-out
- Junction temperature range: –40 to +125°C
- I/Os: 3.3V, 2.5V, 1.8V, 5V tolerant
- High-density diffused RAMs and ROMs
- High-speed mixed-signal macros
- Analog PLLs
- Wide selection of advanced packaging options
- Proven design methodology and tool support
- Two cell libraries: high-performance and high-density

CS81 I/O Interface Capabilities



Description

Fujitsu's CS81, a 0.18µm (0.13µm L_{eff}) standard-cell product, is based on Fujitsu's state-of-the-art CMOS process technology, a deep sub-micron process designed for today's high-density and low-power SOC products. The cell library, which is optimized for synthesis-based designs, has accurate timing and power-characterized data, cell areas, and statistical wire-load models. The CS81 standard-cell library contains both high-performance and high-density cells, giving designers the option of combining both types of standard cell blocks on the same chip. The CS81 library supports popular third-party tools and data-exchange file standards.

The CS81 chip cores can operate at 1.8V to 1.1V. The I/Os, operating at 1.8V, 2.5V, 3.3V, or 5V tolerance, can conveniently interface with various types of devices. Interface options include low-swing, high-speed I/Os and high-speed bus interface I/Os.

Both inline and staggered I/O pad configurations are available. Inline pads are available in both 70µm and 44µm pad pitch. The 70µm pads are wire bonded, whereas the 44µm pads are used with TAB. The 66µm wire-bond stagger pads can be used for optimizing the die area of pad-limited designs.

In addition to the traditional QFP packages, the CS81 family is available in TAB, EBGA, FBGA, and Flip-chip BGA packages.

CS81 offers a rich set of ADCs and DACs, PLLs, high-speed RAMs and ROMs, as well as a variety of other embedded functions. The following blocks will be available in the near future:

- Special high-speed I/Os:
  T-LVTTL, P-CML, LVDS, SSTL, and HSTL
- Special-purpose Interfaces:
  PCI, AGP, and USB

Design Methodology

Fujitsu's design methodology ensures first-time silicon success by integrating proprietary point tools with popular, sign-off-quality, industry-standard CAD tools such as:

- Logic design rule checker
- Delay calculator
- Quasi 3-D parasitic extraction tool

Fujitsu's clock-driven design methodology is devised for low power and low skew. The methodology identifies the best-suited clock distribution strategy for a given design and

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predicts performance in advance. Fujitsu supports co-simulation, emulation and high-level floor-planning to optimize the power, timing, and size of the design. This enables the designer to make effective architectural-level decisions to achieve optimal design solutions.

Fujitsu's design methodology supports cycle-based simulators and formal verification, as well as static timing analysis and the more conventional VHDL and Verilog simulators. Fujitsu's design-for-test strategy includes boundary scan (JTAG) and full and partial scan, as well as a built-in self-test for memory.

Applications

CS81 offers high-density standard cells for very low-power applications. Also provided in CS81 are high-performance and area-optimized memories, mixed-signal blocks, analog functions, a rich set of IP Cores and Mega Macros, and various I/O interfaces. The CS81 ASIC design kit, combined with its supported EDA tool sets, is poised for chip developments that require ease-of-tool use, proven design flow and a quick time to market.

Mixed-Signal Macros

- A/D Converters
  - 8-bit: 50 MS/s high-speed 3.3V
  - 8-bit: 25 MS/s high-speed 3.3V
  - 8-bit: 1 MS/s 3.3V
- D/A Converters
  - 10-bit: 30 MS/s 3.3V
  - 8-bit: 50 MS/s 3.3V
  - 8-bit: 1 MS/s 3.3V

Multiplier Compiler

- Multiplicand (m): $4 \leq m \leq 32$
- Multiplier (n): $4 \leq n \leq 32$ (even numbers only)

Memory Macros

- SRAM Compiler: single and dual port (1RW/1R), up to 72K bits per block
- High-speed SRAMs, up to 144K bits
- High-density SRAMs (1 RW) 512K ~ 1.1M bits (under development)
- Register files: 2R/2W
- ROM Compiler: up to 512K bits per block

Phase-Locked Loops

- Analog: up to 800 MHz

I/Os

- 1.8V, 2.5V, and 3.3V CMOS (2.5V is under development)
- Slew-rate controlled
- Capable of driving large loads: 2, 4, 8, and 12 mA sinking current
- Transceivers under development: P-CML, LVDS, PCI, SSTL, and GTL
- AGP 2X and 4X
- 2.5 Gbps with clock recovery and Serdes (under development)
- To be developed: 5V tolerant buffers

SOC IP Cores

- ARC 32-bit RISC
- 10/100 MAC
- 64/256 QAM
- MPEG2 Decoder/Demultiplexer
- 8VSB TV Demodulator
- AC3 Dolby Voice Decoder
- JPEG Encoder and Decoder
- PCI – 33/66 MHz, 32/64 bit cores
- USB Host Controller/Device
- I^2C
- IDE (ATA3) Host Controller
- Smart Card I/F
- IRDA I/R Interface
- To be developed:
  - ARM 7TDMI Hard Macro
  - Oak DSP Hard Macro
  - More IPs are being added

ASIC Design Kit and EDA Support	
Verilog Logic Simulators from Cadence, Synopsys, and Mentor	Verilog-XL, NC Verilog, VCS, Model-sim (Verilog)
VHDL/VITAL Logic Simulators from Synopsys, Cadence, and Mentor	VSS, Model-sim (VHDL) V-System, Leapfrog
Synthesis, DFT, and STA tools from Synopsys	Design Compiler, Test Compiler, and PrimeTime
Other EDA Tools	Chrysalis Design Verifyer and Cadence DP

PACKAGE AVAILABILITY		
No. of Pins/Balls	**Pin/Ball Pitch**	**Dimensions**
TAB-BGA (Cavity-down)		
304	0.8 mm	21 mm
352	0.8 mm	23 mm
480	1.0 mm	31 mm
560	1.0 mm	35 mm
660	1.0 mm	40 mm
720	1.0 mm	40 mm
EBGA (Cavity-down)		
576	1.27 mm	40 mm
672	1.27 mm	45 mm
HQFP (Cavity-up)		
208	0.50 mm	28 mm
240	0.50 mm	32 mm
256	0.40 mm	28 mm
304	0.50 mm	40 mm
TQFP (Cavity-up)		
100	0.50 mm	14 mm
120	0.50 mm	20 mm
LQFP (Cavity-up)		
144	0.50 mm	20 mm
176	0.50 mm	24 mm
208	0.50 mm	28 mm
FBGA (Cavity-up)		
112	0.80 mm	10 mm
144	0.80 mm	12 mm
168	0.80 mm	12 mm
176	0.80 mm	12 mm
192	0.80 mm	14 mm
224	0.80 mm	16 mm
240	0.50 mm	10 mm
272	0.80 mm	18 mm
288	0.75 mm	18 mm
304	0.50 mm	12 mm
320	0.80 mm	18 mm
368	0.50 mm	14 mm
FC-BGA (Cavity-down)		
1,089	1.27 mm	42.4 mm
1,225	1.27 mm	45.0 mm
1,369	1.27 mm	47.5 mm
1,681	1.00 mm	42.5 mm
1,849	1.00 mm	45.0 mm
2,116	1.00 mm	47.5 mm

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