IEEE1394 Serial Bus Controller for DTV

MB86617A LSI Specification

Rev. 1.0 August 16, 2001

Contents

Chapter 1 Overview

This chapter explains the overview of MB86617A.

MB86617A is Fujitsu's IEEE1394 serial bus controller based on both IEEE1394 Standard (IEEE Std. 1394-1995) and P1394.a Standard Draft (rev.2.0).

This MB86617A has three ports for network under the 1394 cable environment, differential transceiver, and comparator, and the transfer data rate supports S400.

MB86617A integrates PHY and LINK layers into single-chip, and plans for degression of component side product and saving power consumption.

MB86617A has two exclusive ports (one is the combined use for receiving a message of interface for DV) for MPEG2 and DSS data transfer, and performs isolating and packeting of Header and Data department with these two ports automatically. This function is suited for maintaining continuum of transfer.

Chapter 2 Features

This chapter explains the features of MB86617A.

> Compliant with IEEE1394 high performance serial bus standard and P1394.a standard draft
> Integrates PHY and LINK layers into single-chip
> 1394 port number : 3 ports
> Transfer Data Rate : S100, S200, S400
> On-chip PLL (corresponding to Crystal Osci llator) : generate internal clock
> 4K Byte X 2 channels Isochronous transmit and receive data buffer
> 256Byte Asynchronous exclusive buffer for transmit/receive
> Auto isolating and packeting for received header and data of packet
> Two exclusive ports for Isochronous transfer (8 bit bus)
> Loading interface with copy protection LSI (8 bits I/O)
> Generating and Checking Function for 32bit CRC
> 6-pin cable supported
> Power supply system : 3.3V size-D battery
> Package : LQFP-176 (FPT-176P-M03)

Chapter 3 Chip Block

This chapter explains the MB86617A block diagram and the function of each block.

3.1. Block Diagram

MB86617A block diagram is shown below.

■ Normal Operation Mode

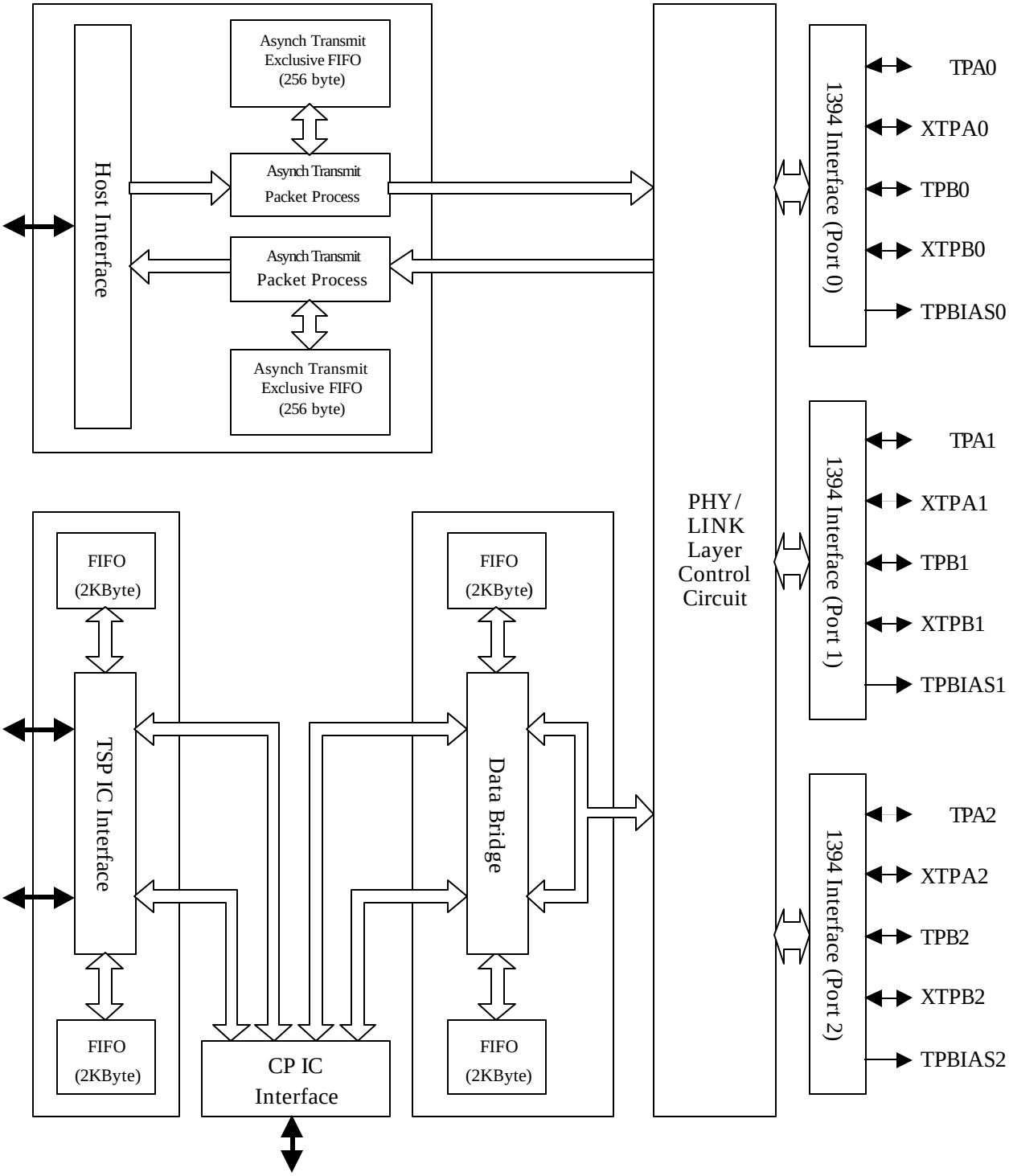


Fig.3.1.1 Block Diagram - Normal Operation Mode -

■ Asynchronous Transmit FIFO Extended Mode

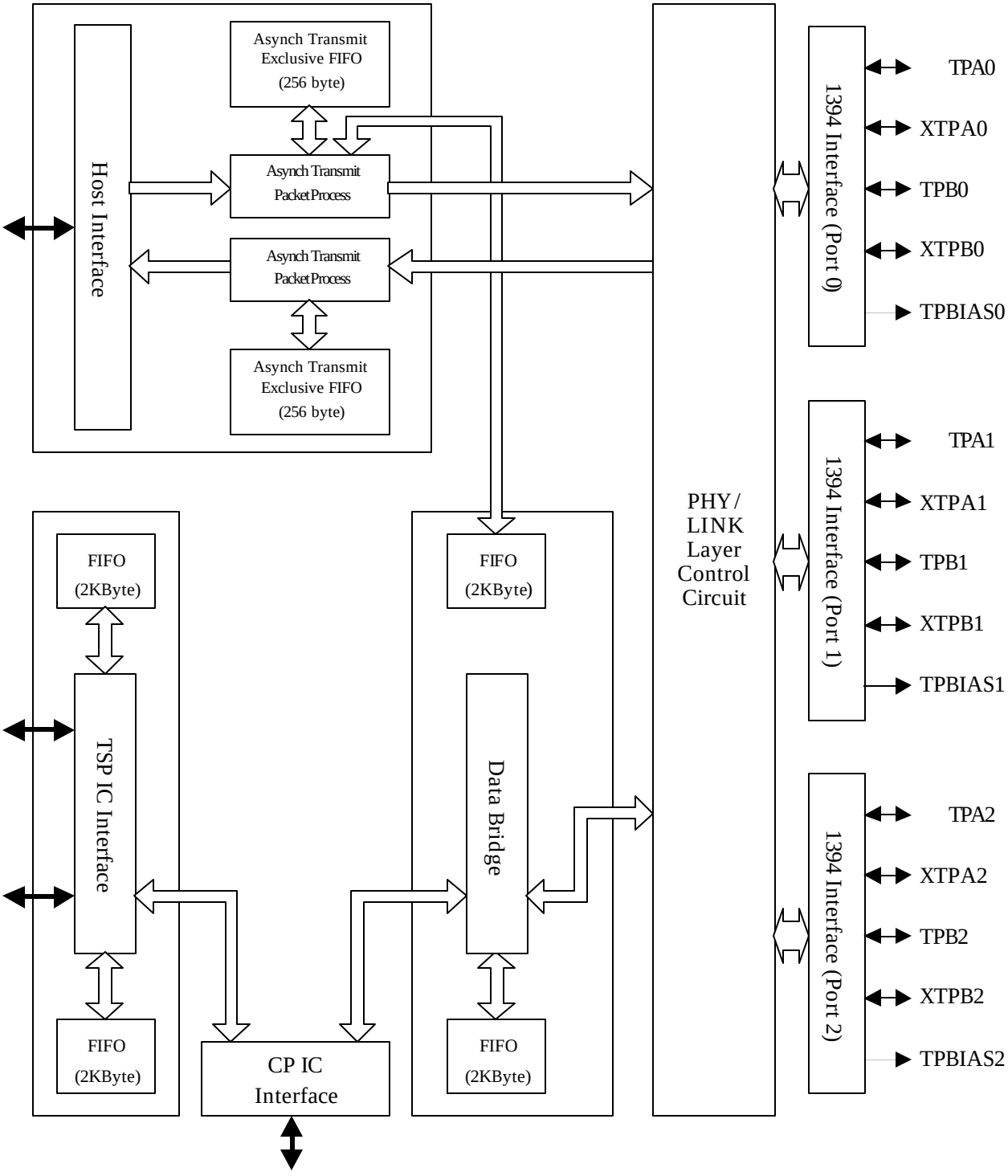


Fig.3.1.2 Block Diagram - Asynchronous Transmit FIFO Extended Mode-

■ Asynchronous Receive FIFO Extended Mode

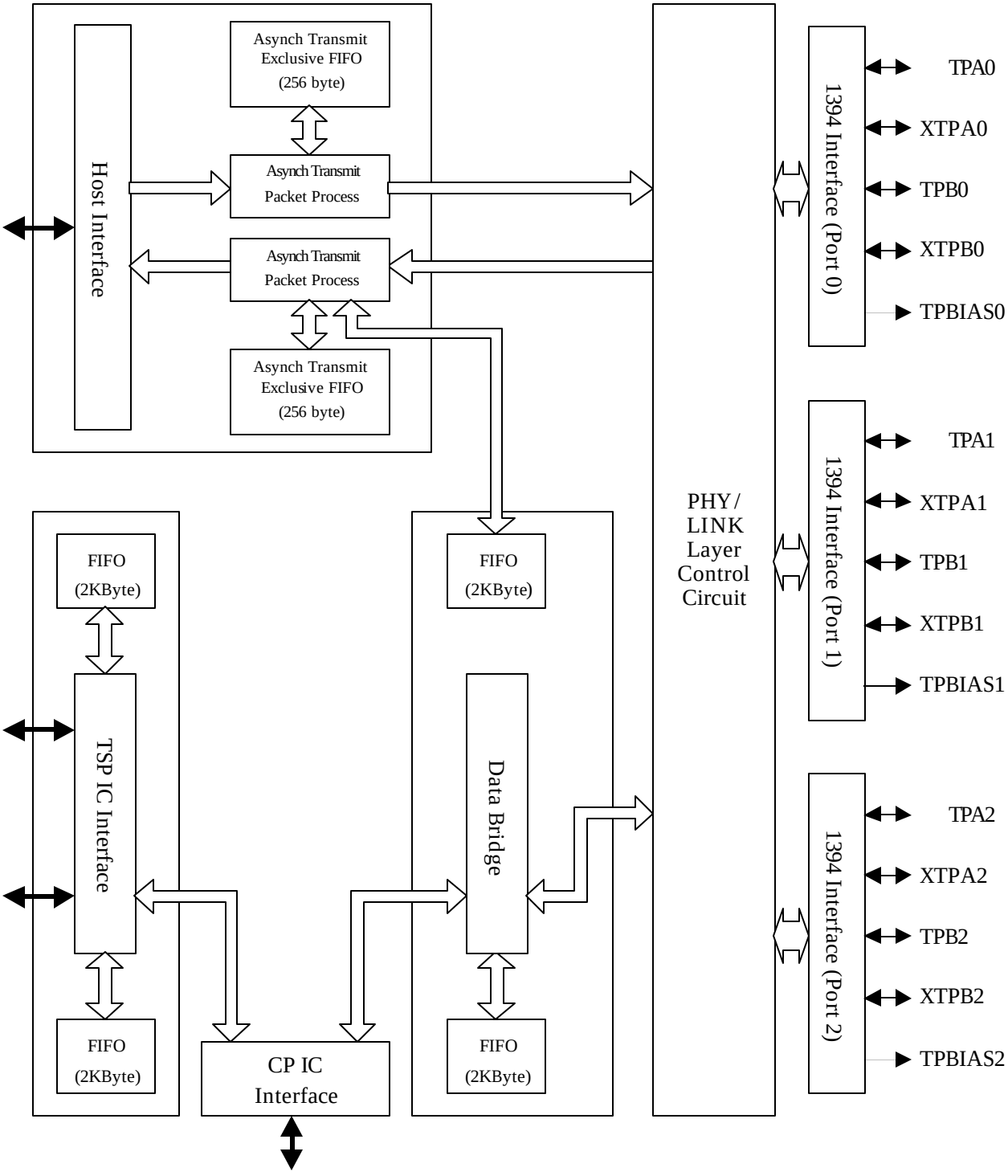


Fig.3.1.3 Block Diagram - Asynchronous Receive FIFO Extended Mode -

3.2. Function of Each Block

This section explains the function of each block for MB86617A.

■ PHY Layer Control Circuit

This circuit is for the Physical layer of IEEE 1394 with the following functions.
> Asynchronous transfer is supported under cable environment.
> Maximum transfer data rate : 393.216Mbit/sec.
> with three ports for transceiver/receiver : transfer IEEE1394 packet
> with bus monitor, initial performance for occurring bus reset, speed signaling, arbitration, encode/decode : transfer/receive data

■ LINK Layer Control Circuit

This circuit generates standard packet for IEEE1394, controls transfer, and performs the following functions.
> Generates and checks 32 bit CRC for header and data of packet.
> Activates cycle master function with integrated 32 bit cycle timer register

■ TSP IC Interface

This TSP IC Interface has two exclusive ports with the following functions for transmitting/receiving TSP IC, MPEG2-TS and DSS data, and receiving DV data.
> Adds time stamp to both MPEG2 -TS and DSS data.
> Outputs received data just when the value of time stamp (SPH) and cycle timer is matched with each other.
> Integrated transmit/receive (dual purpose) FIFO for transferring Isochronous by 2K byte X 2 channels.

■ CP IC Interface

This interface adds the copy information to CP IC so as to correspond to copy protect.

■ Data Bridge

This Data Bridge packets MPEG2-TS, DSS, and DVC, and re-builds the receiving data.
At data transmission, this section adds Isochronous packet header and CIP header, and connects / separates source packet
When transmitting 2ch, it connects Isochronous packet.
At data receipt, it deletes Isochronous packet header and CIP header, restores by unit of source packet.
When receiving 2ch, it separates Isochronous packet and divide them to each FIFO.
> Integrated transmit/receive (dual purpose) FIFO for transferring Isochronous by 2K byte X 2 channels.

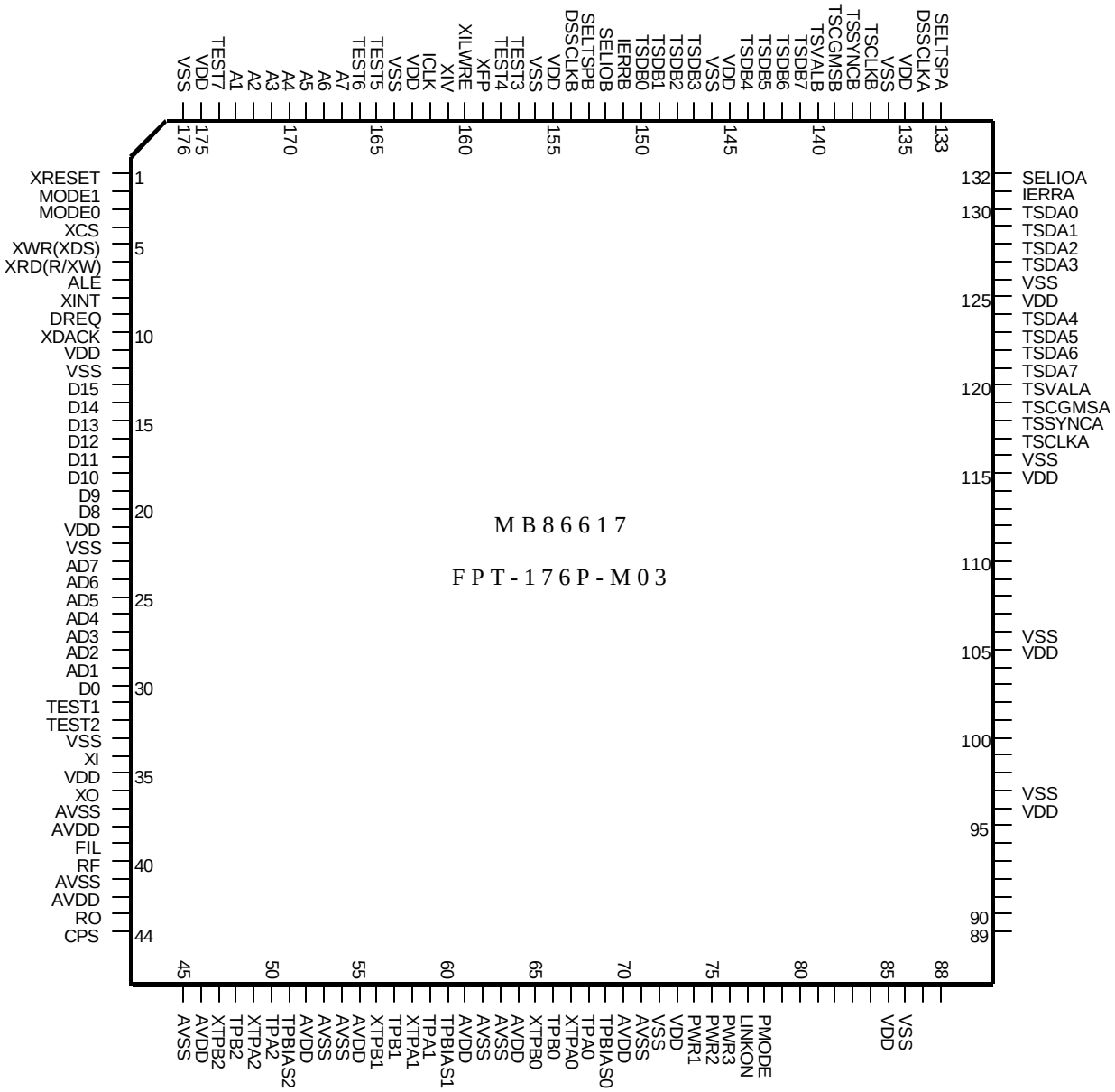
Chapter 4 Pin Assignment

This chapter explains the pin assignment and table of pin function of MB86617A.

4.1. Pin Assignment
4.2. Corresponding Table of MB86617A Pin
4.3. Outline Drawing of Package

4.1. Pin Assignment

The following diagram shows the MB86617A pin assignment.



4.2. Corresponding Table of MB86617A Pin

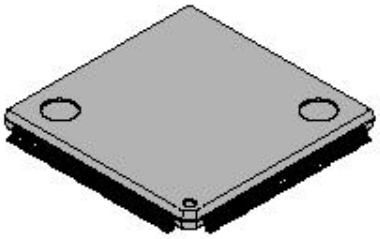
The following table shows the corresponding items of MB86617A pin.

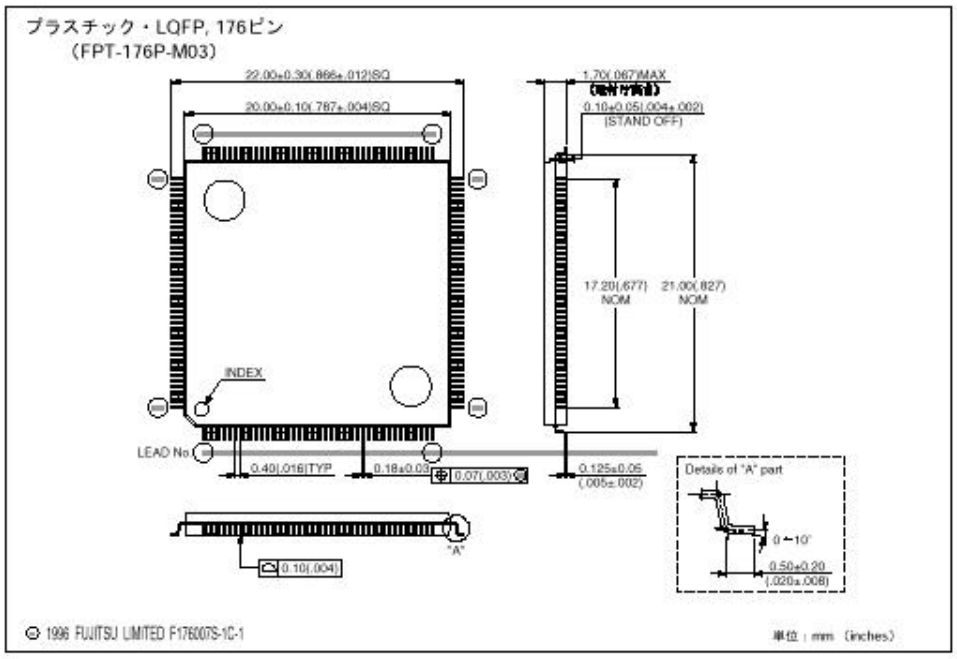
Pin No.	I/O	Pin Name	Pin No.	I/O	Pin Name	Pin No.	I/O	Pin Name	Pin No.	I/O	Pin Name
1	I	XRESET	45	-	AVSS	89			133	O	SELTSPA
2	I	MODE1	46	-	AVDD	90			134	I	DSSCLKA
3	I	MODE0	47	I/O	XTPB2	91			135	-	VDD
4	I	XCS	48	I/O	TPB2	92			136	-	VSS
5	I	XWR(XDS)	49	I/O	XTPA2	93			137	I/O	TSCLKB
6	I	XRD(R/XW)	50	I/O	TPA2	94			138	I	TSSYNCB
7	I	ALE	51	O	TPBIAS2	95			139	I	TSCGMSB
8	O	XINT	52	-	AVDD	96	-	VDD	140	I/O	TSVALB
9	O	DREQ	53	-	AVSS	97	-	VSS	141	I/O	TSDB7
10	I	XDACK	54	-	AVSS	98			142	I/O	TSDB6
11	-	VDD	55	-	AVDD	99			143	I/O	TSDB5
12	-	VSS	56	I/O	XTPB1	100			144	I/O	TSDB4
13	I/O	D15	57	I/O	TPB1	101			145	-	VDD
14	I/O	D14	58	I/O	XTPA1	102			146	-	VSS
15	I/O	D13	59	I/O	TPA1	103			147	I/O	TSDB3
16	I/O	D12	60	O	TPBIAS1	104			148	I/O	TSDB2
17	I/O	D11	61	-	AVDD	105	-	VDD	149	I/O	TSDB1
18	I/O	D10	62	-	AVSS	106	-	VSS	150	I/O	TSDB0
19	I/O	D9	63	-	AVSS	107			151	O	IERRB
20	I/O	D8	64	-	AVDD	108			152	O	SELIOB
21	-	VDD	65	I/O	XTPB0	109			153	O	SELTSPB
22	-	VSS	66	I/O	TPB0	110			154	I	DSSCLKB
23	I/O	AD7	67	I/O	XTPA0	111			155	-	VDD
24	I/O	AD6	68	I/O	TPA0	112			156	-	VSS
25	I/O	AD5	69	O	TPBIAS0	113			157	I/O	TEST3
26	I/O	AD4	70	-	AVDD	114			158	I/O	TEST4
27	I/O	AD3	71	-	AVSS	115	-	VDD	159	O	XFP
28	I/O	AD2	72	-	VSS	116	-	VSS	160	O	XILWRE
29	I/O	AD1	73	-	VDD	117	I/O	TSCLKA	161	I	XIV
30	I/O	D0	74	I	PWR1	118	I/O	TSSYNCA	162	I	ICLK
31	I/O	TEST1	75	I	PWR2	119	I/O	TSCGMSA	163	-	VDD
32	I/O	TEST2	76	I	PWR3	120	I/O	TSVALA	164	-	VSS
33	-	VSS	77	O	LINKON	121	I/O	TSDA7	165	I/O	TEST5
34	I	XI	78	I	PMODE	122	I/O	TSDA6	166	I/O	TEST6
35	-	VDD	79			123	I/O	TSDA5	167	I	A7
36	I/O	XO	80			124	I/O	TSDA4	168	I	A6
37	-	AVSS	81			125	-	VDD	169	I	A5
38	-	AVDD	82			126	-	VSS	170	I	A4
39	O	FIL	83			127	I/O	TSDA3	171	I	A3
40	O	RF	84			128	I/O	TSDA2	172	I	A2
41	-	AVSS	85	-	VDD	129	I/O	TSDA1	173	I	A1
42	-	AVDD	86	-	VSS	130	I/O	TSDA0	174	I/O	TEST7
43	O	RO	87			131	O	IERRA	175	-	VDD
44	I	CPS	88			132	O	SELIOA	176	-	VSS

4.3. Outline Drawing of Package

This section shows the outline drawing of MB86617A package (LQFP-176).

FPT-176P-M03

プラスチック・LQFP, 176ピン  (FPT-176P-M03)	リードピッチ	0.40mm
	パッケージ幅× パッケージ長さ	20×20mm
	リード形状	ガルウィング
	封止方法	プラスチックモールド



Chapter 5 Pin Function

This chapter explains the MB86617A pin function.

5.1. IEEE1394 Interface

This section explains the pin function of IEEE1394 interface.

Signal Name	I/O	Function
TPA0	I/O	I/O pin of TPA + (plus) signal on cable port 0
XTPA0	I/O	I/O pin of TPA - (minus) signal on cable port 0
TPB0	I/O	I/O pin of TPB + (plus) signal on cable port 0
XTPB0	I/O	I/O pin of TPB - (minus) signal on cable port 0
TPA1	I/O	I/O pin of TPA + (plus) signal on cable port 1
XTPA1	I/O	I/O pin of TPA - (minus) signal on cable port 1
TPB1	I/O	I/O pin of TPB + (plus) signal on cable port 1
XTPB1	I/O	I/O pin of TPB - (minus) signal on cable port 1
TPA2	I/O	I/O pin of TPA + (plus) signal on cable port 2
XTPA2	I/O	I/O pin of TPA - (minus) signal on cable port 2
TPB2	I/O	I/O pin of TPB + (plus) signal on cable port 2
XTPB2	I/O	I/O pin of TPB - (minus) signal on cable port 2
TPBIAS0	O	Output pin of reference voltage for common voltage on cable port 0
TPBIAS1	O	Output pin of reference voltage for common voltage on cable port 1
TPBIAS2	O	Output pin of reference voltage for common voltage on cable port 2

5.2. Isochronous Interface

This section explains the pin function of Isochronous interface.

Signal Name	I/O	Function
TSVALIDA	I/O	I.O pin for indicating effective data period of TS packet (on port A) 'H' active signal
TSSYNCA	I/O	Input/Output pin for indicating leading data of TS packet (on port A) 'H' active signal
TSCLKA	I/O	On transmitting: sync clock input pin for input data of TS packet On receiving : sync clock output pin for output data of TS packet (switchable either 6.144MHz or 3.072MHz)
TSDA7 - 0	I/O	I/O pin for TS packet data (on Port A)
TSCGMSA	I	Serial input pin for CGMS and TSCH information (on port A) Effective for 8 clocks since TSSYNCA input signal rising
SELIOA	O	Output pin for switching I/O on port A Outputs 'L' at transmitting and 'H'at receiving
SELTSPA	O	Output pin for switching output device from port A
TSVALIDB	I/O	I.O pin for indicating effective data period of TS packet (on port B) 'H' active signal
TSSYNCB	I/O	Input/Output pin for indicating leading data of TS packet (on port B) 'H' active signal
TSCLKB	I/O	On transmitting: sync clock input pin for input data of TS packet On receiving : sync clock output pin for output data of TS packet (switchable either 6.144MHz or 3.072MHz)
TSDB7 - 0	I/O	I/O pin for TS packet data (on port B)
TSCGMSB	I	Serial input pin for CGMS and TSCH information (on port B) Effective for 8 clocks since TSSYNCA input signal rising
SELIOB	O	Output pin for switching I/O on port B Outputs 'L' at transmitting and 'H'at receiving
SELTSPB	O	Output pin for switching output device from port B
ICLK	I	Clock input pin from DV-IC
XILWRE	O	Output pin for signal to be allowed accessing to Isochronous-FIFO Asserted by completing reception of data for one source packet 'L' active signal
XIV	I	Input signal for enable signal of Isochronous data Output Isochronous-FIFO data to data output pin while this signal in active. Switch data synchronizing with rise edge of ICLK
XFP	O	Output pin of time stamp trigger signal 'L' active signal

IERRA	O	Output pin for noticing error of receive data (on port A) 'H' active signal
IERRB	O	Output pin for noticing error of receive data (on port B) 'H' active signal
DSSCLKA	I	Clock input pin for DSS data (27MHz)
DSSCLKB	I	Clock input pin for DSS data (27MHz)

5.4. MPU Interface

This section explains the pin function of MPU interface.

Signal Name	I/O	Function
A7 – 1	I	Address input pin for selecting internal register Available only when selecting non-multi mode When selecting multiplex mode, set this signal in fixed 'L'
D15 - 8,0 AD7 – 1	I/O	Data I/O pin Corresponding to address input signal when selecting multiplex mode
XCS	I	Chip enable input pin for this device
XRD(R/W)	I	80 system mode: read out strobe input pin for this device 68 system mode: input pin for controlling read out/write for this device
XWR(XDS)	I	80 system mode: strobe input pin for writing into this device 68 system mode: input pin of XDS signal to be output with data bus in available
ALE	I	Input pin of ALE signal to be output with its address in available when selecting multiplex mode When selecting non-multiplex mode, set this signal in fixed 'L'
DREQ	O	Output pin of DMA transfer requiring signal for DMAC
XDACK	I	Input pin of DMA allowance signal from DMAC
XINT	O	Output pin for interruption request

5.5. Other Pins

This section explains the pin function like internal PLL.

Signal Name	I/O	Function
XRESET	I	Input signal for resetting signal When operating with cable supply power, set this pin to 'L'.
MODE1	I	This pin is used for setting operating mode of MPU. This device is operated as follows depending on the setting of MODE1 and MODE0 pins; '00' input: TX1940 mode '01' input: MB90F574 mode '10' input: 80 system non-multiplex mode '11' input: 68 system non-multiplex mode
MODE0		
XO	I/O	Exterior type crystal connecting pin for oscillator circuit (24.576MHz)
XI	I	
RF	O	Connect t o GND through 5.1kΩ register.
FIL	O	Exterior type filter circuit connecting pin for internal PLL
RO	O	Connect to GND through 5.1kΩ register.
CPS	I	Power supply input pin from IEEE1394 cable Detect cable supply power 0 to 33V (requiring of lowering/dividing voltage)
PMODE	I	Criterion pin for inputting power 'L' input : operate with power supplying through IEEE1394 cable 'H' input: operate with system power
PWR3 - 1	I	Setting pin got POWER_CLASS of Self-ID packet to be transmitted when operating with supply power through cable. Note) The POWER_CLASS of the Self_ID packet to be sent when operating under the system power does not use this pin, but follows the setting of Pwr bit (Bit2 to 0) of Physical Register#4.
LINKON	O	Output pin for detecting Link-on packet receive Output 'H' when receiving Link-on packet under operating with supply power through IEEE1394 cable. When PMODE becomes 'H', 'L' is output. With the PMODE in 'H', the output of this pin is not changed. If not using this pin, set this pin as open one.
TEST1 - 7	I/O	This pin is for test. Use this pin as open one.

5.6. Power/GND Pin

This section explains the power/GND pin.

Signal Name	I/O	Function
VDD	-	3.3V digital power pin
VSS	-	Digital ground pin
AVDD	-	3.3V analog power pin
AVSS	-	Analog ground pin

Chapter 6 Internal Register

This chapter explains the MB86617A internal register.
Note that the access of internal register is applied only 16 bits access.

Address (HEX)	WRITE	READ
	Register Name	Register Name
00	mode-control	mode-control
02	(reserved)	flag & status
04	Instruction-fetch	Instruction-fetch
06	Interrupt-mask setting [A]	Interrupt indicate [A]
08	Interrupt-mask setting [B]	Interrupt indicate [B]
0A	(reserved)	Receive Acknowledge
0C	A-buffer data port transmit	A-buffer data port receive
0E	(reserved)	(reserved)
10	TSP transmit information setting [A]	TSP transmit information setting [A]
12	TSP transmit information setting [B]	TSP transmit information setting [B]
14	transmit offset setting [A] (upper)	transmit offset setting [A] (upper)
16	transmit offset setting [A] (lower)	transmit offset setting [A] (lower)
18	transmit offset setting [B] (upper)	transmit offset setting [B] (upper)
1A	transmit offset setting [B] (lower)	transmit offset setting [B] (lower)
1C	TSP receive information setting	TSP receive information setting
1E	transmit DSS packet header setting [A] (most significant)	receive DSS packet header setting [A] (most significant)

Address (HEX)	WRITE	READ
	Register Name	Register Name
20	transmit DSS packet header setting [A] (upper)	receive DSS packet header setting [A] (upper)
22	transmit DSS packet header setting [A] (medium)	receive DSS packet header setting [A] (medium)
24	transmit DSS packet header setting [A] (lower)	receive DSS packet header setting [A] (lower)
26	transmit DSS packet header setting [A] (least significant)	receive DSS packet header setting [A] (least significant)
28	transmit DSS packet header setting [B] (most significant)	receive DSS packet header setting [B] (most significant)
2A	transmit DSS packet header setting [B] (upper)	receive DSS packet header setting [B] (upper)
2C	transmit DSS packet header setting [B] (medium)	receive DSS packet header setting [B] (medium)
2E	transmit DSS packet header setting [B] (lower)	receive DSS packet header setting [B] (lower)
30	transmit DSS packet header setting [B] (least significant)	receive DSS packet header setting [B] (least significant)
32	(reserved)	TSP status
34	data bridge transmit information setting 1 [A]	data bridge transmit information setting 1 [A]
36	data bridge transmit information setting 2 [A]	data bridge transmit information setting 2 [A]
38	data bridge transmit information setting 3 [B]	data bridge transmit information setting 3 [B]
3A	data bridge transmit information setting 4 [B]	data bridge transmit information setting 4 [B]
3C	data bridge receive information setting	data bridge receive information setting
3E	transmit packet concatenate/split setting	transmit packet concatenate/split setting
40	Late packet criterion range setting [A]	Late packet criterion range setting [A]
42	Late packet criterion range setting [B]	Late packet criterion range setting [B]
44	(reserved)	receive Isochronous packet header indicate 1 [A]
46	(reserved)	receive Isochronous packet header indicate 2 [A]
48	(reserved)	receive Isochronous packet header indicate 3 [B]
4A	(reserved)	receive Isochronous packet header indicate 4 [B]
4C	FIFO reset	FIFO reset
4E	(reserved)	data bridge transmit/receive status [A]

Address (HEX)	WRITE	READ
	Register Name	Register Name
50	(reserved)	data bridge transmit/receive status [B]
52	(reserved)	Isochronous channel monitor 1
54	(reserved)	Isochronous channel monitor 2
56	(reserved)	Isochronous channel monitor 3
58	(reserved)	Isochronous channel monitor 4
5A	(reserved)	cycle-time-monitor (upper)
5C	(reserved)	cycle-time-monitor (lower)
5E	(reserved)	Ping time monitor
60	PHY/LINK register address setting	PHY/LINK register address setting
62	PHY/LINK register access port	PHY/LINK register access port
64	(reserved)	Revision indicate register (upper)
66	(reserved)	Revision indicate register (lower)
68	(reserved)	(reserved)
6A	(reserved)	(reserved)
6C	(reserved)	(reserved)
6E	(reserved)	(reserved)
70	(reserved)	(reserved)
72	(reserved)	(reserved)
74	(reserved)	(reserved)
76	(reserved)	(reserved)
78	(reserved)	(reserved)
7A	(reserved)	(reserved)
7C	(reserved)	(reserved)
7E	(reserved)	(reserved)

Address (HEX)	WRITE	READ
	Register Name	Register Name
80	(reserved)	transmit CGMS/TSCH indicate [A]
82	(reserved)	transmit CGMS/TSCH indicate [B]
84	transmit CGMS/TSCH indicate status	transmit CGMS/TSCH indicate status
86	transmit EMI/OE setting	transmit EMI/OE setting
88	(reserved)	(reserved)
8A	(reserved)	(reserved)
8C	(reserved)	(reserved)
8E	(reserved)	(reserved)
90	(reserved)	(reserved)
92	(reserved)	(reserved)
94	(reserved)	(reserved)
96	(reserved)	(reserved)
98	(reserved)	(reserved)
9A	(reserved)	(reserved)
9C	(reserved)	(reserved)
9E	(reserved)	(reserved)
A0	(reserved)	(reserved)
A2	(reserved)	(reserved)
A4	(reserved)	(reserved)
A6	(reserved)	(reserved)
A8	(reserved)	(reserved)
AA	(reserved)	(reserved)
AC	(reserved)	(reserved)
AE	(reserved)	(reserved)

Address (HEX)	WRITE	READ
	Register Name	Register Name
B0	(reserved)	(reserved)
B2	(reserved)	(reserved)
B4	(reserved)	(reserved)
B6	(reserved)	(reserved)
B8	(reserved)	(reserved)
BA	(reserved)	(reserved)
BC	(reserved)	(reserved)
BE	(reserved)	(reserved)
C0	(reserved)	(reserved)
C2	(reserved)	(reserved)
C4	(reserved)	(reserved)
C6	(reserved)	(reserved)
C8	(reserved)	(reserved)
CA	(reserved)	(reserved)
CC	(reserved)	(reserved)
CE	(reserved)	(reserved)
D0	(reserved)	(reserved)
D2	(reserved)	(reserved)
D4	(reserved)	(reserved)
D6	(reserved)	(reserved)
D8	(reserved)	(reserved)
DA	(reserved)	(reserved)
DC	(reserved)	(reserved)
DE	(reserved)	(reserved)

Address (HEX)	WRITE	READ
	Register Name	Register Name
E0	(reserved)	(reserved)
E2	(reserved)	(reserved)
E4	(reserved)	(reserved)
E6	(reserved)	(reserved)
E8	(reserved)	(reserved)
EA	(reserved)	(reserved)
EC	(reserved)	(reserved)
EE	(reserved)	(reserved)
F0	(reserved)	(reserved)
F2	(reserved)	(reserved)
F4	(reserved)	(reserved)
F6	(reserved)	(reserved)
F8	(reserved)	(reserved)
FA	(reserved)	(reserved)
FC	(reserved)	(reserved)
FE	(reserved)	(reserved)

Chapter 7 Internal Register Function Description

This chapter explains the details of the internal register of MB86617A.

7.1. Mode-control Register

Mode-control register is the register that performs the relative setting of various operation mode of this LSI.

AD	R/W	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
00h	R/W	-	-	-	-	CPS soft reset	clk off	s-ID store	Cp_ trhrough	-	-	-	Iso-FIFO no clr	Asyn-FIFOs el	send/rec	TSP stand-by	CP stand-by
Initial Value		'0'	'0'	'0'	'0'	'0'	'0'	'1'	'0'	'0'	'0'	'0'	'1'	'0'	'1'	'1'	'1'

BIT	Bit Name	Action	Value	Function
15 - 12	reserved	Read	-	Always indicate '0'.
		Write	-	Always write in '0'.
11	CPS soft reset	Read/ Write	-	PHY/LINK is reset by writing '0' after writing '1' (not automatic clear) Note: 1) Perform read modify write so as not to re-write other bit. 2) Write '0' after 500 ns minimum passed after writing '1'.
10	clk off	Read/ Write	0	Not stop clock for providing to TSP I/F, CP I/F and data bridge.
			1	Stop clock for providing to TSP I/F, CP I/F and data bridge when PMODE input terminal is in 'H'.
9	s-ID store Note 1)	Read/ Write	0	Deletes Self-ID packet in spite of receiving it during bus reset.
			1	In case of receiving Self-ID packet during bus reset process, this bit stores 512 byte at maximum accompanying with both Asynchronous receive FIFO and Asynchronous transmit FIFO.
8	Cp_through	Read/ Write	0	Enable CP-IC interface.(Needs external CP IC)
			1	Disable CP-IC interface. CP-IC interface is internally by passed.
7	Sync_in	Read/ Write	0	TSSYNCA and TSSYNCB signals are neccesary to detect the first byte of the input data to TSP interface.
			1	TSSYNCA and TSSYNCB signals are not neccesary to detect the first byte of the input data to TSP interface.
6	Sync_out	Read/ Write	0	TSSYNCA and TSSYNCB signals are not asserted when the data is outputted from TSP interface.
			1	TSSYNCA and TSSYNCB signals are asserted when the data is outputted from TSP interface.
5	reserved	Read	0	Always indicate '0'.
		Write	0	Always write in '0'.
4	Iso-FIFO no clr	Read/ Write	0	Clears receive Isochronous-FIFO when bus reset occurred.
			1	Does not clear Isochronous-FIFO when bus reset occurred.

BIT	Bit Name	Action	value	Function
3	Asyn-FIFO sel	Read/ Write	0	Uses 2K byte FIFO on LINK I/F side of bridge for Isochronous transmit/receive.
			1	Uses 2K byte FIFO on LINK I/F side of bridge for Asynchronous transmit/receive.
2	send/rec	Read/ Write	0	Uses 2K byte FIFO for Asynchronous transmit with Asyn-FIFO sel (bit3) '1'.
			1	Uses 2K byte FIFO for Asynchronous receive with Asyn-FIFO sel (bit3) '1'.
1	TSP stand-by	Read/ Write	0	Activates TSP -IC I/F terminal output.
			1	Disables TSP-IC I/F terminal output, and brings it in high impedance status.
0	CP stand-by	Read/ Write	0	Activates CP I/F terminal output.
			0	Disables CP I/F terminal output, and brings it in high impedance status.

Note 1) Refer to "Self-ID Packet Receive Operation" for the internal operation flow and read-out flow of with this bit set at '1'.

7.2. flag & status Register

flag & status register indicates the status of this LSI and data access inquiries.

AD	R/W	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
02h	R	IPC busy	tran ready	tran busy	ISO cycle	A-Tx-buff empty	A-Rx-buff empty	-	-	-	-	-	sleep	data req	recv busy	cmstr	INT
Initial Value		'0'	'0'	'0'	'0'	'1'	'1'	'0'	'0'	'0'	'0'	'0'	'0'	'0'	'0'	'0'	'0'

BIT	Bit Name	Action	Value	Function
15	IPC busy	Read	0	Indicates that receipt of instruction is available.
			1	Indicates that receipt of instruction is not available.
14	tran ready	Read	0	Indicates that bus reset or forced sleep is being executed, and transmit/receive of packet is unavailable.
			1	Indicates that bus reset is completed and forced sleep is not being executed, and transmit/receive of packet is available.
13	tran busy	Read	0	Indicates that packet transmit is not being executed or in the process of packet receive addressed to this node.
			1	Indicates that packet transmit is being executed or in the process of packet receive addressed to this node.
12	ISO cycle	Read	0	Indicates that Isochronous cycle is not being executed.
			1	Indicates that Isochronous cycle is being executed by transmit or receive of cycle start packet.
11	A-Tx-buff Empty	Read	0	Indicates that Asynchronous transmit specific buffer is not empty.
			1	Indicates that Asynchronous transmit specific buffer is empty.
10	A-Rx-buff Empty	Read	0	Indicates that Asynchronous receive specific buffer is not empty.
			1	Indicates that Asynchronous receive specific buffer is empty.
9 – 5	reserved	Read	0	Always indicate '0'.

BIT	Bit Name	Action	Value	Function
4	sleep	Read	0	Indicates that the device is not in forced sleep.
			1	Indicates that the device is in forced sleep by accepting "Start sleep" (01h) instruction.
3	data req	Read	0	Indicates that no data is stored in ASYNC receive specific buffer.
			1	Indicates that data is stored in ASYNC receive specific buffer.
2	recv busy Note 2)	Read	0	Indicates that packet receive is not in busy mode.
			1	Indicates that packet receive is in busy mode due to receipt of Asynchronous packet and self-ID packet.
1	cmstr	Read	0	Indicates that node is not the cycle master now.
			1	Node is the cycle master now.
0	INT	Read	0	Interrupt indicate register does not have interrupt.
			1	Interrupt indicate register has interrupt.

Note 1) IEEE1394 block is in internal reset status until integrated PLL is locked after turning the power ON. PHY layer and Link layer do not operate during this period.

Note 2) In case that Asynchronous packet addressed to this node is received with this Bit indicate '1', it transmits "ack busy X".

7.3. instruction-fetch Register

instruction-fetch register is the register that writes in instructions for this LSI, and consists of the instruction code and operand.
Refer to "Chapter 9 Instruction" for each instruction code and operand code.

AD	R/W	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
04h	R/W	Instruction code								operand							
Initial Value		"00h"								"00h"							

BIT	Bit Name	Action	Value	Function
15 - 8	instruction code	Read/ Write	-	Specify each instruction code.
7 - 0	operand	Read/ Write	-	Specify required operand for each instruction code. Write '0' into all bits for instructions without operand.

Note) Before writing in instruction for this register, read out IPC busy Bit (bit15) of "7.2. flag & status Register", and confirm that the IPC busy value is '0'.

7.4. interrupt-factor Indicate Register/interrupt-mask Setting Register

interrupt-factor indicate register is the register that indicates interrupt reported by this LSI.
Refer to "Chapter 10 Interrupt" for measure against and details of each Bit and interrupt factor.
interrupt-mask setting register is the register that controls mask of each interrupt factor generated by this LSI.

AD	R/	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
06h	R	Interrupt-factor															
	W	interrupt-mask															
08h	R	Interrupt-factor															
	W	interrupt-mask															
Initial Value		'0'	'0'	'0'	'0'	'0'	'0'	'0'	'0'	'0'	'0'	'0'	'0'	'0'	'0'	'0'	'0'

BIT	Bit Name	Action	Value	Function
15 - 0	interrupt-factor	Read	0	Indicate that interrupt factors are not generated.
			1	Indicate that interrupt factors are generated. After reading out this register, clear to '0' automatically.
	interrupt-mask	Write	0	Do not mask interrupt factors.
			1	Mask interrupt factors. Interrupt factors masked by setting of this register are neither stored in interrupt indicate register nor assert INT signal.

7.5. Receive Acknowledge Indicate Register

Receive Acknowledge indicate register is the register that indicates received Acknowledge packet addressed to itself.
Read out this register after interrupt report of "Asynchronous packet send".

AD	R/W	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0Ah	R	-	-	-	-	-	-	-	-	Receive ack-code				Receive ack-parity			
Initial Value		'0'	'0'	'0'	'0'	'0'	'0'	'0'	'0'	"0 h"				"0 h"			

BIT	Bit Name	Action	Value	Function
15 - 8	reserved	Read	-	Always indicate '0'.
7 - 4	Receive Acknowledge-code	Read	-	Indicate code of received Acknowledge packet addressed to it. (MSB: bit7, LSB: bit5)
3 - 0	Receive Acknowledge-parity	Read	-	Indicate parity of received Acknowledge packet addressed to it. (MSB: bit3, LSB: bit0)

Note) In case of not receiving Acknowledge within specified time, this register indicates "00h" and reports interrupt of "Acknowledge missing".

7.6. A-buffer Data Port Receive/Transmit

This integrated register is the buffer access port for both ASYNC receive specific buffer and ASYNC transmit specific one.
Read data is able to be read out IEEE1394 packet data in the order received. (MSB: 1ST read)
Write data is transmitted as IEEE1394 packet data in the order written in. (MSB: 1ST write)

AD	R/W	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0Ch	R	ASYNC Receive Specific Buffer Data															
	W	ASYNC Transmit Specific Buffer Data															
Initial Value		Undefined															

BIT	Bit Name	Action	Value	Function
15 - 0	ASYNC Receive Specific Buffer Data	Read	-	Read out port of Asynchronous receive specific buffer. (MSB: bit15, LSB: bit0)
	ASYNC Transmit Specific Buffer Data	Write	-	Write in port of Asynchronous transmit specific buffer. (MSB: bit15, LSB: bit0)

7.7. TSP Transmit Information Setting Register [A]

TSP transmit information setting register [A] is the register that makes settings for transmit packet processed by bridge-Ach.

AD	R/W	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
10h	R/W	Tx start -A	Tx end -A	Tx select -A	set TS-ID-A						Tx form -A	input DSS size-A	EMI select -A	set EMI-A		27M count -A	pat mask-A
Initial Value		'0'	'0'	'0'	"00 h"						'0'	'0'	'0'	"00 b"		'0'	'0'

BIT	Bit Name	Action	Value	Function
15	Tx start-A	Read/ Write	0	Automatically clears when transmit process is started with bridge-Ach after setting at '1'.
			1	Starts transmit processing with bridge-Ach.
14	Tx end-A	Read/ Write	0	Automatically clears when transmit process is stopped by bridge-Ach after setting at '1'.
			1	Stops transmit process by bridge-Ach.
13	Tx select-A	Read/ Write	0	Outputs 'L' to SELTSPA output terminal.
			1	Outputs 'H' to SELTSPA output terminal.
12 - 7	set TS-ID-A	Read/ Write	-	Set TSCH classification ID to be stored at FIFO of bridge-Ach. (MSB: bit12, LSB: bit7)
6	Tx form-A	Read/ Write	0	Processes transmit data as MPEG2-TS.
			1	Processes transmit data as DSS packet.
5	input DSS size-A	Read/ Write	0	Processes transmit DSS packet as 140 byte.
			1	Processes transmit DSS packet as 130 byte.

BIT	Bit Name	Action	Value	Function
4	EMI select-A	Read/ Write	0	Selects CGMS information input from TSP -IC as EMI information to be output to CP-IC.
			1	Selects setting value of set EMI-A (bit3 to 2) as EMI information to be output to CP-IC.
3 - 2	set EMI-A	Read/ Write	-	Set EMI information to be output to CP-IC. Valid only when EMI select -A (bit4) is '1'. (MSB: bit3, LSB: bit2)
1	27M count-A	Read/ Write	0	Does not insert internal 27 MHz counter value to System clock count ran ge of DSS packet header.
			1	Inserts internal 27 MHz counter value to System clock count range of DSS packet header.
0	port mask -A	Read/ Write	0	Does not mask port A input of TSP-IC interface. Read in input data from port A at transmit.
			1	Masks port A input of TSP -IC interface. Does not read in input data from port A at transmit.

7.8. TSP Transmit Information Setting Register [B]

TSP transmit information setting register [B] is the register that makes settings for transmit packet processed by bridge-Bch.

AD	R/W	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
12h	R/W	Tx start -B	Tx end -B	Tx select -B	set TS-ID-B						Tx form -B	input DSS size-B	EMI select -B	set EMI-B		27M count -B	pat mask-B
Initial Value		'0'	'0'	'0'	"00 h"						'0'	'0'	'0'	"00 b"		'0'	'0'

BIT	Bit Name	Action	Value	Function
15	Tx start-B	Read/ Write	0	Automatically clears when transmit process is started with bridge -Bch after setting at '1'.
			1	Starts transmit process with bridge-Bch.
14	Tx end-B	Read/ Write	0	Automatically clears when transmit process is stopped by bridge-Bch after setting at '1'.
			1	Stops transmit process by bridge-Bch.
13	Tx select-B	Read/ Write	0	Outputs 'L' to SELTSPB output terminal.
			1	Outputs 'H' to SELTSPB output terminal.
12 - 7	set TS-ID-B	Read/ Write	-	Set TSCH classification ID to be stored at FIFO of bridge-Bch. (MSB: bit12, LSB: bit7)
6	Tx form-B	Read/ Write	0	Processes transmit data as MPEG2-TS packet.
			1	Processes transmit data as DSS packet.
5	input DSS size-B	Read/ Write	0	Processes transmit DSS packet as 140 byte.
			1	Processes transmit DSS packet as 130 byte.

BIT	Bit Name	Action	Value	Function
4	EMI select-B	Read/ Write	0	Selects CGMS information input from TSP -IC as EMI information to be output to CP-IC.
			1	Selects setting value of set EMI-A (bit3 to 2) as EMI information to be output to CP-IC.
3 - 2	set EMI-B	Read/ Write	-	Set EMI information to be output to CP-IC. Valid only when EMI select -A (bit4) is '1'. (MSB: bit3, LSB: bit2)
1	27M count-B	Read/ Write	0	Does not insert internal 27 MHz counter to System clock count range of DSS packet header.
			1	Inserts internal 27 MHz counter to System clock count range of DSS packet header.
0	port mask -B	Read/ Write	0	Does not mask port B input of TSP-IC interface. Reads in input data from port A at transmit.
			1	Masks port B input of TSP-IC interface. Does not read in input data from port A at transmit.

7.9. Transmit Offset Setting Register [A]

Transmit offset setting register [A] is the register that sets offset value added to cycle-time-monitor value. Its aim is to generate source packet header (Time-stamp) added to transmit packet processed by bridge-Ach. (Max. 32 ms)
Time-stamp value is generated on the basis of cycle-time-monitor value at input of first byte of source packet from TSP-IC.

AD	R/W	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
14h	R/W	reserved												transmit-offset-A (high)			
16h	R/W	transmit-offset-A (low)															
Initial Value		"0000 h"															

BIT	Bit Name	Action	Value	Function
15 - 4 (high)	reserved	Read	-	Always indicate '0'.
		Write	-	Always write in '0'.
3 - 0 (high) 15 - 12 (low)	transmit-offset-A	Read/ Write	-	Set value to be added to cycle-count range of cycle-time-monitor. Setting range is 0h to FFh. (unit=125µS).
11 - 0				Set value to be added to cycle-offset range of cycle-time-monitor. Setting range is 0h to C00h. (unit=1/24.576 MHz).

7.10. Transmit Offset Setting Register [B]

Transmit offset setting register [B] is the register that sets offset value added to cycle-time-monitor value Its aim is to generate source packet header (Time-stamp) added to transmit packet processed by bridge-Bch. (Max. 32 ms)
Time-stamp value is generated on the basis of cycle-time-monitor value at input of first byte of source packet from TSP-IC.

AD	R/W	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
18h	R/W	reserved												transmit-offset-B (high)			
1Ah	R/W	transmit-offset-B (low)															
Initial Value		"0000 h"															

BIT	Bit Name	Action	Value	Function
15 - 4 (high)	reserved	Read	-	Always indicate '0'.
		Write	-	Always write in '0'.
3 - 0 (high) 15 - 12 (low)	transmit-offset-B	Read/ Write	-	Set value to be added to cycle-count range of cycle-time-monitor. Setting range is 0h to FFh. (unit=125µS).
11 - 0				Set value to be added to cycle-offset range of cycle-time-monitor. Setting range is 0h to C00h. (unit=1/24.576MHz).

7.11. TSP Receive Information Setting Register

TSP receive information setting register performs the setting for outputting received packet to TSP -IC

AD	R/W	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1Ch	R/W	TV2B	TV1B	-	-	output DSS size-B	DV-EN	DSS-EN	TS-EN	TV2A	TV1A	-	-	output DSS size-A	TCLKSL	CMPSEL	TSCMP
Initial Value		'0'	'0'	'0'	'0'	'0'	'0'	'0'	'1'	'0'	'0'	'0'	'0'	'0'	'0'	'0'	'0'

BIT	Bit Name	Action	Value	Function
15	TV2B	Read/ Write	0	Does not output packet received by bridge -Bch to port B of TSP -IC I/F.
			1	Outputs packet received by bridge-Bch to port B of TSP -IC I/F.
14	TV1B	Read/ Write	0	Does not output packet received by bridge -Bch to port A of TSP -IC I/F.
			1	Outputs packet received by bridge-Bch to port A of TSP-IC I/F.
13 - 12	reserved	Read	-	Always indicates '0'.
		Write	-	Always write in '0'.
11	output DSS size-B	Read/ Write	0	Outputs DSS packet received by bridge -Bch, with DSS packet header attached, to TSP-IC in unit of 140 byte.
			1	Outputs DSS packet received by bridge-Bch, without attachment of DSS packet header, to TSP-IC in unit of 130 byte. Removed DSS packet header is stored at receive DSS packet header indicate register [B].
10	DV-EN	Read/ Write	0	Deletes received data and reports FMT error when DV data is received. ISO packet header and CIP header are indicated in register.
			1	Allows receiving DV data.
9	DSS-EN	Read/ Write	0	Deletes received data and reports FMT error when DSS data is received. ISO packet header and CIP header are indicated in register.
			1	Allows receiving DSS data.

BIT	Bit Name	Action	Value	Function
8	TS-EN	Read/ Write	0	Deletes received data and reports FMT error when MPEG2-TS data is received. ISO packet header and CIP header are indicated in register.
			1	Allows receiving MPEG2-TS data.
7	TV2A	Read/ Write	0	Does not output the packet received by bridge-Ach to port B of TSP-IC I/F.
			1	Outputs the packet received by bridge-Ach to port B of TSP-IC I/F.
6	TV1A	Read/ Write	0	Does not output the packet received by bridge-Ach to port A of TSP-IC I/F.
			1	Outputs the packet received by bridge-Ach to port A of TSP-IC I/F.
5 - 4	reserved	Read	-	Always indicates '0'.
		Write	-	Always write in '0'.
3	output DSS size-	Read/ Write	0	Outputs DSS packet with DSS packet header received by bridge-Bch to TSP-IC in unit of 140 byte.
			1	Outputs DSS packet without DSS packet header received by bridge-Ach to TSP-IC in unit of 130 byte. Removed DSS packet header is stored at receive DSS packet header indicate register [A].
2	TCLKSL	Read/ Write	0	Outputs received data to TSP-IC in synchronization with 6.144 MHz TSCLK.
			1	Outputs received data to TSP-IC in synchronization with 3.072 MHz TSCLK.
1	CMPSEL	Read/ Write	0	Outputs to port A when TSCMP (bit0) is '1'.
			1	Outputs to port B when TSCMP (bit0) is '1'.
0	TSCMP	Read/ Write	0	Does not merge packet received by Ach and Bch.
			1	Outputs to one TSP-IC after merging packets received by Ach and Bch.

Note 1) Do not set TV2B (bit15), TV1B (bit14), and DV1B (bit12) to '1' simultaneously.
Note 2) Do not set TV2A (bit7), TV1A (bit6), and DV1A (bit4) to '1' simultaneously.
Note 3) Do not set TV2B (bit15) and TV2A (bit7) to '1' simultaneously.
Note 4) Do not set TV1B (bit14) and TV1A (bit6) to '1' simultaneously.
Note 5) Do not set '1' to TV2B (bit15), TV1B (bit14), TV2A (bit7) and TV1A(bit6) when TSCMP (bit0) is set to '1'.
Note 6) FMT error is reported when receiving data format other than DV-EN (bit10), DSS-EN (bit9) and TS-EN (bit8) regardless of their settings.

Register setting value and selection of output port are shown in the table below.

Receive Status	Bit 15	Bit 14	Bit 7	Bit 6	Bit 1	Bit 0	TSP -IC I/F Port A	TSP -IC I/F Port B
	TV2B	TV1B	TV2A	TV1A	CMP SEL	TS CMP		
1ch receive	0	0	0	1	0	0	Processing-Ach Receive data	-
	0	0	1	0	0	0	-	Processing-Ach Receive data
	0	1	0	0	0	0	Processing-Bch Receive data	-
	1	0	0	0	0	0	-	Processing-Bch Receive data
2ch receive	1	0	0	1	0	0	Processing-Ach Receive data	Processing-Bch Receive data
	0	1	1	0	0	0	Processing-Bch Receive data	Processing-Ach Receive data
	0	0	0	0	0	1	Processing-Ach+Bch Receive data	-
	0	0	0	0	1	1	-	Processing-Ach+Bch Receive data

7.12. Receive DSS Packet Header Indicate Register [A]/Transmit DSS Packet Header Setting Register [A]

Receive DSS packet header indicate register [A] indicates DSS packet header range of DSS packet received by bridge-Ach.
Transmit DSS packet header setting register [A] sets DSS packet header range of DSS packet received by bridge-Ach.

AD	R/W	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1Eh	R	Rx-SIF-A	Rx-System clock count-A(high)														
	W	Tx-SIF-A	Tx-System clock count-A(high)														
20h	R	Rx-System clock count-A(low)								Rx-EF-A	Reserved						
	W	Tx-System clock count-A(low)								Tx-EF-A	reserved						
22h	R	reserved															
	W	reserved															
24h	R	reserved															
	W	reserved															
26h	R	reserved															
	W	reserved															
Initial Value		"0000 h"															

BIT	Bit Name	Active	Value	Function
15 (1Eh)	Rx-SIF-A	Read	-	Indicates SIF range of received DSS packet header.
	Tx-SIF-A	Write	-	Write in SIF range of transmits DSS packet header.
14 - 0 (1Eh) 15 - 8(20h)	Rx-System clock count-A	Read	-	Indicate System clock count range of received DSS packet header. (MSB: 1Eh-bit14 , LSB: 20h-bit8)
	Tx-System clock count-A	Write	-	Write in System clock count range of transmit DSS packet header. (MSB: 1Eh-bit14 , LSB: 20h-bit8)
7(20h)	Rx-EF-A	Read	-	Indicates EF range of received DSS packet header.
	Tx-EF-A	Write	-	Write in EF range of transmits DSS packet header.
6 - 0(20h) 15 - 0(22h) 15 - 0(24h) 15 - 0(26h)	reserved	Read	-	Indicates reserved range of received DSS packet header.
		Write	-	Write in reserved range of transmit DSS packet header.

7.13. Receive DSS Packet Header Indicate Register [B]/Transmit DSS Packet Header Setting Register [B]

Receive DSS packet header indicate register [B] indicates DSS packet header range of DSS packet received by bridge-Bch.
Transmit DSS packet header setting register [B] sets DSS packet header range of DSS packet received by bridge-Bch.

AD	R/W	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
28h	R	Rx-SIF-B	Rx-System clock count-B (high)														
	W	Tx-SIF-B	Tx-System clock count-B (high)														
2Ah	R	Rx-maximum bit rate-B (low)								Rx-EF-B	reserved						
	W	Tx-maximum bit rate-B (low)								Tx-EF-B	reserved						
2Ch	R	reserved															
	W	reserved															
2Eh	R	reserved															
	W	reserved															
30h	R	reserved															
	W	reserved															
Initial Value		"0000 h"															

BIT	Bit Name	Action	Value	Function
15 (28h)	Rx-SIF-B	Read	-	Indicates SIF range of receive DSS packet header.
	Tx-SIF-B	Write	-	Write in SIF range of transmit DSS packet header.
14 - 0 (28h) 15 - 8(2Ah)	Rx-System clock count-B	Read	-	Indicate System clock count range of receive DSS packet header. (MSB: 28h-bit14, LSB: 2Ah-bit8)
	Tx-System clock count-B	Write	-	Write in System clock count range of transmit DSS packet header. (MSB: 28h-bit14, LSB: 2Ah-bit8)
7(2Ah)	Rx-EF-B	Read	-	Indicates EF range of received DSS packet header.
	Tx-EF-B	Write	-	Write in EF range of transmit DSS packet header.
6 - 0 (2Ah) 7 - 0 (2Ch) 15 - 0 (2Eh) 15 - 0 (30h)	reserved	Read	-	Indicates reserved range of receive DSS packet header.
		Write	-	Write in reserved range of transmit DSS packet header.

7.14. TSP Status Register

TSP status register indicates status of TSP -IC I/F.

AD	R/W	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
32h	R	CG chg-B	TS chg-B	no 47h-B	TSP FIFOfull-B	TSP FIFO emp-B	Tx-length-err-B	-	-	CG chg-A	TS chg-A	no 47h-A	TSP FIFO full-A	TSP FIFO emp-A	Tx-length-err-A	-	-
Initial Value		'0'	'0'	'0'	'0'	'1'	'0'	'0'	'0'	'0'	'0'	'0'	'0'	'1'	'0'	'0'	'0'

BIT	Bit Name	Action	Value	Function
15	CG chg-B	Read	0	Indicates that CGMS information input from port B of TSP IC I/F is not changed.
			1	Indicates that CGMS information corresponding to TSCH classification ID of same type input from port B of TSP IC I/F is changed. Clears to '0' by lead of this register.
14	TS chg-B	Read	0	Indicates that TS classification ID input from port B of TSP IC I/F is not changed.
			1	Indicates that TSCH classification ID input from port B of TSP IC I/F is not consistent with TSCH classification ID (10h-bit12 to 7 set TS-ID-A or 12h-bit12 to 7 set TS-ID-B) to be stored to FIFO. Clears to '0' by lead of this register.
13	no 47h-B	Read	0	Indicates that synchronization byte of received MPEG2-TS input from CP-IC by bridge-Bch is 47h
			1	Indicates that synchronization byte of received MPEG2-TS input from CP-IC by bridge-Bch is not 47h Clears to '0' by lead of this register.
12	TSP FIFO full-B	Read	0	Indicates that FIFO on TSP IC I/F side of bridge-Bch is not full.
			1	Indicates that FIFO on TSP IC I/F side of bridge-Bch is full.
11	TSP FIFO emp-B	Read	0	Indicates that FIFO on TSP IC I/F side of bridge-Bch is not empty.
			1	Indicates that FIFO on TSP IC I/F side of bridge-Bch is empty.
10	Tx-length-err-B	Read	0	Indicates that transmit data length input from TSP IC I/F is normal.
			1	Indicates that transmit data length input from TSP IC I/F is not consistent with specified format data length. Deletes transmit data without writing into FIFO. Clears to '0' by lead of this register.

BIT	Bit Name	Active	Value	Function
9~8	reserved	Read	-	Always indicate '0'.
7	CG chg-A	Read	0	Indicates that CGMS information input from port A of TSP IC I/F is not changed.
			1	Indicates that CGMS information input from port A of TSP IC I/F is changed. Clears to '0' by lead of this register.
6	TS chg-A	Read	0	Indicates that TS classification ID input from port A of TSP IC I/F is not changed.
			1	Indicates that TSCH classification ID input from port B of TSP IC I/F is not consistent with TSCH classification ID (10h-bit12 to 7 set TS-ID-A or 12h-bit12 to 7 set TS-ID-B) to be stored to FIFO. Clears to '0' by lead of this register.
5	no 47h-A	Read	0	Indicates that synchronization byte of received MPEG2-TS input from CP-IC by bridge-Bch is 47h
			1	Indicates that synchronization byte of received MPEG2-TS input from CP-IC by bridge-Bch is not 47h Clears to '0' by lead of this register.
4	TSP FIFO full-A	Read	0	Indicates that FIFO on TSP IC I/F side of bridge-Ach is not full.
			1	Indicates that FIFO on TSP IC I/F side of bridge-Ach is full.
3	TSP FIFO emp-A	Read	0	Indicates that FIFO on TSP IC I/F side of bridge-Ach is not empty.
			1	Indicates that FIFO on TSP IC I/F side of bridge-Ach is empty.
2	Tx-length-err-A	Read	0	Indicates transmit data length input from TSP IC I/F is normal.
			1	Indicates transmit data length input from TSP IC I/F is not consistent with specified format data length. Deletes transmit data without writing into FIFO. Clears to '0' by lead of this register.
1 - 0	reserved	Read	-	Always indicate '0'.

7.15. Data Bridge Transmit Information Setting Register 1 [A]

Data bridge transmit information setting register 1 [A] is the register that sets CIP header range added to transmit packet processed by bridge-Ach.

AD	R/W	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
34h	R/W	Tx SID-A						Tx DBS-A								Tx FN-A	
Initial Value		"00 h"						"00 h"								"00 b"	

BIT	Bit Name	Action	Value	Function
15 - 10	Tx SID-A	Read/ Write	-	Write in SID range of transmit CIP header. (MSB: bit15, LSB: bit10)
9 - 2	Tx DBS-A	Read/ Write	-	Write in DBS range of transmit CIP header. (MSB: bit9, LSB: bit2) MPEG2-TS at transmit: "00000110" b DSS at transmit: "00001001" b
1 - 0	Tx FN-A	Read/ Write	-	Write in FN range of transmit CIP header. (MSB: bit1, LSB: bit0) MPEG2-TS at transmit: "11" b DSS at transmit: "10" b

7.16. Data Bridge Transmit Information Setting Register 2 [A]

Data bridge transmit information setting register 2 [A] is the register that sets CIP header range, transmit channel, and speed added to transmit packet processed by bridge-Ach.

AD	R/W	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
36h	R/W	Tx FMT-A						Tx TSF-A	Tx channel-A						Tx speed-A		-
Initial Value		"00" h						'0'	"00" h						"00" b		'0'

BIT	Bit Name	Action	Value	Function
15 - 10	Tx FMT-A	Read/ Write	-	Write in FMT range of transmit CIP header. (MSB: bit15, LSB: bit10) MPEG2-TS at transmit: "100000" b DSS at transmit: "100001" b
9	Tx TSF-A	Read/ Write	-	Write in TSF range of transmits CIP header.
8 - 3	Tx channel-A	Read/ Write	-	Write in channel range of transmit Isochronous packet header. (MSB: bit8, LSB: bit3)
2 - 1	Tx speed-A	Read/ Write	-	Write in transmit packet speed. (MSB: bit2, LSB: bit1) s100 at transmit: "00" b s200 at transmit: "01" b s400 at transmit: "10" b
0	reserved	Read	-	Always indicates '0'.
		Write	-	Always writes in '0'.

7.17. Data Bridge Transmit Information Setting Register 3 [B]

Data bridge transmit information setting register 3 [B] is the register that sets CIP header range added to transmit packet processed by bridge-Bch.

AD	R/W	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
38h	R/W	Tx SID-B						Tx DBS-B								Tx FN-B	
Initial Value		"00 h"						"00 h"								"00 b"	

BIT	Bit Name	Action	Value	Function
15 - 10	Tx SID-B	Read/ Write	-	Write in SID range of transmit CIP header. (MSB: bit15, LSB: bit10)
9 - 2	Tx DBS-B	Read/ Write	-	Write in DBS range of transmit CIP header. (MSB: bit9, LSB: bit2) MPEG2-TS at transmit: "00000110" b DSS at transmit: "00001001" b
1 - 0	Tx FN-B	Read/ Write	-	Write in FN range of transmit CIP header. (MSB: bit1, LSB: bit0) MPEG2-TS at transmit: "11" b DSS at transmit: "10" b

7.18. Data Bridge Transmit Information Setting Register 4 [B]

Data bridge transmit information setting register 4 [B] is the register that sets CIP header range, transmit channel and speed added to transmit packet processed by bridge-Bch.

AD	R/W	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
3Ah	R/W	Tx FMT-B						Tx TSF-B	Tx channel-B						Tx speed-B		-
Initial Value		"00" h						'0'	"00" h						"00" b		'0'

BIT	Bit Name	Action	Value	Function
15 - 10	Tx FMT-B	Read/ Write	-	Write in FMT range of transmit CIP header. (MSB: bit15, LSB: bit10) MPEG2-TS at transmit: "100000" b DSS at transmit: "100001" b
9	Tx TSF-B	Read/ Write	-	Write in TSF range of transmit CIP header.
8 - 3	Tx channel-B	Read/ Write	-	Write in channel range of transmit Isochronous packet header. (MSB: bit8, LSB: bit3)
2 - 1	Tx speed-B	Read/ Write	-	Write in transmit packet speed. (MSB: bit2, LSB: bit1) s100 at transmit: "00" b s200 at transmit: "01" b s400 at transmit: "10" b
0	reserved	Read	-	Always indicates '0'.
		Write	-	Always writes in '0'.

7.19. Data Bridge Receive Information Setting Register

Data bridge receive information register performs the setting of receive packet.

AD	R/W	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
3Ch	R/	Rx start -B	Rx end -B	Rx channel-B						Rx start -A	Rx end -A	Rx channel-A					
Initial Value		'0'	'0'	"00 h"						'0'	'0'	"00 h"					

BIT	Bit Name	Action	Value	Function
15	Rx start-B	Read/ Write	0	Automatically clears when receive process is executed by bridge-Bch after setting at '1'.
			1	Executes receive process by bridge-Bch.
14	Rx end-B	Read/ Write	0	Automatically clears when receive process is stopped by bridge-Bch after setting at '1'.
			1	Stops receive process by bridge-Bch.
13~8	Rx channel-B	Read/ Write	-	Write in Isochronous packet channel to be received by bridge-Bch. (MSB: bit8, LSB: bit3)
7	Rx start-A	Read/ Write	0	Automatically clears when receive process is executed by bridge-Ach after setting at '1'.
			1	Starts receive process by bridge-Ach.
6	Rx end-A	Read/ Write	0	Automatically clears when receive process is stopped by bridge-Ach after setting at '1'.
			1	Stops receive process by bridge-Ach.
5 - 0	Rx-channel-A	Read/ Write	-	Write in Isochronous packet channel to be received by bridge-Ach (MSB: bit5, LSB: bit0)

7.20. Transmit Packet Link/Split Setting Register

Transmit packet link/split setting register is the register that sets number of link and split of source packets to be transmitted.

AD	R/W	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
3Eh	R/W	o/e select-B	Tx o/e-B	NF5 SPB	SPQB			DBQB		o/e select-A	Tx o/e-A	NF5 SPA	SPQA			DBQA	
Initial Value		'0'	'0'	'0'	"000 b"			"00 b"		'0'	'0'	'0'	"000 b"			"00 b"	

BIT	Bit Name	Action	Value	Function
15	o/e select-B	Read/ Write	0	Selects odd/even value to be input from CP-IC as odd/even range of Isochronous packet header to be transmitted by bridge-Bch.
			1	Selects Tx o/e-B (bit14) setting value as odd/even range of Isochronous packet header to be transmitted by bridge-Bch
14	Tx o/e-B	Read/ Write	-	Write in odd/even range of transmit Isochronous packet header. Valid with o/e select-B (bit15) setting value '1', and reads in this setting value to transmit Isochronous packet header.
13	NF5SPB	Read/ Write	0	Executes 2SP combined transmission as FIFO NFULL operation when setting of 2SP separated transmission or combined transmission for less than 2SP. With more than 3 SP, executes according to setting.
			1	Executes 5 SP combined transmission at FIFO FULL.
12 - 10	SPQB	Read/ Write	-	Write in number of link of source packet processed by bridge-Bch.
9 - 8	DBQB	Read/ Write	-	Write in number of split of source packet processed by bridge-Bch.
7	o/e select-A	Read/ Write	0	Selects odd/even value to be input from CP-IC as odd/even range of Isochronous packet header to be transmitted by bridge-Bch.
			1	Selects Tx o/e-B b (bit6) setting value as odd/even range of Isochronous packet header to be transmitted by bridge-Bch
6	Tx o/e-A	Read/ Write	-	Write in odd/even range of transmit Isochronous packet header. Valid with o/e select-B (bit7) setting value '1', and reads in this setting value to transmit Isochronous packet header.

BIT	Bit Name	Action	Value	Function
5	NF5SPA	Read/ Write	0	Executes 2SP combined transmission as FIFO NFULL operation when setting of 2SP separated transmission or combined transmission for less than 2SP. With more than 3 SP, executes according to setting.
			1	Executes 5 SP combined transmission at FIFO FULL.
4 - 2	SPQA	Read/ Write	-	Write in number of links for source packet processed by bridge-Ach.
1 - 0	DBQA	Read/ Write	-	Write in number of links for source packet processed by bridge-Ach.

Note)

>SPQ[2:0] ----- Please specify link number of source packet.
Valid setting values are 0 - 5.
Processes assuming there are no settings from microcomputer during '0' setting.
When 6 - 7 are set, it is regarded to be 5 source packet link.

>DBQ[1:0] ---- Please specify split number of source packet.
'00' ---No setting from microcomputer.
'01' ---2 splits
'10' ---4 splits
'11' ---8 splits, 4 splits at DSS

> When the setting values of both SPQ [2:0] and DBQ [1:0] are not '0', follow the setting of SPQ [2:0].
When the setting values of both SPQ [2:0] and DBQ [1:0] are '0' (no setting from microcomputer), LSI automatically executes link process in 1 source packet unit.

7.21. Late Packet Decision Range Setting Register [A]

Late packet decision range setting register [A] is the register that sets Late decision range of source packet to be transmitted by bridge-Ach.

AD	R/W	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
40h	R/W	late range-A															
Initial Value		"0000 h"															

BIT	Bit Name	Action	Value	Function
15 - 8	late range-A	Read/ Write	-	Write in Late packet decision range. Setting range is 0h to FFh (unit: 125µS).
7 - 0				Write in Late packet decision range. Setting range is 0h to C0h (unit: 16/24.576MHz).

Note)

Late packet decision is performed by comparing the time difference between SPH (Source Packet Header) and CTR (Cycle Time Monitor).

-Transmit:

Packet is transmitted normally when calculation result of "SPH" minus "CTR" for source packet transmitted from Bridhe-Ach is within the "late range-A + '0000'h".

If it is out of range, Late packet process is performed. The packet concerned is deleted and transmit late is reported.

Set the upper 16 bit of the setting value for transmit offset setting register[A] (14h to 16h).

-Receive:

Received packet is output at the point of "SPH = CTR" when calculation result of "SPH" minus "CTR" for source packet received at Bridhe-Ach is within the "late range-A + '0000'h" (the value this register is shifted 4 bits to the left).

If it is out of range, Late packet process is performed. The packet concerned is deleted and receive late is reported.

7.22. Late Packet Decision Range Setting Register [B]

Late packet decision range setting register [B] is the register that sets Late decision range of source packet to be transmitted by bridge-Bch.

AD	R/W	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
42h	R/W	late range-B															
Initial Value		"0000 h"															

BIT	Bit Name	Action	Value	Function
15 - 8	late range-B	Read/ Write	-	Write in Late packet decision range. Setting range is 0h to FFh (unit: 125µS).
7 - 0				Write in Late packet decision range. Setting range is 0h to C0h (unit: 16/24.576MHz).

Note)

Late packet decision is performed by comparing the time difference between SPH (Source Packet Header) and CTR (Cycle Time Monitor).

-Transmit:

Packet is transmitted normally when calculation result of "SPH" minus "CTR" for source packet transmitted from Bridhe-Bch is within the "late range-B + '0000'h".

If it is out of range, Late packet process is performed. The packet concerned is deleted and transmit late is reported.

Set the upper 16 bit of the setting value for transmit offset setting register[B] (14h to 16h).

-Receive:

Received packet is output at the point of "SPH = CTR" when calculation result of "SPH" minus "CTR" for source packet received at Bridhe-Bch is within the "late range-B + '0000'h" (the value this register is shifted 4 bits to the left).

If it is out of range, Late packet process is performed. The packet concerned is deleted and receive late is reported.

7.23. Receive Isochronous Packet Header Indicate Register 1 [A]

Receive Isochronous packet header indicate register 1 [A] is the register that indicates Isochronous packet header information received by bridge-Ach.

AD	R/W	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
44h	R	-	-	-	-	-	-	-	Rx EMI-A		Rx o/e-A	Rx SID-A					
Initial Value		'0'	'0'	'0'	'0'	'0'	'0'	'0'	"00 b"		'0'	"00 h"					

BIT	Bit Name	Action	Value	Function
15 - 9	reserved	Read	-	Always indicate '0'.
8 - 7	Rx EMI-A	Read	-	Indicate EMI range of receive Isochronous packet header. (MSB: bit8, LSB: bit7)
6	Rx o/e-A	Read	-	Indicates odd/even range of receive Isochronous packet header.
5 - 0	Rx SID-A	Read	-	Indicate SI range of CIP header of receive Isochronous packet. (MSB: bit8, LSB: bit3)

7.24. Receive Isochronous Packet Header Indicate Register 2 [A]

Receive Isochronous packet header indicate register 2 [A] is the register that indicates Isochronous packet CIP header information received by bridge-Ach.

AD	R/W	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
46h	R	-	-	-	-	Rx FMT-A						Rx 56-A	Rx STYPE-A				
Initial Value		'0'	'0'	'0'	'0'	"3F"						'0'	"00 h"				

BIT	Bit Name	Action	Value	Function
15 - 12	reserved	Read	-	Always indicate '0'.
11 - 6	Rx FMT-A	Read	-	Indicate FMT range of receive Isochronous packet CIP header. (MSB: bit11, LSB: bit6)
5	Rx 56-A	Read	-	Indicates 50/60 range of receive Isochronous packet CIP header when receiving DV. Indicates TSF range of receive Isochronous packet CIP header when receiving MPEG2-TS or DSS.
4 - 0	Rx STYPE-A	Read	-	Indicate STYPE range of CIP header of receive Isochronous packet. (MSB: bit4, LSB: bit0)

7.25. Receive Isochronous Packet Header Indicate Register 3 [B]

Receive Isochronous packet header indicate register 3 [B] is the register that indicates Isochronous packet header information received by bridge-Bch.

AD	R/W	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
48h	R	-	-	-		-	-	-	Rx EMI-B		Rx o/e-B	Rx SID-B					
Initial Value		'0'	'0'	'0'	'0'	'0'	'0'	'0'	"00 b"		'0'	"00 h"					

BIT	Bit Name	Action	Value	Function
15 - 9	reserved	Read	-	Always indicate '0'.
8 - 7	Rx EMI-B	Read	-	Indicate EMI range of receive Isochronous packet header. (MSB: bit8, LSB: bit7)
6	Rx o/e-B	Read	-	Indicates odd/even range of receive Isochronous packet header.
5 - 0	Rx SID-B	Read	-	Indicate SI range of CIP header of receive Isochronous packet. (MSB: bit5, LSB: bit0)

7.26. Receive Isochronous Packet Header Indicate Register 4 [B]

Receive Isochronous packet header indicate register 4 [B] is the register that indicates Isochronous packet CIP header information received by bridge-Bch.

AD	R/W	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
4Ah	R	-	-	-	-	Rx FMT-B						Rx 56-B	Rx STYPE-B				
Initial value		'0'	'0'	'0'	'0'	"3F"						'0'	"00 h"				

BIT	Bit Name	Action	Value	Function
15 - 12	reserved	Read	-	Always indicate '0'.
11 - 6	Rx FMT-B	Read	-	Indicate FMT range of receive Isochronous packet CIP header. (MSB: bit11, LSB: bit6)
5	Rx 56-B	Read	-	Indicates 50/60 range of receive Isochronous packet CIP header when receiving DV. Indicates TSF range of receive Isochronous packet CIP header when receiving MPEG2-TS or DSS.
4 - 0	Rx STYPE-B	Read	-	Indicate STYPE range of CIP header of receive Isochronous packet. (MSB: bit4, LSB: bit0)

7.27. FIFO Reset Setting Register

FIFO reset setting register sets force reset of bridge and each FIFO.

AD	R/W	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
4Ch	R/W	reset-B	reset TSP FIFO-B	reset BRG FIFO-B	-	-	-	-	-	reset-A	reset TSP FIFO-A	reset BRG FIFO-A	-	-	-	-	-
Initial Value		'0'	'0'	'0'	'0'	'0'	'0'	'0'	'0'	'0'	'0'	'0'	'0'	'0'	'0'	'0'	'0'

BIT	Bit Name	Action	Value	Function
15	reset-B	Read/ Write	0	Releases forced reset of bridge-Bch.
			1	Executes forced reset of bridge-Bch.
14	reset TSP FIFO-B	Read/ Write	0	Releases FIFO reset on TSP -IC I/F side of bridge-Bch.
			1	Resets FIFO on TSP-IC I/F side of bridge-Bch.
13	reset BRG FIFO-B	Read/ Write	0	Releases FIFO reset on LINK-I/F side of bridge-Bch.
			1	Resets FIFO on LINK I/F side of bridge-Bch.
12 - 8	reserved	Read	-	Always indicate '0'.
		Write	-	Always write in '0'.
7	reset-A	Read/ Write	0	Releases forced reset of bridge-Ach.
			1	Execute forced reset of bridge-Ach.
6	reset TSP FIFO-A	Read/ Write	0	Releases FIFO reset on TSP -IC I/F side of bridge-Ach.
			1	Resets FIFO on TSP-IC I/F of bridge-Ach.
5	reset BRG FIFO-A	Read/ Write	0	Releases FIFO reset on LINK-I/F side of bridge-Ach.
			1	Resets FIFO on LINK I/F side of bridge-Ach.
4 - 0	Reserved	Read	-	Always indicate '0'.
		Write	-	Always write in '0'.

Note 1) This register is not cleared automatically.
After writing '1', check the state and then write '0'.
Note 2) Do not set '1' to this register during transmit/receive execution.

7.28. Data Bridge Transmit/Receive Status Register [A]

Data bridge transmit/receive status register indicates status of packet to be transmitted/received by bridge-Ach.

AD	R/W	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
4Eh	R	Tx busy-A	Rx busy-A	Rx 1STP-A	Rx EMI chg-A	Rx o/e chg-A	Rx dlen err-A	-	Tx late-A	Rx late-A	Rx 56 err-A	Rx stype err-A	BRG FIFO full-A	BRG FIFO emp-A	Rx DBC err-A	Rx CIP err-A	Rx FMT err-A
Initial Value		'0'	'0'	'0'	'0'	'0'	'0'	'0'	'0'	'0'	'0'	'0'	'0'	'1'	'0'	'0'	'0'

BIT	Bit Name	Action	Value	Function
15	Tx busy-A	Read	0	Indicates that bridge-Ach is not in the process of transmit. Indicates '0' when Tx end-A (10h-bit14) is set at '1' and transmit process is stopped.
			1	Indicates that bridge-Ach is in the process of transmit. Indicates '1' when Tx start-A (10h-bit15) is set at '1' and transmit process is started.
14	Rx busy-A	Read	0	Indicates that bridge-Ach is not in the process of receive. Indicates '0' when Rx end-A (3Ch-bit6) is set at '1' and receive process is stopped.
			1	Indicates that bridge-Ach is in the process of receive. Indicates '1' when Rx start-A (3Ch-bit7) is set at '1' and receive process is started.
13	Rx 1STP-A	Read	0	Indicates that Isochronous packet received after starting receive process is not the first packet received.
			1	Indicates that the first Isochronous packet is received after receive process is started. Clears to '0' by lead of this register.
12	Rx EMI chg-A	Read	0	Indicates that EMI information of received Isochronous packet header is not changed.
			1	Indicates that EMI information of received Isochronous packet header has changed from just former EMI information of packet received by Isochronous-cycle. Clears to '0' by lead of this register.
11	Rx o/e chg-A	Read	0	Indicates that odd/even information of received Isochronous packet header is not changed.
			1	Indicates that odd/even information of received Isochronous packet header has changed from just former odd/even information of packet received by Isochronous-cycle. Clears to '0' by lead of this register.

BIT	Bit Name	Action	Value	Function
10	Rx dlen-err-A	Read	0	Indicates that the data length of received packet is same as specified data length in format.
			1	Indicates that the data length of received packet differs to the specified data length in the format. Clears to '0' by lead of this register.
9	reserved	Read	-	Always indicates '0'.
8	Tx late-A	Read	0	Indicates that transmit packet is transmitted normally.
			1	Indicates that transmit packet became Late packet. Delete packet, and not transmit. Clears to '0' by lead of this register.
7	Rx late-A	Read	0	Indicates that the received packet is normal.
			1	Indicates that received packet was Late packet. Delete packet, and not output to TSP-IC. Clears to '0' by lead of this register.
6	Rx 56 err-A	Read	0	Indicates that 50/60 range of CIP header for received Isochronous packet is '0'.
			1	Indicates that 50/60 range of CIP header of received Isochronous packet is '1' Clears to '0' by lead of this register.
5	Rx stype err-A	Read	0	Indicates that STYPE range of CIP header of received Isochronous packet is '00000' or '00001'.
			1	Indicates that STYPE range of CIP header of received Isochronous packet is other than '00000' or '00001'. Clears to '0' by lead of this register.
4	BRG FIFO full-A	Read	0	Indicates that FIFO on LINK I/F side of bridge-Ach is not full.
			1	Indicates that FIFO on LINK I/F side of bridge-Ach is full.
3	BRG FIFO emp-A	Read	0	Indicates that FIFO on LINK I/F side of bridge-Ach is not empty.
			1	Indicates that FIFO on LINK I/F side of bridge-Ach is empty.
2	Rx DBC err-A	Read	0	Indicates that DBC range of CIP header of received Isochronous packet is normal.
			1	Indicates that DBC range of CIP header of received Isochronous packet received is not consecutive. Clears to '0' by lead of this register.

BIT	Bit Name	Action	Value	Function
1	Rx CIP err-A	Read	0	Indicates that CIP header of received Isochronous packet is normal.
			1	Indicates that CIP header of received Isochronous packet has an error. Clears to '0' by lead of this register.
0	Rx FMT err-A	Read	0	Indicates that FMT range of CIP header of received Isochronous packet is the value allowed to be received at DV-EN, DSS-EN or TS-EN (1Ch –bit10 to 8) (DV='00000', MPEG2='10000' or DSS='100001').
			1	Indicates that FMT range of CIP header of received Isochronous packet is other than the value allowed to be received at DV-EN, DSS-EN or TS-EN (1Ch –bit10 to 8) (DV='00000', MPEG2='10000' or DSS='100001'). Clears to '0' by reading of this register.

7.29. Data Bridge Transmit/Receive Status Register [B]

Data bridge transmit/receive status register [B] indicates status of packet transmitted/received by bridge-Bch.

AD	R/W	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
50h	R	Tx busy-B	Rx busy-B	Rx 1STP-B	Rx EMI chg-B	Rx o/e chg-B	Rx dlen err-B	-	Tx late-B	Rx late-B	Rx 56 err-B	Rx stype err-B	BRG FIFO full-B	BRG FIFO emp-B	Rx DBC err-B	Rx CIP err-B	Rx FMT err-B
Initial Value		'0'	'0'	'0'	'0'	'0'	'0'	'0'	'0'	'0'	'0'	'0'	'0'	'1'	'0'	'0'	'0'

BIT	Bit Name	Action	Value	Function
15	Tx busy-B	Read	0	Indicates that bridge-Bch is not in the process of transmit. Indicates '0' when Tx end-B (12h-bit14) is set at '1' and transmit process is stopped.
			1	Indicates that bridge-Bch is in the process of transmit. Indicates '1' when Tx start-B (12h-bit15) is set at '1' and transmit process is started.
14	Rx busy-B	Read	0	Indicates that bridge-Bch is not in the process of receive. Indicates '0' when Rx end-B (3Ch-bit14) is set at '1' and receive process is stopped.
			1	Indicates that bridge-Bch is in the process of receive. Indicates '1' when Rx start-B (3Ch-bit15) is set at '1' and receive process is started.
13	Rx 1STP-B	Read	0	Indicates that received Isochronous packet after starting receive process is not the first receive packet.
			1	Indicates that the first Isochronous packet is received after starting receive process. Clears to '0' by lead of this register.
12	Rx EMI chg-B	Read	0	Indicates that EMI information of receive Isochronous packet header is not changed.
			1	Indicates that EMI information of receive Isochronous packet header has changed from just former EMI information of packet received by Isochronous-cycle. Clears to '0' by lead of this register.
11	Rx o/e chg-B	Read	0	Indicates that odd/even information of receive Isochronous packet header is not changed.
			1	Indicates that odd/even information of receive Isochronous packet header has changed from just former odd/even information of packet received by Isochronous-cycle. Clears to '0' by lead of this register.

BIT	Bit Name	Action	Value	Function
10	Rx dlen-err-B	Read	0	Indicates that data length of receive packet is same as specified data length in format.
			1	Indicates that data length of receive packet differs to the specified data length in the format. Clears to '0' by lead of this register.
9	Reserved	Read	-	Always indicates '0'.
8	Tx late-B	Read	0	Indicates that transmit packet is transmitted normally.
			1	Indicates that transmit packet became Late packet. Delete packet, and not transmit. Clears to '0' by lead of this register.
7	Rx late-B	Read	0	Indicates that received packet is normal.
			1	Indicates that received packet was Late packet. Deletes packet, and does not output to TSP-IC. Clears to '0' by lead of this register.
6	Rx 56 err-B	Read	0	Indicates that 50/60 range of CIP header of received Isochronous packet is '0'.
			1	Indicates that 50/60 range of CIP header of received Isochronous packet is '1' Clears to '0' by lead of this register.
5	Rx stype err-B	Read	0	Indicates that STYPE range of CIP header of received Isochronous packet is '00000' or '00001'.
			1	Indicates that STYPE range of CIP header of received Isochronous packet is other than '00000' or '00001'. Clears to '0' by lead of this register.
4	BRG FIFO full-B	Read	0	Indicates that FIFO on LINK I/F side of bridge-Ach is not full.
			1	Indicates that FIFO on LINK I/F side of bridge-Ach is full.
3	BRG FIFO emp-B	Read	0	Indicates that FIFO on LINK I/F side of bridge-Ach is not empty.
			1	Indicates that FIFO on LINK I/F side of bridge-Ach is empty.
2	Rx DBC err-B	Read	0	Indicates that DBC range of CIP header of received Isochronous packet is normal.
			1	Indicates that DBC range of CIP header of received Isochronous packet is not consecutive. Clears to '0' by lead of this register.

BIT	Bit Name	Action	Value	Function
1	Rx CIP err-B	Read	0	Indicates that CIP header of received Isochronous packet is normal.
			1	Indicates that CIP header of received Isochronous packet has an error. Cleared to '0' by lead of this register.
0	Rx FMT err-B	Read	0	Indicates that FMT range of CIP header of received Isochronous packet is the value allowed to be received at DV-EN, DSS-EN or TS-EN (1Ch –bit10 to 8) (DV='00000', MPEG2='10000' or DSS='100001').
			1	Indicates that FMT range of CIP header of received Isochronous packet is other than the value allowed to be received at DV-EN, DSS-EN or TS-EN (1Ch – bit10 to 8) (DV='00000', MPEG2='10000' or DSS='100001'). Clears to '0' by reading of this register.

7.30. Isochronous Channel Monitor Register

Isochronous channel monitor register is the register that indicates Isochronous packet channel flowing through 1394 bus.

AD	R/W	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
52h	R	Isochronous channel monitor1															
54h	R	Isochronous channel monitor2															
56h	R	Isochronous channel monitor3															
58h	R	Isochronous channel monitor4															
Initial Value		"0000 h"															

BIT	Bit Name	Action	Value	Function
15 - 0	Isochronous channel monitor	Read	-	Indicate that '1' at Bit corresponding to channel number of Isochronous packet flowing through 1394 bus. 52h-bit15 - 0: channel0 - channel15 54h-bit15 - 0: channel16 - channel31 56h-bit15 - 0: channel32 - channel47 58h-bit15 - 0: channel48 - channel63

7.31. Cycle-timer-monitor Indicate Register

Cycle-timer-monitor indicate register indicates value of integrated cycle-timer register.

AD	R/W	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
5Ah	R	cycle-timer-monitor (hi)															
5Ch	R	cycle-timer-monitor (lo)															
Initial Value		"0000 h"															

BIT	Bit Name	Action	Value	Function
15 - 0	cycle-timer-monitor	Read	-	Indicate value of built-in cycle-timer register. (MSB: bit15, LSB: bit0)

Note) This register latches the lower word (5A h) by reading out lower word (5Ch), and releases latch by reading out upper word. To read out this register, make sure to read out in the order of 5Ch → 5A h, two as a set.

7.32. Ping Time Monitor Register

Ping time monitor register is the register that indicates time period of transmitting request packet to receiving response packet to the request.

AD	R/W	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
5Eh	R	Ping time monitor															
Initial Value		"0000 h"															

BIT	Bit Name	Action	Value	Function
15 - 0	Ping time monitor	Read	-	Indicate time period from transmitting request packet to receiving response packet to the request. Counts by 20ns unit. (MSB: bit15, LSB: bit0)

7.33. PHY/LINK Register/Address Setting Register

PHY/LINK register/address setting register is the register that sets address in order to access PHY/LINK register indirectly. PHY/LINK register indicated with address set by this register can be accessed from PHY/LINK register/access port.

AD	R/W	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
60h	R/W	-	-	-	-	-	-	-	-	-	phy/link-addr						
Initial Value		'0'	'0'	'0'	'0'	'0'	'0'	'0'	'0'	'0'	"00 h"						

BIT	Bit Name	Action	Value	Function
15 - 7	reserved	Read	-	Always indicate '0'.
		Write	-	Always write in '0'.
6 - 0	phy/link-addr	Read/ Write	-	Set address of PHY/LINK register to be accessed. (MSB: 6, LSB: 0)

7.34. PHY/LINK Register Access Port

PHY/LINK register access port is the port to access PHY/LINK register indirectly. PHY/LINK register indicated with address set by PHY/LINK register/address setting register can be accessed from this port.

AD	R/W	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
62h	R/W	phy/link-data															
Initial Value		"0000 h"															

BIT	Bit Name	Action	Value	Function
15 - 0	phy/link-data	Read	-	Indicates PHY/LINK register contents defined by address set by PHY/LINK register/address setting register. (MSB: 15, LSB: 0)
		Write	-	Executes write in the process of register defined by this address set by PHY/LINK register/address setting register. (MSB: 15, LSB: 0)

7.35. Revision Indicate Register

Revision indicate register is the register that indicates chip revision of this LSI.

AD	R/W	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
64h		Revision code (hi)															
66h	R	Revision code (lo)															
Initial Value		Fixed															

BIT	Bit Name	Action	Value	Function
15 - 0	Revision code	Read	-	Indicate Revision code. (MSB: bit15, LSB: bit0)

7.36. Transmit CGMS/TSCH Indicate Register [A]

Transmit CGMS/TSCH indicate register [A] indicates CGMS information and identification of TS type for source packet input from port A at TSP IC I/F.

AD	R/W	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
80h	R	CGMSA-2		TSCHA-2						CGMSA-1			TSCHA-1				
Initial Value		"00 b"		"00 h"						"00 b"			"00 h"				

BIT	Bit Name	Action	Value	Function
15 - 14	CGMSA-2	Read	-	Indicates CGMS information for source packet indicated in TSCHA-2 (bit13 to 8). (MSB: bit15, LSB: bit14)
13 - 8	TSCHA-2	Read	-	Indicates if ID of TS type for source packet input from port A at TSP IC I/F is different from that in low bit (TSCHA-1). (MSB: bit13, LSB: bit8)
7 - 6	CGMSA-1	Read	-	Indicates CGMS information for source packet indicated in TSCHA-1 (bit5 to 0). (MSB: bit7, LSB: bit6)
5 - 0	TSCHA-1	Read	-	Indicates ID of TS type for source packet input first from port A at TSP IC I/F (MSB: bit5, LSB: bit0)

7.37. Transmit CGMS/TSCH Indicate Register [B]

Transmit CGMS/TSCH indicate register [B] indicates CGMS information and identification of TS type for source packet input from port B at TSP IC I/F.

AD	R/W	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
82h	R	CGMSB-2		TSCHB-2						CGMSB-1			TSCHB-1				
Initial Value		"00 b"		"00 h"						"00 b"			"00 h"				

BIT	Bit Name	Action	Value	Function
15 - 14	CGMSB-2	Read	-	Indicates CGMS information for source packet indicated in TSCHB-2 (bit13 to 8). (MSB: bit15, LSB: bit14)
13 - 8	TSCHB-2	Read	-	Indicates if ID of TS type for source packet input from port B at TSP IC I/F is different from that in low bit (TSCHB-1). (MSB: bit13, LSB: bit8)
7 - 6	CGMSB-1	Read	-	Indicates CGMS information for source packet indicated in TSCHB-1 (bit5 to 0). (MSB: bit7, LSB: bit6)
5 - 0	TSCHB-1	Read	-	Indicates ID of TS type for source packet input first from port B at TSP IC I/F (MSB: bit5, LSB: bit0)

7.38. Transmit CGMS/TSCH Indicate Status Register

Transmit CGMS/TSCH indicate status register indicates validity of source packet input from TSP IC I/F.

AD	R/W	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
84h	R/W	-	-	-	-	-	act-TSC HB	vld-TSC HB-2	vld-TSC HB-1	-	-	-	-	-	act-TSC HA	vld-TSC HA-2	vld-TSC HA-1
Initial Value		'0'	'0'	'0'	'0'	'0'	'0'	'0'	'0'	'0'	'0'	'0'	'0'	'0'	'0'	'0'	'0'

BIT	Bit Name	Action	Value	Function
15 - 11	reserved	Read	-	Always indicate '0'.
		Write	-	Always write in '0'.
10	Act-TSCHB	Read	0	Indicates that the packet indicated in CGMSB-1 and TSCHB-1 (82h-bit7 to 0) was finally input from port B at TSP IC I/F.
			1	Indicates that the packet indicated in CGMSB-2 and TSCHB-2 (82h-bit15 to 8) was finally input from port B at TSP IC I/F.
		Write	-	Clears to '0' by writing "1".
9	Vld-TSCHB-2	Read	0	Indicates that the value indicated in CGMSB-2 and TSCHB-2 (82h-bit15 to 8) is invalid.
			1	Indicates that the value indicated in CGMSB-2 and TSCHB-2 (82h-bit15 to 8) is valid.
		Write	-	Clears to '0' by writing "1".
8	Vld-TSCHB-1	Read	0	Indicates that the value indicated in CGMSB-1 and TSCHB-1 (82h-bit7 to 0) is invalid.
			1	Indicates that the value indicated in CGMSB-1 and TSCHB-1 (82h-bit7 to 0) is valid.
		Write	-	Clears to '0' by writing "1".
7 - 3	reserved	Read	-	Always indicate '0'.
		Write	-	Always write in '0'.

BIT	Bit Name	Action	Value	Function
2	act-TSCHA	Read	0	Indicates that the packet indicated in CGMSA-1 and TSCHA-1 (80h-bit7 to 0) was finally input from port A at TSP IC I/F.
			1	Indicates that the packet indicated in CGMSA-2 and TSCHA-2 (80h-bit15 to 8) was finally input from port A at TSP IC I/F.
		Write	-	Clears to '0' by writing "1".
1	vld-TSCHA-2	Read	0	Indicates that the value indicated in CGMSA-2 and TSCHA-2 (80h-bit15 to 8) is invalid.
			1	Indicates that the value indicated in CGMSA-2 and TSCHA-2 (80h-bit15 to 8) is valid.
		Write	-	Clears to '0' by writing "1".
0	vld-TSCHA-1	Read	0	Indicates that the value indicated in CGMSA-1 and TSCHA-1 (80h-bit7 to 0) is invalid.
			1	Indicates that the value indicated in CGMSA-1 and TSCHA-1 (80h-bit7 to 0) is valid.
		Write	-	Clears to '0' by writing "1".

7.39. Transmit EMI/OE Setting Register

Transmit EMI/OE setting register sets EMI information and Odd/Even value added to empty packet until valid data is transmitted.

AD	R/W	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
86h	R/W	IPH select -B	IPH EMI-B		IPH OE-B	-	-	-	-	IPH select -A	IPH EMI-A		IPH OE-A	-	-	-	-
Initial Value		'0'	"00 b"		'0'	'0'	'0'	'0'	'0'	'0'	"00 b"		'0'	'0'	'0'	'0'	'0'

BIT	Bit Name	Action	Value	Function
15	IPH select -B	Read/ Write	0	Sets the default value (EMI='00', OE = '0') as EMI information and Odd/Even value added to IPH of empty packet until valid data is transmitted after starting transmission.
			1	Selects the setting value of IPH EMI-B (bit14 to 13) and IPH OE-B (bit 12) as EMI information and Odd/Even value added to IPH of empty packet until valid data is transmitted after starting transmission.
14 - 13	IPH EMI-B	Read/ Write	-	Set EMI information which are set in IPH of empty packet transmitted from bridge-Bch. Valid only when IPH select-B (bit15) is set to '1'. (MSB: bit14, LSB: bit13) EMI information after transmitting valid data depends on the setting of EMI select-B (12h-bit4).
12	IPH OE-B	Read/ Write	-	Set Odd/Even value which is set in IPH of empty packet transmitted from bridge-Bch. Valid only when IPH select-B (bit15) is set to '1'. EMI information after transmitting valid data depends on the setting of o/e select-B (3Eh-bit15).
11 - 8	reserved	Read	-	Always indicate '0'.
		Write	-	Always write in '0'.
7	IPH select -A	Read/ Write	0	Sets the default value (EMI='00', OE = '0') as EMI information and Odd/Even value added to IPH of empty packet until valid data is transmitted after starting transmission.
			1	Selects the setting value of IPH EMI-A (bit6 to 5) and IPH OE-A (bit 4) as EMI information and Odd/Even value added to IPH of empty packet until valid data is transmitted after starting transmission.

BIT	Bit Name	Action	Value	Function
6 - 5	IPH EMI-A	Read/ Write	-	Set EMI information which are set in IPH of empty packet transmitted from bridge-Ach. Valid only when IPH select-A (bit7) is set to '1'. (MSB: bit6, LSB: bit5) EMI information after transmitting valid data depends on the setting of EMI select-A (10h-bit4).
4	IPH OE-A	Read/ Write	-	Set Odd/Even value which is set in IPH of empty packet transmitted from bridge-Ach. Valid only when IPH select-A (bit7) is set to '1'. EMI information after transmitting valid data depends on the setting of o/e select-A (3Eh-bit8).
3 - 0	reserved	Read	-	Always indicate '0'.
		Write	-	Always write in '0'.

Chapter 8 PHY/INK Register Function Description

This chapter explains the Physical Register and Link register that enables to access from PHY/LINK register access port (address 62h) by setting PHYT/LINK register address setting register (address 60h) in detail.

8.1. PHY/LINK Register Table

Table of Physical Register and Link Register is shown below.

PHY/LINK addr	Write	Read
00h	(reserved)	Physical register #00
02h	Physical register #01	←
04h	(reserved)	Physical register #02
06h	(reserved)	Physical register #03
08h	Physical register #04	←
0Ah	Physical register #05	←
0Ch	(reserved)	Physical r egister #07
0Eh	(reserved)	Physical register #08
10h	(reserved)	Physical register #09
12h	Physical register #0A	←
14h	Physical register #0B	←
16h	Physical register #0C	←
18h	Physical register #0D	←
1Ah	Physical register #0E	←
1Ch	Physical register #0F	←
1Dh	(reserved)	Physical register #10
1Eh	(reserved)	Physical register #11
20h	(reserved)	Physical register #12
24h	(reserved)	Physical register #13
26h	(reserved)	Physical register #14
28h	(reserved)	Physical register #15
2Ah	(reserved)	Physic al register #16

PHY/LINK addr	Write	Read
2Ch	Physical register #17	←
2Eh	Physical register #18	←
30h	Physical register #19	←
32h	Physical register #1A	←
34h	Physical register #1B	←
36h	Physical register #1C	←
38h	Physical register #1D	←
3Ah	Physical register #1E	←
3Ch	Link register #00	←
3Eh	Link register #01	←
40h	Link register #02	←
42h	Link register #03	←

8.2. Physical register #00 (read)

Physical Register#00 is the register that indicates Physical ID, root status, and cable power st atus of this node.

phy/ link-addr	R/W	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
00 h	R	-	-	-	-	-	-	-	-	Physical_ID						R	PS
Initial value		'0'	'0'	'0'	'0'	'0'	'0'	'0'	'0'	"00 h"						'0'	'0'

Description of Each Bit

BIT	Bit name	Action	Value	Function
15 – 8	Reserved	Read	0	Always indicate '0'.
7 – 2	Physical_ID	Read	-	Indicate node No. of this node determined by Self-identify during processing bus reset. (MSB : 7 , LSB : 2) Effective after completion of bus reset.
1	R	Read	0	Indicates that this node is not root.
			1	Indicates that this node is root.
0	PS	Read	0	Indicates that the supplied cable power is below specification.
			1	Indicates that the supplied cable power is over specification.

8.3. Physical register #01 (read/write)

Physical Register#01 is the register that sets/indicates force-root and gap-count.
Do not write into this register except for the case that the node is Bus manager or Isochronous resource manager in the environment with no Bus manager.

phy/ link-addr	R/W	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
02 h	R/W	-	-	-	-	-	-	-	-	RHB	IRB	Gap_count					
Initial Value		'0'	'0'	'0'	'0'	'0'	'0'	'0'	'0'	'0'	'0'	"3F h"					

Description of Each Bit

BIT	Bit Name	Action	Value	Function
15 - 8	reserved	Read	-	Always indicate '0'.
		Write	-	Always write '0'.
7	RHB Note 1)	Read/ Write	0	This node does not try to be root during next bus reset.
			1	This node tries to be root during next bus reset.
6	IRB	Read/ Write	0	Does not perform bus reset.
			1	Performs bus reset. Automatically clears to "0" at the completion of bus reset.
5 - 0	Gap_count Note 2)	Read	-	Indicate current gap-count value (MSB: 5 , LSB: 0).
		Write	-	Set gap-count value (MSB: 5 , LSB: 0).

Note 1) This bit is automatically set by receiving the PHY configuration packet, too.
Note 2) This bit is automatically set by receiving the PHY configuration packet, too.
Also, this bit value returns to initial value at the second next bus reset.

8.4. Physical register #02 (read)

Physical Register#02 is the register that indicates if the extended PHY register map is in existence or not, and the number of ports (3 port).

phy/ link-addr	R/W	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
04 h	R	-	-	-	-	-	-	-	-	Extended			-	Total_ports			
Fixed value		‘0’	‘0’	‘0’	‘0’	‘0’	‘0’	‘0’	‘0’	“7 h”			‘0’	“3h”			

■ **Description of each Bit**

BIT	Bit Name	Action	Value	Function
15 - 8	reserved	Read	-	Always indicate ‘0’.
7 - 5	Extended	Read	-	Indicate that this node has the extended PHY register map. (MSB: 7 , LSB: 5) Always indicate fixed value “7 h”.
4	reserved	Read	-	Always indicates ‘0’.
3 - 0	Total_ports	Read	-	Indicate the number of ports held by this node (MSB: 4 , LSB: 0). Always indicate fixed value “3 h”.

8.5. Physical register #03 (read)

Physical Register#03 is the register that indicates max. transfer speed (S400) of this node.

phy/ link-addr	R/W	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
06 h	R	-	-	-	-	-	-	-	-	Max _speed			-	Delay			
Fixed value		'0'	'0'	'0'	'0'	'0'	'0'	'0'	'0'	'0'	'1'	'0'	'0'	'0'	'0'	'0'	'0'

■ **Description of Each Bit**

BIT	Bit Name	Action	Value	Function
15 - 8	reserved	Read	-	Always indicate '0'.
7 - 5	Max_speed	Read	-	Indicate max. transfer speed supporting PHY of this node (MSB: 7 , LSB: 5). Always indicates fixed value "010 b" (= S400).
4	reserved	Read	-	Always indicates '0'.
3 - 0	Delay	Read	-	Indicate Delay value at the receive signal repeat (MSB: 3 , LSB: 0). Always indicate fixed value "0000 b".

8.6. Physical register #04 (read/write)

Physical Register#04 is the register that sets the parameter of Self-ID packet to be transmitted by this node.

phy/ link-addr	R/W	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
08 h	R	-	-	-	-	-	-	-	-	Link_active	Contender	Jitter			Pwr_class		
	W											-	-	-			
Initial Value		'0'	'0'	'0'	'0'	'0'	'0'	'0'	'0'	'1'	'1'	'0'	'0'	'0'	'0'	'0'	'0'

■ **Description of Each Bit**

BIT	Bit Name	Action	Value	Function
15 - 8	reserved	Read	-	Always indicate '0'.
		Write	-	Always write in '0'.
7	Link_active Note 1)	Read/ Write	-	Set L bit (Link_active) value of Self-ID packet automatically transmitted by this node with the system power ON.
6	Contender Note 2)	Read/ Write	-	Set c bit (CONTENDER) value of Self-ID packet automatically transmitted by this node with the system power ON.
5 - 3	Jitter	Read	-	Indicate Jitter value at receive signal repeat. (MSB : 5 , LSB : 3) Always indicates fixed value "000 b".
		Write	-	Always write in '0'.
2 - 0	Pwr_class Note 3)	Read/ Write	-	Set pwr field (POWER_CLASS) value of Self-ID packet automatically transmitted by this node with the system power ON.

Note 1) L bit value of Self-ID packet that is automatically transmitted by this node with the cable supply power ON is always set at '0' regardless of the setting of this bit.

Note 2) c bit value of Self-ID packet that is automatically transmitted by this node with the cable supply power ON is always set at '0' regardless of the setting of this bit.

Note 3) pwr field value of Self-ID packet which is automatically transmitted by this node with the cable supply power ON is always set at the value of PWR3 - 1 terminal regardless of the setting of this bit.

8.7. Physical register #05 (read/write)

Physical Register#05 is the register indicating availability of cable supply power standard and timeout detect of arbitration state machine.

phy/ link-addr	R/W	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0A h	R/W	-	-	-	-	-	-	-	-	Resume_Int	ISBR	Loop	Pwr_fail	Timeout	Port_event	Enab_accel	Enab_multi
Initial Value		'0'	'0'	'0'	'0'	'0'	'0'	'0'	'0'	'0"	'0'	'0'	'0'	'0'	'0'	'0'	'0'

■ **Description of Each Bit**

BIT	Bit Name	Action	Value	Function
15 - 8	reserved	Read	-	Always indicate '0'.
		Write	-	Always write in '0'.
7	Resume_Int	Read/ Write	0	Does not indicate '1' at Port_event bit during resume processing.
			1	Indicates '1' at Port_event bit during resume processing.
6	ISBR	Read/ Write	0	Does not perform short bus reset.
			1	Performs short bus reset. Automatically clears to '0' at the completion of bus reset.
5	Loop	Read	0	Indicates that port connection is in a loop.
			1	Indicates that port connection is in a loop.
		Write	-	Clears the bit value to '0' by writing in '1'.
4	Pwr_fail	Read	0	Indicates that the cable supply power satisfies the standard.
			1	Indicates that the cable supply power does not satisfy the standard.
		Write	-	Clears the bit value to '0' by writing in '1'.
3	Timeout	Read	0	Indicates that timeout is not detected by arbitration state machine.
			1	Indicates that timeout is detected by arbitration state machine.
		Write	-	Clears the bit value to '0' by writing in '1'.

BIT	Bit Name	Action	Value	Function
2	Port_event	Read	0	Indicates that port event and resume processing have not occurred.
			1	Indicates that Connected, Bias, Disabled, Fault bit has changed when Int_enable bit is set at '1'. Indicates that resume processing was performed when Resume_Int bit is set at '1'.
		Write	-	Clears the bit value to '0' by writing in '1'.
1	Enab_accel	Read/ Write	0	Disables arbitration acceleration function.
			1	Enables arbitration acceleration function.
0	Enab_multi	Read/ Write	0	Disables multi-speed packet concatenation function.
			1	Enables multi-speed packet concatenation function.

8.8. Physical register #07, 08, 09 (read)

Physical Register#07, 08, 09 are the registers that indicate signal condition of IEEE1394 port and cable connection condition.

phy/ link-addr	R/W	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0C h	R	-	-	-	-	-	-	-	-	Astat-0		Bstate-0		Child-0	Connected0	-	-
0E h	R	-	-	-	-	-	-	-	-	Astat-1		Bstate-1		Child-1	Connected1	-	-
10 h	R	-	-	-	-	-	-	-	-	Astat-2		Bstate-2		Child-2	Connected2	-	-
Initial Value		'0'	'0'	'0'	'0'	'0'	'0'	'0'	'0'	'0'	'0'	'0'	'0'	'0'	'0'	'0'	'0'

■ **Description of Each Bit**

BIT	Bit Name	Action	Value	Function
15 - 8	reserved	Read	-	Always indicate '0'.
7 - 6	Astat-n	Read	-	Indicate TPA line state of 1394 port n (MSB : 7 , LSB : 6). 00 = invalid 01 = '1' 10 = '0' 11 = 'Z'
5 - 4	Bstat-n	Read	-	Indicate TPB line state of 1394 port n (MSB : 5 , LSB : 4). 00 = invalid 01 = '1' 10 = '0' 11 = 'Z'
3	Child-n	Read	0	Indicates that 1394 port n is parent port.
			1	Indicates that 1394 port n is children port.
2	Connected-n	Read	0	Indicates that cable is not connected to 1394 port n.
			1	Indicates that cable is connected to 1394 port n.
1 - 0	reserved	Read	-	Always indicate '0'

8.9. Physical register #0A, 0B, 0C (read/write)

Physical Register#0A, 0B, 0C are the registers that indicate bias detect condition of IEEE1394 installed in this node and performs setting of enable/disable of IEEE1394 port.

phy/ link-addr	R/W	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
12 h	R	-	-	-	-	-	-	-	-	-	-	-	-	-	-	Bias-0	Disabled-0
	W															-	
14h	R	-	-	-	-	-	-	-	-	-	-	-	-	-	-	Bias-1	Disabled-1
	W															-	
16h	R	-	-	-	-	-	-	-	-	-	-	-	-	-	-	Bias-2	Disabled-2
	W															-	
Initial Value		'0'	'0'	'0'	'0'	'0'	'0'	'0'	'0'	'0'	'0'	'0'	'0'	'0'	'0'	'0'	'0'

■ **Description of Each Bit**

BIT	Bit Name	Action	Value	Function
15 - 2	reserved	Read	-	Always indicates '0'.
		Write	-	Always write in '0'.
1	Bias-n	Read	0	Indicates that bias voltage is not detected at 1394 port n.
			1	Indicates that bias voltage is detected at 1394 port n.
		Write	-	Always indicates '0'.
0	Disabled-n	Read/ Write	0	Enables 1394 port n.
			1	Disable 1394 port n.

8.10. Physical register #0D, 0E, 0F (read/write)

Physical Register#0D, 0E, 0F are the registers that indicate maximum transfer speed of the node connected to IEEE1394 port installed in this node.

phy/ link-addr	R/W	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
18 h	R	-	-	-	-	-	-	-	-	Negotiated_speed-0			Int_enable-0	Fault-0	-	-	-
	W									-	-	-					
1A h	R	-	-	-	-	-	-	-	-	Negotiated_speed-1			Int_enable-1	Fault-1	-	-	-
	W									-	-	-					
1C h	R	-	-	-	-	-	-	-	-	Negotiated_speed-2			Int_enable-2	Fault-2	-	-	-
	W									-	-	-					
Initial value		'0'	'0'	'0'	'0'	'0'	'0'	'0'	'0'	'0'	'0'	'0'	'0'	'0'	'0'	'0'	'0'

■ **Description of Each Bit**

BIT	Bit Name	Action	Value	Function
15 - 8	reserved	Read	-	Always indicates'0'.
		Write	-	Always write in '0'.
7 - 5	Negotiated_ speed-n	Read	-	Indicate max. transfer speed between nodes connected to 1394 port n. (MSB: 7, LSB: 5) 000 = S100 001 = S200 010 = S400 011 - 111 = invalid
		Write	-	Always write in '0'.
4	Int_enable-n	Read/ Write	0	Does not indicate '1' at Port_event bit when Connected, Bias, Disabled, Fault bit changed.
			1	Indicates '1' at Port_event bit when Connected, Bias, Disabled, Fault bit changed.
3	Fault	Read	0	Indicates that suspend or resume processing is normal.
			1	Indicates that suspend or resume processing occurred error.
		Write	-	Clears the bit value to '0' by writing in '1'.
2 - 0	reserved	Read/ Write	-	Always indicates'0'.
			-	Always write in '0'.

8.11. Physical register #10 (read)

Physical Register#10 is the register that indicates Compliance_level of this node.

phy/ link-addr	R/W	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1E h	R	-	-	-	-	-	-	-	-	Compliance_level							
Fixed value		'0'	'0'	'0'	'0'	'0'	'0'	'0'	'0'	"01 h"							

Description of Each Bit

BIT	Bit Name	Action	Value	Function
15 - 8	reserved	Read	-	Always indicate '0'.
7 - 0	Compliance_level	Read	-	Indicate that this node supports P1394a standard. (MSB: 7 , LSB: 0) Always indicate fixe value "01 h".

8.12. Physical register #11, 12, 13 (read)

Physical Register#11, 12, 13 are the registers that indicate Vendor_ID of this node.

phy/ link-addr	R/W	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
20 h	R	-	-	-	-	-	-	-	-	Vendor_ID-hi							
Fixed Value		‘0’	‘0’	‘0’	‘0’	‘0’	‘0’	‘0’	‘0’	“00 h”							
22 h	R	-	-	-	-	-	-	-	-	Vendor_ID-mid							
Fixed Value		‘0’	‘0’	‘0’	‘0’	‘0’	‘0’	‘0’	‘0’	“00 h”							
24 h	R	-	-	-	-	-	-	-	-	Vendor_ID-lo							
Fixed Value		‘0’	‘0’	‘0’	‘0’	‘0’	‘0’	‘0’	‘0’	“0E h”							

Description of Each Bit

BIT	Bit Name	Action	Value	Function
15 - 8	reserved	Read	-	Always indicate ‘0’.
7 - 0	Vendor_ID	Read	-	Indicate Vendor ID of Fujitsu (MSB: 7, LSB: 0). Always indicate fixed value “00000E h”.

8.13. Physical register #14, 15, 16 (read)

Physical Register#14, 15, 16 are the registers that indicate Product_ID of this node.

phy/ link-addr	R/W	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
26 h	R	-	-	-	-	-	-	-	-	Product_ID-hi							
Fixed Value		‘0’	‘0’	‘0’	‘0’	‘0’	‘0’	‘0’	‘0’	“08 h”							
28 h	R	-	-	-	-	-	-	-	-	Product_ID-mid							
Fixed Value		‘0’	‘0’	‘0’	‘0’	‘0’	‘0’	‘0’	‘0’	“66 h”							
2A h	R	-	-	-	-	-	-	-	-	Product_ID-lo							
Fixed Value		‘0’	‘0’	‘0’	‘0’	‘0’	‘0’	‘0’	‘0’	“17 h”							

■ **Description of Each Bit**

BIT	Bit Name	Action	Value	Function
15 - 8	reserved	Read	-	Always indicate ‘0’.
7 - 0	Vendor_ID	Read	-	Indicate Product ID of this chip (MSB: 7, LSB: 0). Always indicate fixed value “086617 h”.

8.14. Physical register #17, 18, 19, 1A, 1B, 1C, 1D, 1E (read/write)

Physical Register#17, 18, 19, 1A, 1B, 1C, 1D, 1E are in the range of 8 bit X 8 Free_RAM.

phy/ link-addr	R/W	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
2C h	R/	-	-	-	-	-	-	-	-	Free_RAM-0							
2E h	R/W	-	-	-	-	-	-	-	-	Free_RAM-1							
30 h	R/	-	-	-	-	-	-	-	-	Free_RAM-2							
32 h	R/	-	-	-	-	-	-	-	-	Free_RAM-3							
34 h	R/	-	-	-	-	-	-	-	-	Free_RAM-4							
36 h	R/	-	-	-	-	-	-	-	-	Free_RAM-5							
38 h	R/	-	-	-	-	-	-	-	-	Free_RAM-6							
3A h	R/	-	-	-	-	-	-	-	-	Free_RAM-7							
Initial value		'0'	'0'	'0'	'0'	'0'	'0'	'0'	'0'	"00 h"							

■ **Description of Each Bit**

BIT	Bit Name	Action	Value	Function
15 - 8	reserved	Read	-	Always indicates'0'.
		Write	-	Always write in '0'.
7 - 0	Free_RAM	Read/ Write	-	Range of 8 bit X 8 Free RAM.

8.15. Link register#00 (read/write)

Link Register#00 is the register that sets this node to operate as cycle master.

phy/ link-addr	R/W	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
3Ch	R/W	-	-	-	-	-	-	-	-	-	-	cycle master	-	-	-	-	-
Initial Value		'0'	'0'	'0'	'0'	'0'	'0'	'0'	'0'	'0"	'0'	'1'	'0'	'0'	'0'	'0'	'0'

■ **Description of Each Bit**

BIT	Bit Name	Action	Value	Function
15 - 6	reserved	Read	-	Always indicate '0'.
		Write	-	Always write in '0'.
5	cycle master	Read	0	Does not cycle master.
			1	Operates as cycle master if it is root.
		Write	-	Sets the value of this bit at '1' by writing in '1'.
4 - 0	reserved	Read	-	Always indicate '0'.
		Write	-	Always write in '0'.

8.16. Link register#01 (read/write)

Link Register#00 is the register that sets this node to perform as cycle master.

phy/ link-addr	R/W	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
3E h	R/W	-	-	-	-	-	-	-	-	-	-	cycle master	-	-	-	-	-
Initial Value		'0'	'0'	'0'	'0'	'0'	'0'	'0'	'0'	'0"	'0'	'1'	'0'	'0'	'0'	'0'	'0'

■ **Description of Each Bit**

BIT	Bit Name	Action	Value	Function
15 - 6	reserved	Read	-	Always indicate '0'.
		Write	-	Always write in '0'.
5	cycle master	Read	0	Does not cycle master.
			1	Performs as cycle master if it is root.
		Write	-	Sets the value of this bit at '0' by writing in '1'.
4 - 0	reserved	Read	-	Always indicate '0'.
		Write	-	Always write in '0'.

8.17. Link register #02 (read/write)

Link Register#02 is the register that sets transfer mode of acknowledge packet transmitted by this node and disable setting of Link layer.

phy/ link-addr	R/W	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
40 h	R/W	-	-	-	-	-	-	-	-	-	-	-	-	ack mode	-	Link Enable	-
Initial Value		'0'	'0'	'0'	'0'	'0'	'0'	'0'	'0'	'0"	'0'	'0'	'0'	'1'	'0'	'1'	'0'

■ **Description of Each Bit**

BIT	Bit Name	Action	Value	Function
15 - 4	reserved	Read	-	Always indicate '0'.
		Write	-	Always write in '0'.
3	ack mode	Read/ Write	0	At receipt of normal packet. Automatically transmits Acknowledge packet of "ack_pending" to all request packet. Automatically transmits Acknowledge packet of "ack_complete" to all response packet. Automatically transmits packet. Code value of Acknowledge packet, automatically transmitted when error is detected, depends on the kind of error.
			1	At receipt of normal packet. Automatically transmits Acknowledge packet of "ack_pending" to Read request and Lock request. Automatically transmits Acknowledge packet of "ack_complete" to Write request packet and all response packet. Code value of Acknowledge packet automatically transmitted when error is detected depends on the kind of error.
2	reserved	Read	-	Always indicates '0'.
		Write	-	Always write in '0'.
1	Link Enable	Read/ Write	0	LINK layer is disabled.
			1	LINK layer is enabled.
0	reserved	Read	-	Always indicates '0'.
		Write	-	Always write in '0'.

8.18. Link register #03 (read/write)

Link Register#03 is the register that performs Link layer reset and initializes setting of the node.

phy/ link-addr	R/W	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
42 h	R/W	-	-	-	-		-	-	-	-	-	-	-	-	-	Link init	Link reset
Initial Value		'0'	'0'	'0'	'0'	'0'	'0'	'0'	'0'	'0"	'0'	'0'	'0'	'0'	'0'	'0'	'0'

■ **Description of Each Bit**

BIT	Bit Name	Action	Value	Function
15 - 2	reserved	Read	-	Always indicate '0'.
		Write	-	Always write in '0'.
1	Link init	Read/ Write	0	Releases initialize of LINK layer.
			1	Initializes LINK layer.
0	Link reset	Read/ Write	0	Releases reset of LINK layer.
			1	Resets LINK layer.

Chapter 9 Instruction

This chapter explains the instruction codes and details for respective instructions.

9.1. Instruction Code Table

Instruction name	code	Operand
Start sleep	01	
Remove sleep	02	
Asynchronous receive	03	
Remove busy mode	04	
Send PHY packet	21	
Asynchronous Send	31	Speed code
Data-FIFO init	63	FIFO select code
DMA Transmit (Asynchronous)	71	
DMA Transmit (PHY packet)	72	
DMA Receive	73	

9.2. Description of Each Instruction

■ Start sleep (01 h)

This instruction changes this device into forced sleep, stops the driver/receiver function of 1394 port, and then changed into the status with this device's cable cut.
Also, it stops the clock to be input from integrated PLL to IEEE1394 block.
Access to each register is available.
No interrupt this instruction is reported.
Confirm the sleep condition using sleep Bit (Bit4) of flag & status register (address 02h).

■ Remove sleep (02 h)

This instruction releases this device from forced sleep condition.
No interrupt to this instruction is reported.
Confirm the sleep condition release using sleep Bit (Bit4) of flag & status register (address 02h)

■ Asynchronous Receive (03 h)

This instruction reads the out data stored at ASYNC receive specific buffer.

Even though the receive data length does not satisfy with the quadlet unit, this instruction stores up to quadlet unit.
The receive data does not have CRC code and Logical inverse part.

■ Remove busy mode (04 h)

This instruction releases the busy mode set due to receiving normal Asynchronous packet or Self-ID packet addressed to this node.

■ Send PHY packet (21 h)

This instruction transmits the data stored at ASYNC receive specific buffer.

Do not issue this instruction in case that this instruction is not Bus manager node, or not Isochronous resource manager node without existence of Bus manager.

When packet transmit operation is completed normally, this instruction reports the interrupt of "Physical packet send" (INT25).

Store the transmit data at ASYNC transmit specific buffer beforehand.

Logical inverse part is added automatically by this device.

■ Asynchronous Send (31 h)

This instruction transmits the data stored at the ASYNC transmit specific buffer.

This instruction performs the following serial actions, from access to arbitration by detecting arb-reset-gap, generation and transfer of packet, to receipt of Acknowledge packet.
When the performances from packet transmit to Acknowledge receive are normally completed, this instruction reports interrupt of "Asynchronous packet send" (INT17).
In case of occurring an error, it reports interrupt of error, and completes performance.

Store the transmit data at ASYNC transmit specific buffer beforehand.
In case that the transmit data length does not satisfy with the quadlet unit, write in '0' until quadlet unit.
The CRC code is to be added automatically.

Received Acknowledge is indicated at receive Acknowledge indicate register (address 08h).

Note) When destination-ID is set at Broadcast, it is completed without waiting for receipt of Acknowledge.

BIT	Operand Name	Meaning
7 - 2	Reserved	Always specify '0'.
1 - 0	Speed code	Specify transmit Speed code. (MSB: 1, LSB: 0) 00 = S100 01 = S200 10 = S400 11 = (reserved)

■ Data-FIFO init (63h)

This instruction clears the contents of buffer specified by Operand.

BIT	Operand Name	Meaning
7 - 0	FIFO select code	Specify buffer to be cleared. (MSB: 7, LSB: 0) "11 h" = ASYNC receive specific buffer "12 h" = ASYNC transmit specific buffer Other than above = (reserved)

■ DMA Transmit (Asynchronous) (71h)

This instruction writes in the transmit Asynchronous packet to ASYNC transmit specific buffer using DMA transmit.

Assert DREQ signal after issuing this instruction.
Determine the transmit bite value by transmit data length within packet header, write in up to quadlet unit, then negate DREQ signal.

After completion of writing in, issue the Asynchronous send instruction (31h).

■ DMA Transmit (PHY packet) (72h)

This instruction writes in the transmit PHY packet to ASYNC transmit specific buffer using DMA transfer.

Assert the DREQ signal after issuing this instruction.
Negate the DREQ signal after writing in 2 bites.

After completion of writing in, issue the Send PHY packet instruction (21h).

■ DMA Receive (73h)

This instruction reads out the data stored in ASYNC receive specific FIFO using DMA transfer.

Issue Asynchronous receive instruction (03h) before issuing this instruction.

Assert DREQ signal after issuing this instruction.
Negate DREQ signal when ASYNC receive specific FIFO is empty.

Chapter 10 Interrupt

This chapter explains the inturrput-factors and method for interrupt-mask.

10.1. Interrupt-factor Indicator Register & interrupt-mask Setting Register

AD	R/	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
06h	R	INT 1	INT 2	INT 3	INT 4	INT 5	INT 6	INT 7	INT 8	INT 9	INT 10	INT 11	INT 12	INT 13	INT 14	INT 15	INT 16
	W	interrupt-mask															
08h	R	INT 17	INT 18	INT 19	INT 20	INT 21	INT 22	INT 23	INT 24	INT 25	INT 26	INT 27	INT 28	INT 29	INT 30	INT 31	INT 32
	W	Interrupt-mask															
Intial Value		'0'	'0'	'0'	'0'	'0'	'0'	'0'	'0'	'0'	'0'	'0'	'0'	'0'	'0'	'0'	'0'

> interrupt-factor Indicate Register

This register indicate the interrupt content reported by this device. Do not indicate the interrupt code specified MASK. Do not reflect its code to XINT terminal either.

> interrupt-mask setting register

This register masks the interrupt reported by this device. Do not report the interrupt if '1' is set for Bit corresponding to interrupt factor.

10.2. Interrupt

Interrupt	Interrupt Item
INT1	Loop detected
INT2	Self-ID packet error
INT3	Bus reset complete
INT4	Bus reset detected
INT5	Isochronous packet receive error (A-ch)
INT6	Isochronous packet receive error (B-ch)
INT7	Isochronous cycle too long
INT8	Bus occupancy violation
INT9	Asynchronous packet received
INT10	CPIF output header is no 47h (Transmit)
INT11	Data length short error
INT12	Data length long error
INT13	Packet format error
INT14	Header CRC error
INT15	Data CRC error
INT16	Asynchronous receive FIFO full
INT17	Asynchronous packet send
INT18	Input CGMS or TSCH changed
INT19	Acknowledge missing
INT20	Acknowledge send
INT21	Receive EMI or ODD/EVEN changed
INT22	First packet received
INT23	Cycle start packet received
INT24	Cycle start packet send
INT25	Physical packet send
INT26	Extended PHY packet received
INT27	Physical configuration packet received
INT28	Link-on packet received
INT29	Self-ID packet received
INT30	Receive late occurred
INT31	Instruction abort
INT32	Transmit late occurred

10.3. Description of Interrupt

Each interrupt items are described below.

Interrupt	Interrupt Item	Description
INT1	Loop detected	Topology is in Loop. > Need to issue "Bus reset".
INT2	Self-ID packet error	Occurred convention failure like Physical-ID did not count up each Self-ID packet received during Self Identify process. > Continues to receive Self-ID packet after reporting interrupt, but reports "Bus reset complete" (05h) interrupt.
		Detected logical inverse error while receiving Self-ID packet after sending Ping packet in normal transfer mode. >Delete receive packet.
INT3	Bus reset complete	This device has completed Bus reset process and able to perform packet transfer. > All the follows, Bus reset, Tree Identify, and Self Identify, are completed by this interrupt information.
INT4	Bus reset detected	Reset Bus reset in any of the following conditions. >Detected BUSRESET signal from other node. >Received "Bus reset"
INT5	Isochronous packet receive error (A-ch)	The following errors occurred at bridge-Ach during packet receiving. >Data length value differs from that specified in the format. >The value of 50/60 range at CIP header is '1' at DV receiving. >The value of STYPE range at CIP header is other than '00000' or '00001' at DV receiving. >The value of DBC range at CIP header is discontinuous. >Header error in CIP header. >The value of FMT range at CIP header is other than that all owed to be received at DV-EN, DSS-EN or TS-EN (1Ch-bit10 to 8) (DV= '000000', MPEG2-TS= '100000', DSS='100001').
INT6	Isochronous packet receive error (B-ch)	The following errors occurred at bridge-Bch during packet receiving. >Data length value differs from that specified in the format. >The value of 50/60 range at CIP header is '1' at DV receiving. >The value of STYPE range at CIP header is other than '00000' or '00001' at DV receiving. >The value of DBC range at CIP header is discontinuous. >Header error in CIP header. >The value of FMT range at CIP header is other than that allowed to be received at DV-EN, DSS-EN or TS-EN (1Ch-bit10 to 8) (DV= '000000', MPEG2-TS= '100000', DSS='100001').

Interrupt	Interrupt Item	Description
INT7	Isochronous cycle too long	Isochronous cycle exceeded specified time. >Informs only if this node is Cycle master.
INT8	Bus occupancy violation	Node occupied longer time than MAX_DATA_TIME. >Need to issue "Bus reset".
INT9	Asynchronous packet received	Received Asynchronous packet addressed to self-node normally, and stored data at ASYNC receive specific buffer.
INT10	CPIF output header is no 47h (Transmit)	Header byte of source packet output from CPIF at transmitting MPSG2-TS is not '47h'. >Valid only when transmitting MPSG2-TS.
INT11	Data length short error	Receive packet data length is shorter than data-length of packet header.
INT12	Data length long error	Receive packet data length is longer than data-length of packet header. >Store only data indicated by data-length value to buffer.
INT13	Packet format error	Detected format error in packet received. Occurred convention failure of packet format like Reserved range is not '0'. >Delete packet received.
INT14	Header CRC error	Detected CRC error in the header of packet received. >Delete packet received.
INT15	Data CRC error	Detected CRC error in the data range of packet received. >Do not delete packet received.
INT16	Asynchronous receive FIFO full	ASYNC receive specific buffer is full. >Delete following packet received.
INT17	Asynchronous packet send	Completed sending Asynchronous packet by issueing instruction.
INT18	Input CGMS or TSCH changed	CGMS or TSCH information input from TSP IC I/F was not consistent with the souce packet input just before.
INT19	Acknowledge missing	Not returned Acknowledge packet in correspondance with Asynchronous packet of non-broadcast sent from self-node within specified limit.
INT20	Acknowledge send	Completed sending Acknowledge packet.
INT21	Receive EMI or ODD/EVEN changed	Changede EMI data or ODD/EVEN value of received Isochronous packet.
INT22	First packet received	Received the first packet after setting receive ISO channel.

Interrupt	Interrupt Item	Description
INT23	Cycle start packet received	Received cycle start packet normally when self node is not root > Isochronous cycle starts. Set ISO cycle Bit (Bit12) of flag & status register (address 02h) at '1' simaltaneously with this interrupt report.
INT24	Cycle start packet send	Completed to send Cycle start packet when self node is root.
INT25	Physical packet send	Completed to send Physical packet.
INT26	Extended PHY packet received	Received Extended PHY packet normally.
INT27	Physical configuration packet received	Received Physical configuration packet normally. > Reflect to Physical register#01(address Phy/Link-reg 02h) and switch to specified performance automatically.
INT28	Link on packet received	Received Link-on packet addressed to self-node normally. > Assert LINKON terminal output simultaneously.
INT29	Self-ID packet received	Received Self-ID packet normally. Store data at ASYNC receive specific buffer.
INT30	Receive late occurred	Receive-late was occured. Delete packet received.
INT31	Instruction abort (State)	Though Instruction was issued, it was not accepted because the content was not appropriate for this device. e.g.) >Issued "Remove sleep" (02h) instruction in spite of not in sleep condition. >Issued "Instruction suspend"(62h) instruction without instruction to be stopped. >Used undefine operand against issued instruction. >Issued instruction was undefined. etc.
INT32	Transmit late occurred	Transmit-late was occured. >Delete packet transmitted.

Chapter 11 Operation

This chapter explains the operation of this device and displays the examples of control flow.

11.1. Initialization

The example of control flow from the system power on to the packet transmitting / receiving possible state is shown below. In this examle, the device is not operated with cable power supply before turning on the power of system.

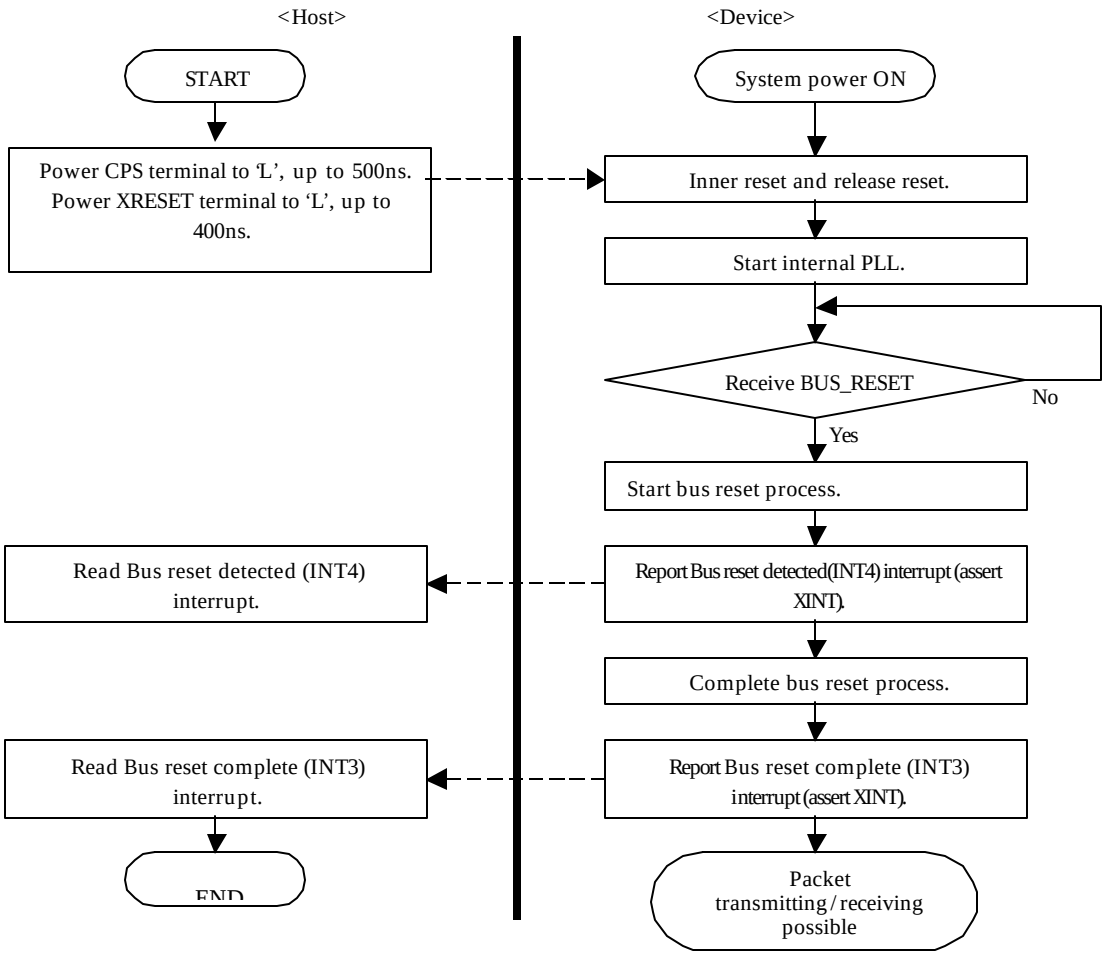


Figure 11.1 Example of flow for Initialization

11.2. Self-ID Packet Receiving

The example of control flow for receiving Self-ID packet is shown below.

11.2.1 Self-ID Packet Receive during Bus Reset Process

11.2.2 Self-ID Packet Receive after Ping Packet Transmitting

11.2.1 Self-ID Packet Receive at Bus Reset Process

This section explains the receiving process of Self-ID packet.

The MB86617A device is capable of receiving self-ID packets that each mode transmit in the self-identity stage of bus reset process. When '1' is written to the s-ID store bit of mode-control register (refer to 7.1), the self-ID packet in the bus reset process can be received and the data removing the logical inverse section is stored in the Asynchronous receive-FIFO and Asynchronous transmit-FIFO (512 bytes maxixum). When the number of total data exceeds 512 bytes, the overflown data are discarded.

Bus reset force-clears FIFO for Asynchronous receiving and FIFO for Asynchronous transmitting to store Self-ID packet.

■ **Flow chart before bus reset completion**

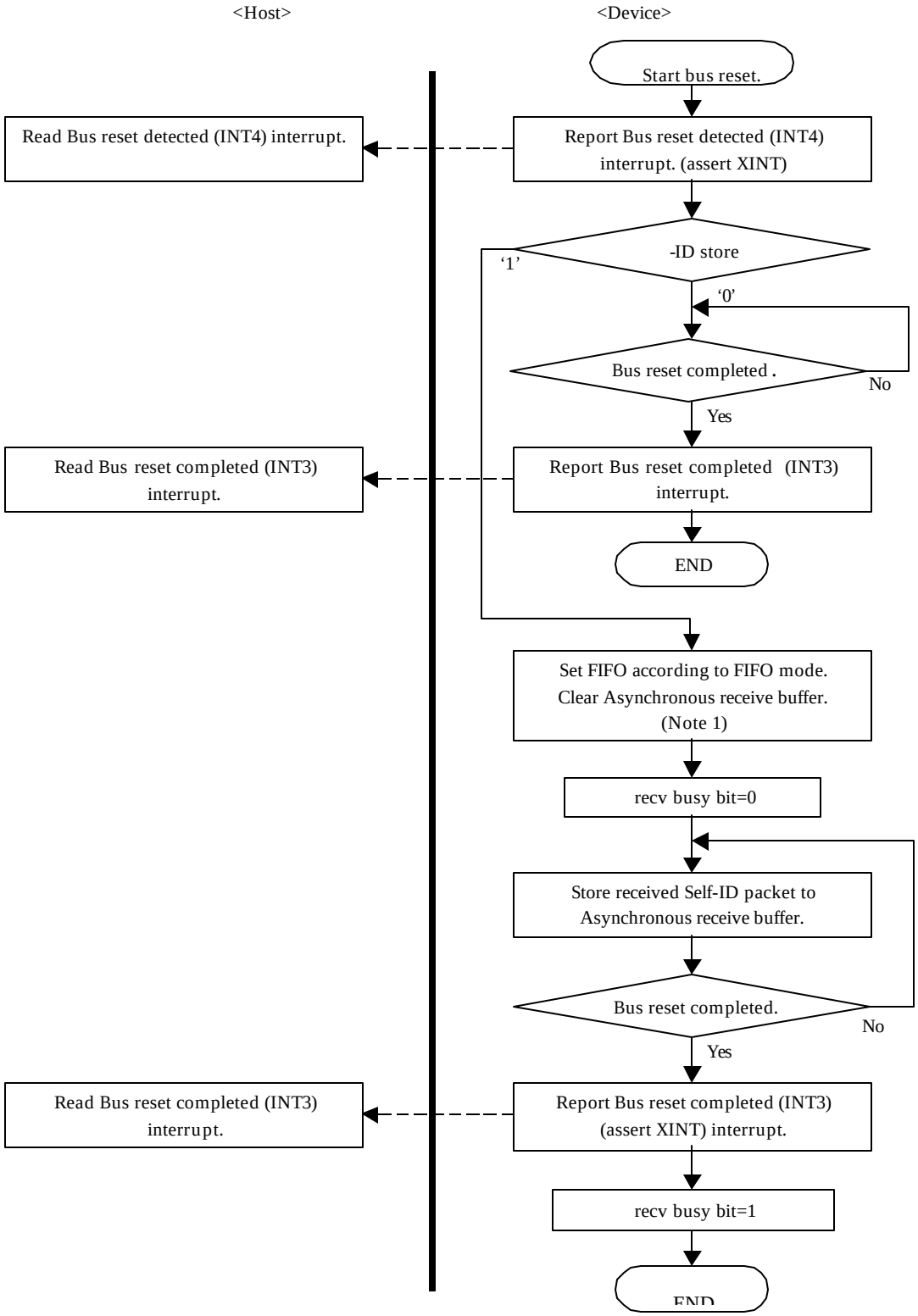


Figure 11.2.1.1 Flow example for Self-ID packet receiving before bus reset completion

■ **Flow chart after bus reset completion**

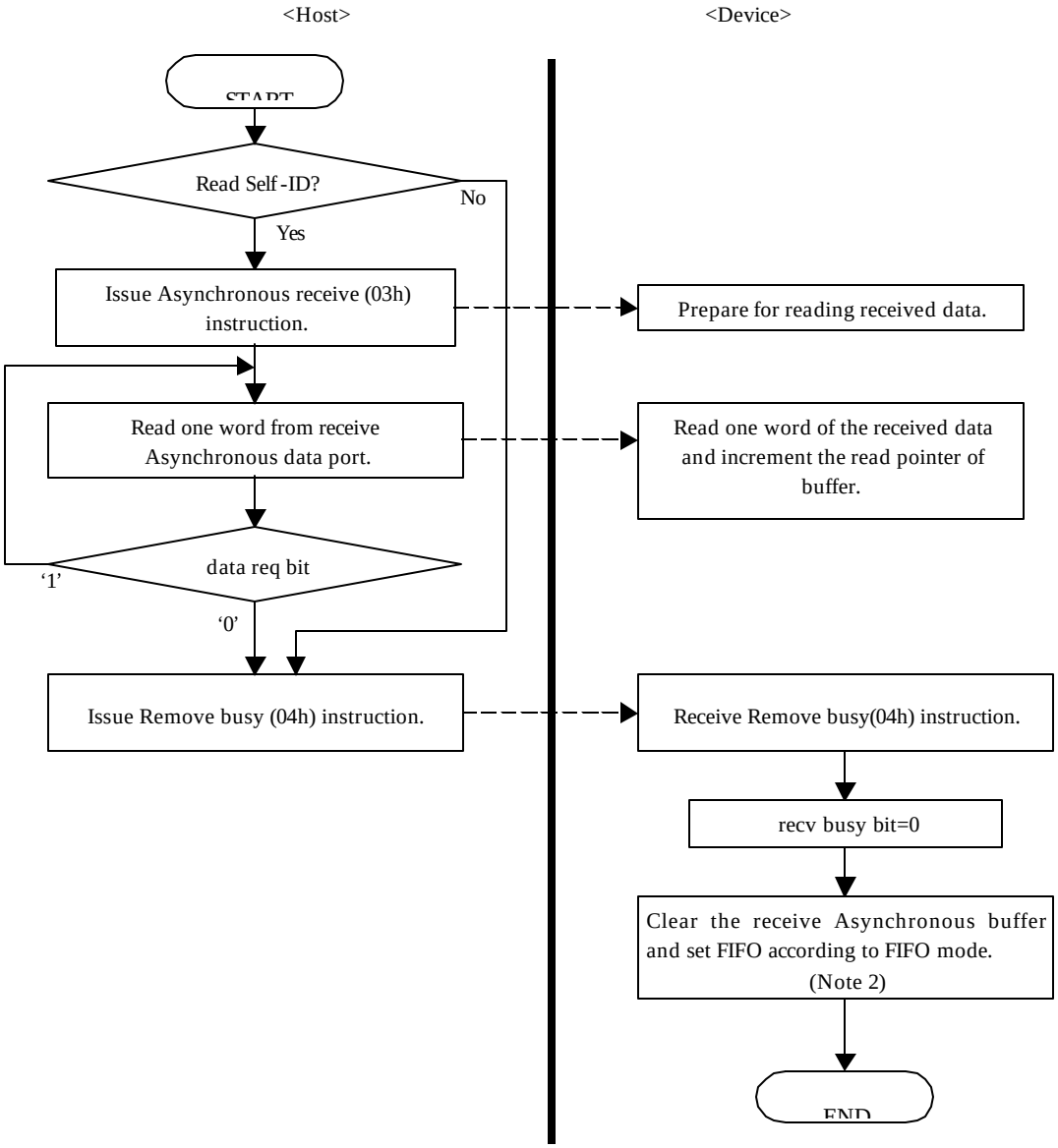


Figure 11.2.1.2 Flow example for Self-ID packet receiving after bus reset completed

Note1: When Asyn-FIFO sel (mode-control register[3]) is 1 and send/rec (mode-control register [2]) is 1, Asynchronous receive FIFO (256 byte) and Bridge FIFO (2048 byte) are used with combined as Asynchronous receive buffer.
In other case, Asynchronous receive FIFO (256 byte) and Asynchronous transmit FIFO (256 byte) are used with combined.

Note2: When Asyn-FIFO sel is 1 and transmit/rec is 1, Asynchronous transmitting FIFO (256 byte) and Bridge FIFO (2048 byt) are cleared,
When Asyn-FIFO SEL is 1 and transmit/rec is 0, Asynchronous receiving FIFO (256 byte) and Asynchronous transmitting FIFO (256 byte) are cleared. Asynchronous transmit FIFO and Bridge FIFO are combined to be set in Asynchronous transmit buffer. Set Asynchronous receive FIFO to Asynchronous receive buffer.
When Asyn-FIFO sel is 0, Asynchronous receive FIFO (256 byte) and Asynchronous transmit FIFO (256 byte) are cleared and re-set Asynchronous receive FIFO to Asynchronous receive buffer, Asynchronous transmit FIFO to Asynchronous transmit buffer.

11.2.2 Self-ID Packet Receive after Transmitting Ping Packet Ping

Regardless of s-ID store bit setting in the mode-control register (refer to 7.1), the device receives self-ID packet after a ping packet transmitted and stores the data removing logical inverse section in the Asynchronous receive-FIFO.

■ **Flow chart from transmitting of Pig packet to receiving Self-ID packet Ping**

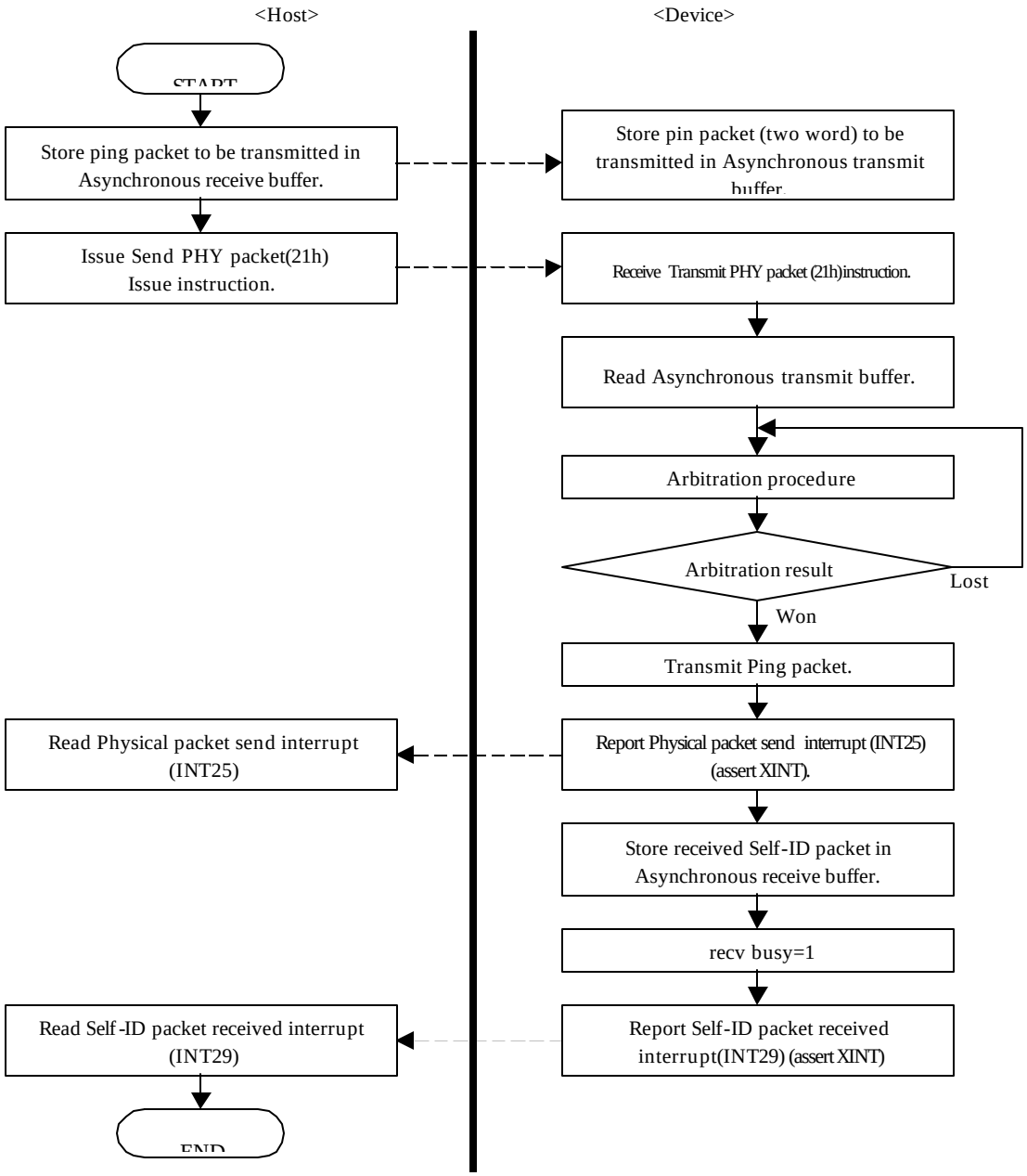


Figure 11.2.2.1 Flow example of operation from Pin packet transmitting to Self-ID packet receiving

■ **Flow chart after receiving Self-ID packet**

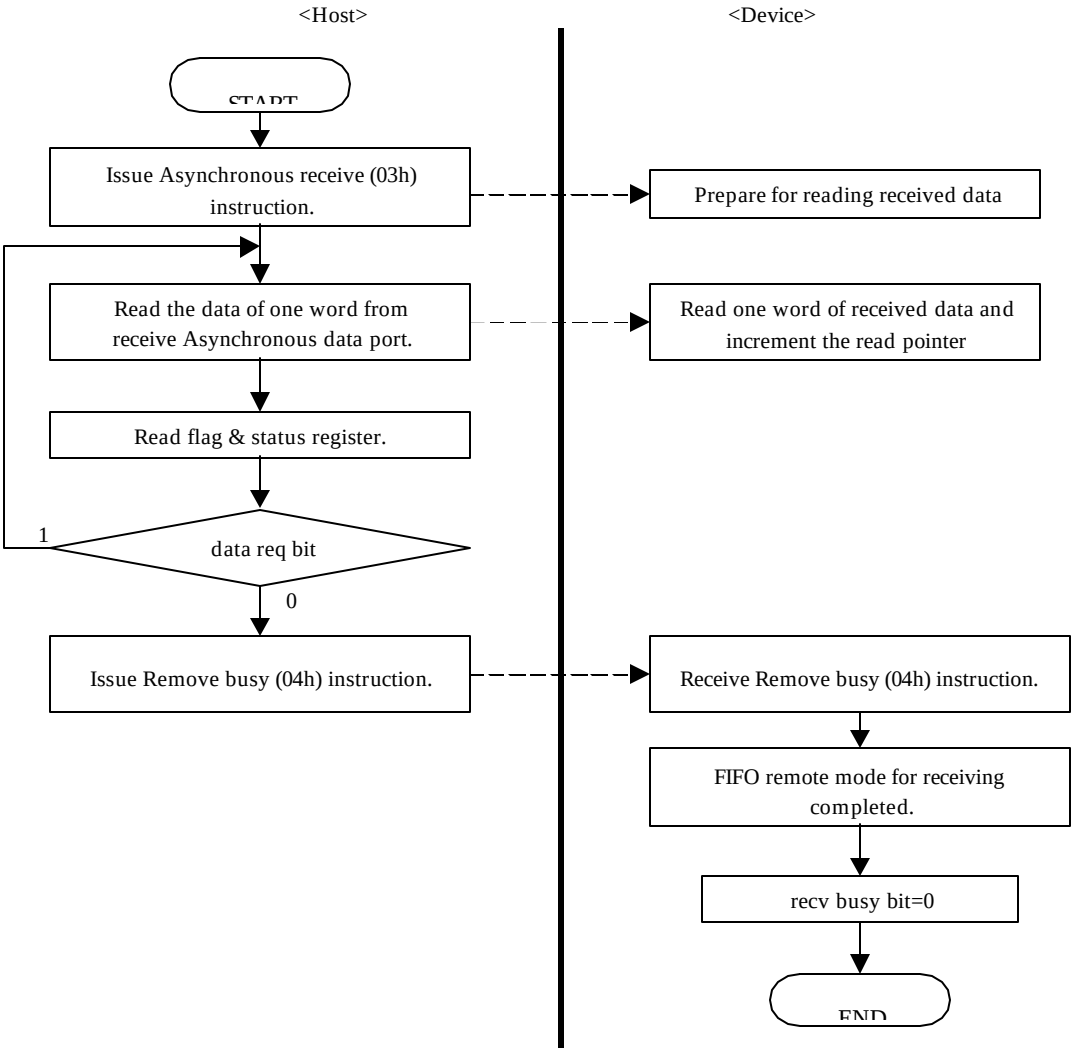


Figure 11.2.2.2 Flow example after receiving Self-ID packet.

11.3. Asynchronous Packet Transmitting

The example of control flow for transmitting of Asynchronous packet is shown below.

■ **Flow chart before storing transmitting data into Asynchronous transmit FIFO**

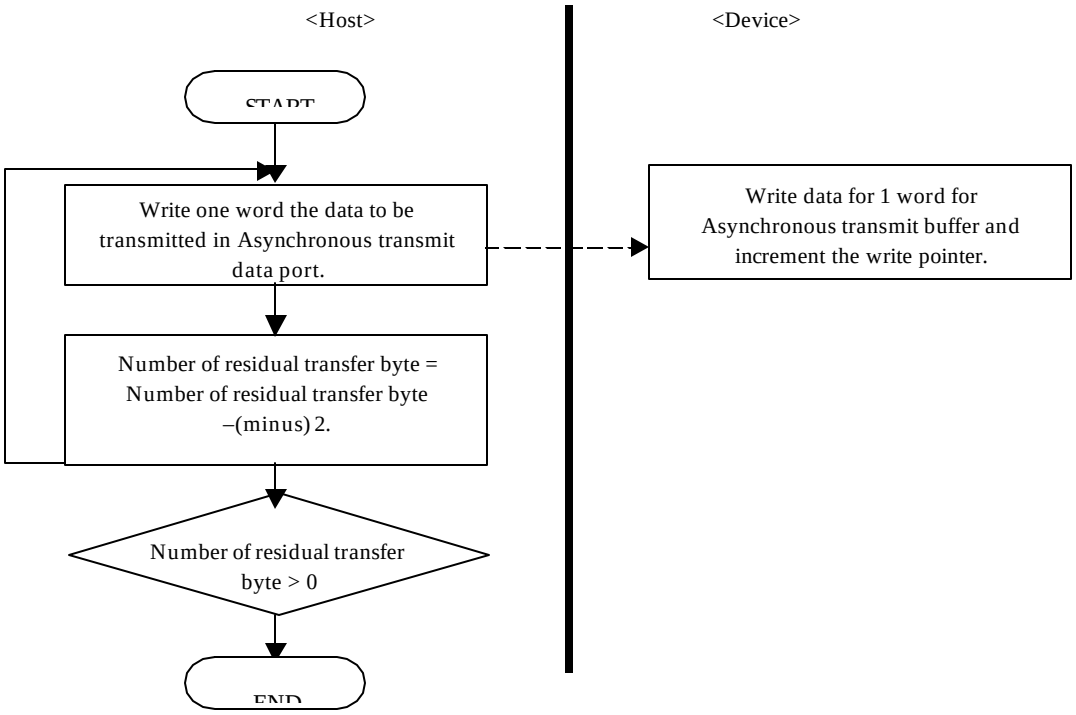


Figure 11.3.1 Flow chart before storing transmitting data in Asynchronous transmit FIFO

Note1: Store the data to be transmit previously in Asynchronous transmit FIFO.
Note2: If the transmitting length is below the digit of quadret, write "0" there up to quadret unit.
Note3: The device can automatically attaches CRC code.

■ **Flow chart after storing transmitting data into Asynchronous transmit FIFO**

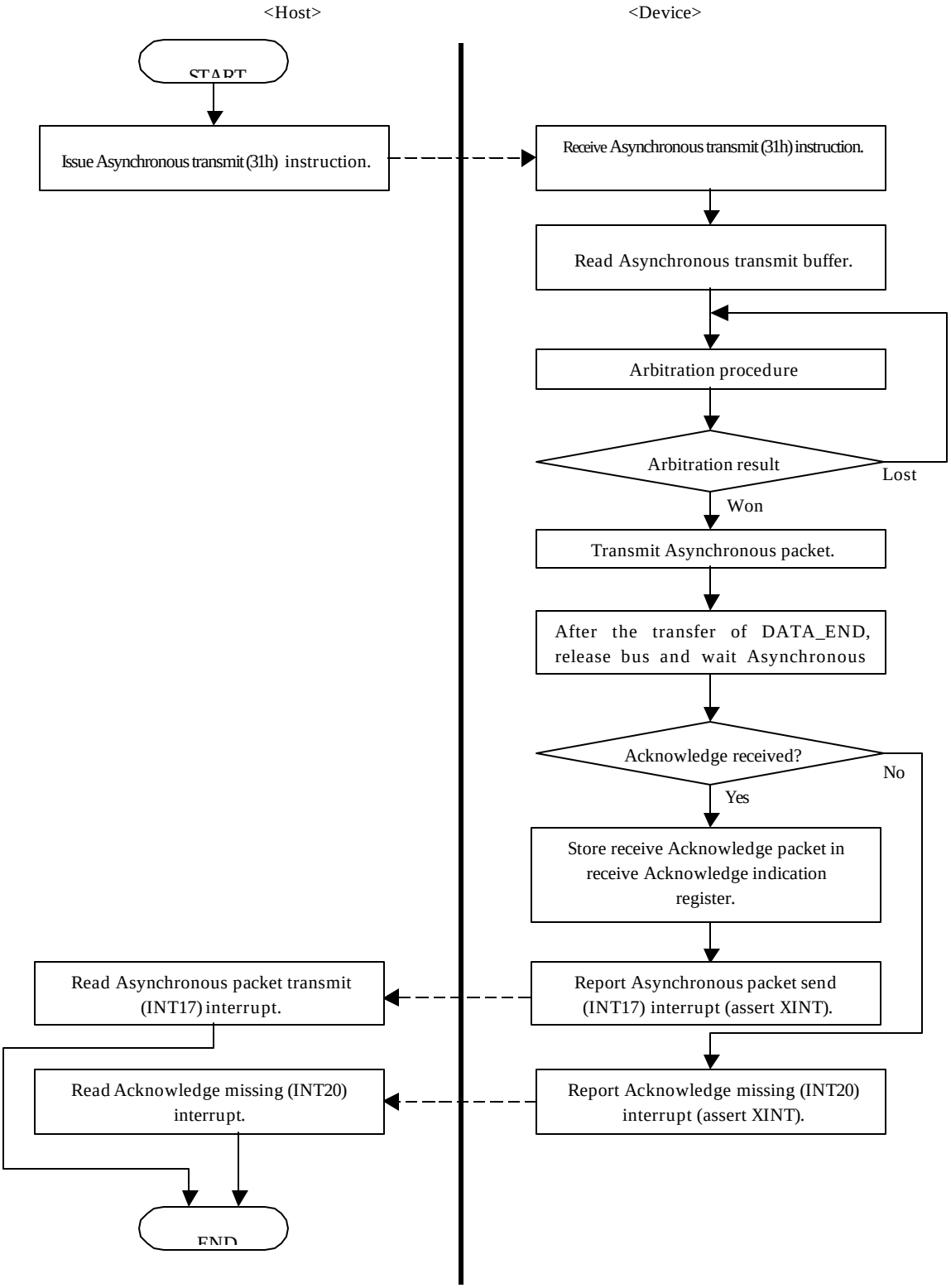


Figure 11.3.2 Flow chart after storing transmitting data in Asynchronous transmit FIFO

11.4. Asynchronous Packet Receiving

The example of control flow for receiving Asynchronous packet is shown below.

■ **Flow chart for received data before storing in Asynchronous receive FIFO**

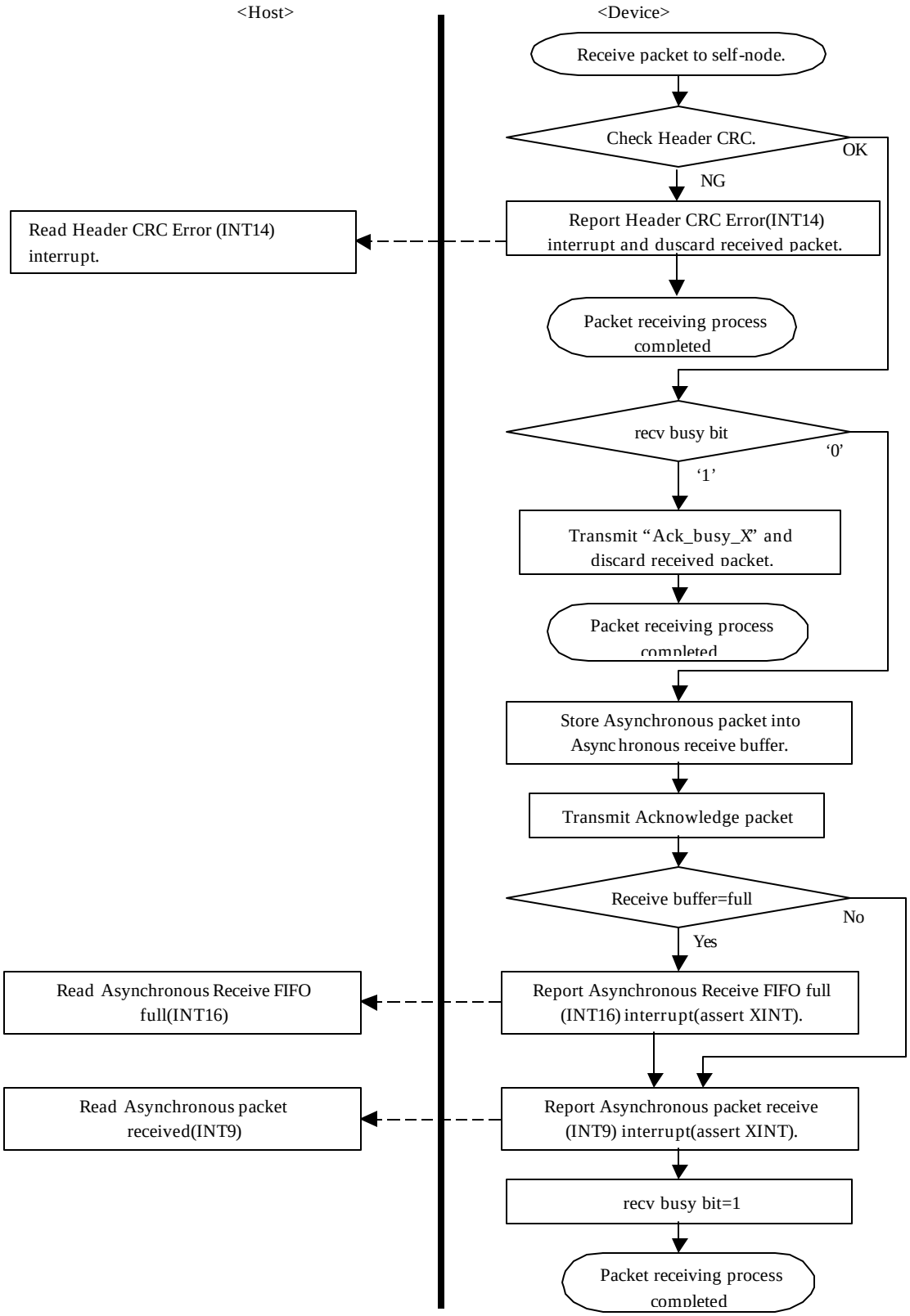


Figure 11.4.1 Flow example for received data before storing in Asynchronous receive FIFO

■ **Flow chart for received data after storing in Asynchronous receive FIFO**

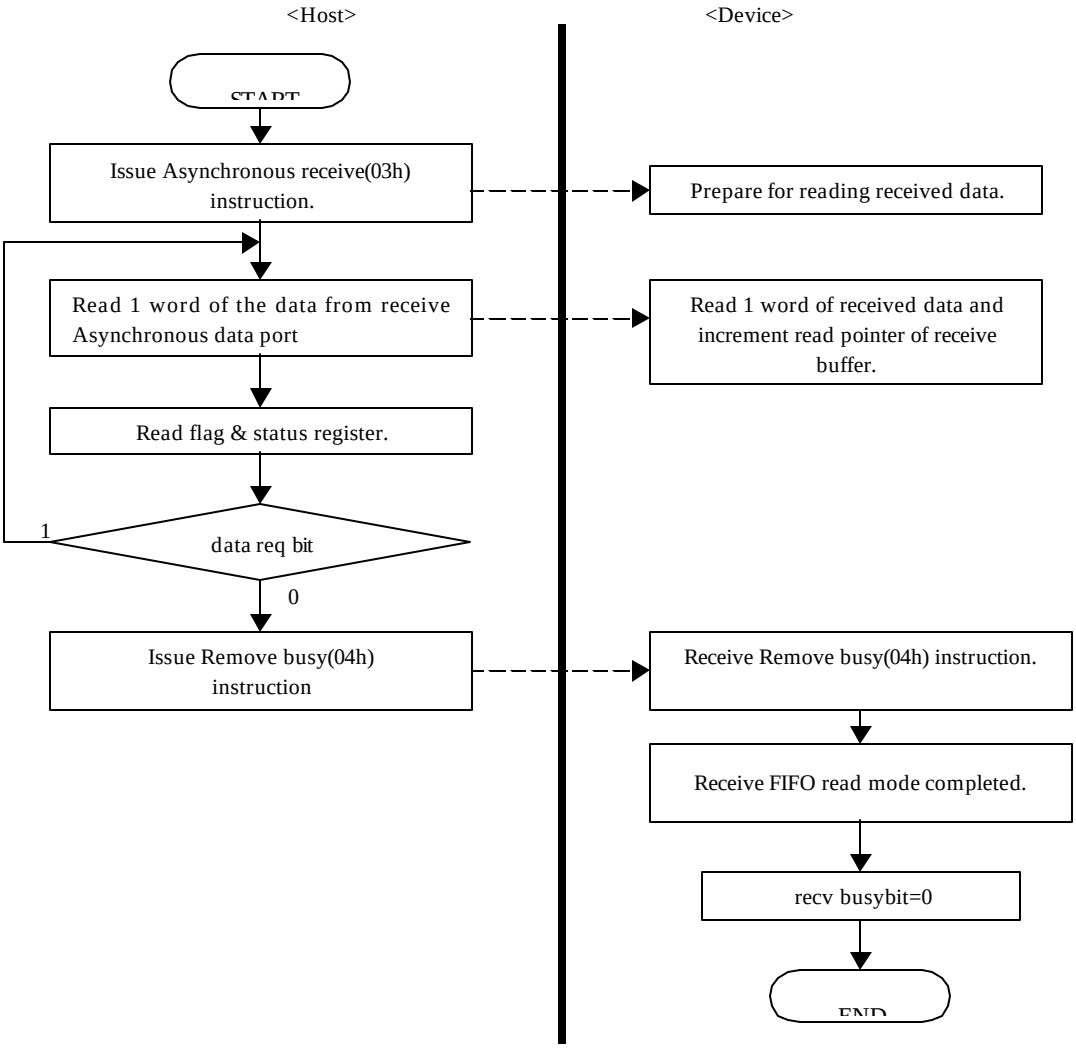


Figure 11.4.2 Flow chart for received data after storing in Asynchronous receive FIFO

Note1: If the length of received data is below quadret digid, it is stored by quadret unit????.
Note2: CRC code is not included in the data.

11.5. Isochronous Packet Transmitting

The example of control flow for transmitting Isochronous packet is shown below.

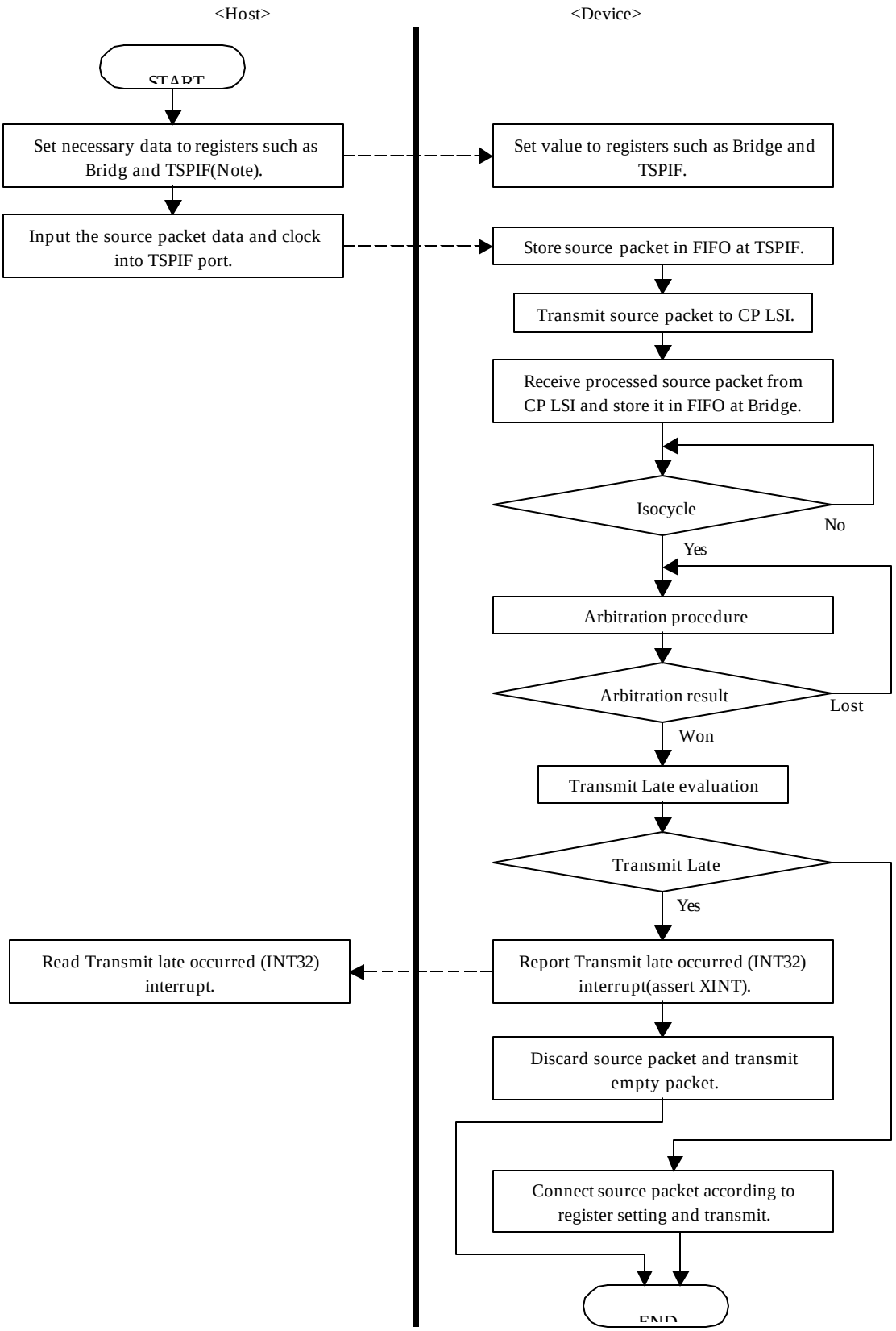


Figure 11.5 Flow example for transmitting Isochronous packet

(Note)Register and bit necessary for transmitting are as follows.

Address	Data	
	MPEG-TS	DSS
00h	TSPSB=0, CPSB=0	
14h,16h 18h,1Ah	Set value of transmit Offset(Ach). Set value of transmit Offset (Bch)	
34h	DBSA=06h, FNA=3h	DBSA=09h, FNA=2h
36h	TXFMTA=20h, TXCHA(Iso channel No.)	TXFMTA=21h, TXCHA(Iso channel No.)
38h	DBSB=06h, FNB=3h	DBSB=09h, FNB=2h
3Ah	TXFMTB=20h, TXCHB(Iso channel No.)	TXFMTB=21h, TXCHB(Iso channel No.)
40h	Set criteria for Late packet (Ach).	
42h	Set criteria for Late packet (Bch).	
10h	Set at Ach transmitting. TXSTA=1, TFA	Set at Ach transmitting. TXSTA=1, TFA, TXFMTA=1, IDSIZEA=1(DSS130)
12h	Set at Bch transmitting. TXSTB=1, TFB	Set at Bch transmitting. TXSTB=1, TFB, TXFMTB=1, IDSIZEB=1(DSS130)

11.6. Isochronous Packet Receiving

The example of control flow for receiving Isochronous packet is shown below.

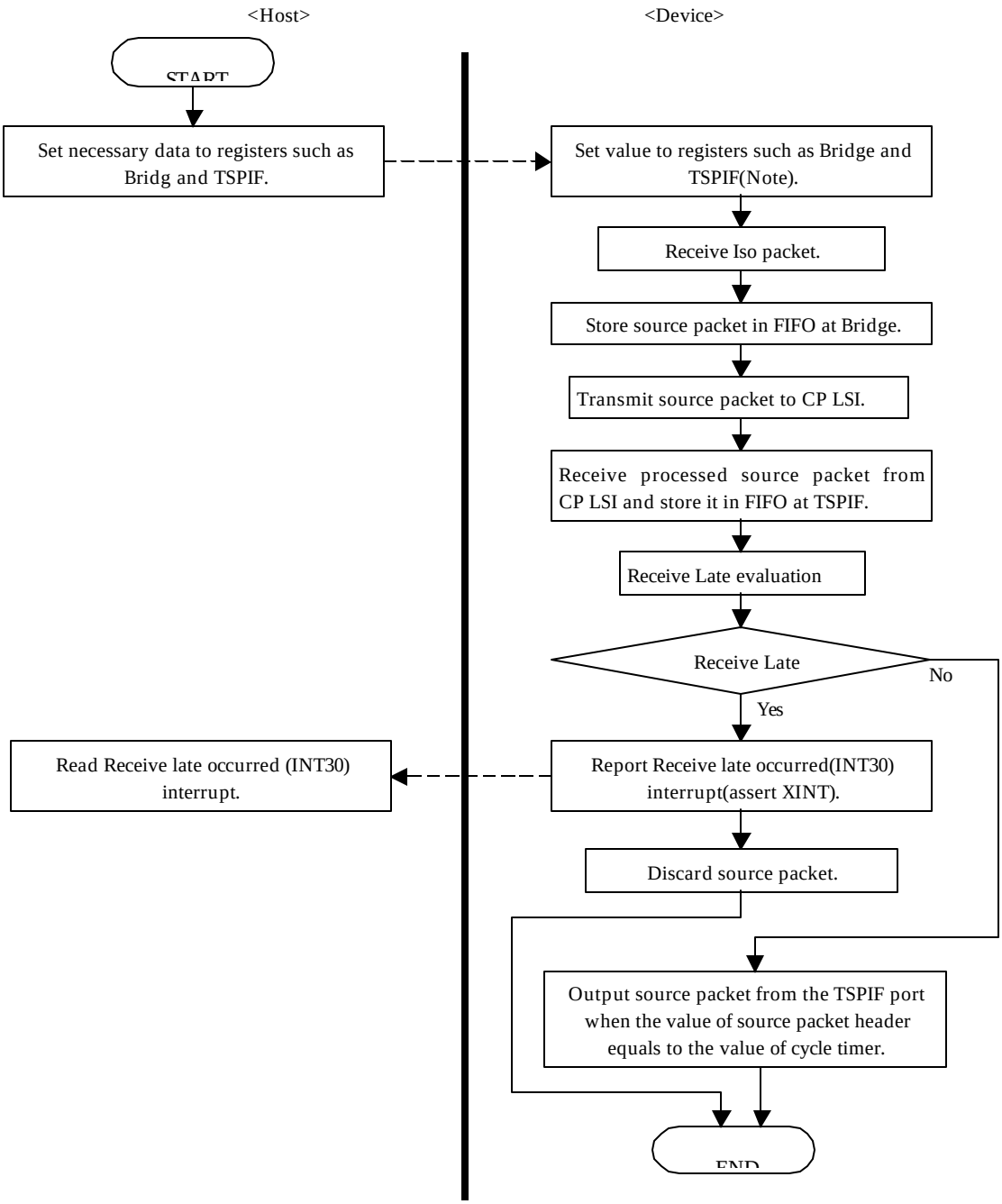


Figure 11.6 Flow example for transmitting Isochronous packet

(Note)Register and bit necessary for receiving are as follows.

Address	Data		
	MPEG-TS	DSS	DV
00h	TSPSB=0, CPSB=0		
1Ch	TSEN=1, Set TV1A,TV1B,TV2A,TV2B according to Ch received and port.	DSSEN=1, Set TV1A,TV1B,TV2A,TV2B according to Ch received and port.	DVEN=1, Set TV1A,TV1B,TV2A,TV2B according to Ch received and port.
40h	Set criteria for Late packet (Ach).		-
42h	Set criteria for Late packet (Bch).		-
3Ch	Ach received : RXSTA=1h, RXCHA(Iso channel No.) Bch received : RXSTB=1h, RXCHB(Iso channel No.)		

Chapter 12 System Configuration

This chapter explains the system configuration of this chip.

12.1. Recommended Connection for 1934 Port (for one port)

The example of recommended connection of 1934 port terminal for one port is shown below.

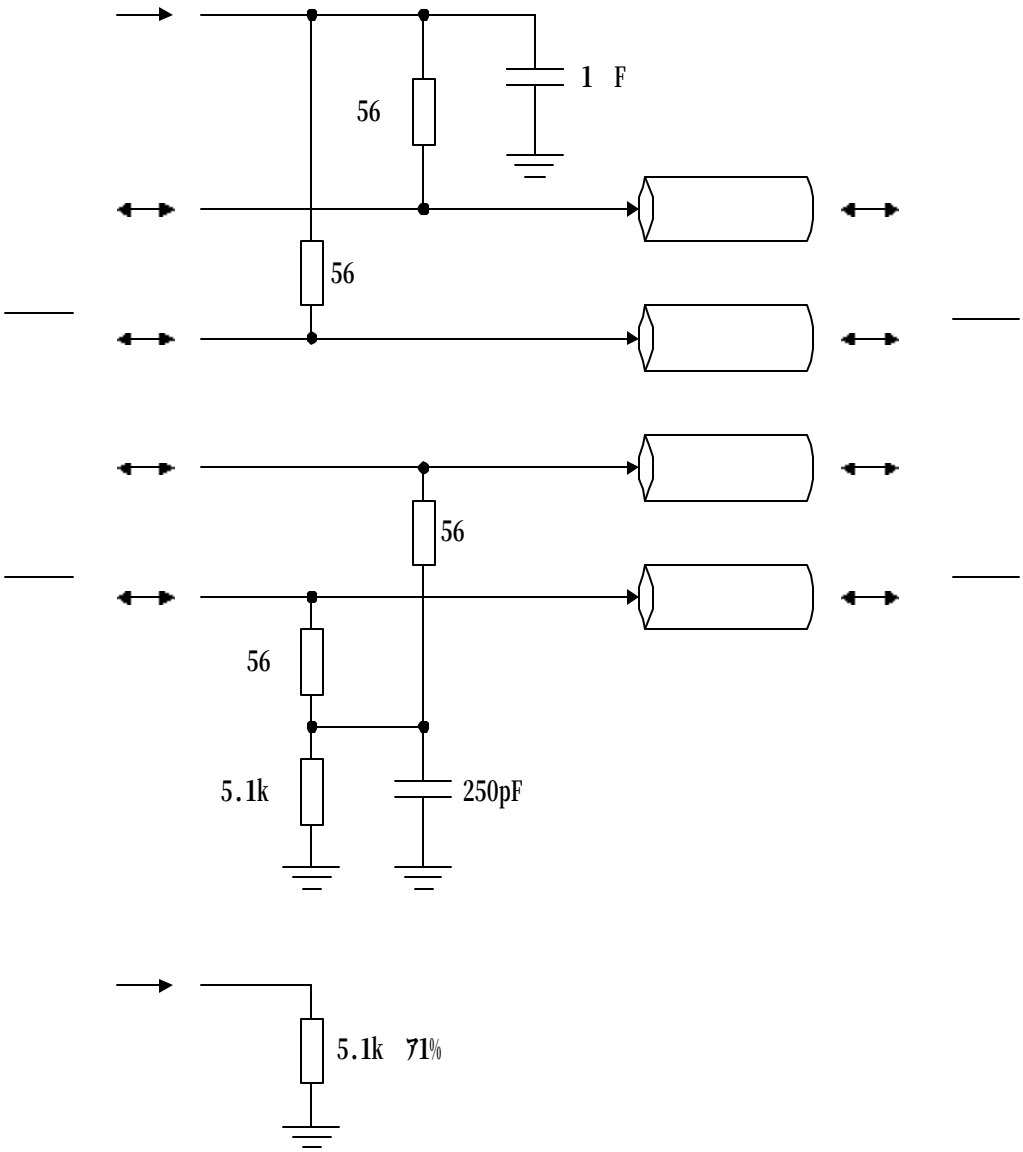


Figure 12.1 Recommended connection for 1934 port (for one port)

For unused 1394 port, TPBIAS should be open and TPA, XTPA, TPB and XTPB should be be connected to GND.

12.2 Recommended Connection for Cable Power Supply

The example of recommended connection of cable power supply for 1394 cable is shown below.

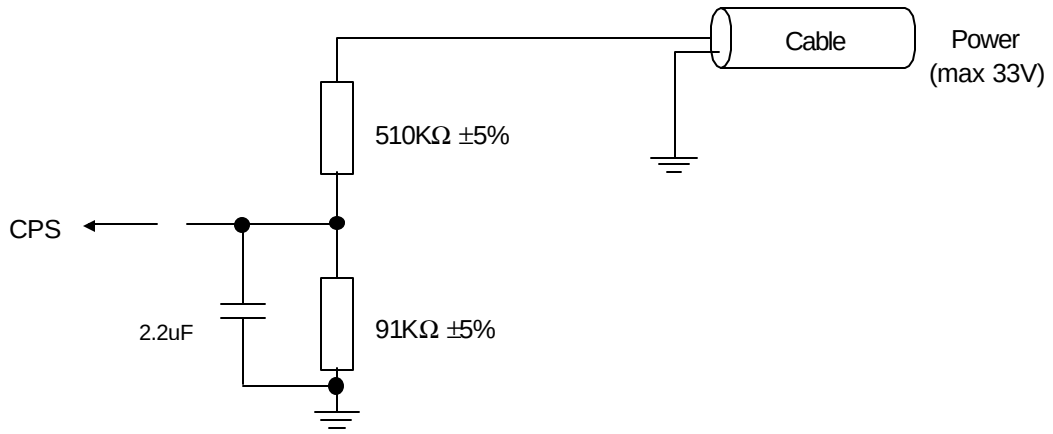


Figure 12.2 Recommended connection for cable power supply

12.3. Recommended Connection for Build-in PLL Loop Filter

The example of recommended connection for build-in PLL loop filter is shown below.

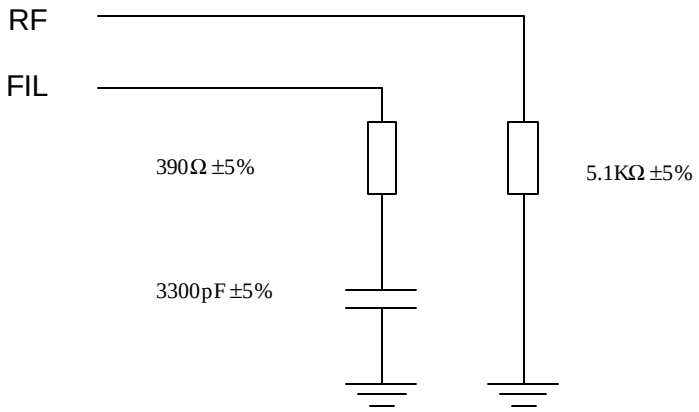


Figure 12.3 Recommended connection for build-in PLL loop filter

12.4. Configuration of Feedback Circuit at Crystal Oscillator

The example of configuration of feedback circuit at crystal oscillator is shown below.
No outside resistance is needed because the feedback resistance is built-in.???

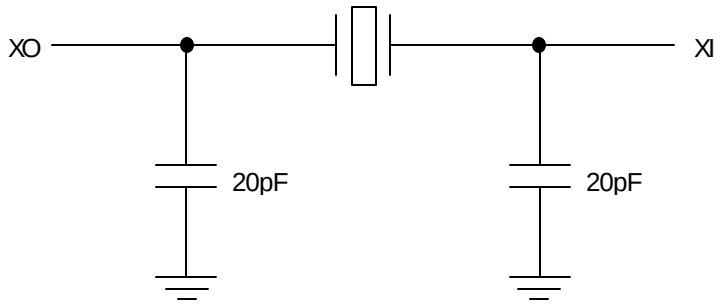


Figure 12.4 Configuration of feedback circuit at crystal oscillator