

ASSP

IF Band PLL Frequency Synthesizer

MB15C101

■ DESCRIPTION

The Fujitsu Microelectronics MB15C101 is an exclusive Intermediate Frequency (IF) band Phase Locked Loop (PLL) frequency synthesizer with pulse swallow operation. The reference divider and comparison divider have fixed divide ratios, so that it is not required to set the divide ratios by a microcontroller externally.

It operates with a supply voltage of 3.0 V typ. and dissipates 1.0 mA typ.(270MHz) of current realized through the use of Fujitsu Microelectronics's CMOS technology.

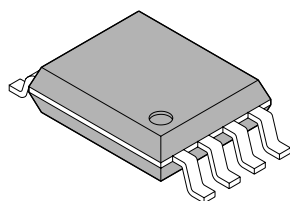
The MB15C101 is ideally suitable for PHS systems.

■ FEATURES

- Low power supply current: $I_{CC} = 1.0 \text{ mA}$ typ. ($V_{CC} = 3 \text{ V}$, 270MHz)
- Pulse swallow function; Prescaler: 16/17
- Setting frequency (Selectable by Div input.)
 - $f_{osc} = 19.2 \text{ MHz}$, $f_{IF} = 233.15 \text{ MHz}$ (Div = "H")
 - $f_{osc} = 19.2 \text{ MHz}$, $f_{IF} = 259.20 \text{ MHz}$ (Div = "L")
- Lock detector
- Low power supply voltage: $V_{CC} = 2.4 \text{ V}$ min.
- Wide operating temperature: $T_a = -40$ to $+85^\circ\text{C}$

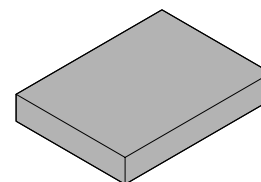
■ PACKAGE

8-pin plastic SSOP



(FPT-8P-M03)

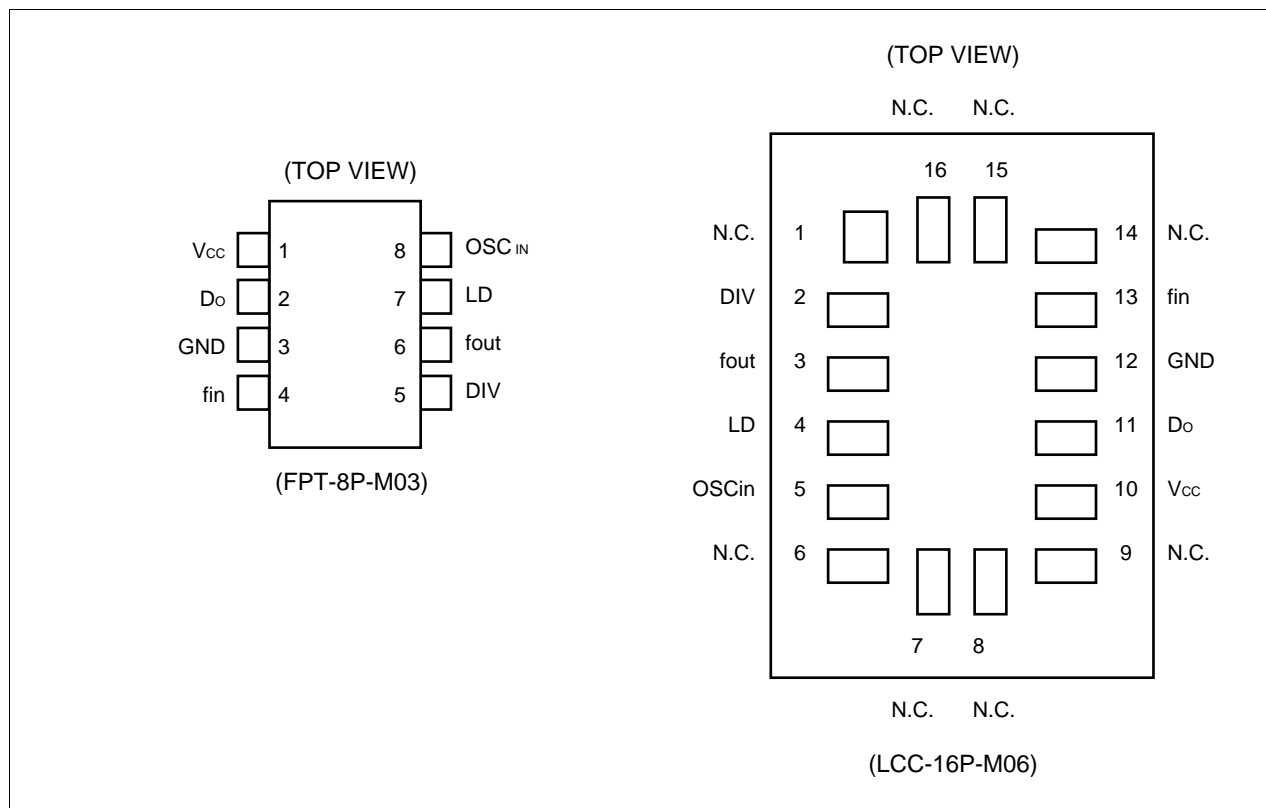
16-pad plastic BCC



(LCC-16P-M06)

MB15C101

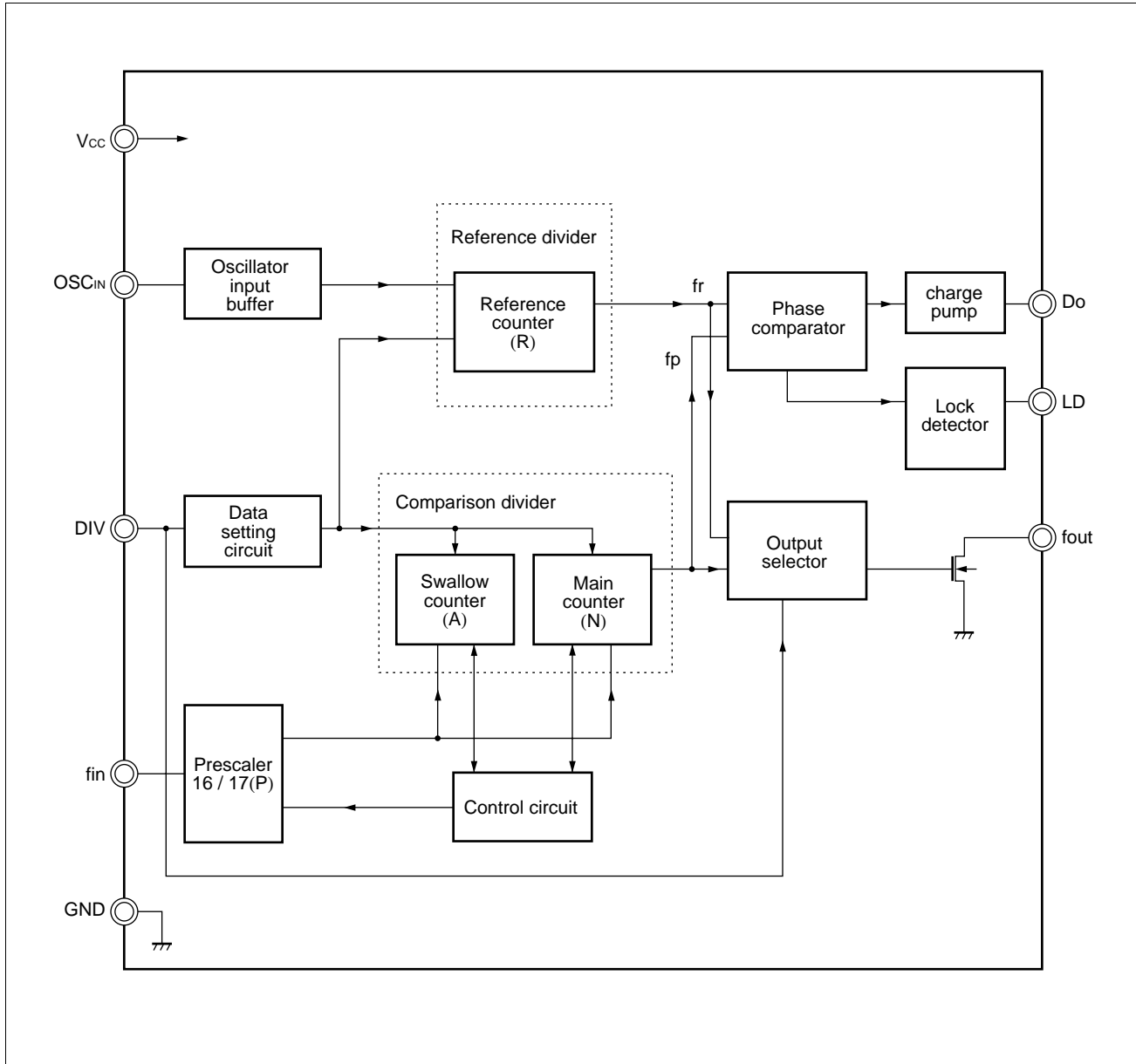
■ PIN ASSIGNMENT



■ PIN DESCRIPTIONS

| Pin No. | | Pin name | I/O | Descriptions |
|---------|--------------------|-------------------|-----|--|
| SSOP-8 | BCC-16 | | | |
| – | 1,6,7,8,9,14,15,16 | N.C | – | No connection |
| 1 | 10 | V _{CC} | – | Power supply voltage input (2.4 V to 3.6 V). |
| 2 | 11 | D _O | O | Charge pump output |
| 3 | 12 | GND | – | Ground |
| 4 | 13 | fin | I | Prescaler input. Connection should be with AC coupling. |
| 5 | 2 | Div | I | Divide ratio switching input. Two kinds of divide ratios are selectable by Div input "H" or "L". |
| 6 | 3 | fout | O | Test purpose output. This pin is an open drain output so that should be left open usually. |
| 7 | 4 | LD | O | Lock detector output. LD = H ; Lock LD = L ; Unlock |
| 8 | 5 | OSC _{IN} | I | Reference counter input. Connection should be with AC coupling. |

■ BLOCK DIAGRAM



MB15C101

■ ABSOLUTE MAXIMUM RATINGS

| Parameter | Symbol | Rating | | Unit |
|----------------------|-----------|--------|----------------|------|
| | | Min. | Max. | |
| Power supply voltage | V_{CC} | -0.5 | +4.0 | V |
| Input voltage | V_I | -0.5 | $V_{CC} + 0.5$ | V |
| Output voltage | V_{OUT} | -0.5 | $V_{CC} + 0.5$ | V |
| Output current | I_{OUT} | 0 | +5 | mA |
| Storage temperature | T_{STG} | -55 | +125 | °C |

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

■ RECOMMENDED OPERATING CONDITIONS

| Parameter | Symbol | Value | | | Unit | Note |
|-----------------------|----------|-------|------|----------|------|------|
| | | Min. | Typ. | Max. | | |
| Power supply voltage | V_{CC} | 2.4 | 3.0 | 3.6 | V | |
| Input voltage | V_{IN} | GND | - | V_{CC} | V | |
| Operating temperature | T_a | -40 | - | +85 | °C | |

Handling Precautions

- This device should be transported and stored in anti-static containers.
- This is a static-sensitive device; take proper anti-ESD precautions. Ensure that personnel and equipment are properly grounded. Cover workbenches with grounded conductive mats.
- Always turn the power supply off before inserting or removing the device from its socket.
- Protect leads with a conductive sheet when handling or transporting PC boards with devices.

■ ELECTRICAL CHARACTERISTICS

Recommended operating conditions unless otherwise noted.

| Parameter | Symbol | Condition | Value | | | Unit | |
|--------------------------------|-------------------|---|--|-----------------------|-----------------------|-----------------|----|
| | | | Min. | Typ. | Max. | | |
| Power supply current | I _{CC} | PLL is locked.(270MHz) V _{CC} = 3.0 V, Ta = +25°C | 0.1 | 1.0 | 2.0 | mA | |
| Operating frequency | f _{in} | AC coupling by 1000 pF capacitor | 50 | – | 270 | MHz | |
| | OSC _{IN} | AC coupling by 1000 pF capacitor | 3 | – | 26 | MHz | |
| Input sensitivity | f _{in} | AC coupling by 1000 pF capacitor | –10 | – | +2 | dBm | |
| | OSC _{IN} | AC coupling by 1000 pF capacitor | 0.5 | – | – | V _{pp} | |
| Input voltage | Div | V _{IH} | – | V _{CC} × 0.7 | – | V | |
| | | V _{IL} | – | – | V _{CC} × 0.3 | V | |
| Input current | Div | I _{IH} | – | – | 1.0 | μA | |
| | | I _{IL} | – | –1.0 | – | μA | |
| Input current | OSC _{IN} | I _{OSC} | – | –100 | 100 | μA | |
| Output voltage | Do | V _{OH} | V _{CC} = 3.0 V, I _{OH} = –0.3mA | 2.6 | – | – | V |
| | | V _{OL} | V _{CC} = 3.0 V, I _{OL} = 0.3mA | – | – | 0.4 | V |
| Output current | Do | I _{OH} | V _{CC} = 3.0 V, V _{OH} = 2V, Ta = +25°C | – | –6.0 | – | mA |
| | | I _{OL} | V _{CC} = 3.0 V, V _{OL} = 1V, Ta = +25°C | – | 6.0 | – | mA |
| High impedance cut off current | Do | I _{OFF} | 0 ≤ V _{DO} ≤ V _{CC} | – | – | 3 | nA |

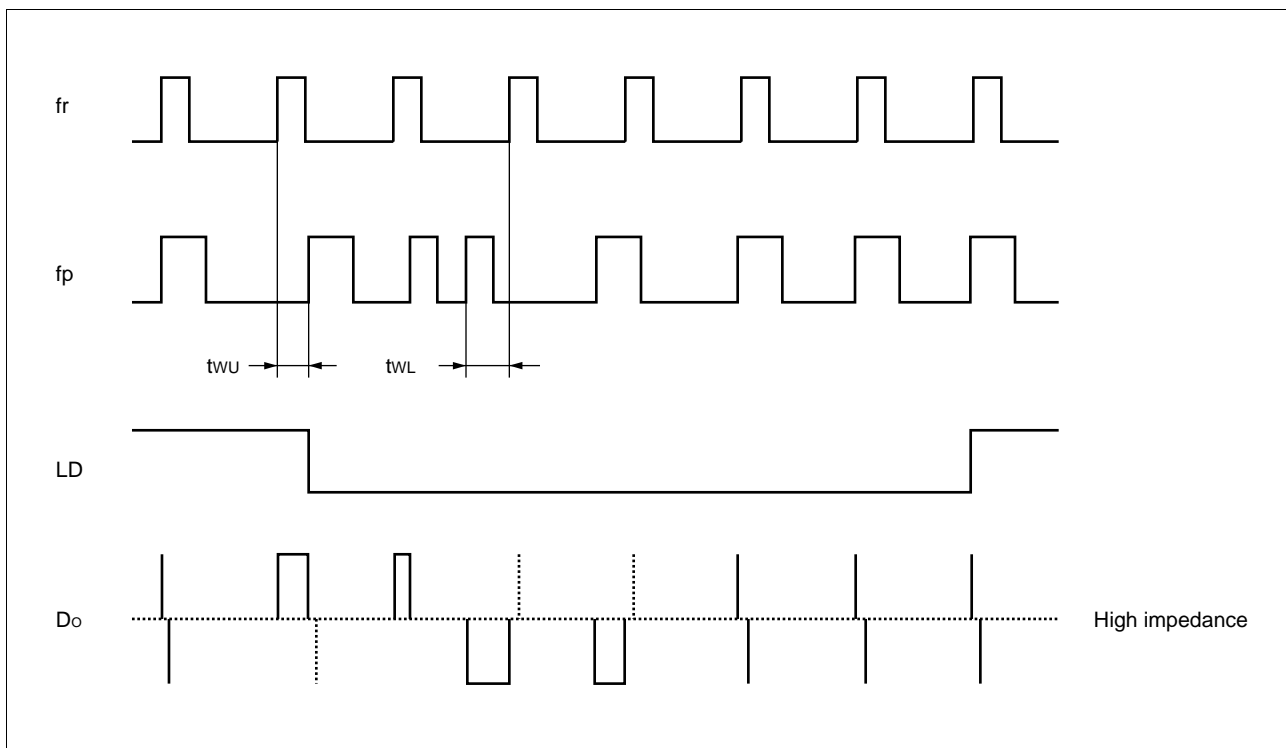
FUNCTIONAL DESCRIPTIONS

Two different frequencies can be selected by Div input "H" or "L".
The divide ratios are calculated using the following equation:

$$f_{vco} = \{(P \times N) + A\} \times f_{osc} \div R \quad (A < N)$$

| Symbol | Description | Div = "H" | Div = "L" |
|------------------|---|-------------------|-------------------|
| f _{vco} | Output frequency of external VCO | 233.15 MHz | 259.20 MHz |
| f _{osc} | Reference oscillation frequency | 19.2 MHz | 19.2 MHz |
| N | Divide ratio of the main counter | 291 | 33 |
| A | Divide ratio of the swallow counter | 7 | 12 |
| P | Preset divide ratio of dual modulus prescaler | 16/17 | 16/17 |
| R | Divide ratio of the reference counter | 384 (fr = 50 kHz) | 40 (fr = 480 kHz) |

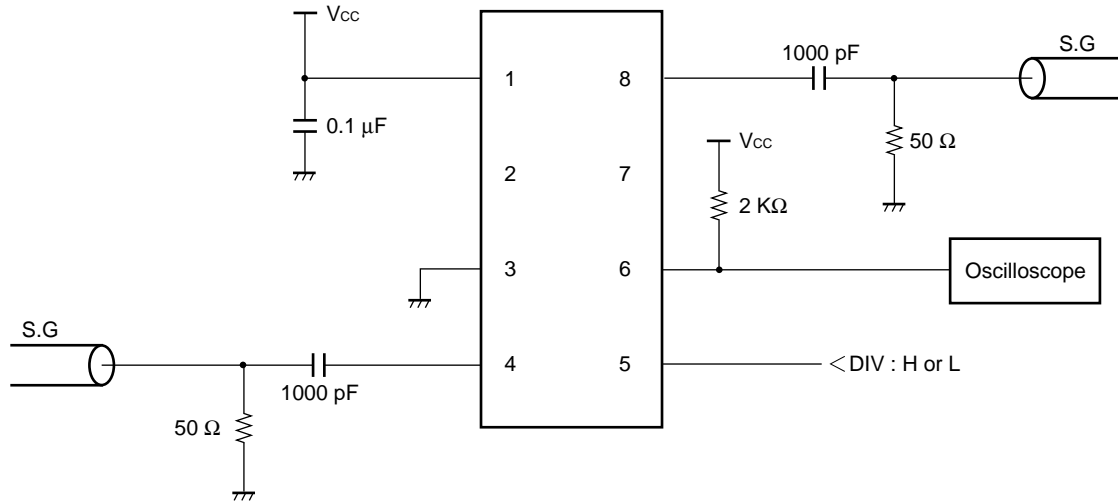
PHASE DETECTOR TIME CHART



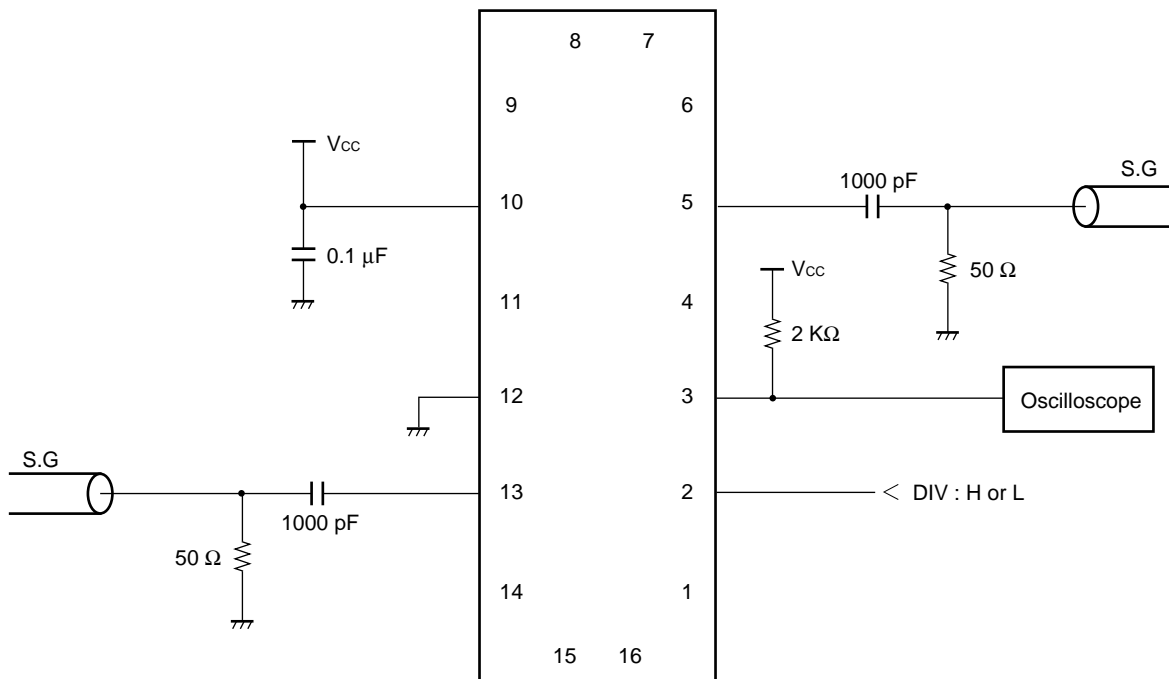
- Note:
- Phase error detection range: -2π to $+2\pi$
 - Pulses on Do output signal during locked state are output to prevent dead zone.
 - LD output becomes low when phase is t_{wU} or more. LD output becomes high when phase error is t_{wL} or less and continues to be so for three cycles or more.
 - t_{wU} and t_{wL} depend on OSCin input frequency.
 - $t_{wU} \geq 8/f_{osc}$ (s) (e. g. $t_{wU} \geq 625.0ns$, $f_{osc} = 12.8$ MHz)
 - $t_{wL} \leq 16/f_{osc}$ (s) (e. g. $t_{wL} \leq 1250.0ns$, $f_{osc} = 12.8$ MHz)

MEASUREMENT CIRCUIT (for measuring input sensitivity fin/OSCin)

SSOP-8



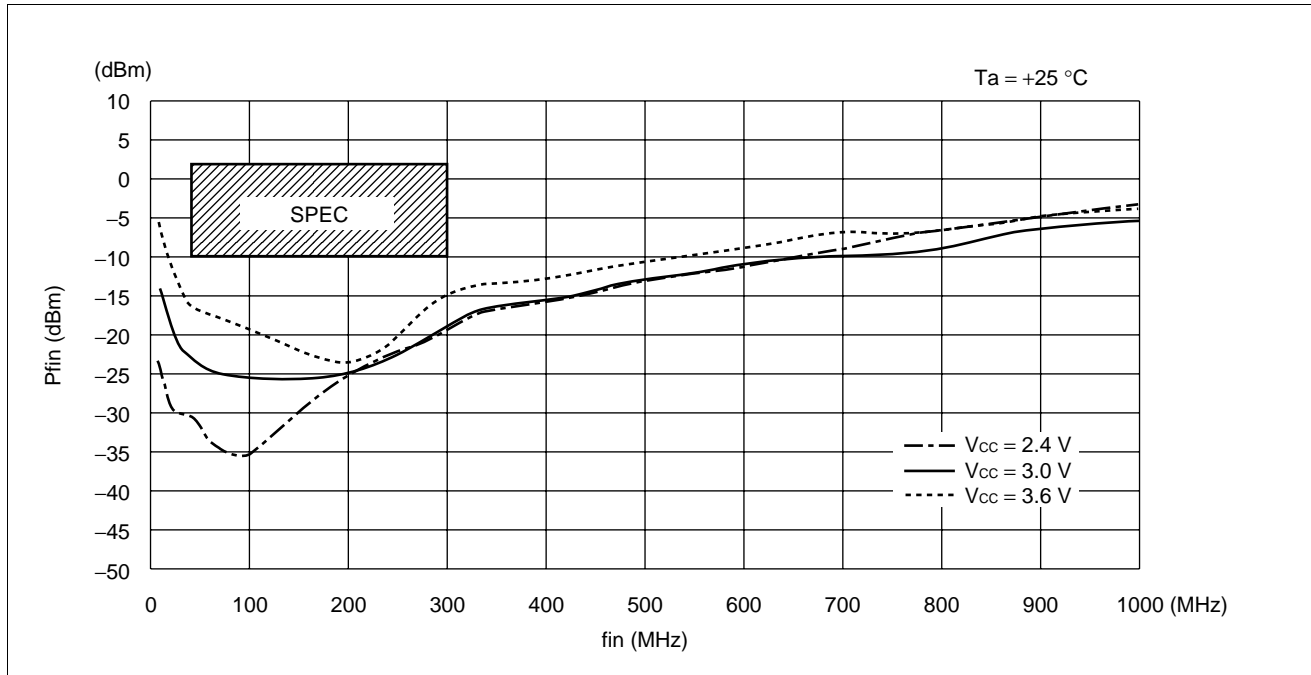
BCC-16



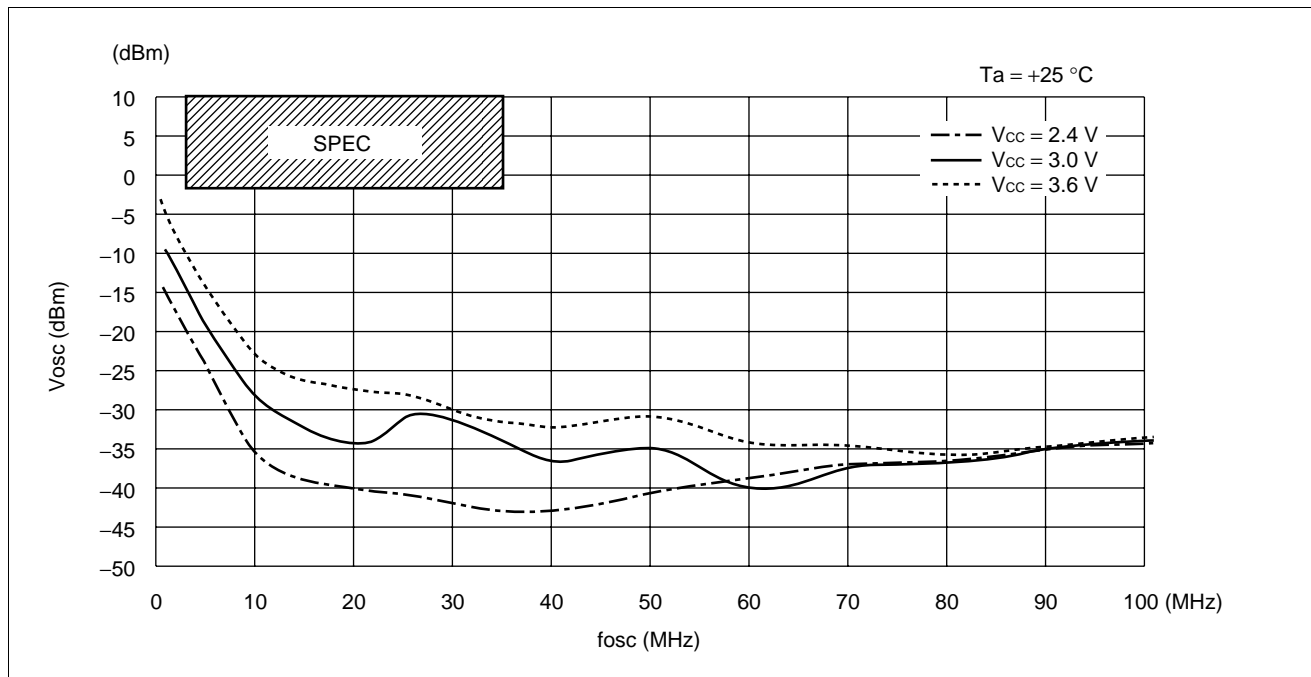
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■ TYPICAL CHARACTERISTICS

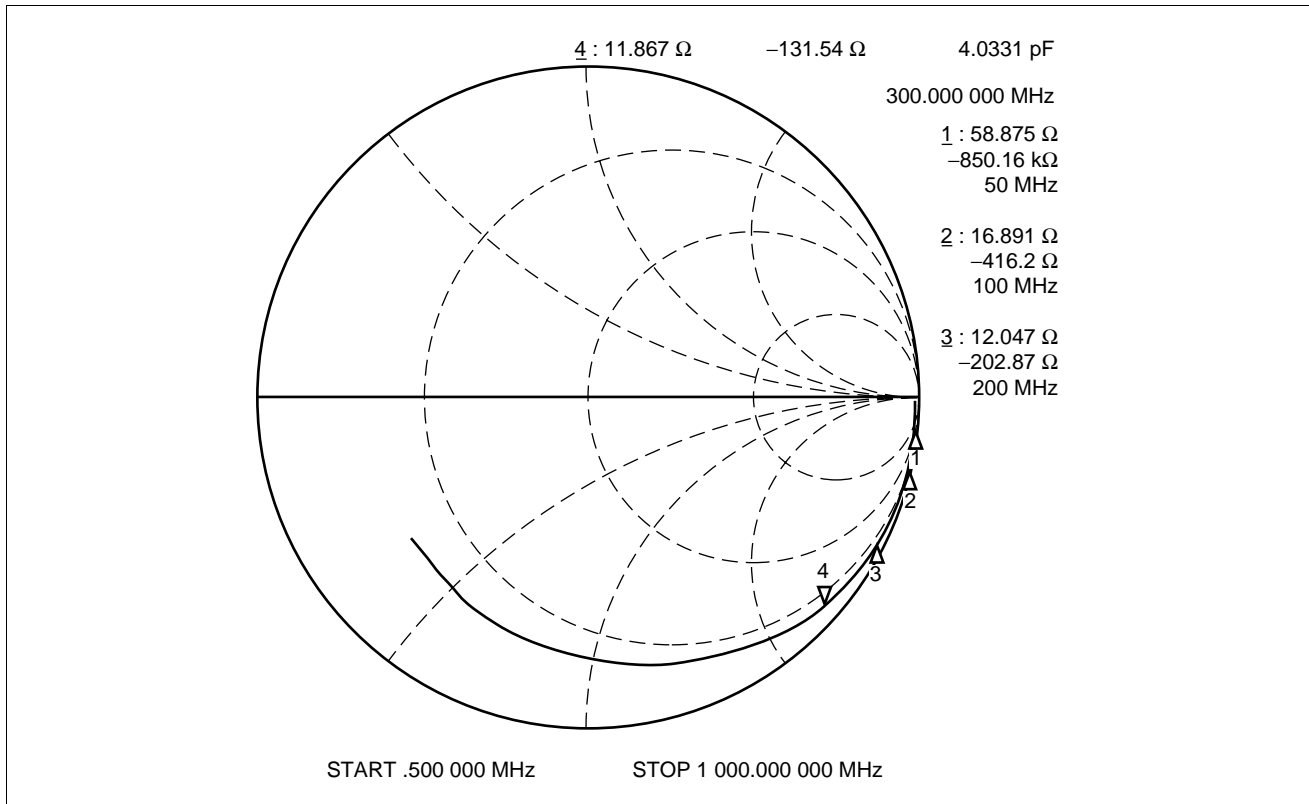
1. f_{in} Input Sensitivity



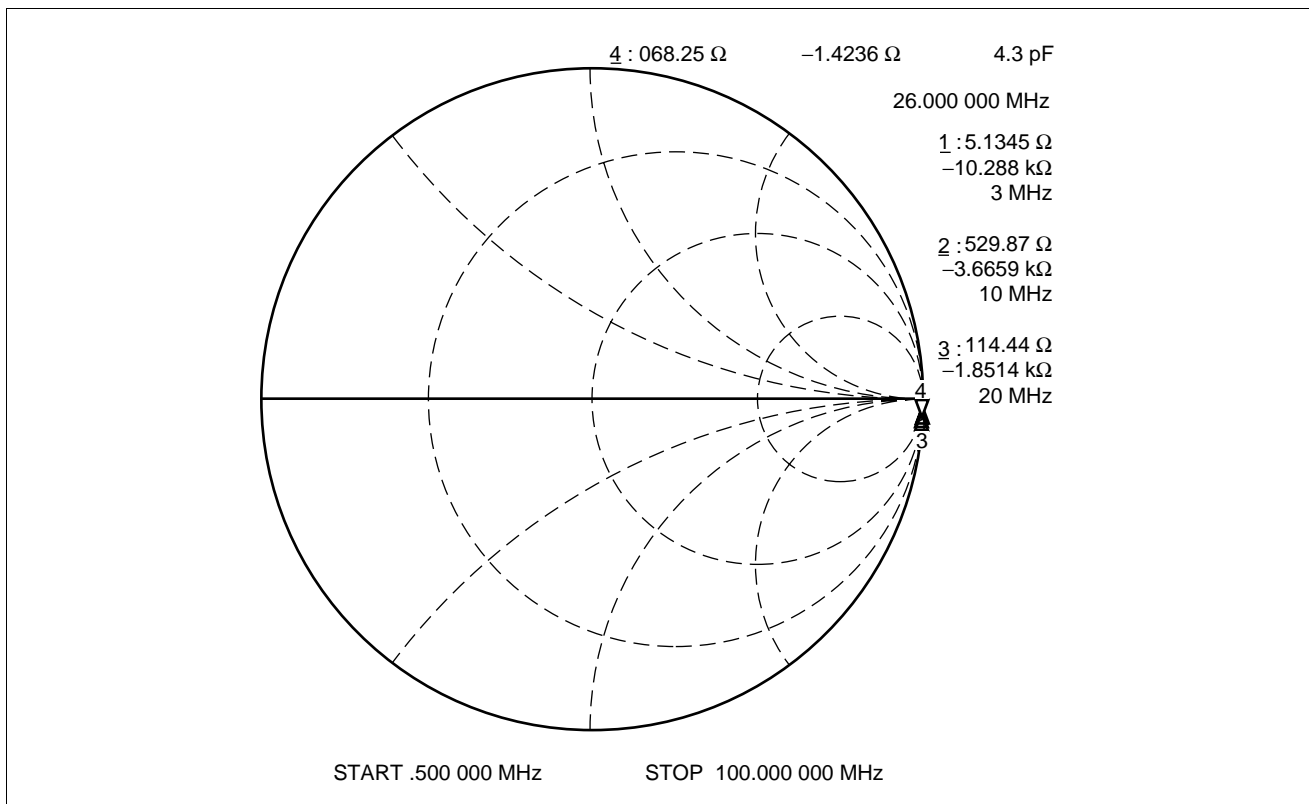
2. OSC_{IN} Input Sensitivity



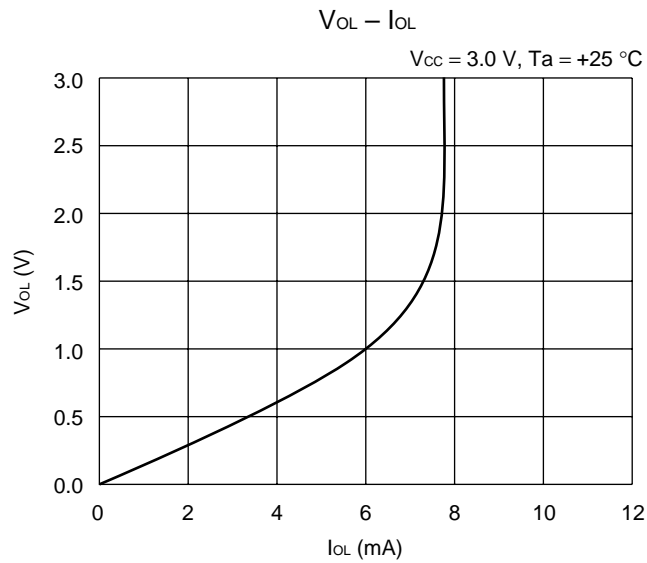
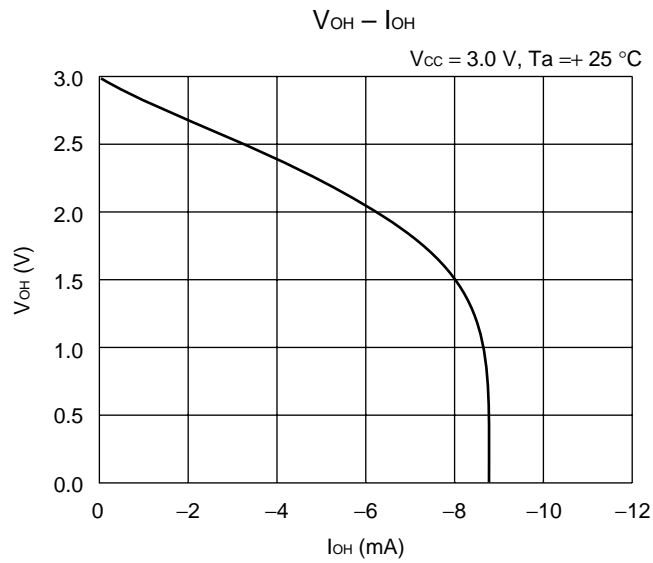
3. fin Input Impedance



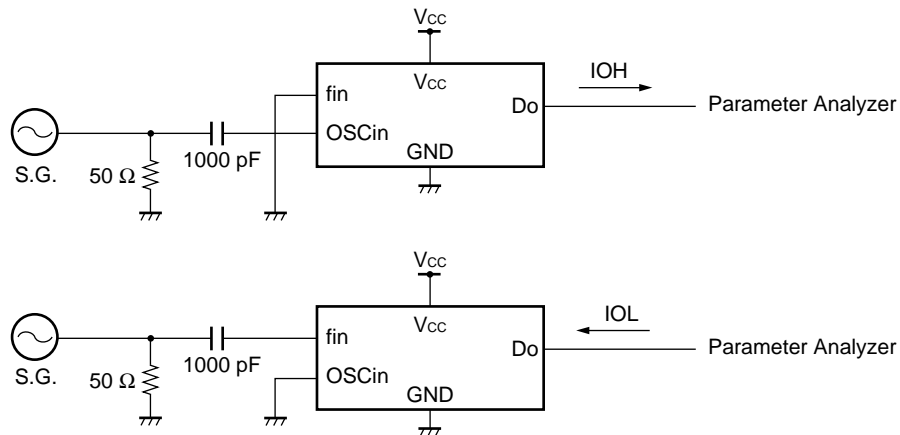
4. OSC_{IN} Input Impedance



5. Do Outut Current



Measurement Circuit



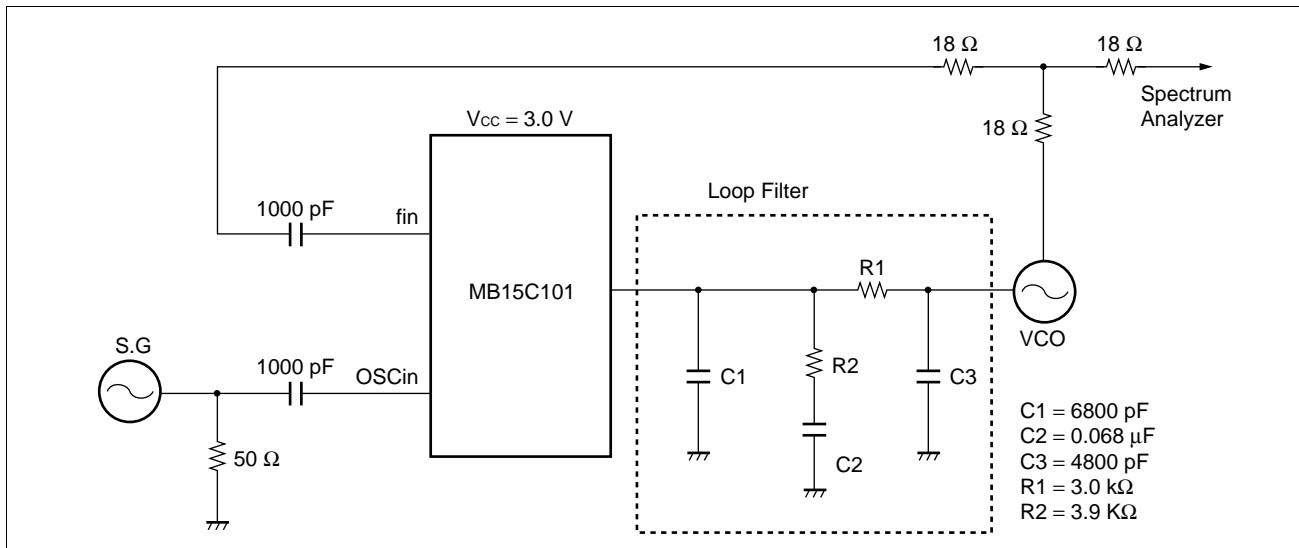
■ REFERENCE INFORMATION

1. Application Measurement

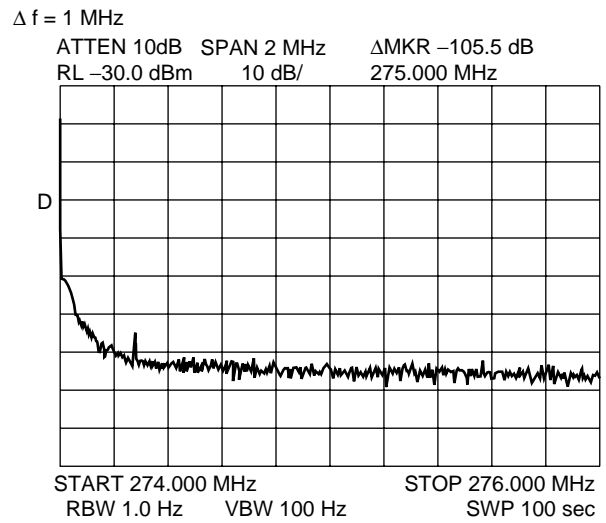
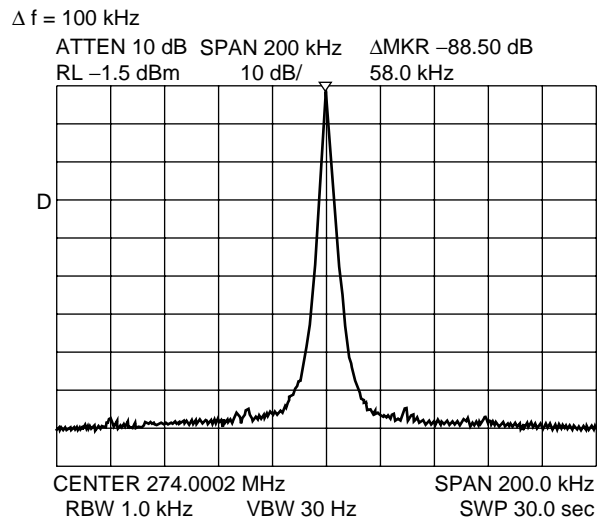
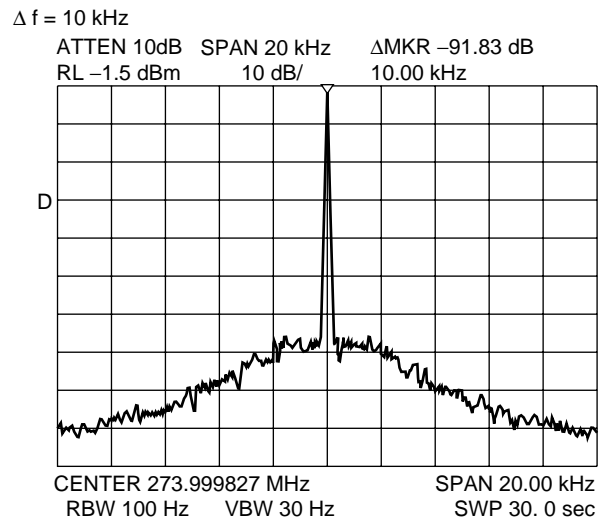
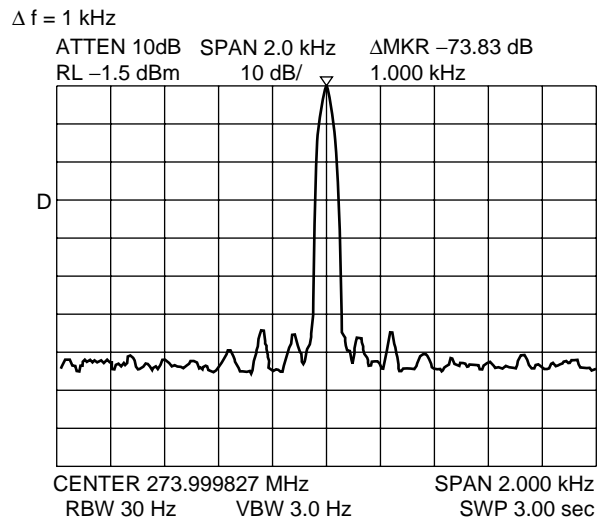
- Test Results

| | Results |
|--|---|
| Lockup time ± 1 kHz Un lock \rightarrow Lock Power on \rightarrow Lock | 2.3 ms 3.4 ms |
| Reference leakage ($\Delta f = 58$ kHz) | -88.5 dBc |
| Phase noise ($\Delta f = 1$ kHz) ($\Delta f = 10$ kHz) ($\Delta f = 100$ kHz) ($\Delta f = 1$ MHz) | -88.0 dBc/Hz -111.0 dBc/Hz -118.0 dBc/Hz -134.0 dBc/Hz |
| V _{CC} (V) | 3.0 V |
| VCO | Discrete VCO ($K_v = 3.5$ MHz/V) Lock Frequency = 274.0 MHz ($f_r = 58$ kHz) |

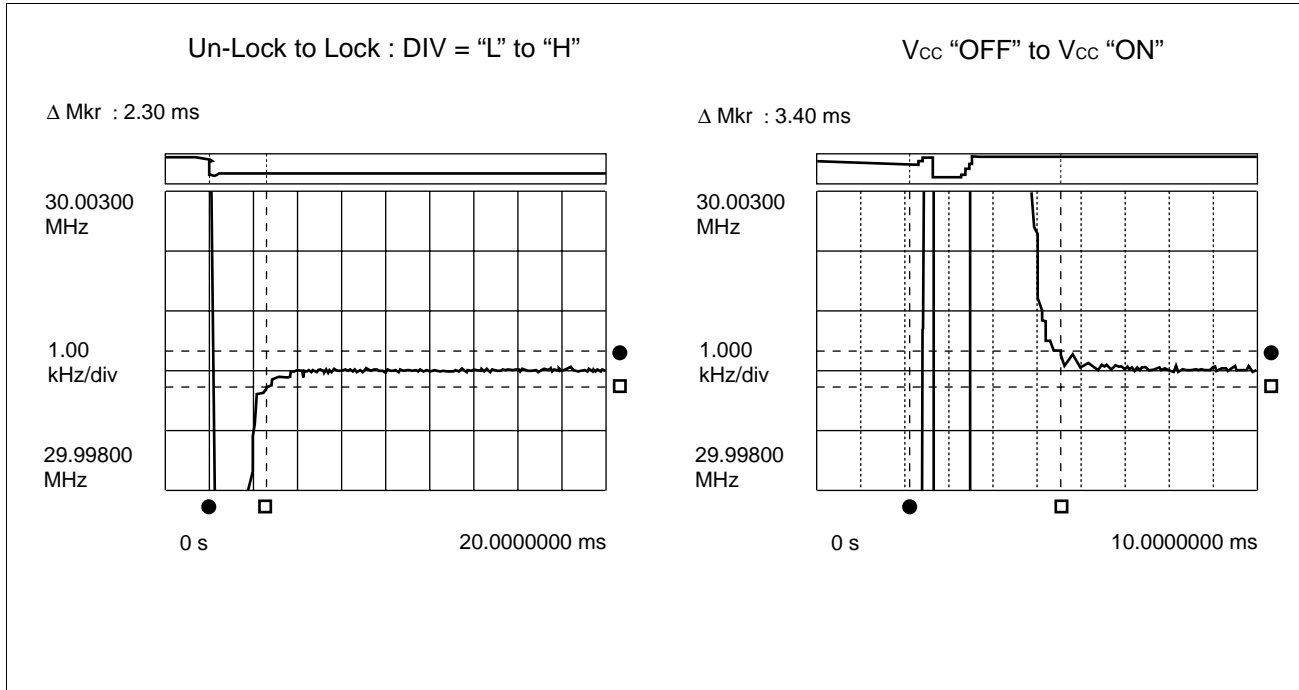
- Measurement Circuit



2. Phase Noise



3. Lockup Time: Un-Lock to Lock

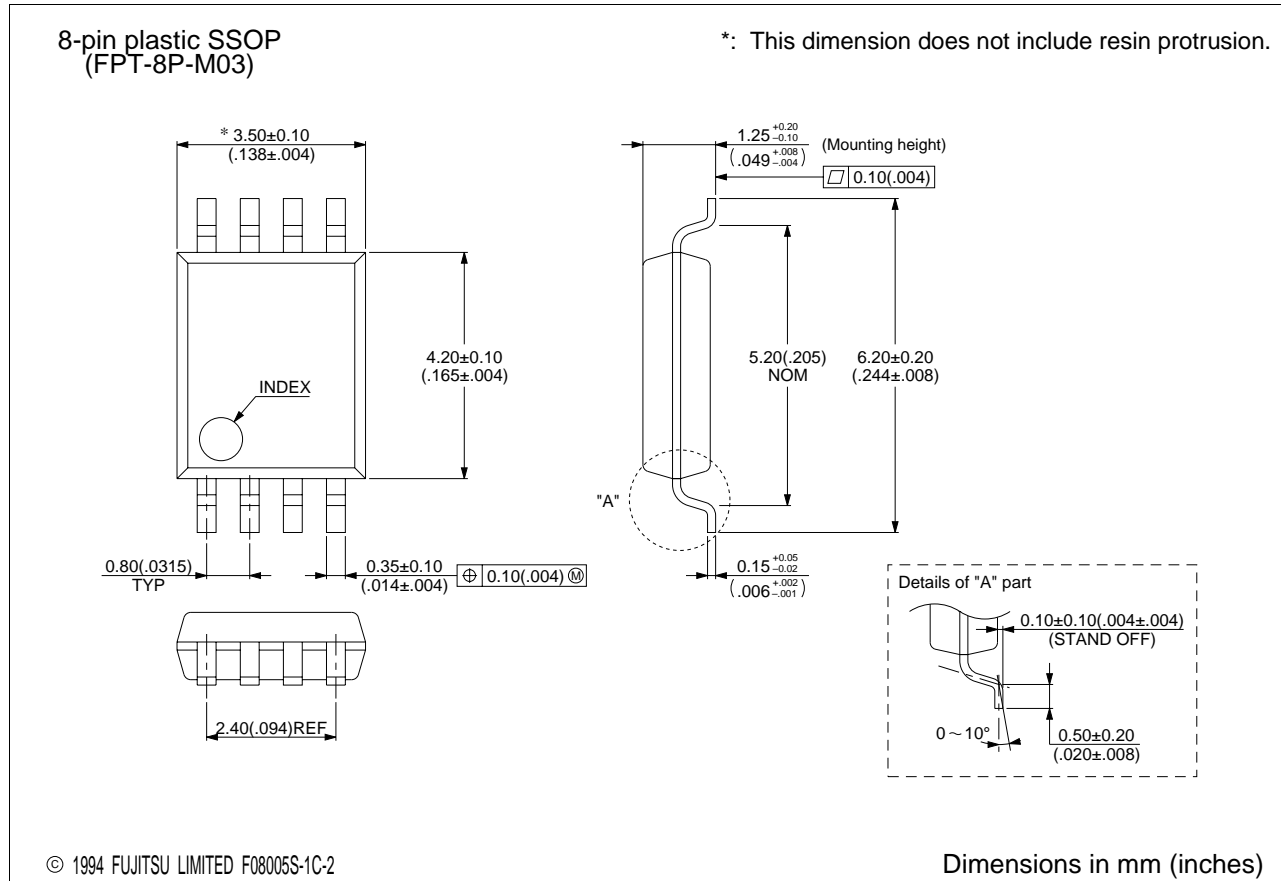


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■ ORDERING INFORMATION

| Part number | Package | Remarks |
|-------------|--------------------------------------|---------|
| MB15C101PFV | 8-pin, Plastic SSOP (FPT-8P-M03) | |
| MB15C101PV1 | 16-pad, Plastic BCC (LCC-16P-M06) | |

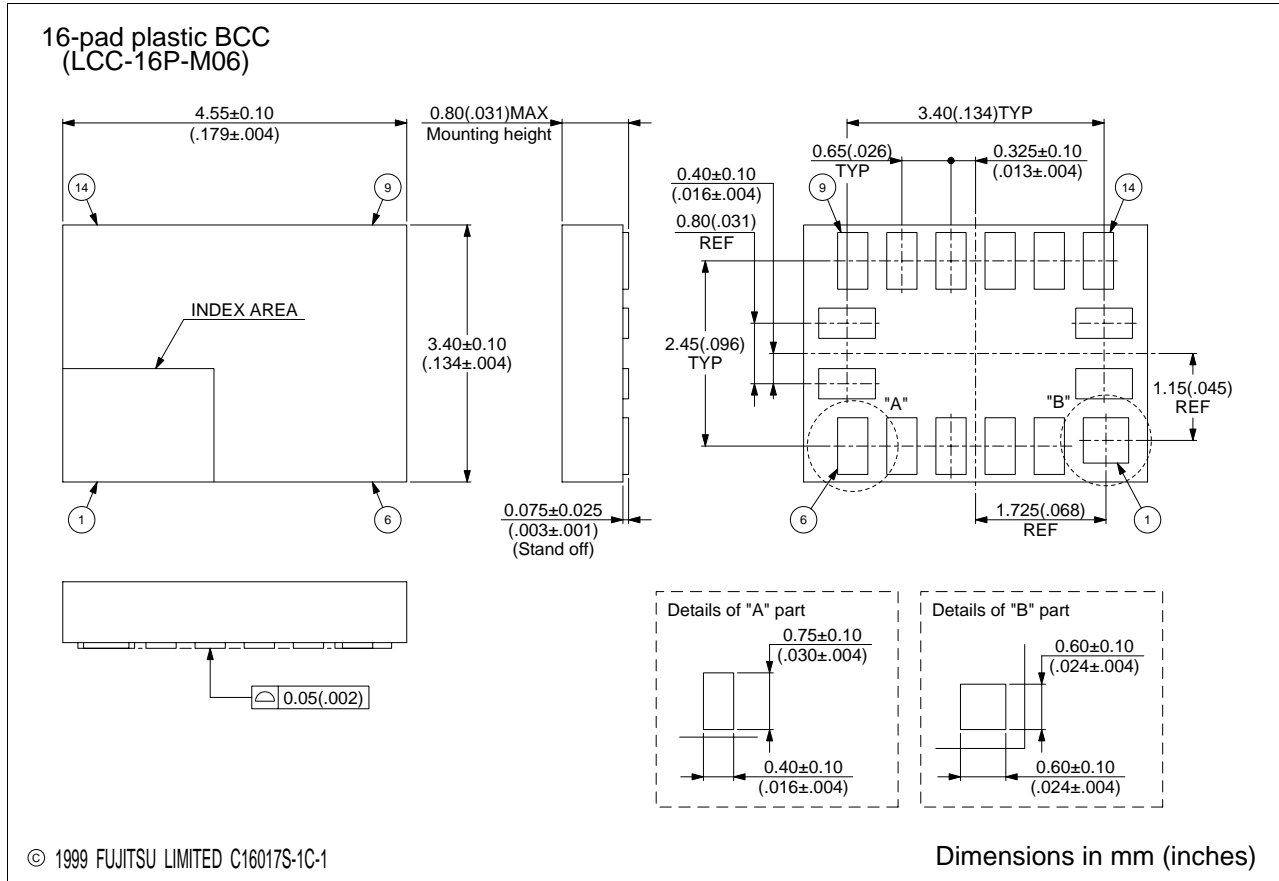
■ PACKAGE DIMENSIONS



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