



## **Technical Reference Guide**

HP Compaq dc7900 Series  
Business Desktop Computers

Document Part Number: 506665-001

### **September 2008**

This document provides information on the design, architecture, function, and capabilities of the HP Compaq dc7900 Series Business Desktop Computers. This information may be used by engineers, technicians, administrators, or anyone needing detailed information on the products covered.

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HP Compaq dc7900 Series Business Desktop Computers

First Edition (September 2008)

Document Part Number: 506665-001

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# Introduction

## 1.1 About this Guide

This guide provides technical information about HP Compaq dc7900 Business PC personal computers that feature Intel processors and the Intel Q45 Express chipset. This document describes in detail the system's design and operation for programmers, engineers, technicians, and system administrators, as well as end-users wanting detailed information.

The chapters of this guide primarily describe the hardware and firmware elements and primarily deal with the system board and the power supply assembly. The appendices contain general data such as error codes and information about standard peripheral devices such as keyboards, graphics cards, and communications adapters.

This guide can be used either as an online document or in hardcopy form.

### 1.1.1 Online Viewing

Online viewing allows for quick navigating and convenient searching through the document. A color monitor will also allow the user to view the color shading used to highlight differential data. A softcopy of the latest edition of this guide is available for downloading in .pdf file format at the following URL: [www.hp.com](http://www.hp.com)

Viewing the file requires a copy of Adobe Acrobat Reader available at no charge from Adobe Systems, Inc. at the following URL: [www.adobe.com](http://www.adobe.com)

### 1.1.2 Hardcopy

A hardcopy of this guide may be obtained by printing from the .pdf file. The document is designed for printing in an 8 ½ x 11-inch format.

## 1.2 Additional Information Sources

For more information on components mentioned in this guide refer to the indicated manufacturers' documentation, which may be available at the following online sources:

- HP Corporation: [www.hp.com](http://www.hp.com)
- Intel Corporation: [www.intel.com](http://www.intel.com)
- Serial ATA International Organization (SATA-IO): [www.serialATA.org](http://www.serialATA.org).
- USB user group: [www.usb.org](http://www.usb.org)

## 1.3 Serial Number

The serial number is located on a sticker placed on the exterior cabinet. The serial number is also written into firmware and may be read with HP Diagnostics or Insight Manager utilities.


## 1.4 Notational Conventions

The notational guidelines used in this guide are described in the following subsections.


### 1.4.1 Special Notices

The usage of warnings, cautions, and notes is described as follows:


---

 **WARNING:** Text set off in this manner indicates that failure to follow directions could result in bodily harm or loss of life.

---

 **CAUTION:** Text set off in this manner indicates that failure to follow directions could result in damage to equipment or loss of information.

---

 Text set off in this manner provides information that may be helpful.

---

### 1.4.2 Values

Differences between bytes and bits are indicated as follows:

MB = megabytes

Mb = megabits

### 1.4.3 Ranges

Ranges or limits for a parameter are shown using the following methods:

---

Example A: Bits <7..4> = bits 7, 6, 5, and 4.

---

Example B: IRQ3-7, 9 = IRQ signals 3 through 7, and IRQ signal 9

---



## 1.5 Common Acronyms and Abbreviations

Table 1-1 lists the acronyms and abbreviations used in this guide.

| <b>Acronym or Abbreviation</b> | <b>Description</b>   |
|--------------------------------|--|
| A                              | ampere   |
| AC                             | alternating current  |
| ACPI                           | Advanced Configuration and Power Interface                 |
| A/D                            | analog-to-digital  |
| ADC                            | Analog-to-digital converter                                |
| ADD or ADD2                    | Advanced digital display (card)                            |
| AGP                            | Accelerated graphics port                                  |
| AHCI                           | SATA Advanced Host controller Interface                    |
| AMT                            | Active Management Technology                               |
| API                            | application programming interface                          |
| APIC                           | Advanced Programmable Interrupt Controller                 |
| APM                            | advanced power management                                  |
| AOL                            | Alert-On-LAN™  |
| ASIC                           | application-specific integrated circuit                    |
| ASF                            | Alert Standard Format                                      |
| AT                             | 1. attention (modem commands) 2. 286-based PC architecture |
| ATA                            | AT attachment (IDE protocol)                               |
| ATAPI                          | ATA w/packet interface extensions                          |
| AVI                            | audio-video interleaved                                    |
| AVGA                           | Advanced VGA   |
| AWG                            | American Wire Gauge (specification)                        |
| BAT                            | Basic assurance test                                       |
| BCD                            | binary-coded decimal                                       |
| BIOS                           | basic input/output system                                  |
| bis                            | second/new revision  |
| BNC                            | Bayonet Neill-Concelman (connector type)                   |
| bps or b/s                     | bits per second  |
| BSP                            | Bootstrap processor  |
| BTO                            | Built to order   |
| CAS                            | column address strobe                                      |
| CD                             | compact disk   |
| CD-ROM                         | compact disk read-only memory                              |

**Table 1-1 (Continued)  
Acronyms and Abbreviations**

| <b>Acronym or Abbreviation</b> | <b>Description</b>   |
|--------------------------------|--|
| CDS                            | compact disk system  |
| CGA                            | color graphics adapter   |
| Ch                             | Channel, chapter   |
| cm                             | centimeter   |
| CMC                            | cache/memory controller  |
| CMOS                           | complimentary metal-oxide semiconductor (configuration memory) |
| Cntrl                          | controller   |
| Cntrl                          | control  |
| codec                          | 1. coder/decoder 2. compressor/decompressor                    |
| CPQ                            | Compaq   |
| CPU                            | central processing unit  |
| CRIMM                          | Continuity (blank) RIMM  |
| CRT                            | cathode ray tube   |
| CSM                            | 1. Compaq system management 2. Compaq server management        |
| DAC                            | digital-to-analog converter                                    |
| DC                             | direct current   |
| DCH                            | DOS compatibility hole   |
| DDC                            | Display Data Channel   |
| DDR                            | Double data rate (memory)                                      |
| DIMM                           | dual inline memory module                                      |
| DIN                            | Deutsche IndustriNorm (connector type)                         |
| DIP                            | dual inline package  |
| DMA                            | direct memory access   |
| DMI                            | Desktop management interface                                   |
| dpi                            | dots per inch  |
| DRAM                           | dynamic random access memory                                   |
| DRQ                            | data request   |
| DVI                            | Digital video interface  |
| dword                          | Double word (32 bits)  |
| EDID                           | extended display identification data                           |
| EDO                            | extended data out (RAM type)                                   |
| EEPROM                         | electrically erasable PROM                                     |
| EGA                            | enhanced graphics adapter                                      |
| EIA                            | Electronic Industry Association                                |

**Table 1-1 (Continued)**  
**Acronyms and Abbreviations**

| <b>Acronym or Abbreviation</b> | <b>Description</b>                                |
|--------------------------------|---|
| EISA                           | extended ISA                                      |
| EPP                            | enhanced parallel port                            |
| EIDE                           | enhanced IDE                                      |
| ESCD                           | Extended System Configuration Data (format)       |
| EV                             | Environmental Variable (data)                     |
| ExCA                           | Exchangeable Card Architecture                    |
| FIFO                           | first in/first out                                |
| FL                             | flag (register)                                   |
| FM                             | frequency modulation                              |
| FPM                            | fast page mode (RAM type)                         |
| FPU                            | Floating point unit (numeric or math coprocessor) |
| FPS                            | Frames per second                                 |
| ft                             | Foot/feet   |
| GB                             | gigabyte  |
| GMCH                           | Graphics/memory controller hub                    |
| GND                            | ground  |
| GPIO                           | general purpose I/O                               |
| GPOC                           | general purpose open-collector                    |
| GART                           | Graphics address re-mapping table                 |
| GUI                            | graphic user interface                            |
| h                              | hexadecimal                                       |
| HDD                            | hard disk drive                                   |
| HW                             | hardware  |
| hex                            | hexadecimal                                       |
| Hz                             | Hertz (cycles-per-second)                         |
| ICH                            | I/O controller hub                                |
| IDE                            | integrated drive element                          |
| IEEE                           | Institute of Electrical and Electronic Engineers  |
| IF                             | interrupt flag                                    |
| I/F                            | interface   |
| IGC                            | integrated graphics controller                    |
| in                             | inch  |
| INT                            | interrupt   |
| I/O                            | input/output                                      |
| IPL                            | initial program loader                            |

**Table 1-1 (Continued)**  
**Acronyms and Abbreviations**

| <b>Acronym or Abbreviation</b> | <b>Description</b>                            |
|--------------------------------|---|
| IrDA                           | Infrared Data Association                     |
| IRQ                            | interrupt request                             |
| ISA                            | industry standard architecture                |
| Kb/KB                          | kilobits/kilobytes (x 1024 bits/x 1024 bytes) |
| Kb/s                           | kilobits per second                           |
| kg                             | kilogram                                      |
| KHz                            | kilohertz                                     |
| kV                             | kilovolt                                      |
| lb                             | pound   |
| LAN                            | local area network                            |
| LCD                            | liquid crystal display                        |
| LED                            | light-emitting diode                          |
| LPC                            | Low pin count                                 |
| LSI                            | large scale integration                       |
| LSb/LSB                        | least significant bit/least significant byte  |
| LUN                            | logical unit (SCSI)                           |
| m                              | Meter   |
| MCH                            | Memory controller hub                         |
| MMX                            | multimedia extensions                         |
| MPEG                           | Motion Picture Experts Group                  |
| ms                             | millisecond                                   |
| MSb/MSB                        | most significant bit/most significant byte    |
| mux                            | multiplex                                     |
| MVA                            | motion video acceleration                     |
| MVW                            | motion video window                           |
| <i>n</i>                       | variable parameter/value                      |
| NIC                            | network interface card/controller             |
| NiMH                           | nickel-metal hydride                          |
| NMI                            | non-maskable interrupt                        |
| NRZI                           | Non-return-to-zero inverted                   |
| ns                             | nanosecond                                    |
| NT                             | nested task flag                              |
| NTSC                           | National Television Standards Committee       |
| NVRAM                          | non-volatile random access memory             |

**Table 1-1 (Continued)**  
**Acronyms and Abbreviations**

| <b>Acronym or Abbreviation</b> | <b>Description</b>                                      |
|--------------------------------|---|
| ODD                            | optical disk drive                                      |
| OS                             | operating system  |
| PAL                            | 1. programmable array logic 2. phase alternating line   |
| PATA                           | Parallel ATA  |
| PC                             | Personal computer                                       |
| PCA                            | Printed circuit assembly                                |
| PCI                            | peripheral component interconnect                       |
| PCI-E                          | PCI Express   |
| PCM                            | pulse code modulation                                   |
| PCMCIA                         | Personal Computer Memory Card International Association |
| PEG                            | PCI express graphics                                    |
| PFC                            | Power factor correction                                 |
| PIN                            | personal identification number                          |
| PIO                            | Programmed I/O  |
| PN                             | Part number   |
| POST                           | power-on self test                                      |
| PROM                           | programmable read-only memory                           |
| PTR                            | pointer   |
| RAID                           | Redundant array of inexpensive disks (drives)           |
| RAM                            | random access memory                                    |
| RAS                            | row address strobe                                      |
| rcvr                           | receiver  |
| RDRAM                          | (Direct) Rambus DRAM                                    |
| RGB                            | red/green/blue (monitor input)                          |
| RH                             | Relative humidity                                       |
| RMS                            | root mean square  |
| ROM                            | read-only memory  |
| RPM                            | revolutions per minute                                  |
| RTC                            | real time clock   |
| R/W                            | Read/Write  |
| SATA                           | Serial ATA  |
| SCSI                           | small computer system interface                         |
| SDR                            | Singles data rate (memory)                              |
| SDRAM                          | Synchronous Dynamic RAM                                 |

**Table 1-1 (Continued)  
Acronyms and Abbreviations**

| <b>Acronym or Abbreviation</b> | <b>Description</b>  |
|--------------------------------|---|
| SDVO                           | Serial digital video output                                   |
| SEC                            | Single Edge-Connector   |
| SECAM                          | sequential colour avec memoire (sequential color with memory) |
| SF                             | sign flag   |
| SGRAM                          | Synchronous Graphics RAM                                      |
| SIMD                           | Single instruction multiple data                              |
| SIMM                           | single in-line memory module                                  |
| SMART                          | Self Monitor Analysis Report Technology                       |
| SMI                            | system management interrupt                                   |
| SMM                            | system management mode  |
| SMRAM                          | system management RAM   |
| SPD                            | serial presence detect  |
| SPDIF                          | Sony/Philips Digital Interface (IEC-958 specification)        |
| SPN                            | Spare part number   |
| SPP                            | standard parallel port  |
| SRAM                           | static RAM  |
| SSD                            | solid state disk (drive)                                      |
| SSE                            | Streaming SIMD extensions                                     |
| STN                            | super twist pneumatic   |
| SVGA                           | super VGA   |
| SW                             | software  |
| TAD                            | telephone answering device                                    |
| TAFI                           | Temperature-sensing And Fan control Integrated circuit        |
| TCP                            | tape carrier package, transmission control protocol           |
| TF                             | trap flag   |
| TFT                            | thin-film transistor  |
| TIA                            | Telecommunications Information Administration                 |
| TPE                            | twisted pair ethernet   |
| TPI                            | track per inch  |
| TTL                            | transistor-transistor logic                                   |
| TV                             | television  |
| TX                             | transmit  |
| UART                           | universal asynchronous receiver/transmitter                   |
| UDMA                           | Ultra DMA   |

**Table 1-1 (Continued)**  
**Acronyms and Abbreviations**

| <b>Acronym or Abbreviation</b> | <b>Description</b>                     |
|--------------------------------|--|
| URL                            | Uniform resource locator               |
| us/μs                          | microsecond                            |
| USB                            | Universal Serial Bus                   |
| UTP                            | unshielded twisted pair                |
| V                              | volt                                   |
| VAC                            | Volts alternating current              |
| VDC                            | Volts direct current                   |
| VESA                           | Video Electronic Standards Association |
| VGA                            | video graphics adapter                 |
| VLSI                           | very large scale integration           |
| VRAM                           | Video RAM                              |
| W                              | watt                                   |
| WOL                            | Wake-On-LAN                            |
| WRAM                           | Windows RAM                            |
| ZF                             | zero flag                              |
| ZIF                            | zero insertion force (socket)          |





---

## System Overview

### 2.1 Introduction

The HP Compaq dc7900 Business PC personal computers (Figure 2-1) deliver an outstanding combination of manageability, serviceability, and compatibility for enterprise environments. Based on the Intel processor with the Intel Q45 Express chipset, these systems emphasize performance along with industry compatibility. These models feature a similar architecture incorporating both PCI 2.3 and PCIe 1.1 buses. All models are easily upgradeable and expandable to keep pace with the needs of the office enterprise.



*Figure 2-1. HP Compaq dc7900 Business PCs*

This chapter includes the following topics:

- Features (2.2)
- System architecture (2.3)
- Specifications (2.4)

## 2.2 Features

The following standard features are included on all models unless otherwise indicated:

- Intel processor in LGA775 (Socket T) package
- Integrated graphics controller with dual monitor support:
  - One VGA connector
  - One DisplayPort (DP) connector with Multimode support
- PC2-6400 and PC2-5300 (DDR2) DIMM support
- Hard drive fault prediction
- Eight USB 2.0-compliant ports
- High definition (HD) audio processor with one headphone output, at least one microphone input, one line output, and one line input
- Network interface controller providing 10/100/1000Base T support
- Plug 'n Play compatible (with ESCD support)
- Intelligent Manageability support
- Management/security features including:
  - Flash ROM Boot Block
  - Diskette drive disable, boot disable, write protect
  - Power-on password
  - Administrator password
  - Serial port disable (SFF and CMT form factors only)
  - Smart Cover (hood) Sense
  - Smart Cover (hood) Lock (SFF and CMT form factors only)
  - USB port disable
  - Intel Standard Manageability support
  - Intel vPro Technology
  - HP Virtual Safe Browser
- PS/2 enhanced keyboard
- PS/2 optical scroll mouse
- Energy Star compliancy met by all USDT form factors (Energy Star-qualified configurations of SFF and CMT form factors are available).

Table 2-1 shows the differences in features between the different PC series based on form factor:

| <b>Table 2-1<br/>Feature Difference Matrix by Form Factor</b>                |  |  |  |
|--|--|--|--|
|  | <b>USDT</b>  | <b>SFF</b>   | <b>CMT</b>   |
| Processor types supported  | Intel Celeron,<br>Pentium dual-core,<br>Core 2 Duo | Intel Celeron,<br>Pentium dual-core,<br>Core 2 Duo,<br>Core 2 Quad | Intel Celeron,<br>Pentium dual-core,<br>Core 2 Duo,<br>Core 2 Quad |
| Processor wattage (max)  | 65 W   | 95 W   | 95 W   |
| Memory:<br># & type of sockets<br>Maximum memory                             | 2 SODIMM<br>8 GB                                   | 4 DIMM<br>16 GB  | 4 DIMM<br>16 GB  |
| Serial ports   | 0  | 1 std., 1 opt. [1]   | 1 std., 1 opt. [1]   |
| Parallel ports   | 0  | optional   | optional   |
| Drive bays:<br>Externally accessible<br>Internal                             | 1<br>1   | 2<br>1   | 4<br>2   |
| Drive types supported  | 1 HDD,<br>1 slimline ODD                           | 2 HDDs,<br>1 ODD,<br>RAID1   | 2 HDDs,<br>2 ODDs,<br>RAID1  |
| PCIe slots:<br>x16 graphics (PCIe 2.0)<br>x1 connector<br>x4 (x16 connector) | 0<br>1 [2]   | 1 [3, 4]<br>1 [3]<br>1 [3, 4]                                      | 1<br>1<br>1  |
| PCI 2.3 32-bit 5-V slots   | 0  | 1 half-height<br>or<br>2 full-height [5]                           | 3<br>full-height   |
| Power Supply Unit:<br>Module type<br>power rating                            | external<br>135-watt                               | internal<br>240-watt   | internal<br>365-watt   |

**NOTES:**

- [1] 2nd serial port requires optional cable/bracket assembly.
- [2] PCIe Mini Card slot.
- [3] Supports low-profile card in standard configuration. Not accessible if PCI riser card field option is installed.
- [4] Accepts low-profile PCIe card: height = 2.5 in., length = 6.6 in.
- [5] Full-height PCI slots require installation of PCI riser card field option (full-height dimensions: height = 4.2 in., length = 6.875 in.).

## 2.3 System Architecture

The systems covered in this guide feature an architecture based on the Intel Q45 Express chipset (Figure 2-2). All systems covered in this guide include the following key components:

- Intel Pentium Dual-Core, Core 2 Duo, Core 2 Quad, or Celeron processor.
- Intel Q45 Express chipset - Includes Q45 GMCH and 82801 ICH10-DO
- Super I/O (SIO) controller supporting PS/2 keyboard and mouse peripherals
- AD1884A audio controller supporting line in, line out, microphone in, and headphones out
- Intel 82567LM GbE network interface controller

The Q45 chipset provides a major portion of system functionality. Designed to complement the latest Intel processors, the Q45 GMCH integrates with the processor through a 800/1066/1333-MHz Front-Side Bus (FSB) and communicates with the ICH10-DO component through the Direct Media Interface (DMI). The integrated graphics controller of the Q45 on SFF and CMT systems can be upgraded through a PCI Express (PCIe) x16 graphics slot. All systems include a serial ATA (SATA) hard drive in the standard configuration.

Table 2-2 lists the differences between models by form factor.

**Table 2-2.  
Architectural Differences By Form Factor**

| Function                              | USDT      | SFF      | CMT      |
|---------------------------------------|-----------|----------|----------|
| Memory sockets                        | 2 SODIMMs | 4 DIMMs  | 4 DIMMs  |
| PCIe 2.0 x16 graphics slot            | No        | 1 [1]    | 1        |
| PCIe x4 (x16 connector) graphics slot | No        | 1 [1]    | 1        |
| # of PCIe 1.1 x1 slots                | 0         | 1 [1]    | 1        |
| # of PCI 2.3 slots                    | 0         | 1 [3]    | 3        |
| Serial port                           | 0         | 1 [4]    | 1 [4]    |
| Parallel ports                        | 0         | optional | optional |
| SATA interfaces                       | 2         | 3        | 4        |
| eSATA capability [2]                  | No        | Yes      | Yes      |

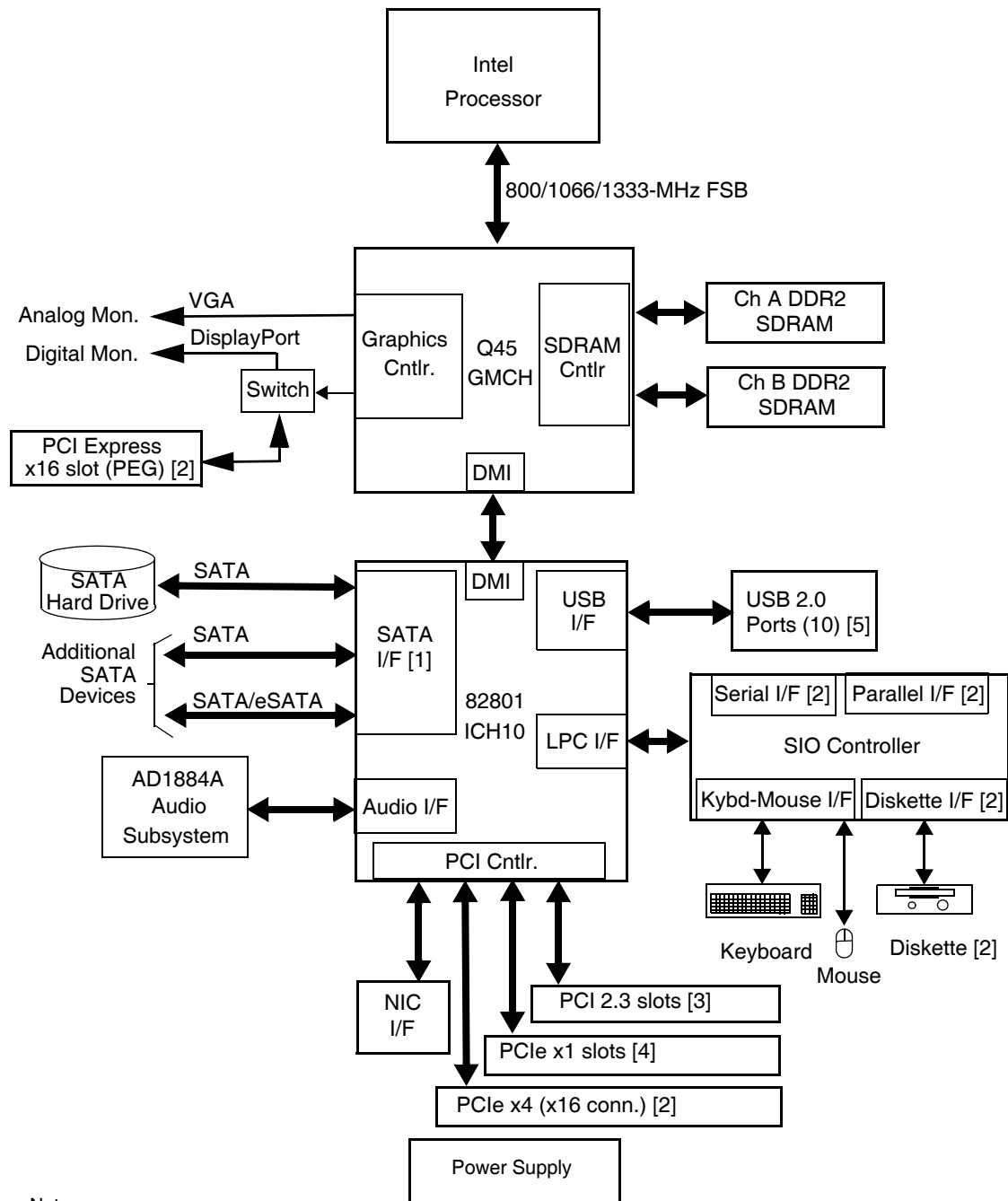
Notes:

[1] Low-profile slot. Not accessible if PCI riser is installed.

[2] Requires optional bracket/cable assembly.

[3] Low-profile slot in standard configuration. 2 full-height slots supported with optional PCI riser.

[4] 2nd serial port possible with optional adapter.



## Notes:

- [1] 2 SATA ports in USDT, 3 SATA ports in SFF, 4 SATA ports in CMT, and 1 eSATA port in SFF and CMT.
- [2] SFF and CMT only
- [3] 0 slots in USDT, 1 or 2 slots in SFF, 3 slots in CMT
- [4] 1 MiniCard slot in USDT, 1 slot in SFF and CMT
- [5] 8 ports accessible externally, 2 ports accessible internally

Figure 2-2. HP Compaq dc7900 Business PC Architecture, Block diagram

## 2.3.1 Intel Processor Support

The models covered in this guide are designed to support the following processor types:

- Intel Celeron: single- and dual-core performance
- Intel Pentium Dual-Core: Dual core performance
- Intel Core2 Duo: energy-efficient dual-core performance
- Intel Core2 Quad: energy efficient quad-core design

These processors are backward-compatible with software written for earlier x86 microprocessors and include streaming SIMD extensions (SSE, SSE2, and SSE3) for enhancing 3D graphics and speech processing performance. Intel processors with vPro Technology include hardware-based tools that allow corporate IT organizations to remotely manage and protect systems.

The system board includes a zero-insertion-force (ZIF) Socket-T designed for mounting an LGA775-type processor package.

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**CAUTION:** The USDT form factor can support a processor rated up to 65 watts. The SFF and CMT form factors can support a processor rated up to 95 watts. Exceeding these limits can result in system damage and loss of data.

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The processor heatsink/fan assembly mounting differs between form factors. Always use the same assembly or one of the same type when replacing the processor. Refer to the applicable Service Reference Guide for detailed removal and replacement procedures of the heatsink/fan assembly and the processor.

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## 2.3.2 Chipset

The Intel Q45 Express chipset consists of a Graphics Memory Controller Hub (GMCH) and an enhanced I/O controller hub (ICH10-DO). Table 2-3 compares the functions provided by the chipsets.

**Table 2-3  
Chipset Components and Functionality**

| Components     | Function  |
|----------------|---|
| Q45 GMCH       | Intel Graphics Media Accelerator 4500 (integrated graphics controller)<br>PCIe 2.0 x16 graphics interface (1)<br>SDRAM controller supporting unbuffered, non-ECC PC2-6400 DDR2 DIMMs or SODIMMs<br>800-, 1066-, or 1333-MHz FSB   |
| 82801 ICH10-DO | PCI 2.3 bus I/F<br>PCI Express x1<br>LPC bus I/F<br>SMBus I/F<br>SATA I/F<br>HD audio interface<br>RTC/CMOS<br>IRQ controller<br>Power management logic<br>USB 1.1/2.0 controllers supporting 12 ports<br>(these systems provide 8 external, 3 internal)<br>Gigabit Ethernet controller |

The I/O controller hub (ICH10-DO) supports Intel vPro, which uses Active Management Technology (AMT). AMT is a hardware/firmware solution that operates on auxiliary power to allow 24/7 support of network alerting and management of the unit without regard to the power state or operating system. AMT capabilities include:

- System asset recovery (hardware and software configuration data)
- OS-independent system wellness and healing
- Software (virus) protection/management

## 2.3.3 Support Components

Input/output functions not provided by the chipset are handled by other support components. Some of these components also provide “housekeeping” and various other functions as well. Table 2-4 shows the functions provided by the support components.

**Table 2-4**  
**Support Component Functions**

| Component Name                             | Function  |
|--|---|
| WPCD376H SIO Controller                    | Keyboard and pointing device I/F<br>Diskette I/F [1]<br>Serial I/F (COM1 and COM2) [2]<br>Parallel I/F (LPT1, LPT2, or LPT3) [3]<br>PCI reset generation<br>Interrupt (IRQ) serializer<br>Power button and front panel LED logic<br>GPIO ports<br>Processor over temperature monitoring<br>Fan control and monitoring<br>Power supply voltage monitoring<br>SMBus and Low Pin Count (LPC) bus I/F |
| Intel 82567LM Network Interface Controller | 10/100/1000 Fast Ethernet network interface controller.   |
| AD1884A HD Audio Codec                     | Audio mixer<br>Two digital-to-analog stereo converters<br>Two analog-to-digital stereo converters<br>Analog I/O<br>Supports stereo (two-channel) audio streams  |

**NOTE:**

[1] Not used in USDT form factor.

[2] Com1 supported only on SFF and CMT form factors. COM2 requires external bracket/cable assembly.

[3] Supported only on SFF and CMT form factors, requires external bracket/cable assembly.

## 2.3.4 System Memory

These systems implement a dual-channel Double Data Rate (DDR2) memory architecture. All models support DDR2 800- and 667-MHz DIMMs. The USDT system provides two SODIMM sockets supporting up to eight gigabytes of memory while the SFF and CMT form factors provide four DIMM sockets and support a total of 16 gigabytes of memory.



DDR and DDR2 DIMMs are NOT interchangeable.



SODIMM and DIMM components are NOT interchangeable.



### 2.3.5 Mass Storage

All models support at least two mass storage devices, with one being externally accessible for removable media. These systems provide the following interfaces for internal storage devices:

USDT: two SATA interfaces

SFF: three SATA interfaces and one eSATA port

CMT: four SATA interfaces and one eSATA port

These systems may be preconfigured or upgraded with a SATA hard drive and one removable media drive such as a CD-ROM drive.

### 2.3.6 Serial Interface

The SFF and CMT form factors include a serial port accessible at the rear of the chassis. The SFF and CMT form factors may be upgraded with a second serial port option. The serial interface is RS-232-C/16550-compatible and supports standard baud rates up to 115,200 as well as two high-speed baud rates of 230K and 460K.

### 2.3.7 Universal Serial Bus Interface

All models provide ten Universal Serial Bus (USB) ports. Two ports are accessible at the front of the unit, six ports are accessible on the rear panel, and two ports are accessible through a header on the system board. The SFF and CMT form factors support a media card reader module that connects to the internal header. These systems support USB 1.1 and 2.0 functionality on all ports.

BIOS Setup allows for the disabling of USB ports individually or in groups. In order to secure the system against a physical attack, ports may be disabled even if there is nothing physically connected to them, such as the two front ports for the media card reader module when the module is not present.

### 2.3.8 Network Interface Controller

All models feature an Intel gigabit Network Interface Controller (NIC) integrated on the system board. The controller provides automatic selection of 10BASE-T, 100BASE-TX, or 1000BASE-T operation with a local area network and includes power-down, wake-up, Alert-On-LAN (AOL), Alert Standard Format (ASF), and AMT features. An RJ-45 connector with status LEDs is provided on the rear panel.

## 2.3.9 Graphics Subsystem

These systems use the Q45 GMCH component, which includes an integrated graphics controller that can drive both an external VGA monitor and a DisplayPort digital display. The controller implements Dynamic Video Memory Technology (DVMT 3.0) for video memory. Table 2-5 lists the key features of the integrated graphics subsystem.

**Table 2-5**  
**Integrated Graphics Subsystem Statistics**

| <b>Q45 GMCH<br/>Integrated Graphics Controller</b> |  |
|--|--|
| Recommended for                                    | Hi 2D, Entry 3D  |
| Bus Type   | Int. PCI Express   |
| Memory Amount                                      | 32 MB pre-allocated  |
| Memory Type  | DVMT 3.0   |
| DAC Speed  | 400 MHz  |
| Maximum 2D Resolution                              | 2048x1536 @ 85 Hz  |
| Hardware Acceleration                              | Quick Draw,<br>DirectX 9,<br>Direct Draw,<br>Direct Show,<br>Open GL 1.45,<br>MPEG 1-2,<br>Indeo |
| Outputs  | 1 VGA, 1 DisplayPort 1.1 [see text]  |

All systems include a legacy VGA connector and a DisplayPort connector and support dual monitor operation. The DisplayPort includes a multimode feature that allows a DVI or VGA adapter to be connected to the DisplayPort.

These systems also include two PCIe graphics slots (one x16, one x4/x16 connector) to ensure full graphics upgrade capabilities.

## 2.3.10 Audio Subsystem

These systems use the integrated High Definition audio controller of the chipset and the ADI AD1884A High Definition audio codec. HD audio provides enhanced audio performance with higher sampling rates, refined signal interfaces, and audio processors with increased signal-to-noise ratio. The audio line input jack can be re-configured as a microphone input, and multi-streaming is supported. These systems include a 1.5-watt output amplifier driving an internal speaker, which can be muted with the F10 BIOS control. All models include front panel-accessible stereo microphone input and headphone output audio jacks.

## 2.4 Specifications

This section includes the environmental, electrical, and physical specifications for the systems covered in this guide. Where provided, metric statistics are given in parenthesis. Specifications are subject to change without notice.

**Table 2-6  
Environmental Specifications (Factory Configuration)**

| Parameter               | Operating  | Non-operating   |
|-------------------------|--|---|
| Ambient Air Temperature | 50° to 95° F (10° to 35° C, max. rate of change ≤ 10°C/Hr) | -22° to 140° F (-30° to 60° C, max. rate of change ≤ 20°C/Hr) |
| Shock (w/o damage)      | 5 Gs [1]   | 20 Gs [1]   |
| Vibration               | 0.000215 G <sup>2</sup> /Hz, 10-300 Hz                     | 0.0005 G <sup>2</sup> /Hz, 10-500 Hz                          |
| Humidity                | 10-90% Rh @ 28° C max. wet bulb temperature                | 5-95% Rh @ 38.7° C max. wet bulb temperature                  |
| Maximum Altitude        | 10,000 ft (3048 m) [2]                                     | 30,000 ft (9144 m) [2]  |

NOTE:

- [1] Peak input acceleration during an 11 ms half-sine shock pulse.
- [2] Maximum rate of change: 1500 ft/min.

**Table 2-7  
Power Supply Electrical Specifications**

| Parameter   | Value       |
|---|-------------|
| Input Line Voltage:                                 |             |
| Nominal:  | 100–240 VAC |
| Maximum:  | 90–264 VAC  |
| Input Line Frequency Range:                         |             |
| Nominal:  | 50–60 Hz    |
| Maximum:  | 47–63 Hz    |
| Energy Star 4.0 with 80Plus Bronze-level compliancy |             |
| USDT  | Standard    |
| SFF & CMT   | Optional    |
| Maximum Continuous Power:                           |             |
| USDT  | 135 watts   |
| SFF   | 240 watts   |
| CMT   | 365 watts   |

NOTE:

Energy Star 4.0 with 80Plus Bronze-level compliancy option available for SFF and CMT form factors.

**Table 2-8  
Physical Specifications**

| <b>Parameter</b>                    | <b>USDT [2]</b>       | <b>SFF [2]</b>        | <b>CMT [3]</b>        |
|-------------------------------------|-----------------------|-----------------------|-----------------------|
| Height                              | 2.60 in<br>(6.60 cm)  | 3.95 in<br>(10.03 cm) | 17.63 in<br>(44.8 cm) |
| Width                               | 9.90 in<br>(25.15 cm) | 13.3 in<br>(33.78 cm) | 7.0 in<br>(16.8 cm)   |
| Depth                               | 10.0 in<br>(25.40 cm) | 14.9 in<br>(37.85 cm) | 17.8 in<br>(45.21 cm) |
| Weight [1]                          | 7.0 lb<br>(3.18 kg)   | 18.75 lb<br>(8.50 kg) | 26.2 lb<br>(11.89 kg) |
| Load-bearing ability of chassis [4] | 77.1 lb<br>(35 kg)    | 77.1 lb<br>(35 kg)    | 77.1 lb<br>(35 kg)    |

## NOTES:

- [1] System configured with 1 hard drive, 1 diskette drive (SFF and CMT only), and no PCI cards.
- [2] Desktop (horizontal) configuration.
- [3] Minitower configuration. For desktop configuration, swap Height and Width dimensions.
- [4] Applicable to unit in desktop orientation only and assumes reasonable type of load such as a monitor.

**Table 2-9  
Optical Drive Specifications**

| <b>Parameter</b>                     | <b>DVD-ROM</b>   | <b>CD-RW/DVD-ROM Combo</b>  | <b>HP SuperMulti LightScribe Combo</b>  |
|--------------------------------------|--|---|---|
| Interface Type                       | SATA [1]   | SATA [1]  | SATA [1]  |
| Max. read/write speeds by media type | DVD-RAM: 4x/na<br>DVD+RW: 8x/na<br>DVD-RW: 8x/na<br>DVD+R DL: 8x/na<br>DVD-R DL: 8x/na<br>DVD-ROM: 16x/na<br>DVD+R: 8x/na<br>DVD-R: 8x/na<br>CD-ROM: 48x/na<br>CD-RW: 32x/na<br>CD-R: 48x/na | DVD-RAM: 12x/12x<br>DVD+RW: 8x/8x<br>DVD-RW: 8x/6x<br>DVD+R DL: 8x/8x<br>DVD-R DL: 8x/8x<br>DVD-ROM: 16x/na<br>DVD-ROM DL: 8x/na<br>DVD+R: 16x/16x<br>DVD-R: 16x/16x<br>CD-ROM: 48x/na<br>CD-RW: 32x/32x<br>CD-R: 48x/48x | DVD-RAM: 12x/12x<br>DVD+RW: 8x/8x<br>DVD-RW: 8x/6x<br>DVD+R DL: 8x/8x<br>DVD-R DL: 8x/8x<br>DVD-ROM: 16x/na<br>DVD-ROM DL: 8x/na<br>DVD+R: 16x/16x<br>DVD-R: 16x/16x<br>CD-ROM: 48x/na<br>CD-RW: 32x/32x<br>CD-R: 48x/48x |
| Maximum Transfer Rate (Reads)        | DVD:, 21.6 KB/s;<br>CD: 7.2 KB/s   | DVD:, 21.6 KB/s;<br>CD: 7.2 KB/s  | DVD:, 21.6 KB/s;<br>CD: 7.2 KB/s  |
| Media Capacity (DVD)                 | DL: 8.5 GB, Std: 4.7 GB  | DL: 8.5 GB, Std: 4.7 GB   | DL: 8.5 GB, Std: 4.7 GB   |
| Average Access Time:                 |  |   |   |
| Random                               | DVD: <140 ms, CD: <125 ms  | DVD: <140 ms, CD: <125 ms   | DVD: <140 ms, CD: <125 ms   |
| Full Stroke                          | DVD: <250 ms, CD: <210 ms  | DVD: <250 ms, CD: <210 ms   | DVD: <250 ms, CD: <210 ms   |
| Media lable creation?                | No   | No  | Yes [2]   |

## NOTE

[1] USDT models use "slim" drive.

[2] Requires special label-etchable media.

**Table 2-10  
Hard Drive Specifications**

| <b>Parameter</b>                 | <b>80 GB</b>              | <b>160 GB</b>             | <b>250 GB [4]</b> |
|----------------------------------|---------------------------|---------------------------|-------------------|
| Drive Size                       | 2.5 & 3.5 in.[1]          | 2.5 & 3.5 in [1]          | 3.5 in            |
| Interface                        | SATA                      | SATA                      | SATA              |
| Transfer Rate                    | 1.5 & 3.0 Gb/s [2]        | 1.5 & 3.0 Gb/s [2]        | 3.0 Gb/s          |
| Drive Protection System Support? | Yes                       | Yes                       | Yes               |
| Typical Seek Time (w/settling)   |                           |                           |                   |
| Single Track                     | 0.8 ms                    | 0.8 ms                    | 1.0 ms            |
| Average                          | 9 ms                      | 9 ms                      | 11 ms             |
| Full Stroke                      | 17 ms                     | 17 ms                     | 18 ms             |
| Disk Format (logical blocks)     | 156,301,488               | 320,173,056               | 488,397,168       |
| Rotation Speed                   | 5400/7200/<br>10K RPM [3] | 5400/7200/<br>10K RPM [3] | 7200 RPM          |
| Drive Fault Prediction           | SMART IV                  | SMART IV                  | SMART IV          |

## NOTES:

[1] USDT supports 2.5-in. drives only.

[2] USDT supports 1.5 Gb/s drives only.

[3] USDT supports up to 7200-RPM drives only.

[4] Supported by SFF and CMT form factors only.

## Processor/Memory Subsystem

### 3.1 Introduction

This systems support the Intel Pentium and Core processor families and use the Q45 chipset (Figure 3-1). These systems support PC2-6400 and PC2-5300 DDR2 memory modules. This chapter describes the processor/memory subsystem.

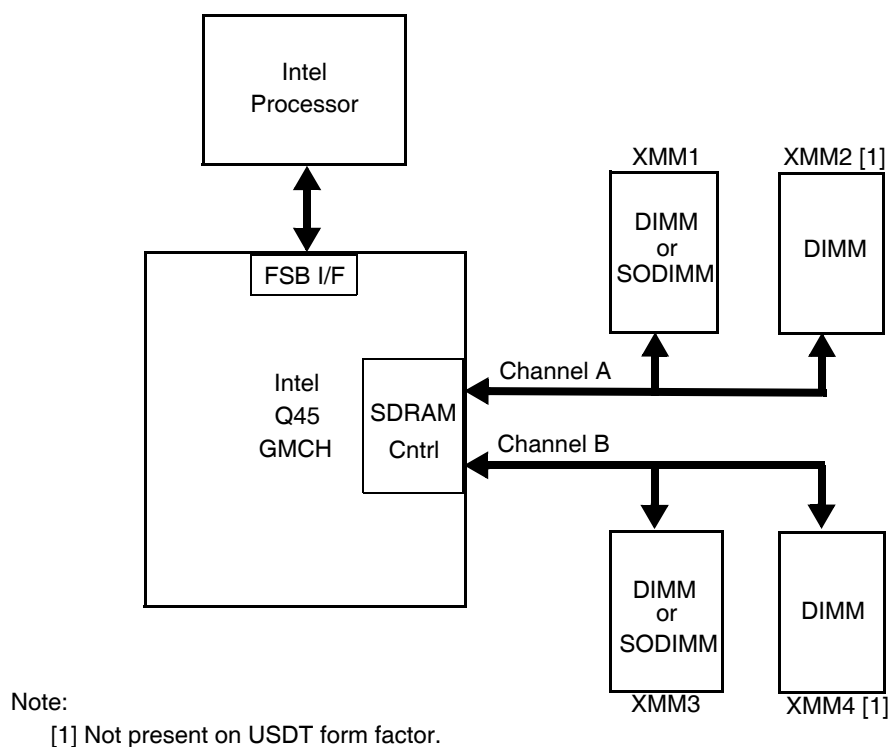


Figure 3-1. Processor/Memory Subsystem Architecture

This chapter includes the following topics:

- Intel processor (3.2)
- Memory subsystem (3.3)

## 3.2 Intel Processors

These systems each feature an Intel processor in a FC-LGA775 package mounted with a heat sink in a zero-insertion force socket. The mounting socket allows the processor to be easily changed for upgrading.

### 3.2.1 Intel Processor Overview

The models covered in this guide support Intel Celeron, Pentium, and Core 2 processors, including the latest Intel Core 2 Duo, and Core 2 Quad processors.

Key features of supported Intel processors include:

- Dual- or quad-core architecture—Provides full parallel processing.
- Execution Trace Cache— A new feature supporting the branch prediction mechanism, the trace cache stores translated sequences of branching micro-operations (ops) and is checked when suspected re-occurring branches are detected in the main processing loop. This feature allows instruction decoding to be removed from the main processing loop.
- Rapid Execution Engine—Arithmetic Logic Units (ALUs) run at twice (2x) processing frequency for higher throughput and reduced latency.
- Up to 12-MB of L2 cache—Using a 32-byte-wide interface at processing speed, the large L2 cache provides a substantial increase.
- Advanced dynamic execution—Using a larger (4K) branch target buffer and improved prediction algorithm, branch mis-predictions are significantly reduced
- Additional Streaming SIMD extensions (SSE2 and SSE3)—In addition to the SSE support provided by earlier processors, the latest processors include additional MMX instructions that enhance:
  - Streaming video/audio processing
  - Photo/video editing
  - Speech recognition
  - 3D processing
  - Encryption processing
- Quad-pumped Front Side Bus (FSB)—The FSB uses a 200-MHz clock for qualifying the buses' control signals. However, address information is transferred using a 2x strobe while data is transferred with a 4x strobe, providing a maximum data transfer rate that is four times that of earlier processors.

The Intel processor increases processing speed by using higher clock speeds with hyper-pipelined technology, therefore handling significantly more instructions at a time. The Arithmetic Logic Units (ALUs) of all processors listed above run at twice the core speed.



### 3.2.2 Processor Changing/Upgrading

All models use the LGA775 ZIF (Socket T) mounting socket. These systems require that the processor use an integrated heatsink/fan assembly. A replacement processor must use the same type heatsink/fan assembly as the original to ensure proper cooling. The heatsink and attachment clip are specially designed provide maximum heat transfer from the processor component.



**CAUTION:** Attachment of the heatsink to the processor is critical on these systems. Improper attachment of the heatsink will likely result in a thermal condition. Although the system is designed to detect thermal conditions and automatically shut down, such a condition could still result in damage to the processor component. Refer to the applicable Service Reference Guide for processor installation instructions.

Table 3-1 provides a sample listing of processors supported by these systems.

**Table 3-1**  
**Supported Processors (partial listing)**

| Intel Model | Core design | Features           | Clock Speed in GHz | FSB Speed in MHz | L2 Cache | Form Factor support |
|-------------|-------------|--------------------|--------------------|------------------|----------|---------------------|
| Q6700       | quad        | VT, [1]            | 2.66               | 1066             | 8 MB     | SFF, CMT            |
| Q6600       | quad        | VT, [1]            | 2.40               | 1066             | 8 MB     | SFF, CMT            |
| E6850       | dual        | vPro, VT, TXT, [1] | 3.00               | 1333             | 4 MB     | all                 |
| E6750       | dual        | vPro, VT, TXT, [1] | 2.66               | 1333             | 4 MB     | all                 |
| E6550       | dual        | vPro, VT, TXT, [1] | 2.33               | 1333             | 4 MB     | all                 |
| E4500       | dual        | [1]                | 2.20               | 800              | 2 MB     | all                 |
| E4400       | dual        | [1]                | 2.00               | 800              | 2 MB     | all                 |
| E2180       | dual        | [1]                | 2.00               | 800              | 1 MB     | all                 |
| E2160       | dual        | [1]                | 1.80               | 800              | 1 MB     | all                 |
| 440         | single      | [1]                | 2.00               | 800              | 512 KB   | all                 |

NOTE:

[1] Standard Intel feature set including EM64T, XD, and EIST support. Refer to [www.intel.com](http://www.intel.com) for detailed information.



**CAUTION:** The USDT form factor can support a processor with a maximum power consumption of 65 watts. The SFF and CMT form factors can support a processor with a maximum power consumption of 95 watts. Exceeding these limits can result in system damage and lost data.

### 3.3 Memory Subsystem

All models support non-ECC PC2-5300 and PC2-6400 DDR2 memory. The USDT form factor supports up to eight gigabytes of memory while the SFF and CMT form factors support up to 16 gigabytes of memory.



The DDR SDRAM “PCxxxx” reference designates bus bandwidth (i.e., a PC2-5300 module can, operating at a 667-MHz effective speed, provide a throughput of 5300 MBps (8 bytes × 667MHz)). Memory speed types may be mixed within a system, although the system BIOS will set the memory controller to work at speed of the slowest memory module.

The USDT system board provides two SODIMM sockets and the SFF and CMT system boards provide four DIMM sockets

- XMM1, channel A (black)
- XMM2, channel A (white, not present in USDT form factor)
- XMM3, channel B (white)
- XMM4, channel B (white, not present in USDT form factor)

Memory modules do not need to be installed in pairs although installation of pairs (especially matched sets) provides the best performance. The XMM1 socket must be populated for proper support of Intel Active Management Technology (AMT). The BIOS will detect the module population and set the system accordingly as follows:

- Single-channel mode - memory installed for one channel only
- Dual-channel asymmetric mode - memory installed for both channels but of unequal channel capacities.
- Dual-channel interleaved mode (recommended) - memory installed for both channels and offering equal channel capacities, providing the highest performance.

These systems support memory modules with the following parameters:

- Unbuffered, compatible with SPD rev. 1.0
- 512-Mb, and 1-Gb memory technologies for x8 and x16 devices
- CAS latency (CL) of 5 or 6 (depending on memory speed)
- Single or double-sided
- Non-ECC memory only

The SPD format supported by these systems complies with the JEDEC specification for 128-byte EEPROMs. This system also provides support for 256-byte EEPROMs to include additional HP-added features such as part number and serial number.


If BIOS detects an unsupported memory module, a “**memory incompatible**” message will be displayed and the system will halt. **These systems are shipped with non-ECC modules only.**

An installed mix of memory module types is acceptable but operation will be constrained to the level of the module with the lowest (slowest) performance.

If an incompatible memory module is detected the NUM LOCK will blink for a short period of time during POST and an error message may or may not be displayed before the system hangs.

### 3.3.1 Memory Upgrading

Table 3-2 shows suggested memory configurations for these systems. Note that the USDT form factor provides only two memory sockets.

 Table 3-2 does not list all possible configurations.

**Table 3-2.  
Memory Socket Loading [1]**

| Channel A |              | Channel B |              | Total        |
|-----------|--------------|-----------|--------------|--------------|
| Socket 1  | Socket 2 [2] | Socket 3  | Socket 4 [2] |              |
| 512 MB    | none         | none      | none         | 512-MB       |
| 512 MB    | none         | 512 MB    | none         | 1-GB [3]     |
| 1-GB      | none         | none      | none         | 1-GB         |
| 1 GB      | none         | 1 GB      | none         | 2 GB [3]     |
| 1 GB      | 1 GB         | 1 GB      | 1 GB         | 4-GB [3]     |
| 2 GB      | none         | 2 GB      | none         | 4-GB [3]     |
| 4 GB      | 4 GB         | 4 GB      | 4 GB         | 16-GB [3, 4] |

NOTE:

[1] USDT form factor uses SODIMM sockets. SFF and CMT form factors use DIMM sockets.

[2] Not present on USDT form factor.

[3] Dual-channel symmetrical

[4] Only SFF and CMT support this size memory

HP recommends using symmetrical loading (same-capacity, same-speed modules across both channels) to achieve the best performance.



**CAUTION:** Always power down the system and disconnect the power cord from the AC outlet before adding or replacing memory modules. Changing memory modules while the unit is plugged into an active AC outlet could result in equipment damage.



Memory amounts over 3 GB may not be fully accessible with 32-bit operating systems due to system resource requirements. Addressing memory above 4 GB requires a 64-bit operating system.

### 3.3.2 Memory Mapping and Pre-allocation

Figure 3-2 shows the system memory map. The Q45 Express chipset includes a Management Engine that pre-allocates a portion of system memory (16 MB for one module, 32 MB for two modules) for management functions. In addition, the internal graphics controller pre-allocates a portion of system memory for video use (refer to chapter 6). Pre-allocated memory is not available to the operating system. The amount of system memory reported by the OS will be the total amount installed less the pre-allocated amount.

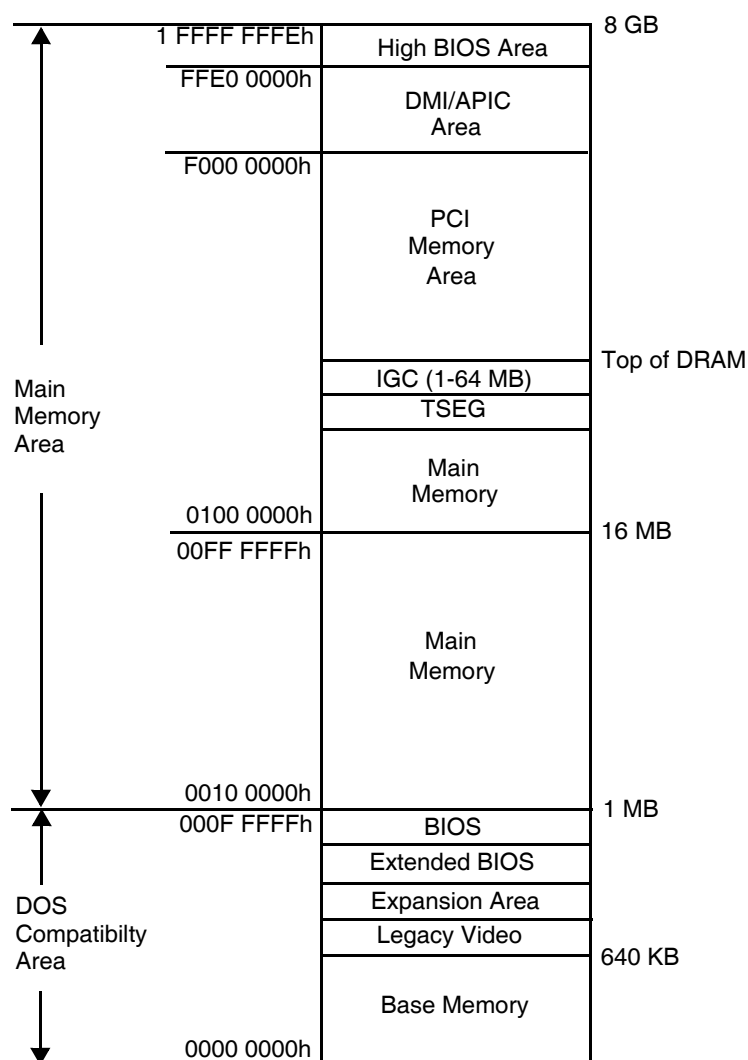


Figure 3-2. System Memory Map (for maximum of 8 gigabytes)



All locations in memory are cacheable. Base memory is always mapped to DRAM. The next 128 KB fixed memory area can, through the north bridge, be mapped to DRAM or to PCI space. Graphics RAM area is mapped to PCI locations.

## 4.1 Introduction

This chapter covers subjects dealing ICH10 with basic system architecture and covers the following topics:

- PCI bus overview (4.2)
- System resources (4.3)
- Real-time clock and configuration memory (4.4)
- System management (4.5)
- Register map and miscellaneous functions (4.6)

This chapter covers functions provided by off-the-shelf chipsets and therefore describes only basic aspects of these functions as well as information unique to the systems covered in this guide. For detailed information on specific components, refer to the applicable manufacturer's documentation.

## 4.2 PCI Bus Overview



This section describes the PCI bus in general and highlights bus implementation for systems covered in this guide. For detailed information regarding PCI bus operation, refer to the appropriate PCI specification or the PCI web site: [www.pcisig.com](http://www.pcisig.com).

These systems implement the following types of PCI buses:

- PCI 2.3 - Legacy parallel interface operating at 33-MHz
- PCI Express - High-performance interface capable of using multiple TX/RX high-speed lanes of serial data streams

### 4.2.1 PCI 2.3 Bus Operation

The PCI 2.3 bus consists of a 32-bit path (AD31-00 lines) that uses a multiplexed scheme for handling both address and data transfers. A bus transaction consists of an address cycle and one or more data cycles, with each cycle requiring a clock (PCICLK) cycle. High performance is achieved during burst modes in which a transaction with contiguous memory locations requires that only one address cycle be conducted and subsequent data cycles are completed using auto-incremented addressing.

Devices on the PCI bus must comply with PCI protocol that allows configuration of that device by software. In this system, configuration mechanism #1 (as described in the PCI Local Bus specification Rev. 2.3) is employed.

Table 4-1 shows the standard configuration of device numbers and IDSEL connections for components and slots residing on a PCI 2.3 bus.

**Table 4-1  
PCI Component Configuration Access**

| PCI Component                 | Notes | Function # | Device # | PCI Bus # | IDSEL Wired to: |
|-------------------------------|-------|------------|----------|-----------|-----------------|
| Q45 GMCH:                     |       |            |          |           |                 |
| Host/DMI Bridge               |       | 0          | 28       | 0         | --              |
| Host/PCI Expr. Bridge         |       | 0          | 1        | 0         |                 |
| Integrated Graphics Cntrl.    |       | 0          | 2        | 0         |                 |
| PCI Express x16 graphics slot |       |            |          |           |                 |
|                               |       | 0          | 0        | 1         | --              |
| 82801 ICH10                   |       |            |          |           |                 |
| PCI Bridge                    |       | 0          | 30       | 0         |                 |
| LPC Bridge                    |       | 0          | 31       | 0         |                 |
| SATA Controller #1            |       | 2          | 31       | 0         |                 |
| SMBus Controller              |       | 3          | 31       | 0         |                 |
| SATA/eSATA Controller #2      | [5]   | 5          | 31       | 0         |                 |
| Thermal System                |       | 6          | 31       | 0         |                 |
| USB 1.1 Controller #1         |       | 0          | 29       | 0         |                 |
| USB 1.1 Controller #2         |       | 1          | 29       | 0         |                 |
| USB 1.1 Controller #3         |       | 2          | 29       | 0         |                 |
| USB 1.1 Controller #4         |       | 0          | 26       | 0         |                 |
| USB 1.1 Controller #5         |       | 1          | 26       | 0         |                 |
| USB 1.1 Controller #6         |       | 3 [2]      | 29 [2]   |           |                 |
| USB 2.0 Controller #1         |       | 7          | 29       | 0         |                 |
| USB 2.0 Controller #2         |       | 7          | 26       | 0         |                 |
| GbE NIC                       |       | 0          | 25       | 0         |                 |
| Intel HD audio controller     |       | 0          | 27       | 0         |                 |
| PCIe port 1                   | [3]   | 0          | 28       | 0         |                 |
| PCIe port 2                   | [1]   | 1          | 28       | 0         |                 |
| PCIe port 3                   | [1]   | 2          | 28       | 0         |                 |
| PCIe port 4                   | [1]   | 3          | 28       | 0         |                 |
| PCIe port 5                   |       | 4          | 28       | 0         |                 |
| PCIe port 6                   |       | 5          | 28       | 0         |                 |
| PCI 2.3 slot 1                | [3]   | 0          | 4        | 7         | AD20            |
| PCI 2.3 slot 2                | [3]   | 0          | 11       | 7         | AD25            |
| PCI 2.3 slot 3                | [4]   | 0          | 10       | 7         | AD27            |
| PCIe x1 slot 1                | [3]   | 0          | 0        | 32        |                 |
| PCIe x1 slot 2                | [3]   | 0          | 0        | 48        |                 |

## NOTES:

[1] Function not used in these systems.

[2] USB 1.1 controllers in 6+6 configuration. 8+4 configuration will have USB 1.1 controller #6 use Function 26, Device 2.

[3] SFF and CMT form factors only.

[4] CMT form factor only

[5] Function is only visible in IDE mode (not visible in AHCI or RAID SATA emulation mode).

The PCI bus supports a bus master/target arbitration scheme. A bus master is a device that has been granted control of the bus for the purpose of initiating a transaction. A target is a device that is the recipient of a transaction. The Request (REQ), Grant (GNT), and FRAME signals are used by PCI bus masters for gaining access to the PCI bus. When a PCI device needs access to the PCI bus (and does not already own it), the PCI device asserts its REQ<sub>n</sub> signal to the PCI bus arbiter (a function of the system controller component). If the bus is available, the arbiter asserts the GNT<sub>n</sub> signal to the requesting device, which then asserts FRAME and conducts the address phase of the transaction with a target. If the PCI device already owns the bus, a request is not needed and the device can simply assert FRAME and conduct the transaction. Table 4-2 shows the grant and request signals assignments for the devices on the PCI bus.

**Table 4-2.  
PCI Bus Mastering Devices**

| Device               | REQ/GNT Line | Note |
|----------------------|--------------|------|
| PCI Connector Slot 1 | REQ0/GNT0    | [1]  |
| PCI Connector Slot 2 | REQ1/GNT1    | [1]  |
| PCI Connector Slot 3 | REQ2/GNT2    | [2]  |

NOTE:

[1] SFF and CMT form factors only.

[2] CMT form factor only

PCI bus arbitration is based on a round-robin scheme that complies with the fairness algorithm specified by the PCI specification. The bus parking policy allows for the current PCI bus owner (excepting the PCI/ISA bridge) to maintain ownership of the bus as long as no request is asserted by another agent. Note that most CPU-to-DRAM accesses can occur concurrently with PCI traffic, therefore reducing the need for the Host/PCI bridge to compete for PCI bus ownership.

## 4.2.2 PCI Express Bus Operation

The PCI Express (PCIe) v1.1 bus is a high-performance extension of the legacy PCI bus specification. The PCI Express bus uses the following layers:

- Software/driver layer
- Transaction protocol layer
- Link layer
- Physical layer

### Software/Driver Layer

The PCI Express bus maintains software compatibility with PCI 2.3 and earlier versions so that there is no impact on existing operating systems and drivers. During system initialization, the PCI Express bus uses the same methods of device discovery and resource allocation that legacy PCI-based operating systems and drivers are designed to use.

### Transaction Protocol Layer

The transaction protocol layer processes read and write requests from the software/driver layer and generates request packets for the link layer. Each packet includes an identifier allowing any required response packets to be directed to the originator.

## Link Layer

The link layer provides data integrity by adding a sequence information prefix and a CRC suffix to the packet created by the transaction layer. Flow-control methods ensure that a packet will only be transferred if the receiving device is ready to accommodate it. A corrupted packet will be automatically re-sent.

## Physical Layer

The PCI Express bus uses a point-to-point, high-speed TX/RX serial lane topology. One or more full-duplex lanes transfer data serially, and the design allows for scalability depending on end-point capabilities. Each lane consists of two differential pairs of signal paths; one for transmit, one for receive (Figure 4-1).

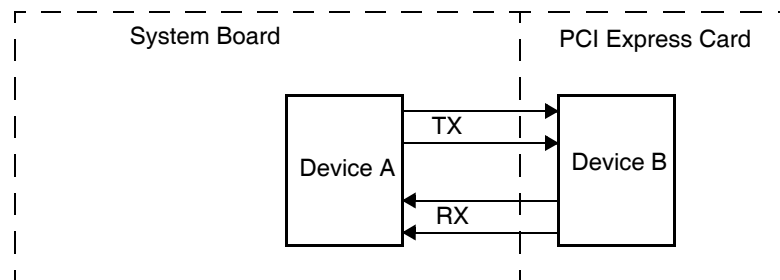


Figure 4-1. PCI Express Bus Lane

Each byte is transferred using 8b/10b encoding, which embeds the clock signal with the data. Operating at a 2.5 Gigabit transfer rate, a single lane can provide a data flow of 200 MBps. The bandwidth is increased if additional lanes are available for use. During the initialization process, two PCI Express devices will negotiate for the number of lanes available and the speed the link can operate at. In a x1 (single lane) interface, all data bytes are transferred serially over the lane. In a multi-lane interface, data bytes are distributed across the lanes using a multiplex scheme.

### 4.2.3 Option ROM Mapping

During POST, the PCI bus is scanned for devices that contain their own specific firmware in ROM. Such option ROM data, if detected, is loaded into system memory's DOS compatibility area (refer to the system memory map shown in chapter 3).

### 4.2.4 PCI Interrupts

Eight interrupt signals (INTA- thru INTH-) are available for use by PCI devices. These signals may be generated by on-board PCI devices or by devices installed in the PCI slots. For more information on interrupts including PCI interrupt mapping refer to the "System Resources" section 4.3.

### 4.2.5 PCI Power Management Support

This system complies with the PCI Power Management Interface Specification (rev 1.0). The PCI Power Management Enable (PME-) signal is supported by the chipset and allows compliant PCI peripherals to initiate the power management routine.



## 4.2.6 PCI Connectors

### PCI 2.3 Connector

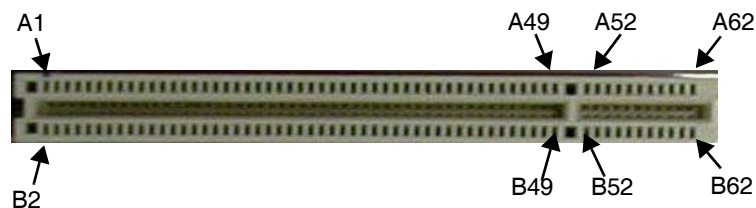


Figure 4-2. 32-bit, 5.0-volt PCI 2.3 Bus Connector

**Table 4-3.**  
**PCI 2.3 Bus Connector Pinout**

| Pin | B Signal | A Signal | Pin | B Signal | A Signal           | Pin | B Signal | A Signal |
|-----|----------|----------|-----|----------|--------------------|-----|----------|----------|
| 01  | -12 VDC  | TRST-    | 22  | GND      | AD28               | 43  | +3.3 VDC | PAR      |
| 02  | TCK      | +12 VDC  | 23  | AD27     | AD26               | 44  | C/BE1-   | AD15     |
| 03  | GND      | TMS      | 24  | AD25     | GND                | 45  | AD14     | +3.3 VDC |
| 04  | TDO      | TDI      | 25  | +3.3 VDC | AD24               | 46  | GND      | AD13     |
| 05  | +5 VDC   | +5 VDC   | 26  | C/BE3-   | IDSEL              | 47  | AD12     | AD11     |
| 06  | +5 VDC   | INTA-    | 27  | AD23     | +3.3 VDC           | 48  | AD10     | GND      |
| 07  | INTB-    | INTC-    | 28  | GND      | AD22               | 49  | GND      | AD09     |
| 08  | INTD-    | +5 VDC   | 29  | AD21     | AD20               | 50  | Key      | Key      |
| 09  | PRSENT1- | Reserved | 30  | AD19     | GND                | 51  | Key      | Key      |
| 10  | RSVD     | +5 VDC   | 31  | +3.3 VDC | AD18               | 52  | AD08     | C/BE0-   |
| 11  | PRSENT2- | Reserved | 32  | AD17     | AD16               | 53  | AD07     | +3.3 VDC |
| 12  | GND      | GND      | 33  | C/BE2-   | +3.3 VDC           | 54  | +3.3 VDC | AD06     |
| 13  | GND      | GND      | 34  | GND      | FRAME-             | 55  | AD05     | AD04     |
| 14  | RSVD     | +3.3 AUX | 35  | IRDY-    | GND                | 56  | AD03     | GND      |
| 15  | GND      | RST-     | 36  | +3.3 VDC | TRDY-              | 57  | GND      | AD02     |
| 16  | CLK      | +5 VDC   | 37  | DEVSEL-  | GND                | 58  | AD01     | AD00     |
| 17  | GND      | GNT-     | 38  | GND      | STOP-              | 59  | +5 VDC   | +5 VDC   |
| 18  | REQ-     | GND      | 39  | LOCK-    | +3.3 VDC           | 60  | ACK64-   | REQ64-   |
| 19  | +5 VDC   | PME-     | 40  | PERR-    | SDONE <sub>n</sub> | 61  | +5 VDC   | +5 VDC   |
| 20  | AD31     | AD30     | 41  | +3.3 VDC | SBO-               | 62  | +5 VDC   | +5 VDC   |
| 21  | AD29     | +3.3 VDC | 42  | SERR-    | GND                |     |          |          |

## PCI Express Connectors

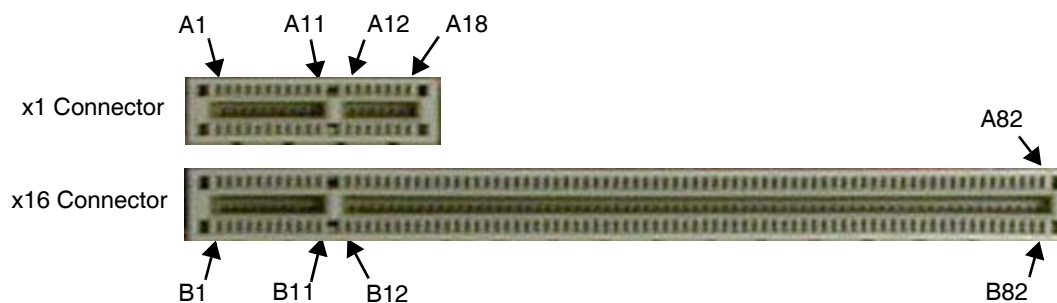


Figure 4-3. PCI Express Bus Connectors

**Table 4-4.**  
**PCI Express Bus Connector Pinout**

| Pin | B Signal             | A Signal | Pin | B Signal | A Signal | Pin | B Signal | A Signal |
|-----|----------------------|----------|-----|----------|----------|-----|----------|----------|
| 01  | +12 VDC              | PRSNT1#  | 29  | GND      | PERp3    | 57  | GND      | PERn9    |
| 02  | +12 VDC              | +12 VDC  | 30  | RSVD     | PERn3    | 58  | PETp10   | GND      |
| 03  | RSVD                 | +12 VDC  | 31  | PRSNT2#  | GND      | 59  | PETn10   | GND      |
| 04  | GND                  | GND      | 32  | GND      | RSVD     | 60  | GND      | PERp10   |
| 05  | SMCLK                | +5 VDC   | 33  | PETp4    | RSVD     | 61  | GND      | PERn10   |
| 06  | +5 VDC               | JTAG2    | 34  | PETn4    | GND      | 62  | PETp11   | GND      |
| 07  | GND                  | JTAG4    | 35  | GND      | PERp4    | 63  | PETn11   | GND      |
| 08  | +3.3 VDC             | JTAG5    | 36  | GND      | PERn4    | 64  | GND      | PERp11   |
| 09  | JTAG1                | +3.3 VDC | 37  | PETp5    | GND      | 65  | GND      | PERn11   |
| 10  | 3.3 V <sub>aux</sub> | +3.3 VDC | 38  | PETn5    | GND      | 66  | PETp12   | GND      |
| 11  | WAKE                 | PERST#   | 39  | GND      | PERp5    | 67  | PETn12   | GND      |
| 12  | RSVD                 | GND      | 40  | GND      | PERn5    | 68  | GND      | PERp12   |
| 13  | GND                  | REFCLK+  | 41  | PETp6    | GND      | 69  | GND      | PERn12   |
| 14  | PETp0                | REFCLK-  | 42  | PETn6    | GND      | 70  | PETp13   | GND      |
| 15  | PETn0                | GND      | 43  | GND      | PERp6    | 71  | PETn13   | GND      |
| 16  | GND                  | PERp0    | 44  | GND      | PERn6    | 72  | GND      | PERp13   |
| 17  | PRSNT2#              | PERn0    | 45  | PETp7    | GND      | 73  | GND      | PERn13   |
| 18  | GND                  | GND      | 46  | PETn7    | GND      | 74  | PETp14   | GND      |
| 19  | PETp1                | RSVD     | 47  | GND      | PERp7    | 75  | PETn14   | GND      |
| 20  | PETn1                | GND      | 48  | PRSNT2#  | PERn7    | 76  | GND      | PERp14   |
| 21  | GND                  | PERp1    | 49  | GND      | GND      | 77  | GND      | PERn14   |
| 22  | GND                  | PERn1    | 50  | PETp8    | RSVD     | 78  | PETp15   | GND      |
| 23  | PETp2                | GND      | 51  | PETn8    | GND      | 79  | PETn15   | GND      |
| 24  | PETn2                | GND      | 52  | GND      | PERp8    | 80  | GND      | PERp15   |
| 25  | GND                  | PERp2    | 53  | GND      | PERn8    | 81  | PRSNT2#  | PERn15   |
| 26  | GND                  | PERn2    | 54  | PETp9    | GND      | 82  | RSVD     | GND      |
| 27  | PETp3                | GND      | 55  | PETn9    | GND      |     |          |          |
| 28  | PETn3                | GND      | 56  | GND      | PERp9    |     |          |          |

## 4.3 System Resources

This section describes the availability and basic control of major subsystems, otherwise known as resource allocation or simply “system resources.” System resources are provided on a priority basis through hardware interrupts and DMA requests and grants.

### 4.3.1 Interrupts

The microprocessor uses two types of hardware interrupts; maskable and nonmaskable. A maskable interrupt can be enabled or disabled within the microprocessor by the use of the STI and CLI instructions. A nonmaskable interrupt cannot be masked off within the microprocessor, but may be inhibited by legacy hardware or software means external to the microprocessor.

The maskable interrupt is a hardware-generated signal used by peripheral functions within the system to get the attention of the microprocessor. Peripheral functions produce a unique INTA-H (PCI) or IRQ0-15 (ISA) signal that is routed to interrupt processing logic that asserts the interrupt (INTR-) input to the microprocessor. The microprocessor halts execution to determine the source of the interrupt and then services the peripheral as appropriate.

Most IRQs are routed through the I/O controller of the super I/O component, which provides the serializing function. A serialized interrupt stream is then routed to the ICH component.

Interrupts may be processed in one of two modes (selectable through the F10 Setup utility):

- 8259 mode
- APIC mode

These modes are described in the following subsections.

#### 8259 Mode

The 8259 mode handles interrupts IRQ0-IRQ15 in the legacy (AT-system) method using 8259-equivalent logic. If more than one interrupt is pending, the highest priority (lowest number) is processed first.

#### APIC Mode

The Advanced Programmable Interrupt Controller (APIC) mode provides enhanced interrupt processing with the following advantages:

- Eliminates the processor's interrupt acknowledge cycle by using a separate (APIC) bus
- Programmable interrupt priority
- Additional interrupts (total of 24)

The APIC mode accommodates eight PCI interrupt signals (PIRQA-..PIRQH-) for use by PCI devices. The PCI interrupts are evenly distributed to minimize latency and wired as shown in Table 4-5.

**Table 4-5.  
PCI Interrupt Distribution**

| System Board Connector | System Interrupts |        |        |        |        |        |        |        |
|------------------------|-------------------|--------|--------|--------|--------|--------|--------|--------|
|                        | PIRQ A            | PIRQ B | PIRQ C | PIRQ D | PIRQ E | PIRQ F | PIRQ G | PIRQ H |
| PCI slot 1 (J20) [1]   |                   |        |        |        | A      | B      | C      | D      |
| PCI slot 2 (J21) [1]   |                   |        |        |        | D      | A      | B      | C      |
| PCI slot 3 (J22) [2]   |                   |        |        |        | C      | D      | A      | B      |

## NOTES:

[1] SFF and CMT only

[2] CMT only

The PCI interrupts can be configured by PCI Configuration Registers 60h..63h to share the standard ISA interrupts (IRQn).



The APIC mode is supported by Windows NT, Windows 2000, and Windows XP, and Windows Vista operating systems. Systems running the Windows 95 or 98 operating system will need to run in 8259 mode.

### 4.3.2 Direct Memory Access

Direct Memory Access (DMA) is a method by which a device accesses system memory without involving the microprocessor. Although the DMA method has been traditionally used to transfer blocks of data to or from an ISA I/O device, PCI devices may also use DMA operation as well. The DMA method reduces the amount of CPU interactions with memory, freeing the CPU for other processing tasks. For detailed information regarding DMA operation, refer to the data manual for the Intel 82801 ICH10 I/O Controller Hub.

## 4.4 Real-Time Clock and Configuration Memory

The Real-time clock (RTC) and configuration memory (also referred to as “CMOS”) functions are provided by the 82801 component and is MC146818-compatible. As shown in the following figure, the 82801 ICH10 component provides 256 bytes of battery-backed RAM divided into two 128-byte configuration memory areas. The RTC uses the first 14 bytes (00-0Dh) of the standard memory area. All locations of the standard memory area (00-7Fh) can be directly accessed using conventional OUT and IN assembly language instructions through I/O ports 70h/71h, although the suggested method is to use the INT15 AX=E823h BIOS call.

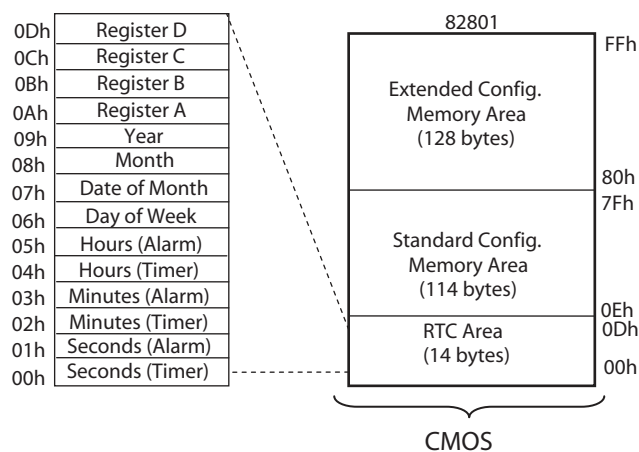


Figure 4.4. Configuration Memory Map

A lithium 3-VDC battery is used for maintaining the RTC and configuration memory while the system is powered down. During system operation a wire-Or-ed circuit allows the RTC and configuration memory to draw power from the power supply. The battery is located in a battery holder on the system board and has a life expectancy of three or more years. When the battery has expired it is replaced with a CR2032 or equivalent 3-VDC lithium battery.

### 4.4.1 Clearing CMOS

The contents of configuration memory (including the Power-On Password) can be cleared by the following procedure:

1. Turn off the unit.
2. Disconnect the AC power cord from the outlet and/or system unit.
3. Remove the chassis hood (cover) and insure that no LEDs on the system board are illuminated.
4. On the system board, press and hold the CMOS clear button (switch SW50, colored yellow) for at least 5 seconds.
5. Replace the chassis hood (cover).
6. Reconnect the AC power cord to the outlet and/or system unit.
7. Turn the unit on.

To clear only the Power-On Password refer to section 4.5.1.

## 4.4.2 Standard CMOS Locations

Table 4-6 describes standard configuration memory locations 0Ah-3Fh. These locations are accessible through using OUT/IN assembly language instructions using port 70/71h or BIOS function INT15, AX=E823h.

**Table 4-6.**  
**Configuration Memory (CMOS) Map**

| Location | Function                           | Location | Function                           |
|----------|------------------------------------|----------|------------------------------------|
| 00-0Dh   | Real-time clock                    | 24h      | System board ID                    |
| 0Eh      | Diagnostic status                  | 25h      | System architecture data           |
| 0Fh      | System reset code                  | 26h      | Auxiliary peripheral configuration |
| 10h      | Diskette drive type                | 27h      | Speed control external drive       |
| 11h      | Reserved                           | 28h      | Expanded/base mem. size, IRQ12     |
| 12h      | Hard drive type                    | 29h      | Miscellaneous configuration        |
| 13h      | Security functions                 | 2Ah      | Hard drive timeout                 |
| 14h      | Equipment installed                | 2Bh      | System inactivity timeout          |
| 15h      | Base memory size, low byte/KB      | 2Ch      | Monitor timeout, Num Lock Cntrl    |
| 16h      | Base memory size, high byte/KB     | 2Dh      | Additional flags                   |
| 17h      | Extended memory, low byte/KB       | 2Eh-2Fh  | Checksum of locations 10h-2Dh      |
| 18h      | Extended memory, high byte/KB      | 30h-31h  | Total extended memory tested       |
| 19h      | Hard drive 1, primary controller   | 32h      | Century                            |
| 1Ah      | Hard drive 2, primary controller   | 33h      | Miscellaneous flags set by BIOS    |
| 1Bh      | Hard drive 1, secondary controller | 34h      | International language             |
| 1Ch      | Hard drive 2, secondary controller | 35h      | APM status flags                   |
| 1Dh      | Enhanced hard drive support        | 36h      | ECC POST test single bit           |
| 1Eh      | Reserved                           | 37h-3Fh  | Power-on password                  |
| 1Fh      | Power management functions         | 40-FFh   | Feature Control/Status             |

NOTES:

Assume unmarked gaps are reserved.

Higher locations (>3Fh) contain information that should be accessed using the INT15, AX=E845h BIOS function (refer to Chapter 8 for BIOS function descriptions).

## 4.5 System Management

This section describes functions having to do with security, power management, temperature, and overall status. These functions are handled by hardware and firmware (BIOS) and generally configured through the Setup utility.

### 4.5.1 Security Functions

These systems include various features that provide different levels of security. Note that this subsection describes only the hardware functionality (including that supported by Setup) and does not describe security features that may be provided by the operating system and application software.

## Power-On / Setup Password

These systems include a power-on and setup passwords, which may be enabled or disabled (cleared) through a jumper on the system board. The jumper controls a GPIO input to the 82801 ICH10 that is checked during POST. The password is stored in configuration memory (CMOS) and if enabled and then forgotten by the user will require that either the password be cleared (preferable solution and described below) or the entire CMOS be cleared (refer to section 4.4.1).

To clear the password, use the following procedure:

1. Turn off the system and disconnect the AC power cord from the outlet and/or system unit.
2. Remove the cover (hood) as described in the appropriate User Guide or Maintenance And Service Reference Guide. Insure that all system board LEDs are off (not illuminated).
3. Locate the password clear jumper (header is colored green and labeled E49 on these systems) and move the jumper from pins 1 and 2 and place on (just) pin 2 (for safekeeping).
4. Replace the cover.
5. Re-connect the AC power cord to the AC outlet and/or system unit.
6. Turn on the system. The POST routine will clear and disable the password.
7. To re-enable the password feature, repeat steps 1-6, replacing the jumper on pins 1 and 2 of header E49.

## Setup Password

The Setup utility may be configured to be always changeable or changeable only by entering a password. Refer to the previous procedure (Power On / Setup Password) for clearing the Setup password.

## Cable Lock Provision

These systems include a chassis cutout (on the rear panel) for the attachment of a cable lock mechanism.

## I/O Interface Security

The SATA, serial, parallel, USB, and diskette interfaces may be disabled individually through the Setup utility to guard against unauthorized access to a system. In addition, the ability to write to or boot from a removable media drive (such as the diskette drive) may be enabled through the Setup utility. The disabling of the serial, parallel, and diskette interfaces are a function of the SIO controller. The USB ports are controlled through the 82801.

## Chassis Security

Some systems feature Smart Cover (hood) Sensor and Smart Cover (hood) Lock mechanisms to inhibit unauthorized tampering of the system unit.

## Smart Cover Sensor

These systems include a plunger switch that, when the cover (hood) is removed, closes and grounds an input of the 82801 component. The battery-backed logic will record this “intrusion” event by setting a specific bit. This bit will remain set (even if the cover is replaced) until the system is powered up and the user completes the boot sequence successfully, at which time the bit will be cleared. Through Setup, the user can set this function to be used by Alert-On-LAN and or one of three levels of support for a “cover removed” condition:

**Level 0**—Cover removal indication is essentially disabled at this level. During POST, status bit is cleared and no other action is taken by BIOS.

**Level 1**—During POST the message “The computer's cover has been removed since the last system start up” is displayed and time stamp in CMOS is updated.

**Level 2**—During POST the “The computer's cover has been removed since the last system start up” message is displayed, time stamp in CMOS is updated, and the user is prompted for the administrator password. (A Setup password must be enabled in order to see this option).

### Smart Cover Lock (Optional)

The SFF and CMT systems support an optional solenoid-operated locking bar that, when activated, prevents the cover (hood) from being removed. The GPIO ports 44 and 45 of the SIO controller provide the lock and unlock signals to the solenoid. A locked hood may be bypassed by removing special screws that hold the locking mechanism in place. The special screws are removed with the Smart Cover Lock Failsafe Key.

## 4.5.2 Power Management

These systems provide baseline hardware support of ACPI- and APM-compliant firmware and software. Key power-consuming components (processor, chipset, I/O controller, and fan) can be placed into a reduced power mode either automatically or by user control. The system can then be brought back up (“wake-up”) by events defined by the ACPI 2.0 specification. The ACPI wake-up events supported by this system are listed as follows:

**Table 4-7.**  
**ACPI Wake-Up Events**

| ACPI Wake-Up Event  | System Wakes From   |
|---------------------|---------------------|
| Power Button        | Suspend or soft-off |
| RTC Alarm           | Suspend or soft-off |
| Wake On LAN (w/NIC) | Suspend or soft-off |
| PME                 | Suspend or soft-off |
| Serial Port Ring    | Suspend or soft-off |
| USB                 | Suspend only        |
| Keyboard            | Suspend only        |
| Mouse               | Suspend only        |



### 4.5.3 System Status

These systems provide a visual indication of system boot, ROM flash, and operational status through the power LED and internal speaker, as described in Table 4-8.

**Table 4-8.**  
**System Operational Status LED Indications**

| System Status                            | PowerLED                       | Beeps [2] | Action Required                        |
|--|--------------------------------|-----------|--|
| S0: System on (normal operation)         | Steady green                   | None      | None                                   |
| S1: Suspend                              | Blinks green @ .5 Hz           | None      | None                                   |
| S3: Suspend to RAM                       | Blinks green @ .5 Hz           | None      | None                                   |
| S4: Suspend to disk                      | Off – clear                    | None      | None                                   |
| S5: Soft off                             | Off – clear                    | None      | None                                   |
| Processor thermal shutdown               | Blinks red 2 times @ 1 Hz [1]  | 2         | Check air flow, fans, heatsink         |
| Processor not seated / installed         | Blinks red 3 times @ 1 Hz [1]  | 3         | Check processor presence/seating       |
| Power supply overload failure            | Blinks red 4 times @ 1 Hz [1]  | 4         | Check system board problem [3],        |
| Memory error (pre-video)                 | Blinks red 5 times @ 1 Hz [1]  | 5         | Check DIMMs, system board              |
| Video error                              | Blinks red 6 times @ 1 Hz [1]  | 6         | Check graphics card or system board    |
| PCA failure detected by BIOS (pre-video) | Blinks red 7 times @ 1 Hz [1]  | 7         | Replace system board                   |
| Invalid ROM checksum error               | Blinks red 8 times @ 1 Hz [1]  | 8         | Reflash BIOS ROM                       |
| Boot failure (after power on)            | Blinks red 9 times @ 1 Hz [1]  | 9         | Check power supply, processor, sys. bd |
| Bad option card                          | Blinks red 10 times @ 1 Hz [1] | None      | Replace option card                    |

NOTES:

Beeps are repeated for 5 cycles, after which only blinking LED indication continues.

[1] Repeated after 2 second pause.

[2] Beeps are produced by the internal chassis speaker.

[3] Check that CPU power connector P3 is plugged in.

### 4.5.4 Thermal Sensing and Cooling

All systems feature a variable-speed fan mounted as part of the processor heatsink assembly. All systems also provide or support an auxiliary chassis fan. All fans are controlled through temperature sensing logic on the system board and/or in the power supply. There are some electrical differences between form factors and between some models, although the overall functionality is the same. Typical cooling conditions include the following:

1. Normal—Low fan speed.
2. Hot processor—ASIC directs Speed Control logic to increase speed of fan(s).
3. Hot power supply—Power supply increases speed of fan(s).
4. Sleep state—Fan(s) turned off. Hot processor or power supply will result in starting fan(s).

The RPM (speed) of all fans is the result of the temperature of the CPU as sensed by speed control circuitry. The fans are controlled to run at the slowest (quietest) speed that will maintain proper cooling.

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Units using chassis and CPU fans must have both fans connected to their corresponding headers to ensure proper cooling of the system.

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## **4.6 Register Map and Miscellaneous Functions**

This section contains the system I/O map and information on general-purpose functions of the ICH10 and I/O controller.

### **4.6.1 System I/O Map**

Table 4-9 lists the fixed addresses of the input/output (I/O) ports.

**Table 4-9**  
**System I/O Map**

| <b>I/O Port</b> | <b>Function</b>  |
|-----------------|--|
| 0000..001Fh     | DMA Controller 1   |
| 0020..002Dh     | Interrupt Controller 1   |
| 002E, 002Fh     | Index, Data Ports to SIO Controller (primary)  |
| 0030..003Dh     | Interrupt Controller   |
| 0040..0042h     | Timer 1  |
| 004E, 004Fh     | Index, Data Ports to SIO Controller (secondary)  |
| 0050..0052h     | Timer / Counter  |
| 0060..0067h     | Microcontroller, NMI Controller (alternating addresses)                                  |
| 0070..0077h     | RTC Controller   |
| 0080..0091h     | DMA Controller   |
| 0092h           | Port A, Fast A20/Reset Generator   |
| 0093..009Fh     | DMA Controller   |
| 00A0..00B1h     | Interrupt Controller 2   |
| 00B2h, 00B3h    | APM Control/Status Ports   |
| 00B4..00BDh     | Interrupt Controller   |
| 00C0..00DFh     | DMA Controller 2   |
| 00F0h           | Coprocessor error register   |
| 0170..0177h     | IDE Controller 2 (active only if standard I/O space is enabled for secondary controller) |
| 01F0..01F7h     | IDE Controller 1 (active only if standard I/O space is enabled for primary controller)   |
| 0278..027Fh     | Parallel Port (LPT2)   |
| 02E8..02EFh     | Serial Port (COM4)   |
| 02F8..02FFh     | Serial Port (COM2)   |
| 0370..0377h     | Diskette Drive Controller Secondary Address  |
| 0376h           | IDE Controller 2 (active only if standard I/O space is enabled for primary drive)        |
| 0378..037Fh     | Parallel Port (LPT1)   |
| 03B0..03DFh     | Graphics Controller  |
| 03BC..03BEh     | Parallel Port (LPT3)   |
| 03E8..03EFh     | Serial Port (COM3)   |
| 03F0..03F5h     | Diskette Drive Controller Primary Addresses  |
| 03F6h           | IDE Controller 1 (active only if standard I/O space is enabled for sec. drive)           |
| 03F8..03FFh     | Serial Port (COM1)   |
| 04D0, 04D1h     | Interrupt Controller   |
| 0678..067Fh     | Parallel Port (LPT2)   |
| 0778..077Fh     | Parallel Port (LPT1)   |
| 07BC..07BEh     | Parallel Port (LPT3)   |
| 0CF8h           | PCI Configuration Address (dword access only )   |
| 0CF9h           | Reset Control Register   |
| 0CFCh           | PCI Configuration Data (byte, word, or dword access)                                     |

**NOTE:**

Assume unmarked gaps are unused, reserved, or used by functions that employ variable I/O address mapping. Some ranges may include reserved addresses.

## 4.6.2 GPIO Functions

### ICH10 Functions

The ICH10 provides various functions through the use of programmable general purpose input/output (GPIO) ports. These systems use GPIO ports and associate registers of the ICH10 for the following functions:

- PCI interrupt request control
- Chassis and board ID
- Hood (cover) sensor and lock detect
- Media card reader detect
- S4 state indicator
- USB port over-current detect
- Flash security override
- Serial port detect
- REQn#/GNTn# signal control
- Password enable
- Boot block enable

### SIO Controller Functions

In addition to the serial and parallel port functions, the SIO controller provides the following specialized functions through GPIO ports:

- Power/Hard drive LED control for indicating system events (refer to Table 4-8)
- Hood lock/unlock controls the lock bar mechanism
- Thermal shutdown control turns off the CPU when temperature reaches certain level
- Processor present/speed detection detects if the processor has been removed. The occurrence of this event will, during the next boot sequence, initiate the speed selection routine for the processor.
- Legacy/ACPI power button mode control uses the pulse signal from the system's power button and produces the PS On signal according to the mode (legacy or ACPI) selected. Refer to chapter 7 for more information regarding power management.

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# Input/Output Interfaces

## 5.1 Introduction

This chapter describes the standard interfaces that provide input and output (I/O) porting of data and that are controlled through I/O-mapped registers. The following I/O interfaces are covered in this chapter:

- SATA/eSATA interfaces (5.2)
- Diskette drive interface (5.3)
- Serial interfaces (5.4)
- Parallel interface support (5.5)
- Keyboard/pointing device interface (5.6)
- Universal serial bus interface (5.7)
- Audio subsystem (5.8)
- Network interface controller (5.9)

## 5.2 SATA/eSATA Interfaces

These systems provide two, three, or four serial ATA (SATA) interfaces that support transfer rates up to 3.0 Gb/s and RAID data protection functionality. The SFF and CMT form factors can also support an external SATA (eSATA) device through an optional bracket/cable assembly.

### 5.2.1 SATA interface

The SATA interface duplicates most of the functionality of the EIDE interface through a register interface that is equivalent to that of the legacy IDE host adapter. The ICH10 DO component includes Intel RAID migration technology that simplifies the migration from a single hard to a RAID0 or RAID1 dual hard drive array without requiring OS reinstallation. Intel Matrix RAID provides exceptional storage performance with increased data protection for configurations using dual drive arrays. A software solution is included that provides full management and status reporting of the RAID array, and the BIOS ROM also supports RAID creation, naming, and deletion of RAID arrays.

The standard 7-pin SATA connector is shown in the figure below.

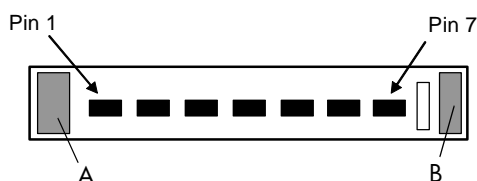


Figure 5-1. 7-Pin SATA Connector (P60-P64 on system board).

**Table 5-1.**  
**7-Pin SATA Connector Pinout**

| Pin | Description | Pin | Description  |
|-----|-------------|-----|--------------|
| 1   | Ground      | 6   | RX positive  |
| 2   | TX positive | 7   | Ground       |
| 3   | TX negative | A   | Holding clip |
| 4   | Ground      | B   | Holding clip |
| 5   | RX negative | --  | --           |



The USDT system includes a notebook-type SATA connector (J102) that mates directly (i.e., without a cable) to a 2.5-inch mass storage device.

## 5.2.2 eSATA interface

The SFF and CMT form factors provide a SATA/eSATA port (connector P64 on the system board) that can support an external SATA (eSATA) storage device. The eSATA interface provides higher bandwidth than USB 2.0 and Firewire (1394) interfaces.

An optional bracket/cable assembly (Figure 5-2) is required to attach an eSATA device to the SFF or CMT system.

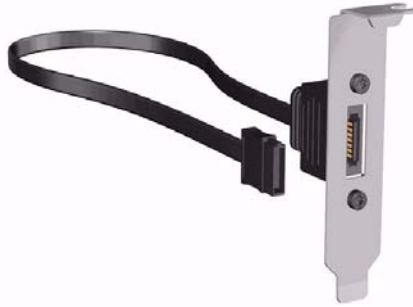


Figure 5-2. Optional eSATA Bracket/Cable Assembly.

The following operating parameters of the eSATA interface can be set in the ROM-based Setup utility:

- Transfer speed: 1.5 or 3 Gbps (default set to 1.5 Gbps for reliability)
- Emulation mode: IDE, AHCI, or RAID (default set to AHCI)
- Port availability: Available or Hidden (default set to Available)

In the IDE or AHCI modes, the system BIOS ROM controls the hard drives and Removeable Media Boot setting applies. In the RAID mode, the RAID option ROM controls the hard drives and the Removeable Media Boot setting does *not* apply.

For hot-plug functionality, the eSATA port must be set to the AHCI or RAID mode and an AHCI driver with hot-plug support must be loaded onto the system. This driver is pre-loaded on systems shipped with a Windows XP or Vista image. If the system is wiped clean or the Windows OS is re-installed, the AHCI driver can be loaded by installing the OS while the eSATA emulation mode is set to AHCI.

## 5.3 Diskette Drive Interface

The SFF and CMT form factors support a diskette drive through a standard 34-pin diskette drive connector.

The diskette drive interface function is integrated into the super I/O component. The internal logic of the I/O controller is software-compatible with standard 82077-type logic. The diskette drive controller has three operational phases in the following order:

- Command phase—The controller receives the command from the system.
- Execution phase—The controller carries out the command.
- Results phase—Status and results data is read back from the controller to the system.

The Command phase consists of several bytes written in series from the CPU to the data register (3F5h/375h). The first byte identifies the command and the remaining bytes define the parameters of the command. The Main Status register (3F4h/374h) provides data flow control for the diskette drive controller and must be polled between each byte transfer during the Command phase.

The Execution phase starts as soon as the last byte of the Command phase is received. An Execution phase may involve the transfer of data to and from the diskette drive, a mechanical control function of the drive, or an operation that remains internal to the diskette drive controller.

Data transfers (writes or reads) with the diskette drive controller are by DMA, using the DRQ2 and DACK2- signals for control.

The Results phase consists of the CPU reading a series of status bytes (from the data register (3F5h/375h)) that indicate the results of the command. Note that some commands do not have a Result phase, in which case the Execution phase can be followed by a Command phase.

During periods of inactivity, the diskette drive controller is in a non-operation mode known as the Idle phase.



The SFF and CMT form factors use a standard 34-pin connector for diskette drives (refer to Figure 5-3 and Table 5-3 for the pinout). Drive power is supplied through a separate connector.

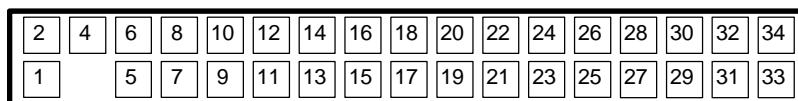


Figure 5-3. 34-Pin Diskette Drive Connector (P10 on system board).

**Table 5-3.**  
**34-Pin Diskette Drive Connector Pinout**

| Pin | Signal     | Description             | Pin | Signal     | Description                  |
|-----|------------|-------------------------|-----|------------|------------------------------|
| 1   | GND        | Ground                  | 18  | DIR-       | Drive head direction control |
| 2   | LOW DEN-   | Low density select      | 19  | GND        | Ground                       |
| 3   | ---        | (KEY)                   | 20  | STEP-      | Drive head track step cntrl. |
| 4   | MEDIA ID-  | Media identification    | 21  | GND        | Ground                       |
| 5   | GND        | Ground                  | 22  | WR DATA-   | Write data                   |
| 6   | DRV 4 SEL- | Drive 4 select          | 23  | GND        | Ground                       |
| 7   | GND        | Ground                  | 24  | WR ENABLE- | Enable for WR DATA-          |
| 8   | INDEX-     | Media index is detected | 25  | GND        | Ground                       |
| 9   | GND        | Ground                  | 26  | TRK 00-    | Heads at track 00 indicator  |
| 10  | MTR 1 ON-  | Activates drive motor   | 27  | GND        | Ground                       |
| 11  | GND        | Ground                  | 28  | WR PRTK-   | Media write protect status   |
| 12  | DRV 2 SEL- | Drive 2 select          | 29  | GND        | Ground                       |
| 13  | GND        | Ground                  | 30  | RD DATA-   | Data and clock read off disk |
| 14  | DRV 1 SEL- | Drive 1 select          | 31  | GND        | Ground                       |
| 15  | GND        | Ground                  | 32  | SIDE SEL-  | Head select (side 0 or 1)    |
| 16  | MTR 2 ON-  | Activates drive motor   | 33  | GND        | Ground                       |
| 17  | GND        | Ground                  | 34  | DSK CHG-   | Drive door opened indicator  |

## 5.4 Serial Interface

Systems covered in this guide may include one RS-232-C type serial interface to transmit and receive asynchronous serial data with external devices. Some systems may allow the installation of a second serial interface through an optional bracket/cable assembly that attaches to header P52 on the system board. The serial interface function is provided by the super I/O controller component that includes two NS16C550-compatible UARTs.

The UART supports the standard baud rates up through 115200, and also special high speed rates of 239400 and 460800 baud. The baud rate of the UART is typically set to match the capability of the connected device. While most baud rates may be set at runtime, baud rates 230400 and 460800 must be set during the configuration phase.

The serial interface uses a DB-9 connector as shown in the following figure with the pinout listed in Table 5-4.

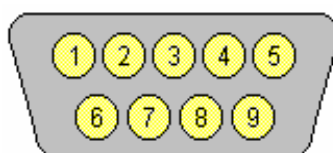


Figure 5-4. DB-9 Serial Interface Connector (as viewed from rear of chassis)

**Table 5-4.**  
**DB-9 Serial Connector Pinout**

| Pin | Signal  | Description         | Pin | Signal | Description     |
|-----|---------|---------------------|-----|--------|-----------------|
| 1   | CD      | Carrier Detect      | 6   | DSR    | Data Set Ready  |
| 2   | RX Data | Receive Data        | 7   | RTS    | Request To Send |
| 3   | TX Data | Transmit Data       | 8   | CTS    | Clear To Send   |
| 4   | DTR     | Data Terminal Ready | 9   | RI     | Ring Indicator  |
| 5   | GND     | Ground              | --  | --     | --              |

The standard RS-232-C limitation of 50 feet (or less) of cable between the DTE (computer) and DCE (modem) should be followed to minimize transmission errors. Higher baud rates may require shorter cables.

## 5.5 Parallel Interface Support

The SFF and CMT form factors include a system board header (J50) that supports an optional parallel bracket/cable assembly that provides a parallel interface for a peripheral device such as a printer. The parallel interface supports bi-directional 8-bit parallel data transfers with a peripheral device. The parallel interface supports three main modes of operation:

- Standard Parallel Port (SPP) mode
- Enhanced Parallel Port (EPP) mode
- Extended Capabilities Port (ECP) mode

These three modes (and their submodes) provide complete support as specified for an IEEE 1284 parallel port.

### 5.5.1 Standard Parallel Port Mode

The Standard Parallel Port (SPP) mode uses software-based protocol and includes two sub-modes of operation, compatible and extended, both of which can provide data transfers up to 150 KB/s. In the compatible mode, CPU write data is simply presented on the eight data lines. A CPU read of the parallel port yields the last data byte that was written.

### 5.5.2 Enhanced Parallel Port Mode

In Enhanced Parallel Port (EPP) mode, increased data transfers are possible (up to 2 MB/s) due to a hardware protocol that provides automatic address and strobe generation. EPP revisions 1.7 and 1.9 are both supported. For the parallel interface to be initialized for EPP mode, a negotiation phase is entered to detect whether or not the connected peripheral is compatible with EPP mode. If compatible, then EPP mode can be used. In EPP mode, system timing is closely coupled to EPP timing. A watchdog timer is used to prevent system lockup.

### 5.5.3 Extended Capabilities Port Mode

The Extended Capabilities Port (ECP) mode, like EPP, also uses a hardware protocol-based design that supports transfers up to 2 MB/s. Automatic generation of addresses and strobes as well as Run Length Encoding (RLE) decompression is supported by ECP mode. The ECP mode includes a bi-directional FIFO buffer that can be accessed by the CPU using DMA or programmed I/O. For the parallel interface to be initialized for ECP mode, a negotiation phase is entered to detect whether or not the connected peripheral is compatible with ECP mode. If compatible, then ECP mode can be used.

The ECP mode includes several sub-modes as determined by the Extended Control register. Two submodes of ECP allow the parallel port to be controlled by software. In these modes, the FIFO is cleared and not used, and DMA and RLE are inhibited.

## 5.5.4 Parallel Interface Connector

Figure 5-5 and Table 5-5 show the connector and pinout of the parallel connector provided on the optional parallel bracket/cable assembly. Note that some signals are redefined depending on the port's operational mode.

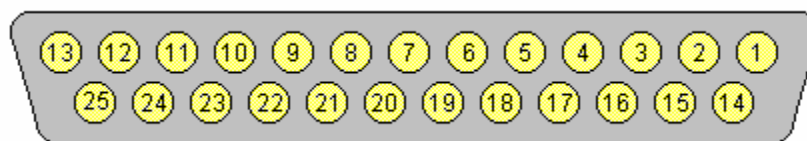


Figure 5-5. DB-25 Parallel Interface Connector (as viewed from rear of chassis)

**Table 5-5.**  
**DB-25 Parallel Connector Pinout**

| Pin | Signal | Function                     | Pin | Signal  | Function                        |
|-----|--------|------------------------------|-----|---------|---------------------------------|
| 1   | STB-   | Strobe / Write [1]           | 14  | LF-     | Line Feed [2]                   |
| 2   | D0     | Data 0                       | 15  | ERR-    | Error [3]                       |
| 3   | D1     | Data 1                       | 16  | INIT-   | Initialize Paper [4]            |
| 4   | D2     | Data 2                       | 17  | SLCTIN- | Select In / Address. Strobe [1] |
| 5   | D3     | Data 3                       | 18  | GND     | Ground                          |
| 6   | D4     | Data 4                       | 19  | GND     | Ground                          |
| 7   | D5     | Data 5                       | 20  | GND     | Ground                          |
| 8   | D6     | Data 6                       | 21  | GND     | Ground                          |
| 9   | D7     | Data 7                       | 22  | GND     | Ground                          |
| 10  | ACK-   | Acknowledge / Interrupt [1]  | 23  | GND     | Ground                          |
| 11  | BSY    | Busy / Wait [1]              | 24  | GND     | Ground                          |
| 12  | PE     | Paper End / User defined [1] | 25  | GND     | Ground                          |
| 13  | SLCT   | Select / User defined [1]    | --  | --      | --                              |

NOTES:

[1] Standard and ECP mode function / EPP mode function

[2] EPP mode function: Data Strobe

ECP modes: Auto Feed or Host Acknowledge

[3] EPP mode: user defined

ECP modes: Fault or Peripheral Req.

[4] EPP mode: Reset

ECP modes: Initialize or Reverse Req.

## 5.6 Keyboard/Pointing Device Interface

The keyboard/pointing device interface function is provided by the SIO controller component, which integrates 8042-compatible keyboard controller logic (hereafter referred to as simply the “8042”) to communicate with the keyboard and pointing device using bi-directional serial data transfers. The 8042 handles scan code translation and password lock protection for the keyboard as well as communications with the pointing device.

### 5.6.1 Keyboard Interface Operation

The data/clock link between the 8042 and the keyboard is uni-directional for Keyboard Mode 1 and bi-directional for Keyboard Modes 2 and 3. (These modes are discussed in detail in Appendix C). This section describes Mode 2 (the default) mode of operation.

Communication between the keyboard and the 8042 consists of commands (originated by either the keyboard or the 8042) and scan codes from the keyboard. A command can request an action or indicate status. The keyboard interface uses IRQ1 to get the attention of the CPU.

The 8042 can send a command to the keyboard at any time. When the 8042 wants to send a command, the 8042 clamps the clock signal from the keyboard for a minimum of 60 us. If the keyboard is transmitting data at that time, the transmission is allowed to finish. When the 8042 is ready to transmit to the keyboard, the 8042 pulls the data line low, causing the keyboard to respond by pulling the clock line low as well, allowing the start bit to be clocked out of the 8042. The data is then transferred serially, LSb first, to the keyboard (Figure 5-6). An odd parity bit is sent following the eighth data bit. After the parity bit is received, the keyboard pulls the data line low and clocks this condition to the 8042. When the keyboard receives the stop bit, the clock line is pulled low to inhibit the keyboard and allow it to process the data.

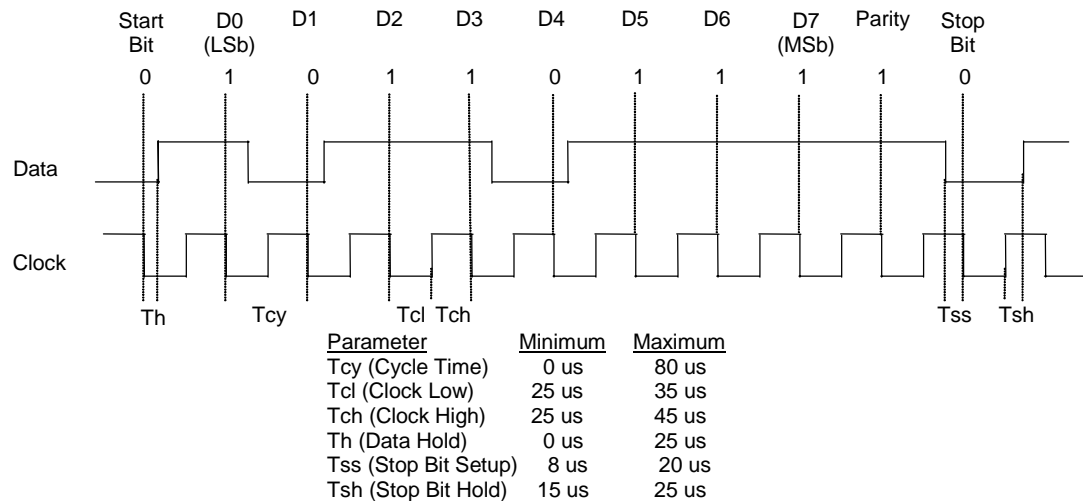


Figure 5-6. 8042-To-Keyboard Transmission of Code EDh, Timing Diagram

Control of the data and clock signals is shared by the 8042 and the keyboard depending on the originator of the transferred data. Note that the clock signal is always generated by the keyboard.

After the keyboard receives a command from the 8042, the keyboard returns an ACK code. If a parity error or timeout occurs, a Resend command is sent to the 8042.

## 5.6.2 Pointing Device Interface Operation

The pointing device (typically a mouse) connects to a 6-pin DIN-type connector that is identical to the keyboard connector both physically and electrically. The operation of the interface (clock and data signal control) is the same as for the keyboard. The pointing device interface uses the IRQ12 interrupt.

## 5.6.3 Keyboard/Pointing Device Interface Connector

The legacy-light model provides separate PS/2 connectors for the keyboard and pointing device. Both connectors are identical both physically and electrically. Figure 5-7 and Table 5-6 show the connector and pinout of the keyboard/pointing device interface connectors.

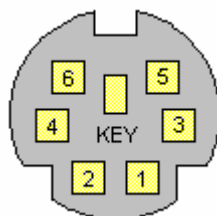


Figure 5-7. PS/2 Keyboard or Pointing Device Interface Connector (as viewed from rear of chassis)

**Table 5-6.**  
**Keyboard/Pointing Device Connector Pinout**

| Pin | Signal | Description   | Pin | Signal  | Description   |
|-----|--------|---------------|-----|---------|---------------|
| 1   | DATA   | Data          | 4   | + 5 VDC | Power         |
| 2   | NC     | Not Connected | 5   | CLK     | Clock         |
| 3   | GND    | Ground        | 6   | NC      | Not Connected |

## 5.7 Universal Serial Bus Interface

The Universal Serial Bus (USB) interface provides asynchronous/isochronous data transfers with compatible peripherals such as keyboards, printers, or modems. This high-speed interface supports hot-plugging of compatible devices, making possible system configuration changes without powering down or even rebooting systems.

These systems provide eight externally-accessible USB ports, two front panel USB ports (which may be disabled) and six USB ports on the rear panel. In addition, the SFF and CMT form factors support a media reader accessory that uses two USB ports through a system board connection. The USB ports are dynamically configured to either a USB 1.1 controller or the USB 2.0 controller depending on the capability of the peripheral device. The 1.1 controllers provide a maximum transfer rate of 12 Mb/s while the 2.0 controller provides a maximum transfer rate of 480 Mb/s. Table 5-7 shows the mapping of the USB ports.

**Table 5-7.**  
**ICH10 USB Port Mapping**

| <b>ICH10 Controller</b>   | <b>Signals</b>                 | <b>USB Connector Location (all form factors)</b>     |
|---------------------------|--------------------------------|--|
| USB 1.1 #1,<br>USB 2.0 #1 | Data 0P, 0N<br>Data 1P, 1N     | System board header P151<br>not connected            |
| USB 1.1 #2,<br>USB 2.0 #1 | Data 2P, 2N<br>Data 3P, 3N     | System board header P150<br>System board header P150 |
| USB 1.1 #3,<br>USB 2.0 #1 | Data 4P, 4N<br>Data 5P, 5N     | Front panel USB<br>Front panel USB                   |
| USB 1.1 #4,<br>USB 2.0 #2 | Data 6P, 6N<br>Data 7P, 7N     | Rear panel USB<br>Rear panel USB                     |
| USB 1.1 #5,<br>USB 2.0 #2 | Data 8P, 8N<br>Data 9P, 9N     | Rear panel USB<br>Rear panel USB                     |
| USB 1.1 #6,<br>USB 2.0 #2 | Data 10P, 10N<br>Data 11P, 11N | Rear panel USB<br>Rear panel USB                     |

### 5.7.1 USB Connector

These systems provide type-A USB ports as shown in Figure 5-7.

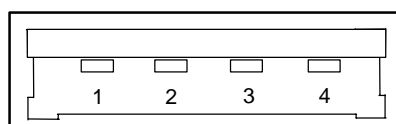


Figure 5-8. Universal Serial Bus Connector (as viewed from rear of chassis)

**Table 5-8.  
USB Connector Pinout**

| Pin | Signal | Description  | Pin | Signal | Description |
|-----|--------|--------------|-----|--------|-------------|
| 1   | Vcc    | +5 VDC       | 3   | USB+   | Data (plus) |
| 2   | USB-   | Data (minus) | 4   | GND    | Ground      |

## 5.7.2 USB Cable Data

The recommended cable length between the host and the USB device should be no longer than sixteen feet for full-channel (12 MB/s) operation, depending on cable specification (see following table).

**Table 5-9.  
USB Cable Length Data**

| Conductor Size | Resistance     | Maximum Length   |
|----------------|----------------|------------------|
| 20 AWG         | 0.036 $\Omega$ | 16.4 ft (5.00 m) |
| 22 AWG         | 0.057 $\Omega$ | 9.94 ft (3.03 m) |
| 24 AWG         | 0.091 $\Omega$ | 6.82 ft (2.08 m) |
| 26 AWG         | 0.145 $\Omega$ | 4.30 ft (1.31 m) |
| 28 AWG         | 0.232 $\Omega$ | 2.66 ft (0.81 m) |

**NOTE:**

For sub-channel (1.5 MB/s) operation and/or when using sub-standard cable shorter lengths may be allowable and/or necessary.

The shield, chassis ground, and power ground should be tied together at the host end but left unconnected at the device end to avoid ground loops.

**Table 5-10.  
USB Color Code**

| Signal | Insulation color |
|--------|------------------|
| Data + | Green            |
| Data - | White            |
| Vcc    | Red              |
| Ground | Black            |



## 5.8 Audio Subsystem

These systems use the HD audio controller of the 82801 component to access and control an Analog Devices AD1884A HD Audio Codec, which provides 2-channel high definition analog-to-digital (ADC) and digital-to-analog (DAC) conversions. A block diagram of the audio subsystem is shown in Figure 5-9. All control functions such as volume, audio source selection, and sampling rate are controlled through software through the HD Audio Interface of the 82801 ICH component. Control data and digital audio streams (record and playback) are transferred between the ICH and the Audio Codec over the HD Audio Interface. The codec's speaker output is applied to a 1.5-watt amplifier that drives the internal speaker. A device plugged into the Headphone jack or the line input jack is sensed by the system, which will inhibit the Speaker Audio signal.

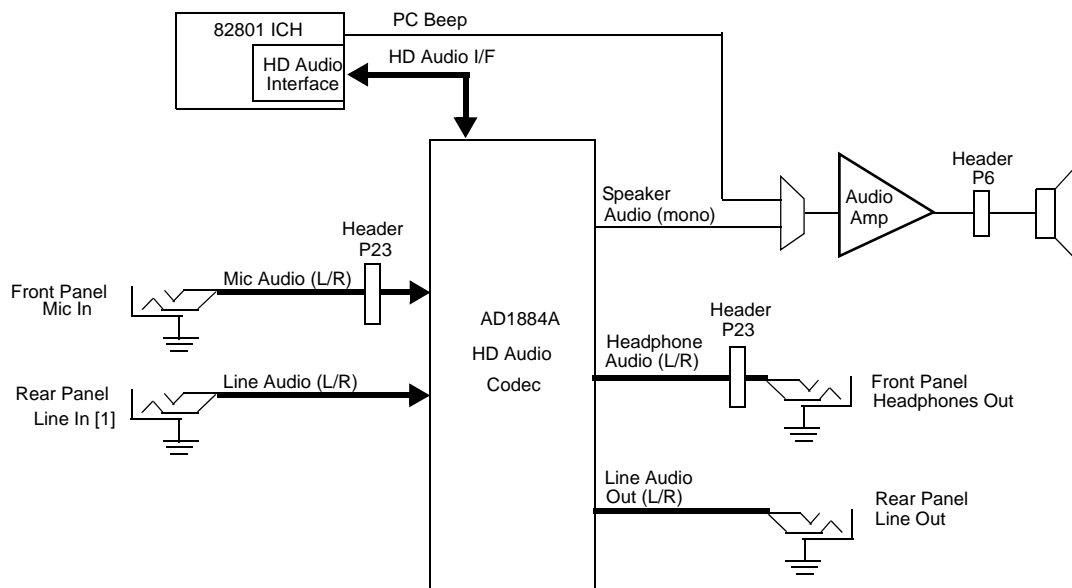
These systems provide the following analog interfaces for external audio devices:

**Microphone In**—This input uses a three-conductor 1/8-inch mini-jack that accepts a stereo microphone.

**Line In**—This input uses a three-conductor (stereo) 1/8-inch mini-jack designed for connection of a high-impedance audio source such as a tape deck. This jack can be re-tasked to a Microphone In function.

**Headphones Out**—This input uses a three-conductor (stereo) 1/8-inch mini-jack that is designed for connecting a set of 32-ohm (nom.) stereo headphones. Plugging into the Headphones jack mutes the signal to the internal speaker and the Line Out jack as well.

**Line Out**—This output uses a three-conductor (stereo) 1/8-inch mini-jack for connecting left and right channel line-level signals. Typical connections include a tape recorder's Line In (Record In) jacks, an amplifier's Line In jacks, or to powered speakers that contain amplifiers.



**NOTES:**

L/R = Separate left and right channels (stereo). L+R = Combined left and right channels (mono).

[1] Can be re-configured as Microphone In

Figure 5-9. Audio Subsystem Functional Block Diagram

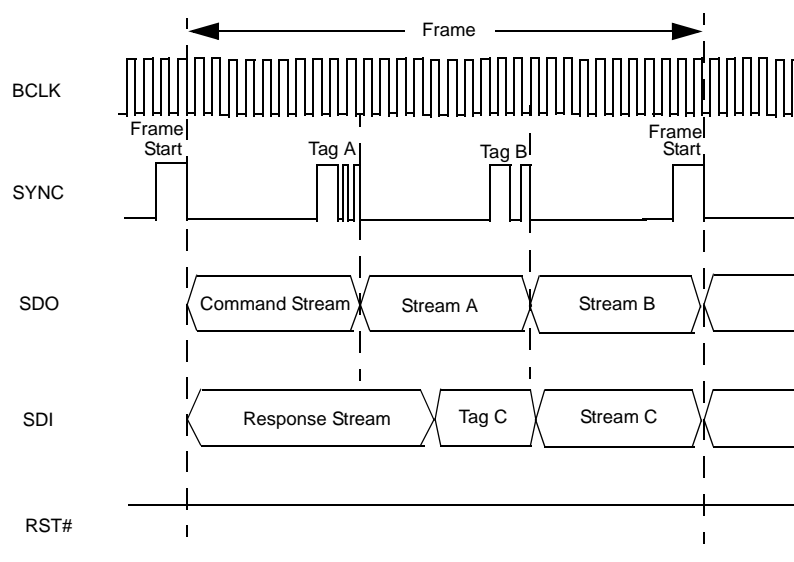
## 5.8.1 HD Audio Controller

The HD Audio Controller is a PCI Express device that is integrated into the 82801 ICH component and supports the following functions:

- Read/write access to audio codec registers
- Support for greater than 48-KHz sampling
- HD audio interface

## 5.8.2 HD Audio Link Bus

The HD audio controller and the HD audio codec communicate over a five-signal HD Audio Link Bus (Figure 5-10). The HD Audio Interface includes two serial data lines; serial data out (SDO, from the controller) and serial data in (SDI, from the audio codec) that transfer control and PCM audio data serially to and from the audio codec using a time-division multiplexed (TDM) protocol. The data lines are qualified by the 24-MHz BCLK signal driven by the audio controller. Data is transferred in frames synchronized by the 48-KHz SYNC signal, which is derived from the clock signal and driven by the audio controller. When asserted (typically during a power cycle), the RESET- signal (not shown) will reset all audio registers to their default values.



NOTE: Clock not drawn to scale.

Figure 5-10. HD Audio Link Bus Protocol

## 5.8.3 Audio Multistreaming

The audio subsystem can be configured (through the ADI control panel) for processing audio for multiple applications. The Headphone Out jack can provide audio for one application while the Line Out jack can provide external speaker audio from another application.

## 5.8.4 Audio Specifications

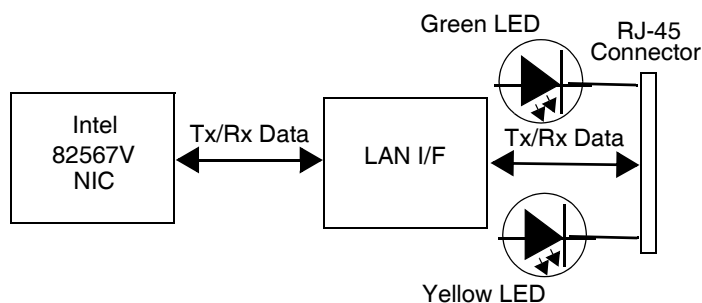
The specifications for the HD Audio subsystem are listed in Table 5-11.

**Table 5-11.  
HD Audio Subsystem Specifications**

| <b>Parameter</b>  | <b>Measurement</b>         |
|---|----------------------------|
| Sampling Rates:   |                            |
| DAC   | 44.1-, 48-, 96-, & 192-KHz |
| ADC   | 44.1-, 48-, 96-, & 192KHz  |
| Resolution:   |                            |
| DAC   | 24-bit                     |
| ADC   | 24-bit                     |
| Nominal Input Voltage:  |                            |
| Mic In (w/+20 db gain)  | .283 Vp-p                  |
| Line In   | 2.83 Vp-p                  |
| Subsystem Impedance:  |                            |
| Mic In  | 20K ohms                   |
| Line In   | 20K ohms                   |
| Line Out (minimum expected load)                                      | 10K ohms                   |
| Headphones Out (minimum expected load)                                | 32 ohms                    |
| Signal-to-Noise Ratio   |                            |
| Line out  | 90 db (nom)                |
| Headphone out   | 90 db (nom)                |
| Microphone / line in  | 85 db (nom)                |
| Total Harmonic Distortion (THD)                                       |                            |
| Line out  | -84 db                     |
| Headphone out   | -80 db                     |
| Microphone / line in  | -78 db                     |
| Max. Subsystem Power Output to 4-ohm Internal Speaker (with 10% THD): | 1.5 watts                  |
| Gain Step   | 1.5 db                     |
| Master Volume Range   | -58.5 db                   |
| Frequency Response:   |                            |
| ADC/DAC   | 20– 20000 Hz               |
| Internal Speaker  | 450–20000 Hz               |

## 5.9 Network Interface Controller

These systems provide 10/100/1000 Mbps network support through an Intel 82567V network interface controller (NIC), a PHY component, and a RJ-45 jack with integral status LEDs (Figure 5-11). The support firmware is contained in the system (BIOS) ROM. The NIC can operate in half- or full-duplex modes, and provides auto-negotiation of both mode and speed. Half-duplex operation features an Intel-proprietary collision reduction mechanism while full-duplex operation follows the IEEE 802.3x flow control specification.



| LED    | Function  |
|--------|---|
| Green  | Activity/Link. Indicates network activity and link pulse reception. |
| Yellow | Speed: Off = 10 Mb/s, yellow = 100Mb/s, green = 1 Gb/s.             |

Figure 5-11. Network Interface Controller Block Diagram

The Network Interface Controller includes the following features:

- VLAN tagging with Windows XP and Linux
- Multiple VLAN support with Windows XP
- Power management support for ACPI 1.1, PXE 2.0, WOL, ASF 1.0, and IPMI
- Cisco Etherchannel support
- Link and Activity LED indicator drivers

The controller features high and low priority queues and provides priority-packet processing for networks that can support that feature. The controller's micro-machine processes transmit and receive frames independently and concurrently. Receive runt (under-sized) frames are not passed on as faulty data but discarded by the controller, which also directly handles such errors as collision detection or data under-run.

The NIC uses 3.3 VDC auxiliary power, which allows the controller to support Wake-On-LAN (WOL) and Alert-On-LAN (AOL) functions while the main system is powered down.



For the features in the following paragraphs to function as described, the system unit must be plugged into a live AC outlet. Controlling unit power through a switchable power strip will, with the strip turned off, disable any wake, alert, or power management functionality.

## 5.9.1 Wake-On-LAN Support

The NIC supports the Wired-for-Management (WfM) standard of Wake-On-LAN (WOL) that allows the system to be booted up from a powered-down or low-power condition upon the detection of special packets received over a network. The NIC receives 3.3 VDC auxiliary power while the system unit is powered down in order to process special packets. The detection of a Magic Packet by the NIC results in the PME- signal on the PCI bus to be asserted, initiating system wake-up from an ACPI S1 or S3 state.

## 5.9.2 Alert Standard Format Support

Alert Standard Format (ASF) support allows the NIC to communicate the occurrence of certain events over a network to an ASF 1.0-compliant management console and, if necessary, take action that may be required. The ASF communications can involve the following:

- Alert messages sent by the client to the management console.
- Maintenance requests sent by the management console to the client.
- Description of client's ASF capabilities and characteristics.

The activation of ASF functionality requires minimal intervention of the user, typically requiring only booting a client system that is connected to a network with an ASF-compliant management console.

## 5.9.3 Power Management Support

The NIC features Wired-for-Management (WfM) support providing system wake up from network events (WOL) as well as generating system status messages (AOL) and supports ACPI power management environments. The controller receives 3.3 VDC (auxiliary) power as long as the system is plugged into a live AC receptacle, allowing support of wake-up events occurring over a network while the system is powered down or in a low-power state.

The Advanced Configuration and Power Interface (ACPI) functionality of system wake up is implemented through an ACPI-compliant OS and is the default power management mode. The following wakeup events may be individually enabled/disabled through the supplied software driver:

- Magic Packet—Packet with node address repeated 16 times in data portion



The following functions are supported in NDIS5 drivers but implemented through remote management software applications (such as LanDesk).

- Individual address match—Packet with matching user-defined byte mask
- Multicast address match—Packet with matching user-defined sample frame
- ARP (address resolution protocol) packet
- Flexible packet filtering—Packets that match defined CRC signature

The PROSet Application software (pre-installed and accessed through the System Tray or Windows Control Panel) allows configuration of operational parameters such as WOL and duplex mode.

## 5.9.4 NIC Connector

Figure 5-12 shows the RJ-45 connector used for the NIC interface. This connector includes the two status LEDs as part of the connector assembly.

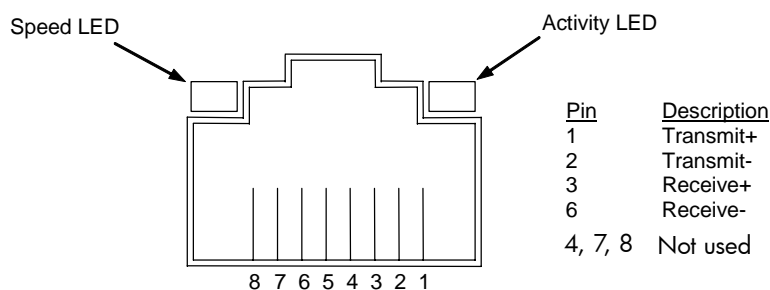


Figure 5-12. RJ-45 Ethernet TPE Connector (as viewed from rear of chassis)

## 5.9.5 NIC Specifications

**Table 5-12.**  
**NIC Specifications**

| Parameter                | Compatibility standard or protocol   |
|--------------------------|--|
| Modes Supported          | 10BASE-T half duplex @ 10 Mb/s<br>10Base-T full duplex @ 20 Mb/s<br>100BASE-TX half duplex @ 100 Mb/s<br>100Base-TX full duplex @ 200 Mb/s<br>1000BASE-T half duplex @ 1 Gb/s<br>1000BASE-TX full duplex @ 2 Gb/s  |
| Standards Compliance     | IEEE 802.1P, 802.1Q<br>IEEE 802.2<br>IEEE 802.3, 802.3ab, 802.3ad, 802.3u, 802.3x,<br>802.3z   |
| OS Driver Support        | MS-DOS<br>MS Windows 3.1<br>MS Windows 95 (pre-OSR2), 98, and 2000 Professional, XP Home, XP Pro, Vista Home, Vista Pro<br>MS Windows NT 3.51 & 4.0<br>Novell Netware 3.x, 4.x, 5x<br>Novell Netware/IntraNetWare<br>SCO UnixWare 7<br>Linux 2.2, 2.4<br>PXE 2.0 |
| Boot ROM Support         | Intel PRO/100 Boot Agent (PXE 3.0, RPL)  |
| F12 BIOS Support         | Yes  |
| Bus Interface            | PCI Express x1   |
| Power Management Support | ACPI, PCI Power Management Spec.   |

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# Integrated Graphics Subsystem

## 6.1 Introduction

This chapter describes the graphics subsystem that is integrated into the Q45 GMCH component. This graphics subsystem employs the use of system memory to provide efficient, economical 2D and 3D performance.

All systems provide dual-monitor support in the standard configuration. The SFF and CMT systems include two PCIe graphics slots for upgrading the graphics controller by:

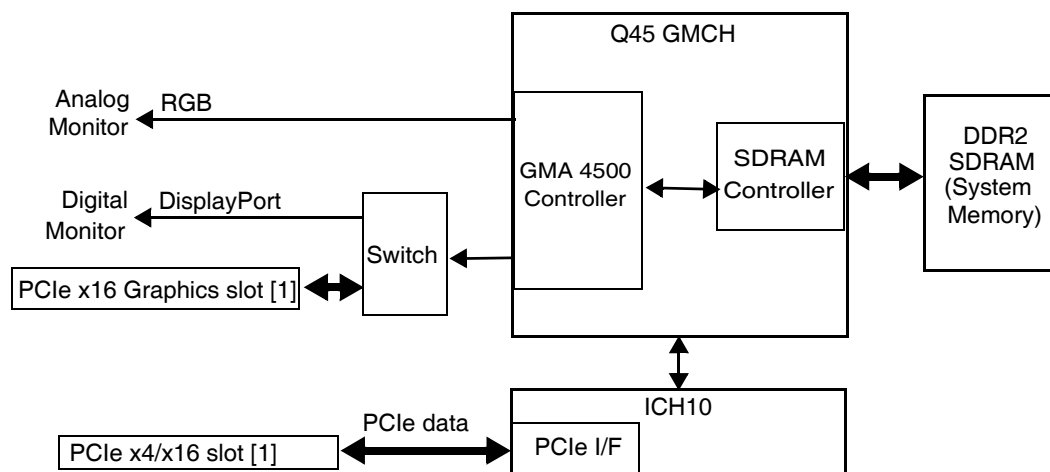
- Installing a PCIe x16 graphics card in the PCIe x16 graphics slot, which disables the integrated graphics controller
- Installing a PCIe x4 graphics card in the PCIe x4 slot (x16 connector), in which the integrated graphics controller can be re-enabled through the BIOS settings

This chapter covers the following subjects:

- Functional description (6.2)
- Display Modes (6.3)
- Upgrading (6.4)
- Monitor connectors (6.5)

## 6.2 Functional Description

The Intel Q45 GMCH component includes an Intel integrated Graphics Media Accelerator (GMA) 4500 controller (Figure 6-1). The GMA 4500 operates off the internal PCIe x16 bus and can directly drive an external, analog multi-scan monitor *and* a DisplayPort-compatible digital monitor simultaneously. The GMA 4500 includes a memory management feature that allocates portions of system memory for use as the frame buffer and for storing textures and 3D effects.



NOTE: [1] SFF and CMT form factors only.

Figure 6-1. Q45-based Graphics, Block diagram

The GMA 4500 provides the following features:

- Rapid pixel and texel rendering using four pipelines that allow 2D and 3D operations to overlap, speeding up visual effects, reducing the amount of memory for texture storage
- Zone rendering for optimizing 3D drawing, eliminating the need for local graphics memory by reducing the bandwidth
- Dynamic video memory allocation, where the amount of memory required by the application is acquired (or released) by the controller
- Intelligent memory management allowing tiled memory addressing, deep display buffering, and dynamic data management
- 400-MHz core engine
- 350-MHz 24-bit RAMDAC
- 2D engine supporting GDI+ and alpha stretch blithering up to 2048 x 1536 w/32-bit color @ 75 Hz refresh (QVGA)
- 3D engine supporting Z-bias and up to 1600 x 1200 w/32-bit color @ 85 hz refresh



The GMA 4500 uses a portion of system memory for instructions, textures, and frame (display) buffering. Using a process called Dynamic Video Memory Technology (DVMT), the controller dynamically allocates display and texture memory amounts according to the needs of the application running on the system.

The total memory allocation is determined by the amount of system memory installed in a system. The video BIOS pre-allocates 8 megabytes of memory during POST. System memory that is pre-allocated is not seen by the operating system, which will report the total amount of memory installed **less** the amount of pre-allocated memory.

The GMA 4500 will use, in standard VGA/SVGA modes, pre-allocated memory as a true dedicated frame buffer. If the system boots with the OS loading the GMA Extreme Graphics drivers, the pre-allocated memory will then be re-claimed by the drivers and may or may not be used by the GMA in the “extended” graphic modes. However, it is important to note that pre-allocated memory is available only to the GMA, not to the OS.

The Q45's DVMT function is an enhancement over the Unified Memory Architecture (UMA) of earlier systems. The DVMT of the Q45 selects, during the boot process, the maximum graphics memory allocation possible according on the amount of system memory installed:

**Table 6-1.**  
**GMA 4500 Memory Allocation**

| <b>SDRAM Installed</b> | <b>Maximum Memory Allocation</b> |
|------------------------|----------------------------------|
| 1 GB                   | 256 or 512 MB                    |
| > 1 GB                 | 384 MB                           |

The actual amount of system memory used by the GMA in the “extended” or “extreme” modes will increase and decrease dynamically according to the needs of the application. The amount of memory used solely for graphics (video) may be reported in a message on the screen, depending on the operating system and/or applications running on the machine.

For viewing the maximum amount of available frame buffer memory MS Windows go to the Control Panel and select the Display icon, then > **Settings** > **Advanced** > **Adapter**.

The Microsoft Direct Diagnostic tool included in most versions of Windows may be used to check the amount of video memory being used. The Display tab of the utility the “Approx. Total Memory” label will indicate the amount of video memory. The value will vary according to OS.



Some applications, particularly games that require advanced 3D hardware acceleration, may not install or run correctly on systems using the GMA.

## 6.3 Display Modes

The GMA supports the following standard display modes for 2D video displays:

| <b>Resolution</b> | <b>Maximum Refresh Rate</b> |                        |
|-------------------|-----------------------------|------------------------|
|                   | <b>Analog Monitor</b>       | <b>Digital Monitor</b> |
| 640 x 480         | 85 Hz                       | 60 Hz                  |
| 800 x 600         | 85 Hz                       | 60 Hz                  |
| 1024 x 768        | 85 Hz                       | 60 Hz                  |
| 1280 x 720        | 85 Hz                       | 60 Hz                  |
| 1280 x 1024       | 85 Hz                       | 60 Hz                  |
| 1440 x 900        | 85 Hz                       | 60 Hz                  |
| 1600 x 900        | 85 Hz                       | 60 Hz                  |
| 1600 x 1200       | 85 Hz                       | 60 Hz                  |
| 1680 x 1050       | 85 Hz                       | 60 Hz                  |
| 1920 x 1080       | 85 Hz                       | 60 Hz                  |
| 1920 x 1200       | 85 Hz                       | 60 Hz                  |
| 1920 x 1440       | 85 Hz                       | 60 Hz                  |
| 2048 x 1536       | 75 Hz                       | 60 Hz                  |

The highest resolution available will be determined by the following factors:

- Memory speed and amount
- Single or dual channel memory
- Number and type of monitors

All systems include both a legacy VGA connector and a DisplayPort interface. The DisplayPort is an alternate solution to (but not compatible with) HDMI and DVI. The DisplayPort interface consists of four data pair links, each of which can carry video, audio, and clock signals at a transfer rate of 1.62 or 2.7 Gb/s.

The DisplayPort interface provides multimode support through the use of an optional external adapter for connecting a DVI or VGA monitor.

## 6.4 Upgrading

All systems provide direct, dual-monitor support; a VGA monitor and a DisplayPort monitor can be connected and driven simultaneously. The SFF and CMT systems also include a PCIe x16 graphics connector that specifically supports a PCIe x16 graphics card and a PCIe x16 connector that provides PCIe x4 operation for an x4 or x16 PCIe card. These two PCIe slots provide the SFF and CMT form factors with flexible graphics upgrade paths.

The upgrade procedure for SFF and CMT formfactors is as follows:

1. Shut down the system through the operating system.
2. Unplug the power cord from the rear of the system unit.
3. Remove the chassis cover.
4. Install the graphics card into the PCIe x16 graphics slot or the PCIe x4/x16 slot.
5. Replace the chassis cover.
6. Reconnect the power cord to the system unit.
7. Power up the system unit:



---

If a PCIe graphics controller card is installed in the PCIe x16 graphics slot, the BIOS will detect the presence of the PCIe card and disable the integrated GMA of the Q45 GMCH. In this configuration, the integrated GMA cannot be enabled.

If a PCIe graphics controller card is installed in the PCIe x4 /x16 slot, the integrated GMA will be disabled by default, but can be re-enabled through the BIOS settings to allow an alternate method of multi-monitor operation. Press the **F10** key during the boot process to enter the ROM-based Setup utility and re-enable the GMA for multi-monitor operation. A PCIe x16 card installed in the PCIe x4/x16 slot will be limited to x4 operation.

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Two PCIe graphics can be installed in an SFF or CMT simultaneously to provide an alternate method for multi-monitor support. In this configuration, the integrated GMA will be disabled.

---

## 6.5 Monitor Connectors

All form factors provide an analog VGA connector and a DisplayPort connector, and can drive both types of monitors simultaneously.

### 6.5.1 Analog Monitor Connector

All form factors include a legacy VGA connector (Figure 6-2) for attaching an analog video monitor:

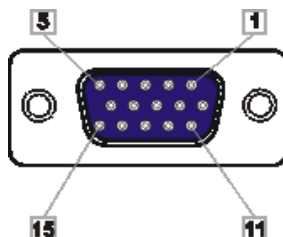


Figure 6-2. DB-15 Analog VGA Monitor Connector, (as viewed from rear of chassis).

**Table 6-3.**  
**DB-15 Monitor Connector Pinout**

| Pin | Signal | Description         | Pin | Signal | Description        |
|-----|--------|---------------------|-----|--------|--------------------|
| 1   | R      | Red Analog          | 9   | PWR    | +5 VDC (fused) [1] |
| 2   | G      | Blue Analog         | 10  | GND    | Ground             |
| 3   | B      | Green Analog        | 11  | NC     | Not Connected      |
| 4   | NC     | Not Connected       | 12  | SDA    | DDC Data           |
| 5   | GND    | Ground              | 13  | HSync  | Horizontal Sync    |
| 6   | R GND  | Red Analog Ground   | 14  | VSynC  | Vertical Sync      |
| 7   | G GND  | Blue Analog Ground  | 15  | SCL    | DDC Clock          |
| 8   | B GND  | Green Analog Ground | --  | --     | --                 |

NOTE:

[1] Fuse automatically resets when excessive load is removed.

## 6.5.2 DisplayPort Connector

All systems include a DisplayPort connector (Figure 6-3) for attaching a digital monitor. This interface also supports the use of an optional adapter for converting the DisplayPort output to a DVI or analog VGA output.

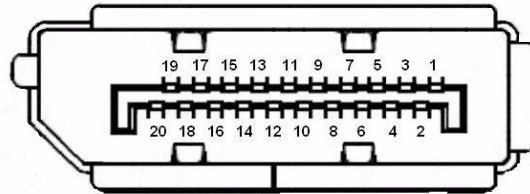


Figure 6-3. DisplayPort Connector, (as viewed from rear of chassis).

**Table 6-4.**  
**DB-15 Monitor Connector Pinout**

| Pin | Signal        | Pin | Signal          |
|-----|---------------|-----|-----------------|
| 1   | ML Lane (p) 0 | 11  | Ground          |
| 2   | Ground        | 12  | ML Lane (n) 3   |
| 3   | ML Lane (n) 0 | 13  | Ground          |
| 4   | ML Lane (p) 1 | 14  | Ground          |
| 5   | Ground        | 15  | AUX Ch (p)      |
| 6   | ML Lane (n) 1 | 16  | Ground          |
| 7   | ML Lane (p) 2 | 17  | AUX Ch (n)      |
| 8   | Ground        | 18  | Hot Plug Detect |
| 9   | ML Lane (n) 2 | 19  | DP Power Return |
| 10  | ML Lane (p) 3 | 20  | DP Power        |



# Power and Signal Distribution

## 7.1 Introduction

This chapter describes the power supplies and discusses the methods of general power and signal distribution. Topics covered in this chapter include:

- Power distribution (7.2)
- Power Control (7.3)
- Signal distribution (7.4)

## 7.2 Power Distribution

Each form factor uses a unique power supply assembly and implements different methods of power generation and distribution. The USDT form factor uses an external (“brick”) supply while the SFF and CMT form factors use a power supply unit contained within the system chassis. The subassemblies are not interchangeable between the three form factors.

### 7.2.1 USDT Power Distribution

The USDT form factor uses an external (“brick”) supply that connects to the chassis through a three-conductor cable (Figure 7-1). All voltages required by the processing circuits, peripherals, and storage devices are produced on the system board from the 19.5 VDC produced by the external power supply assembly. The external power supply always produces 19.5 VDC as long as it is connected to an active AC outlet.

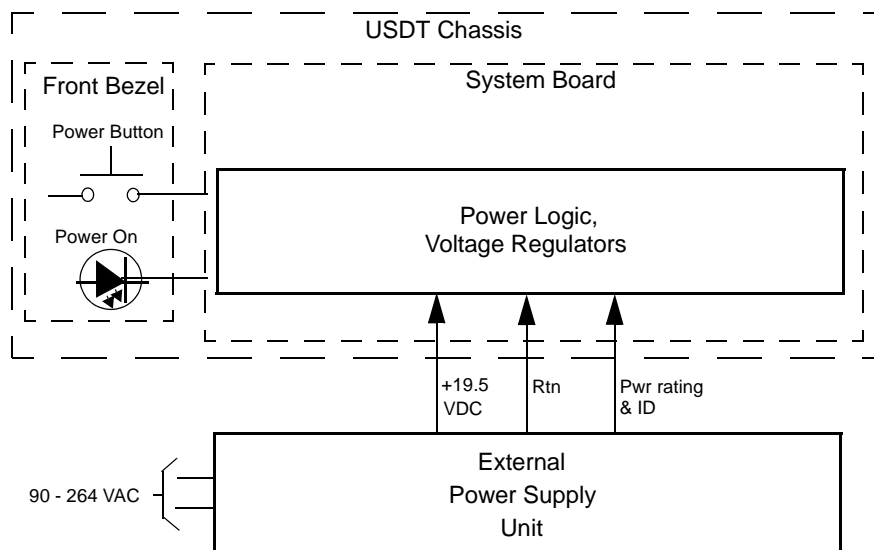


Figure 7-1. USDT Power Generation, Block Diagram

Table 7-1 lists the specifications of the external supply.

**Table 7-1.**  
**USDT 135-Watt Power Supply Unit Specifications**

| Parameter                                  |            |
|--|------------|
| Input Line Voltage Range                   | 90–265 VAC |
| Line Frequency                             | 47–63 Hz   |
| Input Current, Maximum load @ 90 VAC       | 2.4 A      |
| Output Voltage                             | 19.5 VDC   |
| Output Current, nominal load               | 3.5 A      |
| Output Current, maximum load               | 6.9 A      |
| Output Current, peak load (300 ms max) [1] | 9.0 A      |

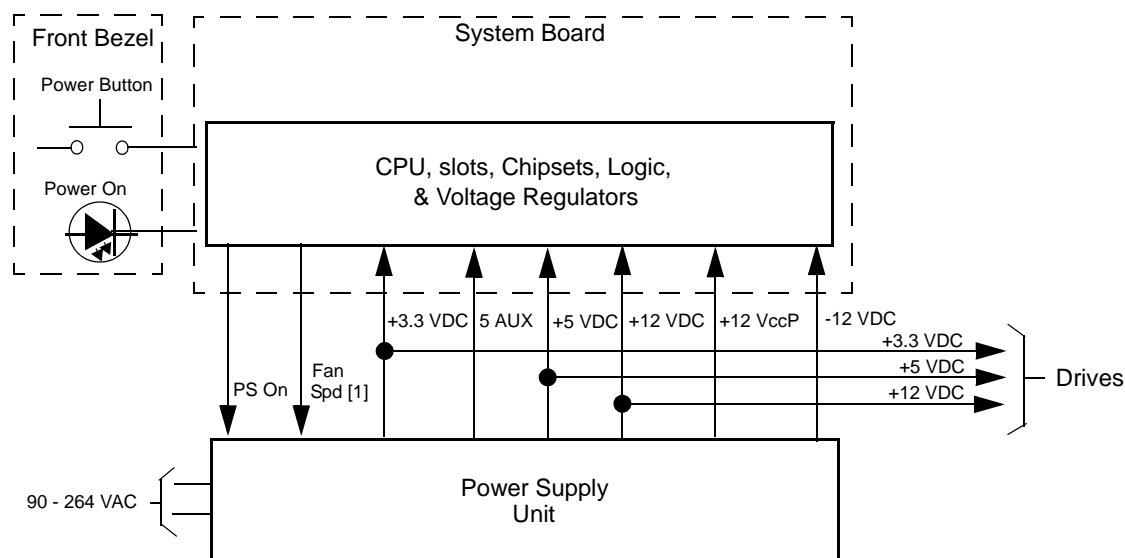
NOTES:

Total continuous power should not exceed 135 watts. Total surge power (<10 seconds w/duty cycle < 5 %) should not exceed 170 watts.

[1] Using 100 VAC input. The output voltage is allowed to drop to a minimum of 15 VDC during the transient period.

## 7.2.2 SFF/CMT Power Distribution

The SFF and CMT form factors use a power supply unit contained within the system chassis. Figure 7-2 shows the block diagram for power generation in the SFF and CMT.



NOTE:

[1] Not present on CMT.

Figure 7-2. SFF Power Generation, Block Diagram

Table 7-2 lists the specifications of the SFF power supply unit.



**Table 7-2.**  
**SFF 240-Watt Power Supply Unit Specifications**

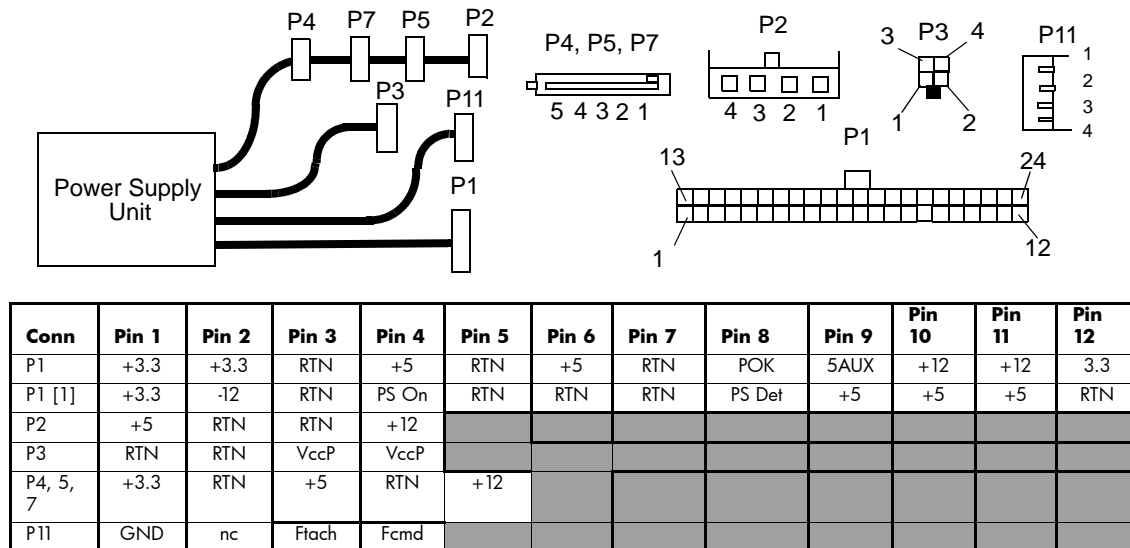
|                       | Range/<br>Tolerance | Min.<br>Current<br>Loading [1] | Max.<br>Current | Surge<br>Current | Max.<br>Ripple |
|-----------------------|---------------------|--------------------------------|-----------------|------------------|----------------|
| Input Line Voltage    | 90–264 VAC          | --                             | --              | --               | --             |
| Line Frequency        | 47–63 Hz            | --                             | --              | --               | --             |
| Input (AC) Current    | --                  | --                             | 5.0 A           | --               | --             |
| +3.3 VDC Output       | ± 4%                | 0.1 A                          | 15.0 A          | 15.0 A           | 50 mV          |
| +5.08 VDC Output      | ± 3.3 %             | 0.3 A                          | 17.0 A          | 17.0 A           | 50 mV          |
| +5.08 AUX Output      | ± 3.3 %             | 0.0 A                          | 3.0 A           | 3.5 A            | 50 mV          |
| +12 VDC Output        | ± 5 %               | 0.1 A                          | 7.5 A           | 9.0 A            | 120 mV         |
| +12 VDC Output (Vcpu) | ± 5 %               | 0.1 A                          | 11.0 A          | 14.5 A           | 120 mv         |
| -12 VDC Output        | ± 10 %              | 0.0 A                          | 0.15 A          | 0.15 A           | 200 mV         |

## NOTES:

Total continuous power should not exceed 240 watts. Total surge power (<10 seconds w/duty cycle < 5 %) should not exceed 260 watts.

[1] The minimum current loading figures apply to a PS On start up only.

Figure 7-3 shows the power supply cabling for the SFF system.



All + and - values are VDC.

RTN = Return (signal ground)

sns = sense

GND = Power ground

RS = Remote sense

FC = Fan command

FO = Fan off

FSpd = Fan speed

FS = Fan Sink

POK = Power OK (power good)

VccP = +12 for CPU

nc = not connected

Fach = Fan speed

Fcmd = Fan command

[1] This row represents pins 13–24 of connector P1

Figure 7-3. SFF Power Cable Diagram

Table 7-3 lists the specifications for the 365-watt power supply used in the CMT form factor.

**Table 7-3.  
CMT 365-Watt Power Supply Unit Specifications**

|   | <b>Range or<br/>Tolerance</b> | <b>Min.<br/>Current<br/>Loading [1]</b> | <b>Max.<br/>Current</b> | <b>Surge<br/>Current [2]</b> | <b>Max.<br/>Ripple</b> |
|---|-------------------------------|---|-------------------------|------------------------------|------------------------|
| Input Line Voltage:<br>115–230 VAC (auto-ranging) | 90–264 VAC                    | --                                      | --                      | --                           | --                     |
| Line Frequency                                    | 47–63 Hz                      | --                                      | --                      | --                           | --                     |
| Input (AC) Current                                | --                            | --                                      | 6.0 A                   | --                           | --                     |
| +3.3 VDC Output                                   | ± 4 %                         | 0.10 A                                  | 24.0 A                  | 24.0 A                       | 50 mV                  |
| +5.08 VDC Output                                  | ± 3.3 %                       | 0.30 A                                  | 19.0 A                  | 19.0 A                       | 50 mV                  |
| +5.08 AUX Output                                  | ± 3.3 %                       | 0.00 A                                  | 3.00 A                  | 3.00 A                       | 50 mV                  |
| +12 VDC Output                                    | ± 5 %                         | 0.20 A                                  | 12.0 A                  | 14.5 A                       | 120 mV                 |
| +12 VDC Output (Vcpu)                             | ± 5 %                         | 0.00 A                                  | 14.5 A                  | 17.5 A                       | 200 mv                 |
| -12 VDC Output                                    | ± 10 %                        | 0.00 A                                  | 0.15 A                  | 0.15 A                       | 200 mV                 |

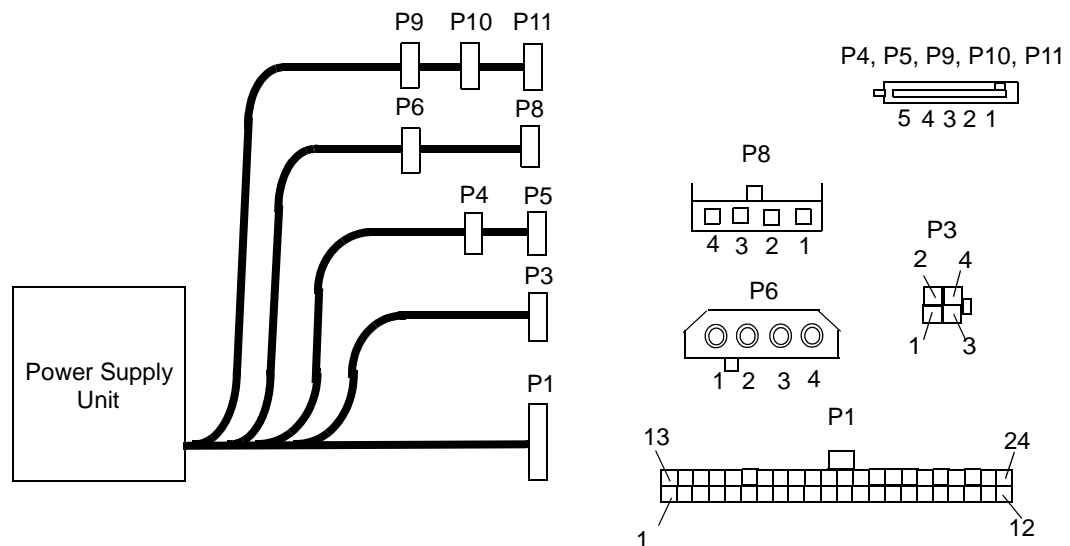
NOTES:

Total continuous output power should not exceed 365 watts. Maximum surge power should not exceed 385 watts.. Maximum combined power of +5 and +3.3 VDC is 160 watts.

[1] Minimum loading requirements must be met at all times to ensure normal operation and specification compliance.

[2] Maximum surge duration for +12Vcpu is 1 second with 12-volt tolerance +/- 10%.

Figure 7-4 shows the power supply cabling for CMT systems.



| Conn             | Pin 1 | Pin 2 | Pin 3 | Pin 4 | Pin 5 | Pin 6 | Pin 7 | Pin 8 | Pin 9 | Pin 10 | Pin 11 | Pin 12 |
|------------------|-------|-------|-------|-------|-------|-------|-------|-------|-------|--------|--------|--------|
| P1               | +3.3  | +3.3  | RTN   | +5    | RTN   | +5    | RTN   | POK   | 5 aux | +12    | +12    | +3.3   |
| P1 [1]           | +3.3  | -12   | RTN   | PS On | RTN   | RTN   | RTN   | PSDef | +5    | +5     | +5     | RTN    |
| P3               | RTN   | RTN   | VccP  | VccP  |       |       |       |       |       |        |        |        |
| P4, 5, 9, 10, 11 | +3.3  | RTN   | +5.08 | RTN   | +12   |       |       |       |       |        |        |        |
| P6               | +12   | RTN   | RTN   | +5    |       |       |       |       |       |        |        |        |
| P8               | +5    | RTN   | RTN   | +12   |       |       |       |       |       |        |        |        |

NOTES:

- Connectors not shown to scale.
- All + and - values are VDC.
- RTN = Return (signal ground)
- GND = Power ground
- RS = Remote sense
- POK = Power ok (power good)
- [1] This row represents pins 13–24 of connector P1.

Figure 7-4. CMT Power Cable Diagram

## 7.2.3 Energy Star Compliance

The standard USDT power supply unit is 87 percent efficient and compliant with the Energy Star 4.0 specification. The standard power supply unit for SFF and CMT systems is Energy Star 3.0-compliant. An Energy Star 4.0 (80Plus Bronze-compliant) power supply unit is available as an option for the SFF and CMT form factors.

## 7.3 Power Control

The generation of +3, +5, and  $\pm 12$  VDC is controlled digitally with the PS On signal. When the PS On signal is asserted, all DC voltages are produced. When PS On is de-asserted, only auxiliary power (+5 AUX) is generated. The +5 AUX voltage is always produced as long as the system is connected to a live AC source.

### 7.3.1 Power Button

The PS On signal is typically controlled through the Power Button which, when pressed and released, applies a negative (grounding) pulse to the power control logic on the system board. The resultant action of pressing the power button depends on the state and mode of the system at that time and is described as follows:

**Table 7-4.**  
**Power Button Actions**

| <b>System State</b> | <b>Pressed Power Button Results In:</b>   |
|---------------------|---|
| Off                 | Negative pulse, of which the falling edge results in power control logic asserting PS On signal to Power Supply Assembly, which then initializes. ACPI four-second counter is not active.   |
| On, ACPI Disabled   | Negative pulse, of which the falling edge causes power control logic to de-assert the PS On signal. ACPI four-second counter is not active.   |
| On, ACPI Enabled    | <p>Pressed and Released Under Four Seconds:<br/>           Negative pulse, of which the falling edge causes power control logic to generate SMI-, set a bit in the SMI source register, set a bit for button status, and start four-second counter. Software should clear the button status bit within four seconds and the Suspend state is entered. If the status bit is not cleared by software in four seconds PS On is de-asserted and the power supply assembly shuts down (this operation is meant as a guard if the OS is hung).</p> <p>Pressed and Held At least Four Seconds Before Release:<br/>           If the button is held in for at least four seconds and then released, PS On is negated, de-activating the power supply.</p> |

A dual-color LED located on the front panel (bezel) is used to indicate system power status. The front panel (bezel) power LED provides a visual indication of key system conditions listed as follows:

**Table 7-5.  
Power LED Indications**

| <b>Power LED</b>               | <b>Condition</b>   |
|--------------------------------|--|
| Steady green                   | Normal full-on operation   |
| Blinks green @ 0.5 Hz          | Suspend state (S1) or suspend to RAM (S3)  |
| Blinks red 2 times @ 1 Hz [1]  | Processor thermal shut down. Check air flow, fan operation, and CPU heat sink.   |
| Blinks red 3 times @ 1 Hz [1]  | Processor not installed. Install or reseat CPU.  |
| Blinks red 4 times @ 1 Hz [1]  | Power failure (power supply is overloaded). Check storage devices, expansion cards and/or system board (CPU power connector P3).   |
| Blinks red 5 times @ 1 Hz [1]  | Pre-video memory error. Incompatible or incorrectly seated DIMM.   |
| Blinks red 6 times @ 1 Hz [1]  | Pre-video graphics error. On system with integrated graphics, check/replace system board. On system with graphics card, check/replace graphics card.   |
| Blinks red 7 times @ 1 Hz [1]  | PCA failure. Check/replace system board.   |
| Blinks red 8 times @ 1 Hz [1]  | Invalid ROM (checksum error). Reflash ROM using CD or replace system board.  |
| Blinks red 9 times @ 1 Hz [1]  | System powers on but fails to boot. Check power supply, CPU, system board.   |
| Blinks red 10 times @ 1 Hz [1] | Bad option card.   |
| No light                       | System dead. Press and hold power button for <b>less</b> than 4 seconds. If HD LED turns green then check voltage select switch setting or expansion cards. If no LED light then check power button/power supply cables to system board or system board. |

NOTE:

[1] Will be accompanied by the same number of beeps, with 2-second pause between cycles. Beeps stop after 5 cycles.

## 7.3.2 Wake Up Events

The PS On signal can be activated with a power “wake-up” of the system due to the occurrence of a magic packet, serial port ring, or PCI power management event (PME). These events can be individually enabled through the Setup utility to wake up the system from a sleep (low power) state.



---

Wake-up functionality requires that certain circuits receive auxiliary power while the system is turned off. The system unit must be plugged into a live AC outlet for wake up events to function. Using an AC power strip to control system unit power will disable wake-up event functionality.

---

The wake up sequence for each event occurs as follows:

### **Wake-On-LAN**

The network interface controller (NIC) can be configured for detection of a “Magic Packet” and wake the system up from sleep mode through the assertion of the PME- signal on the PCI bus. Refer to Chapter 5, “Network Support” for more information.

### **Modem Ring**

A ring condition on a serial port can be detected by the power control logic and, if so configured, cause the PS On signal to be asserted.

### **Power Management Event**

A power management event that asserts the PME- signal on the PCI bus can be enabled to cause the power control logic to generate the PS On. Note that the PCI card must be PCI ver. 2.2 (or later) compliant to support this function.

### 7.3.3 Power Management

These systems include power management functions designed to conserve energy. These functions are provided by a combination of hardware, firmware (BIOS) and software. The system provides the following power management support:

- ACPI v2.0 compliant (ACPI modes C1, S1, and S3-S5)
- APM 1.2 compliant
- U.S. EPA Energy Star 3.0 and 4.0 compliant

Table 7-6 shows the comparison in power states.

**Table 7-6.  
System Power States**

| <b>Power State</b>                    | <b>System Condition</b>   | <b>Power Consumption</b> | <b>Transition To S0 by [2]</b>                                   | <b>OS Restart Required</b> |
|---------------------------------------|---|--------------------------|--|----------------------------|
| G0, S0, D0                            | System fully on. OS and application is running, all components.   | Maximum                  | N/A  | No                         |
| G1, S1, C1, D1                        | System on, CPU is executing and data is held in memory. Some peripheral subsystems may be on low power. Monitor is blanked. | Low                      | < 2 sec after keyboard or pointing device action                 | No                         |
| G1, S2/3, C2, D2 (Standby/or suspend) | System on, CPU not executing, cache data lost. Memory is holding data, display and I/O subsystems on low power.             | Low                      | < 5 sec. after keyboard, pointing device, or power button action | No                         |
| G1, S4, D3 (Hibernation)              | System off. CPU, memory, and most subsystems shut down. Memory image saved to disk for recall on power up.                  | Low                      | <25 sec. after power button action                               | Yes                        |
| G2, S5, D3 <sub>cold</sub>            | System off. All components either completely shut down or receiving minimum power to perform system wake-up.                | Minimum                  | <35 sec. after power button action                               | Yes                        |
| G3                                    | System off (mechanical). No power to any internal components except RTC circuit. [1]  | None                     | —  | —                          |

**NOTES:**

G<sub>n</sub> = Global state.

S<sub>n</sub> = Sleep state.

C<sub>n</sub> = ACPI state.

D<sub>n</sub> = PCI state.

[1] Power cord is disconnected for this condition.

[2] Actual transition time dependent on OS and/or application software.

## 7.4 Signal Distribution

Table 7-7 lists the reference designators for LEDs, connectors, headers, and switches used on the system boards for systems covered in this guide. Unless otherwise indicated, components are used on all system boards.

**Table 7-7.**  
**System Board Component Designations**

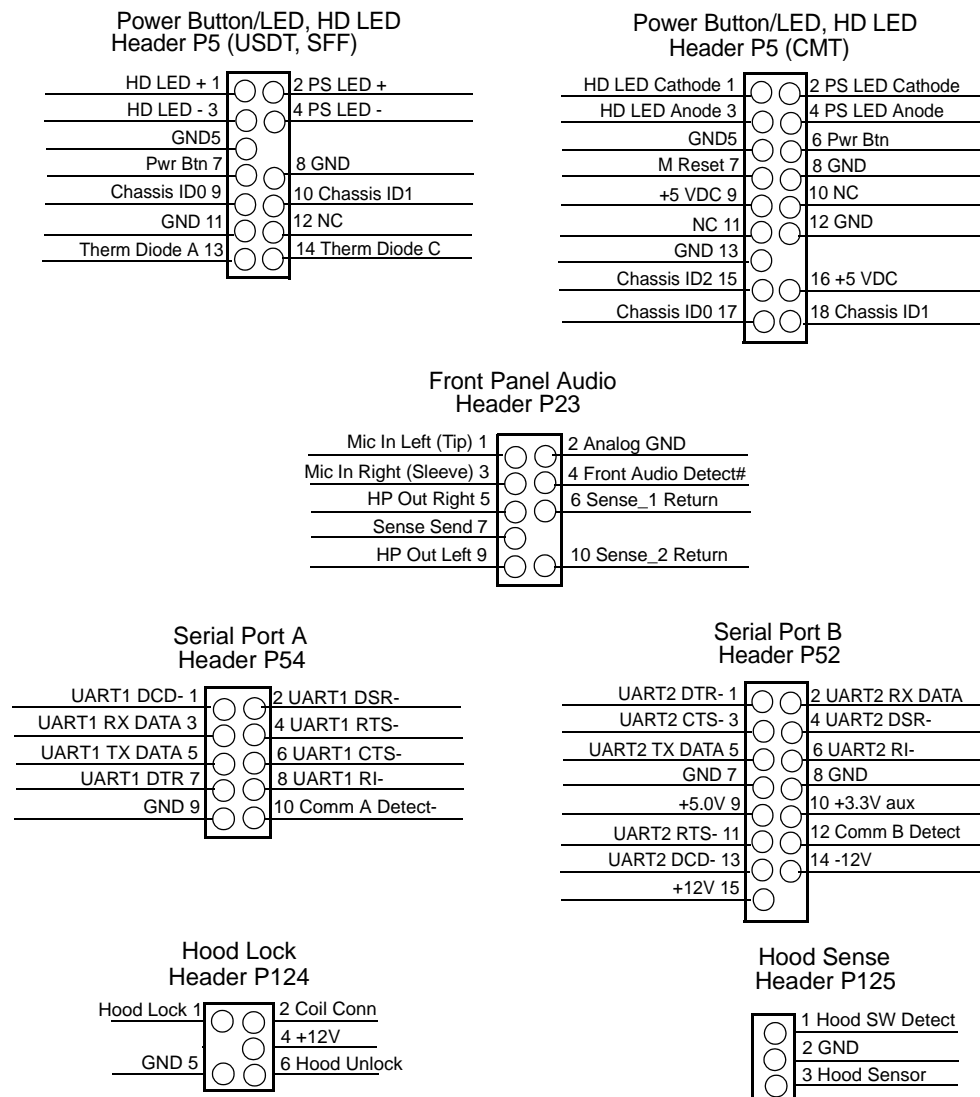
| <b>Designator</b> | <b>Component function</b>                                      | <b>Notes</b>     |
|-------------------|--|------------------|
| CR1               | +5 VDC LED   |                  |
| E1                | Descriptor table override header                               |                  |
| E14               | SPI ROM boot block header                                      |                  |
| E49 / JP49        | Password clear header / jumper                                 |                  |
| J9                | Stacked RJ-45 & dual USB connectors                            |                  |
| J10               | Stacked quad USB connectors                                    |                  |
| J20               | PCI 2.3 connector  | SFF & CMT only   |
| J21               | PCI 2.3 connector  | CMT only         |
| J22               | PCI 2.3 connector  | CMT only         |
| J31               | PCIe x1 connector  | SFF & CMT only   |
| J32               | PCIe x1 connector  | SFF & CMT only   |
| J41               | PCIe x16 graphics connector                                    | SFF & CMT only   |
| J42               | PCIe x4 graphics (x16) connector                               | SFF & CMT only   |
| J50               | Parallel port  | SFF & CMT only   |
| J68               | Stacked keyboard, mouse PS/2 connectors                        |                  |
| J69               | VGA monitor DB-15 connector                                    |                  |
| J78               | Stacked audio line-in, headphone/line-out 1/8" jacks           |                  |
| J103              | DC input   | USDT only        |
| P1                | Power supply connector   | SFF & CMT only   |
| P3                | Vccp (PWRCPU) header   |                  |
| P5                | Control panel (power button, power LED) header                 |                  |
| P6                | Internal speaker header  |                  |
| P8                | CPU fan header   |                  |
| P9                | Chassis fan, primary, header                                   |                  |
| P10               | Diskette drive connector                                       | SFF & CMT only   |
| P23               | Front panel audio header                                       |                  |
| P24               | Front panel USB header   |                  |
| P52               | Serial port, secondary, header                                 | SFF & CMT only   |
| P53               | Serial port, primary connector                                 | SFF & CMT only   |
| P54               | Serial port, primary header                                    | SFF only         |
| P60               | SATA0 (controller 1, primary master) connector (dark blue)     |                  |
| P61               | SATA1 (controller 1, secondary master) connector (white)       | SFF & CMT only   |
| P62               | SATA2 (controller 1, primary slave) connector (light blue)     | SFF & CMT only   |
| P63               | SATA3 (controller 1, secondary slave) connector (orange)       | CMT only         |
| P64               | SATA4 / eSATA (controller 2, primary master) connector (black) | SFF & CMT only   |
| P124              | Hood lock header   | SFF & CMT only   |
| P125              | Hood sense header  |                  |
| P126              | Parallel port header   | SFF and CMT only |
| P150              | Media reader header  |                  |
| P151              | Ready boost / dash NIC header                                  |                  |



**Table 7-7. (Continued)**  
**System Board Component Designations**

|      |                     |                |
|------|---------------------|----------------|
| SW50 | Clear CMOS switch   |                |
| XMM1 | Memory slot (black) |                |
| XMM2 | Memory slot (white) |                |
| XMM3 | Memory slot (white) | SFF & CMT only |
| XMM4 | Memory slot (white) | SFF & CMT only |
| XU1  | Processor socket    |                |
| XB2  | Battery socket      |                |

Figure 7-5 shows pinouts of headers used on the system boards.



**NOTE:**

No polarity consideration required for connection to speaker header P6.

NC = Not connected

Figure 7-5. System Board Header Pinouts



## 8.1 Introduction

The System Basic Input/Output System (BIOS) of the computer is a collection of machine language programs stored as firmware in read-only memory (ROM). The system BIOS includes such functions as Power-On Self Test (POST), PCI device initialization, Plug 'n Play support, power management activities, and the Setup utility. The firmware contained in the system BIOS ROM supports the following operating systems and specifications:

- DOS 6.2, Windows 2000, XP, and Vista (Home and Professional versions)
- Windows NT 4.0 (SP6 required for PnP support)
- OS/2 ver 2.1 and OS/2 Warp
- SCO Unix
- DMI 2.1
- Intel Wired for Management (WfM) ver. 2.2
- Alert Standard Format (ASF) 2.0
- ACPI and OnNow
- SMBIOS 2.5
- Intel PXE boot ROM for the integrated LAN controller
- BIOS Boot Specification 1.01
- Enhanced Disk Drive Specification 3.0
- “El Torito” Bootable CD-ROM Format Specification 1.0
- ATAPI Removeable Media Device BIOS Specification 1.0
- Serial ATA Advanced Host Controller Interface (AHCI) 1.2
- ATA with Packet Interface (ATA/ATAPI-7)

The BIOS firmware is contained in a 32 Mb flash ROM part. The runtime portion of the BIOS resides in a 128KB block from E0000h to FFFFh.

This chapter includes the following topics:

- ROM flashing (8.2)
- Boot functions (8.3)
- Client management functions (8.4)
- SMBIOS support (8.5)
- USB legacy support (8.6)
- Management engine functions (8.7)

## 8.2 ROM Flashing

The system BIOS firmware is contained in a flash ROM device that can be re-written with new BIOS code using a flash utility locally (with F10 setup), with the HPQFlash program in a Windows environment, or with the FLASHBIN.EXE utility in a DOS or DOS-like environment.

### 8.2.1 Upgrading

Upgrading the BIOS is not normally required but may be necessary if changes are made to the unit's operating system, hard drive, or processor. All System BIOS upgrades are available directly from HP. Flashing is done either locally through F10 setup, the HPQFlash program in a Windows environment, or with the FLASHBIN.EXE utility in a DOS or DOS-like environment. Flashing may also be done by deploying either HPQFlash or FLASHBIN.EXE through the network boot function.

This system includes 64 KB of write-protected boot block ROM that provides a way to recover from a failed flashing of the system BIOS ROM. If the system BIOS ROM fails the flash check, the boot block code provides the minimum amount of support necessary to allow booting the system and re-flashing the system BIOS ROM with a CD or USB disk/thumb drive.

### 8.2.2 Changeable Splash Screen



---

A corrupted splash screen may be restored by reflashing the BIOS image through F10 setup, running HPQFlash, or running FLASHBIN.EXE. Depending on the system, changing (customizing) the splash screen may only be available with assistance from HP.

---

The splash screen (image displayed during POST) is stored in the system BIOS ROM and may be replaced with another image of choice by using the Image Flash utility (Flashi.exe). The Image Flash utility allows the user to browse directories for image searching and pre-viewing. Background and foreground colors can be chosen from the selected image's palette.

The splash screen image requirements are as follows:

- Format = Windows bitmap with 4-bit RLE encoding
- Size = 424 (width) x 320 (height) pixels
- Colors = 16 (4 bits per pixel)
- File Size = < 64 KB

The Image Flash utility can be invoked at a command line for quickly flashing a known image as follows:

```
>\Flashi.exe [Image_Filename] [Background_Color] [Foreground_Color]
```

The utility checks to insure that the specified image meets the splash screen requirements listed above or it will not be loaded into the ROM.

## 8.3 Boot Functions

The BIOS supports various functions related to the boot process, including those that occur during the Power On Self-Test (POST) routine.

### 8.3.1 Boot Device Order

The default boot device order is as follows:

1. CD-ROM drive (EL Torito CD images)
2. Diskette drive (A:)
3. USB device
4. Hard drive (C:)
5. Network interface controller (NIC)



The above order assumes all devices are present in the initial configuration. If, for example, a diskette drive is not initially installed but added later, then drive A would be added to the end of the order (after the NIC)

The order can be changed in the ROM-based Setup utility (accessed by pressing F10 when so prompted during POST). The options are displayed only if the device is attached, except for USB devices. The USB option is displayed even if no USB storage devices are present. The hot IPL option is available through the F9 utility, which allows the user to select a hot IPL boot device.

### 8.3.2 Network Boot (F12) Support

The BIOS supports booting the system to a network server. The function is accessed by pressing the F12 key when prompted at the lower right hand corner of the display during POST. Booting to a network server allows for such functions as:

- Flashing a ROM on a system without a functional operating system (OS).
- Installing an OS.
- Installing an application.

These systems include, as standard, an integrated Intel 82562-equivalent NIC with Preboot Execution Environment (PXE) ROM and can boot with a NetPC-compliant server.

### 8.3.3 Memory Detection and Configuration

This system uses the Serial Presence Detect (SPD) method of determining the installed DIMM configuration. The BIOS communicates with an EEPROM on each DIMM through the SMBus to obtain data on the following DIMM parameters:

- Presence
- Size
- Type
- Timing/CAS latency



Refer to Chapter 3, “Processor/Memory Subsystem” for the SPD format and DIMM data specific to this system.

The BIOS performs memory detection and configuration with the following steps:

1. Program the buffer strength control registers based on SPD data and the DIMM slots that are populated.
2. Determine the common CAS latency that can be supported by the DIMMs.
3. Determine the memory size for each DIMM and program the GMCH accordingly.
4. Enable refresh.

### 8.3.4 Boot Error Codes

The BIOS provides visual and audible indications of a failed system boot by using the system's power LED and the system board speaker. The error conditions are listed in the following table.

**Table 8-1**  
**Boot Error Codes**

| <b>Visual (power LED)</b>  | <b>Audible (speaker)</b> | <b>Meaning</b>   |
|----------------------------|--------------------------|--|
| Blinks red 2 times @ 1 Hz  | 2 beeps                  | Processor thermal shut down. Check air flow, fan operation, and CPU heat sink.   |
| Blinks red 3 times @ 1 Hz  | 3 beeps                  | Processor not installed. Install or reseal CPU.  |
| Blinks red 4 times @ 1 Hz  | None                     | Power failure (power supply is overloaded). Check storage devices, expansion cards and/or system board (CPU power connector P3).                     |
| Blinks red 5 times @ 1 Hz  | 5 beeps                  | Pre-video memory error. Incompatible or incorrectly seated DIMM.   |
| Blinks red 6 times @ 1 Hz  | 6 beeps                  | Pre-video graphics error. On system with integrated graphics, check/replace system board. On system with graphics card, check/replace graphics card. |
| Blinks red 7 times @ 1 Hz  | 7 beeps                  | PCA failure. Check/replace system board.   |
| Blinks red 8 times @ 1 Hz  | 8 beeps                  | Invalid ROM (checksum error). Reflash ROM using CD or replace system board.  |
| Blinks red 9 times @ 1 Hz  | 9 beeps                  | System powers on but fails to boot. Check power supply, CPU, system board.   |
| Blinks red 10 times @ 1 Hz | 10 beeps                 | Bad option card.   |

NOTE: Audible indications occur only for the five cycles of the error indication. Visual indications occur indefinitely until power is removed or until error is corrected.

## 8.4 Client Management Functions

Table 8-2 provides a partial list of the client management BIOS functions supported by the systems covered in this guide. These functions, designed to support intelligent manageability applications, are HP-specific unless otherwise indicated.

**Table 8-2.**  
**Client Management Functions (INT15)**

| <b>AX</b> | <b>Function</b>             | <b>Mode</b>               |
|-----------|-----------------------------|---------------------------|
| E800h     | Get system ID               | Real, 16-, & 32-bit Prot. |
| E813h     | Get monitor data            | Real, 16-, & 32-bit Prot. |
| E814h     | Get system revision         | Real, 16-, & 32-bit Prot. |
| E816h     | Get temperature status      | Real, 16-, & 32-bit Prot. |
| E819h     | Get chassis serial number   | Real, 16-, & 32-bit Prot. |
| E820h [1] | Get system memory map       | Real                      |
| E81Ah     | Write chassis serial number | Real                      |
| E827h     | DIMM EEPROM Access          | Real, 16-, & 32-bit Prot. |

NOTE:

[1] Industry standard function.

All 32-bit protected-mode functions are accessed by using the industry-standard BIOS32 Service Directory. Using the service directory involves three steps:

1. Locating the service directory.
2. Using the service directory to obtain the entry point for the client management functions.
3. Calling the client management service to perform the desired function.

The BIOS32 Service Directory is a 16-byte block that begins on a 16-byte boundary between the physical address range of 0E0000h-0FFFFFh.

The following subsections provide a brief description of key Client Management functions.

## 8.4.1 System ID and ROM Type

Diagnostic applications can use the INT 15, AX=E800h BIOS function to identify the type of system. This function will return the system ID in the BX register. Systems have the following IDs and ROM family types:

---

**Table 8-3**  
**System ID Numbers**

---

| <b>System (Form Factor)</b> | <b>System ID</b> | <b>Subsystem Device ID</b> |
|-----------------------------|------------------|----------------------------|
| USDT                        | 3033h            | 3036h                      |
| SFF                         | 3031h            | 3034h                      |
| CMT:                        | 3032h            | 3035h                      |

---

NOTE: For all systems, BIOS ROM Family = 786G1, PnP ID = CPQ0968, and Subsystem vendor ID = 103Ch. The ROM family and version numbers can be verified with the Setup utility or the System Insight Manager or Diagnostics applications.

## 8.4.2 Temperature Status

The BIOS includes a function (INT15, AX=E816h) to retrieve the status of a system's interior temperature. This function allows an application to check whether the temperature situation is at a Normal, Caution, or Critical condition.



## 8.5 SMBIOS

In support of the DMI specification, PnP functions 50h and 51h are used to retrieve the SMBIOS data. Function 50h retrieves the number of structures, size of the largest structure, and SMBIOS version. Function 51h retrieves a specific structure. This system supports SMBIOS version 2.5 and the structure types listed in the following table:

**Table 8-3**  
**SMBIOS Functions**

| Type | Data                               |
|------|------------------------------------|
| 0    | BIOS Information                   |
| 1    | System Information                 |
| 2    | Base board information             |
| 3    | System Enclosure or Chassis        |
| 4    | Processor Information              |
| 7    | Cache Information                  |
| 8    | Port Connector Information         |
| 9    | System Slots                       |
| 13   | BIOS Language Information          |
| 15   | System Event Log Information       |
| 16   | Physical Memory Array              |
| 17   | Memory Devices                     |
| 19   | Memory Array Mapped Addresses      |
| 20   | Memory Device Mapped Addresses     |
| 24   | Cooling Device Structure           |
| 27   | Hardware Security Structure        |
| 31   | Boot Integrity Service Entry Point |
| 32   | System Boot Information            |



System information on these systems is handled exclusively through the SMBIOS.

## 8.6 USB Legacy Support

The system BIOS ROM checks the USB port, during POST, for the presence of a USB keyboard. This allows a system with only a USB keyboard to be used during ROM-based setup and also on a system with an OS that does not include a USB driver.

On such a system a keystroke will generate an SMI and the SMI handler will retrieve the data from the device and convert it to PS/2 data. The data will be passed to the keyboard controller and processed as in the PS/2 interface. Changing the delay and/or typematic rate of a USB keyboard though BIOS function INT 16 is not supported.

## 8.7 Management Engine Functions

The management engine function of Intel AMT allows a system unit to be managed remotely over a network, where or not the system is powered up or not<sup>1</sup>. The system BIOS can request the management engine to generate the following alerts:

- Temperature alert
- Fan failure alert
- Chassis intrusion alert
- Watchdog timer alert
- No memory installed alert

---

1.Assumes the unit is connected to an active AC outlet.

# Error Messages and Codes

## A.1 Introduction

This appendix lists the error codes and a brief description of the probable cause of the error.



Errors listed in this appendix are applicable only for systems running HP/Compaq BIOS. Not all errors listed in this appendix may be applicable to a particular system model and/or configuration.

## A.2 Beep/Power LED Codes



Beep and Power LED indications listed in Table A-1 apply only to HP-branded models.

**Table A-1.**  
**Beep/Power LED Codes**

| Beeps    | Power LED                  | Probable Cause   |
|----------|----------------------------|--|
| 2 beeps  | Blinks red 2 times @ 1 Hz  | Processor thermal shut down. Check air flow, fan operation, and CPU heatsink   |
| 3 beeps  | Blinks red 3 times @ 1 Hz  | Processor not installed. Install or reseal CPU.  |
| 4 beeps  | Blinks red 4 times @ 1 Hz  | Power failure (power supply is overloaded). Check storage devices, expansion cards and/or system board (CPU power connector P3).                     |
| 5 beeps  | Blinks red 5 times @ 1 Hz  | Pre-video memory error. Incompatible or incorrectly seated DIMM.   |
| 6 beeps  | Blinks red 6 times @ 1 Hz  | Pre-video graphics error. On system with integrated graphics, check/replace system board. On system with graphics card, check/replace graphics card. |
| 7 beeps  | Blinks red 7 times @ 1 Hz  | PCA failure. Check/replace system board.   |
| 8 beeps  | Blinks red 8 times @ 1 Hz  | Invalid ROM (checksum error). Reflash ROM using CD or replace system board.  |
| 9 beeps  | Blinks red 9 times @ 1 Hz  | System powers on but fails to boot. Check power supply, CPU, system board.   |
| 10 beeps | Blinks red 10 times @ 1 Hz | Bad option card.   |

NOTE: Audible indications occur only for the first five cycles of the error indication. Visual indications occur indefinitely until power is removed or until error is corrected.

## A.3 Power-On Self Test (POST) Messages

**Table A-2.**  
**Power-On Self Test (POST) Messages**

| <b>Error Message</b>  | <b>Probable Cause</b>  |
|---|--|
| Invalid Electronic Serial Number  | Chassis serial number is corrupt. Use Setup to enter a valid number.                 |
| Network Server Mode Active (w/o kybd)                                     | System is in network mode.   |
| 101-Option ROM Checksum Error   | A device's option ROM has failed/is bad.   |
| 110-Out of Memory Space for Option ROMs                                   | Recently added PCI card contains and option ROM too large to download during POST.   |
| 102-system Board Failure  | Failed ESCD write, A20, timer, or DMA controller.                                    |
| 150-Safe POST Active  | An option ROM failed to execute on a previous boot.                                  |
| 162-System Options Not Set  | Invalid checksum, RTC lost power, or invalid configuration.                          |
| 163-Time & Date Not Set   | Date and time information in CMOS is not valid.                                      |
| 164-Memory Size Error   | Memory has been added or removed.  |
| 201-Memory Error  | Memory test failed.  |
| 213-Incompatible Memory Module  | BIOS detected installed DIMM(s) as being not compatible.                             |
| 214-DIMM Configuration Warning  | A specific error has occurred in a memory device installed in the identified socket. |
| 216-Memory Size Exceeds Max   | Installed memory exceeds the maximum supported by the system.                        |
| 217-DIMM Configuration Warning  | Unbalanced memory configuration.   |
| 219-ECC Memory Module Detected ECC Modules not supported on this platform | Recently added memory module(s) support ECC memory error correction.                 |
| 301-Keyboard Error  | Keyboard interface test failed (improper connection or stuck key).                   |
| 303-Keyboard Controller Error   | Keyboard buffer failed empty (8042 failure or stuck key).                            |
| 304-Keyboard/System Unit Error  | Keyboard controller failed self-test.  |
| 404-Parallel Port Address Conflict  | Current parallel port address is conflicting with another device.                    |
| 417-Network Interface Card Failure  | NIC BIOS could not read Device ID of embedded NIC.                                   |
| 501-Display Adapter Failure   | Graphics display controller.   |
| 510-Splash Image Corrupt  | Corrupted splash screen image. Restore default image w/flash utility.                |
| 511-CPU Fan Not Detected  | Processor heat sink fan is not connected.  |
| 512-Chassis Fan Not Detected  | Chassis fan is not connected.  |

**Table A-2. (Continued)**  
**Power-On Self Test (POST) Messages**

| <b>Error Message</b>   | <b>Probable Cause</b>   |
|--|---|
| 514-CPU or Chassis Fan not detected.   | CPU fan is not connected or may have malfunctioned.   |
| 601-Diskette Controller Error  | Diskette drive removed since previous boot.   |
| 605-Diskette Drive Type Error  | Mismatch in drive type.   |
| 912-Computer Cover Removed Since Last System Start Up                                      | Cover (hood) removal has been detected by the Smart Cover Sensor.   |
| 914-Hood Lock Coil is not Connected  | Smart Cover Lock mechanism is missing or not connected.   |
| 916-Power Button Not Connected   | Power button harness has been detached or unseated from the system board.   |
| 917-Expansion Riser Not Detected   | Expansion (backplane) board not seated properly.  |
| 919-Front Panel, MultiPort, and/or MultiBay Risers not Detected                            | Riser card has been removed or has not been reinstalled properly in the system.   |
| 1156-Serial Port A Cable Not Detected  | Cable from serial port header to I/O connector is missing or not connected properly.  |
| 1157-Front Cables Not Detected   | Cable from front panel USB and audio connectors is missing or not connected properly.   |
| 1720-SMART Hard Drive Detects Imminent Failure   | SMART circuitry on an IDE drive has detected possible equipment failure.  |
| 1721-SMART SCSI Hard Drive Detects Imminent Failure  | SMART circuitry on a SCSI drive has detected possible equipment failure.  |
| 1785-MultiBay incorrectly installed  | <b>For integrated MultiBay/ USDT systems:</b><br>MultiBay device not properly seated.<br>or<br>MultiBay riser not properly seated.  |
| 1794-Inaccessible device attached to SATA 1<br>(for systems with 2 SATA ports)             | A device is attached to SATA 1. Any device attached to this connector will be inaccessible while "SATA Emulation" is set to "Combined IDE Controller" in Computer Setup.                |
| 1794-Inaccessible devices attached to SATA 1 and/or SATA 5 (for systems with 4 SATA ports) | A device is attached to SATA 1 and/or SATA 5.<br>Devices attached to these connectors will be inaccessible while "SATA Emulation" is set to "Combined IDE Controller" in Computer Setup |
| 1796-SATA Cabling Error  | One or more SATA devices are improperly attached. For optimal performance, the SATA 0 and SATA 1 connectors must be used before SATA 2 and SATA 3.                                      |

**Table A-2. (Continued)**  
**Power-On Self Test (POST) Messages**

| <b>Error Message</b>                                | <b>Probable Cause</b>  |
|---|--|
| 1801-Microcode Patch Error                          | A processor is installed for which the BIOS ROM has no patch.<br>Check for ROM update. |
| Invalid Electronic Serial Number                    | Electronic serial number has become corrupted.   |
| Network Server Mode Active and No Keyboard Attached | Keyboard failure while Network Server Mode enabled.                                    |
| Parity Check 2                                      | Keyboard failure while Network Server Mode enabled.                                    |

## A.4 System Error Messages (1xx-xx)

**Table A-3.**  
**System Error Messages**

| <b>Message</b> | <b>Probable Cause</b>               | <b>Message</b> | <b>Probable Cause</b>                    |
|----------------|-------------------------------------|----------------|--|
| 101            | Option ROM error                    | 109-02         | CMOS clock rollover test failed          |
| 102            | System board failure [1]            | 109-03         | CMOS not properly initialized (clk test) |
| 103            | System board failure                | 110-01         | Programmable timer load data test failed |
| 104-01         | Master int. cntlr. test failed      | 110-02         | Programmable timer dynamic test failed   |
| 104-02         | Slave int. cntlr. test failed       | 110-03         | Program timer 2 load data test failed    |
| 104-03         | Int. cntlr. SW RTC inoperative      | 111-01         | Refresh detect test failed               |
| 105-01         | Port 61 bit <6> not at zero         | 112-01         | Speed test Slow mode out of range        |
| 105-02         | Port 61 bit <5> not at zero         | 112-02         | Speed test Mixed mode out of range       |
| 105-03         | Port 61 bit <3> not at zero         | 112-03         | Speed test Fast mode out of range        |
| 105-04         | Port 61 bit <1> not at zero         | 112-04         | Speed test unable to enter Slow mode     |
| 105-05         | Port 61 bit <0> not at zero         | 112-05         | Speed test unable to enter Mixed mode    |
| 105-06         | Port 61 bit <5> not at one          | 112-06         | Speed test unable to enter Fast mode     |
| 105-07         | Port 61 bit <3> not at one          | 112-07         | Speed test system error                  |
| 105-08         | Port 61 bit <1> not at one          | 112-08         | Unable to enter Auto mode in speed test  |
| 105-09         | Port 61 bit <0> not at one          | 112-09         | Unable to enter High mode in speed test  |
| 105-10         | Port 61 I/O test failed             | 112-10         | Speed test High mode out of range        |
| 105-11         | Port 61 bit <7> not at zero         | 112-11         | Speed test Auto mode out of range        |
| 105-12         | Port 61 bit <2> not at zero         | 112-12         | Speed test variable speed mode inop.     |
| 105-13         | No int. generated by failsafe timer | 113-01         | Protected mode test failed               |
| 105-14         | NMI not triggered by timer          | 114-01         | Speaker test failed                      |
| 106-01         | Keyboard controller test failed     | 116-xx         | Way 0 read/write test failed             |
| 107-01         | CMOS RAM test failed                | 162-xx         | Options failed (mismatch in drive type)  |
| 108-02         | CMOS interrupt test failed          | 163-xx         | Time and date not set                    |
| 108-03         | CMOS not properly initialized       | 164-xx         | Memory size                              |
| 109-01         | CMOS clock load data test failed    | 199-00         | Installed devices test failed            |

NOTES:

[1] 102 message code may be caused by one of a variety of processor-related problems that may be solved by replacing the processor, although system board replacement may be needed.

## A.5 Memory Error Messages (2xx-xx)

**Table A-4.**  
**Memory Error Messages**

| <b>Message</b> | <b>Probable Cause</b>                                      |
|----------------|--|
| 200-04         | Real memory size changed                                   |
| 200-05         | Extended memory size changed                               |
| 200-06         | Invalid memory configuration                               |
| 200-07         | Extended memory size changed                               |
| 200-08         | CLIM memory size changed                                   |
| 201-01         | Memory machine ID test failed                              |
| 202-01         | Memory system ROM checksum failed                          |
| 202-02         | Failed RAM/ROM map test                                    |
| 202-03         | Failed RAM/ROM protect test                                |
| 203-01         | Memory read/write test failed                              |
| 203-02         | Error while saving block in read/write test                |
| 203-03         | Error while restoring block in read/write test             |
| 204-01         | Memory address test failed                                 |
| 204-02         | Error while saving block in address test                   |
| 204-03         | Error while restoring block in address test                |
| 204-04         | A20 address test failed                                    |
| 204-05         | Page hit address test failed                               |
| 205-01         | Walking I/O test failed                                    |
| 205-02         | Error while saving block in walking I/O test               |
| 205-03         | Error while restoring block in walking I/O test            |
| 206-xx         | Increment pattern test failed                              |
| 207-xx         | ECC failure  |
| 210-01         | Memory increment pattern test                              |
| 210-02         | Error while saving memory during increment pattern test    |
| 210-03         | Error while restoring memory during increment pattern test |
| 211-01         | Memory random pattern test                                 |



**Table A-4. (Continued)  
Memory Error Messages**

| <b>Message</b> | <b>Probable Cause</b>  |
|----------------|--|
| 211-02         | Error while saving memory during random memory pattern test    |
| 211-03         | Error while restoring memory during random memory pattern test |
| 213-xx         | Incompatible DIMM in slot x                                    |
| 214-xx         | Noise test failed  |
| 215-xx         | Random address test  |

## A.6 Keyboard Error Messages (30x-xx)

**Table A-5.  
Keyboard Error Messages**

| <b>Message</b> | <b>Probable Cause</b>                  | <b>Message</b> | <b>Probable Cause</b>                      |
|----------------|--|----------------|--|
| 300-xx         | Failed ID test                         | 303-05         | LED test, LED command test failed          |
| 301-01         | Kybd short test, 8042 self-test failed | 303-06         | LED test, LED command test failed          |
| 301-02         | Kybd short test, interface test failed | 303-07         | LED test, LED command test failed          |
| 301-03         | Kybd short test, echo test failed      | 303-08         | LED test, command byte restore test failed |
| 301-04         | Kybd short test, kybd reset failed     | 303-09         | LED test, LEDs failed to light             |
| 301-05         | Kybd short test, kybd reset failed     | 304-01         | Keyboard repeat key test failed            |
| 302-xx         | Failed individual key test             | 304-02         | Unable to enter mode 3                     |
| 302-01         | Kybd long test failed                  | 304-03         | Incorrect scan code from keyboard          |
| 303-01         | LED test, 8042 self-test failed        | 304-04         | No Make code observed                      |
| 303-02         | LED test, reset test failed            | 304-05         | Cannot /disable repeat key feature         |
| 303-03         | LED test, reset failed                 | 304-06         | Unable to return to Normal mode            |
| 303-04         | LED test, LED command test failed      | --             | --   |

## A.7 Printer Error Messages (4xx-xx)

**Table A-6**  
**Printer Error Messages**

| <b>Message</b> | <b>Probable Cause</b>                  | <b>Message</b> | <b>Probable Cause</b>                               |
|----------------|--|----------------|---|
| 401-01         | Printer failed or not connected        | 402-11         | Interrupt test, data/cntrl. reg. failed             |
| 402-01         | Printer data register failed           | 402-12         | Interrupt test and loopback test failed             |
| 402-02         | Printer control register failed        | 402-13         | Int. test, LpBk. test., and data register failed    |
| 402-03         | Data and control registers failed      | 402-14         | Int. test, LpBk. test., and cntrl. register failed  |
| 402-04         | Loopback test failed                   | 402-15         | Int. test, LpBk. test., and data/cntrl. reg. failed |
| 402-05         | Loopback test and data reg. failed     | 402-16         | Unexpected interrupt received                       |
| 402-06         | Loopback test and cntrl. reg. failed   | 402-01         | Printer pattern test failed                         |
| 402-07         | Loopback test, data/cntrl. reg. failed | 403-xx         | Printer pattern test failed                         |
| 402-08         | Interrupt test failed                  | 404-xx         | Parallel port address conflict                      |
| 402-09         | Interrupt test and data reg. failed    | 498-00         | Printer failed or not connected                     |
| 402-10         | Interrupt test and control reg. failed | --             | --  |

## A.8 Video (Graphics) Error Messages (5xx-xx)

**Table A-7.**  
**Video (Graphics) Error Messages**

| <b>Message</b> | <b>Probable Cause</b>             | <b>Message</b> | <b>Probable Cause</b>                 |
|----------------|-----------------------------------|----------------|---------------------------------------|
| 501-01         | Video controller test failed      | 508-01         | 320x200 mode, color set 0 test failed |
| 502-01         | Video memory test failed          | 509-01         | 320x200 mode, color set 1 test failed |
| 503-01         | Video attribute test failed       | 510-01         | 640x200 mode test failed              |
| 504-01         | Video character set test failed   | 511-01         | Screen memory page test failed        |
| 505-01         | 80x25 mode, 9x14 cell test failed | 512-01         | Gray scale test failed                |
| 506-01         | 80x25 mode, 8x8 cell test failed  | 514-01         | White screen test failed              |
| 507-01         | 40x25 mode test failed            | 516-01         | Noise pattern test failed             |

See Table A-14 for additional video (graphics) messages.

## A.9 Diskette Drive Error Messages (6xx-xx)

**Table A-8.**  
**Diskette Drive Error Messages**

| <b>Message</b> | <b>Probable Cause</b>              | <b>Message</b> | <b>Probable Cause</b>                |
|----------------|------------------------------------|----------------|--------------------------------------|
| 6xx-01         | Exceeded maximum soft error limit  | 6xx-20         | Failed to get drive type             |
| 6xx-02         | Exceeded maximum hard error limit  | 6xx-21         | Failed to get change line status     |
| 6xx-03         | Previously exceeded max soft limit | 6xx-22         | Failed to clear change line status   |
| 6xx-04         | Previously exceeded max hard limit | 6xx-23         | Failed to set drive type in ID media |
| 6xx-05         | Failed to reset controller         | 6xx-24         | Failed to read diskette media        |
| 6xx-06         | Fatal error while reading          | 6xx-25         | Failed to verify diskette media      |
| 6xx-07         | Fatal error while writing          | 6xx-26         | Failed to read media in speed test   |
| 6xx-08         | Failed compare of R/W buffers      | 6xx-27         | Failed speed limits                  |
| 6xx-09         | Failed to format a tract           | 6xx-28         | Failed write-protect test            |
| 6xx-10         | Failed sector wrap test            | --             | --                                   |

600-xx = Diskette drive ID test

601-xx = Diskette drive format

602-xx = Diskette read test

603-xx = Diskette drive R/W compare test

604-xx = Diskette drive random seek test

605-xx = Diskette drive ID media

606-xx = Diskette drive speed test

607-xx = Diskette drive wrap test

608-xx = Diskette drive write-protect test

609-xx = Diskette drive reset controller test

610-xx = Diskette drive change line test

611-xx = Pri. diskette drive port addr. conflict

612-xx = Sec. diskette drive port addr. conflict

694-00 = Pin 34 not cut on 360-KB drive

697-00 = Diskette type error

698-00 = Drive speed not within limits

699-00 = Drive/media ID error (run Setup)

## A.10 Serial Interface Error Messages (11 xx-xx)

**Table A-9.**  
**Serial Interface Error Messages**

| <b>Message</b> | <b>Probable Cause</b>           | <b>Message</b> | <b>Probable Cause</b>                 |
|----------------|---------------------------------|----------------|---------------------------------------|
| 1101-01        | UART DLAB bit failure           | 1101-13        | UART cntrl. signal interrupt failure  |
| 1101-02        | Line input or UART fault        | 1101-14        | DRVR/RCVR data failure                |
| 1101-03        | Address line fault              | 1109-01        | Clock register initialization failure |
| 1101-04        | Data line fault                 | 1109-02        | Clock register rollover failure       |
| 1101-05        | UART cntrl. signal failure      | 1109-03        | Clock reset failure                   |
| 1101-06        | UART THRE bit failure           | 1109-04        | Input line or clock failure           |
| 1101-07        | UART Data RDY bit failure       | 1109-05        | Address line fault                    |
| 1101-08        | UART TX/RX buffer failure       | 1109-06        | Data line fault                       |
| 1101-09        | Interrupt circuit failure       | 1150-xx        | Comm port setup error (run Setup)     |
| 1101-10        | COM1 set to invalid INT         | 1151-xx        | COM1 address conflict                 |
| 1101-11        | COM2 set to invalid INT         | 1152-xx        | COM2 address conflict                 |
| 1101-12        | DRVR/RCVR cntrl. signal failure | 1155-xx        | COM port address conflict             |

## A.11 Modem Communications Error Messages (12xx-xx)

**Table A-10.**  
**Modem Communications Error Messages**

| <b>Message</b> | <b>Probable Cause</b>                 | <b>Message</b> | <b>Probable Cause</b>                        |
|----------------|---------------------------------------|----------------|--|
| 1201-XX        | Modem internal loopback test          | 1204-03        | Data block retry limit reached [4]           |
| 1201-01        | UART DLAB bit failure                 | 1204-04        | RX exceeded carrier lost limit               |
| 1201-02        | Line input or UART failure            | 1204-05        | TX exceeded carrier lost limit               |
| 1201-03        | Address line failure                  | 1204-06        | Time-out waiting for dial tone               |
| 1201-04        | Data line fault                       | 1204-07        | Dial number string too long                  |
| 1201-05        | UART control signal failure           | 1204-08        | Modem time-out waiting for remote response   |
| 1201-06        | UART THRE bit failure                 | 1204-09        | Modem exceeded maximum redial limit          |
| 1201-07        | UART DATA READY bit failure           | 1204-10        | Line quality prevented remote response       |
| 1201-08        | UART TX/RX buffer failure             | 1204-11        | Modem time-out waiting for remote connection |
| 1201-09        | Interrupt circuit failure             | 1205-XX        | Modem auto answer test                       |
| 1201-10        | COM1 set to invalid interrupt         | 1205-01        | Time-out waiting for SYNC [5]                |
| 1201-11        | COM2 set to invalid                   | 1205-02        | Time-out waiting for response [5]            |
| 1201-12        | DRVR/RCVR control signal failure      | 1205-03        | Data block retry limit reached [5]           |
| 1201-13        | UART control signal interrupt failure | 1205-04        | RX exceeded carrier lost limit               |
| 1201-14        | DRVR/RCVR data failure                | 1205-05        | TX exceeded carrier lost limit               |
| 1201-15        | Modem detection failure               | 1205-06        | Time-out waiting for dial tone               |
| 1201-16        | Modem ROM, checksum failure           | 1205-07        | Dial number string too long                  |
| 1201-17        | Tone detect failure                   | 1205-08        | Modem time-out waiting for remote response   |
| 1202-XX        | Modem internal test                   | 1205-09        | Modem exceeded maximum redial limit          |
| 1202-01        | Time-out waiting for SYNC [1]         | 1205-10        | Line quality prevented remote response       |
| 1202-02        | Time-out waiting for response [1]     | 1205-11        | Modem time-out waiting for remote connection |
| 1202-03        | Data block retry limit reached [1]    | 1206-XX        | Dial multi-frequency tone test               |
| 1202-11        | Time-out waiting for SYNC [2]         | 1206-17        | Tone detection failure                       |
| 1202-12        | Time-out waiting for response [2]     | 1210-XX        | Modem direct connect test                    |

**Table A-10. (Continued)**  
**Modem Communications Error Messages**

| <b>Message</b> | <b>Probable Cause</b>              | <b>Message</b> | <b>Probable Cause</b>                        |
|----------------|------------------------------------|----------------|--|
| 1202-13        | Data block retry limit reached [2] | 1210-01        | Time-out waiting for SYNC [6]                |
| 1202-21        | Time-out waiting for SYNC [3]      | 1210-02        | Time-out waiting for response [6]            |
| 1202-22        | Time-out waiting for response [3]  | 1210-03        | Data block retry limit reached [6]           |
| 1202-23        | Data block retry limit reached [3] | 1210-04        | RX exceeded carrier lost limit               |
| 1203-XX        | Modem external termination test    | 1210-05        | TX exceeded carrier lost limit               |
| 1203-01        | Modem external TIP/RING failure    | 1210-06        | Time-out waiting for dial tone               |
| 1203-02        | Modem external data TIP/RING fail  | 1210-07        | Dial number string too long                  |
| 1203-03        | Modem line termination failure     | 1210-08        | Modem time-out waiting for remote response   |
| 1204-XX        | Modem auto originate test          | 1210-09        | Modem exceeded maximum redial limit          |
| 1204-01        | Time-out waiting for SYNC [4]      | 1210-10        | Line quality prevented remote response       |
| 1204-02        | Time-out waiting for response [4]  | 1210-11        | Modem time-out waiting for remote connection |

## NOTES:

- |                                    |                               |
|------------------------------------|-------------------------------|
| [1] Local loopback mode            | [4] Modem auto originate test |
| [2] Analog loopback originate mode | [5] Modem auto answer test    |
| [3] Analog loopback answer mode    | [6] Modem direct connect test |

## A.12 System Status Error Messages (16xx-xx)

**Table A-11**  
**System Status Error Messages**

| <b>Message</b> | <b>Probable Cause</b> |
|----------------|-----------------------|
| 1601-xx        | Temperature violation |
| 1611-xx        | Fan failure           |

## A.13 Hard Drive Error Messages (17xx-xx)

**Table A-12**  
**Hard Drive Error Messages**

| <b>Message</b> | <b>Probable Cause</b>                     | <b>Message</b> | <b>Probable Cause</b>                  |
|----------------|---|----------------|--|
| 17xx-01        | Exceeded max. soft error limit            | 17xx-51        | Failed I/O read test                   |
| 17xx-02        | Exceeded max. Hard error limit            | 17xx-52        | Failed file I/O compare test           |
| 17xx-03        | Previously exceeded max. soft error limit | 17xx-53        | Failed drive/head register test        |
| 17xx-04        | Previously exceeded max.hard error limit  | 17xx-54        | Failed digital input register test     |
| 17xx-05        | Failed to reset controller                | 17xx-55        | Cylinder 1 error                       |
| 17xx-06        | Fatal error while reading                 | 17xx-56        | Failed controller RAM diagnostics      |
| 17xx-07        | Fatal error while writing                 | 17xx-57        | Failed controller-to-drive diagnostics |
| 17xx-08        | Failed compare of R/W buffers             | 17xx-58        | Failed to write sector buffer          |
| 17xx-09        | Failed to format a track                  | 17xx-59        | Failed to read sector buffer           |
| 17xx-10        | Failed diskette sector wrap during read   | 17xx-60        | Failed uncorrectable ECC error         |
| 17xx-19        | Cntrl. failed to deallocate bad sectors   | 17xx-62        | Failed correctable ECC error           |
| 17xx-40        | Cylinder 0 error                          | 17xx-63        | Failed soft error rate                 |
| 17xx-41        | Drive not ready                           | 17xx-65        | Exceeded max. bad sectors per track    |
| 17xx-42        | Failed to recalibrate drive               | 17xx-66        | Failed to initialize drive parameter   |
| 17xx-43        | Failed to format a bad track              | 17xx-67        | Failed to write long                   |
| 17xx-44        | Failed controller diagnostics             | 17xx-68        | Failed to read long                    |
| 17xx-45        | Failed to get drive parameters from ROM   | 17xx-69        | Failed to read drive size              |
| 17xx-46        | Invalid drive parameters from ROM         | 17xx-70        | Failed translate mode                  |
| 17xx-47        | Failed to park heads                      | 17xx-71        | Failed non-translate mode              |
| 17xx-48        | Failed to move hard drive table to RAM    | 17xx-72        | Bad track limit exceeded               |
| 17xx-49        | Failed to read media in file write test   | 17xx-73        | Previously exceeded bad track limit    |
| 17xx-50        | Failed I/O write test                     | --             | --                                     |

NOTE:

|   |   |
|---|---|
| xx = 00, Hard drive ID test                 | xx = 19, Hard drive power mode test           |
| xx = 01, Hard drive format test             | xx = 20, SMART drive detects imminent failure |
| xx = 02, Hard drive read test               | xx = 21, SCSI hard drive imminent failure     |
| xx = 03, Hard drive read/write compare test | xx = 24, Network preparation test             |
| xx = 04, Hard drive random seek test        | xx = 36, Drive monitoring test                |
| xx = 05, Hard drive controller test         | xx = 71, Pri. IDE controller address conflict |
| xx = 06, Hard drive ready test              | xx = 72, Sec. IDE controller address conflict |
| xx = 07, Hard drive recalibrate test        | xx = 80, Disk 0 failure                       |
| xx = 08, Hard drive format bad track test   | xx = 81, Disk 1 failure                       |
| xx = 09, Hard drive reset controller test   | xx = 82, Pri. IDE controller failure          |
| xx = 10, Hard drive park head test          | xx = 90, Disk 0 failure                       |
| xx = 14, Hard drive file write test         | xx = 91, Disk 1 failure                       |
| xx = 15, Hard drive head select test        | xx = 92, Sec. controller failure              |
| xx = 16, Hard drive conditional format test | xx = 93, Sec. Controller or disk failure      |
| xx = 17, Hard drive ECC test                | xx = 99, Invalid hard drive type              |



## A.14 Hard Drive Error Messages (19xx-xx)

**Table A-13**  
**Hard Drive Error Messages**

| <b>Message</b> | <b>Probable Cause</b>         | <b>Message</b> | <b>Probable Cause</b>                      |
|----------------|-------------------------------|----------------|--|
| 19xx-01        | Drive not installed           | 19xx-21        | Got servo pulses second time but not first |
| 19xx-02        | Cartridge not installed       | 19xx-22        | Never got to EOT after servo check         |
| 19xx-03        | Tape motion error             | 19xx-23        | Change line unset                          |
| 19xx-04        | Drive busy error              | 19xx-24        | Write-protect error                        |
| 19xx-05        | Track seek error              | 19xx-25        | Unable to erase cartridge                  |
| 19xx-06        | Tape write-protect error      | 19xx-26        | Cannot identify drive                      |
| 19xx-07        | Tape already Servo Written    | 19xx-27        | Drive not compatible with controller       |
| 19xx-08        | Unable to Servo Write         | 19xx-28        | Format gap error                           |
| 19xx-09        | Unable to format              | 19xx-30        | Exception bit not set                      |
| 19xx-10        | Format mode error             | 19xx-31        | Unexpected drive status                    |
| 19xx-11        | Drive recalibration error     | 19xx-32        | Device fault                               |
| 19xx-12        | Tape not Servo Written        | 19xx-33        | Illegal command                            |
| 19xx-13        | Tape not formatted            | 19xx-34        | No data detected                           |
| 19xx-14        | Drive time-out error          | 19xx-35        | Power-on reset occurred                    |
| 19xx-15        | Sensor error flag             | 19xx-36        | Failed to set FLEX format mode             |
| 19xx-16        | Block locate (block ID) error | 19xx-37        | Failed to reset FLEX format mode           |
| 19xx-17        | Soft error limit exceeded     | 19xx-38        | Data mismatch on directory track           |
| 19xx-18        | Hard error limit exceeded     | 19xx-39        | Data mismatch on track 0                   |
| 19xx-19        | Write (probably ID ) error    | 19xx-40        | Failed self-test                           |
| 19xx-20        | NEC fatal error               | 19xx-91        | Power lost during test                     |

1900-xx = Tape ID test failed  
 1901-xx = Tape servo write failed  
 1902-xx = Tape format failed  
 1903-xx = Tape drive sensor test failed

1904-xx = Tape BOT/EOT test failed  
 1905-xx = Tape read test failed  
 1906-xx = Tape R/W compare test failed  
 1907-xx = Tape write-protect failed

## A.15 Video (Graphics) Error Messages (24xx-xx)

**Table A-14**  
**Video (Graphics) Error Messages**

| <b>Message</b> | <b>Probable Cause</b>                       | <b>Message</b> | <b>Probable Cause</b>               |
|----------------|---|----------------|-------------------------------------|
| 2402-01        | Video memory test failed                    | 2418-02        | EGA shadow RAM test failed          |
| 2403-01        | Video attribute test failed                 | 2419-01        | EGA ROM checksum test failed        |
| 2404-01        | Video character set test failed             | 2420-01        | EGA attribute test failed           |
| 2405-01        | 80x25 mode, 9x14 cell test failed           | 2421-01        | 640x200 mode test failed            |
| 2406-01        | 80x25 mode, 8x8 cell test failed            | 2422-01        | 640x350 16-color set test failed    |
| 2407-01        | 40x25 mode test failed                      | 2423-01        | 640x350 64-color set test failed    |
| 2408-01        | 320x200 mode color set 0 test failed        | 2424-01        | EGA Mono. text mode test failed     |
| 2409-01        | 320x200 mode color set 1 test failed        | 2425-01        | EGA Mono. graphics mode test failed |
| 2410-01        | 640x200 mode test failed                    | 2431-01        | 640x480 graphics mode test failed   |
| 2411-01        | Screen memory page test failed              | 2432-01        | 320x200 256-color set test failed   |
| 2412-01        | Gray scale test failed                      | 2448-01        | Advanced VGA controller test failed |
| 2414-01        | White screen test failed                    | 2451-01        | 132-column AVGA test failed         |
| 2416-01        | Noise pattern test failed                   | 2456-01        | AVGA 256-color test failed          |
| 2417-01        | Lightpen text test failed, no response      | 2458-xx        | AVGA BitBLT test failed             |
| 2417-02        | Lightpen text test failed, invalid response | 2468-xx        | AVGA DAC test failed                |
| 2417-03        | Lightpen graphics test failed, no resp.     | 2477-xx        | AVGA data path test failed          |
| 2417-04        | Lightpen graphics tst failed, invalid resp. | 2478-xx        | AVGA BitBLT test failed             |
| 2418-01        | EGA memory test failed                      | 2480-xx        | AVGA linedraw test failed           |

## A.16 Audio Error Messages (3206-xx)

**Table A-15**  
**Audio Error Messages**

| <b>Message</b> | <b>Probable Cause</b>          |
|----------------|--------------------------------|
| 3206-xx        | Audio subsystem internal error |

## A.17 DVD/CD-ROM Error Messages (33xx-xx)

**Table A-16**  
**DVD/CD-ROM Error Messages**

| <b>Message</b> | <b>Probable Cause</b> |
|----------------|-----------------------|
| 3301-xx        | Drive test failed     |
| 3305-xx        | Seek test failed      |

## A.18 Network Interface Error Messages (60xx-xx)

**Table A-17**  
**Network Interface Error Messages**

| <b>Message</b> | <b>Probable Cause</b>              | <b>Message</b> | <b>Probable Cause</b>                |
|----------------|------------------------------------|----------------|--------------------------------------|
| 6000-xx        | Pointing device interface error    | 6054-xx        | Token ring configuration test failed |
| 6014-xx        | Ethernet configuration test failed | 6056-xx        | Token ring reset test failed         |
| 6016-xx        | Ethernet reset test failed         | 6068-xx        | Token ring int. loopback test failed |
| 6028-xx        | Ethernet int. loopback test failed | 6069-xx        | Token ring ext. loopback test failed |
| 6029-xx        | Ethernet ext. loopback test failed | 6089-xx        | Token ring open                      |

## A.19 SCSI Interface Error Messages (65xx-xx, 66xx-xx, 67xx-xx)

**Table A-18**  
**SCSI Interface Error Messages**

| <b>Message</b> | <b>Probable Cause</b>          | <b>Message</b> | <b>Probable Cause</b>                        |
|----------------|--------------------------------|----------------|--|
| 6nyy-02        | Drive not installed            | 6nyy-33        | Illegal controller command                   |
| 6nyy-03        | Media not installed            | 6nyy-34        | Invalid SCSI bus phase                       |
| 6nyy-05        | Seek failure                   | 6nyy-35        | Invalid SCSI bus phase                       |
| 6nyy-06        | Drive timed out                | 6nyy-36        | Invalid SCSI bus phase                       |
| 6nyy-07        | Drive busy                     | 6nyy-39        | Error status from drive                      |
| 6nyy-08        | Drive already reserved         | 6nyy-40        | Drive timed out                              |
| 6nyy-09        | Reserved                       | 6nyy-41        | SSI bus stayed busy                          |
| 6nyy-10        | Reserved                       | 6nyy-42        | ACK/REQ lines bad                            |
| 6nyy-11        | Media soft error               | 6nyy-43        | ACK did not deassert                         |
| 6nyy-12        | Drive not ready                | 6nyy-44        | Parity error                                 |
| 6nyy-13        | Media error                    | 6nyy-50        | Data pins bad                                |
| 6nyy-14        | Drive hardware error           | 6nyy-51        | Data line 7 bad                              |
| 6nyy-15        | Illegal drive command          | 6nyy-52        | MSG, C/D, or I/O lines bad                   |
| 6nyy-16        | Media was changed              | 6nyy-53        | BSY never went busy                          |
| 6nyy-17        | Tape write-protected           | 6nyy-54        | BSY stayed busy                              |
| 6nyy-18        | No data detected               | 6nyy-60        | Controller CONFIG-1 register fault           |
| 6nyy-21        | Drive command aborted          | 6nyy-61        | Controller CONFIG-2 register fault           |
| 6nyy-24        | Media hard error               | 6nyy-65        | Media not unloaded                           |
| 6nyy-25        | Reserved                       | 6nyy-90        | Fan failure                                  |
| 6nyy-30        | Controller timed out           | 6nyy-91        | Over temperature condition                   |
| 6nyy-31        | Unrecoverable error            | 6nyy-92        | Side panel not installed                     |
| 6nyy-32        | Controller/drive not connected | 6nyy-99        | Autoloader reported tape not loaded properly |

n = 5, Hard drive  
 = 6, CD-ROM drive  
 = 7, Tape drive

yy = 00, ID  
 = 03, Power check  
 = 05, Read  
 = 06, SA/Media  
 = 08, Controller  
 = 23, Random read  
 = 28, Media load/unload

## A.20 Pointing Device Interface Error Messages (8601-xx)

**Table A-19**  
**Pointing Device Interface Error Messages**

| <b>Message</b> | <b>Probable Cause</b>              | <b>Message</b> | <b>Probable Cause</b>          |
|----------------|------------------------------------|----------------|--------------------------------|
| 8601-01        | Mouse ID fails                     | 8601-07        | Right block not selected       |
| 8601-02        | Left mouse button is inoperative   | 8601-08        | Timeout occurred               |
| 8601-03        | Left mouse button is stuck closed  | 8601-09        | Mouse loopback test failed     |
| 8601-04        | Right mouse button is inoperative  | 8601-10        | Pointing device is inoperative |
| 8601-05        | Right mouse button is stuck closed | 8602-xx        | I/F test failed                |
| 8601-06        | Left block not selected            | --             | --                             |



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